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Concept of a SOT-MRAM based on 1Transistor-1MTJ-Cell Structure

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Abstract

We propose a concept of in-plane spin orbit torque magnetic random access memory (SOT-MRAM) based on a 1Transistor-1MTJ cell with different paths for read and write operations. By performing extensive micromagnetic modeling our concept has been verified.

1. Introduction

New types of spin-based memory utilizing all-electrical magnetization manipulation by current have been intensely developed based on MgO magnetic tunnel junctions (MTJs). Depending on the current paths for read and write operations, memory can be classified in two categories: (i) with the same path (1Transistor-1MTJ cell) or (ii) with different paths (2Transistors-1MTJ cell) for read and write operations. The two main shortcomings of the first category of devices are reliability and endurance: indeed, (i) the high write current density can occasionally damage the MTJ barrier and (ii) it remains a challenge to guarantee reliable reading without ever causing switching [1]. These shortcomings do not exist in the devices of the second category; however, they require more space and thus cause lower area density due to the second transistor needed for writing [1, 2].

In this work we propose a concept of an in-plane SOT-MRAM based on a 1Transistor-1MTJ cell with different paths for read and write operations.

2. Concept Description

Fig.1 (top) shows the investigated structures for which the write operation is based on two consecutive orthogonal sub-nanosecond in-plane current pulses. The switching is governed by the torques generated by the spin-Hall effect (SHE). The first pulse is necessary for tilting the magnetization of the free layer from its stable state and creating a small initial angle. The second pulse is used for switching the free layer to a new state.

To prove the efficiency of the proposed structure it is necessary to show the absence of switching in the case of using only one from the two pulses, as it is an unwanted event and leads to the loss of information in half-selected cell at the cross-point architecture (Fig.1, bottom).

3. Results and Discussion

Our analyses are based on the magnetization dynamics described by the Landau-Lifschitz-Gilbert (LLG) equation, including the additional SHE term [3].

In all our simulations the first pulse width ranges from 0.01 to 0.1ns. These ranges of pulse widths are not sufficient to tilt the magnetization from the initial state by an angle sufficient to switch the free layer. Thereby, we examine the switching by two schemes (Fig.1, middle), the “write pulse 2” (Type I) and the “two write pulses” (Type II) scheme. As expected, the switching occurs in both cases (Fig.2). But for the “two write pulses” scheme the small initial angle provided by the first pulse leads to a reduction of the second pulse duration required for switching the free layer to a new state. As our simulations show (Fig.3), the switching probability for the proposed “two write pulses” scheme is 1, when the second pulse width ranges from 2.63 to 5.5ns (depending on the first pulse width). These pulse durations are shorter than the respective value of 6ns required to achieve the non-zero switching probability, when the “write pulse 2” scheme is used. This excludes unwanted switching in half-selected cells (for a current of 10μA).

Our simulations show, that in the case of using the “write pulse 2” scheme, the increase of the current leads to a drastic reduction of the switching time (Fig.4). Therefore, we also investigated the influence of the pulse width and the current value on the switching occurrence for the “two write pulses” scheme. Our results indicate that increasing the current value shifts the area where the switching is observed towards the region with lower pulse widths (Fig.5) and also leads to a reduced dependence of the switching time on the first pulse width (Fig.6). To note, increasing the current value to 40μA accelerates switching under half a nanosecond (Fig.6 and Fig.7, left) while still preserving half-selected cells from unwanted switching (Fig.7, right).

4. Conclusions

We propose a new concept of SOT-MRAM based on a 1Transistor-1MTJ cell with different paths for read and write operations. Our analysis of the proposed structures shows a wide range of currents and write pulses’ widths which do not lead to switching in half-selected cells.

Acknowledgements

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References

[1] G. Prenat *et al.*, Spintronics-based Computing (2015) 145-157.
[2] D. Suzuki *et al.*, Jpn. J. Appl. Phys. **54** (2015) 04DE01.
[3] A. Giordano *et al.*, Appl. Phys. Lett. **105** (2014) 042412.

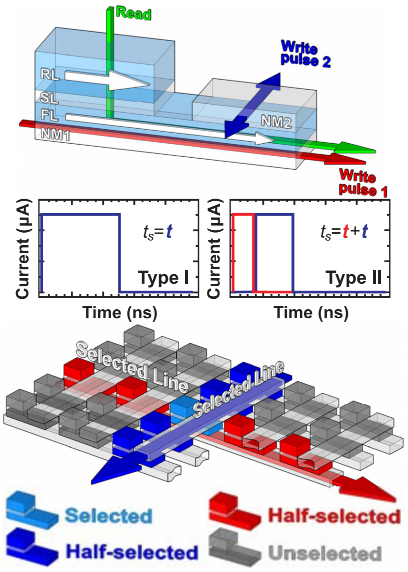

Fig. 1. Schematic illustration of (top) proposed SOT-MRAM; (middle) “write pulse 2” (Type I) and “two write pulses” (Type II) schemes; (bottom) memory array.

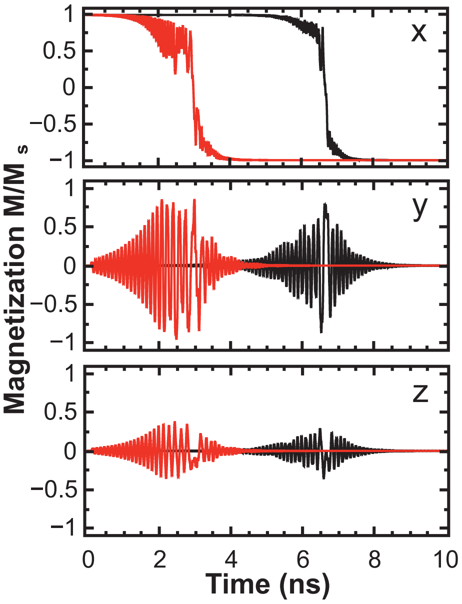

Fig. 2. Magnetization components as a function of time: (top) *x*-component; (middle) *y*-component; (bottom) *z*-component. The current is 10μA. The "two write pulses" scheme is shown in red and the "write pulse 2" scheme is shown in black.

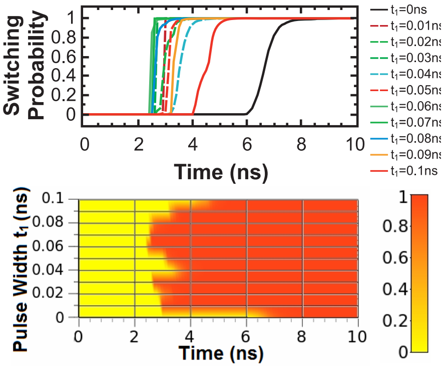

Fig. 3. Switching probability for the “two write pulses” scheme as a function of the time for different values of pulse width t_1. For switching probability estimation, 250 simulations of switching were performed on each pulse width t_1.

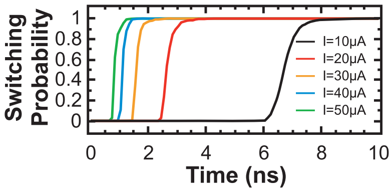

Fig. 4. Switching probability for the “write pulse 2” scheme as a function of the pulse duration for five current values. For switching probability estimation, 250 simulations of switching were performed on each current value.

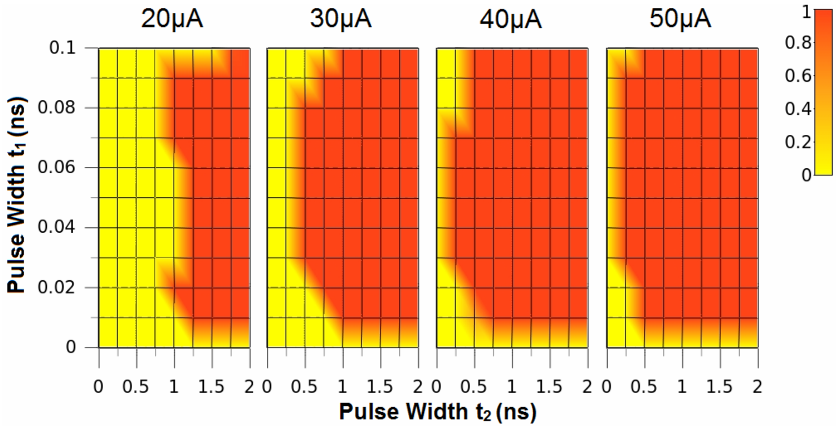

Fig. 5. Schematic illustration of the dependence of the switching probability for the “two write pulses” scheme on the current and pulses width. The dependencies are shown for four current values: 20μA, 30μA 40μA, 50μA. For switching probability estimation, 100 simulations of switching were performed on each combination of pulses’ widths.

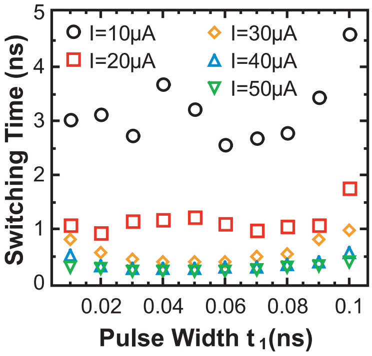

Fig. 6. Switching time for the “two write pulses” scheme as a function of the pulse width t_1 for five current values.

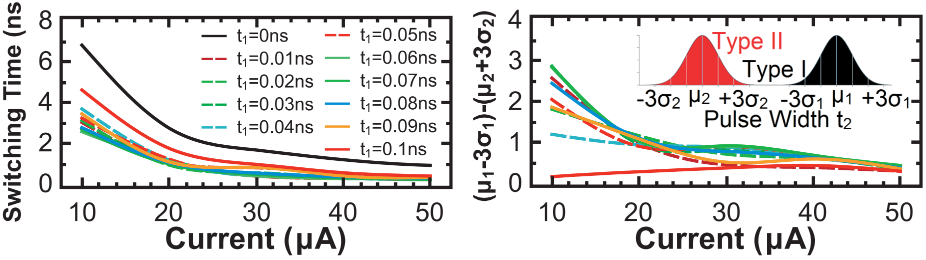

Fig. 7. (left) Switching time as a function of current. (right) The difference between the minimum value of the pulse width t_2 required to achieve a non-zero probability of switching by using the "write pulse 2" scheme (μ_1-3σ_1) and a value of the pulse width t_2 needed to achieve guaranteed switching with the "two write pulses" scheme (μ_2+3σ_2) as a function of current.