Title: Spin-Driven Applications of Silicon and CMOS-Compatible Devices

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Abstract

Silicon, the main material of microelectronics, is now gaining momentum to be used in electronic applications involving spin. Recently, all-electrical spin injection and propagation at room temperature in lightly- and heavily-doped silicon has been successfully demonstrated. However, the several orders of magnitude larger than expected amplitude of the spin accumulation signal obtained within the three-terminal method is still under intense discussion. Silicon is a perfect material for spin-driven applications due to the weak strength of the spin-orbit interaction in the conduction band and is predominantly composed of non-magnetic atoms, which results in a long electron spin diffusion length even at room temperature. In silicon-on-insulator and fin-based structures additional spin relaxation due to surface roughness and phonons causes spin lifetime shortening, by analogy to the mobility degradation in ultra-thin silicon body MOSFETs. However, in contrast to the momentum relaxation determined by intra-valley scattering, the spin relaxation is determined by intra-valley transitions. In (001)-oriented ultrathin films the valley degeneracy is partly lifted, so the main spin-flip processes defining the spin relaxation are the g-type transitions between the two low-energy valleys along the same [001] direction. The remaining degeneracy is lifted due to the valley-orbit interaction which can be greatly enhanced by applying uniaxial [110] stress. This suppresses the most efficient spin-flips due to inter-valley scattering which results in a giant, almost exponential with shear strain, spin lifetime enhancement. Therefore, mechanical stress routinely applied now to enhance the electron mobility can also be used to boost the spin lifetime. This makes strained silicon thin films and nanowires strong candidates for spin interconnects in all-spin logic devices and circuits.
The weak spin-orbit interaction in the conduction band of silicon renders the all-electrical spin manipulation by means of Rashba-type electric field dependent spin-orbit fields inefficient. A lack of an efficient way to couple spins with the electric field makes the realization of silicon-based SpinFETs improbable in a near future, and the search for an all-electric way to manipulate spins in silicon must be continued. An efficient coupling between the electrical and the magnetic degrees of freedom is achieved in magnetic tunnel junctions at the quantum-mechanical level. This makes magnetic memory cells with all-electrical switching, STT-MRAM, a viable candidate for future universal memory, which is fast, nonvolatile, and CMOS compatible. While the first MRAM arrays are already commercially available, the reduction of the switching current, while preserving the high thermal stability barrier, is the main challenge in the area. A composite structure of the recording layer helps reducing the critical current density without compromising the thermal stability in MRAM cells with in-plane magnetization orientation. Finally, an example of implementation for an STT-MRAM based intrinsic logic-in-memory architecture, where the same elements are employed to store and to process information, is discussed. Indeed, an implication logic gate can be built by using any of two MRAM cells, which opens the way to store and to process the data on the same elements.
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Biography

Dr. Viktor Sverdlov received his Master of Science and PhD degrees in physics from the State University of St.Petersburg, Russia, in 1985 and 1989, respectively. From 1989 to 1999 he worked as a staff research scientist at the V.A.Fock Institute of Physics, St.Petersburg State University. During this time, he visited ICTP (Italy, 1993), the University of Geneva (Switzerland, 1993-1994), the University of Oulu (Finland, 1995), the Helsinki University of Technology (Finland, 1996, 1998), the Free University of Berlin (Germany, 1997), and NORDITA (Denmark, 1998). In 1999 he became a staff research scientist at the State University of New York at Stony Brook. He joined the Institute for Microelectronics, Technische Universität Wien, in 2004. In May 2011 he received the Venia Docendi in microelectronics. His scientific interests include device simulations, computational physics, solid-state physics, and nanoelectronics.