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The role of cold carriers and the multiple-carrier process of Si–H bond dissociation for hot-carrier degradation in n- and p-channel LDMOS devices

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ABSTRACT

We apply our hot-carrier degradation (HCD) model, which uses the information about the carrier energy distribution, to represent HCD data measured in n- and p-channel LDMOS transistors. In the first version of our model we use the spherical harmonics expansion approach to solve the Boltzmann transport equation (BTE), while in the second version we employ the drift–diffusion scheme. In the latter case the carrier energy distribution function is approximated by an analytic expression with parameters found using the drift–diffusion scheme. The model, which has already been verified with nLDMOS transistors, is used to represent the carrier distribution functions, interface state density profiles, and changes of the drain currents vs. stress time in pLDMOS transistor. Particular attention is paid to study the role of the cold fraction of the carrier ensemble. We check the validity of the model by neglecting the effect of cold carriers in HCD modeling in the case of nLDMOS devices stressed at high voltages. In our model, cold carriers are represented by the corresponding term in the analytic formula for the carrier distribution function as well as by the multiple-carrier process of the Si–H bond dissociation. We show that even in high-voltage devices stressed at high drain voltages the thermalized carriers still have a substantial contribution to HCD.
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1. Introduction

Hot-carrier degradation (HCD) is a very complex phenomenon which includes several elements: the microscopic mechanisms of defect generation, carrier transport treatment and the modeling of the degraded devices [1–4]. All these elements are coupled and have to be treated within the same simulation framework. For instance, the traps at the Si/SiO_2 interface are generated due to depassivation of the electrically inactive Si–H bonds. There are two competing modes responsible for the generation of these defects: the single-carrier (SC) and the multiple-carrier (MC) processes [5–7]. The first process is related to a solitary high-energetic particle which can induce a bond-breakage event in a single collision, while the second one is triggered by a series of colder carriers which subsequently bombard the bond, excite it and eventually break it. The resultant electrically active dangling bonds affect the device performance, i.e. they contribute to the electrostatic disturbance of the device and lead to the degradation of the drain current, threshold voltage, transconductance, on resistance, etc.

The SC-process is assumed to be the dominant HCD mechanism in MOSFETs stressed at high voltages, while the MC-process is more typical for scaled devices stressed at lower voltages. However, it was recently shown that the MC degradation mode can result in a significant contribution also in high-voltage devices with channel lengths up to 2 μm [2,4,8], while the SC-process can be important even in decananometer MOSFETs [4,8,9]. Therefore, in order to properly represent the contributions of these processes one needs be able to distinguish between cold and hot carriers. This information is contained in the carrier energy distribution function (DF) which can be obtained as a solution of the Boltzmann transport equation (BTE). There are two main strategies to achieve such a solution: the stochastic Monte-Carlo method [10,11] and deterministic methods which are based on a representation of the carrier DF by a spherical harmonics expansion [12–14]. Both methods are

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computationally quite challenging even for ultra-scaled planar MOSFETs. For high-voltage devices, which typically have non-planar interfaces and geometrical features (bird's beak, shallow trench isolation, etc.), the computational burden increases dramatically.

As a result, simplified techniques to obtain the BTE solution appear very attractive. These techniques are often based on the moments of the Boltzmann transport equation [15,16]. The most popular among them are the drift–diffusion (DD) and energy transport schemes. We have previously shown that these methods cannot properly describe HCD in planar nMOSFETs with relatively short channel lengths [17]. However, these models can be applicable for the description of HCD in LDMOS transistors which have larger dimensions. It appears reasonable to combine them with some analytic expression used to represent the carrier DF with the parameters linked to the moments of BTE. Some commonly used analytic approximations are the heated Maxwellian, a polynomial in the exponential [18], models developed by Cassi et al. [19], Hasnat and co-authors [20], Reggiani et al. [21,22], etc. However, in this work we used our model proposed in [23].

The LDMOS transistor is a very important device for industrial applications such as mixed-signal integrated circuits and high-voltage automotive. Unfortunately, a proper treatment of carrier transport in LDMOS devices is problematic. First, due to the large dimensions of these devices as compared to nanoscale CMOS transistors, the simulation mesh contains a large number of elements. Second, this transistor usually has a the bird's beak/STI corner and curved interfaces, see Fig. 1, and also high doping gradients in various regions. Finally, LDMOS transistors are usually operated/stressed at high voltages.

As a consequence of the high voltages, a promising strategy of hot-carrier degradation modeling in LDMOS devices would be to neglect the effect of cold carriers and their contribution to the entire damage. In practice, however, both single- and multiple-carrier processes of bond rupture appear to play important roles also under these stress conditions and neglecting one of them leads to a substantial underestimation of HCD [24].

In this paper we analyze the contribution of cold carriers to hot-carrier degradation using our DD-based HCD model derived from our HCD model which relies on the full BTE solution [23]. This DD-based model mimics the DF simulated by the spherical harmonics expansion method by using an analytic expression. The effect of cold carriers in our HCD model is twofold: a cold carrier term in the energy distribution function and the multiple-carrier process of Si–H bond dissociation. We analyze the importance of each of them. Finally, we check the capabilities of our model to comprehend the HCD in pLDMOS devices as well.

2. Experiment and simulation framework

The n- and p-LDMOS transistors (sketched in Fig. 1) designed in 0.35 μm and 0.18 μm standard CMOS processes have been subjected to hot-carrier stress at different combinations of gate and drain voltages V_{gs} and V_{ds}. The n-channel devices have a Si/SiO_2 interface length of ∼3.4 μm, and a gate length of ∼2.5 μm, while the p-channel devices have an interface length of ∼4.4 μm, and a gate length of ∼3.3 μm.

The nLDMOS transistors were subjected to hot-carrier stress with three different combinations of drain and gate voltages V_{ds}, V_{gs} (i.e. at V_{gs} = 2.0 V and V_{ds} = 18, 20, 22 V) at room temperature for stress times up to ∼1 Ms. The pLDMOS devices, on the other hand, were stressed at V_{ds} = −50 V and V_{gs} = −1.5, −1.7 V for stress times up to ∼40 ks. To monitor HCD, the normalized changes in the linear drain current $\Delta I_{d,lin}$ (measured at V_{ds} = 0.1 V and V_{gs} = 3.6 V) and the saturation drain current $\Delta I_{d,sat}$ (at V_{ds} = 10 V and V_{gs} = 3.6 V) were recorded as a function of stress time for nLDMOS devices. For pLDMOS, we monitor the $\Delta I_{d,sat}$ at V_{ds} = −50 V and V_{gs} = −2.5 V. These relative drifts in the currents at any time t are defined as:

$$\Delta I_{d,sat/lin}(t) = \frac{I_{d,sat/lin}(t) - I_{d,sat/lin}(0)}{I_{d,sat/lin}(0)} \quad (1)$$

For simulations, we generated the device structure using the Sentaurus Process simulator [25], while MINIMOS-NT [26] was used for device simulations. Simulation of such large LDMOS devices which are stressed/operated at high voltages requires a proper mesh which provides good resolution at the important regions of the device and also keeps the total number of mesh points to a moderate amount. For this purpose, we used the highly adaptive meshing framework ViennaMesh [27,28] as it generates meshes based on the built-in potential, see Fig. 1.

3. Model details

Both versions of our HCD model consolidate three main modules: evaluation of the carrier energy distribution function, computation of the defect generation rates and interface state densities

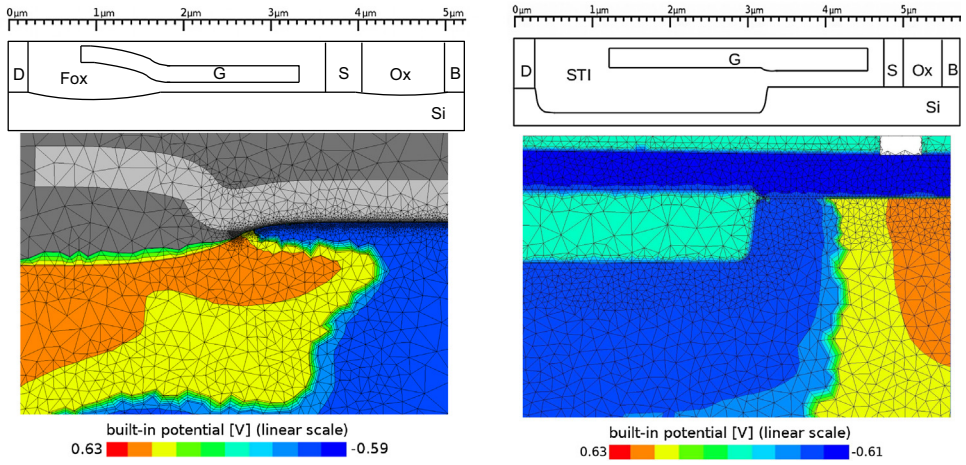

Fig. 1. Upper panel: sketch of n-LDMOS and p-LDMOS transistors with all the segments marked: D – drain, S – source, Ox – oxide, Fox – field oxide, G – gate, B – bulk contact. Lower panel: the adaptive mesh for a near interface device section with the built-in potential represented by the color map. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

for each coordinate at the Si/SiO_2 interface for each stress time step, and finally the simulation of the degraded device. The two versions differ only in the manner the carrier DFs are obtained. The "full" version is implemented into our deterministic BTE solver ViennaSHE [4,8,9,29], while the drift–diffusion based version employs our device and circuit simulator MINIMOS-NT [26] within the GTS framework [30]. We model the Si–H bond depassivation process using the carrier energy distribution function and considering all possible superpositions of the SC- and MC-mechanisms with the corresponding rates determined by the carrier DF.

3.1. Carrier transport

The carrier energy distribution function obtained from the carrier transport is the main ingredient of our HCD model. The HCD model has been implemented into our deterministic BTE solver ViennaSHE [4,8,9,29]. The DFs simulated with ViennaSHE are used as a benchmark for our DD-based approach. In the latter approach the DF is calculated using our previously suggested approach [31]

$$f(\varepsilon) = A\exp\left[-\left(\frac{\varepsilon}{\varepsilon_{\mathrm{ref}}}\right)^{b}\right] + C\exp\left[-\frac{\varepsilon}{k_{\mathrm{B}}T_{\mathrm{L}}}\right]. \quad (2)$$

This expression contains two terms: the first one represents the hot carrier fraction in the carrier ensemble, while the second, Maxwellian term, corresponds to the pool of thermalized (cold) carriers. The parameters of the DF are found using the information on the available moments of the Boltzmann transport equation and DF normalization [23]. For the density of states, we use the generalized expression proposed in [15].

The carrier DF obtained from the above technique can represent carriers in thermal equilibrium as well as the non-equilibrium ones. For the nLDMOS device, the carrier DF have a Maxwellian rudiment visible at low energies in the drain region, the DF calculated for the bird's beak do not have such a rudiment. In all cases the carrier DFs have long high-energy tails and can be represented by (2)[23].

3.2. Defect generation kinetics

Our HCD model considers self-consistently the single- and multiple-carrier bond-breakage mechanisms as two competing pathways of the same reaction which converts electrically passive Si–H bond to active interface traps. The activation energy for this reaction can be reduced by the interaction of the bond dipole moment with the electric field [4,8,9]. This energy also varies due to the structural disorder at the Si/SiO_2 interface and is modeled as a normal distribution.

In the case of both SC- and MC-mechanisms, the corresponding rates are determined by the carrier acceleration integral:

$$I_{\mathrm{SC/MC}} = \int_0^{\infty} f(\varepsilon)g(\varepsilon)v(\varepsilon)\sigma_0(\varepsilon-\varepsilon_{th})^p d\varepsilon, \quad (3)$$

with $f(\varepsilon)$ is the DF, $g(\varepsilon)$ the density of states, $v(\varepsilon)$ the carrier group velocity, and $\sigma(\varepsilon)$ the reaction cross section [4,8,9]. A self-consistent consideration of the SC- and MC-processes means that first the bond can be excited by a series of cold carriers to a certain intermediate state and then dissociated by a solitary hot carrier which induces hydrogen release to the transport state [5,8,32–34]. Note that in the case of a preheated bond the potential barrier which separates the bond and transport state is reduced and the probability of finding a carrier which brings a bond-breakage portion of energy is higher [4,8,9]. The solution of the rate equation set that describes the kinetics of the Si–H bond leads to an analytic expression for the interface state density N_{it} as described in [8]. These $N_{\mathrm{it}}(x)$ profiles are used by our device simulator MINIMOS-NT to generate the characteristics of the degraded device such as $\Delta I_{\mathrm{d,lin}}$ and $\Delta I_{\mathrm{d,sat}}$.

4. Results and discussion

The validity of our model for the nLDMOS devices has already been proven in [23]. Our DD-based model is not only able to represent the DFs at the source and channel regions in nLDMOS transistor where the DFs are not severely perturbed from equilibrium but also the agreement between the non-equilibrium DFs obtained with the SHE and DD-based methods is quite good. Hence, the $\Delta I_{\mathrm{d,lin}}(t)$ and $\Delta I_{\mathrm{d,sat}}(t)$ curves simulated with both approaches are similar and agree with the measurement data for the entire experimental time window. It is important to emphasize that the DD-based version does not require substantial computational resources and has good accuracy. This makes the DD-based HCD model very attractive for predictive HCD simulations in nLDMOS transistors.

In order to study if the effect of cold carriers can be neglected at such high voltages as $V_{\mathrm{ds}} \geqslant 16$ V we have calculated the $N_{\mathrm{it}}(x)$ profiles without the contribution of the SC-mechanism, see Fig. 2. One can see that the channel N_{it} peak disappears if the MC-process is ignored. This behavior can be easily explained because carriers near the source are in equilibrium, and therefore the electrons near the channel N_{it} peak are characterized by moderate energies which are not enough to trigger the SC-mechanisms.

The important issue which needs to be addressed in more detail is whether the effect of cold carriers can be neglected in nLDMOS devices stressed at high voltages. This effect is twofold: the population of cold carriers is described by the second term of the energy distribution function (see (2)) and these low-energetic particles contribute to HCD via the MC-mechanism. To analyze the role of the first aspect we have plotted the drain DFs obtained with ViennaSHE and with the DD-based model, excluding the term for cold carriers in the DF, for two different drain voltages of 20 and 22 V, see Fig. 3. One can see that at moderate and high energies the agreement is very good while for low energies the Maxwellian rudiments visible in SHE-based DFs are not represented by DD-based method.

To check if this omission in the DFs at low energies translates into changes in the linear and saturation drain current degradation, we have plotted $\Delta I_{\mathrm{d,lin}}(t)$ and $\Delta I_{\mathrm{d,sat}}(t)$ curves calculated without the effect of cold carriers for $V_{\mathrm{gs}} = 2$ V and $V_{\mathrm{ds}} = 18$ and 22 V, Figs. 4 and 5. These degradation curves are evaluated using the same

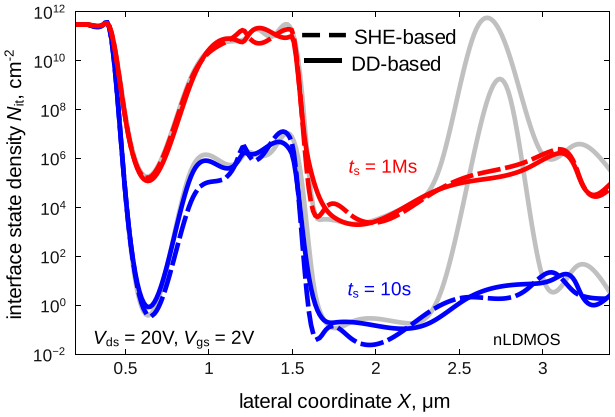

Fig. 2. Interface state density profiles obtained with SHE- and DD-based models, for the nLDMOS transistor, without the effect of MC-process. The stress voltages are $V_{\mathrm{ds}} = 20$ and $V_{\mathrm{gs}} = 2$ V applied for stress times 10 s and 1 Ms. The case where all the superpositions of SC- and MC-processes are considered in the DD-based model are also plotted for comparison (gray lines).

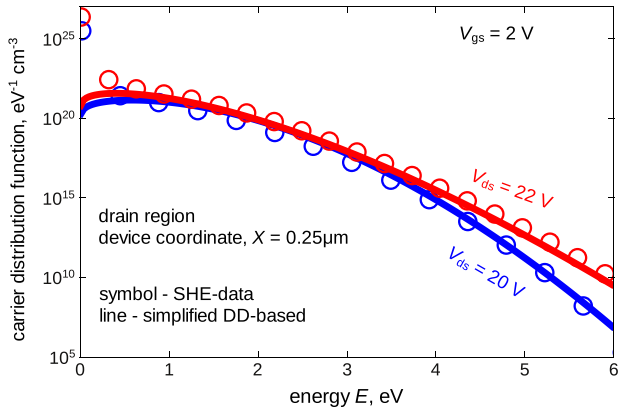

Fig. 3. DFs for the nLDMOS transistor from ViennaSHE and the DD-based approach without the term for cold carriers in (2), for stress voltages: V_{gs} = 2 V, V_{ds} = 20 V and 22 V.

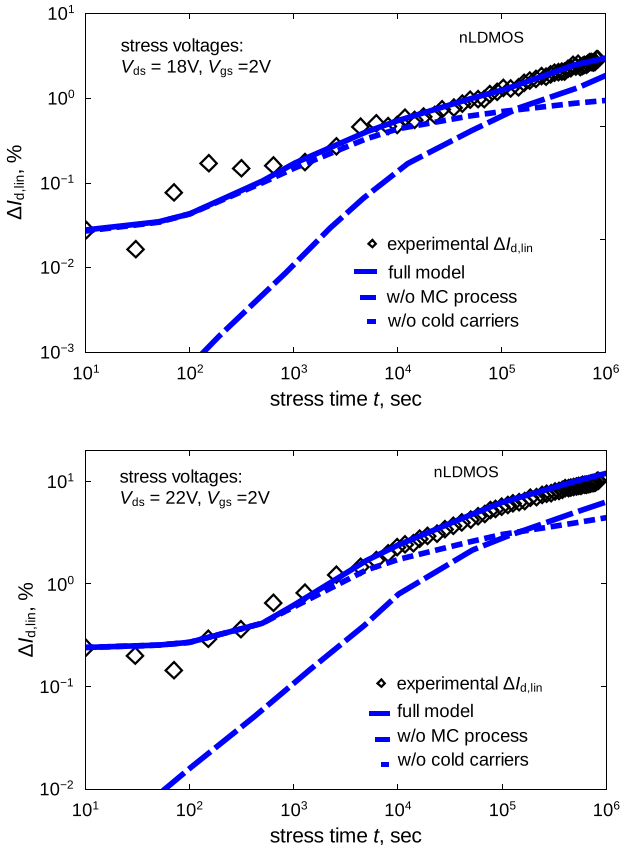

Fig. 4. The change of the linear drain current $\Delta I_{d,lin}$ as a function of stress time: experimental data, the results of the full model, and the traces obtained neglecting the cold carrier term in (2) and without the MC process. The stress voltages were V_{gs} = 2 V and V_{ds} = 18 and 20 V.

parameter set as those obtained with the "full" model. One can see that at short stress times neglecting the cold carrier contribution does not affect HCD, while at times longer than ~5 ks the drain current change is substantially underestimated. This is because – as we discussed in [24] – short term HCD is determined by the drain N_{it} peak which is visible already at 10 s, see Fig. 2. In this device area carriers are rather hot, and therefore both SC- and MC-mechanisms are coupled and have high rates. This means that if one of these mechanisms is neglected, the drain N_{it} peak remains the same, and as a result ignoring the contribution of cold carriers

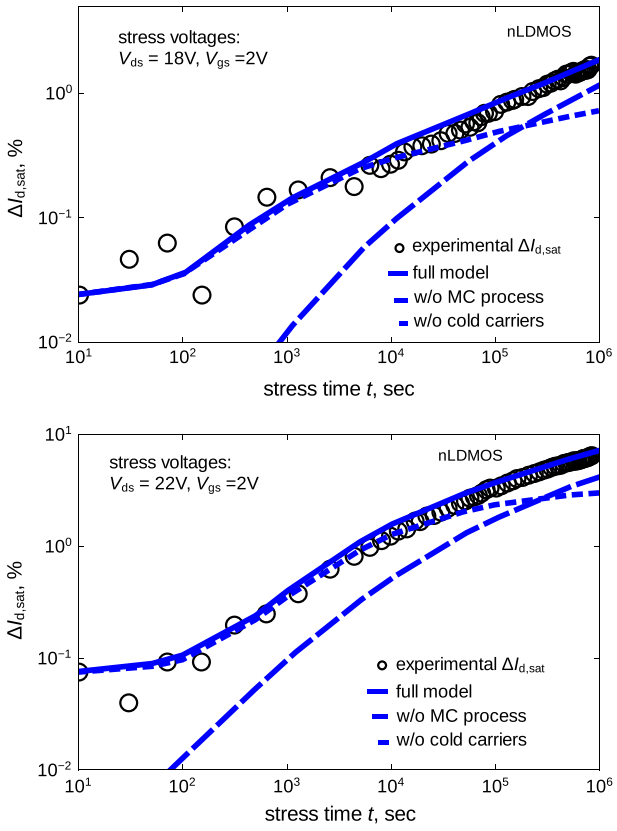

Fig. 5. The same as in Fig. 4 but for the saturation drain current.

does not change the $\Delta I_{d,lin}(t)$ and $\Delta I_{d,sat}(t)$ traces. The same trend is visible when the SC-process is ignored.

With increasing stress time the drain N_{it} peak becomes broader, i.e. HCD propagates into the device. However, at these times a substantial contribution is made by the growing channel and bird's beak N_{it} peaks, see Fig. 2. The peak in the channel is determined by the MC-process (in combination with the bond-breakage energy reduction due to the field-dipole interaction). Suppressing either the cold carrier fraction effect or the MC-process contribution leads to HCD underestimation at moderate and long stress times. This leads us to conclude that even in the case of high-voltage devices the cold carrier contribution cannot be omitted.

The cold carriers in the drain region having very high occupation probability cannot be represented if the second term corresponding to the cold carriers in (2) is omitted, see Fig. 3. Note that the DF in Fig. 3 was evaluated by just setting the cold carrier coefficient C to zero without further renormalization (i.e. the area under the DF curve no longer represents the local carrier concentration). This can severely affect the predictive capability of the HCD model.

Fig. 4 shows $\Delta I_{d,lin}(t)$ obtained from HCD model considering both SC and MC processes but ignoring the second term in (2) corresponding to the cold carriers for two stress conditions, i.e. V_{gs} = 2.0 V and V_{ds} = 18 and 22 V. The $\Delta I_{d,lin}(t)$ obtained from the full model, i.e. HCD model considering both SC and MC processes with DF evaluated using (2) are plotted for the comparison. Interestingly, the drain current degradation is not dramatically affected at short stress times by the second term, but at high stress times, where other processes have nearly saturated, the consideration of cold carriers in the drain region results in a significant difference of $\Delta I_{d,lin}(t)$. Fig. 4 also shows the importance of the MC process in the HCD model.

The rate of the MC process, as already discussed, is determined by (3), where the threshold energy ε_{th} is the distance between the Si–H bond vibrational levels and is equal to ~0.025 eV [6,35]. As for the SC process, which has an activation energy of ~1.5 eV, the corresponding rate is not affected if the DFs with the omitted cold carrier term are used, as opposed to the rate of the MC mechanism.

As can be seen, the HCD model considering just the SC process fails to describe $\Delta I_{d,lin}(t)$. In the nLDMOS transistor short-term HCD is determined by the drain N_{it} peak. Near the drain, the carriers are rather hot, and therefore one may expect that if the effect of cold particles is neglected, the corresponding N_{it} peak and changes of the device characteristics at short stress times will not be affected. Fig. 4 shows, however, that this is only partially true and neglecting the MC mechanism leads to severe underestimation of both $\Delta I_{d,lin}$ and $\Delta I_{d,sat}$ at short stress times and for both combinations of V_{ds}, V_{gs}. This originates from the fact that hot carriers contribute also to the MC bond-breakage process. Let us consider an electron which has gained an energy of 1.4 eV. This electron cannot trigger the SC process which has an activation energy of 1.5 eV [6,35] but it can excite the bond to a higher energy level. Now the bond-breakage energy needed to desorb the hydrogen atom is 0.1 eV and a probability to find carriers with this energy or above is very large. Therefore, we conclude that in the drain area the MC and SC processes are strongly coupled and neglecting the former mechanism leads to spurious $\Delta I_{d,lin}$ and $\Delta I_{d,sat}$ results.

As for the role of the low energetical fraction of the carrier ensemble, in the context of the drain N_{it} peak the contribution of these particles is screened by those electrons which have higher energies. Therefore, if the cold carrier term in the DF expression is omitted, the drain N_{it} peak is not impacted and the error in the $\Delta I_{d,lin}$ and $\Delta I_{d,sat}$ values is visible at stress times of ~3 ks and longer. An additional factor which is also responsible for this HCD underestimation is due to the fact that the cold carriers (together with the field-dipole lowering of the activation energy) are responsible for the channel N_{it} peak which contributes to HCD also in the case of long stresses [23,24].

The validity of the model beyond the nLDMOS transistor was tested by following a similar procedure for calculating DF, $N_{it}(x)$ profiles, and drain current degradation curves for the pLDMOS transistor. The DF in this case have a slightly different appearance in the drain region, lacking the cold carrier part, see Fig. 6, while near the STI corner, they look the same as for the bird's beak region in nLDMOS. This is due to differences in the architectures (and even different technology nodes) of n- and p-channel LDMOS transistors. Another reason which leads to the different shapes of the DFs simulated for the pLDMOS devices is the different stress

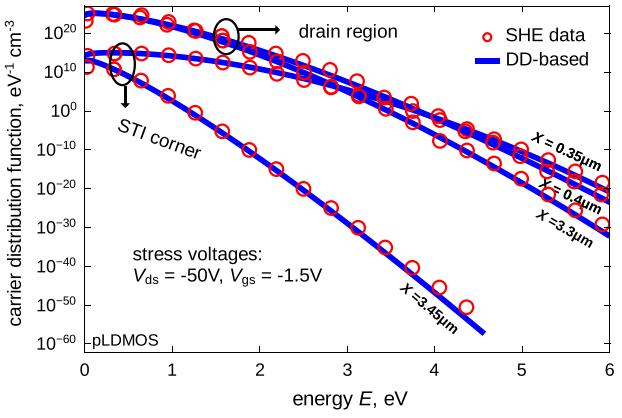

Fig. 6. Comparison of the DFs for the pLDMOS device obtained from the DD-based model with those obtained from ViennaSHE for stress voltages: $V_{ds} = -50$ V, $V_{gs} = -1.5$ V, calculated for different positions near the drain and STI corner.

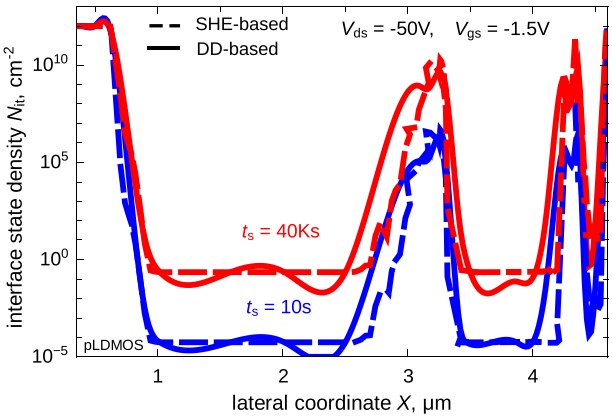

Fig. 7. Interface state density profiles obtained with SHE- and DD-based models, for the pLDMOS transistor. The stress voltages are $V_{ds} = -50$ and $V_{gs} = -1.5$ V applied for stress times 10 s and 40 Ks.

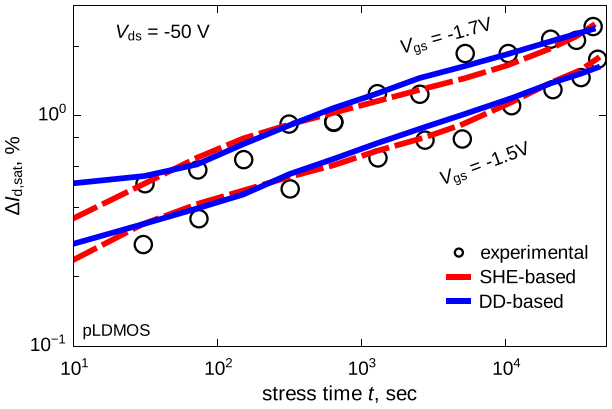

Fig. 8. Comparison of the change in the saturation drain current obtained from experiments and simulations, using the SHE- and DD-based models, for stress voltages $V_{ds} = -50$ V and $V_{gs} = -1.5$, -1.7 V for stress times up to 40 ks.

conditions for n- and p-channel transistors. Due to the high stress voltages used for the pLDMOS device ($V_{ds} = -50$ V) as compared to the nLDMOS counterpart ($V_{ds} = 20$ V), we do not see a very high concentration of cold carriers at the drain in the former case. As a result, the DFs for the pLDMOS lacks the Maxwellian rudiment which was present in the DF corresponding to the nLDMOS. Even in this case, the DF obtained from the DD-based approach and SHE method are quite similar.

These DFs are then used to calculate the $N_{it}(x)$ profiles for the entire lateral coordinate of the pLDMOS transistor. The $N_{it}(x)$ profiles are plotted in Fig. 7. To prove that the model works well for pLDMOS device too, the $\Delta I_{d,sat}(t)$ obtained from simulations is plotted against the experimental data in Fig. 8. As can be seen, the simulated curves agree well with the experiments.

Finally, we report the $\Delta I_{d,sat}(t)$ neglecting the MC-process in the HCD model in Fig. 9 for the pLDMOS transistor. Again, we see an underestimation of degradation if the MC process is not included. Since at such high stress voltages as $V_{ds} = -50$ V the concentration of hot-carriers is higher as compared to the nLDMOS device, the underestimation is not as severe. As the stress time increases, the underestimation reduces due to the increase in number of hot-carriers and the SC-process dominates at higher stress times. Neglecting the cold carrier term in (2) does not affect the DF and the HCD in the pLDMOS as the cold carriers concentration is not very high in this device at stress voltages of $V_{ds} = -50$ V and $V_{ds} = -1.5$ and -1.7 V.

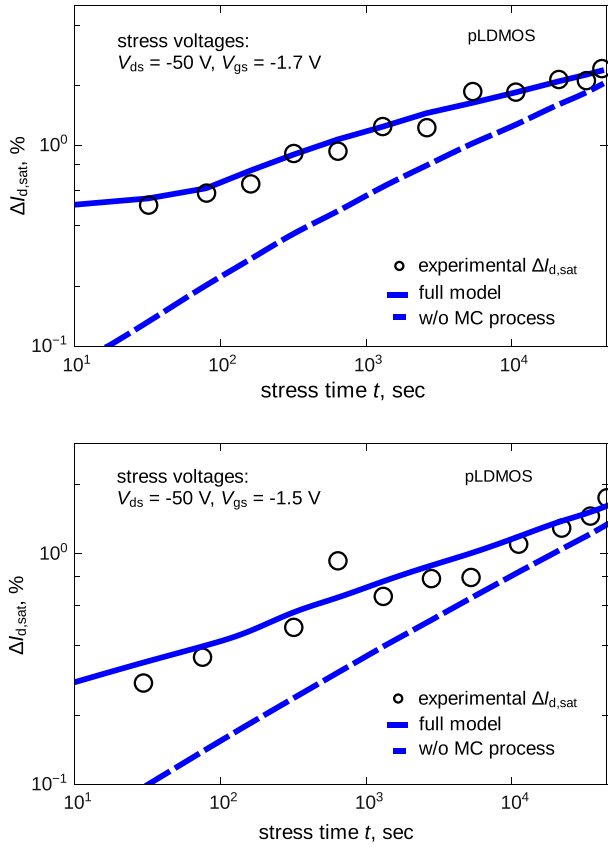

Fig. 9. The change of the saturation drain current $\Delta I_{d,sat}$ as a function of stress time: experimental data, the results of the full model, and the traces obtained neglecting the MC-process. The stress voltages were $V_{ds} = -50$ V and $V_{ds} = -1.5$ and -1.7 V.

5. Conclusions

Using our physics-based model for hot-carrier degradation, we check the role of colder carriers in HCD of n- and p-channel LDMOS transistors. For this purpose, we employ two versions of the model: the first one is based on the solution of the Boltzmann transport equation using the spherical harmonics expansion method, while the second one employs an analytic expression for the carrier energy distribution function with the parameters based on the macroscopic characteristics of the device found using drift–diffusion simulations. Note that the first model realization is more thorough but at the same time requires more computational resources, while the second variant was shown to be applicable for HCD in long-channel and/or high-voltage devices. Furthermore, the analytic formula for the distribution function contains two terms, i.e. the one which represents the hot carrier fraction of the statistical ensemble and the second one which models the thermalized cold carriers. The effect of cold carriers on HCD is twofold: these carriers contribute to the low energy fraction of the carrier energy distribution function and also trigger the multiple-particle process of Si–H bond dissociation. As a result, the drift–diffusion based version of our model is more feasible for analysis of the role of cold carriers in HCD.

Both versions of the model are capable of representing the degradation of the linear and saturation drain currents in both n- and p-channel devices and using the same set of the model parameters. If the multiple-carrier process rate is neglected, $\Delta I_{d,lin}$ and $\Delta I_{d,sat}$ are severely underestimated in both LDMOS transistors. Note that this trend is especially pronounced at short stress times. We have shown in our previous publications that short-term HCD is determined by the drain N_{it} [23,24]. In the drain the carriers are hot enough and have a high concentration. As a result, both single- and multiple-carrier processes of bond dissociation are strongly coupled. For instance, those carriers with energies slightly below the Si–H bond-breakage activation energy can excite the bond, therefore contributing to the multiple-carrier process. If the bond is pre-excited by this process, a substantially lower energy is needed to trigger the bond rupture event. Therefore, ignoring the MC process rate can also impact the rate of the SC mechanism.

If the cold particle term is omitted in the analytic expression for the carrier distribution function, this leads to an error in the predicted $\Delta I_{d,lin}$ and $\Delta I_{d,sat}$ values. Such a behavior stems from the fact that at short stress times the effect of these cold carriers is screened by the contribution of their hotter counterparts. In addition, the common effect of cold carriers with the bond weakening due to the field-dipole interaction leads to a channel N_{it} peak which also contributes to HCD at longer stress times. Finally, it is important to emphasize that all trends are the same for both n- and p-channel devices and that for both transistors a unique set of the model parameters has been used.

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