

# Modeling of Hot-Carrier Degradation in LDMOS Devices Using a Drift-Diffusion Based Approach

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**Abstract**—We model hot-carrier degradation (HCD) in n- and p-channel LDMOS transistors using an analytic approximation of the carrier energy distribution function (DF). Carrier transport, which is an essential ingredient of our HCD model, is described using the drift-diffusion (DD) method. The analytical DF is used to evaluate the bond-breakage rates. As a reference, we also obtain the DF from the solution of the Boltzmann transport equation using the spherical harmonics expansion (SHE) method. The distribution functions and interface state density profiles computed using the SHE and DD-based approaches are compared. The comparison of the device degradation characteristics simulated by these two approaches with the experimental data shows that the DD-based variant, which is considerably less computationally expensive, provides good accuracy. We, therefore, conclude that the DD-based version is efficient for predictive HCD simulations in LDMOS devices.

**Index Terms**—hot-carrier degradation, LDMOS transistor, carrier transport, spherical harmonics expansion, drift-diffusion scheme, modeling

## I. INTRODUCTION

It has been recently shown that even in high-voltage devices the contribution of cold carriers to hot-carrier degradation (HCD) can play a significant role [1]–[4]. As a result, it is important to properly capture the interplay between the single- and multiple-carrier Si-H bond dissociation mechanisms (SC and MC processes) driven by hot and cold carriers, respectively. In the SC process a single hot carrier supplies the activation energy required for the Si-H bond breakage in a collision. Conversely, in the MC process, a single carrier does not have enough energy to rupture the bond in one collision and, thus, results in the excitation of the bond. After multiple such encounters with colder carriers, the bond ends up in an excited state with sufficiently high energy and only a small portion of energy needed to release the hydrogen atom. In order to quantify the hot and cold carriers, one needs to address carrier transport and evaluate the carrier energy distribution function (DF) [5]–[7].

The carrier energy DF is calculated as the solution of the Boltzmann transport equation (BTE) which, in LDMOS devices, is a very complicated task. First, this is related to the computationally expensive schemes required to solve the BTE such as the stochastic Monte-Carlo method [8], [9] or the deterministic spherical harmonics expansion method [10]–[12]. Second, LDMOS devices typically have very complex structures (bird’s beak, shallow trench isolation, curved interfaces,

etc.) and large dimensions. This implies a large mesh and many variables which further complicates the computation. As a result, the application of a predictive hot-carrier degradation model, which can properly capture carrier transport [5], [6], appears to be difficult for LDMOS transistors. However, as shown in [13], [14], simplified approaches to the BTE solution can be used for transistors with channel lengths longer than  $\sim 500$  nm. Such approaches are based on the moments of the Boltzmann transport equation [15]–[18] and one of the most attractive among them is the drift-diffusion (DD) scheme. These models attempt to mimic the carrier energy distribution function by an analytic expression which is linked to the electric field and the concentration of minority carriers, obtained using the DD approach to the BTE solution.

Although some of these models are capable of representing the carrier DF with reasonable accuracy they often fail to properly describe HCD [19]. This is because even small discrepancies in the DF can translate to substantial errors in calculated changes of the device characteristics. In this paper we check the applicability of our DD-based HCD model for both n- and p-channel LDMOS devices. We use an analytical expression for the energy distribution of the minority carriers. This expression mimics the DF obtained from the full solution of the BTE using the spherical harmonics expansion method. We use these DFs in our physics-based HCD model which are validated against experimental data on LDMOS devices and compare the results with those obtained using the full BTE solution.

## II. EXPERIMENT

We used n- and p-LDMOS transistors (sketched in Fig. 1) fabricated on standard 0.35 and 0.18  $\mu\text{m}$  processes with maximum operating drain voltages ( $V_{\text{ds}}$ ) of 20 and -50 V. The n-channel devices have a Si/SiO<sub>2</sub> interface length of  $\sim 3.4$   $\mu\text{m}$ , and a gate length of  $\sim 2.5$   $\mu\text{m}$ , while the p-channel devices have an interface length of  $\sim 4.4$   $\mu\text{m}$ , and a gate length of  $\sim 3.3$   $\mu\text{m}$ . The n-LDMOS transistors have been subjected to hot carrier stress at two combinations of drain and gate voltages, i.e.  $V_{\text{ds}} = 18$  V,  $V_{\text{gs}} = 2$  V and  $V_{\text{ds}} = 22$  V,  $V_{\text{gs}} = 2$  V for  $\sim 1$  Ms, while the p-channel devices have been stressed at  $V_{\text{ds}} = -50$  V,  $V_{\text{gs}} = -1.5$  V and  $V_{\text{ds}} = -50$  V,  $V_{\text{gs}} = -1.7$  V for  $\sim 40$  ks. All measurements were performed at room temperature. As a manifestation of HCD, the relative change

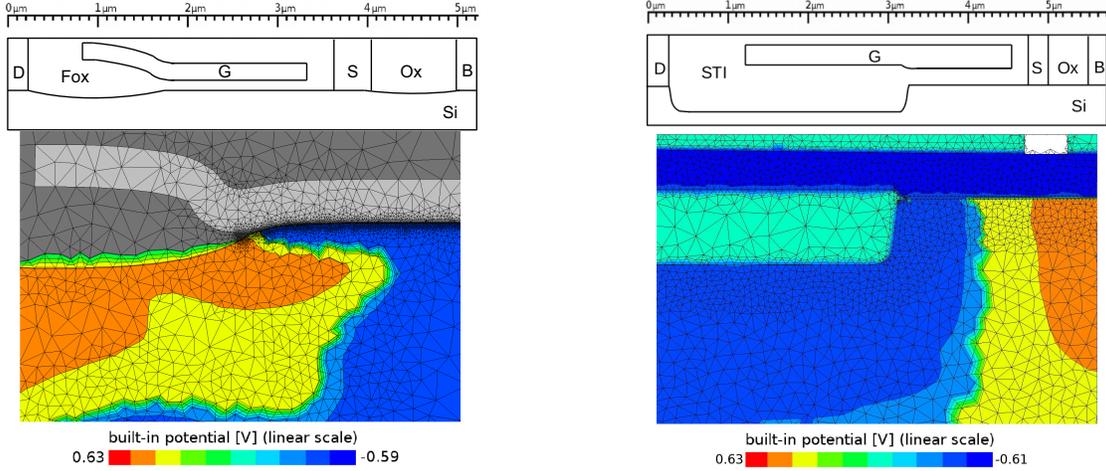


Fig. 1: Upper panel: sketch of the n-LDMOS and p-LDMOS transistors with all the segments marked: D - drain, S - source, Ox - oxide, Fox - field oxide, G - gate, B - bulk contact. Lower panel: the adaptive mesh for a near interface device section with the built-in potential represented by the color map.

of the saturation drain current ( $\Delta I_{d,sat}$ ) was recorded as a function of stress time  $t$ .

### III. MODEL DETAILS

Our model consists of three sub-tasks: In the first sub-task, the carrier DF is evaluated to determine the concentrations of hot and cold carriers. Next, the rates of the competing SC and MC mechanisms are evaluated using these DFs [5], [6]. Finally, the degraded device is simulated to obtain the change of the device characteristics with time.

The DF is obtained as a solution of the BTE for a particular device architecture and given stress/operating conditions. There are two realizations of our HCD model: the first version is based on the full BTE solution, while the second one uses an analytic expression for the DF. The full BTE solution is obtained with our deterministic solver ViennaSHE which employs the spherical harmonics expansion method [20]. In the second case the DF is described by the analytic expression [21]:

$$f(\varepsilon) = A \exp\left[-(\varepsilon/\varepsilon_{ref})^b\right] + C \exp\left[-\varepsilon/(k_B T_n)\right], \quad (1)$$

where the first term represents the population of hot carriers, while the second term accounts for the contribution of colder carriers.

The parameters  $A$ ,  $C$ , and  $\varepsilon_{ref}$  in (1), are found using the carrier concentration and the carrier temperature in the DF normalization criterion [22]:

$$\int_0^\infty f(\varepsilon)g(\varepsilon)d\varepsilon = n \quad (2)$$

$$\int_0^\infty \varepsilon f(\varepsilon)g(\varepsilon)d\varepsilon = \frac{3}{2}n k_B T_n \quad (3)$$

$$\int_0^\infty f(\varepsilon)d\varepsilon = 1, \quad (4)$$

while a constant value of  $b$  (1 for contact regions, 2 otherwise) is used. The carrier temperature ( $T_n$ ) is approximately linked

to the lattice temperature  $T_L$ :

$$T_n = T_L + 2q\tau\mu F^2/3k_B, \quad (5)$$

where  $\tau$  and  $F$  are the energy relaxation time and the electric field (obtained from DD simulations) [15].

The carrier DFs are then used to compute the density of interface states  $N_{it}$  as a function of the lateral coordinate  $x$  along the Si/SiO<sub>2</sub> interface for each stress time step  $t$ . We consider the single- and multiple-carrier bond-breakage mechanisms as two competing pathways converting electrically passive Si-H bonds to active interface traps. Note that the concentration of cold carriers is important even for large devices such as these LDMOS transistors because the SC and MC mechanisms are strongly coupled [6], [23]. Carriers with energies below the activation energy of the SC process cannot directly provoke a bond rupture event but they can contribute to the MC process by heating up the bond to an excited level thereby substantially reducing the bond-breakage portion of energy. Therefore, relatively low energetic carriers can also efficiently break the bond. As a result, hot carriers make a substantial contribution to the MC process, while their cold counterparts can be important also for the SC mechanism.

Another important model ingredient is the reduction of the activation energy for the bond breakage reaction by the interaction of the bond dipole moment with the electric field [6], [23], [24] and the variation in this energy due to the structural disorder at the Si/SiO<sub>2</sub> interface.

The  $N_{it}(x, t)$  profiles obtained are then loaded into our DD-based device simulator MiniMOS-NT [25] which simulates the characteristics of the degraded devices. It is important to emphasize that for fast and reliable SHE and DD simulations a proper mesh is needed. Such a mesh should be fine in all the important devices regions (at the interface, near the bird's beak, etc.) and still contain a moderate number of elements. To generate such a mesh we use our highly adaptive meshing framework ViennaMesh [26], [27] which generates meshes

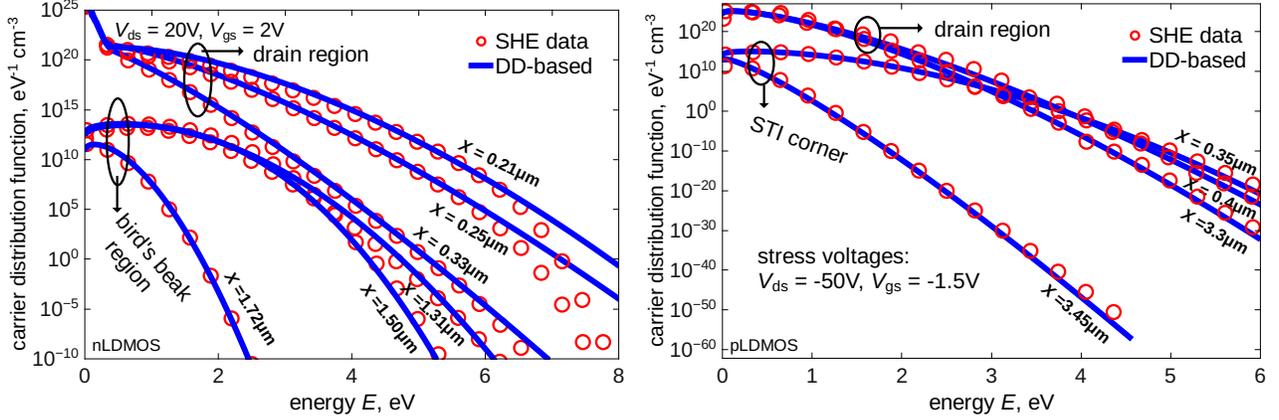


Fig. 2: The distribution functions for minority carriers simulated for the n-LDMOS (for  $V_{ds} = 20$  V and  $V_{gs} = 2$  V) and p-LDMOS ( $V_{ds} = -50$  V,  $V_{gs} = -1.5$  V) devices using the solution of the Boltzmann transport equation with ViennaSHE and the DD-based model. The DFs are shown for different values of the lateral coordinate related to the drain and bird's beak/STI corner positions.

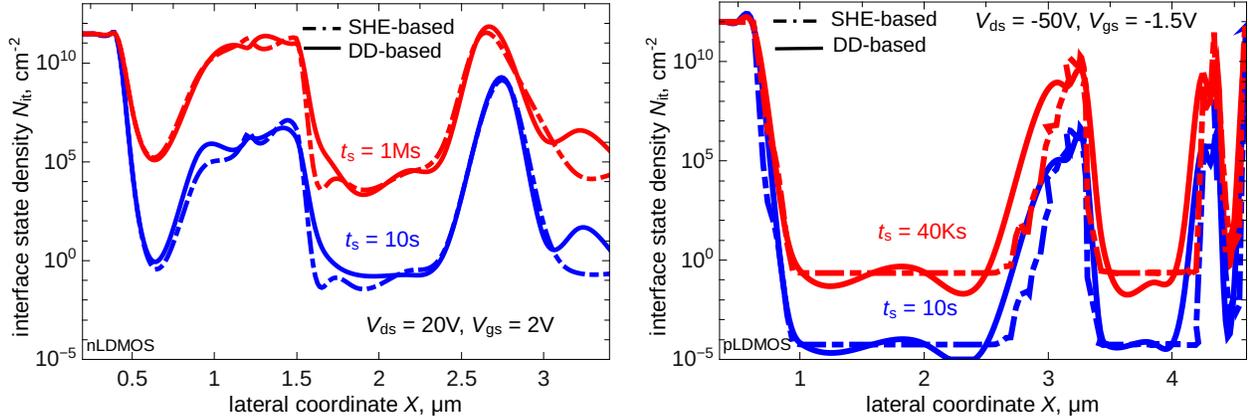


Fig. 3: The interface trap density profiles evaluated with the SHE- and DD-based version of our HCD model for the n-LDMOS (stress time steps are 10 s and 1 Ms) and p-LDMOS devices (stress times are 10 s and 40 ks). The stress voltages used are the same as in Fig. 2.

based on the built-in potential, see Fig. 1.

#### IV. RESULTS AND DISCUSSION

The DFs for minority carriers in the n- and p-LDMOS devices evaluated with the SHE method and with the DD-based analytical model are summarized in Fig. 2. The exemplary DFs given in Fig. 2 are calculated for  $V_{ds} = 20$  V,  $V_{gs} = 2$  V (n-LDMOS transistor) and  $V_{ds} = -50$  V,  $V_{gs} = -1.5$  V (p-LDMOS device) and plotted for different values of the lateral coordinate  $x$ , which correspond to the bird's beak in the nLDMOS, the STI corner in the pLDMOS and the drain region. One can see that the DFs are severely non-equilibrium in both the devices. Another important pronounced peculiarity is that the drain region of the nLDMOS device has a high concentration of cold carriers which is not visible for the pLDMOS. Such a trend is attributed to the difference in the device topology and the operating voltages. The pLDMOS has been stressed at very high voltages ( $V_{ds} = -50$  V) as compared to the nLDMOS ( $V_{ds} = 20$  V). One can see that the agreement between the DFs simulated with ViennaSHE and those obtained with the analytic model is very good for both types of carriers in all

device regions.

The  $N_{it}(x)$  profiles evaluated with the SHE- and DD-based DFs for the same combinations of stress  $V_{ds}$  and  $V_{gs}$  as those used in Fig. 2 are shown in Fig. 3. Remarkably for both devices,  $N_{it}(x)$  profiles simulated with different versions of the model are very similar. The peak in  $N_{it}(x)$  profiles at the drain region is attributed to the saturation of both the single- and the multiple-carrier mechanisms. This trend stems from a combination of high energies typical for the near drain device area and high particle concentrations. In the case of the nLDMOS transistor, the second  $N_{it}$  peak is pronounced near the bird's beak which is the outcome of the single-carrier Si-H bond breakage process. The rate of the multiple-carrier process is very low in this region as the concentration of colder carrier is not very high as was seen for the drain region. Similarly, the  $N_{it}$  peak near the STI corner for the pLDMOS is attributed to the bond breakage by hot carriers in this area. The third peak in the channel- of both kind of devices- is due to the multiple-carrier process and also the interaction of the bond's dipole moment with the electric field because the carrier concentration and the average carrier energy are high

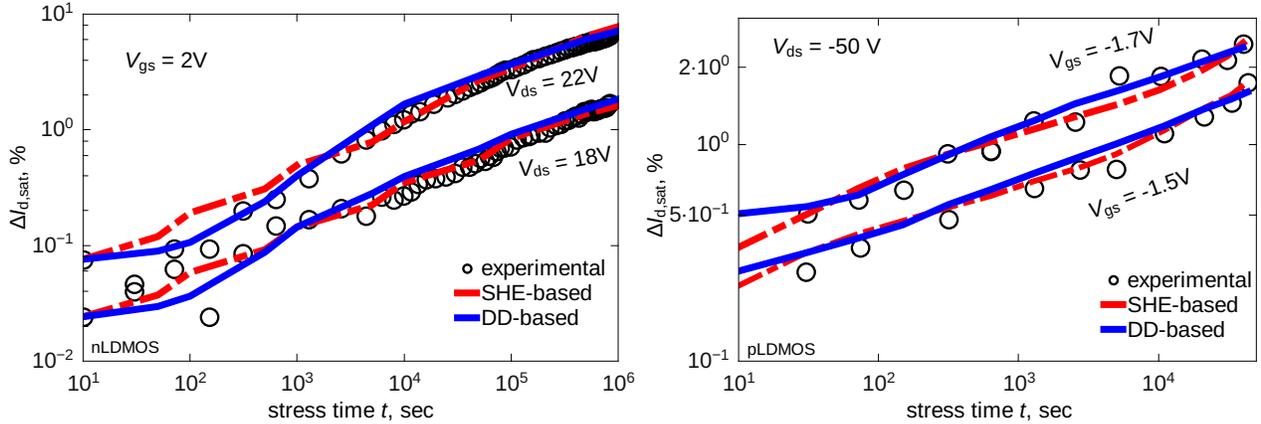


Fig. 4: The  $\Delta I_{d,sat}(t)$  degradation traces – experiment vs. simulation results (obtained with the SHE- and DD-based versions of our HCD model) – are plotted for n- and p-LDMOS devices and both stress conditions. One can see that both versions of the model lead to very similar results which can properly represent the experimental HCD data.

in this region of the device.

The measured relative changes of the saturation drain currents as a function of stress time are plotted in Fig. 4 against those obtained with the SHE- and DD-based versions of the model. These plots show that for both n- and p-channel LDMOS transistors, the agreement between the experimental and theoretical traces is very good. Moreover, the two different versions of the model lead to similar results. It is important to emphasize that the DD-based version of our HCD model does not need substantial computational resources and is fast. This circumstance makes it very attractive for predictive HCD simulations in high-voltage transistors.

#### V. CONCLUSIONS

We use an analytic expression for the carrier DFs which only requires the results of DD simulations. Our expression accounts for both the hot and cold carriers which are important for the SC and MC mechanisms considered in our HCD model. The DFs computed with this approach are compared with the full BTE solution using the spherical harmonics expansion method for the case of n- and p-channel LDMOS devices and good agreement is obtained. The DD-based model for the energy DFs is valid for both electrons and holes. The DFs obtained using the SHE method and the DD-based approach are then used in our physics-based hot-carrier degradation model to evaluate the interface state density profiles. We have shown that both versions of the model lead to very similar results for both n- and p-channel devices. In order to test the predictive capabilities of our model, we simulated the saturation drain current for a series of stress times and compared the results obtained from both version of the model with the experiments. The saturation drain current during hot-carrier stress obtained from the experiments were well represented by both the SHE- and DD-based versions in the LDMOS devices. This makes the fast and flexible DD-based HCD model very attractive for predictive simulations in the case of high-voltage transistors.

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