Global statistical methodology for the analysis of equipment parameter effects on TSV formation

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***Abstract* — We describe a global methodology for the extraction and the quantification of the effects of the most relevant equipment parameters involved in TSV processing. With a specific focus on the DRIE step of the TSVs' fabrication, we propose a dedicated simulation flow describing the distribution of the species over the wafer inside the etching chamber, the physical plasma simulation of polymer deposition and etching loops, and the electrical performance simulation of the resulting structures. Statistical techniques such as Pareto Graphs and Design of Experiments are used for the extraction of the most relevant equipment parameters on the electrical and metal stress responses.**

Keywords— TSV, TCAD, equipment parameter variability, DRIE etching, screening, DoE

I. INTRODUCTION

The recent developments in semiconductor technology have enabled devices to connect vertically, by means of an electrical interconnection that crosses the entire thickness of the wafer [1] [2]. In this technology, different possibilities to integrate devices have become available, for example, chips can be piled vertically according to functionality, instead of being deployed laterally. The benefits of vertical integration include smaller interconnection paths, higher integration, reduced power consumption, and multi-functionality [2].

The core of the vertical integration lies in the ability to connect electrically the front and back sides of the wafer. A Through Silicon Via (TSV) is the element responsible to provide this integration capability. A TSV is a large metal structure carefully built by drilling a hole through a wafer and filling it with a conducting metal (filled TSVs). An alternative to the metal filling is to deposit a thin metal layer along the TSV's wall, leaving most of the hole empty (unfilled TSVs). Filled TSVs are more readily available in the literature, but this work refers to a particular technology of unfilled TSVs [1].

The manufacture of unfilled TSVs is a process which involves deep etching through the silicon wafer, followed by the deposition of an isolation oxide, a barrier material (to prevent silicon contamination), a metal film, and a passivation layer. The entire process is rather complex and small deviations of the process conditions are expected. In this work a first attempt to quantify those deviations in an unfilled TSV technology is made. Our goal is to relate the variability of the equipment used on the TSV processing to the electrical and mechanical performance of the via.

In this study the main sources of variability are identified by statistical analysis of equipment and process simulations. The actual range of variation of the processing parameters in the equipment during manufacture are taken into consideration. The structures originated from the process simulations are then used for electrical and mechanical simulations, in order to assess the impact of equipment variability to the TSV performance.

This manuscript is divided into six sections. The next section describes the TSV process in details, where the relevant processing parameters of the equipment are presented. In the third section the approach to identify the main variability sources and how to treat them statistically is discussed, in order to properly understand the impact on TSV performance. The fourth section describes the simulation methodology, where a scheme to link equipment, process, and physical (electrical and mechanical) simulations is proposed. In the fifth section the results of the simulation scheme are discussed and the relation between variability on the equipment level and TSV performance is delineated. Finally the work is summarized and the main conclusions are drawn, while an insight into the direction of our future work is given.

II. TSVS PROCESSING DESCRIPTION

The TSV devices are built after the standard CMOS processing sequence including backend interconnection and bond oxide deposition. The wafer is polished using chemical-mechanical polishing (CMP) and the bulk substrate is thinned to the desired thickness, here to 250µm. The subsequent TSV processing is performed in three main steps [3] [4].

A. Deep Reactive Ion Etch

After the opening of the inter-metal dielectrics, the bulk is etched using a Deep Reactive Ion Etch (DRIE) process down to the metal layer, deposited on the second face of the wafer and used as an etch-stop. The DRIE process proceeds according to the so called "Bosch" process [5] steps and is applied on SPTS Rapier etch equipment. This process consists of a sequence of a polymer deposition step for sidewall passivation and an etching step to remove the bottom section of the deposited polymer and

partially etch the bulk silicon, while avoiding the TSV sidewall, in order to have an anisotropic etching process down to the bottom metal layer. At the beginning of the etching process, a minimum undercut is necessary for the initialization of the process which involves two subsidiary steps. A first low etch rate cycle is performed for good control of the TSV etching for a few cycles, followed by a higher etch rate process to the bottom of the TSV. Similar to the DRIE process, a sequence of passivation and etching phases is applied, resulting in imprinted markings along the TSV sidewall; markings which are also referred to as scallops. The size of these scallops depends on the rates used during the DRIE process.

B. *Spacer oxide*

For the isolation of the bulk substrate along the TSV sidewall, a spacer oxide is deposited. Because the TSVs are processed at the end of the full process flow and particularly after the backend part with aluminum interconnect deposition, the maximal temperature process is limited to 400ºC. To overcome this issue, the spacer oxide deposition is performed using multiple deposition methods. Initially, a Plasma Enhanced Chemical Vapor Deposition (PECVD) technique is used for its low process temperature and to initiate the oxide deposition. To compensate for the lack of conformality of the oxide deposited by PECVD, a Sub-Atmospheric Chemical Vapor Deposition (SACVD) is used as a second spacer oxide deposition step, performed at low temperature. A final PECVD deposition step is applied in order to get an optimal spacer oxide layer deposition along the TSV sidewall.

C. *Metallization*

For proper electrical conduction of the signals between the two sides of the wafer a thin tungsten layer is deposited with a conventional Chemical Vapor Deposition (CVD) technique in an open TSV structure approach. This layer connects the aluminum metal layers placed on the top of the TSV structure and the bottom aluminum plate, which is simultaneously used as an etch stop layer during the DRIE process step.

D. *Passivation*

Additional oxide and nitride layers are also deposited for electrical and moisture isolation of the open TSV. These layers are not considered in our study due to their insignificant impact on the variability of the electrical parameters. Fig. 1 depicts a detailed cross section of the TSV with the different layers – and DRIE scallops caused in the via processing.

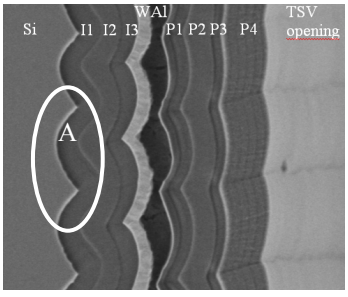


Fig. 1. TSV sidewall layer showing the scallops resulting after DRIE (A), PECVD, SACVD oxides (I1, I2, I3) of the oxide spacer deposition step and the tungsten layer (W)

E. *Identification of equipment variability sources*

Based on the TSV process flow described above, different sources of variability can be extracted:

The first source results from the impact of the scallops on the layers deposited after the DRIE step. This step requires a large number (few hundreds) of sub-phases of polymer deposition and etching loops and, despite a rigorous control of the species injected in the chamber, we can observe a variation of the quantities and a variation of the timing allocated to these steps.

The second variability source for the TSV performance is the variation of the oxide deposited along the TSV sidewall. As this oxide is deposited in different steps, variations of the oxide thickness can be observed. In [6] it is demonstrated that a variation of the oxygen distribution above the wafer can lead to a variation of a few percent of the oxide deposited along the TSV sidewall, which leads to variations in the parasitic capacitance of the TSV electrical performance.

Finally, a variation in the tungsten quantity available during CVD deposition leads to a variation in the tungsten thickness and has an impact on the TSV resistance value [1].

III. VARIABILITY METHODOLOGY ANALYSIS

A. *Generic methodology*

We propose the extraction of the most relevant equipment parameters of the different process steps involved in the TSV generation, and to quantify their impact on the electrical performance of the TSV. Due to the complexity of the TSV processing and the difficulty to control small variations of a large amount of equipment parameters, a global approach combining equipment TCAD simulation of the different steps, statistical analysis, and modeling is presented.

For each process step presented in the previous section, equipment parameters are identified and monitored inline. Based on their statistical distribution and range variation, a specific Design of Experiments (DoE) [7] is generated. Because of the large number of equipment parameters, a first sequence of DoE is carried out with the aim to extract the most relevant parameters by using Plackett and Burman designs [8] and Pareto graphs.

Several responses are also defined at this level such as the scallops' morphology (width and depth), layer thicknesses (oxide, tungsten), electrical parameters (resistance, capacitance, and inductance), and reliability parameters (maximum current density in TSV sidewall at a current injection of 100mA and stress). The analysis of the effects of the equipment parameters on the responses by Pareto graphs highlights the most relevant parameters. In addition to reducing the number of parameters to analyze in the second step of the methodology, these results provide invaluable information to the process engineers in order to increase the process control of these parameters in the different chamber tools and to improve the yield of the TSV.

In the second sequence, based on the most relevant parameters extracted beforehand, a full DoE is performed in order to quantify the variability of the responses as a quadratic

function of the equipment parameters with a Response Surface Modeling (RSM) approach. The thereby obtained models are used for sensitivity analysis in order to compare the distribution variability of the responses to inline measurements of the electrical parameters such as the TSV resistance and capacitance.

Finally, as the TSV can be described as an RCL sub-circuit device, the models is used at the SPICE circuit level for analysis of the impact of the TSV variability at the circuit level.

Fig. 2 outlines the global methodology described above from the equipment parameters involved at each main TSV process step up to the sensitivity analysis of the electrical performance of the TSV.

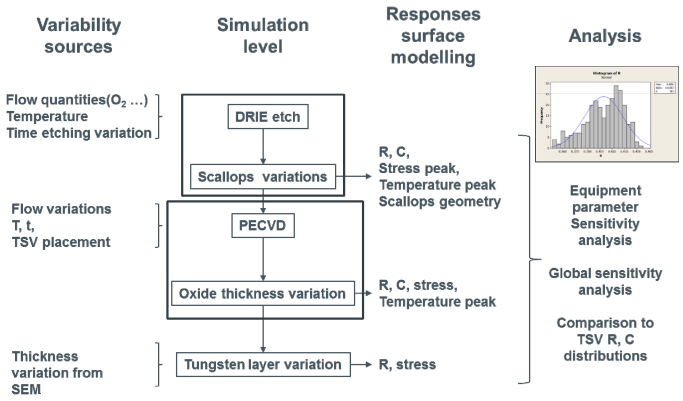


Fig. 2. Analysis methodology of TSV equipment parameters' variability on TSV electrical performances.

B. *Application to DRIE*

In this part, we focus on the DRIE process of TSV formation. As previously stated, this process step is performed in two phases of successive loops of polymer deposition and etching. The relative quantities of the species involved during the different phases (C_4F_8 for polymer deposition, SF_6 and O_2 for etching) at their own states (on and off), and their durations have been monitored on the plasma equipment used for DRIE.

The resulting number of independent equipment parameters used at this level reduces to an analysis of 30 parameters. An L32 Plackett and Burman design [8] for the screening of the parameters' effects is taken into consideration for the rest of the study.

IV. Simulation Methodology

Our analysis aims to correlate the variability sources on equipment level to the electrical parameters of the final device. Hence, the simulation flow must properly account for the plasma generation, the wafer etching, and finally the electrical parameter extraction. It is unfeasible to treat those three steps together in a unique physical based model, but a more suitable approach is to resolve them separately, linking them in a forward chain as depicted on Fig. 3. Each step is detailed in the following sections.

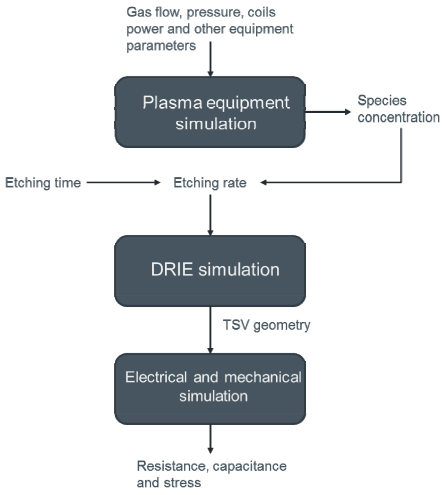


Fig. 3. Simulation flow connecting every step necessary to obtain the electrical and mechanical parameters. Input and output from each step is also depicted.

A. *Species distribution*

The plasma equipment is simulated by Quantemol VT [9]. It is a software based on the Hybrid Plasma Equipment Model (HPEM) used to obtain the species distribution and other physical quantities inside the chamber, especially over the wafer surface. It takes as input the flow of SF_6, O_2 and C_4F_8, pressure, and coil power, accordingly to each DRIE step as defined in the L32 design. From the results the relevant species' distributions on the wafer are extracted and then used to compute the rates for the next step (as described in the next section).

One of the critical points in the plasma equipment simulation is to establish the suitable chemistry set to describe the particle kinetics inside the chamber. We have based our chemical model on a reduced set of the most relevant reactions found in the literature, while the complete set is omitted in this paper, since it is not pertinent to the current discussion and the amount of data is substantial. However, one can find the chemistry used in our simulation in the works of Mao et al. [10] and Rauf et al. [11] for the SF_6/O_2 steps and in the work of Li et al. [12] for the C_4F_8 step.

Typical simulation results for relevant species are depicted in Fig. 4 and Fig. 5 for SF_6/O_2 and C_4F_8 chemistry respectively. The equipment used in our technology is an SPTS Rapier for DRIE processes.

From the equipment simulation the species concentrations are extracted along the wafer surface, the etch rates are calculated at the middle of the wafer, and the rates of the relevant species are finally used as input for the etching simulation as described in the following.

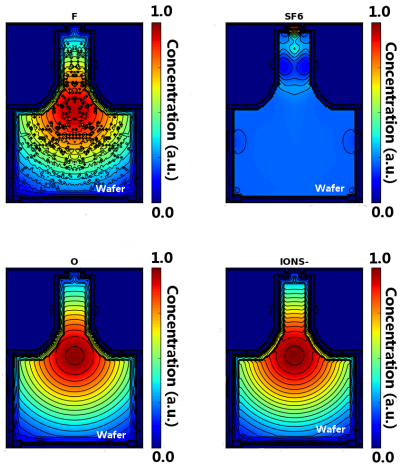


Fig. 4. Species concentration of a typical plasma equipment simulation, considering the SF_6/O_2 chemistry.

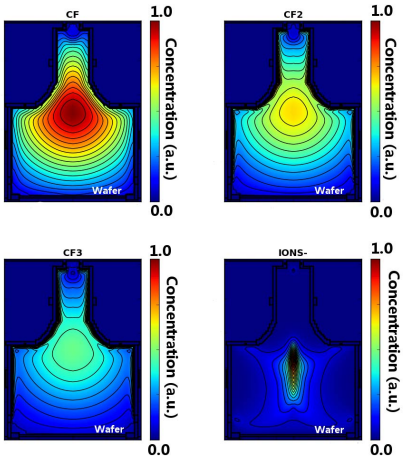


Fig. 5. Species concentration of a typical plasma equipment simulation, considering the C_4F_8 chemistry.

B. *DRIE etching*

1) Physical modeling

In order to generate the TSV structures necessary for the extraction of electrical parameters and stress, several simulation methodologies must be implemented. DRIE involves the deposition of a polymer in a fluorocarbon (C_4F_8) gas environment and an etching step in an SF_6/O_2 environment. The simulations are performed using a TU Wien in-house process simulator based on the level set and ray tracing techniques [13] in combination with several models for polymer deposition and silicon etching [14], [15], [16]. The model for the polymer deposition incorporates the presence of two fluxes at the wafer surface: neutral CFx and ion. The CFx flux is responsible for the isotropic chemical deposition, while the ions have little influence on the sidewall and deposit mainly along the flat horizontal surfaces. The influence of both fluxes on the growth rate of the depositing material are calculated and applied to the level set description of the wafer and trench surfaces.

For the etching cycle a more complex model is required for several reasons:

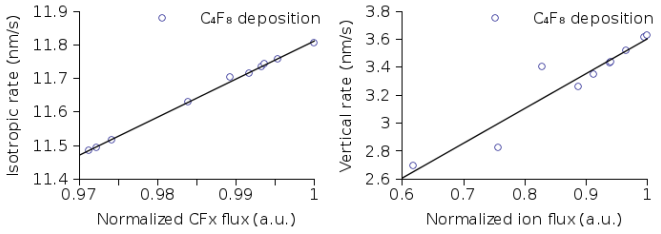
1. The etching in an oxygen environment cannot be represented with a simple neutral/ion flux, because the oxygen atoms effectively act as a coating agent reducing the amount of lateral etching which can proceed during a step, thereby promoting a more vertical etch.
2. Each material involved (oxide mask, polymer, silicon) has a different etch rate in the presence of the SF_6 and SF_6/O_2 plasma.
3. The early cycles use a pure SF_6 plasma as the etch cycle component, while later cycles are a three-step process, where the second step involves an added SF_6/O_2 plasma etching.

The models used to simulate etching in an SF_6 or SF_6/O_2 plasma are given in [15] and [16], respectively. In this model, the fluxes of three different particles are monitored, those of the chemical etch component, the physical ions, and the oxygen atom. The etch rate through the silicon is a combination of the chemical etch in the presence of fluoride, the physical sputtering due to the interaction of ions with the silicon surface, and ion-enhanced etching. The chemical and ion-enhanced etching components are a function of the fluoride coverage along the trench sidewalls and bottom; however, the coverage of some surface sites with oxygen limits the fluoride presence on the silicon surface, resulting in a reduced rate, especially for the chemical etch component. During every simulated time step the fluoride and oxygen surface coverages must be calculated and only then can the etch rates along the surface be found.

Precise simulations of TSV etching using the physical DRIE models described here require simulations of millions of particles at each time step, which would require an unfeasible amount of processing power, memory, and time in order to generate even a single structure. Therefore, instead of generating all structures using the physical models, the physical models are used to calculate the surface rates resulting during each step and the structures are then generated using a simplified model, where the rates are directly applied and the flux does not need to be calculated at every time step.

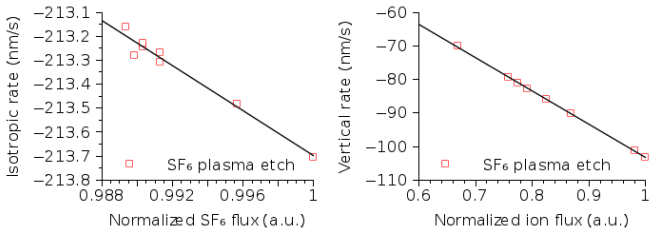
2) Empirical rate calculation

In order to find the deposition or etch rates during each step of the DRIE cycle sequence, sample simulations using physical models are performed. For the initial cycles of the sequence a deposition step is followed by SF_6 plasma etching, generating "small" scallops along the etched sidewall. The later cycles are then generated using a deposition step followed by an SF_6/O_2 plasma etch and an SF_6 plasma etch step to generate "large" scallops. The effects of the variation of fluxes found at the wafer surface on the deposition and etch rates through silicon for each step are calculated and given in Fig. 6, Fig. 7, and Fig. 8, respectively. It is evident that there is a linear influence between varying the relevant fluxes and the resulting deposition/etch rates. Even in the case of SF_6/O_2 plasma etching the vertical rate, which is the main etch component during this processing step, is primarily influenced by the ion flux.



(a) (b)

Fig. 6. Effect of varying (a) neutral and (b) ion fluxes on the surface rates during C_4F_8 deposition versus normalized flux at the maximum value.



(a) (b)

Fig. 7. Effect of varying (a) neutral and (b) ion fluxes on the surface rates during etching in SF_6 plasma versus normalized flux at the maximum value.

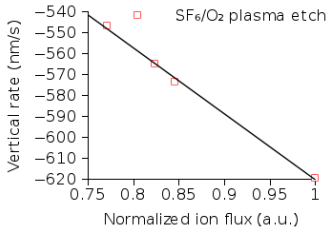


Fig. 8. Effect of varying the ion flux on the surface rate during etching in a SF_6/O_2 plasma versus normalized flux at the maximum value.

Using the relationships between the deposition/etch rates and the respective fluxes, several TSV structures are generated using a method similar to the one presented in [17] and the scallop size dependence on the variation of the flux of the neutral and ion species, and thereby the dependence on the gas concentration in the chamber, can be found.

C. *Electrical and stress simulation*

Structures generated in the previous step are used as input structures of the COMSOL Multiphysics software for the simulation of the electrical and stress performance of the resulting TSV structure. A nominal conformal oxide layer and a thin tungsten layer are deposited above the scallops. The thicknesses considered are placed at the nominal values of the targeted TSV structure, in order to disassociate the effects of the DRIE step from the effects of the layers thicknesses variations [6].

Because of the axis symmetry of the TSV structure, two-dimensional simulations are performed, with cylindrical coordinate considerations for the electrical simulations.

Fig. 9 presents the resulting structure after a DRIE simulation, with the presence of the first scallops on top of the structures followed by larger scallops resulting from the higher etching rate down to the bottom of the structure. Conformal oxide and tungsten layers are placed above the scallops for isolation of the structure and for and to create a conduction path between the two sides of the wafer.

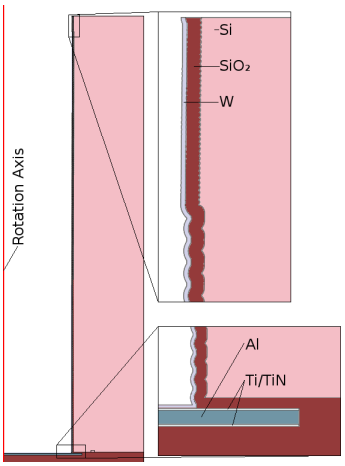


Fig. 9. Resulting TSV structure with scallops formation along the TSV sidewall, with small scallops located on the top of the structure

V. RESULTS

TABLE I. RELATIVE VARIATION OF THE RESPONSES WITHIN THE L32 DESIGN

	% Variation		% Variation
Large scallops width	9.64%	**R (mOhm)**	1.08%
Large scallops depth	10.34%	**C (pF)**	0.70%
Small scallops width	28.89%	**L (pH)**	1.20%
Small scallops depth	32.58%	**Average stress (MPa)**	3.04%

Table 1 summarizes the variations of the studied responses within the L32 design. We observe that despite large variations of the resulting scallops from 10% for the small ones up to 30% for the large ones, the variation of the electrical responses such as Resistance (R), Capacitance (C) and Inductance (L) are relatively contained at less than 2%. This indicates that regardless of the modification of the conduction path or the modification of the oxide shape along the TSV sidewall due to the change of the scallops' morphology, the main cause of TSV performance variability is not coming from the DRIE step, but certainly directly from the oxide and tungsten deposition steps' variations [1] [2].

However, in terms of structure reliability, we can observe that the maximum stress observed in the structure has a large variability, in the same order of magnitude of the scallops' variation. The stress peaks, as shown in Fig 10, are localized in the tungsten layer in front of the scallops' locations, which explains the higher sensibility of the stress responses to the equipment parameters variations.

Fig. 11 presents a Pareto graph of the normalized effects of the most relevant equipment parameters involved in the Resistance and Capacitance responses. The Dep 1 and Etch 1 parameters are related to the first loops of the DRIE step generating small scallops, while Dep 2, Etch 2, and Etch 3 are dedicated to the second sequence of deposition and etching loops generating the larger scallops.

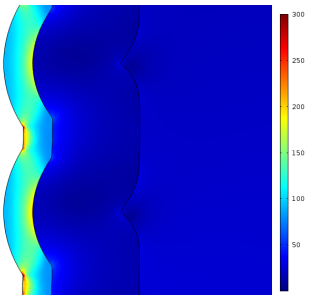


Fig. 10. Stress location along TSV sidewall structure

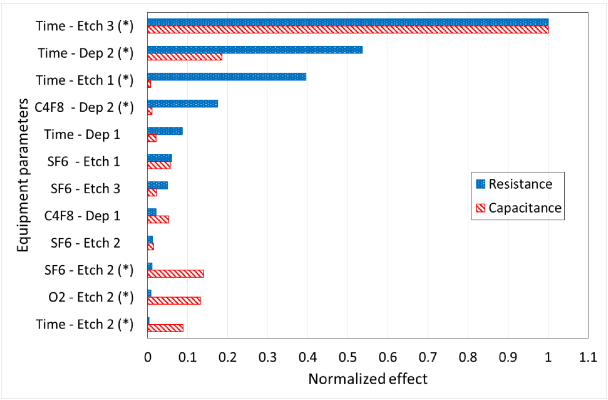


Fig. 11. Pareto graph of the effects of the most relevant equipment parameters involved in the resistance and capacitance responses.

We can observe that the parameters generating the larger scallops have the strongest impact on R and C responses (quantities related to Dep 2, Etch 2 and Etch 3). This is due to the larger amount of scallops involved in that sequence compared to the first sequence generating scallops only in the first micrometers of the TSV (as depicted in Fig. 10).

The aim of the full methodology is to provide a SPICE meta-model of the TSV sub circuit including variability of the SPICE model parameters (R, C, and L) as a function of the equipment parameters. Thus, we can select from Fig. 11 seven most relevant equipment parameters (* symbol), which allows the synthesis of a full TSV for the generation of empirical models using the RSM technique.

VI. Conclusion

We have proposed a full comprehensive methodology for the analysis of the impact of the most relevant parameters involved in TSV formation with a specific focus on the DRIE process. This methodology combines several techniques from inline measurement of the equipment parameters' variation and statistical analysis of their distribution, with the use of advanced statistical tools for the analysis of the effects.

A specific simulation flow has been proposed to handle the equipment parameters' variations and distribution inside the plasma chamber and the direct simulation of the DRIE processing step.

The analysis of the electrical parameters of the resulting TSV structures has highlighted seven most relevant equipment parameters. This first selection was necessary in order to limit the number of global simulations which must be performed, and to start the second part of the full methodology consisting of the quantification of the electrical parameters of the TSV as a function of the equipment parameters. This quantification can be used for the generation of meta-models at a SPICE level analysis for the study of the TSV variations at circuit level.

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