

An Advanced Electro-Thermal Simulation Methodology For Nanoscale Device

L. Wang^a, T. Sadi^a, M. Nedjalkov^b, A.R. Brown^c, C. Alexander^c, B. Cheng^c, C. Millar^c, A. Asenov^{a,c}

^a School of Engineering, University of Glasgow, Glasgow G12 8LT, U.K.

^b Institute for Microelectronics, TU Wien, Gußhausstraße 27–29/E360, 1040 Wien, Austria

^c Gold Standard Simulations Ltd, 11 Somerset Place, Glasgow, G3 7JT, U.K.

e-mail: Liping.Wang @glasgow.ac.uk

ABSTRACT

In this work, we propose an advanced electro-thermal simulation methodology for nanoscale device based on a macroscopic model for acoustic and optical phonon energy transfer, which will be demonstrated on an SOI FinFET example.

INTRODUCTION

With the continuous scaling of semiconductor transistors down to nanoscale regime, further driven by the emerging novel architecture such as FinFETs, thermal transport has become one of the major concerns for in terms of performance and reliability. Modeling and analysis of self-heating effects in nanoscale devices such as FinFETs have attracted increasingly more interests [1-3]. Recently we have developed a thermal simulation module [4], implemented in GSS ‘atomistic’ simulator GARAND [5], based on the solution of the coupled Heat Flow, Poisson, and Current Continuity Equations (CCE). In this work, we are going to further incorporate an advanced methodology into GARAND for electro-thermal simulation of FinFETs.

MODEL AND EXAMPLE

The advanced electro-thermal simulation methodology for nanoscale device is based on a macroscopic model [6]. The model for acoustic and optical phonon energy transfer involves the temperature of electrons, acoustic phonons and optical phonons T_e , T_A and T_o , and the relaxation times between them τ_{e-o} , τ_{e-A} and τ_{o-A} respectively. These can be naturally implemented in Monte Carlo (MC) simulation, however, in the cost of long computational time. If focusing on the stationary state, these equations can be simplified. Starting from the energy transfer equations, a new

equation in the form of new heat flow equation can be derived, which includes the terms about T_e and T_A .

$$\nabla(k_T \nabla T_A) = -C_o \frac{T_o - T_A}{\tau_{o-A}} - \frac{3nk}{2} \frac{T_e - T_A}{\tau_{e-A}} \quad (1)$$

$$= -C_o \left(\frac{3nkT_e + nm_e v_d^2 - 3nkT_A}{2\tau_{e-o} C_o + 3nk\tau_{o-A}} \right) - \frac{3nk}{2} \frac{T_e - T_A}{\tau_{e-A}}$$

where n is the electron density, v_d is the drift velocity, and C_o is heat capacities. This can be coupled within Drift-Diffusion framework, which is more computationally efficient. The electrons temperature T_e can be pre-calculated by MC simulations and a lookup table of T_e with respect to E can be constructed. Then the coupled Poisson, CCE, and energy transfer equations can be solved iteratively. At each iteration, T_e will be refreshed as well as recalculation of T_A . Thermal conductivity in the refined fin region will be modeled by position and temperature dependent formula. The flow chart of the methodology is illustrated in Fig. 1. An SOI FinFET example (schematics as shown in Fig. 2) is used as a testbed for the advanced methodology. It consists of complex 3D structure and material composition, as shown in Fig. 3. Lattice temperature and potential distributions obtained from coupled Heat Flow, Poisson, and CCE will be used as the initial conditions for the advanced electro-thermal simulation, as shown in Fig. 4 (a) (b).

CONCLUSION

An advanced electro-thermal simulation methodology for nanoscale device based on a macroscopic model for acoustic and optical phonon energy transfer is being implemented in GSS ‘atomistic’ simulator GARAND. A full scale simulation on SOI FinFET will be presented following the complete implementation.

ACKNOWLEDGMENT

The research leading to these results has received funding from the European Union Seventh Framework Programme (FP7/2007 – 2013) under grant agreement no. 318458 SUPERTHEME.

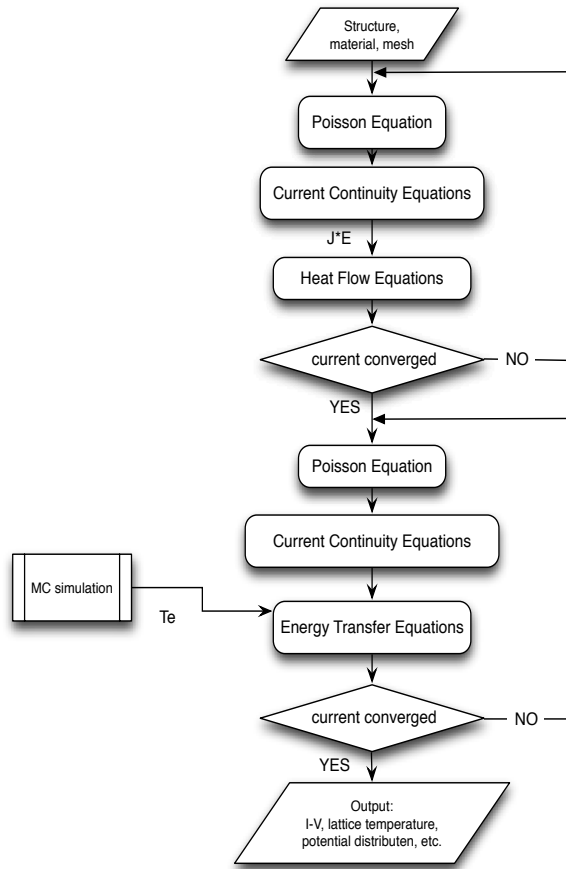


Fig. 1. Flow chart for the advanced electro-thermal simulation methodology.

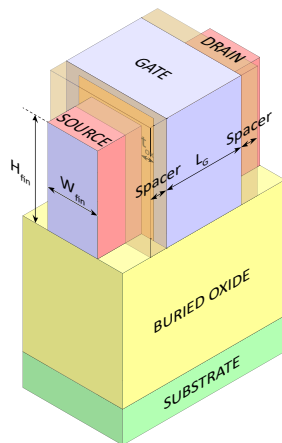


Fig.2. Schematics of SOI FinFET

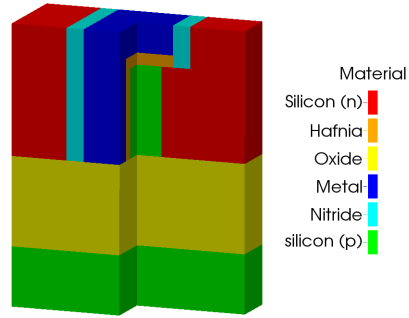


Fig. 3. Materials and structures of the SOI FinFET's electrical simulation domain, showing 3 quarters.

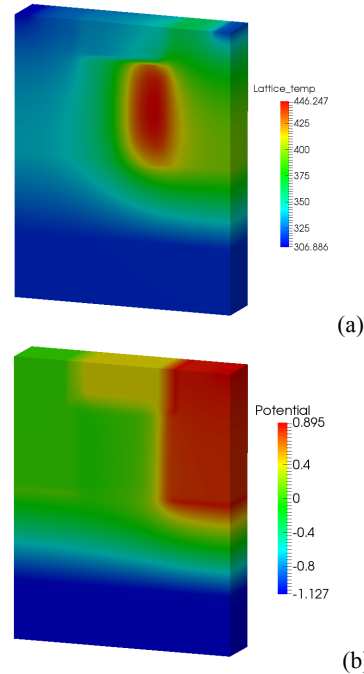


Fig. 3. (a) Lattice temperature distributions and (b) potential distribution at high drain and high gate biases resulted from coupled Heat Flow, Poisson, and Current Continuity Equations, which will be the initial conditions for the advanced electro-thermal simulation.

REFERENCES

- [1] I. N. Adisusilo, K. Kukita, and Y. Kamakura. "Analysis of Heat Conduction Property in FinFETs Using Phonon Monte Carlo Simulation," SISPAD 2014, pp.17-20, Sep. 2014.
- [2] S. Kolluri, K. Endo, E. Suzuki, K. Banerjee. "Modelling and analysis of self-heating in FinFET devices for improved circuit and EOS/ESD performance," IEDM 2007, Dec 2007.
- [3] T. Sadi, R.W. Kelsall and N. J. Pilgrim, "Electrothermal Monte Carlo Simulation of Submicrometer Si/SiGe MODFETs", IEEE Trans. Electron. Dev., Vol. 54, No. 2, pp. 332-339, 2007
- [4] L. Wang, A. R. Brown, et al. "3D Coupled Electro-Thermal FinFET Simulations Including the Fin Shape Dependence of the Thermal Conductivity," SISPAD 2014, pp.269-272, Sep. 2014.
- [5] GARAND Statistical 3D TCAD Simulator [Online]. Available: <http://www.GoldStandardSimulations.com/products/garand/>
- [6] K. Raleva, D. Vasilevska, S. M. Goodnick, M. Nedjalkov. "Modeling Thermal Effects in Nanodevices," IEEE Trans. Electron. Dev., Vol. 55, No. 6, pp.1306-1316, June 2008.