Experimental Evidences and Simulations of Trap Generation along a Percolation Path

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***Abstract*— In this paper we present experimental results of single trap impact on bulk MOSFETs, shedding light on counter intuitive behavior when increasing the gate bias. Using a well calibrated 3D TCAD model, statistical simulations at atomistic level are performed, demonstrating that the interactions between the traps and the percolation path are responsible for the unexpected bias dependences of the trap impact and therefore that a trap generation enhanced by higher current densities along this path can explain measured data.**

I. INTRODUCTION

With downscaling Statistical Variability (SV) became a major threat to devices and circuits performances. However on the top of this built-in variability a Time Dependent Variability (TDV) concern arose from oxide wear-out, leading to further reduction in design margins [1] and requiring the development of specific tools and methodology towards a variability and reliability aware CMOS design [1-4].

Whereas a self-averaging continuous degradation was observed for larger devices, the drastic reduction in dimensions has highlighted the discrete degradation nature associated with discrete charge trapping events [5-7]. Moreover experimental evidences identified Random Telegraph Noise (RTN) and Bias Temperature Instabilities (BTI) as two different expression of the same phenomenon [5-11]. Charge trapping is strongly interacting with SV both in terms of its electrostatic impact and its dynamics [10]. For planar bulk MOSFETs this is mainly due to the percolative behavior of the current. Indeed the channel energy barrier between source and drain is strongly affected by discrete dopants number and positions, defining peaks and valleys of the potential along which the current percolates [12]. Therefore a single trap can induce a drastic change in the conduction by blocking a dominant source to drain percolation path [10- 13].

Extensive work have been presented in the past years to assess this effects [3, 11, 14], aiming to reproduce RTN and BTI impacts at circuit level, including their dependence in bias and time. Beside the bottom-up TCAD methodology presented in [11, 15], traps impact and dynamics distribution have been derived from measurement [8, 16, 17] and injected into circuit level workload dependent model [14]. However the bias dependence of the interactions between SV and TDV

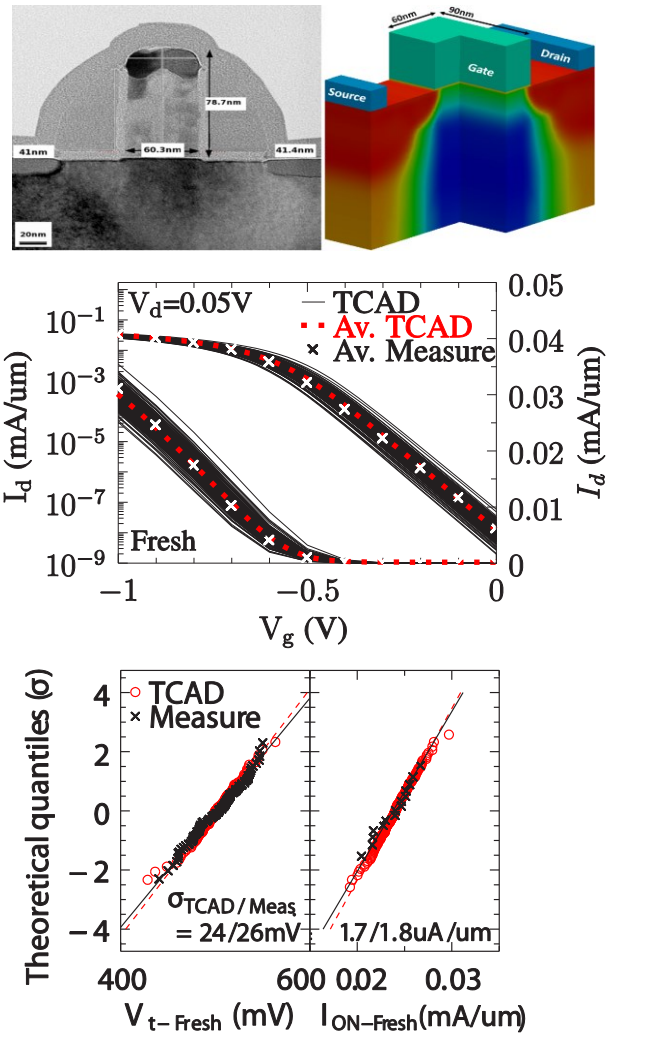

Figure 1. The TCAD model (upper right) is calibrated against measurement by combining imagery techniques such as Transmission Electron Microscopy (upper left) and electrical characterization in an iterative process until a good agreement has been reached (middle), including Statistical Variability (bottom).

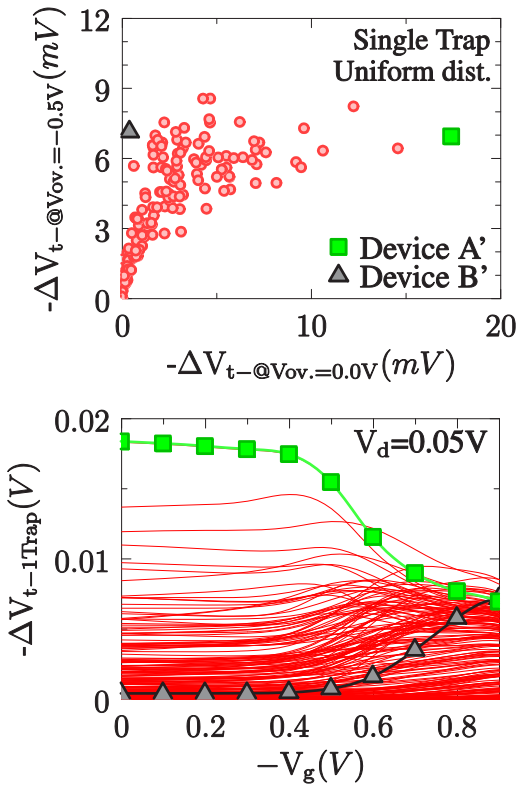

Figure 2. Single charged trap impact at low and high overdrive biases ($V_{ov}=V_{gate}-V_{threshold}$) voltage for a uniform distribution of traps over the channel area (top) and bias dependence of single trap impacts (bottom). Extreme devices A' and B', presenting the largest bias dependence are enlighten.

is not fully understood [8, 13, 17] and a combination of statistical TCAD simulations and experimental evidences is required to fully unveil this phenomenon. As illustrated in Fig.1, a fully calibrated TCAD model including SV is used in this work to investigate the bias dependence of traps impact on a statistical device sample. From the comparison with experimental data we propose an alternative distribution of traps, proven to be closer to silicon measurement.

II. METHODOLOGY

A 60x90nm long and wide PMOSFET transistor is fabricated and characterized by IMEC. It features a 2.2nm thick silicon oxide under a polysilicon gate. As detailed in [18, 19] an extensive calibration is performed, involving Transmission Electron Microscopy, Spread Sheet Resistance imagery as well as statistical electrical characterization in an iterative process. Back-bias and threshold voltage roll-off measurements and simulations are compared in order to validate the vertical and horizontal doping profiles. Fig.1 demonstrates the quality of the obtained TCAD model, not only for the average measured device but also for the measured SV and reliability [18, 19]. The 3D 'atomistic' density gradient corrected drift-diffusion simulator GSS GARAND [20, 21] is used to simulate the device sensitivity to oxide degradation, in combination with our in house reliability module [15], using a sample of 200 devices suffering from SV. Individual traps induced steps in the threshold voltage

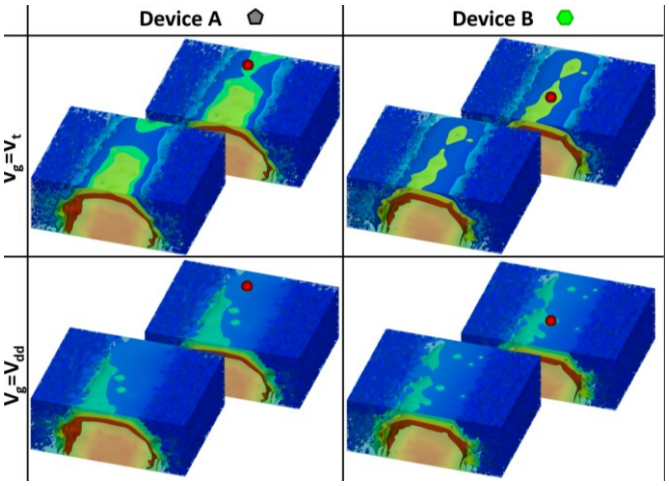

Figure 3. Source to drain percolation path illustrated by the potential in the channel 1nm away from the interface at $V_g=V_t$ for the upper line and $V_g=V_{dd}$=0.9V in the lower line. Fresh devices percolation paths are shown in the foreground and traps impacts on the background. Devices A and B correspond to those indexed in Fig.5.

presented in Fig.4 have been measured during the NBTI relaxation phase [8, 17]; they present a typical exponential distribution due to their interactions with the percolation path [5, 10, 17]. Measured traps characteristics are presented in [8, 17] and well compare to the simulated ones in Fig. 2 and 5.

III. RESULTS

In a first step, single traps are uniformly distributed at the channel/oxide interface of the devices. Following [8], the trap impact is evaluated as a shift in the gate bias named in the following ΔV_t. As can be seen in the upper Fig.2, a trap can have a large impact at $V_g=V_t$ and a low impact at higher gate bias. On the contrary some traps are strongly impacting the device at high gate bias but have a weak effect at lower biases. The lower fig.2 illustrates the full trap impact characteristics, from which different dependence in V_g can be identified: increasing, decreasing or a combination of both as measured in [8]. This behavior is explained by the source to drain percolation path dependence on V_g. Indeed as can be seen in Fig.3, on one hand the most conductive part of the channel can move with the bias and on the other hand the percolation path is much less localized at higher gate biases, because of the dopants screening by the gate. For example for the device A the trap is located exactly on the top of the percolation path at V_t, inducing a large shift, but far enough from it at higher biases, leading to a smaller shift. On the contrary for device B, the trap is far away from the percolation path at V_t but close enough at high gate bias to affect it.

This results in the distributions of traps impact illustrated in the upper Fig.4, in which the average impact is slightly increasing with V_g, whereas the maximum impact decreases. On the contrary, the measured trap-induced step distributions (Fig.4 bottom) present no dependence on V_g. We can conclude that the simulated trap distributions do not reproduce realistic traps interactions with the percolation path and we should aim for higher maximum impact at large gate biases and for an increased average impact at lower biases.

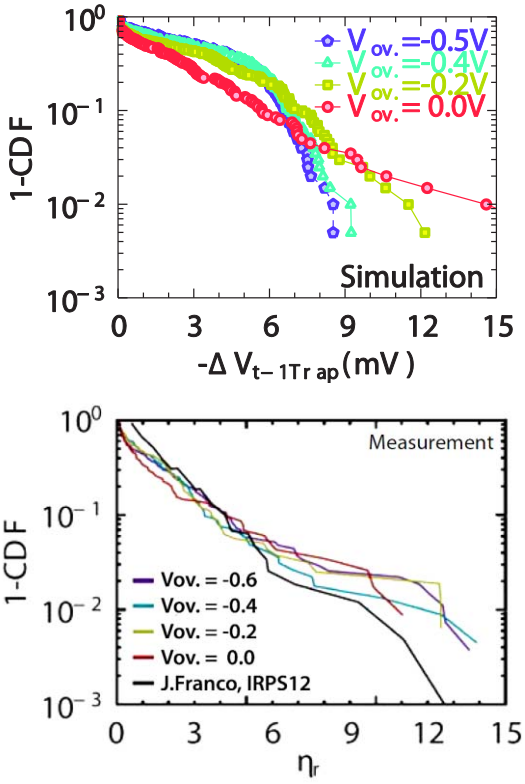

Figure 4. ΔV_t distributions for an increasing gate bias for uniformly distributed traps in the TCAD simulation (top) and for measured data on the same device (bottom).

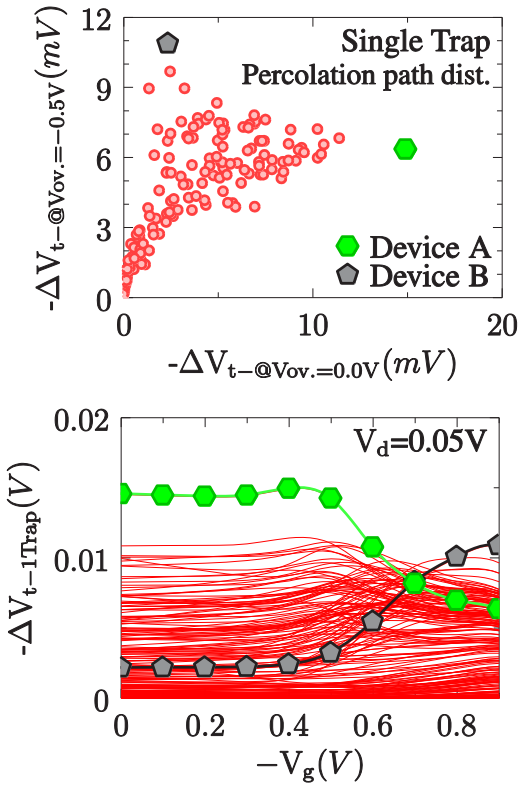

Figure 5. Single charged trap impact at low and high gate biases for a traps distribution along the percolation path (top) and bias dependence of single trap impacts (bottom). Extreme devices A and B, presenting the largest bias dependence are enlighten.

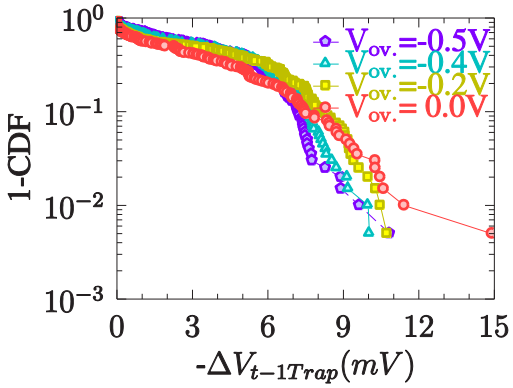

Figure 6. ΔV_t distributions for an increasing gate bias for traps distributed along the percolation path.

To do so, instead of considering uniformly distributed traps all over the channel area, we add them in a post processing step, after having simulated the fresh device at high gate bias and identified the most conductive part of the device channel. Then the average trap distribution along the device remains the same but is weighted by the current density to select the traps position across the channel. The weighting factor is obtained by extracting and normalizing a current density cutline across the channel, 1nm away from the oxide interface which corresponds to the maximum of the inversion layer. After having randomly selected the trap position along the channel, its position across the channel is randomly selected among the positions where the current density is larger than 80% of the current density maximum along this line. In this way we make sure that the trap impact is higher at higher gate bias. A more advanced way of selecting traps positions would be to use the rejection technique based on the current density map at the interface or even better based on the temperature; this will be developed in the near future. It is worth noting that this degradation scenario is actually very realistic: the parts of the device in which the current flows are locally enduring self-heating and thermal stress. Results are presented in Fig. 5 and 6. As expected we increased the maximum traps impact at high biases and we balanced the impacts at low and high gate bias, therefore obtaining a reduced bias dependence of the traps impacts. Fig.6 demonstrates that this trap distribution along the percolation path results in a better agreement with the measurement shown in Fig.4. However the slope of the distributions are now slightly bended because to the presence of many low impact traps; this should be readily solved with an additional refinement of the simulation setup by reducing the occurrence of trapped charge in the close proximity of source and drain electrodes, where their impact and gate bias dependences are minimal.

IV. CONCLUSION

In this paper we are shedding light on the bias dependence of reliability interactions with SV. Trap impact characteristics are investigated and explained using statistical TCAD simulations and the results are compared with experimental measurements. Discrepancies between measurement and simulations at high gate bias demonstrate the uniform distribution of traps over the channel area to be an improper

choice. We implement an original traps generation method, in which their position across the channel is weighted by the current density, so that the traps are correlated to the percolation path. As a result we reduced the bias dependence of the trap induced step height distributions and we obtain a more realistic behavior of the simulated degradation.

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