The Defect-Centric Perspective of Device and Circuit Reliability—From Individual Defects to Circuits

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Abstract—As-fabricated (time-zero) variability and mean device aging are nowadays routinely considered in circuit simulations and design. Time-dependent variability (reliability variability) is an emerging trend that needs to be considered in circuit design as well. This phenomenon in deeply scaled devices can be best understood within the so-called defect-centric picture in terms of an ensemble of individual defects and their time, voltage, and temperature dependent properties. The properties of gate oxide defects are discussed and it is shown how these properties can be used to construct time-dependent variability distributions and can be propagated up to transistor-level circuits.

Keywords: variability, reliability, defects, RTN, BTI, HCI, circuit simulations

I. Introduction

Variability of as-fabricated (i.e., time-zero) parameters of modern VLSI devices has been considered in circuit design tools for some time (Fig. 1a). With the exception of TDDB [1], circuit lifetime estimation due to FEOL degradation (aging) mechanisms is presently based on projecting only the *mean* parameters shifts (Fig. 1b). The combination of both hitherto orthogonal efforts used in determining circuit operating margins is illustrated in Fig. 1c.

It has long been accepted that in mechanisms associated with FET *gate* current, such as SILC and TDDB, only a handful of defects will cause significant current increases and can bridge the gate oxide, presently ~ 1 nm thick. Similarly, as lateral dimensions of VLSI devices are reduced toward the 10 nm range, just a few stochastically-behaving defects present in the FET gate oxide will have sizable impact on the *drive* current as well [2,3]. We have previously claimed that this will lead to *time-dependent* variability in the associated degradation mechanisms, such as RTN, BTI, and HCI [4,5]. This paradigm shift is illustrated in Fig. 2. Consequently, we argue that to estimate the full device and circuit parameter distributions at the end of useful lifetime, time-zero and time-dependent statistics need to be combined, as illustrated in Figs. 1d-f.

Since only a handful of defects will be responsible for the time-dependent effects in each deeply-scaled device, we claim that understanding of degradation mechanisms at individual defect level is essential for simulations of time-dependent variability in circuits. This notion is the basis of the so-called *defect-centric* picture and is hierarchically illustrated in Fig. 3. We will start by reviewing the properties of individual defects and show how to propagate these properties to higher hierarchical levels. We then show how, based on this understanding, the time-dependent distributions (Fig. 1e) can be constructed and propagated to the circuit level. Finally, a defect-centric transient circuit simulation is described.

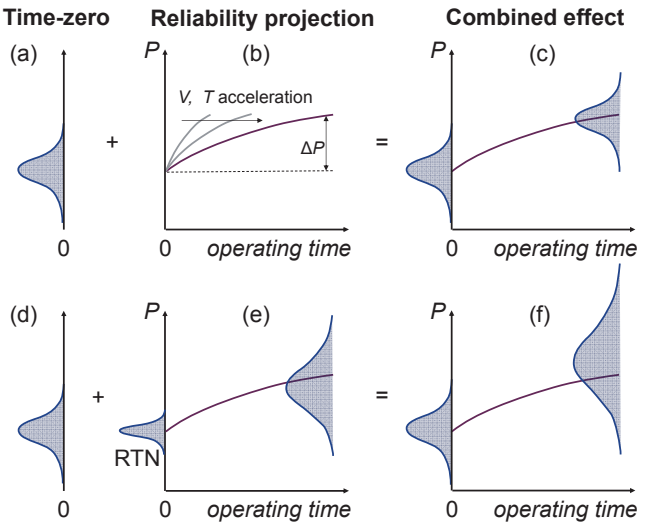

Fig. 1: A schematic representation of time-zero and time-dependent effects considered in circuit design. (a-c) Presently, time-zero variability of a device parameter *P* is considered together with the projection of the *mean* parameter shift Δ*P* (obtained by reliability engineers through bias and temperature accelerated tests) during aging. (d-f) Time-dependent variability is also considered, in contrast to (a-c).

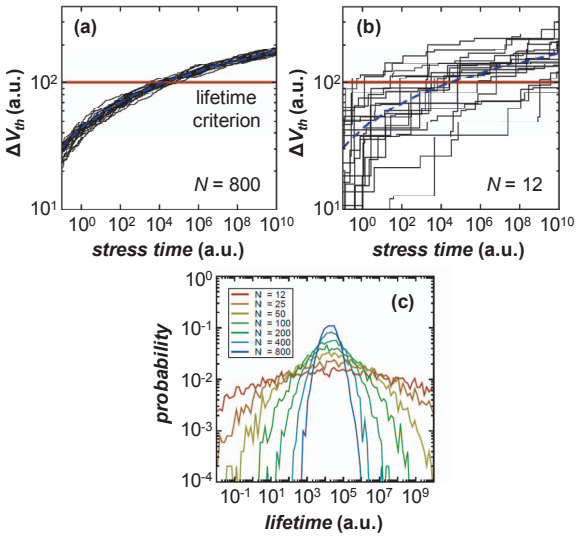

Fig. 2: (a) The random properties of many defects N_T in large devices average out, resulting in a well-defined lifetime while (b) the stochastic nature of a handful of defects in deeply-scaled devices becomes apparent, (c) resulting in large variation in the lifetime. This also illustrates the paradigm shift in projecting reliability in deeply scaled devices (Figs. 1b and 1e) [4].

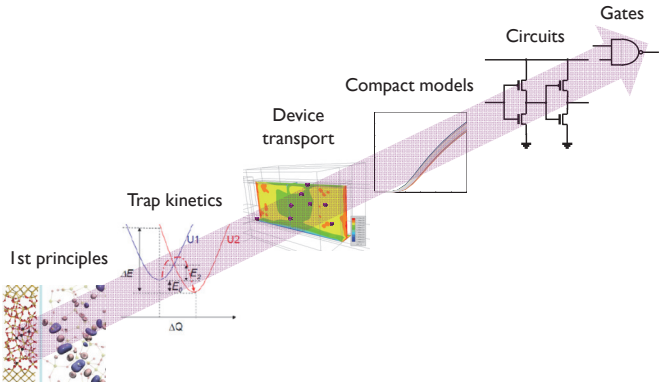

Fig. 3: Hierarchical levels of the defect-centric picture: Understanding of defect properties at the atomic level [6] can be propagated up to circuit design.

II. Device Variability

Generally, the time-zero variability is due to random and systematic (process-induced) effects [7, 8]. Limiting ourselves to FET threshold voltage V_{th}, it has been observed to follow the Normal distribution up to about ±6.5σ [9].

A. Time-dependent variability

Similarly to time-zero variability, time-dependent variability also has random and systematic components [10-13]. An example of time-dependent variability due to gate-oxide breakdown (TDDB) is illustrated in Fig. 4 [14]. Not only is the time-to-breakdown widely distributed (Fig. 4a), but so is the impact on the (ring-oscillator) circuit after the breakdown occurs (Fig. 4b).

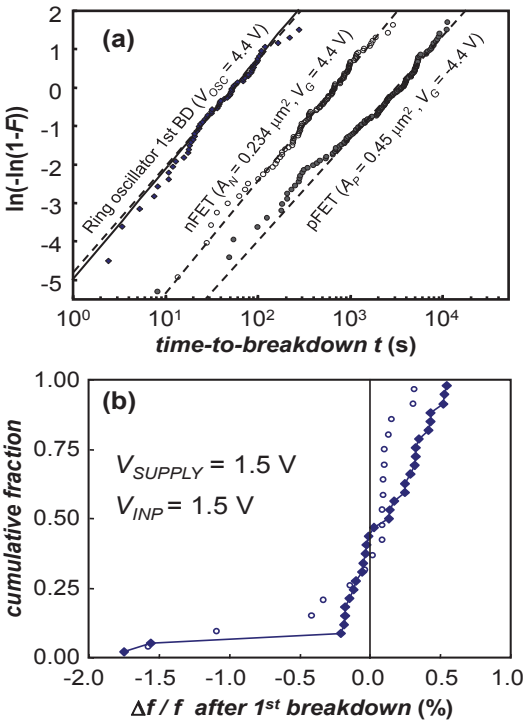

Fig. 4: The measured cumulative distribution of the time-to-first-breakdown of ring oscillator circuits (diamonds) is excellently matched by the distribution F_{OSC} (solid line), obtained by combining and scaling t_{BD} distributions of individual n- and pFETs (circles) to the total number of n- and pFETs under stress. (b) The measured distributions of changes in output frequency after the first hard gate oxide breakdown (solid diamonds) are well matched by SPICE simulations of a ring oscillator with one "broken" nFET represented by an equivalent circuit for nFET after gate oxide breakdown (open circles) [14].

Because of the limited number of defects N_T present in modern deeply downscaled FETs (e.g., N_T = 10 with defect density 10^{12} cm^{-2} and gate area 10^3 nm^2), other degradation mechanisms, such as RTN/BTI and HCI will be distributed as well [2,5,15]. Based on this simple fact we claim that *the time-dependent variability in deeply scaled devices can be best understood in terms of an ensemble of individual defects and their time, voltage, and temperature dependent properties.* This is indeed the underlying foundation of the defect-centric approach. To illustrate this approach, we now discuss some of the relevant properties of individual defects.

B. Properties of individual defects

In the most general view, the properties of each gate oxide defect (trap) are formed by the spatial location of the defect in the FET as well as the immediate configuration of atoms around it [6]. Because of the amorphous nature of the presently-used gate dielectrics, each defect will have substantially different properties, such as the ground level and the relaxation energy.

All these properties will then project into two main sets of parameters usable at higher abstraction levels, namely i) the defect time constants and ii) the defect impact on the FET parameters. An illustration of distribution of these properties for several defects in a single device is given in Fig. 5.

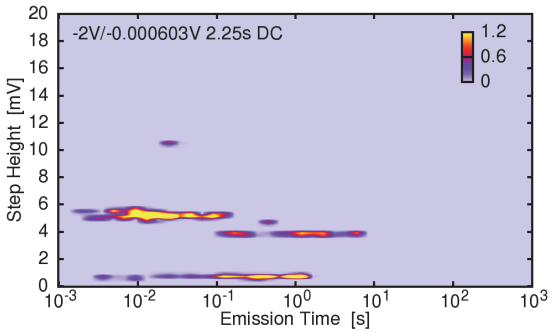

Fig. 5: Time-Dependent Defect Spectroscopy (TDDS) spectrum of three traps in a single FinFET device. The distribution of emission times and impacts on the FinFET V_{th} ("step height") is apparent. The TDDS technique was developed specifically within the defect-centric approach [16].

i) The time constants are typically the *mean times* for the defect to *capture* and *emit* a carrier. These vary drastically from defect to defect, from at least µs to months. In addition to that, each capture and emission event will be stochastic and hence *distributed* around the respective mean value (cf. Fig. 5). These time constants τ_c and τ_e will furthermore depend strongly on the FET biases and temperature, as illustrated in Fig. 6, and understood in the framework of the Non-radiative Multi-Phonon (NMP) theory [18]. These dependences will again differ substantially from defect to defect. A convenient way to describe the temporal properties of a large ensemble of defects is then the so-called CET map (Fig. 7) [19].

The concept of time constants characterizing individual traps can be easily extended to defect generation, e.g. by assuming additional time to convert a precursor site into a trap [21].

ii) A defect can impact one or multiple FET properties. It can e.g. act as a "stepping stone" between the FET body and the gate and thus contribute to gate leakage [22-24], or it can influence the channel current when charged [25]. Again, the impact will be widely distributed. E.g., the impact of charged defects on the drain current, for the sake of convenience converted into the threshold voltage shift ΔV_{th}, is approximately exponentially distributed (Fig. 8).

The expectation value of this distribution, η, represents the *mean* impact of a single trap and is crucial parameter in the defect-centric model. It scales as

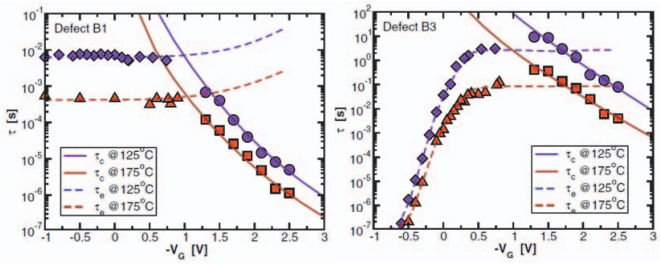

Fig. 6: Voltage and temperature dependences of τ_c and τ_e for two different defects. Considerable qualitative and quantitative differences between the traps are apparent [17].

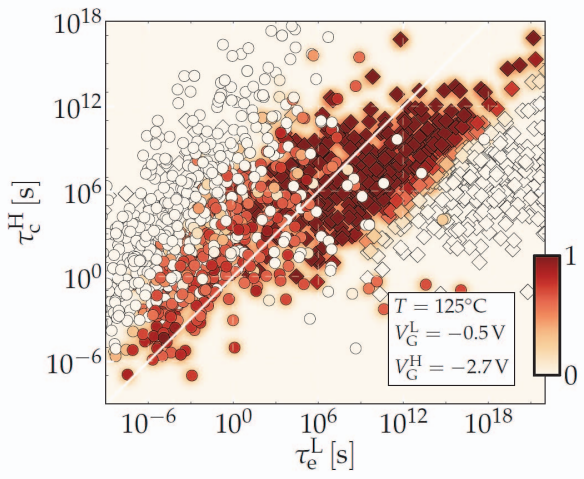

Fig. 7: Based on $\tau_c(V_G)$ and $\tau_e(V_G)$ dependences (cf. Fig. 6) of a population of defects, a CET map can be computed [19,20]. $\tau_c^H = \tau_c(V_G^H)$ and $\tau_e^L = \tau_e(V_G^L)$ define where a defect contributes in the CET map and the average contribution of a defect to V_{th} (0-1 gradient scale) is given by its equilibrium occupancy difference and its distance from the substrate [20].

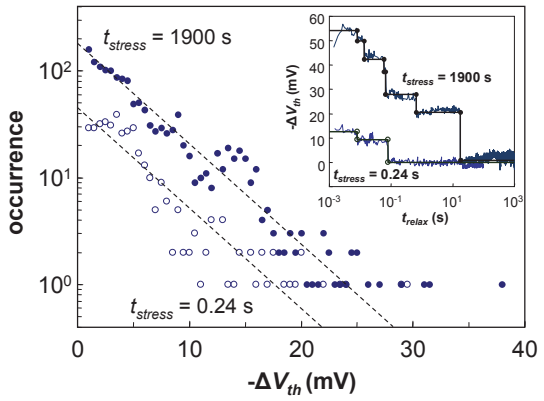

Fig. 8: Histograms of NBTI transient step heights for 72 planar Si/SiON devices show an exponential distribution. Inset: Two typical NBTI relaxation transients corresponding to the same stress times. Individual down-steps are marked with abscissas [2].

$$\eta \cong \frac{t_{inv} N_A^{\alpha}}{A_G}, \qquad (1)$$

where t_{inv} is the oxide thickness corresponding to capacitance in inversion, A_G the area of the device channel, and N_A the channel doping. However, other sources randomizing the channel potential are expected to take the place of N_A in low-doped channel devices [26]. The exponent α has been observed to be around 0.5 in simulations [27,28]. The dependence of A_G is confirmed in Fig. 9 [29]. In nanolaminate high-k dielectrics used in modern FET devices, each layer will contribute with its own η value and the resulting distribution will be bi- or multimodal [30-33].

The impact of a charged defect is obviously not limited to $V_G = V_{th}$, and can vary with gate and drain biases. The V_G dependence is illustrated in Fig. 10 for both the impact on drain and gate currents.

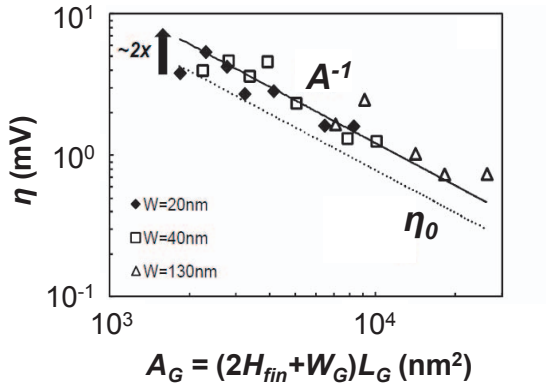

Fig. 9: The average impact per trap η as A_G^{-1} in pFinFETs (high-k/MG, $t_{inv} \approx$ 1.7nm) with varying fin width W_G and gate length L_G (fin height H_{fin} is fixed). Each point is extracted from a distribution such as those in in Fig. 8. The value of η is ~2× higher than the expected ΔV_{th} for a single charge from a charge sheet approximation $\eta_0 = q/C_{ox}$ [29].

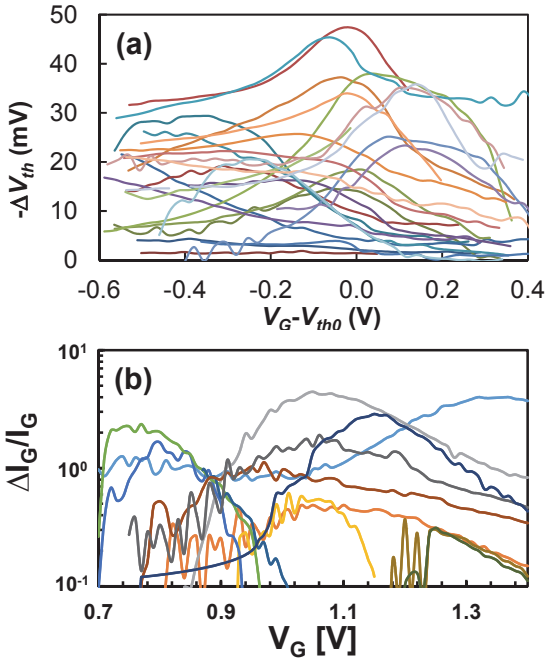

Fig. 10: (a) Different $\Delta V_{th}(V_G)$ defect characteristics are found when measuring 30 different (but nominally identical) pFETs before and after the capture of a single hole [29]. (b) Different $\Delta I_G(V_G)$ characteristics are found when measuring several (but nominally identical) nFETs before and after the activation of a single defect [24].

C. *Multiple defects: Defect-centric statistics*

Identical stress of a population of deeply scaled devices will result in a *distribution* of FET parameter shifts, as illustrated in Fig. 11 (cf. Fig. 2b). Note that in a population of ~400 devices, ΔV_{th} of some devices after identical BTI stress is negligible, while other devices shift by ~ 100 mV(!). This contrasts with the large-area devices of the past, in which identical stress resulted in identical degradation (cf. Fig. 2a). Understanding of BTI and HCI distributions in deeply-scaled devices requires the new, defect-centric approach. The information presented so far in the previous section is sufficient to achieve this goal.

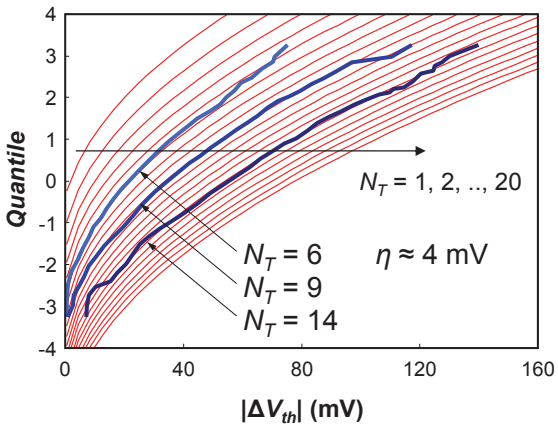

Fig. 11: Total ΔV_{th} distribution (Eq. 2) for the average number of defects N_T from 1 to 20 (thin lines) rescaled to fit experimental distributions from Fig. 10 of Ref. [34], with the corresponding values of N_T and η readily extracted.

As the individual gate oxide defects charge during operation, corresponding to RTN/BTI and/or HCI degradation, they will concurrently modify the channel current [35]. To describe their combined impact on V_{th} in a population of FETs, we simply assume that the number of charged defects varies from device to device following the Poisson statistics with the mean number of defects per device N_T. When combined with the ΔV_{th} exponential distribution of each contributing charged defect, it can be shown that the resulting statistics will have a cumulative distribution given by [2,3,36]

$$H_{\eta,N_T}(\Delta V_{th}) = \sum_{n=0}^{\infty} \frac{e^{-N} N^n}{n!} \left[1 - \frac{n}{n!} \Gamma\left(n, \frac{\Delta V_{th}}{\eta} \right) \right] . \quad (2)$$

Note that the above ΔV_{th} distribution is controlled by only two parameters, η and N_T, where the latter is simply linked to the defect density N_{ot} as $N_T = N_{ot} A_G$. As is apparent from Fig. 11, Eq. 2 excellently describes the measured distributions.

Having an analytical description of the ΔV_{th} distribution has several advantages. It allows to i) make projections to high percentiles without the need to measure billions of devices, and ii) provide a crucial link between the first two statistical moments of the ΔV_{th} distribution [2,3,36]

$$\sigma^2_{\Delta V_{th}}(t) = 2\eta \left\langle \Delta V_{th}(t) \right\rangle . \quad (3)$$

$\langle \Delta V_{th}(t) \rangle$ is the mean shift of the population, linked with the two parameters of Eq. 2 as $\langle \Delta V_{th}(t) \rangle = \eta\, N_T(t)$. $\Delta V_{th}(t)$ is projected to operating conditions using established acceleration techniques. Eq. 3 also allows to extract η directly from measured ΔV_{th} distributions (typically at accelerated conditions), without having to analyze the statistics of individual steps. To that end, techniques based on local arrays [11,33] and matched-pairs [12,13] have been developed to filter out the systematic time-dependent variability component.

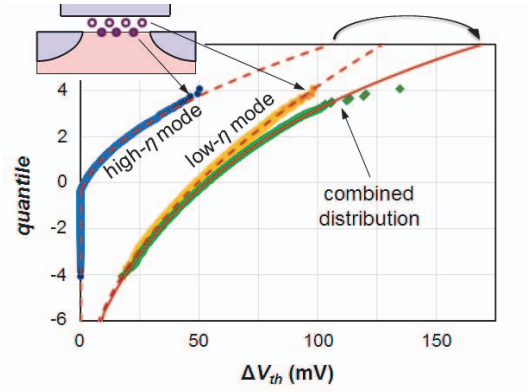

Fig. 12: Bimodal defect-centric distribution ΔV_{th} corresponding to CHC stress: Monte Carlo and analytic fit [5,33]. The high-σ tail of the full distribution is controlled by defects at the substrate (high η; inset: solid symbols).

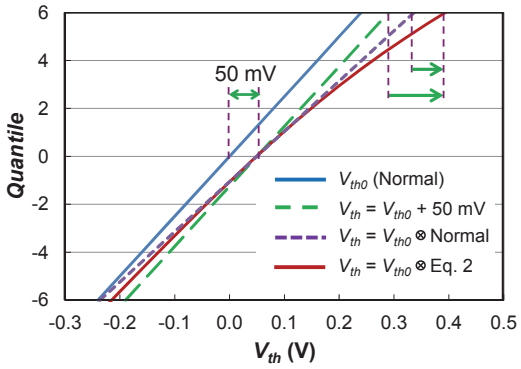

Fig. 13: Three ways of adding time-dependent variability to time-zero distribution (solid straight line): i) a simple shift of $\langle \Delta V_{th}(t) \rangle$ in all devices (dashed line), ii) a Normal (Gaussian, dotted line), and iii) the defect-centric statistics given by Eq. 2 (solid curve). Discrepancies with respect to the defect-centric model at 6σ are demarcated [36].

In devices with high-k dielectrics, trapping in multiple layers will be combined, resulting in a bi- or multi-modal distribution [32,33]. The high-percentile tail may be controlled by the defects low in density, but with high η value (i.e., closer to the substrate), as illustrated in Fig. 12 [5].

D. Combined Time-Dependent Variability

As illustrated in Fig. 1f, the *total* distribution of a FET parameter after operation at nominal operating conditions is a convolution of time-zero and time-dependent distributions [37]. Fig. 13 illustrates this convolution for 3 different cases: i) no time-dependent variability (uniform shift, corresponds to Fig. 1c), ii) Normally-distributed time-dependent variability [38], and iii) Eq. 2 (defect centric). Note that the defect-centric model (Eq. 2) predicts larger V_{th} shifts at high percentiles.

We also note that in some cases, a correlation between time-zero and time-dependent variability may exist. This is because devices with higher V_{th} may degrade less at fixed gate bias as both the oxide field and self-heating effects driving the degradation will be lower [39]. Such correlations need to be factored into the convolution discussed in this section.

III. Application to Circuits

The conventional reliability margins in modern technologies generally decrease due to the higher electric fields, while simultaneously, voltage-overdriving techniques are employed by designers to maximize performance [31]. Consequently, more elaborate reliability projection methods are needed to guarantee product reliability. The methods are based on the realization that i) in real circuits, the devices seldom see constant stress at the supply voltage throughout their entire operating lifetime, as has been assumed in the past conservative technology reliability qualification, ii) the failure criterion for each device will be different, depending on its function in the circuit, and iii) the time-dependent variability needs to be considered in deeply-scaled technologies, as argued hitherto. All of these notions require a *technology*- and *reliability-aware simulation* and *design*.

For the purposes of this paper, the different levels of implementation of device aging in circuit simulations are defined in Fig. 14. Level 1 corresponds to predicting the device degradation by assuming the device operates at a fixed "effective" workload throughout its entire lifetime in the circuit. Level 2, an improvement over Level 1, acknowledges that devices can be exposed to a sequence of different workloads throughout their operation, including e.g. short bursts of data activity (at ns – ms time scales) to "turbo", "sleep", and "off" modes (ms – day time scales) [40]. Implementations of Level 2 range from the so-called reaction-diffusion model [41] to CET map-based (cf. Fig. 7) [42,43]. Level 3 then adds the time-dependent variability parameter distributions, as derived above (Eq. 2), on top of the projected mean parameter shift (cf. Level 3 in Fig. 14 and Fig. 1e) [44-48].

Level 1-3 circuit simulations evaluate the circuit at *static* degradation projected at a specified time. In contrast to that, Level 4 simulation incorporates the *temporal* stochastic behavior of individual traps and allows transient simulations. Level 3 and Level 4 simulations are now discussed.

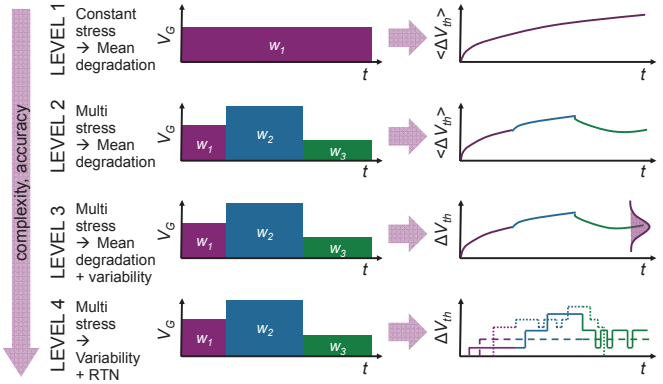

Fig. 14. Complexity/accuracy levels of incorporating device aging (specifically here, the threshold voltage shift) in circuit simulations. The full workload on each device can be *approximated* by a series of phases w_i with duration t, voltage V, duty factor DF, frequency f, and temperature T. (In reality the number of workload phases is typically very large.)

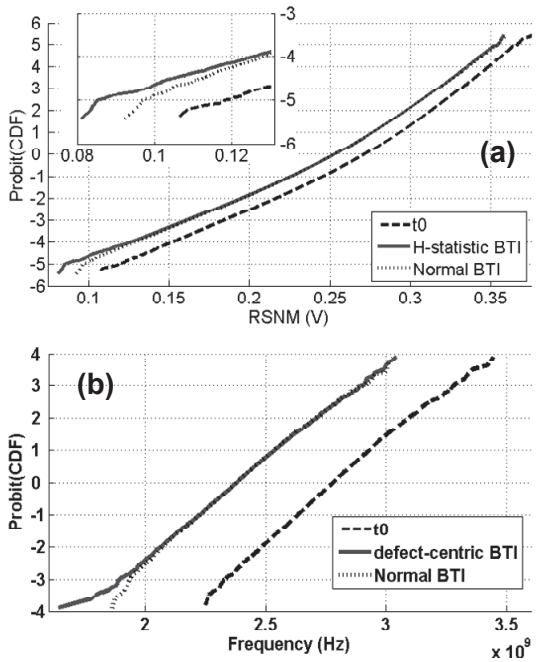

Fig. 15: (a) Probit plot of the Read Signal Noise Margin (RSNM) of 28nm technology SRAM cell for an average 50mV NBTI shift. Inset shows the discrepancy at higher quantiles. (b) Impact of binning at time-zero. Using the yield criterion of *mean-σ* on the ring oscillator frequency distributions results in a wider discrepancy between the defect-centric and Normal degradation statistics [49].

A. Level 3 circuit simulations

The significance of incorporating time-dependent variability and in particular, our defect-centric approach (Eq. 2) in circuit simulations, is addressed in Fig. 15. For high-σ designs, such as large SRAM arrays [50], circuit simulations show that incorporation of time-dependent variability will influence the distribution tails [49], as was already alluded to in Fig. 13. The distribution tails determine the product failure rates in the field and correct incorporation of time-dependent variability is therefore essential.

For low-σ designs, such as logic data paths [38,46,47], we notice that the choice of the time-dependent variability distribution will be visible even at low σ values, if product binning is considered [49]. This is because this standard manufacturing procedure allows the manufacturer to compensate for time-zero variability, which, however, increases the relative weight of time-dependent variability, not present in the product at time-zero. At the moment it appears that the Level 3 approach (cf. Fig. 14 and Figs. 1d-f) has the best chance of being integrated in commercial EDA tools.

To achieve the distributions in Fig. 15, simulations were repeated with the same circuit instantiated with the FET threshold voltages randomly selected from the total distribution (Fig. 13) in each iteration. This brute-force Monte Carlo (MC) technique, however, does not scale well to offer insights into the distribution tails. We have therefore recently developed a fully *non*-MC technique, relying on first describing the circuit with a *response surface*, followed by numerically propagating the total V_{th} distribution (Fig. 13) through it. Using this method, projections to $\pm 7\sigma$ (Fig. 16) can be made with a modest CPU effort [51].

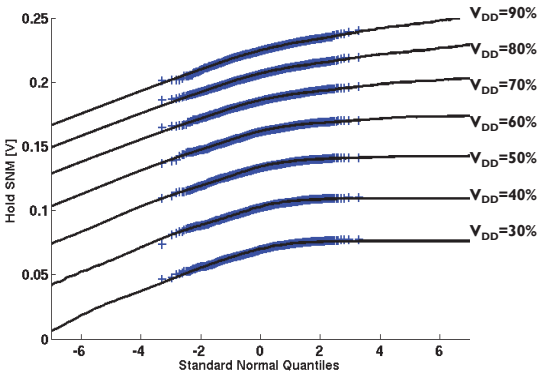

Fig. 16: Hold SNM distribution at decreasing supply voltage V_{DD}. Lines: the non-MC numerical propagation technique can predict the tails of the distribution up to $\pm 7\sigma$. Symbols: MC simulation added for comparison shows excellent agreement with the non-MC method [51].

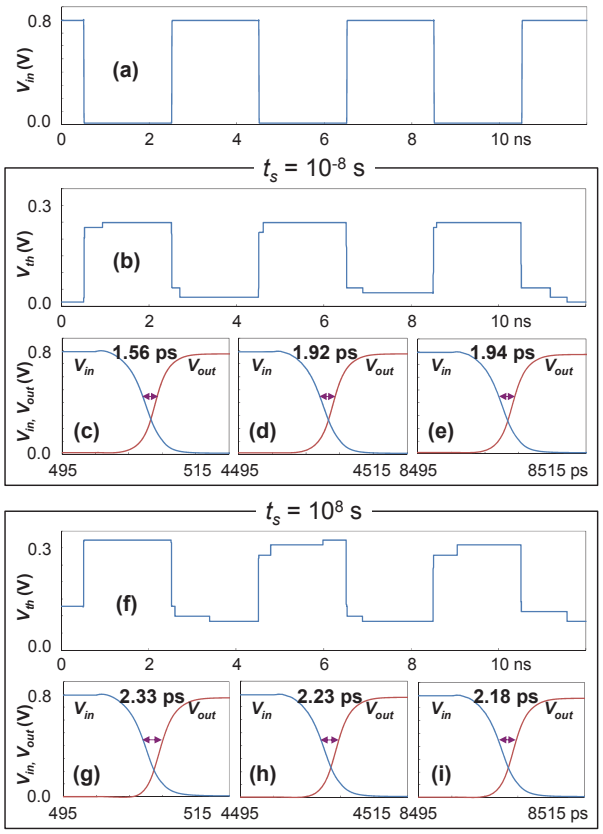

Fig. 17: Inverter degradation simulation transient snapshots. (a) Three periods of a $f = 250$ MHz input signal of the studied inverter. Corresponding time-dependent pFET threshold voltage V_{th} (b) after 10^{-8} s and (f) 10^{8} s. Two fast defects modulate the V_{th} in both cases. Note that due to short channel effects, V_{th} is also modulated by V_D, i.e., the output signal of the inverter. (f) V_{th} after 10^{8} s is futher degraded with respect to (b) due to the capture of charge in slow defects. Switching delay of the studied inverter during the three periods (c-e) after 10^{-8} s and (g-i) 10^{8} s [4].

B. Level 4 circuit simulations

Level 4 circuit simulations (Fig. 14) are physically the most accurate, but also correspondingly more CPU intensive. They draw on the insights reviewed above—each device is instantiated with a Poisson-distributed number of traps and each trap is instantiated with $\tau_e(V_G)$, $\tau_c(V_G)$, and ΔV_{th}, taken from the corresponding distributions (Figs. 6-8, 10) [4,52]. The impact on ΔV_{th} is adjusted according the FET size (cf. Fig.8). During the simulation, the trap occupancies are dynamically evaluated in each simulation time step depending on $\tau_e(V_G)$ and $\tau_c(V_G)$ of each trap.

Fig. 17 shows snapshots of one instance of the inverter simulation at the beginning of its operating lifetime (Figs. 17b-e) and after 10^8 s (Figs. 17f-i). Fig. 17b shows the pFET threshold voltage V_{th} behavior at the beginning of the circuit operation. V_{th} is changing as single holes are captured in two fast "cyclo-stationary RTN" [53] defects when the inverter input is low (i.e., the pFET gate is stressed), and subsequently emitted when the inverter input is high (i.e., pFET $V_G = V_S$). The same two defects are still active 10^8 s into the circuit operation (Fig. 17f); note, however, the pFET V_{th} is further degraded with respect to its initial value (Fig. 17b) due to the charge capture in slow defects. This latter behavior thus naturally emulates the "classical" BTI degradation.

The inverter switching transients are also illustrated in Fig. 17. It is apparent that there is a variation in the inverter switching delay from period to period (see Figs. 17c-e and 17g-i), resulting in the so-called delay jitter [54]. The overall slowdown of the inverter after 10^8 s of operation is also apparent (cf. Figs. 17c-e and 17g-i).

Level 4 circuit simulation should be employed for circuits susceptible to RTN, such as sensor arrays.

IV. Conclusions

We have argued that time-dependent variability (reliability variability) is an emerging trend that needs to be considered in circuit design in addition to time-zero variability and mean device degradation. We moreover have claimed that the time-dependent variability in deeply scaled devices can be best understood in terms of an ensemble of individual defects and their time, voltage, and temperature dependent properties. We have discussed the properties of gate oxide defects and have shown how, within the so-called defect-centric picture, these properties can be used to construct time-dependent variability distributions and can be propagated up to transistor-level circuits.

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