SOT-MRAM based on 1Transistor-1MTJ-Cell Structure

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New types of spin-based memory utilizing all-electrical magnetization manipulation by current have been intensely developed based on MgO magnetic tunnel junctions (MTJs). Depending on the current paths for read and write operations, memory can be classified in two categories: (i) with the same path (1Transistor-1MTJ cell) or (ii) with different paths (2Transistors-1MTJ cell) for read and write operations. Two main shortcomings of the first category of devices are still limiting the reliability and endurance: indeed, (i) the high write current density can occasionally damage the MTJ barrier and (ii) it remains a challenge to fulfill reliable reading without ever causing switching [1]. These shortcomings are absent for devices of the second category; however, they require more space and thus cause lower area density due to the second transistor needed for writing [1, 2]. In this work we propose a concept of in-plane spin orbit torque magnetic random access memory (SOT-MRAM) based on a 1Transistor-1MTJ cell with different paths for read and write operations (Fig.1). With the proposed structure the write operation is based on two consecutive orthogonal sub-nanosecond in-plane current pulses. The switching is governed by the torques generated by the spin-Hall effect (SHE). We verify the proposed concept by using the Landau-Lifshitz-Gilbert equation, including the additional SHE term [3]. We examine the switching by two schemes, the "write pulse 2" and the "two write pulses" scheme. The switching occurs in both cases (Fig.2a). The switching under the "write pulse 2" scheme is an unwanted event and leads to the loss of the information. However, as our simulations show (Fig.2b), the switching probability for the proposed "two write pulses" scheme is 1, when the second pulse is longer than 4.45ns. This pulse duration is shorter than the respective value of 6ns required to achieve the non-zero switching probability, when the "write pulse 2" scheme is used. This excludes the possibility of unwanted switching in not selected cells. Finally, increasing the current value to 30μA accelerates switching under a nanosecond (Fig.2c) while still preserving not selected cells from unwanted switching (Fig.2d).

References

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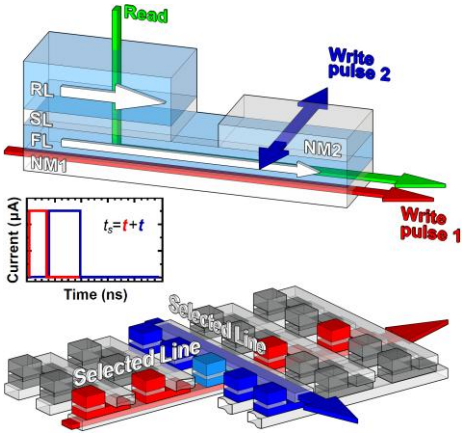

Fig. 1: Schematic illustration of (top) proposed SOT-MRAM; (middle) "two write pulses" scheme; (bottom) memory array.

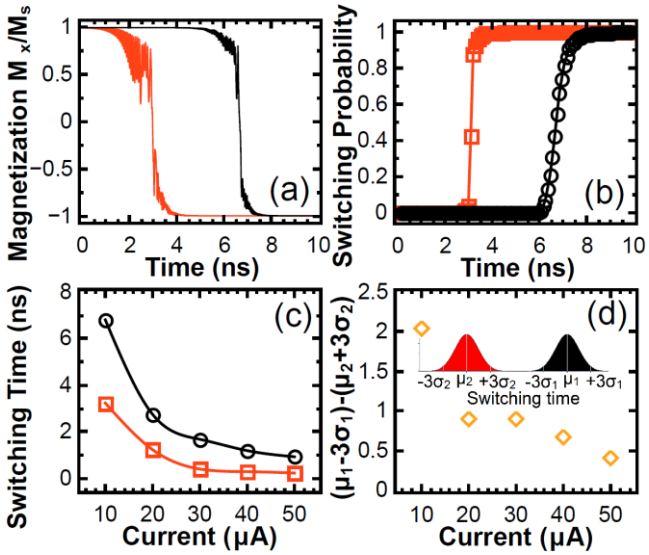

Fig. 2: (a) Averaged magnetization component in the direction of the long axis. (b) Switching probability as a function of time. (c) Switching time as a function of current. (d) The difference between the minimum value of "write pulse 2" required to achieve a non-zero probability of switching by using only "write pulse 2" (μ_1-3σ_1) and a value of "write pulse 2" needed to achieve guaranteed switching with "two write pulses" (μ_2+3σ_2) as a function of current. In (a), (b), (c), (d) the "two write pulses" scheme is shown in red and the "write pulse 2" scheme is shown in black.