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Intrinsic stress analysis of tungsten-lined open TSVs

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ABSTRACT

The effects of silicon etching and subsequent metallization during the fabrication of tungsten-lined open TSVs are examined using a combination of measurements and simulations. The total stress through a tungsten film deposited on a flat wafer is measured and finite element simulations are performed in order to identify the intrinsic and thermal stress components in the film. The data is then used to observe and model the stress through a TSV structure, which is etched using the DRIE process, resulting in scalloped inner sidewalls through the TSV opening. The scalloped structure is then compared to the ideal flat alternative with regard to the stress through the metal film and the TSV's electrical parameters, including resistance, capacitance, and inductance. It is found that the stress around the scallop varies significantly while the average stress through the tungsten in the flat TSV is only slightly higher than the stress observed through the scalloped structure. The resistance, capacitance, and inductance are all found to increase in the presence of scallops.

1. Introduction

Recently, a considerable amount of effort has been directed towards introducing more functionality to applications beyond memory and logic, deemed more than Moore integration. This type of three-dimensional (3D) integration is realized using a through-silicon via (TSV) process, which allows for the vertical stacking of systems and technologies, enabling dense device packing, lower power consumption, and reduced RC delays [1]. The TSV structure is generated with a sequence of multiple etching and deposition steps after CMOS processing followed by the deposition of the isolation layer, the metal film, and the liner layers of oxide and nitride.

Several studies deal with the reliability and performance of filled copper TSVs [2] as well as open tungsten-lined TSVs [3]. Open TSVs are desired when the stress build-up due to material thermal expansion is a concern. The presence of a void in the middle of the TSV allows for material expansion, avoiding the reliability concerns related to copper pumping which is common to filled TSVs [4]. However, an open TSV requires more wafer area and quite complex processing techniques [3]. The processing steps to manufacture an open TSV include deep reactive ion etching (DRIE) as well as several deposition steps, usually performed with a form of chemical vapor deposition (CVD) [3]. The processing can have a significant negative impact on the TSV performance and stress build-up. In particular the DRIE step results in scalloped sidewalls along the full depth of the TSV, which can have adverse effects on the electrical performance as well as the stress distribution in the metal layer [5].

In this study a methodology is presented by which the stress distribution through complex TSV structures can be modeled. The stress can be a result of the intrinsic stress, generated during the metallization process, or thermal stress, generated during the wafer cooling to room temperature after a thermal anneal or deposition step [6]. Both stresses are analyzed and their influence on the overall stress through a sample TSV is given. Knowing the intrinsic stress leads to a better understanding of the thin film material and improves our modeling capabilities. In addition, the stress and performance of a scalloped TSV are compared to that of an ideal flat-sidewalled alternative in order to understand the role which the scallops have in the operation and reliability of an open TSV structure.

2. TSV fabrication steps

The fabrication of open tungsten-lined TSVs is complex and requires several carefully executed steps. Prior to fabricating the TSV, the CMOS processing sequence is applied to generate the devices. Subsequently, the wafer is thinned down to a required thickness and bonded. Three main steps describe the TSV fabrication: (1) the opening of the intermetal dielectrics; (2) the etching of the CMOS wafer using a DRIE process with an etch-stop metal layer at the bond side; and (3) oxide isolation, metallization, and further passivation deposition steps [3]. The steps are addressed in further detail in the following.

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2.1. Etching through the wafer with a DRIE process

After opening the inter-metal dielectrics on the top side of the wafer and depositing an etch-stop layer (metal or oxide) at the bottom side, the etching proceeds using the so-called Bosch process [7]. This process consists of a sequence of polymer deposition and etching steps. The polymer is applied using a plasma deposition in a C_4F_8 environment. A subsequent etching step in an ion-enhanced SF_6 plasma environment ensures that the bottom of the deposited polymer is etched away, while the sidewall is protected. The etching step is a simultaneous physical and chemical process. After the physical ion etching process removes the polymer at the trench bottom, the chemical etching process is free to proceed with a further removal of the silicon at the exposed bottom of the trench, while the sides remain protected with the previously-deposited polymer. After hundreds of deposition/etch cycles are applied, a trench remains with a sidewall roughness in the form of scallops which result from the cycled nature of the process. The sizes of the scallops depend on the deposition and etch rates used during the DRIE process.

2.2. Isolation oxide deposition

After the etch process is complete, an oxide layer must be deposited to isolate the silicon substrate from the TSV metal which will connect the top and bottom of the wafer. This layer may not be deposited using high-temperature CVD techniques, because the TSV processing is performed at the end of the full CMOS process flow. Therefore the maximum allowed temperature is in the order of 400 °C, which is achieved using three deposition steps: (1) Plasma Enhanced Chemical Vapor Deposition (PECVD) is used to initiate oxide deposition; (2) Sub-Atmospheric Chemical Vapor Deposition (SACVD) is used as a second spacer oxide deposition step; and (3) PECVD is used once again in order to get the optimal spacer layer thickness along the full TSV sidewall [3]. The effect of these deposition steps on the performance of the TSV is given in more details by Baer et al. in [8] where statistical Monte Carlo simulations are performed on a similar TSV structure and the effects of the across-wafer variation of oxide flux on the device performance are analyzed.

After the deposition of the isolation oxide, a layer of Ti/TiN is deposited as liner, followed by a CVD of tungsten. On top of the tungsten additional oxide and nitride layers are deposited for electrical and moisture isolation of the open TSV.

3. Tungsten stress measurements

It is important to note that the values mentioned in this work, both measured and simulated, which refer to material thicknesses and measured stress levels, do not represent actual device values, but are rather used as a reference in order to properly describe the applied simulation methodology.

Measuring the stress through a scalloped TSV is very challenging, time consuming, and expensive; therefore, the ability to accurately simulate the stress through the scalloped TSV layers is highly desired. After the full structure is fabricated the TSV must be sliced through its diameter in order to apply the synchrotron X-ray nanodiffraction technique [9] and thereby to extract the strain in the layers along the sidewall. This technique only provides the final stress through the structure and does not allow insight into the stress build-up during metallization. In order to understand how the stress in the tungsten arises during the deposition process and metal growth, further measurements and simulations are performed. The processes required for the deposition of the TSV sidewall layers are applied to a blank, flat wafer after which the stress through the isolation oxide, Ti/TiN and tungsten is measured.

3.1. Measured stress in a scalloped tungsten-lined TSV

The stress through the scalloped TSV sidewall was measured for one sample using the synchrotron X-ray nanodiffraction method pictured in Fig. 1, which allows determining the axial and tangential strains in a thin film. First, a slice of the silicon wafer with a TSV was scanned using a 100 nm beam with a photon energy of E = 13 keV oriented in parallel to the film substrate in order to obtain power diffraction data for the sample in transmission geometry [9]. To evaluate the stresses in the metal, the distortion of Debye–Scherrer – or power diffraction – rings of tungsten reflections is considered [9], which gives insight into the microstructure properties of the material. By observing the diffraction peaks in the rings, the strain in each lattice direction – (211), (200), and (110) for tungsten – is computed, resulting in the strain mappings of the material for each relevant lattice direction [10]. The scanning was performed by translating the beam sample along the horizontal and vertical axis with steps matching the 100 nm applied beam size. The diffraction data was collected using a CCD detector located about 10 cm away from the sample and the measured strain was extracted using the program package Fit2D [11].

3.2. Measured stress in a flat wafer

The stress through the films deposited on the flat wafer is measured and the results are shown in Table 1. The measurements are performed using X-ray diffraction at room temperature, meaning that the total stress is a combination of the intrinsic post-processing stress and the thermal stress, which results after cooling to room temperature. With measurements alone we are unable to separate the two stress effects; therefore, the individual stress components are calculated using simulations, as described in Section 5.1.

4. Simulating a TSV structure

In order to ensure precise simulations of the stress through metal films in scalloped TSV structures a sample structure is generated with an in-house topography simulator implemented in a level set framework [12]. The simulation is performed using a DRIE model to etch through the silicon wafer, followed by the deposition of isolation oxide (SiO_2), Ti/TiN, tungsten (W), SiO_2 liner, and silicon nitride (Si_3N_4). The deposition and etch rates used in order to generate a hole with a diameter of 80 μm and an aspect ratio of approximately 1:3 are given in Table 2.

The final two-dimensional profile along the TSV sidewall is shown in Fig. 2(a). The deposition steps are performed assuming simple isotropic rates in order to generate the desired film thicknesses. The deposition steps can also be performed with physically more meaningful statistical Monte Carlo models; however, this would require very long simulation times due to the large size of the TSV geometry. Since this study con-

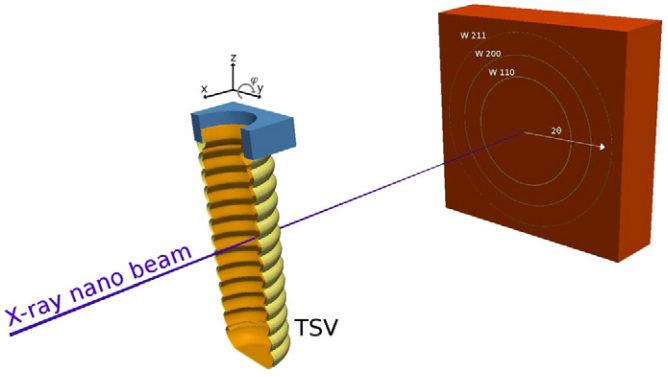

Fig. 1. Schematic view of the TSV strain measurement using position-resolved X-ray nanodiffraction.

Table 1
Deposition temperature and stress through the films after deposition.

Deposition material	Deposition temperature	Total stress (MPa) [a]
SiO_2	High	140
Ti/TiN	Low	−1000
Tungsten	Medium	1600

[a] Simulated stress (negative is compressive).

Table 2
Etch parameters used to generate a TSV structure with a sidewall scallop height of μm, as shown in Fig. 2(a).

Process	Rate (nm/s)	Etch ratio		Cycle time (s)
Polymer deposition	10	–		4.8
Silicon etch	120	Si:mask	27:1	
(Isotropic)		Si:polymer	40:1	12
Silicon etch	50	Si:mask	85:1	
(Directional)		Si:polymer	9:1	
Total number of cycles				229
Resulting scallop height				1000 nm
Resulting scallop width				300 nm
Total simulation time for the etch simulation				9 h

cerns itself mainly with the effects of the DRIE process on the TSV performance, the deposition steps are assumed to be ideal. The assumption is not expected to have a significant effect on the simulation results, especially since the purpose of the simulation is a comparison with a flat-sidewalled TSV, where a pronounced difference is expected. The TSV geometry and material thicknesses correspond to the structure which was used for the measurements in Section 3.1 as well as previous studies of similar structures [3].

After the structure is generated using process simulations the device is meshed and imported into a finite element simulator for stress and electrical performance analysis; the generated mesh contains approximately 1.3 million triangular elements. The simulations are performed using two-dimensional models with rotational symmetry and the rotation axis located in the middle of the TSV, as shown in Fig. 2(a).

5. Simulation and analysis of the intrinsic stress

The material properties used for the simulations in Sections 5 and 6 are given in Table 3. The intrinsic stress in the tungsten is determined by the generation and interaction, through collision, of metal islands during film growth, described in more detail in Section 5.1. The mismatch

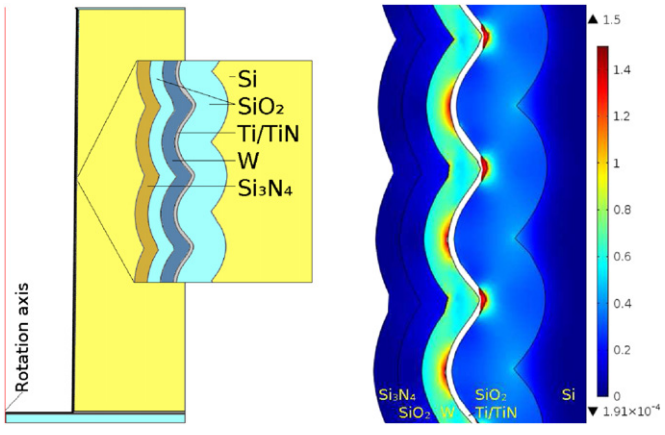

Fig. 2. (a) TSV structure generated using an in-house level set based process simulator and the rates from Table 2 and (b) simulated radial component of the stress (GPa) along the scalloped TSV sidewalls.

Table 3
Properties of the materials used in this study.

Material	CTE (/K)	E (GPa)	ν	Density (kg/m^3)	Cond. (S/m)
Silicon	$2.6 \cdot 10^{-6}$	135	0.28	2329	–
Oxide	$0.5 \cdot 10^{-6}$	70	0.17	2200	–
Ti/TiN	$9.4 \cdot 10^{-6}$	600	0.25	5200	$0.5 \cdot 10^{7}$
Tungsten	$4.5 \cdot 10^{-6}$	403	0.27	17,800	$1.33 \cdot 10^{7}$
Aluminum	$23 \cdot 10^{-6}$	70	0.33	2700	$2.5 \cdot 10^{7}$

in the coefficient of thermal expansion (CTE) is the main factor which determines the amount of thermo-mechanical stress which builds up after cooling [13]. The thermal stress is a critical TSV reliability issue for copper-filled and metal-lined open TSVs [4]. In a filled structure, the pressure caused by the expanding copper leads to the build-up of shear stress between the copper and the adjoining oxide; this results in sliding and delamination along the copper/oxide interface and ultimately copper pumping [4]. For open TSVs, although thermal stress does build up due to the varying CTEs of tungsten and silicon, the concern is not as high as in filled TSVs due to the void in the middle of the TSV which allows for the metal to expand inward during thermal expansion. Nevertheless, the thermo-mechanical stress is still a concern and the strain in a material resulting from a temperature increase or decrease from T_{ref} to T is given by

$$\epsilon = \alpha(T - T_{ref}), \tag{1}$$

where α is the CTE. The introduction of a temperature difference causes a material to expand or compress according to its α value.

5.1. Simulated stress in a flat wafer

The process temperatures used to deposit the required layers on a flat wafer and the resulting measured stresses are given in Table 1. In order to understand the origin of the total stress, it is essential to isolate the thermal stress component. A flat wafer, equivalent to the one measured in Section 3.2, is generated and meshed in a finite element simulation environment. The processing steps used to generate the measured structure are repeated within the simulator and the thermal stress component is calculated. The results show that the thermal stress components for the oxide, Ti/TiN, and tungsten films are −170 MPa, 1000 MPa, and 400 MPa, respectively. This means that approximately 1200 MPa of the stress generated in the tungsten layer correspond to the intrinsic stress component. Although the measured tensile stress in the tungsten exceeds its expected ultimate yield strength of about 1 GPa, the deposited film is nevertheless reliable. The ability for the material to be operational at such high stresses lies in the fact that the deposited metal has a thickness in the order of nanometers, while the yield strength is a bulk value. In [14], Kim et al. measured the yield strength of tungsten at varying thicknesses and found that reducing the metal thickness results in an increased yield strength.

In addition, it was noted in [15] that the deposition temperature plays a significant role in the resulting tungsten yield strength, concluding that a high temperature results in low yield strength values. Since the tungsten deposition for the studied structure is performed at medium temperatures (low temperatures in relation to the temperatures used in [15]), it may be the case that this provides a higher yield strength in the metal film. Table 4 gives a summary of the thermal and intrinsic stress components through the deposited films.

5.2. Intrinsic stress through tungsten

During the deposition of metal films on oxidized surfaces, the Volmer–Weber growth mode best describes the growth process taking place [16]. This mode is characterized by a film deposition in the form of islands which coalesce and then grow to form larger grains. The intrinsic

Table 4
Thermal and intrinsic stresses through the deposited films after deposition.

Material	Thermal (MPa)[a]	Intrinsic (MPa)[a]	Total (MPa)[b]
SiO_2	−170	310	140
Ti/TiN	1000	−2000	−1000
Tungsten	400	1200	1600

[a] Simulated stress (negative is compressive).
[b] Total stress is obtained from measurements given in Table 1.

stress develops during this process and can go through stages of compressive and tensile stress, depending on the film properties. The initial stages of film deposition are depicted in Fig. 3, where island nucleation, impingement between islands, and eventual coalescence are shown.

Upon impingement a grain boundary is formed between two islands as shown in Fig. 4, resulting in a part of the free surface of each island being eliminated and in a significant energy reduction.

This process generates a tensile stress in the grains, lasting from the initial impingement until coalescence, and resulting in a stress given by

$$\sigma_{tensile} = \frac{1}{2}\cdot\frac{E}{1-r^2}\left(\frac{y_0}{r}\right)^{1.3892}, \quad (2)$$

where E is the Young modulus, and r and y_0 are geometric parameters given in Fig. 4. After coalescence, thickening can proceed in one of two ways: (1) columnar, a growth mode for films with a high adatom mobility or low melting temperature, such as copper; or (2) polycrystalline, a growth which refers to the deposition of films with a low adatom mobility or high melting temperature, such as tungsten. During impingement and up to coalescence, a film's tensile stress will grow to a peak value. This stress level will then decrease and might switch to compressive during columnar growth. However, during polycrystalline growth, the stress level remains at its peak coalesced value. The build-up of stress during the deposition of tungsten is shown in Fig. 5. At about 20 nm, the film is fully coalesced as a stress of approximately 1.2 GPa develops. During further thickening, the stress level remains unchanged.

6. Scalloped TSV simulation and discussion

6.1. Stress in the scalloped TSV tungsten layer

In Fig. 6 a scanning electron micrograph shows evidence of the scalloped morphology of the inner TSV sidewall. After performing the described synchrotron X-ray nanodiffraction measurements, the resulting stress along the line given in Fig. 6 is plotted in Fig. 7. The peaks and valleys of the stress measured along the scallops are evident, with the stress ranging from about 500 MPa to 900 MPa.

In this section the scalloped TSV structure from Fig. 2(a), which is generated using the method described in Section 4, is used for simulations. After applying the intrinsic stress, obtained with the help of measurements and simulations of the flat wafer and the tungsten deposition temperature, a simulation of the thermo-mechanical stress through the tungsten was performed. The resulting stress through the middle of the tungsten layer is plotted in Fig. 7, where it can be seen that the simulated stress peaks and valleys match the measured values very well. The height of the individual scallops can be estimated by observing the distance between the stress peaks or valleys; from Fig. 7, it can be deduced that both the measured and simulated TSVs have a scallop height of approximately 1 μm.

In Fig. 2(b) the stress through the sidewall of the simulated TSV structure is shown. The peaks and valleys of the plotted stress from Fig. 7 correspond to the concave and convex sections of the scalloped tungsten metal shown in Fig. 6 as it follows the curvature of the oxide and Ti/TiN layers. The successful implementation of this methodology allows the improvement of modeling of the stress through open TSVs and eliminates the need for further expensive measurements.

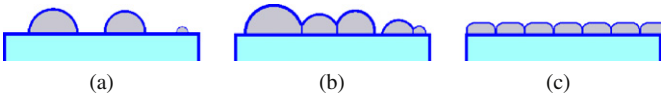

Fig. 3. Initial steps during film formation using the Volmer–Weber growth mode, including (a) nucleation, (b) impingement, and (c) coalescence.

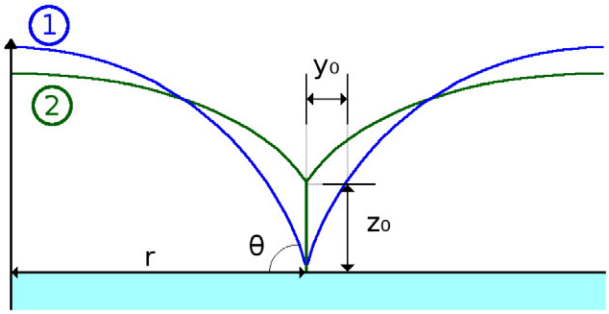

Fig. 4. During the early stages of thin film deposition and the expansion of metal islands, impingement between two islands takes place. From position 1 to position 2, two islands impinge, resulting in a grain boundary with height z_0.

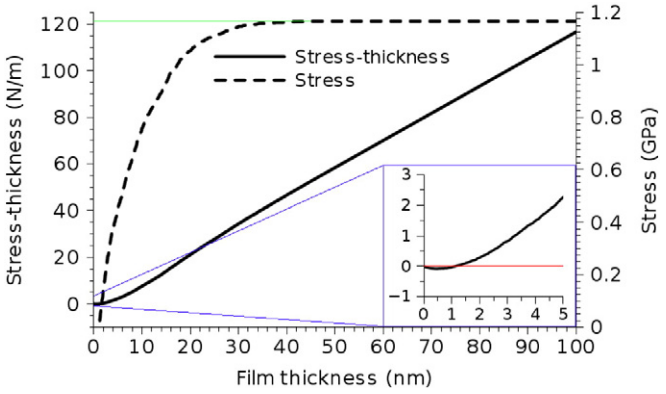

Fig. 5. Intrinsic stress development in a flat tungsten thin film.

6.2. Effect of scallops on TSV reliability

In order to quantify the effect that the scallops have on the stress and electrical performance of the TSV, a structure with the same diameter, aspect ratio, and material thicknesses was generated with flat sidewalls in a finite element environment. The same simulation sequence was carried out on the scalloped and flat structures and the results are discussed in this section.

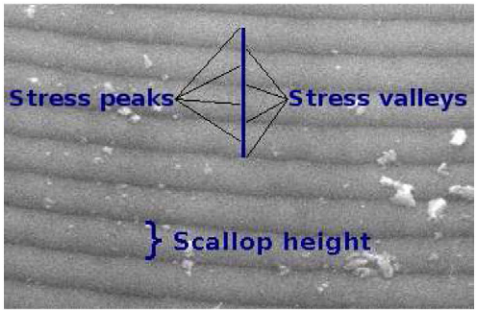

Fig. 6. Scanning electron micrograph showing a scalloped morphology of the TSV sidewall [9]. The stress peaks and valleys refer to the peaks and valleys noted in the final stress simulation in Fig. 7.

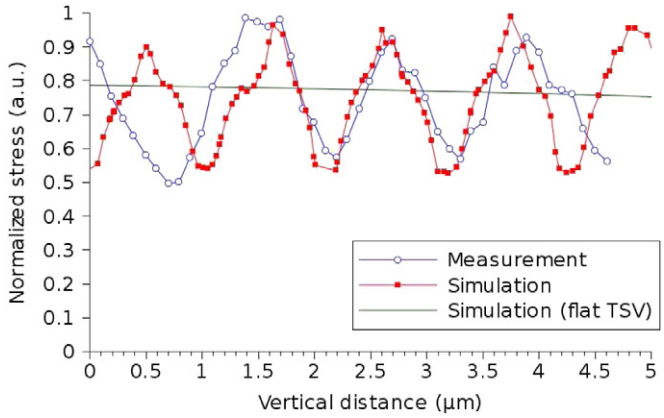

Fig. 7. Stress through the tungsten layer along the sidewall of the open TSV. The simulated TSV matches the measured one very well, while the stress through the flat-sidewalled TSV stays almost constant. The measured results were performed at ESRF in Grenoble by the group of Dr. Jozef Keckes.

The stress through the flat-sidewalled TSV is plotted in Fig. 7 together with the plot of the stress through the scalloped structure. It is clear that the stress does not exhibit peaks and valleys, but that it is generally flat through the entire depth of the structure and lies approximately halfway between the maximum and minimum stresses observed in the scalloped TSV. The average stresses through the flat and scalloped structures are found to be 816 MPa and 740 MPa, respectively. Although the scalloped geometry causes local stresses to vary significantly through peaks and valleys, the average stress through the tungsten layer is reduced by about 9.31% in the presence of scallops. A reduction in stress in the presence of sidewall scallops was also noted in experiments presented in [17].

6.3. Effect of scallops on the electrical performance of TSVs

The electrical parameters of the scalloped and flat TSVs were simulated in a finite element environment, with the resulting equivalent resistance (R_{TSV}), capacitance (C_{TSV}), and inductance (L_{TSV}) given in Table 5. With this knowledge a small-signal model can be generated by describing the metal layer as an inductance and a resistance in series between the top and bottom of the TSV and a capacitance coupling to the substrate [18].

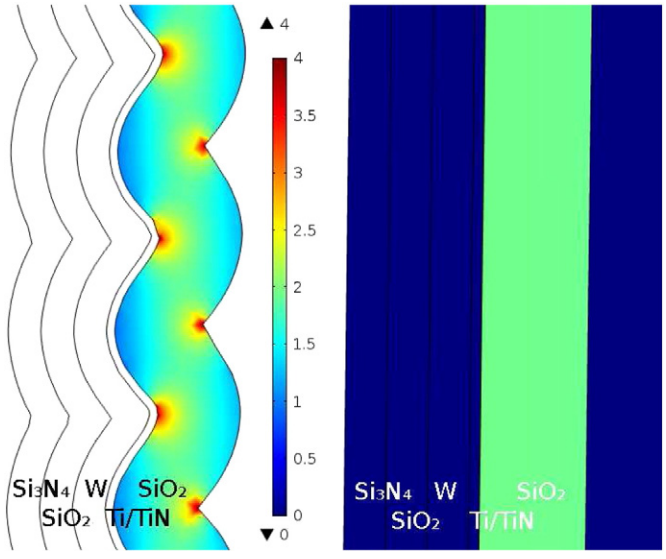

Fig. 8. Electric field (MV/m) through the silicon dioxide isolating tungsten from the silicon substrate.

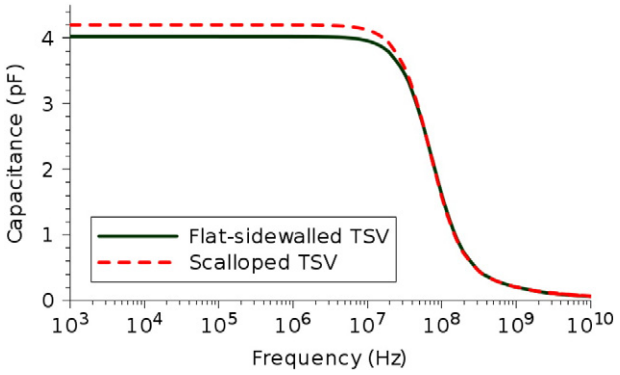

Fig. 9. Frequency-dependent capacitance for the scalloped and flat-sidewalled TSVs. A higher low-frequency or DC capacitance is noted for scalloped TSVs.

It is evident that the values of all electrical parameters increase in the presence of scallops. The increased resistance is due to the increased length in the tungsten layer as an effect of its curvature around the scallops. The effective length of the tungsten layer from the top to the bottom of the TSV is 226 μm and 252 μm for the flat and scalloped structures, respectively; this is an effective increase of about 10% in the current path through the wafer. The increased amount of tungsten can also explain the increased inductance noted in Table 5. A similar effect was observed when analyzing the effect of increasing scallop size on the TSV electrical parameters [19].

The capacitance increases due to the thinning which occurs during the deposition around individual scallops [20]. In addition, the presence of scallops on the isolation oxide results in peaks in the electric field, as shown in Fig. 8, where the flat TSV displays a very even electric field throughout the isolation oxide, while the scalloped TSV shows the electric field peaking at the scallop pinch-off points. However, lower values are noted at the rounded scallop edges, which is why the capacitance increases by only about 4.8%. The difference in the capacitance is only relevant when operating at DC and frequencies below 1 MHz, as depicted in Fig. 9. For high frequencies above 1.1 MHz, the structure enters the resistive regime and the scallops do not play any role in the capacitance.

In this section the influence of the scallops along the TSV sidewall on the performance and stress in the device is examined. Some negative aspects have been identified, mainly concerning the electrical performance of the TSV in the presence of scallops. However, there is also a positive aspect of the scallops in that they prevent interfacial sliding along the interface between the metal and isolation oxide. In [21] the shear stress which develops at the interface between the copper in a filled TSV and the surrounding oxide is examined. With experimental evidence, it is reported that interfacial sliding is one of the main reliability concerns of Cu-filled TSV. It was found that the presence of scallops reduced the potential for this phenomenon, thereby increasing the overall reliability of the device. Although the study was performed on a filled TSV, it can be deduced that similar conclusions may be drawn for open TSVs. Even though metal pumping is not a critical concern, having scallops to reduce the potential for delamination improves the overall reliability of open TSVs.

Table 5
Simulated electrical parameters and average stress for the TSVs with flat and scalloped sidewalls.

Property	Flat TSV	Scalloped TSV	Difference (%)
Resistance — R_{TSV} (mΩ)	349	370	+6.02
Capacitance — C_{TSV} (pF)	4.02	4.20	+4.48
Inductance — I_{TSV} (pH)	4.02	4.70	+16.92
Average stress (MPa)	816	740	−9.31

7. Conclusion

The measured stress through a flat tungsten film in combination with finite element simulations is used to separate the intrinsic and thermal stress components. The results were used to analyze the stress in the tungsten metal layer of an open TSV structure with scalloped sidewalls. The findings of the simulation match well with measurements performed with synchrotron X-ray nanodiffraction. Additionally, simulations were carried out to analyze the difference in electrical performance and stress between the scalloped and flat TSVs. It was found that the electrical parameters such as resistance, inductance, and parasitic capacitance increase in the presence of scallops. The resistance and the inductance increase due to an increase in the current path through the curved, and thereby elongated, tungsten metal. The capacitance, however, increases due to peaks in the electric field in the isolation oxide in the presence of scallops. When deposition is performed on an etched silicon trench, the concave sections become convex and vice versa. Therefore, at the scallop pinch-off points, the effective thickness through the oxide is reduced, causing an increased electric field and thereby an increased coupling capacitance. The average stress in the tungsten layer is slightly reduced in the presence of scallops; however, the stress is characterized by peaks and valleys along the entire length of the TSV sidewall.

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