Simulation Analysis of the Electro-Thermal Performance of SOI FinFETs

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1. Introduction

FinFETs, with their superior electrostatic integrity, performance and variability, are replacing the traditional planar MOSFETs [1]. However, because of their 3D architecture, the FinFETs' thermal properties are significantly degraded. Self-heating effects will be exacerbated in SOI FinFETs (a schematic of an SOI FinFET is shown in Fig. 1), due to the low thermal conductivity of the buried oxide layer beneath the fin. To maximise the benefits of FinFET technology, an enhancement of TCAD tools is required, to allow accurate analysis and modelling of self-heating in FinFETs and its influence on device performance [2]. A progressive electro-thermal FinFET simulation study has been presented [3]. Recently, the thermal simulation module in the GSS 'atomistic' simulator GARAND [4] has been enhanced to capture accurately the fin geometry dependence of the thermal conductivity [5]. In this paper, GARAND is used to investigate the electro-thermal performance of SOI FinFETs under different external thermal resistances connected to the gate.

2. Simulation Methodology

Our electro-thermal simulation module, as used in this work, is based on the solution of the coupled Heat Flow, Poisson and Current Continuity Equations. A special thermal conductivity model is developed considering the effects of thermal confinement in FinFETs, where the thickness and width of the fin is less than 100 nm. The thermal conductivity in the fin can be significantly reduced compared to bulk Si, due to phonon-boundary scattering. The new approximate formula generalises a previous 1D paradigm [6] to 2D confined structures by assuming a similar integral dependency in the second direction [3]. The thermal environment, where heat is dissipated, is a large domain including transistors, the substrate, the interconnect layers, the die, the heat sink and packaging. The usual electrical simulation domain is typically restricted to the active region of the device in order to minimise simulation time. The inclusion of external thermal resistances is crucial for thermal simulations. In FinFETs the heat dissipation through the gate is more complicated because the shape and materials of the gate stack and surrounding region are much more complex. At thermally conducting interfaces, nonhomogeneous Neumann boundary conditions can be imposed.

3. SOI FinFET example

An SOI FinFET designed to meet the specifications for the 14/16nm CMOS technology generation is used in this study. Its channel length is 25 nm with spacers of 6nm on both sides of the gate, while the fin width and height are 12nm and 30nm respectively. A high-κ metal gate stack is employed. Three external resistances are used to account for heat dissipation through the top of the gate, the front and the back of the gate. By employing GARAND with the coupled thermal simulation module, five different cases with various external thermal resistances connected to the gate of the SOI FinFET example are simulated, as summarised in Table I. The external thermal resistances are user-specified parameters for the electro-thermal simulation module. The values used here demonstrate the effect and importance of the choice of relevant thermal resistances.

Joule heat distribution at high drain and high gate biases resulting from the 3D coupled electro-thermal simulations for "Case 1" are illustrated in Fig. 2. Lattice temperature distributions at high drain and high gate biases for five cases are illustrated in Fig.3, as well as the temperature variation according to the gate voltage at high drain bias. The Id-Vg characteristics at high drain bias from the 3D electro-thermal simulations are illustrated in Fig.4.

4. Conclusions

Using GARAND with enhanced 3D coupled electro-thermal simulation capabilities, the electro-thermal performance for an SOI FinFET example, aiming for the 14/16nm CMOS technology generation, has been simulated. The lattice temperature profiles under different external thermal resistances and the corresponding Id-Vg characteristics are investigated and analysed. The results show a significant hot spot generated near the drain because of the much lower thermal conductivity of the fin, as the peak lattice temperature exceeds 420 K for all five cases in this study, and strong temperature gradients are also generated in this region. The impact of external thermal resistances at different places connected to the gate is different, consequently affecting the electrical performance of the SOI FinFET.

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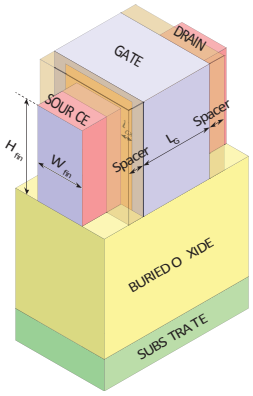
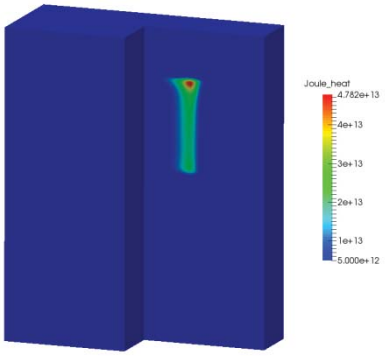


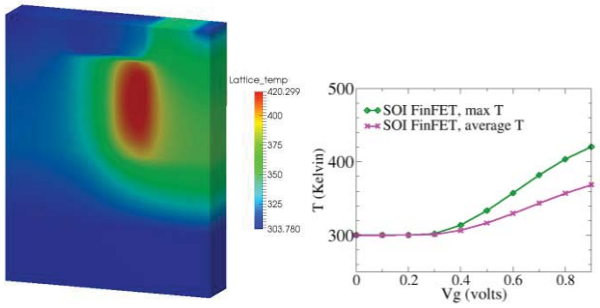
Schematics of SOI FinFET.

FIVE DIFFERENT CASES WITH VARIOUS EXTERNAL THERMAL RESISTANCES FOR 3D COUPLED ELECTRO-THERMAL SIMULATION

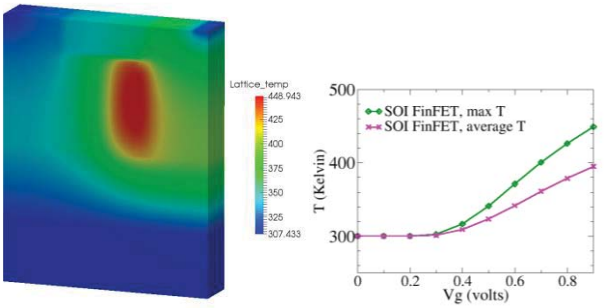
	External thermal resistance connected to		
	Top gate	***Front gate***	***Back gate***
Case 1	4800	32	32
Case 2	4800	320	320
Case 3	4800	3200	3200
Case 4	480	32	32
Case 5	480	320	320



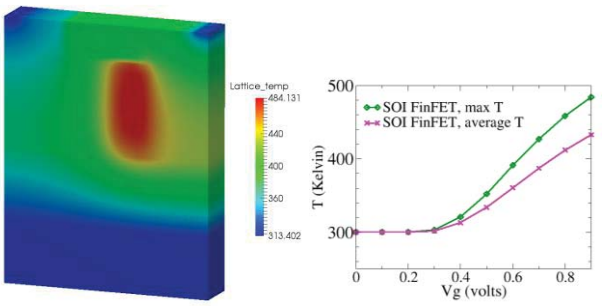
Joule heat distribution at high drain and high gate biases resulted from the 3D coupled electro-thermal simulations for "Case 1".



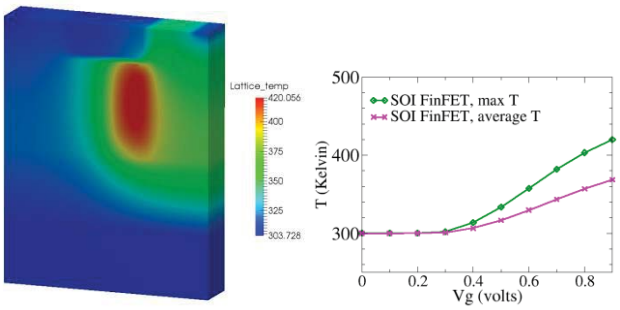
(a) Case 1



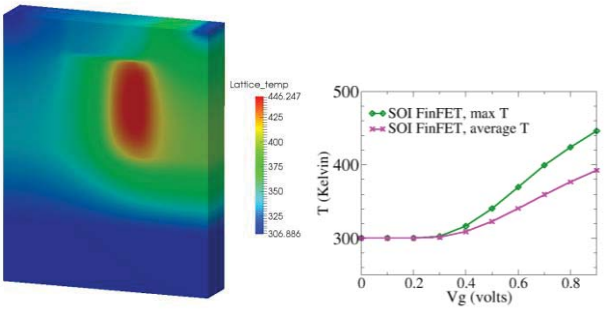
(b) Case 2



(c) Case 3

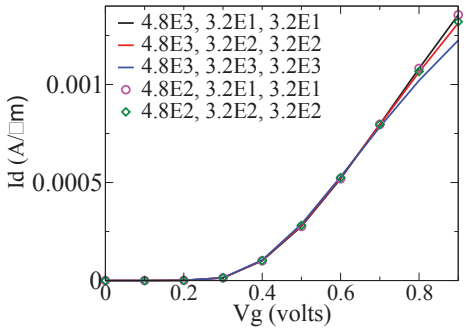


(d) Case 4



(e) Case 5

Lattice temperature distributions at high drain and high gate biases (left) and the temperature variation according to gate voltage at high drain (right), resulting from the 3D couped electro-thermal simulations for five cases.



Id-Vg characteristics at high drain bias from the 3D electro-thermal simulations, comparing five cases.