

Analog-circuit NBTI degradation and time-dependent NBTI variability: An efficient physics-based compact model

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Abstract—We experimentally and theoretically investigate the NBTI degradation of pMOS devices due to analog stress voltages and thus go beyond existing NBTI studies for digital stress. As a result, we propose a physics-based compact model for analog-stress NBTI which builds upon the extensive TCAD analysis of our ultra-short-delay experimental data. The numerical efficiency of the compact model allows its direct coupling to electric circuit simulators and permits to accurately account for NBTI degradation already during circuit design. Our model enables the calculation of the time-dependent NBTI variability of single device and of circuit performance parameters. We demonstrate our NBTI model on an operational amplifier and calculate the mean drift and variability of its offset voltage.

I. INTRODUCTION

The performance of analog circuits can be highly sensitive to the electrical aging of their constituent devices. Consider for instance an operational amplifier circuit: the negative bias temperature instability (NBTI, [1–3]) can here induce a mismatch of the differential pair input transistors, which has a detrimental impact on the circuit’s proper functioning. In contrast to the typical behavior in digital circuits, where only a degradation above a certain level negatively affects the circuit logic, in analog circuits already a small degradation can have an immediate effect.

Advanced digital-stress NBTI or random telegraph noise models [4–9] are based on capture-emission-time (CET) maps or otherwise exploit the fact that the stress voltage takes on only two values. In contrast, the continuous stress voltage levels of analog signals necessitate a more complex model that takes into account extensive information about the defect dynamics: The Markov two-state NBTI model [3] is based on a differential equation describing defect charging. For the case of periodic digital stress, the closed-form solution to this differential equation is known [4]. This solution was generalized to periodic analog stress voltages in [10]; a related approach was given in [11]. The parametrization [12] of the gate-source voltage (V_{gs}) dependence of CET maps can be an input to future analog-stress NBTI models.

In addition to the degradation of the mean values, NBTI compact models are of particular interest for the study of time-dependent NBTI variability in analog circuits. For digital circuits, this question was already considered: based on a log t -degradation model, the second moment of the threshold voltage distribution was calculated [6, 13]. Reference [14]

presents an analytical NBTI modeling for the entire threshold voltage distribution under digital stress.

We here propose an accurate NBTI compact model for analog design, including time-dependent NBTI variability. The present analog-stress study combines the results of experiments, TCAD simulations and the new compact modeling. After giving the technical details of our method, we compare experimental and theoretical results on the NBTI aging of single transistors due to analog gate-source voltages. We finally apply our model and study the NBTI degradation of an operational amplifier circuit. In particular, we demonstrate how our model provides access to the NBTI variability of analog circuits.

II. TECHNICAL DETAILS

A. Experimental setup

All measurements were performed on production quality pMOSFETs of a 130 nm technology with a 2.2 nm SiON gate oxide and a nominal operation voltage $V_{dd} = 1.5V$. Using a measure-stress-measure (MSM) technique with an ultra-short readout delay ($\sim 1 \mu s$, [15]) minimizes the unmonitored recovery of the devices after stress. The measurement principle is shown in Fig. 1. To keep the 0h and drift variation of the threshold voltage shift ΔV_{th} low, all tests were run on hardware of the same process and only on adjacent chips. Every measurement was run at 125 °C to allow a pronounced NBTI degradation and consists of a sequence of 4 stress times, (10^{-2} , 1, 10^2 and 10^4) s, each followed by a recovery trace of 100 s. The analog stress signals (sine, sawtooth, inverse sawtooth, digital) vary in the maximum stress voltage $V_h = (1.8, 2.3$ and $2.8)$ V and are in the kHz frequency range (500 Hz to 2 kHz). These waveforms are applied to the gate terminal of the device employing an arbitrary waveform generator which is built into the ultra-fast measurement equipment. That assembly enables a short wiring between the transistor under test and the test equipment and therefore provides superior signal integrity.

B. TCAD simulation

Our compact model is based on a physically accurate description of the capture and emission time constants of the defects which cause BTI. The time-dependent defect-spectroscopy (TDDS, [16]) allows to measure the time constants of individual defects directly. Unfortunately, these

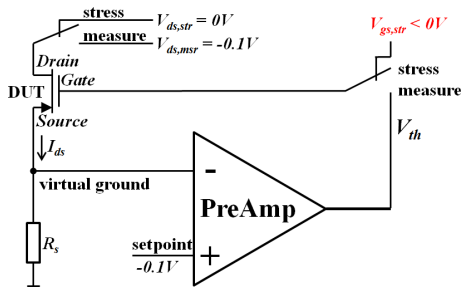


Fig. 1: The measurement principle of the ultra-fast NBTI gadget [15]. To apply the stress signal to the device under test, the switches connect the preset drain-source and gate-source voltage to the corresponding terminals. We employ an operational amplifier and measure the threshold voltage directly at its output in dependence of the chosen setpoint and sense resistor R_s .

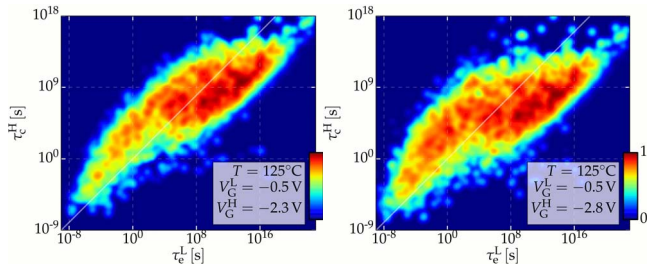


Fig. 2: Our approach is based on multi-state defects with statistically distributed physical properties. It uses the NMP model for the recoverable NBTI defect component and a DW model for the more permanent part. We illustrate the present defect dataset calibrated to the technology under investigation by two capture-emission-time maps relevant for digital-circuit studies. Notice that analog-stress NBTI calculations necessitate more complex information about the defect dynamics, see Fig. 3.

TDDS measurements are very time consuming and therefore often impractical for the acquisition of a large set of defects. In order to provide the bias dependent capture and emission time constants for a large set of defects we therefore employed TCAD simulations. Our TCAD simulations use defect models which account for bias-dependent energy barriers along the transition path between two different charge states of a defect [3, 17]. This is consistent with non-radiative multi-phonon (NMP) theory [17–19] and is important for correct modeling as it strongly affects the time constants of the capture and emission processes of oxide defects. Furthermore, the four-state NMP model [3] which we have used in this work, accounts for additional metastable states, a defect property which was confirmed by recent studies [20, 21]. The generation of interface states is modeled using a simple double-well (DW) model, while their charge is determined by an amphoteric SRH model [1, 22]. We remark here that this interface state generation is a first-order approximation only. A more detailed physical explanation, which is consistent with the observed volatility of defects, accounts for the release of hydrogen [20, 23] and will be considered in future work. All traps and their physical parameters are sampled from distributions which had been calibrated to extensive measurement data of the investigated technology [24] in earlier work [25]. The resulting microscopic traps are depicted in CET maps [5, 12] in Fig. 2, and the time constants of the individual defects which are passed on to the compact model are shown in Fig. 3. The

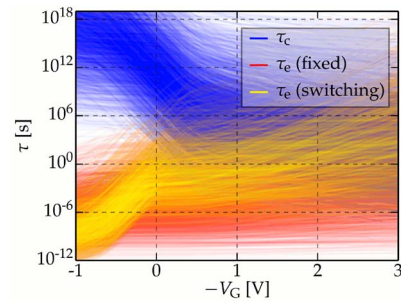


Fig. 3: Bias dependence of the capture and emission times of 4000 oxide traps at 125°C, resulting from the calibrated four-state NMP model (TCAD simulation). Oxide traps come in two distinct flavors: with weakly bias dependent emission time (*fixed oxide traps*) and with a pronounced bias dependence at low gate voltages (*switching oxide traps*).

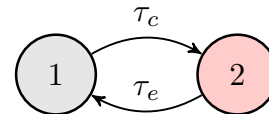


Fig. 4: Two-state-model defects undergo transitions from a neutral state “1” to a positively charged state “2” with a (mean) capture time τ_c , and a transition back with a (mean) emission time τ_e . These defect-specific times sensitively depend on gate voltage (see Fig. 3) and on temperature.

simulation of arbitrary stress signals is in principle straight forward also at the TCAD level, but as the required number of time steps increases with increasing signal frequency, this approach becomes computationally prohibitive for longer signal durations. An accurate compact model which anticipates the periodicity of the stress signal is thus necessary for the simulation of such signals as presented in the following.

C. Compact model

The two-state DW model and the projection of the four-state NMP model lead to the Markov two-state model (Fig. 4, [3]): each defect occupies either an electrically neutral or a positively charged state. The latter contributes to the NBTI threshold voltage shift via a modification of the oxide electric potential. We parametrize our effective NBTI model with the statistical defect sampling obtained earlier: a comprehensive TCAD analysis provides the transition rates (discretized in voltage and temperature space) and the defect-specific step height. The defect-specific transition rates sensitively depend on the gate voltage (see Fig. 3) and temperature.

The probability $w(t)$ of being in the positively charged state “2” satisfies the first-order ordinary differential equation (ODE)

$$\dot{w}(t) = a(t)w(t) + b(t), \quad w(t_0) = w_0. \quad (1)$$

Its coefficients

$$a(t) = -(\tau_e^{-1}(t) + \tau_c^{-1}(t)), \quad (2)$$

$$b(t) = \tau_c^{-1}(t) \quad (3)$$

are functions of the capture and emission times and inherit (from the analog V_{gs}) the property of taking continuous values. This is in contrast to digital NBTI models, where the coefficients only take one of two discrete values, corresponding

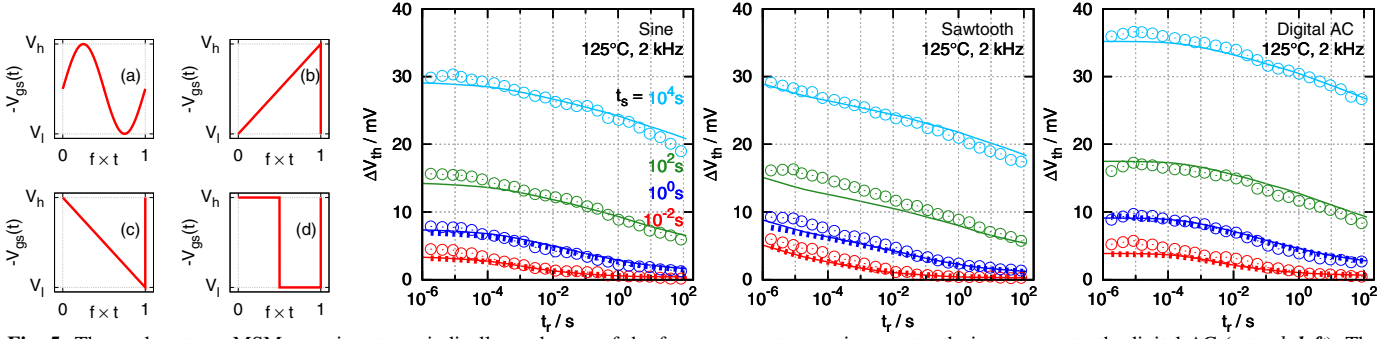


Fig. 5: The analog-stress MSM experiments periodically apply one of the four stress patterns: sine, sawtooth, inverse sawtooth, digital AC (a to d, left). The stress voltage oscillates between the values $V_i \leq -V_{gs}(t) \leq V_h$. Right (three plots): The MSM ΔV_{th} recovery curves after four stress durations 10^{-2} s, 10^0 s, 10^2 s and 10^4 s (bottom-up in the plots) show a good agreement of experimental data (symbols), TCAD results (thick dashes) and compact model results (solid line). Due to the large numerical effort, there is currently no TCAD data available for the two larger stress times. The present setup uses a stress frequency of 2kHz, a temperature of 125°C and stress voltages between $V_i = 0.5$ V and $V_h = 2.8$ V.

to high/low gate bias. Notice that digital models including dynamic voltage scaling (DVS) mostly also make direct use of this two-level stress structure and employ CET maps, which then are switched at each DVS event.

Our fast solution algorithm [10] to the above ODE rewrites $w(t)$ using matrix notation. We calculate the time integrals

$$P_1(t_2, t_1) = \exp\left(\int_{t_1}^{t_2} ds a(s)\right), \quad (4)$$

$$P_2(t_2, t_1) = \int_{t_1}^{t_2} ds b(s) \exp\left(\int_s^{t_2} dr a(r)\right) \quad (5)$$

over functions of the time-dependent ODE coefficients a , b and arrange these quantities in the 2×2 matrix

$$P(t_2, t_1) = \begin{pmatrix} P_1(t_2, t_1) & P_2(t_2, t_1) \\ 0 & 1 \end{pmatrix}. \quad (6)$$

This matrix propagates the ODE solution w from the initial time t_1 to the solution time $t_2 > t_1$,

$$\begin{pmatrix} w(t_2) \\ 1 \end{pmatrix} = P(t_2, t_1) \begin{pmatrix} w(t_1) \\ 1 \end{pmatrix}. \quad (7)$$

It furthermore satisfies the ‘‘group property’’ $P(t_2, t_0) = P(t_2, t_1)P(t_1, t_0)$, which states that the solution w at time t_2 can simply be obtained by propagating through an intermediate time t_1 . Therefore, the quantity $P(t_2, t_1)$ can be efficiently calculated for arbitrary large $t_2 - t_1$ from its values for $0 < t_2 - t_1 < T$, where T is the V_{gs} time period. This provides a numerically fast and at the same time exact method (within the two-state model) for calculating the NBTI degradation even at large stress times (days to years). Thereby, the compact model has access to the degradation after an arbitrarily large number n of stress periods, where TCAD simulations are numerically unacceptable, while featuring the accuracy of TCAD calculations also at smaller n . We remark that the compact model has no free parameters and follows directly from the TCAD model.

III. SINGLE TRANSISTORS EXPOSED TO ANALOG NBTI STRESS

We have calibrated our TCAD model to extensive experimental measurements for time-independent stress at various

gate-source voltages and various temperatures. Based on this calibration, we here compare the resulting ΔV_{th} predictions for time-dependent analog stress and thereby check the consistency of our approaches. We choose four V_{gs} stress patterns (Fig. 5, left) that are typical for analog-circuit waveforms: sine, sawtooth, inverse sawtooth and digital AC.

The MSM experiments periodically apply one of these patterns during stress times between 10^{-2} s and 10^4 s and then measure the resulting relaxation transients. These MSM tests show a very good agreement in the degradation curves obtained from experiment and theory, see Fig. 5. Due to the numerical complexity, TCAD data so far is only available for the two smaller stress times. The difference between TCAD and compact model results is often hardly noticeable. The consistency of experimental and compact model data at large stress times validates our compact model for large stress times also from a practical point of view.

Although we have experimentally no access to ΔV_{th} during the MSM stress phase, the theoretical models provide this information. We therefore compare the TCAD and compact model results for ΔV_{th} during the first five V_{gs} periods of the MSM stress phase. Figure 6 shows that both methods are in excellent agreement.

IV. NBTI STUDY OF AN OPERATIONAL AMPLIFIER

In the last section, we have validated our analog-stress NBTI compact model at single-transistor level. We continue with the NBTI analysis of an entire analog circuit and again employ the novel compact model.

For this purpose, we study a Miller operational amplifier (Fig. 7). The two pMOS transistors M31 and M32 form the differential pair and are subject to NBTI degradation. Different NBTI stress conditions for M31 and M32, caused by two differing signals to the two amplifier inputs, lead to a time-dependent mismatch: M31 and M32 drift apart. This translates into an NBTI-induced drift of the amplifier’s performance parameters, such as an increase in the offset voltage.

We study the amplifier in an open-loop configuration with its two inputs connected to two different signals: the inverting input ‘‘vinn’’ connects to half of the supply voltage, $V_{dd}/2$,

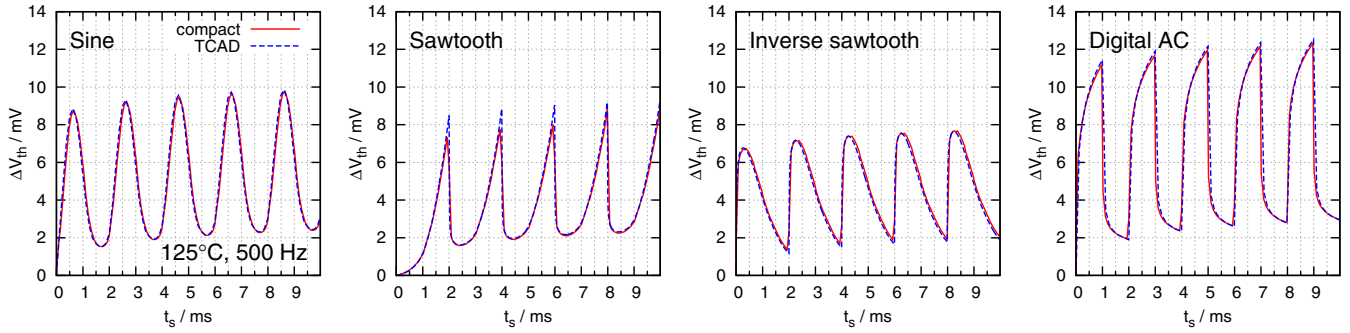


Fig. 6: Threshold voltage shift during analog stress. We compare TCAD (dashed line) to compact model (solid line) results on ΔV_{th} during the first five periods of the MSM stress phase. For all four stress patterns, both methods are in excellent agreement. The calculations use a stress frequency of 500Hz, a temperature of 125°C and voltage values $V_l = 0.5V$ and $V_h = 2.8V$.

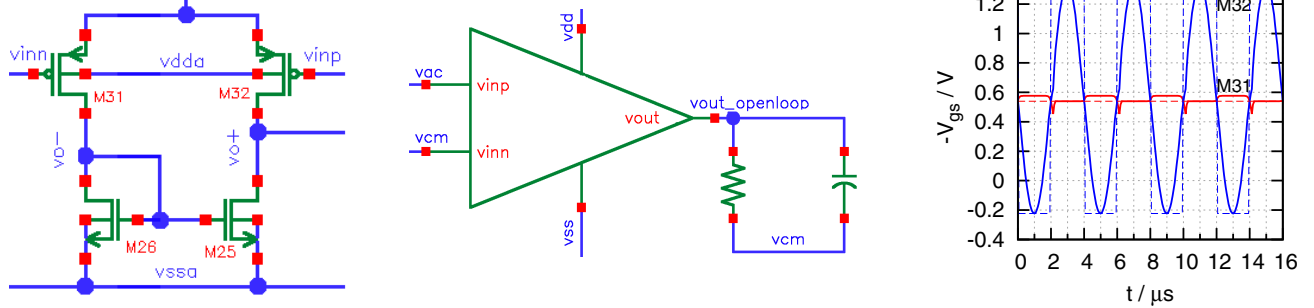


Fig. 7: Miller operational amplifier. *Left:* Differential amplifier stage (sub-circuit) of the operational amplifier. The two pMOS devices M31 and M32 form the differential pair and are subject to NBTI degradation. *Mid:* We examine the amplifier in an open-loop configuration (comparator) with its two inputs connected to two different signals, causing an asymmetric NBTI aging of M31 and M32. *Right:* Spice simulation of the nominal behavior (i.e. without degradation) of the amplifier circuit. The resulting gate-source voltages (solid lines) of the transistors M31, M32 differ from the amplifier input signals “vinn”, “vinp”. Therefore, the coupling of the NBTI compact model to an electric circuit simulator is essential. The dashed lines refer to a digital approximation for V_{gs} , the inaccuracy of which is further discussed in the text.

while a 250kHz sine signal around $V_{dd}/2$ is applied to the non-inverting input “vinp”. We choose a large amplitude (see Fig. 7, right) of this oscillatory signal and a temperature of 170°C to generate high NBTI stress. A resistor of 1 MΩ and a capacitor of 2pF represent the output load of the amplifier.

A spice simulation for the nominal behavior of the circuit provides the $V_{gs}(t)$ inputs (Fig. 7, right) to our NBTI compact model: the gate-source stress voltages seen by M31 and M32 deviate from the input voltage levels at “vinn” and “vinp” due to the biasing transistors in the amplifier. Therefore, the coupling of the NBTI compact model to an electric circuit simulator is essential. Clearly, M31 sees a non-constant V_{gs} . The V_{gs} stress to M32 is a distorted sine, as noticeable for instance at the beginning of each second half-period.

A. Mean NBTI drift of the amplifier’s offset voltage

From the analog gate-source voltages of Fig. 7, our NBTI compact model calculates the (mean) threshold voltage shift of the transistors M31 and M32 as a function of the circuit operation time (solid lines in Fig. 8). The asymmetric NBTI aging of both transistors generates an offset voltage for the amplifier (solid line in Fig. 9). After 10^4 s of operation, the mean offset voltage μ amounts to $\approx 1mV$; operating the device for three years generates a drastic amplifier mean offset of $\approx 8mV$. Fixing the maximum acceptable offset to 3mV, for instance, the lifetime of the circuit under the present (NBTI enforcing) operation conditions will be $\approx 10^6$ s.

Note that replacing the analog-stress NBTI model by an NBTI model for digital stress leads to large errors: to see this, we approximate the voltages $V_{gs}(t)$ by digital patterns (dashed lines in Fig. 7), i.e. by a time-independent V_{gs} for M31 and by a digital-AC waveform with the same frequency and amplitude as the true signal for M32. The resulting threshold voltage shifts are shown by the dashed lines in Fig. 8, and they significantly deviate from the true ΔV_{th} . As a consequence, the digital model also overestimates the offset voltage drift (dashed line in Fig. 9), mostly because it overestimates the NBTI aging of M32. This discrepancy leads to the (wrong) prediction of reaching a 3mV offset voltage already after 10^5 s, i.e. the digital model drastically underestimates the circuit lifetime by a factor of 10.

B. NBTI variability of the amplifier’s offset voltage

Our method enables furthermore the calculation of the time-dependent NBTI device-to-device variability, beyond the mean drifts determined in the previous subsection. For this, We set up a Monte Carlo (MC) simulation: each MC loop randomly fixes, for each pFET in the circuit, the number of NBTI-relevant defects from a Poisson distribution [14]. The resulting number of defects is then randomly drawn from the set of database defects, such that the defect properties like time “constants” and step heights are random. Finally, each MC loop analyzes the NBTI effect of the present defect configurations with the help of the compact model. The numerical efficiency

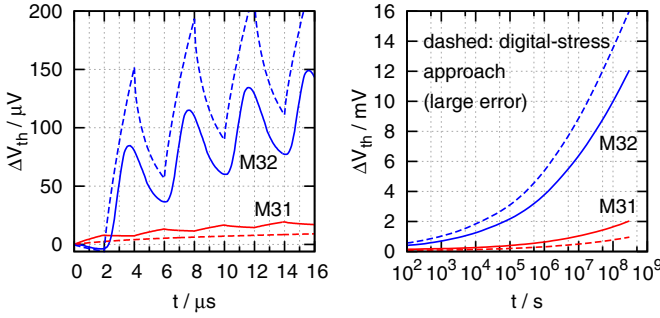


Fig. 8: Compact-model NBTI simulation: mean threshold voltage shift (solid lines) for the input transistors M31 and M32 of the operational amplifier. *Left:* Threshold voltage shift during the first four stress periods. *Right:* Threshold voltage shift after large operation times. Notice that at all time scales the approximation of $V_{gs}(t)$ by a digital pattern (dashed lines) leads to a large error; this finding emphasizes the need for an analog-stress NBTI model.

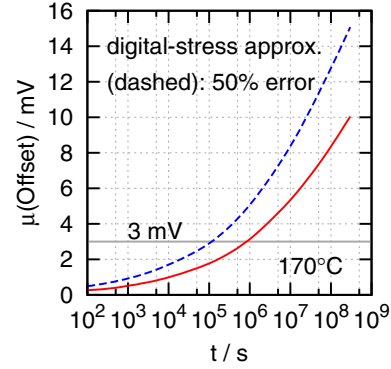


Fig. 9: Drift of the amplifier's mean offset voltage μ (solid line). The digital-stress approach (dashed line) largely underestimates the 3mV-lifetime by a factor of ten (compare intersections with the gray line).

of our model permits a fast calculation even for large circuit operation times (1 year), 10^4 MC loops run in a few seconds on standard single-core hardware. In this way, we have access to the NBTI variability of transistors and of entire circuits.

We illustrate the method on the example of the Miller operational amplifier. Figure 10 shows the probability distribution for the threshold voltage shift of the amplifier input transistors M31 and M32 after one year of circuit operation and for three different transistor sizes. The mean ΔV_{th} was already calculated above and is independent of $W \times L$. However, the transistor size affects the form of the ΔV_{th} distribution: Large devices (dotted line, Fig. 10 left) show a Gaussian-like distribution. In contrast, small devices (solid line in the plots) feature a long tail towards large ΔV_{th} and a peak near 0 mV. Figure 10 (right) shows the ΔV_{th} standard deviation extracted from the distributions: time-dependent NBTI variability increases with stress time and with reduction of the transistor size.

Notice that the probability of M32 having a $\Delta V_{th} < 0$ does not vanish (mid plot in Fig. 10), though is quite small. Such a behavior is not encountered in digital NBTI models [14]. It goes back to the strong recovery phases in the M32 $V_{gs}(t)$ pattern (Fig. 7), which produce this effect for very particular defect configurations.

V. CONCLUSIONS

The present analog-stress NBTI study demonstrates the consistency of three approaches, namely experiment, microscopic multi-state TCAD model and compact model. The encountered large error of a digital-stress approximation emphasizes the need for a novel compact model suitable for the analysis of

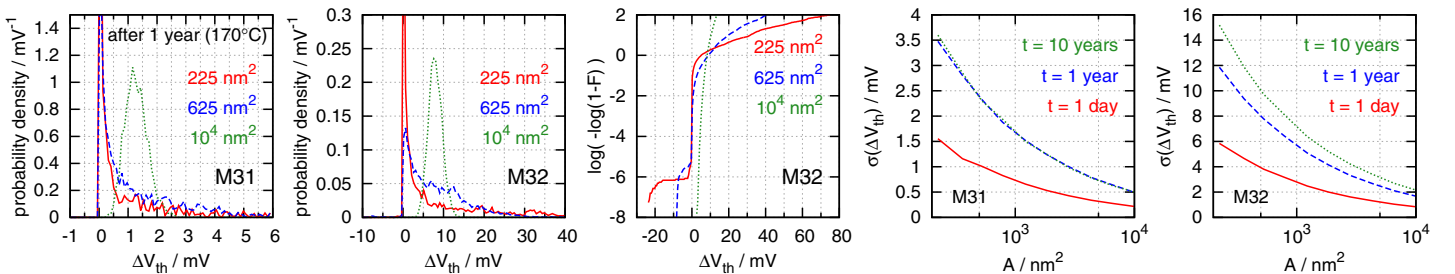


Fig. 10: The compact model provides access to the statistical variability of NBTI threshold voltage shifts. *Left:* The ΔV_{th} probability distribution of the amplifier pFETs M31 and M32 is shown for a circuit operation time of 3×10^7 s and for three device sizes $W \times L / \text{nm}^2 = 225, 625, 10^4$ (top-down). Large devices (dotted line) show a Gaussian-like distribution. In contrast, small devices (solid line) feature long tails and a peak near $\Delta V_{th} = 0$ mV. Since the analog stress pattern contains strong recovery phases (Fig. 7), the distribution does not vanish for $\Delta V_{th} < 0$, see the cumulative probability F given in the mid plot. However, the distribution is quite small for these ΔV_{th} values. *Right:* Standard deviation σ of ΔV_{th} for the transistors M31 and M32. The plots show $\sigma(\Delta V_{th})$ as a function of the device size $A = W \times L$ for three operation times t .

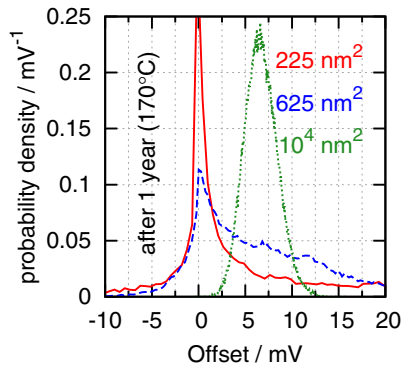


Fig. 11: Variability of the amplifier offset voltage: offset probability distribution after one year of operation. The different electrical stress conditions (Fig. 7) for M31 and M32 lead to a time-dependent mismatch. Small devices feature long tails towards large offsets and a sharp peak near 0 mV.

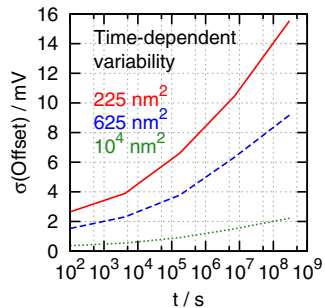


Fig. 12: Time-dependent NBTI variability: Standard deviation σ of the amplifier's offset voltage as a function of circuit operation time t and for three device sizes $W \times L / \text{nm}^2 = 225, 625, 10^4$ (top-down). For small devices, σ is much larger than the mean value μ , compare Fig. 9.

analog circuits. This compact model is numerically efficient and therefore convenient for NBTI-aware analog or digital design: all simulations presented here run in less than 10s. Finally, our compact model provides access to the time-dependent NBTI variability of deeply scaled pFET devices and of entire analog (and digital) circuits.

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