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Nanoelectronics with Spin

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The breath-taking increase in performance of nanoelectronic circuits has been continuously supported by the uninterrupted miniaturization of devices and interconnects. Among the most crucial technological changes lately adopted by the semiconductor industry is the introduction of a new type of multi-gate three-dimensional (3D) transistors [1]. This technology combined with strain techniques and high-k dielectrics/metal gates offers great performance and power saving advantages over the planar structures and allows continuing scaling down to 14nm feature size and beyond. In order to continue with scaling further, a new material with improved transport characteristics for the channel must be introduced [2]. Although single devices with gate length as short as a few nanometers have been demonstrated [3], fabrication, control, and integration costs combined with reliability issues will gradually bring conventional transistor scaling to an end. The principle of transistor operation is fundamentally based on the charge of an electron interacting with the gate voltage induced electrostatic field. Another intrinsic electron characteristic, the electron spin, attracts at present much attention as a possible candidate for complementing or even replacing the charge degree of freedom in future electronic devices. The electron spin state is characterized by two projections on an axis and could be potentially used in digital information processing. In addition, it takes an amazingly small amount of energy to invert the spin orientation. The key advantages of all spin-based computing as compared to a conventional processor with equivalent functions are zero static power, small device count, and low supply voltage, as listed in a recent review [4].

Silicon, the most important material of electronics, predominantly consists of nonmagnetic $_{28}$Si nuclei and is characterized by weak spin-orbit interaction. Because of these properties the electron spin lifetime in silicon is relatively long. This makes silicon a perfect candidate for spin-driven device applications. However, even a demonstration of basic elements necessary for spin-related applications, such as spin injection, detection, and propagation was missing until recently. The fundamental reason has been identified as an impedance mismatch problem [5]. Even though there is a large spin imbalance between the majority and minority spins in a metal ferromagnet, both channels with spin-up and spin-down are equally populated in a semiconductor due to the small density of states as compared to that for the minority spins in a ferromagnet. In other words, because of the large resistance of the semiconductor, the voltage applied to the contact between the ferromagnet and the semiconductor drops completely within the semiconductor, and the properties of the contact are dominated by the non-magnetic semiconductor, thus resulting in a current without spin polarization. A solution to overcome this problem is to use the hot electron injection [6]; however, the efficiency of spin injection and detection is low. Another solution to the impedance mismatch problem is the introduction of a potential barrier between a metal ferromagnet and a semiconductor [7]. In this case the influx of carriers from the ferromagnet into the semiconductor is reduced proportionally to the ration of the densities of states in a semiconductor and a ferromagnet. This guarantees the spin injection into the semiconductor. A successful experimental proof of spin injection at low temperature from an iron electrode through aluminium oxide [8] was demonstrated in 2007. At room temperature spin injection into n- and p-doped silicon was shown in 2009 [9]. The authors used heavily doped silicon samples to avoid an extended depletion layer causing large tunnel barriers. The problem of making good contacts with low resistance per area is critical for spin injection. Tunnel contacts made of a single layer graphene [10] have been shown to be close to optimal [11]. Electrical spin injection through silicon dioxide at temperatures as high as 500K has also been demonstrated [12].

Regardless of an ultimate success in demonstrating spin injection into silicon at room temperature, there are unsolved issues, which may compromise the present understanding of the spin injection process in general. One problem is a several orders of magnitude discrepancy between the signal measured in a scheme where the same ferromagnetic contact is used to inject and to measure the spin accumulation and its theoretical value [11]. Similar observations were also made for germanium [13] as well as for other semiconductors [14]. These discrepancies are heavily debated [15], [16], [17] and more research is needed to resolve the controversies. The excess spin is not a conserved quantity: While diffusing, it gradually relaxes to its equilibrium value which

is zero in a nonmagnetic semiconductor. Spin can propagate 350 microns through a silicon wafer at 77K [6]. The spin diffusion length in silicon at room temperature is around 200nm [11]. In a confined electron structure the spin lifetime is further reduced due to the additional spin relaxation at the interfaces [18]. This shortens the spin diffusion length further, which represents a threat for using CMOS transistors for spin-driven applications.

Technologies to boost the spin lifetime are needed. The spin lifetime is determined by the spin-flip processes. Several important spin relaxation mechanisms are identified [19, 20]. The Elliot-Yafet mechanism is mediated by electron-phonon interaction and the intrinsic interaction between the orbital motion of an electron and its spin is responsible for the spin relaxation in silicon [21].The main contribution to the spin relaxation is due to optical phonon scattering between the valleys residing at different crystallographic axis, or f-phonon scattering [22]. Stress lifts the degeneracy between the non-equivalent valleys and can suppress the spin relaxation by a factor of three. The theory of spin relaxation in inversion layers and thin films must account for the most relevant scattering mechanisms, namely electron-phonon interaction and surface roughness scattering. It turns out that in (001) silicon films, where the non-equivalent valley degeneracy is lifted by confinement, the spin lifetime is controlled by the intervalley scattering processes between the equivalent valleys [23]. This is in contrast to the effect on the momentum relaxation time which is determined by the elastic intravalley scattering. Uniaxial stress along [110] direction lifts the remaining degeneracy between the two equivalent valleys thus reducing the intervalley spin relaxation [24]. This results in a giant, close to two orders of magnitude, spin lifetime enhancement [23] at saturation for shear strain values of about 1.5%. At the intermediate strain values the spin lifetime increase is almost exponential. Strain techniques are now routinely used to boost the electron mobility. It is therefore straightforward to apply the same techniques to obtain a spin lifetime close to 1ns required for spin-driven applications in CMOS transistor technology.

For building a SpinFET [25] purely electrical spin manipulation in the channel is required. However, the channel length required to rotate the spin substantially in silicon is several microns and thus too large [26]. The only viable option left to use nanoscale CMOS is likely to convert a MOSFET to a SpinFET by adding the spin degree through introducing ferromagnetic source and drain contacts [27]. The current in this structure depends on the relative orientation of the magnetizations of source and drain paving the path towards programmable nonvolatile logic. The contact magnetization direction can be switched electrically by using spin torque transfer. However, due to the low spin injection efficiency at room temperature, a SpinFET has not yet been realized. Although significant progress in understanding spin injection, transport, and detection in silicon has been achieved, more research is urgently needed to increase the spin injection efficiency at room temperature and to resolve the issue of spin manipulation by pure electrical means. The most viable option for practical spin-driven applications in the near future is to use magnetic tunnel junctions (MTJs). MTJ-based spin transfer torque MRAM is CMOS compatible, non-volatile, and scalable. It is fast and, in addition, characterized by an infinite endurance and high density. 64Mb MRAM arrays are already in production. A combination of an MTJ with a MOSFET opens a new opportunity to built non-conventional non-volatile logic-in-memory systems [28].

Biography:

Professor Siegfried Selberherr was born in Klosterneuburg, Austria, in 1955. He received the degree of *Diplomingenieur* in electrical engineering and the doctoral degree in technical sciences from the *Technische Universität Wien* in 1978 and 1981, respectively. Dr. Selberherr has been holding the *venia docendi* on computer-aided design since 1984. Since 1988 he has been the Chair Professor of the *Institut für Mikroelektronik*. From 1998 to 2005 he served as Dean of the *Fakultät für Elektrotechnik und Informationstechnik*. Prof. Selberherr published more than 350 papers in journals and books, where more than 100 appeared in Transactions of the IEEE. He and his research teams achieved more than 1000 articles in conference proceedings of which more than 150 have been with an invited talk. Prof. Selberherr authored two books and co-edited more than 30 volumes, and he supervised, so far, more than 100 dissertations. His current research interests are modeling and simulation of problems for microelectronics engineering. Prof. Selberherr is a Fellow of the IEEE, a Fellow of the Academia Europaea, a Fellow of the European Academy of Science and Arts, and a Distinguished Lecturer of the IEEE Electron Devices Society.