

Influence of the Free Layer Alignment on the Reliability of a Non-Volatile Magnetic Shift Register

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Due to physical limitations and financial constraints a reduced progress rate through CMOS scaling is foreseeable for the near future. Among the smorgasbord of possible successor technologies, spin-based electronics (spintronics) shows considerable potential. Spintronic devices feature non-volatility, fast switching, high endurance, and CMOS compatibility. First competitive MRAM circuits are already commercially available and more applications will for sure follow soon [1]-[4]. Although promising logic CMOS/spintronic hybrids already exist, they cannot compete with respect to the integration density - one of the keys of success of CMOS technology. In order to enable a higher integration density, we proposed to omit the extra transistors required for the communication between the CMOS and the spintronic circuit parts and shift as much as possible of the CMOS functionality into the spintronic domain. The results are an extremely small non-volatile magnetic flip flop [5], a very compact buffered logic gate grid [6], and a dense shift register [7]. We will present our most recent results related to these novel structures, particularly the reliability of the devices, where the influence of free layer alignment variations appears to be of major importance.

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