

# 2D Materials

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11 July 2016**The role of charge trapping in MoS<sub>2</sub>/SiO<sub>2</sub> and MoS<sub>2</sub>/hBN field-effect transistors**Yury Yu Illarionov<sup>1,2</sup>, Gerhard Rzepa<sup>1</sup>, Michael Waltl<sup>1</sup>, Theresia Knobloch<sup>1</sup>, Alexander Grill<sup>1</sup>, Marco M Furchi<sup>3</sup>, Thomas Mueller<sup>3</sup> and Tibor Grasser<sup>1</sup><sup>1</sup> Institute for Microelectronics (TU Wien), Gusshausstrasse 27-29, 1040 Vienna, Austria<sup>2</sup> Ioffe Physical-Technical Institute, Polytechnicheskaya 26, 194021 St-Petersburg, Russia<sup>3</sup> Institute for Photonics (TU Wien), Gusshausstrasse 27-29, 1040 Vienna, Austria

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**Abstract**  
The commonly observed hysteresis in the transfer characteristics of MoS<sub>2</sub> transistors is typically associated with charge traps in the gate insulator. Since in Si technologies such traps can lead to severe reliability issues, we perform a combined study of both the hysteresis as well as the arguably most important reliability issue, the bias-temperature instability. We use single-layer MoS<sub>2</sub> FETs with SiO<sub>2</sub> and hBN insulators and demonstrate that both phenomena are indeed due to traps in the gate insulator with time constants distributed over wide timescales, where the faster ones lead to hysteresis and the slower ones to bias-temperature instabilities. Our data show that the use of hBN as a gate insulator considerably reduces the number of accessible slow traps and thus improves the reliability. However, the reliability of hBN insulators deteriorates with increasing temperature due to the thermally activated nature of charge trapping.

## Introduction

Molybdenum disulfide (MoS<sub>2</sub>) is currently one of the most promising transition metal dichalcogenides considered for future electronic device applications. Single-layer MoS<sub>2</sub> has a direct bandgap of around 1.85 eV [1, 2], which allows the main limitation of the gapless graphene to be overcome. The first practical realization of a functional single-layer MoS<sub>2</sub> FET [3] in 2011, together with simulations predicting an excellent performance of MoS<sub>2</sub> FETs [4], resulted in a number of other attempts at fabricating related devices with either SiO<sub>2</sub> [5–15], Al<sub>2</sub>O<sub>3</sub> [16–19], HfO<sub>2</sub> [20, 21] or hBN [22] as a gate insulator. The primary focus of these papers was on the analysis of on/off current ratios and mobilities. In addition, several studies on MoS<sub>2</sub> FETs for high-frequency applications [23] and circuit integration [24, 25] have been reported. Although these considerable advances in overall technology of MoS<sub>2</sub> FETs have been achieved, further integration of these devices requires a detailed study of their reliability. In particular, device non-idealities such as hysteresis and especially slow changes in the

transistor characteristics due to bias-temperature instabilities (BTI) have not yet been considered in depth [6, 7, 10, 11, 13, 14, 18, 22]. Existing studies are mostly restricted to a cursory observation of a hysteresis in the gate transfer characteristics for different measurement conditions [6, 7, 13, 18, 22], and typically report a poor hysteresis stability of the analyzed devices. While some more recent works ascribe the hysteresis in MoS<sub>2</sub> FETs to charge trapping at the MoS<sub>2</sub>/SiO<sub>2</sub> interface [26, 27] or intrinsic impact of MoS<sub>2</sub> [28], a more general study based on a reliable experimental technique accompanied with a qualitative analysis is needed. Furthermore, attempts to analyze BTI in MoS<sub>2</sub> FETs are rare [10, 11, 14], although BTI is arguably the most important reliability issue in Si technologies [29]. In Si technologies it is often assumed that BTI is due to slowly charging oxide defects as well as the creation of interface states which result in a threshold voltage shift over time [30–34]. Available studies are limited to MoS<sub>2</sub>/SiO<sub>2</sub> FETs and report considerable threshold voltage shifts without providing a detailed analysis of BTI degradation/recovery dynamics. Furthermore, no analysis of BTI

has been reported for MoS<sub>2</sub> FETs with hBN gate insulators, the arguably most promising material system.

Here we perform a combined study of both the hysteresis and BTI in single-layer MoS<sub>2</sub> FETs with SiO<sub>2</sub>, hBN/SiO<sub>2</sub> and/or hBN insulators, and capture the correlation between these phenomena. Also, we quantify the observed BTI degradation/recovery dynamics using the universal relaxation model [35] which has been previously developed for Si technologies.

## Devices

Our devices are single-layer MoS<sub>2</sub> FETs with SiO<sub>2</sub> and hBN as a gate insulator [36]. The channel length is around 1 μm, while the width for different FETs varies between 4 and 8 μm. The schematic configuration and output and transfer characteristics of our MoS<sub>2</sub> FETs, which look similar to those reported previously [7, 22], can be found in the SI (figures S1 and S2, respectively).

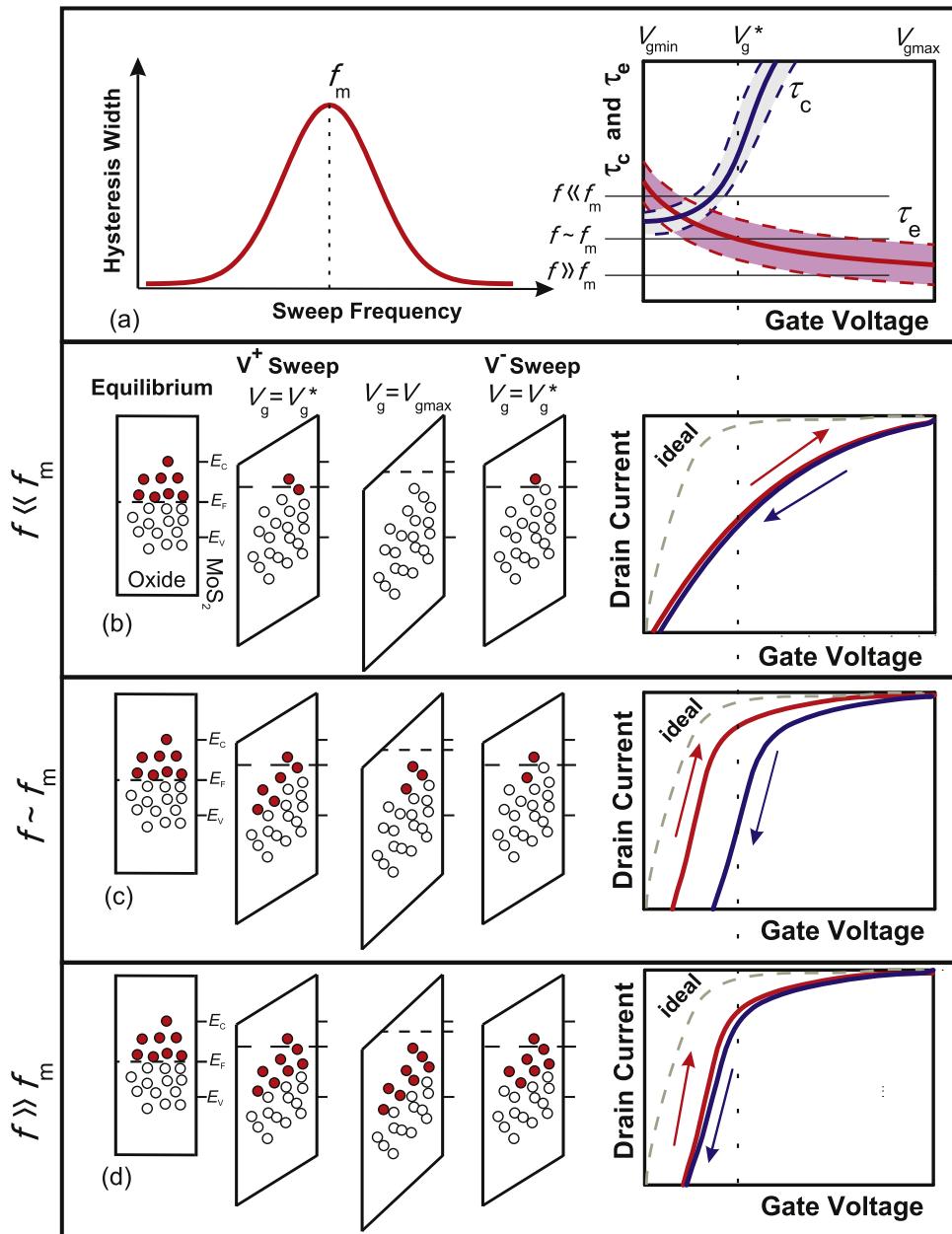
## Results and discussions

We start our study from the qualitative description of the hysteresis and BTI dynamics which are expected in MoS<sub>2</sub> FETs. Based on the results of previous studies for Si technologies [34, 37], we assume initially that both issues are due to the charging/discharging of oxide traps which are situated within a few nanometers from the interface and thus can follow the change in the applied voltage by tunneling exchange with the channel. While some of these traps are introduced by immature processing conditions of the device and can be removed by process optimization, the others present a natural consequence of pairing certain insulator and channel materials and thus remain unavoidable. As shown in figure 1, we assume that the resulting hysteresis width  $\Delta V_H$  extracted from the  $I_d - V_g$  characteristics around the threshold voltage should be strongly dependent on the sweep frequency  $f = 1/t_{sw}$ , with  $t_{sw}$  being the total time required for the whole hysteresis sweep. Furthermore, since the charging/discharging dynamics of oxide traps is determined by the wide distributions of their capture and emission times  $\tau_c$  and  $\tau_e$ ,  $\Delta V_H$  is expected to exhibit a maximum at a certain frequency,  $f = f_m$  (figure 1(a)). This behavior can be explained as follows: if the sweep is too slow and  $f \ll f_m$  (figure 1(b)), those defects which were originally charged in equilibrium discharge during the sweep from  $V_{gmin}$  to  $V_{gmax}$  ( $V^+$  sweep). However, since most of these defects stay below the Fermi level for gate voltages between  $V_g \sim V_g^*$ , which is close to  $V_{th}$ , and  $V_{gmax}$ , they remain discharged during the sweep from  $V_{gmax}$  to  $V_{gmin}$  ( $V^-$  sweep). Hence, the hysteresis around  $V_g = V_g^*$  will be small. Conversely, for faster  $V^+$  sweeps with  $f \sim f_m$  (figure 1(c)) a number of defects

at  $V_g = V_g^*$  will remain charged. Since most of them will have time to discharge by reaching  $V_g = V_g^*$  during the  $V^-$  sweep, one should expect a large hysteresis. Finally, for extremely fast sweeps with  $f \gg f_m$  (figure 1(d)) most defects will retain their equilibrium occupancy, which will again lead to a small hysteresis. Obviously, the exact position and width of the maximum will depend on the distribution of  $\tau_c$  and  $\tau_e$ . As the time constants are thermally activated, a shift of  $f_m$  with temperature is expected. These considerations already reveal the link to reliability issues, as for slow sweeps the transfer characteristics become severely distorted.

In figure 2 we show that the dynamics of BTI in MoS<sub>2</sub> FETs can be explained by assuming charging/discharging of the same defects as those responsible for the hysteresis. Namely, during stress with  $V_g > V_{th}$  (figure 2(a)), which corresponds to positive BTI (PBTI), the Fermi level is shifted toward the conduction band. This leads to discharging of defects which were charged in equilibrium. As a result, the threshold voltage is shifted toward more positive values. However, when the stress is removed the defects above the Fermi level become charged, which leads to the recovery of the  $I_d - V_g$  characteristic. Conversely, during negative BTI (NBTI) stress with  $V_g < V_{th}$  (figure 2(b)) the Fermi level is close to the valence band. Hence, the number of charged defects increases, which makes  $V_{th}$  more negative. Finally, discharging of these defects after the end of the stress leads to recovery of NBTI degradation. Again, the time constants  $\tau_c$  and  $\tau_e$  and the defect concentration  $N_T$  are the main quantities which determine the magnitude and recovery rate of the degradation.

In order to verify the issues discussed above, we have performed qualitative simulations of the hysteresis behavior for different sweep frequencies using our TCAD simulator Minimos-NT [38], which has been previously applied to assess the reliability of modern nanoscale Si MOSFETs [34]. To account for charge trapping, the four-state non-radiative multiphonon model [29] which has been developed to explain the intricate bias and temperature dependence of single traps in SiO<sub>2</sub> [37] is used. The  $\Delta V_H(f)$  dependences extracted from the  $I_d - V_g$  characteristics simulated for an MoS<sub>2</sub>/SiO<sub>2</sub> device with a number of interface and oxide traps are shown in figure 3. In agreement with our qualitative predictions, we observe a clear maximum of  $\Delta V_H$  at moderate frequencies. At higher temperatures this maximum is shifted toward higher  $f$ , which is also intuitive, since the time constants become smaller. At the same time, for narrower sweep ranges the hysteresis is less pronounced, since a narrower active energy region reduces the number of traps which are able to contribute to the hysteresis. Finally, the results clearly show that the hysteresis is fully consistent with trapping/detrapping at oxide traps, which also contribute to BTI. As for the interface traps, since they are very fast, they come into play only

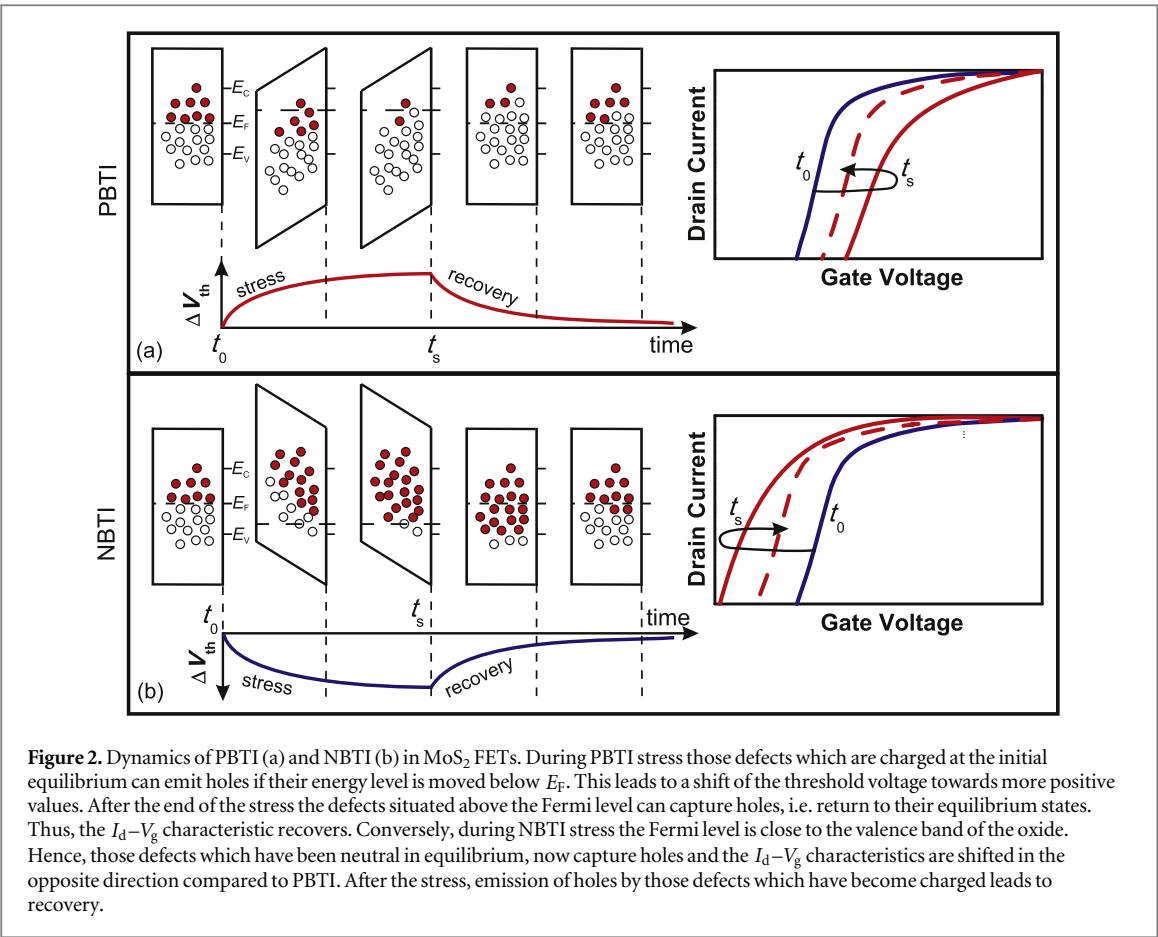


**Figure 1.** (a) Left: schematic dependence of the hysteresis width versus  $I_d - V_g$  sweep frequency in MoS<sub>2</sub> FETs. Right: schematic plot showing the bias dependence of the distributed capture and emission times,  $\tau_c$  and  $\tau_e$ . (b) At low  $f$  some of the traps which are charged at the initial equilibrium have enough time to emit a hole if their energy level moves below  $E_F$  at  $V_g = V_g^*$  during the  $V^+$  sweep. Furthermore, at  $V_g = V_{g\max}$  almost all defects become neutralized. Since within  $V_g^* < V_g < V_{g\max}$  most of the defects are below  $E_F$  and  $\tau_c > \tau_e$ , only very few defects will be charged at  $V_g = V_g^*$  during the  $V^-$  sweep. Hence, the hysteresis at  $V_g = V_g^*$  is small. (c) At moderate  $f$  many defects will not have enough time to emit a hole by reaching  $V_g = V_g^*$  during the  $V^+$  sweep. But as  $V_g$  increases further,  $\tau_e$  of these defects decreases and in addition they have more time to emit. Hence, at  $V_g = V_{g\max}$  many defects will become neutral. However, since  $\tau_c$  is large, most traps will remain neutral at  $V_g = V_g^*$  during the  $V^-$  sweep. Thus, a large hysteresis will be observed. (d) At very high  $f$  most traps, except those with extremely small  $\tau_e$ , will neither emit nor capture a hole because the time constants are large compared to the period  $1/f$ . As a consequence, the hysteresis remains small.

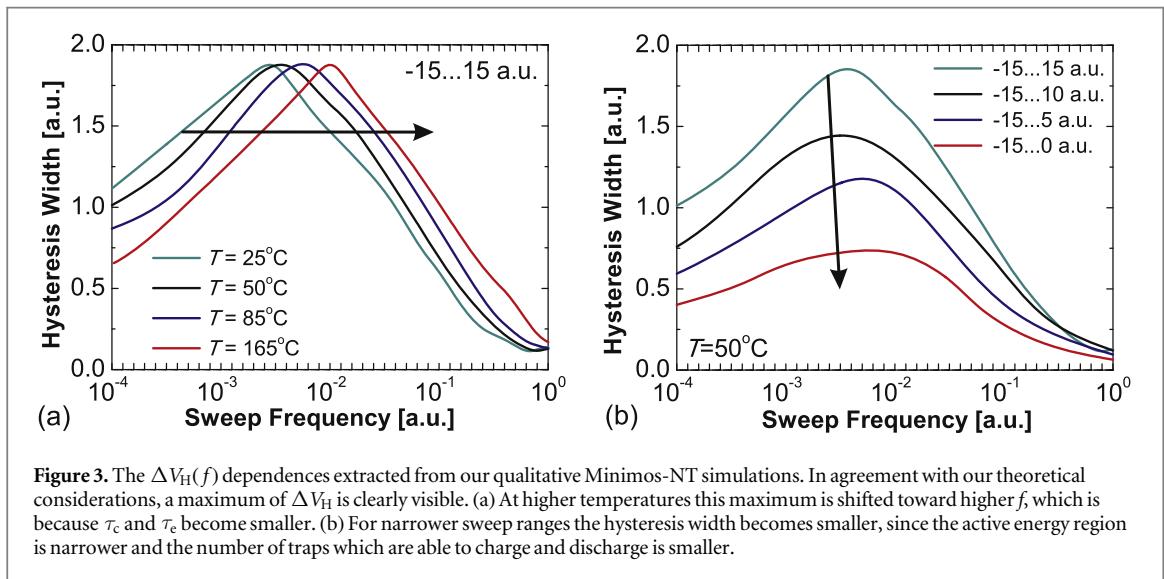
at very high frequencies and introduce some instability below  $V_{th}$  for typical trap levels. As discussed in the SI, the impact of interface states on the transfer characteristics can be simulated by assuming  $f \sim 100$  Hz, which is much larger than the typical sweep frequencies at which the oxide trap hysteresis appears. Furthermore, the results can be reasonably matched to the experimental data measured for our MoS<sub>2</sub>/SiO<sub>2</sub>

FETs using extremely fast sweeps (see figure S3 in the SI).

Based on the qualitative background discussed above, we proceed with the experimental part of our study. In order to avoid the detrimental impact of the environment [7], all our measurements were performed in vacuum ( $5 \times 10^{-6}$ – $10^{-5}$  Torr). The hysteresis was investigated by measuring the  $I_d - V_g$



**Figure 2.** Dynamics of PBTI (a) and NBTI (b) in  $\text{MoS}_2$  FETs. During PBTI stress those defects which are charged at the initial equilibrium can emit holes if their energy level is moved below  $E_F$ . This leads to a shift of the threshold voltage towards more positive values. After the end of the stress the defects situated above the Fermi level can capture holes, i.e. return to their equilibrium states. Thus, the  $I_d-V_g$  characteristic recovers. Conversely, during NBTI stress the Fermi level is close to the valence band of the oxide. Hence, those defects which have been neutral in equilibrium, now capture holes and the  $I_d-V_g$  characteristics are shifted in the opposite direction compared to PBTI. After the stress, emission of holes by those defects which have become charged leads to recovery.

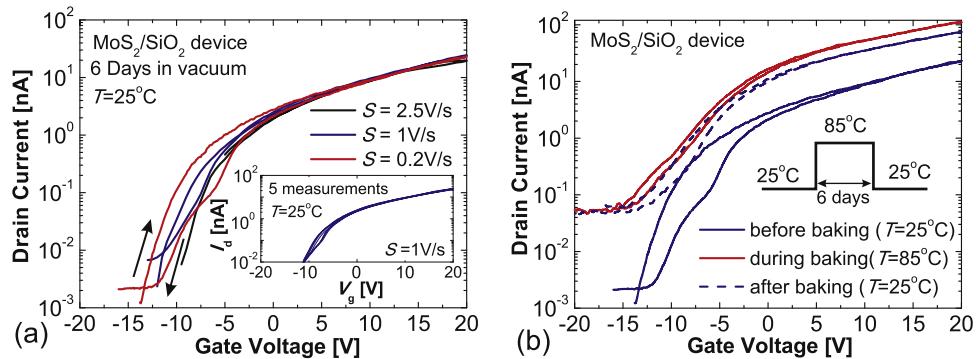


**Figure 3.** The  $\Delta V_H(f)$  dependences extracted from our qualitative Minimos-NT simulations. In agreement with our theoretical considerations, a maximum of  $\Delta V_H$  is clearly visible. (a) At higher temperatures this maximum is shifted toward higher  $f$ , which is because  $\tau_c$  and  $\tau_e$  become smaller. (b) For narrower sweep ranges the hysteresis width becomes smaller, since the active energy region is narrower and the number of traps which are able to charge and discharge is smaller.

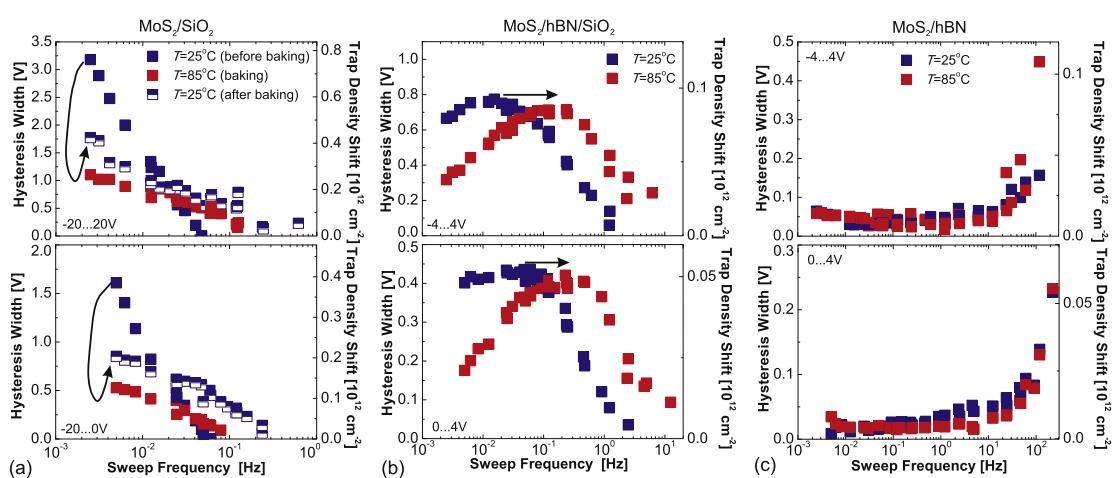
characteristics using  $V_d = 0.1$  V and different sweep rates  $S$ . In order to capture the full frequency range of the traps responsible for the hysteresis,  $S = V_{\text{step}}/t_{\text{step}}$  was varied between 0.04 and 8000 V s $^{-1}$  by adjusting the step voltage  $V_{\text{step}}$  and the sampling time  $t_{\text{step}}$ . It is expected that the use of a smaller  $V_{\text{step}}$  increases the number of accessible traps inside the insulators while an increase in  $t_{\text{step}}$  will allow slower traps to contribute to the hysteresis as well. BTI in our  $\text{MoS}_2$  devices was studied using an experimental technique previously

employed for graphene FETs [39]. Namely, subsequent stress/recovery cycles with either increasing stress time  $t_s$  or gate voltage  $V_g$  were used. By measuring the full  $I_d-V_g$  characteristics of our devices at each recovery stage, we were able to extract the threshold voltage shift  $\Delta V_{\text{th}}$  at a fixed drain current, and express the BTI recovery in terms of  $\Delta V_{\text{th}}$  versus the relaxation time  $t_r$ .

An initial check of our  $\text{MoS}_2/\text{SiO}_2$  devices after several days in a vacuum at  $T = 25^\circ\text{C}$  shows that the



**Figure 4.** (a) The  $I_d$ - $V_g$  characteristics of the  $\text{MoS}_2/\text{SiO}_2$  FET measured with different sweep rates  $S$ . Clearly, the hysteresis becomes more pronounced with smaller  $S$ , revealing an increasing contribution of slower traps. At the same time, at constant  $S$  the hysteresis is stable and well reproducible (inset). (b) At  $T = 85^\circ\text{C}$  the drain current is larger, while the slow sweep hysteresis is significantly reduced. After returning back to  $T = 25^\circ\text{C}$  following six days of measurements,  $I_d$  was considerably larger and  $\Delta V_H$  considerably reduced.



**Figure 5.** (a) The frequency dependence of  $\Delta V_H$  measured for  $\text{MoS}_2/\text{SiO}_2$  FETs using the gate voltage sweep ranges  $-20$  to  $20\text{ V}$  (top) and  $-20$  to  $0\text{ V}$  (bottom). The three datasets correspond to the results obtained before, during and after 6 days of baking at  $T = 85^\circ\text{C}$ . Initially, the hysteresis is dominated by slower traps. During baking, some of these traps become annealed, while those which remain become faster. (b) The frequency dependence of  $\Delta V_H$  measured for  $\text{MoS}_2/\text{hBN}/\text{SiO}_2$  FETs using the sweep ranges  $-4$  to  $4\text{ V}$  (top) and  $0$  to  $4\text{ V}$  (bottom). In agreement with our qualitative predictions, we observe a maximum of  $\Delta V_H$ . At  $T = 85^\circ\text{C}$  the maximum is shifted toward higher  $f$ . (c) The corresponding results for  $\text{MoS}_2/\text{hBN}$  FETs. Contrary to the previous two devices, the fraction of slower traps is negligible, while the hysteresis is dominated by ultra-fast traps. Hence, the maximum of  $\Delta V_H$  is most likely at even higher frequencies outside our measurements range.

$I_d$ - $V_g$  characteristics exhibit some hysteresis. While being reproducible at a constant sweep rate, similarly to [7], this hysteresis becomes larger when  $S$  is decreased (figure 4(a)). When the temperature is increased to  $85^\circ\text{C}$ , the drain current increases (figure 4(b)). At the same time, the hysteresis width  $\Delta V_H$  measured using a very small  $S$  significantly decreases. However, when after six days at  $85^\circ\text{C}$  the temperature was changed back to  $25^\circ\text{C}$ , neither drain current nor hysteresis width returned back to their initial values. Thus, after baking, the device exhibits better performance in terms of both  $I_d$  and  $\Delta V_H$ . This implies that in our  $\text{MoS}_2/\text{SiO}_2$  FETs, baking anneals a considerable fraction of slower traps (see more details in the SI, figure S4). We speculate that these slower traps are associated with water molecules [7], which

are desorbed from the uncovered  $\text{MoS}_2$  surface at higher temperatures.

We proceed with a more detailed analysis of the hysteresis by measuring the  $I_d$ - $V_g$  characteristics using different  $t_{\text{step}}$ ,  $V_{\text{step}}$  and gate voltage sweep intervals  $V_{g\min}$  to  $V_{g\max}$ . In order to allow for a qualitative interpretation of our results and their comparison for different gate insulators, we operate with the sweep frequency  $f = 1/t_{\text{sw}}$ , where the sweep time  $t_{\text{sw}} = N t_{\text{step}}$  and the number of points  $N = 2 ((V_{g\max} - V_{g\min})/V_{\text{step}} + 1)$ . In figure 5 we show that for all three insulators the hysteresis widths measured using different  $V_{\text{step}}$  and  $t_{\text{step}}$  form a universal frequency dependence of  $\Delta V_H$ , while the typical charge trap density shifts  $\Delta N_{\text{th}} = \Delta V_H C_{\text{ox}}/q$  are comparable to those reported in [19]. Figure 5(a) shows the  $\Delta V_H(f)$  dependences measured for  $\text{MoS}_2/\text{SiO}_2$  FETs

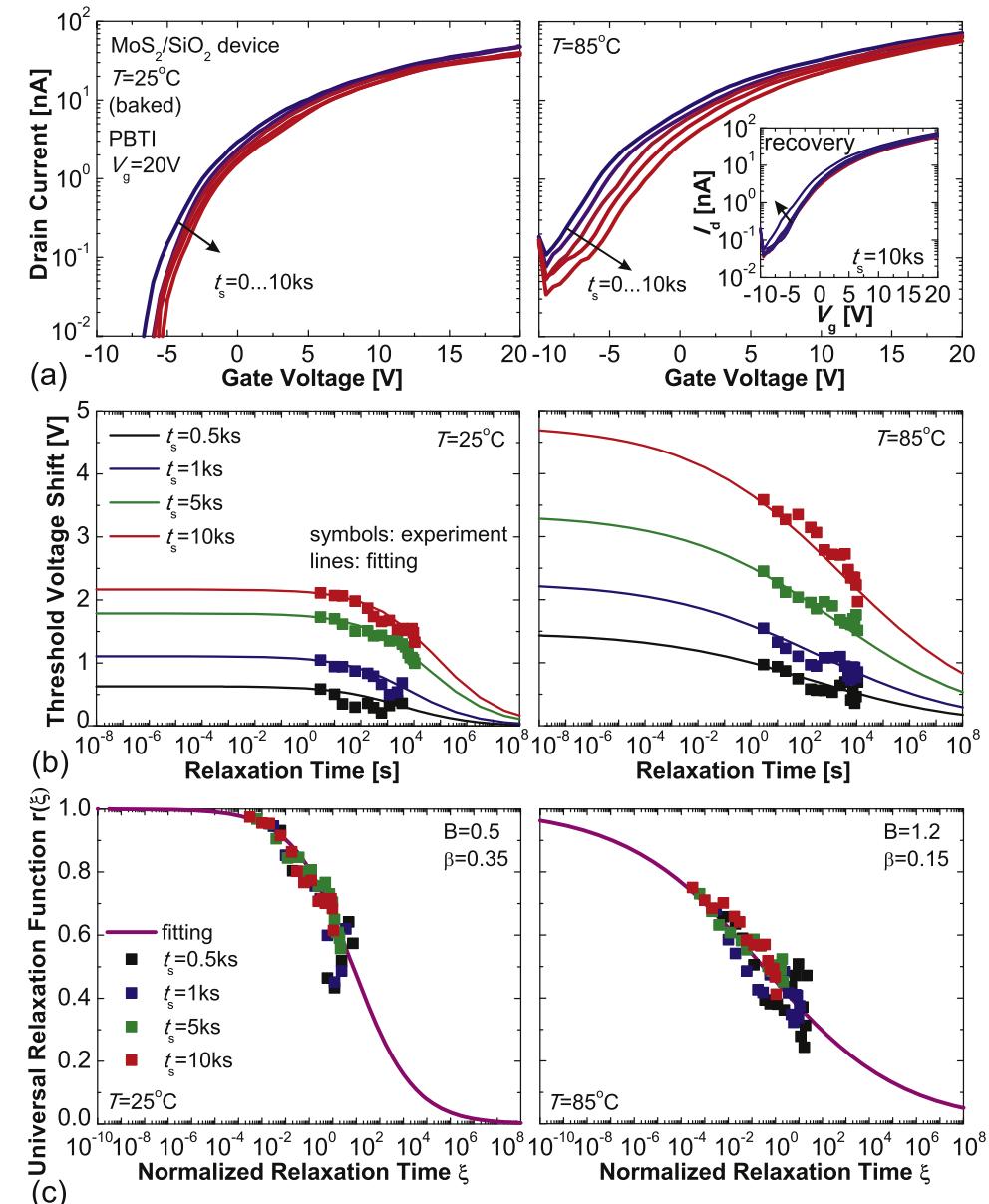
at  $T = 85^\circ\text{C}$  and also at  $T = 25^\circ\text{C}$  before and after the  $T = 85^\circ\text{C}$  measurements. In all cases  $\Delta V_{\text{H}}$  becomes larger for lower frequencies, which confirms that the hysteresis in these devices is dominated by slower traps with  $f < 0.01\text{ Hz}$ . Hence, within our measurement range we observe only the right part of the  $\Delta V_{\text{H}}(f)$  maximum, as predicted by theory (figure 3). At the same time, the contribution of faster traps ( $0.01\text{ Hz} < f < 1\text{ Hz}$ ) becomes more pronounced at  $T = 85^\circ\text{C}$ . This also agrees with the theoretical prediction, showing that the  $\Delta V_{\text{H}}(f)$  maximum at higher temperatures is shifted toward higher frequencies. Conversely,  $\Delta V_{\text{H}}$  associated with slower traps is considerably reduced during and after baking at  $T = 85^\circ\text{C}$ , which means that a number of traps have been annealed. Hence, we stipulate that in our  $\text{MoS}_2/\text{SiO}_2$  FETs the hysteresis is not only due to oxide traps, but also due to defects situated on top of the non-covered  $\text{MoS}_2$  surface (e.g. water molecules), which have not been accounted for in our simulations (see figure S5 in the SI). In figure 5(b) we provide the corresponding results for  $\text{MoS}_2/\text{hBN}/\text{SiO}_2$  FETs. Contrary to  $\text{MoS}_2/\text{SiO}_2$  devices, here we observe a clear maximum of  $\Delta V_{\text{H}}(f)$ , which again fully agrees with our qualitative predictions. Also, the presence of the whole maximum means that the typical time constants of the defects in  $\text{MoS}_2/\text{hBN}/\text{SiO}_2$  devices are smaller compared to their  $\text{MoS}_2/\text{SiO}_2$  counterparts. Furthermore, at  $T = 85^\circ\text{C}$  the maximum is shifted toward higher frequencies, which has been confirmed using different sweep ranges. As such, we conclude that all traps which contribute to the hysteresis in  $\text{MoS}_2/\text{hBN}/\text{SiO}_2$  FETs are thermally activated, which fully agrees with theory. The results for  $\text{MoS}_2/\text{hBN}$  FETs are shown in figure 5(c). Contrary to the previous two cases, the hysteresis in  $\text{MoS}_2/\text{hBN}$  FETs is dominated by ultra-fast traps ( $f > 1\text{ Hz}$ ), while the contribution of slower traps is negligible. Hence, the typical time constants of the defects for these devices are the smallest. At the same time, an increase of  $\Delta V_{\text{H}}$  for higher  $f$  means that only the left part of the maximum can be captured within our measurement range. Interestingly, for all three cases the same trends are observed independently of the gate voltage sweep range, and in agreement with our simulations (figure 3(b)) and [13]  $\Delta V_{\text{H}}$  becomes smaller for narrower sweep ranges.

A comparison of our findings for different gate insulators allows us to conclude that for  $\text{MoS}_2/\text{SiO}_2$  FETs the hysteresis is mostly dominated by slower traps. Hence, only the right part of the  $\Delta V_{\text{H}}$  maximum lies within our measurement range. Conversely, the defects in  $\text{MoS}_2/\text{hBN}/\text{SiO}_2$  devices have smaller time constants, which allows us to observe the maximum of  $\Delta V_{\text{H}}$ . Finally, for  $\text{MoS}_2/\text{hBN}$  devices we observe only the left edge of the maximum, since the hysteresis is purely related to ultra-fast traps (the transfer characteristics for  $\text{MoS}_2/\text{hBN}/\text{SiO}_2$  and  $\text{MoS}_2/\text{hBN}$  devices can be found in the SI, figure S6). Interestingly, in

all three cases the time constants of the involved traps become smaller at higher temperature, as expected by theory. At the same time, our devices exhibit a better hysteresis stability compared to results reported by other groups (for more details see figure S7 and related discussion in the SI).

We proceed with an analysis of the degradation/recovery dynamics of NBTI and PBTI for our  $\text{MoS}_2/\text{SiO}_2$  and  $\text{MoS}_2/\text{hBN}$  FETs. As stated before, as hysteresis and BTI are due to the same defects, the features observed in the hysteresis should be consistent with the BTI results, bearing in mind that BTI in our slow measurements is dominantly due to slow oxide traps. First we have found that the BTI degradation in our  $\text{MoS}_2$  FETs is strongly dependent on the magnitude of applied bias stress. Similarly to Si technologies [34], for larger  $V_g$  the degradation is stronger and more recoverable (see figure S8 in the SI). In figure 6 we show the results obtained for our  $\text{MoS}_2/\text{SiO}_2$  FETs using subsequent PBTI stress/recovery cycles with increasing  $t_s$ . In order to compare the BTI degradation/recovery dynamics with Si technologies, we use the universal relaxation model [35]. This model assumes the normalized recovery  $\Delta V_{\text{th}}(t_r)/\Delta V_{\text{th}}(t_r = 0)$  to follow  $r(\xi) = 1/(1 + B\xi^\beta)$  with the normalized relaxation time  $\xi = t_r/t_s$  and empirical fitting parameters  $B$  and  $\beta$ . All recovery traces for our  $\text{MoS}_2/\text{SiO}_2$  devices can be fitted reasonably well (figure 6(b)), since the normalized recovery is universal (figure 6(c)). Just like in Si technologies, stronger degradation and faster recovery are observed at higher  $T$ , which is due to the thermally activated nature of charge trapping [29]. This agrees with our hysteresis measurements and qualitative simulations, which show that at higher  $T$  traps become faster (see figures 3 and 5). However,  $\text{MoS}_2$  FETs are known to exhibit both PBTI and NBTI on the same device [11, 14]. While the dynamics of NBTI are similar to those of PBTI, the observed shifts are larger (the results are given in the SI figure S9). The latter means that at the initial equilibrium state the concentration of charged defects is smaller than that of neutral defects. Hence, as was shown in figure 2, trapping of holes at negative  $V_g$  is more favorable than their emission at positive  $V_g$  with the same absolute value.

In figure 7 we provide the results for PBTI and NBTI measured for our  $\text{MoS}_2/\text{hBN}$  FETs. While these devices exhibit a negligible degradation at  $T = 25^\circ\text{C}$ , at  $T = 85^\circ\text{C}$  both PBTI and NBTI shifts become more pronounced and agree with the universal model. Also, the use of this model allows us to extrapolate initial shifts  $\Delta V_{\text{th}}(t_r = 0)$  for both  $\text{MoS}_2/\text{SiO}_2$  and  $\text{MoS}_2/\text{hBN}$  FETs and further verify the thermally activated nature of charge trapping (see the results in the SI figure S10). Interestingly, the  $\text{MoS}_2/\text{hBN}$  device remains considerably more stable than its  $\text{MoS}_2/\text{SiO}_2$  counterpart even at  $T = 165^\circ\text{C}$ , although the BTI shifts are further increased (see figures S11–S13 in the SI). At the same time, NBTI in



**Figure 6.** (a) Degradation of the gate transfer characteristics of the  $\text{MoS}_2/\text{SiO}_2$  FET after subsequent PBTI stresses with  $V_g = 20\text{ V}$  and increasing  $t_s$  at  $T = 25^\circ\text{C}$  (left) and  $T = 85^\circ\text{C}$  (right). (b) The resulting  $\Delta V_{th}$  recovery traces can be fitted using the universal relaxation model [35]. (c) The normalized recovery traces follow the universal relaxation relation. Similarly to Si technologies, at higher  $T$ , degradation is stronger and the degree of recovery is larger. The parameters  $B$  and  $\beta$  are very similar to those obtained from Si data (figure 8), which confirms the similarity in the underlying physical degradation processes.

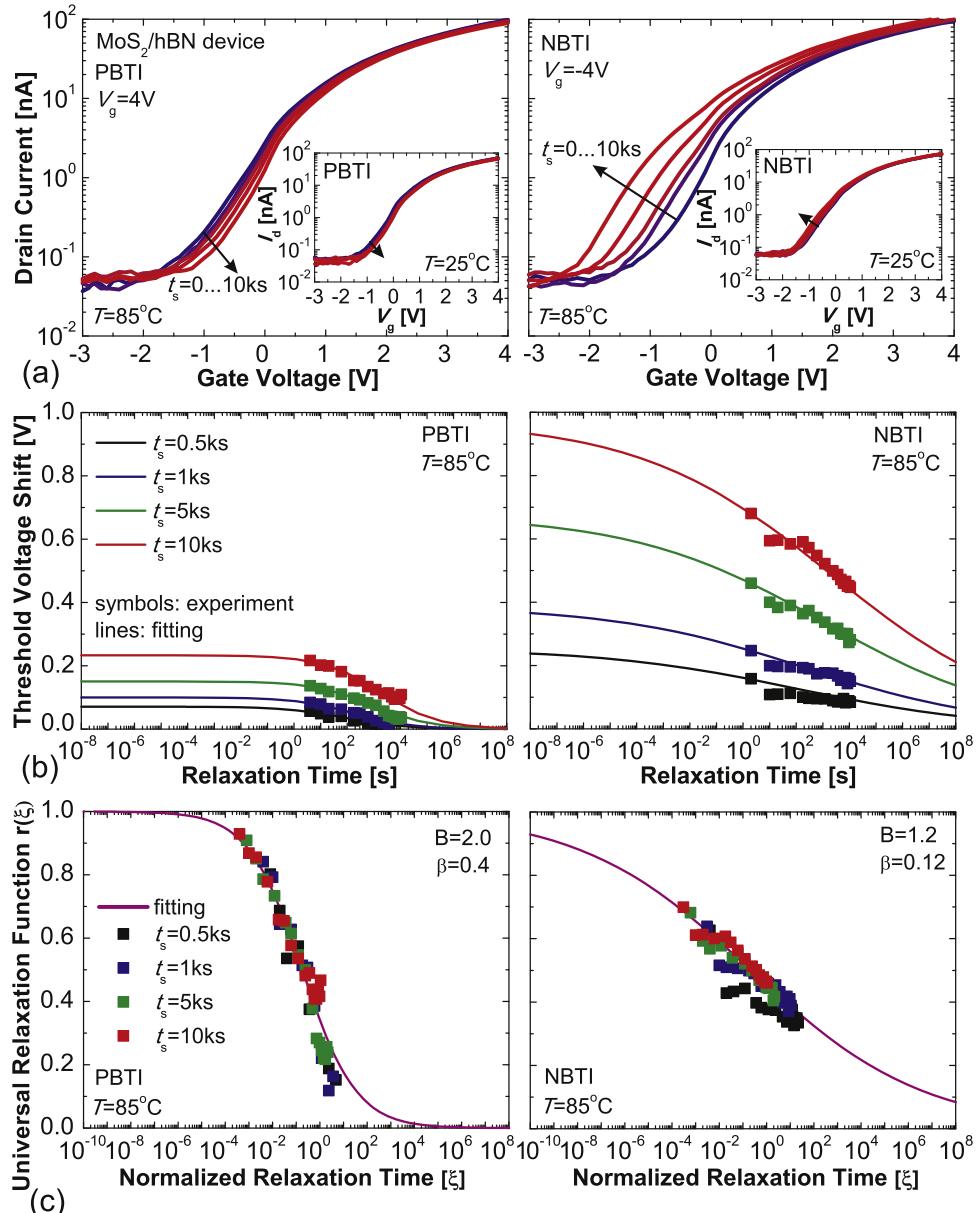
$\text{MoS}_2/\text{hBN}$  devices is stronger than PBTI, which is similar to  $\text{MoS}_2/\text{SiO}_2$  FETs.

Figure 8(a) shows that the parameters  $B$  and  $\beta$  which have been used for fitting of the PBTI and NBTI recovery traces of our  $\text{MoS}_2$  FETs are very similar to those previously used for Si technologies and graphene FETs. This indicates a similarity in the physical processes underlying the BTI dynamics. In figure 8(b) we compare the normalized  $\Delta V_{th}$  measured within this work with the results from [11, 14]. Clearly, our  $\text{MoS}_2/\text{SiO}_2$  FETs show better stability with respect to PBTI stress, while the  $V_{th}$  shifts caused by NBTI are comparable to previous literature reports. The smallest PBTI shifts are likely because of the higher quality

of the  $\text{MoS}_2/\text{SiO}_2$  interface, which has been achieved by careful processing and annealing of our devices in vacuum. At the same time, hBN devices exhibit the best BTI reliability. This is in agreement with our hysteresis results, showing that the amount of accessible slow traps in  $\text{MoS}_2/\text{hBN}$  FETs is considerably smaller than in  $\text{SiO}_2$ .

## Conclusions

In summary, we have performed a comprehensive study of the hysteresis and the slow drifts due to the bias-temperature instability in  $\text{MoS}_2$  FETs and found that both issues are dominated by thermally activated



**Figure 7.** (a) Degradation of the gate transfer characteristics of the  $\text{MoS}_2/\text{hBN}$  FET after subsequent PBTI (left) and NBTI (right) stresses at  $T = 85^\circ\text{C}$ . The insets show that the degradation observed after both PBTI and NBTI at  $T = 25^\circ\text{C}$  is significantly smaller. (b) The  $\Delta V_{th}$  recovery traces at  $T = 85^\circ\text{C}$  can again be well fitted using the universal relaxation model as the normalized recovery is universal (c). Similarly to  $\text{MoS}_2/\text{SiO}_2$  devices, the threshold voltage shifts are larger for NBTI than for PBTI and more recoverable. Also, the significant increase in the drifts of the  $\text{MoS}_2/\text{hBN}$  devices at higher  $T$  agrees with the increased hysteresis.

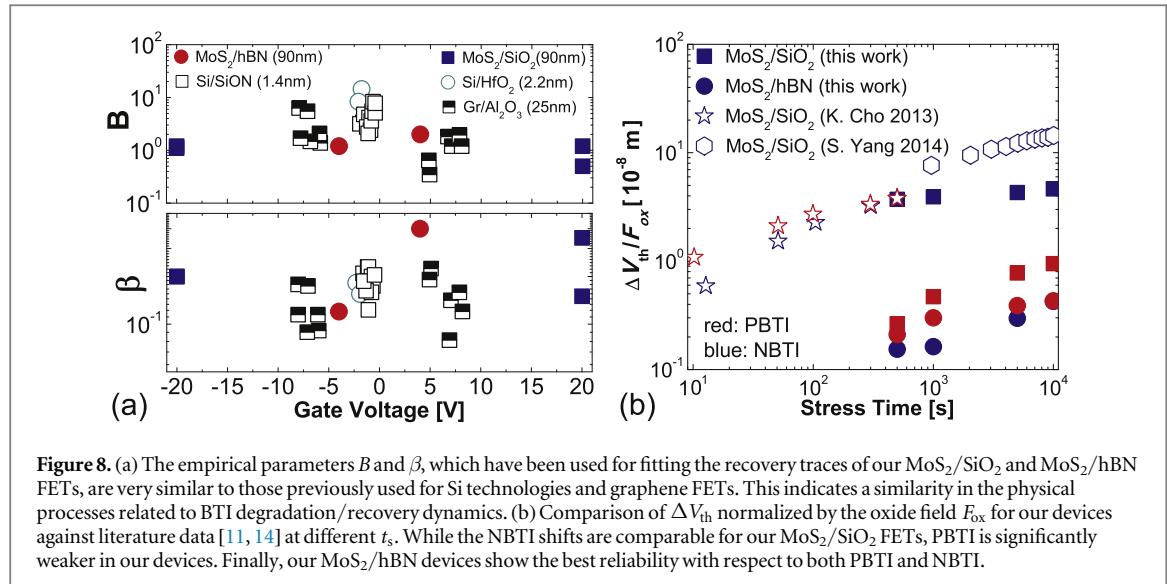
charging/discharging of oxide traps. Also, if the  $\text{MoS}_2$  channel is not covered, the trapping sites situated on top of it can contribute to the hysteresis as well. While our  $\text{MoS}_2$  FETs with  $\text{SiO}_2$  and hBN exhibit a smaller hysteresis and better BTI stability than similar devices reported by other groups, hBN as a gate insulator reduces the impact of slow traps and improves the BTI reliability. Furthermore, we found that the main reliability issue in the most promising  $\text{MoS}_2/\text{hBN}$  FETs is associated with ultra-fast traps, although at higher  $T$  the BTI reliability of hBN is reduced due to thermally activated charge trapping. Also, we have demonstrated that the BTI recovery traces measured for all our  $\text{MoS}_2$  FETs follow the universal relaxation

relation previously developed for Si technologies. Together with our previous results for graphene FETs [39], this underlines that the BTI degradation/recovery dynamics in next-generation 2D FETs are similar to their counterparts in Si technologies.

## Methods

### Device fabrication

The  $\text{MoS}_2/\text{SiO}_2$  devices were fabricated on double side polished and thermally oxidized Si substrates with a resistivity of  $1\text{--}5\ \Omega\text{ cm}$  and  $\text{SiO}_2$  thickness of 90 nm.  $\text{MoS}_2$  flakes were mechanically exfoliated from a natural bulk crystal on top of a  $\text{SiO}_2$  layer using the



**Figure 8.** (a) The empirical parameters  $B$  and  $\beta$ , which have been used for fitting the recovery traces of our  $\text{MoS}_2/\text{SiO}_2$  and  $\text{MoS}_2/\text{hBN}$  FETs, are very similar to those previously used for Si technologies and graphene FETs. This indicates a similarity in the physical processes related to BTI degradation/recovery dynamics. (b) Comparison of  $\Delta V_{th}$  normalized by the oxide field  $F_{ox}$  for our devices against literature data [11, 14] at different  $t_s$ . While the NBTI shifts are comparable for our  $\text{MoS}_2/\text{SiO}_2$  FETs, PBTI is significantly weaker in our devices. Finally, our  $\text{MoS}_2/\text{hBN}$  devices show the best reliability with respect to both PBTI and NBTI.

method of [40]. After that, the flakes with the best quality were selected using an optical microscope and their final thickness was determined by Raman spectroscopy to identify single-layer  $\text{MoS}_2$  (i.e. around 6.5 Å). Then Ti/Au electrodes were created by electron beam lithography and metal evaporation techniques (e.g. [7]). In the case of  $\text{MoS}_2/\text{hBN}$  devices, a 22 nm thick Ti/Au back gate pad was evaporated on top of a 90 nm thick  $\text{SiO}_2$  layer. Next, the hBN/ $\text{MoS}_2/\text{hBN}$  stack produced using the stacking method [41, 42] was placed on top of the Ti/Au pad. The essential ingredients of this stack are mechanically exfoliated single-layer  $\text{MoS}_2$  flakes and two 90 nm thick hBN layers, also obtained from bulk hBN crystals using mechanical exfoliation. While single-layer  $\text{MoS}_2$  flakes were identified using Raman spectroscopy, the thickness and quality of hBN flakes were controlled using atomic-force microscopy. Also, those hBN flakes which were used as the uppermost layer were pre-structured by electron beam lithography and reactive ion etching in order to create the slots for source and drain contacts. Finally, our  $\text{MoS}_2$  FETs have been annealed in vacuum ( $< 5 \times 10^{-6}$  Torr,  $T = 120^\circ\text{C}$ ) during 12 hr.

### Experimental technique

All our measurements have been performed using a Keithley-2636A in a chamber of a Lakeshore vacuum probestation ( $5 \times 10^{-6}$ – $10^{-5}$  Torr). For a detailed analysis of the hysteresis behavior, we measured the transfer characteristics of our  $\text{MoS}_2/\text{SiO}_2$  FETs in both sweep directions using the sweep ranges –20 to 20 V and 0 to 20 V; for the  $\text{MoS}_2/\text{SiO}_2/\text{hBN}$  and  $\text{MoS}_2/\text{hBN}$  devices the sweep ranges –4 to 4 V and 0 to 4 V have been used. At the same time, the sweep rate  $S = V_{step}/t_{step}$  has been varied from 0.04 to 8000 V s<sup>-1</sup> by changing the sampling time  $t_{step}$  and the step voltage  $V_{step}$ . For each of the measured  $I_d-V_g$  characteristics we extracted the hysteresis width  $\Delta V_H$

around the threshold voltage. Next, the dependences of  $\Delta V_H$  on the measurement frequency  $f = 1/(N t_{step})$  with the number of voltage step points  $N = 2((V_{gmax} - V_{gmin})/V_{step} + 1)$  have been analyzed at different temperatures.

The BTI degradation/recovery dynamics have been studied using subsequent stress/recovery rounds with increasing stress times at  $T = 25^\circ\text{C}$ ,  $T = 85^\circ\text{C}$  and  $T = 165^\circ\text{C}$  (for  $\text{MoS}_2/\text{hBN}$  device). The full  $I_d-V_g$  characteristics have been measured at each degradation/recovery stage. This typically introduces a measurement delay of about 3 s.

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