Chapter 2

Device physics, modeling, and technology for nano-scaled semiconductor devices

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This chapter introduces the device physics, modeling, and technology for the different silicon-based device structures. Quantum-mechanical treatment for the device physics is done as well as the different and alternative approaches for advanced device simulation. The last section takes over the potential use that can be given to new materials and device structures. A preliminary set of applications are reviewed, such as Si-based materials with nanostructured properties, amorphous SiGe alloys applications such as thermal and photodetector sensors. Furthermore, the possibility to make use of CMOS fabrication steps for 3D Si die stacking is also reviewed.

2.1 Bulk MOSFETs and related device structures

The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) has been and still is the workhorse device behind the semiconductor industry. The MOSFET was born in the United States under the fatherhood of Atalla and Kahng in 1960 [2.1], but its birth certificate was issued until 1963 as a patent number 3,102,230 [2.2]. Once the MOSFET showed good and reproducible electrical characteristics, the idea to form a circuit composed of multiple field-effect transistors (FETs) flourished with the realization of a commercial integrated circuit (IC) in 1963. Later in 1968 RCA produced the first commercial IC made of 120 p-type FETs as a 20-bit shift register [2.3]. Later in 1968 RCA produced the first commercial complementary metal-oxide-semiconductor (CMOS) IC, the 4000 series of CMOS logic gates [2.4]. Of course the concept of the IC is attributed to Jack Kilby who in 1958 patented the idea [2.5], and later in 2000 was granted the Nobel Prize. In 1963 Wanlass and Sah also introduced [2.6], in an experimental way, a set of CMOS logical gates, flip-flops, and ring oscillator with a maximum operating voltage of 40 V.

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This technology showed a transconductance $g_m = 5 \times 10^{-4}$ A/V, and a leakage current for a single inverter that would amount to 1 W of standby power for 10^7 inverters, which is about 100 nW per inverter, or 2.5 nA leakage current per inverter. The propagation delay time is about 100 ns. While today a 28 nm CMOS technology, for instance, can have a $g_m = 7 \times 10^{-3}$ A/V, and a delay time in the order of ps.

In the two following sections a description of the conventional FET physics and its limitations will be introduced, and then alternative FET-related structures that alleviate the limited electrical performance of traditional FET devices are introduced in the second section. In the subsequent sections advanced FET-related devices, quantum effects, different approaches for semiconductor modeling and simulation, alternative materials and device structures, are reviewed.

2.1.1 *Conventional field-effect transistor (FET) physics and limitations*

As already mentioned the MOSFET concept was demonstrated in early 1960s based on the surface semiconductor charge controlled by the electric field as shown in Figure 2.1.

The charge Q_s at the semiconductor surface, close to the semiconductor–gate oxide interface, is controlled by the electric field E_y in the y-axis as shown at the right side, which in turn is controlled by the gate (G) voltage. However, when a potential difference between the drain (D) and source (S) electrodes increases (in the x-axis direction), the charge Q_s becomes dependent of both electric field components, E_y and E_x. Basically what we have is a cloud of charges, either electrons or holes, that modulates the drain-source conductance controlled by the four potentials V_G, V_S, V_D, and V_B. In a conventional MOSFET of the 1980s–1990s, with a typical channel length L from 10 to 0.5 μm, a gate oxide T_{ox} from some 60 nm down to 14 nm, the electrical characteristics are like those depicted in Figure 2.2. Both are conventional, non-LDD, polysilicon gate technologies, with a SiO_2 gate oxide.

These are well-behaved MOSFETs with electrical characteristics close to the ideal behavior for non-low-voltage analog applications. The 10 μm transistor has been fabricated with an experimental process at INAOE [2.7], while the 0.5 μm

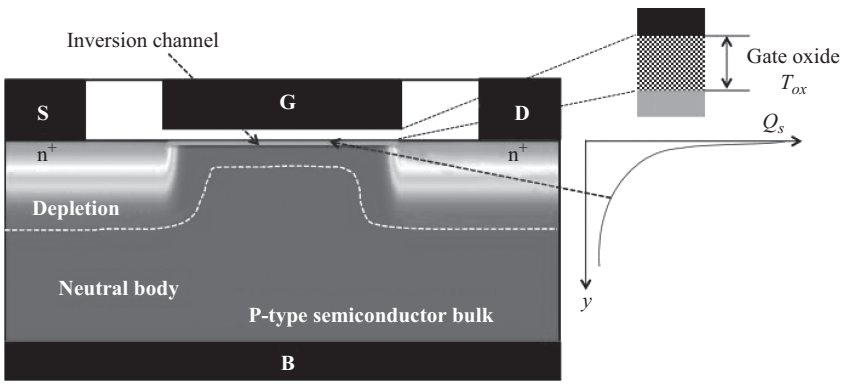

Figure 2.1 A conventional n-type MOSFET device

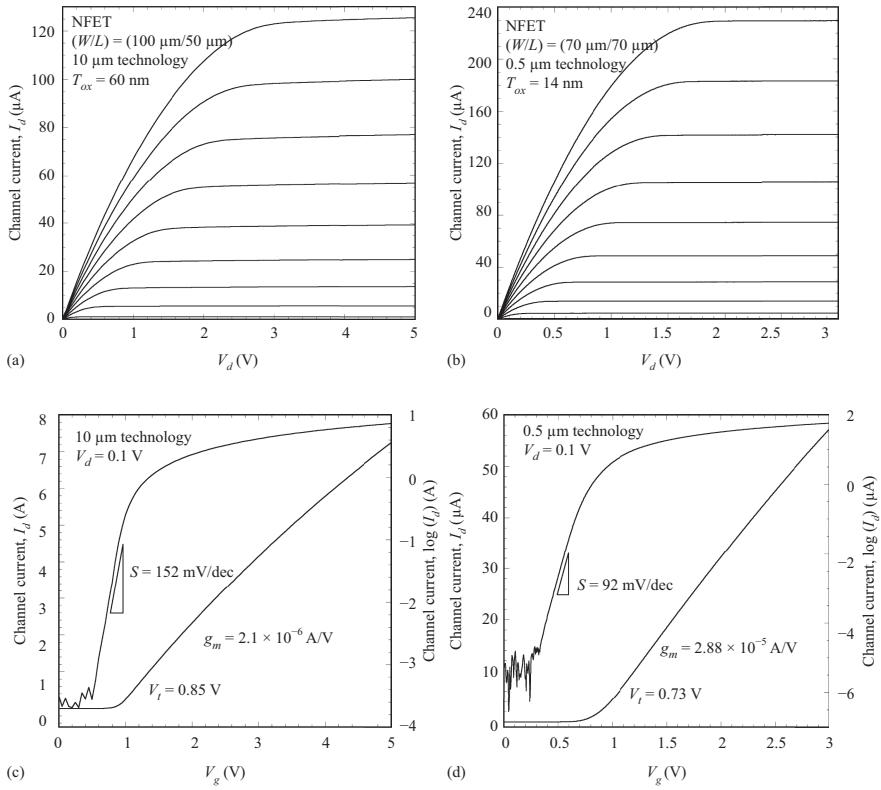

Figure 2.2 Electrical characteristics of two conventional MOSFET technologies of 10 μm and 0.5 μm. Plots (a) and (b) have V_g as a parameter from low to high values, while plots (c) and (d) correspond to I_d–V_g characteristics in both log and linear scales

transistor is from a commercial AMI technology [2.8]. From the I_d–V_d characteristics a desirable high output resistance is observed for the 0.5 μm technology. In both cases the saturation, or high output resistance region (a and b), is well defined. The subthreshold regime (c and d) in both cases is also well defined. The 0.5 μm transistor, because of the thinner gate oxide, has a larger current drive capability than that of the 10 μm technology. The subthreshold slope S, a speed-switching feature, is smaller for a 10 μm technology, while the threshold voltage V_t is smaller for the 0.5 μm technology with respect to that of 10 μm.

Smaller transistors with advanced technology features, such as thinner gate oxide, show better performance, faster switching, smaller threshold voltage V_t, higher current drive capability, and higher transconductance g_m ($\partial I_d/\partial V_g$), which result in lower bias voltage, faster circuits, and larger transistor density integration. The device physics and technology behind the enhanced electrical performance, as well as the limitations for a further down scaling, are described as follows.

At the semiconductor–oxide interface the energy bands bend as shown in Figure 2.3.

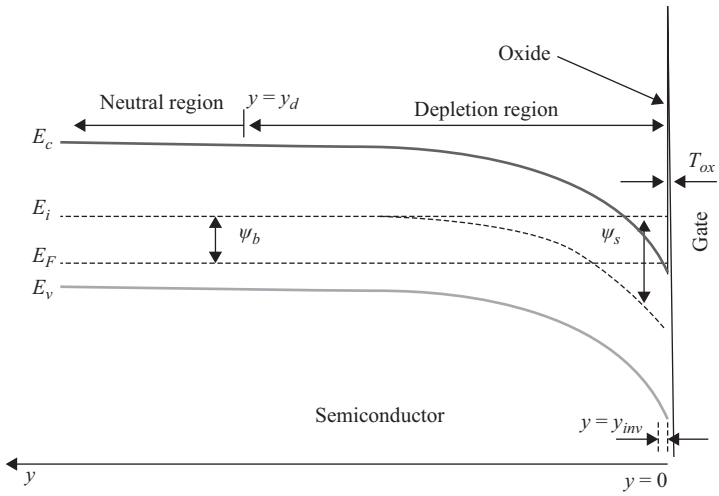

Figure 2.3 Energy band bending at the semiconductor–oxide interface for a p-type semiconductor case

Several features are observed, which are fundamental for the electrical performance of a MOSFET. Under the influence of a positive potential V_g applied to the gate terminal, the energy bands, E_c and E_v, bend down at the semiconductor-oxide interface. The energy band bending produces, in the semiconductor region, a region depleted of holes with an extension y_d, and very close the surface, within an extension y_{inv}, an inverted region populated with electrons. Such an inversion layer populated with electrons connects electrically the source with the drain terminal. The conductance of the MOSFET channel depends on both the gate (V_g) and the drain voltage (V_d) in such a way that it produces the electrical characteristics shown in Figure 2.2. A potential barrier at the semiconductor-oxide, and through the gate oxide thickness T_{ox}, develops as well. Such a potential barrier at the oxide prevents electrons from the inversion layer to flow to the gate. However, if the gate oxide T_{ox} is thinner than 10 nm, a considerable amount of electrons can tunnel through the gate oxide to the gate electrode. Another relevant feature is the thickness of the inversion layer y_{inv}, which is in the range within the 10 nm as shown in Figure 2.4.

Figure 2.4 shows the simulated current density for an n-type MOSFET with a gate oxide $T_{ox} = 14$ nm for a particular bias condition $V_g = 0.3$ V and $V_d = 0.1$ V. Most of the current that flows from source-to-drain is confined into a well potential of a thickness y_{inv} of about 5 nm. Such a thickness, which determines the channel conductivity, is bias and technology dependent. It is uniform along the channel if the drain-to-source potential is zero. The gate voltage dependence of y_{inv}, the inversion charge n, the surface potential ψ_s, and the channel current I_d are shown in Figure 2.5. The inversion channel gets thinner as the V_g voltage increases, while the inversion charge in the channel n increases exponentially, which compensates the thinning of the inversion channel. The surface potential ψ_s first increases linearly in the subthreshold regime, $0 < V_g < 1.0$ V, and then tends

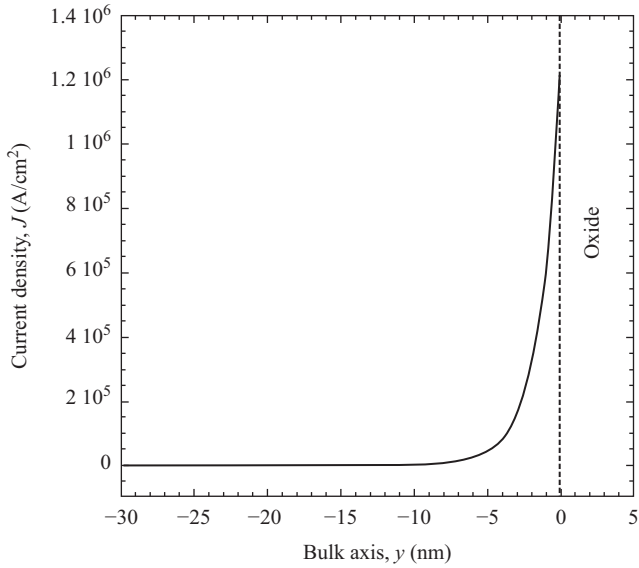

Figure 2.4 Current density J distribution from the semiconductor surface into the bulk axis y

to saturate at higher V_g voltages. The ψ_s potential is a measure of the energy band bending at the surface, and because both n and I_d are exponentially dependent on ψ_s, they follow the ψ_s–V_g shape.

It follows that the subthreshold slope S, as well as the transconductance g_m, is tightly related to ψ_s, and its derivative with respect to V_g.

The optimization of the electrical performance of a MOSFET, i.e., a high current drive capability, a small subthreshold slope S, a high transconductance g_m, and a low threshold voltage V_t, is intimately linked to the ability of the gate electrode to control the energy band bending at the semiconductor surface, and the capability of the channel to drive the charge from the source to the drain electrode. The impact of the gate oxide thickness T_{ox} on the subthreshold slope S, the transconductance g_m, the threshold voltage V_t, and the current drive capability I_d at the gate overdrive voltage $V_g + 1.0$ V is shown in Figure 2.6. The thinning of T_{ox} makes the MOSFET faster as the subthreshold slope S becomes smaller, which implies a faster digital off-on-off commutation. A larger transconductance g_m means the MOSFET is able to charge and discharge a capacitive load in a shorter time. For very thin gate oxides the reduction of the threshold voltage with T_{ox}, makes the MOSFET very leaky at low V_g voltages. The channel current I_d at the same gate overdrive voltage ($V_g = V_t + 1.0$ V), for the different gate oxide thicknesses, increases for thinner T_{ox}, which is good in terms of an enhanced current drive capability. It is not only the drastic reduction of the threshold voltage V_t, which degrades the electrical performance, but two other effects like tunneling through the gate oxide [2.9] and polysilicon depletion at the gate electrode [2.10].

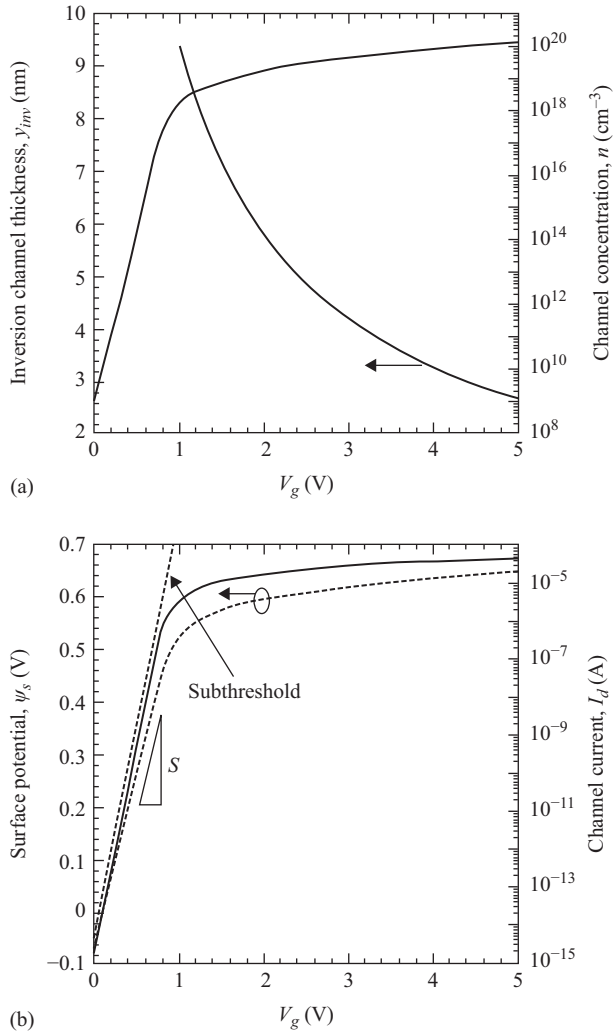

Figure 2.5 (a) Simulated inversion channel thickness y_{inv} and channel concentration n, and (b) surface potential ψ_s and channel current I_d as a function of the gate voltage V_g for $V_d = 0.1$ V. The simulation is for a $T_{ox} = 14$ nm

These two performance degradation mechanisms are shown in Figure 2.7. As the gate oxide thickness T_{ox} becomes thinner, the probability for carriers to tunnel through the oxide potential barrier increases and becomes evident for $T_{ox} < 10$ nm as shown in Figure 2.7b. For oxides thinner than 4 nm the direct tunneling (DT) [2.11] dominates, while for thicker oxides the tunneling is assisted by trap-assisted tunneling (TAT) [2.12]. For T_{ox} in the order of 2 nm the gate oxide leakage current can be in the range of 300 pA.

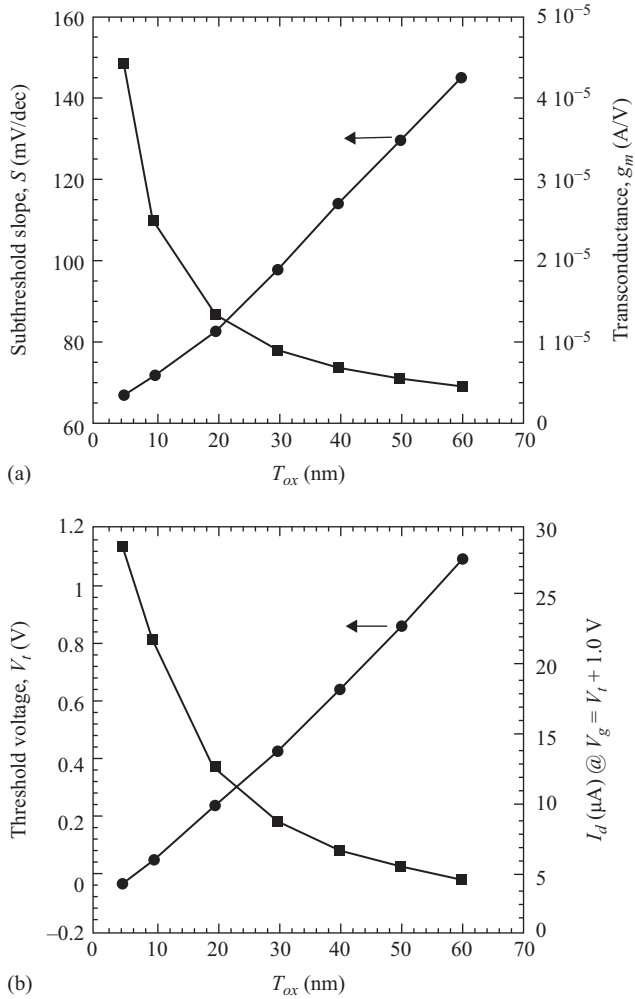

Figure 2.6 Simulated subthreshold slope S ((a) left axis), transconductance g_m ((a) right axis), threshold voltage V_t ((B) left axis), and current drive capability I_d at $V_g = V_t + 1.0$ V ((b) right axis), versus gate oxide thickness Tox

With the increase of the V_g voltage the lower part of the polysilicon gate at the interface with the oxide depletes. This mechanism is more pronounced for thinner gate oxides where the polysilicon gate is not uniformly doped, but has a lower doping profile at the gate–oxide interface. This makes the gate oxide effectively to increase from its nominal value T_{ox} to $T_{oxeff} = (T_{ox} + W_{pd})$, where W_{pd} is the thickness of the polysilicon depletion region. The straightforward effect is a reduction of current drive capability at high V_g values and a reduction of the transconductance as shown in Figure 2.7b. However, when the MOSFET drain voltage V_d increases, the distribution of the oxide electric field is not homogeneous anymore as shown in Figure 2.8.

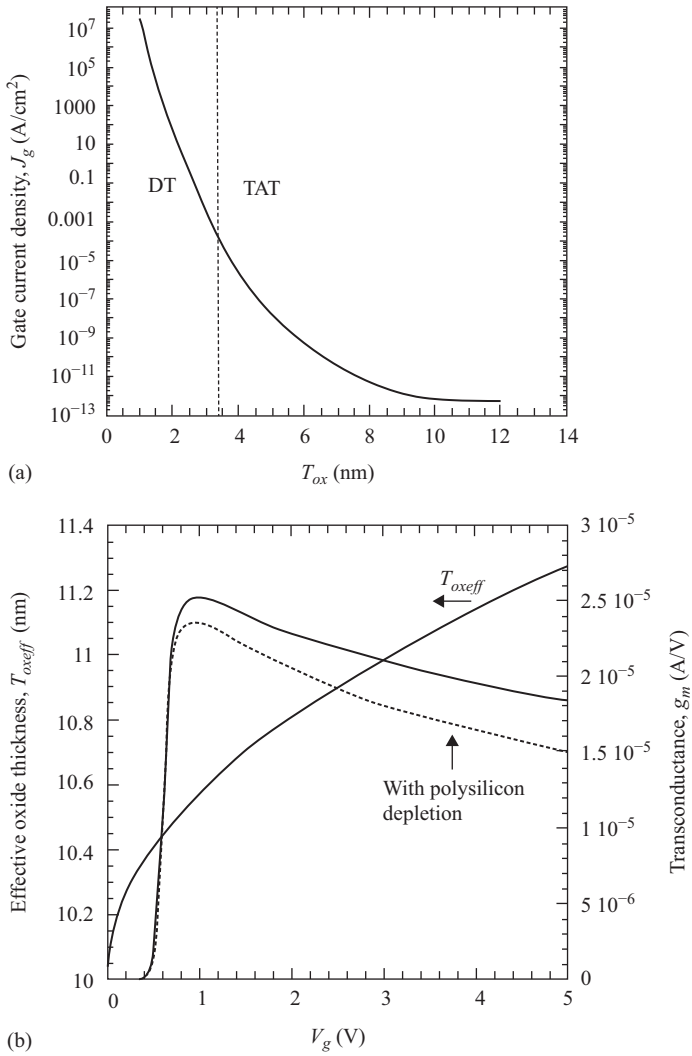

Figure 2.7 (a) Simulated gate current density J_g versus oxide thickness T_{ox}, and (b) effective oxide thickness T_{oxeff} and transconductance g_m versus V_g

The depletion of the polysilicon gate at the bottom side of the gate–oxide interface makes the oxide to virtually extend a little bit into the polysilicon material, which results in a thicker effective oxide $T_{oxeff} = (T_{ox} + W_{pd})$. The non-uniform polysilicon doping, in the *y*-axis, as shown at the upper right side, is responsible for the polysilicon depletion effect. However, when the drain voltage V_d increases, the distribution of the oxide electric field E_{ox} along the channel axis (*x*-axis) is not uniform anymore, and thus the polysilicon depletion effect becomes *x*-dependent through the bias condition as shown by the dotted line drawn through the oxide. The polysilicon

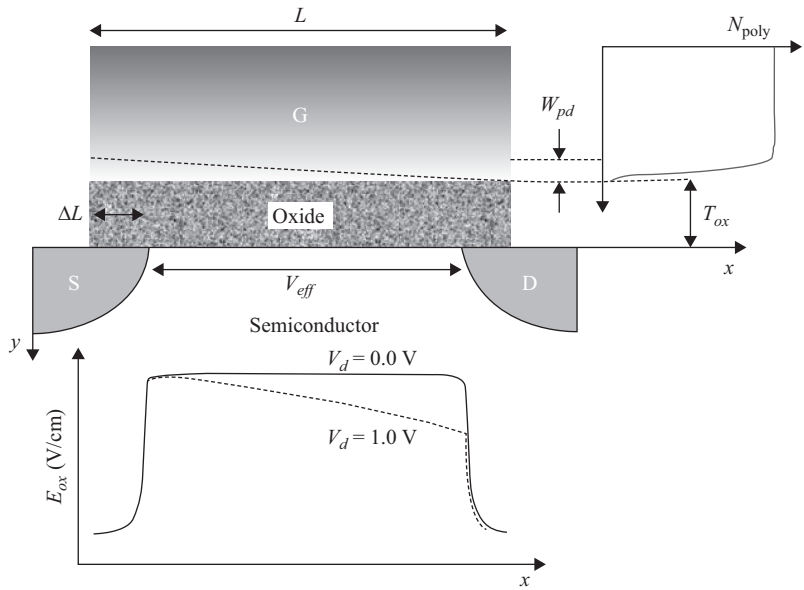

Figure 2.8 Schematic representation of the polysilicon depletion effect at the bottom side of the gate electrode (G), and simulation of the oxide electric field as a function of the x-axis for $V_d = 0.0$ V and 1.0 V

becomes less depleted at the drain than at the source side. The physics inside of the MOSFET becomes two-dimensional (2D). The 2D nature of the physics inside of the MOSFET becomes more evident when looking at the conduction band bending E_c and channel electric field $-E$ for two MOSFET with channel length L of 1.0 μm and 30 nm (see Figure 2.9). Three relevant differences are readily observed. The magnitude and the shape of the longitudinal or channel electric field $-E$, which for an $L =$ 30 nm MOSFET is wide and extends over almost all the channel length with a magnitude above 1×10^5 V/cm. For the $L = 1$ μm MOSFET the electric field $-E$ is narrow in shape with a magnitude above 1×10^5 V/cm extending only about 10 nm close to the drain side. The maximum electric field for an $L = 30$ nm peaks at 1.5×10^6 V/cm, while for $L = 1.0$ μm peaks at 2.5×10^5 V/cm. The conduction band edge E_c for $L = 1.0$ μm is linear in the channel, while that for $L = 30$ nm is never linear, which indicates a strong penetration of the longitudinal electric field lines into the channel. This implies that the charge in the inversion channel, for short channel devices, is not only controlled by the gate voltage (transversal electric field) but by the longitudinal electric field as well.

The second relevant feature for a short channel MOSFET is the generation of hot carriers [2.13]. A high electric field means the carriers, either electrons for an n-type or holes for a p-type MOSFET, acquire enough energy above the lattice temperature producing electron–hole pair ionization along the channel where they multiply by the avalanche mechanism. This is measured as an impact ionization bulk current I_b as shown in Figure 2.10a.

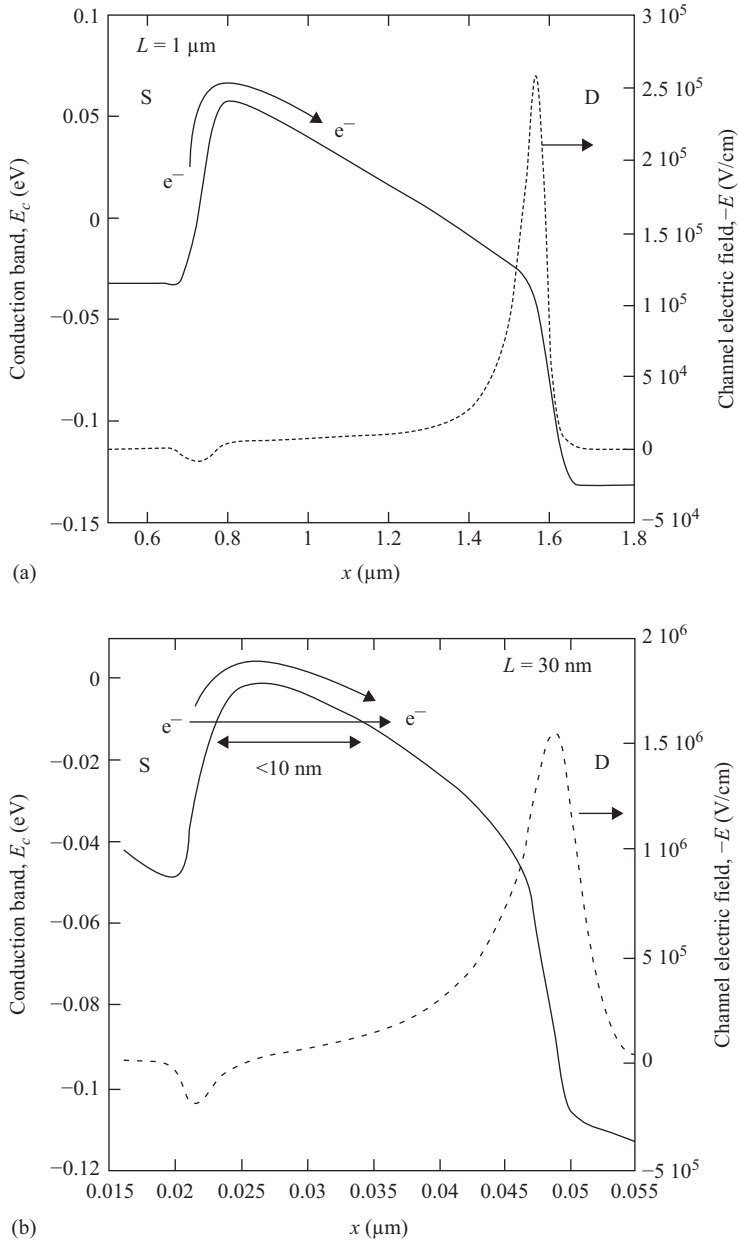

Figure 2.9 Simulated conduction band energy E_c and channel electric field versus channel axis x for two MOSFET of (a) L = 1 μm, and (b) L = 30 nm

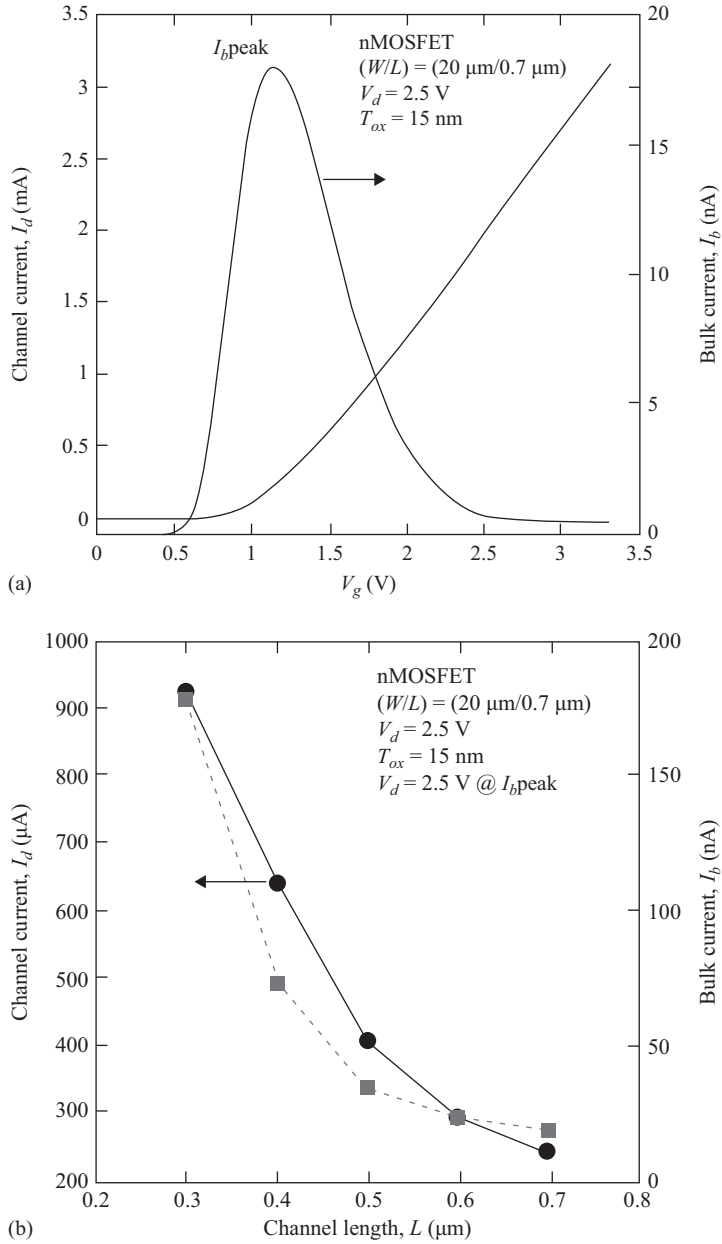

Figure 2.10 (a) Experimental I_d and bulk current I_b versus V_g, and (b) I_d and I_b versus channel length L

The experimental results shown in Figure 2.10 were taken from a 0.7 μm LDD technology with $T_{ox} = 15$ nm. As seen from Figure 2.10a the I_b current follows the classical bell-shaped curve, with a maximum value I_b peak [2.14]. The I_d follows the expected $(1/L)$ increase as L is reduced from 0.7 μm down to 0.3 μm. However, the I_b current, measured at its maximum value I_b peak, follows a rather more pronounced increase $(1/L^{3.5})$ when L is reduced down to 0.3 μm. This implies that impact ionization generated by hot carriers worsens at shorter device dimensions, which prompts for a device structure redesign to reduce impact ionization. An alternative structure to reduce impact ionization will be shown in the next section.

Together with hot carrier and impact ionization comes the third relevant feature, which is self-heating [2.15]. Self-heating is a deleterious effect of the electrical performance of MOSFETs. It reduces the carrier mobility in the channel by increasing the local temperature and the phonon population, and adversely impacts its reliability. The self-heating originates at the device region where carriers reach their maximum energy, close to the drain-bulk junction for a conventional bulk MOSFET. And because of the poor thermal conductivity of the gate oxide thickness, the heat flows into the bulk as shown in Figure 2.11.

The simulation shown in Figure 2.11 was performed with the gtsFramework tool [2.16]. The x–y profile of the differential temperature ΔT is shown in Figure 2.12. The differential temperature $\Delta T = (T_{Si} - T_{amb})$ is the difference of the internal device temperature T_{Si} and that of the ambient T_{amb}. The increase of the local temperature due to self-heating concentrates close to the drain/bulk junction and spreads out toward the source side and into the bulk. The gate oxide blocks the heat flow toward the gate electrode as shown in Figure 2.12b.

The differential temperature ΔT or the device temperature above the room temperature (300 K) follows an almost linear behavior with respect to the electrical power consumed by the device (see Figure 2.13a).

As shown by the simulated results in Figure 2.13b the rate of increase of the local temperature per mW of device power consumption ($d\Delta T/dP$) is proportionally larger for shorter devices. Combining the use of the gtsFramework simulation tool and data published in References 2.17 and 2.18, the thermal conductance G_{th} as a function of the channel length is shown in Figure 2.14a. It is seen that the ability of

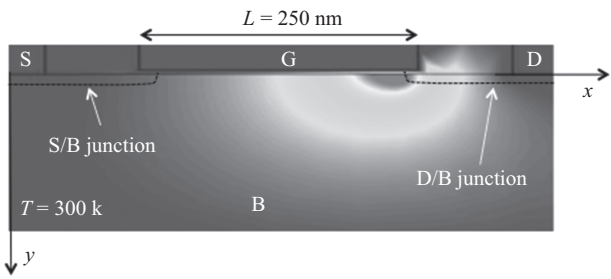

Figure 2.11 Simulated lattice temperature for a (W/L) = (10 μm/250 nm) nMOSFET biased at $V_g = 2.0$ V and $V_d = 5.0$ V

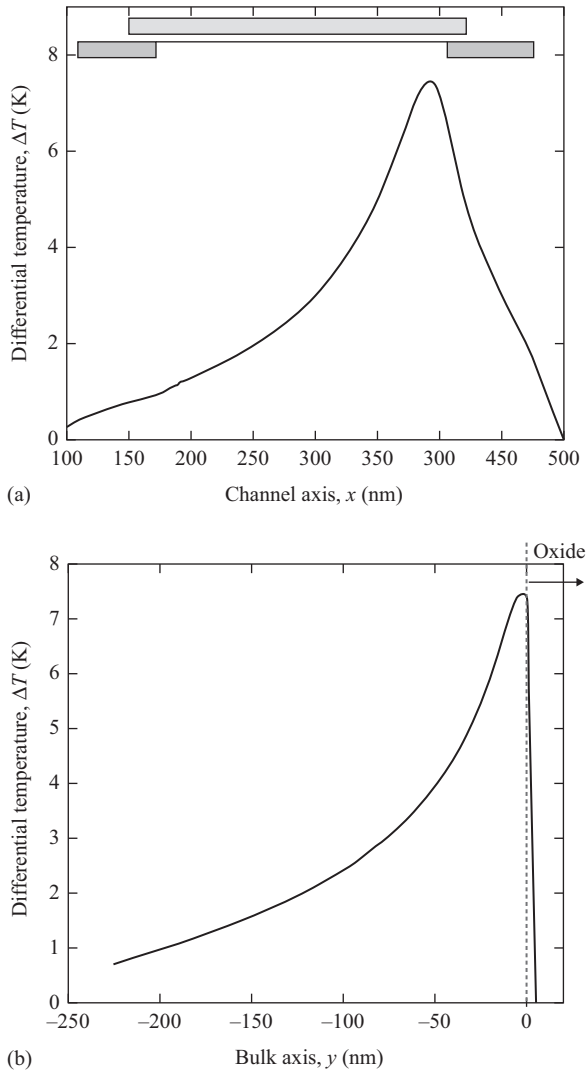

Figure 2.12 (a) Simulated differential temperature ΔT along the channel axis, and (b) differential temperature ΔT along the bulk axis

a MOSFET to conduct heat decreases as the channel length becomes shorter. For the gtsFramework simulation case a nMOSFET with a bulk thickness $T_b = 10$ μm has been assumed, while the simulation is performed for different channel lengths with a constant width $W = 1.0$ μm.

The self-heating effect worsens as the device length reduces from the micro- to the nanometer scale size. The thermal conductance G_{th} is also less dependent on temperature as the device dimensions shrinks down as shown in Figure 2.14b. The

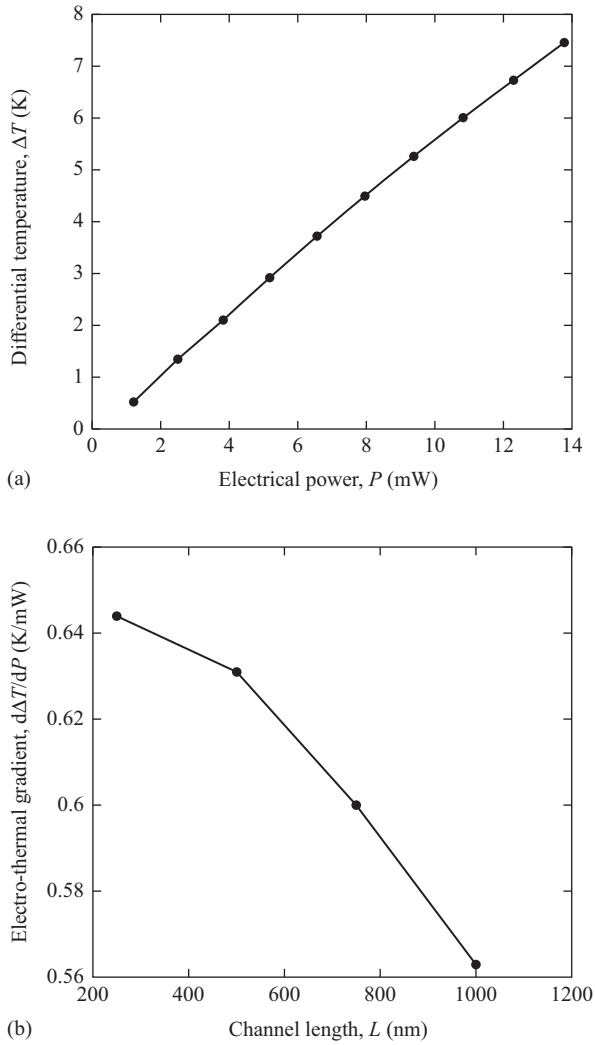

Figure 2.13 (a) Simulated ΔT temperature versus the device electrical power consumption, and (b) electro-thermal gradient dΔT/dP versus channel length L

modeling and prediction of self-heating in nano-scaled semiconductor devices becomes quite complex and requires solving the lattice heat flow equation.

$$\nabla \cdot (G_{th} \nabla T_L) = \rho C_{th} \cdot \frac{\partial T_L}{\partial T} - H \tag{2.1}$$

The coefficient ρ is the mass density, while C_{th} is the specific heat or the equivalent thermal capacity, and H is the heat generation. However, the model for

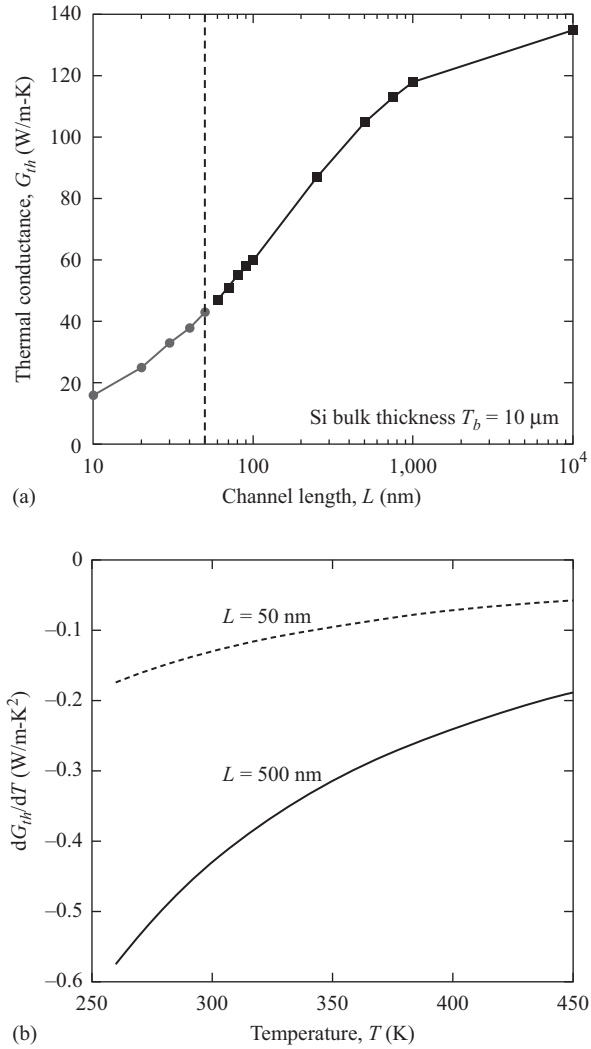

Figure 2.14 (a) Simulated thermal conductance G_{th} versus channel length L, and (b) simulated temperature gradient of G_{th} versus temperature for two different lengths L

the heat generation H depends on the charge transport model to be used, which can be Drift-Diffusion (DD), Hydrodynamic (HD), Monte-Carlo (MC), or Density Gradient (DG). The classical Drift-Diffusion (DD) and semiclassical approach considering HD transport are expected to fail at the sub 0.1-μm regime [2.19]. In order to cover quantum-mechanical effects, such as quantum confinement or charge tunneling, in a computationally economical approach, the DD model is modified through the DG approach, which recreates the inversion centroid charge

[2.20] and improves the calculation of tunneling through the gate oxide. For carriers under high electric field, they might reach carrier temperatures above the lattice temperature. In this case HD must be used for carrier transport simulation.

The conventional way of treating charge transport in large semiconductor devices, in the order of micrometers in size, has been through the combined solution of the Poisson equation, the continuity equation for electrons and holes, and the charge transport equations, which can be DD or any other approach as shown in the next set of equations.

$$\varepsilon\Delta\varphi = q(n - p - C) \tag{2.2}$$

$$qR = \nabla \cdot \vec{J}_n - q\frac{\partial n}{\partial t} \tag{2.3}$$

$$-qR = \nabla \cdot \vec{J}_p + q\frac{\partial p}{\partial t} \tag{2.4}$$

$$\vec{J}_n = q\mu_n n\left[\nabla\left(\frac{E_c}{q} - \varphi\right) + \frac{kT_L}{q}\cdot\frac{N_c}{n}\nabla\left(\frac{n}{N_c}\right)\right] \tag{2.5}$$

$$\vec{J}_p = -q\mu_p p\left[\nabla\left(\frac{E_v}{q} - \varphi\right) - \frac{kT_L}{q}\cdot\frac{N_v}{p}\nabla\left(\frac{p}{N_v}\right)\right] \tag{2.6}$$

The relation between charges and potential φ is captured with the Poisson equation (2.2), where n and p are the electron and hole charge concentrations in the semiconductor, respectively. C represents the concentration of fixed ionized charges. The mass conservation is captured with the continuity equations (2.3) and (2.4), where R represents the net generation of electron–hole pairs minus the net recombination rate of electron–hole pairs. Under thermal equilibrium R is neglected. $\vec{J}_n$ and $\vec{J}_p$ give the current density for electrons and holes, respectively. This couple of equations states that the semiconductor system will contain neither charge sources nor sinks. Under the presence of hot electrons, which causes either impact ionization or gate-oxide tunneling current, the mass conservation is violated, which requires the model to be modified.

Finally, when the charges, either electrons or holes n and p, are exposed to a gradient of the electric potential φ, or a gradient of the charges, which represents forces upon the charges, the charges will move or transport from an initial to a final position. This charge displacement or transport is conventionally represented by (2.5) and (2.6). In these two equations *drift* is represented by the first term, and *diffusion* by the second term between brackets. The gradient of the internal potential is referred to the conduction band edge E_c for electrons, and to the valence band edge E_v for holes. N_c and N_v refer to the effective density of states for electrons and holes, respectively. T_L refers to the lattice temperature, which may be different to that of the carriers $T_{n(p)}$. However, for the DD case $T_{n(p)} = T_L$. The carrier mobility for electrons and holes are represented by μ_n and μ_p. The force of an externally applied electric field $\boldsymbol{E}$ contributes to the charge drift. The charge flux originated by the externally applied electric field leads to an internal gradient of the

charge distribution, which contributes to the charge diffusion. In general, the DD approach states that a charge can move either by drift or diffusion. However, under the action of a high electric field carrier temperature T_n or T_p may differ from that of the lattice T_L. In this case the hydrodynamic model (HD) must be used to calculate the current density as shown by the next set of equations [2.21].

$$\vec{J}_n = q\mu_n n\left[\nabla\left(\frac{E_c}{q} - \varphi\right) + \frac{k}{q}\cdot\frac{N_c}{n}\nabla\left(\frac{n\cdot T_n}{N_c}\right)\right] \tag{2.7}$$

$$\vec{J}_p = q\mu_p p\left[\nabla\left(\frac{E_v}{q} - \varphi\right) + \frac{k}{q}\cdot\frac{N_v}{p}\nabla\left(\frac{p\cdot T_p}{N_v}\right)\right] \tag{2.8}$$

If average carrier energies are to be conserved, then the energy balance equations stay as follows [2.22].

$$\nabla\cdot\left(-G_{thn}\cdot\nabla T_n - \frac{5}{2}\cdot\frac{kT_n}{q}\cdot\vec{J}_n\right) = \nabla\left(\frac{E_c}{q} - \varphi\right)\cdot\vec{J}_n - \frac{3k}{2}\left[\frac{\partial(n\cdot T_n)}{\partial t} + R\cdot T_n + n\cdot\frac{T_n - T_L}{\tau_{rn}}\right] \tag{2.9}$$

$$\nabla\cdot\left(-G_{thp}\cdot\nabla T_p + \frac{5}{2}\cdot\frac{kT_p}{q}\cdot\vec{J}_p\right) = \nabla\left(\frac{E_v}{q} - \varphi\right)\cdot\vec{J}_p - \frac{3k}{2}\left[\frac{\partial(p\cdot T_p)}{\partial t} + R\cdot T_p + p\cdot\frac{T_p - T_L}{\tau_{rp}}\right] \tag{2.10}$$

Here, τ_{rn} and τ_{rp} refer to the energy relaxation times, while the term between brackets at the left side of the equation refers to the energy fluxes. G_{thn} and G_{thp} are the thermal conductivities for electrons and holes, which follow the Wiedemann-Franz law [2.23] that represents the ratio of the electronic contribution of the thermal conductivity to the electrical conductivity.

$$G_{thn} = \frac{5}{2}\cdot\frac{k^2}{q}\cdot T_n\cdot\mu_n\cdot n \tag{2.11}$$

$$G_{thp} = \frac{5}{2}\cdot\frac{k^2}{q}\cdot T_p\cdot\mu_p\cdot p \tag{2.12}$$

In the case of DD the heat generation H in the heat flow equation (2.1), becomes

$$H = \nabla\left(\frac{E_c}{q} - \varphi\right)\cdot\vec{J}_n + \nabla\left(\frac{E_v}{q} - \varphi\right)\cdot\vec{J}_p + R(E_c - E_v) \tag{2.13}$$

While for the HD case, the heat generation H stays as

$$H = \frac{3}{2}k \cdot \left(n\frac{T_n - T_L}{\tau_{rn}} + p\frac{T_p - T_L}{\tau_{rp}} \right) \tag{2.14}$$

As mentioned earlier DG is a computationally inexpensive an alternative way to incorporate quantum corrections without the need of self-consistently solving the coupled Schrodinger-Poisson equation system. The quantum corrections in the DG approach are introduced through the use of quantum correction potentials γ_n and γ_p for electrons and holes, which results in a modified transport equations as follows [2.24]:

$$\vec{J}_n = q\mu_n n\left[\nabla\left(\frac{E_c}{q} - \varphi - \gamma_n \right) + \frac{kT_L}{q} \cdot \frac{N_c}{n} \nabla\left(\frac{n}{N_c} \right) \right] \tag{2.15}$$

$$\vec{J}_p = q\mu_p p\left[\nabla\left(\frac{E_v}{q} - \varphi - \gamma_p \right) - \frac{kT_L}{q} \cdot \frac{N_v}{p} \nabla\left(\frac{p}{N_c} \right) \right] \tag{2.16}$$

The quantum correction potentials are given by [2.25]

$$\gamma_n = \frac{\hbar^2}{m_0 \lambda_n q} \frac{\nabla^2 \sqrt{n}}{\sqrt{n}} \tag{2.17}$$

$$\gamma_{np} = \frac{\hbar^2}{m_0 \lambda_p q} \frac{\nabla^2 \sqrt{p}}{\sqrt{p}} \tag{2.18}$$

where the $\lambda_{n,p}$ parameters can take values of 3 for the non-degenerate semiconductor case, or 9 for the degenerate case. In practice this is fitting parameter that can be adjusted to values between 3 and 9 depending on the doping level.

Overall, for devices at or below the 100 nm size-scale the incorporation of quantum effects is a must, and requires the combined solution of the Schrodinger and Poisson equations together with those of transport, and the adoption of the MC method for their multi-dimensional solution. A detailed discussion of advanced modeling and simulation techniques will be described in Section 2.1.3.

2.1.2 Alternative FET-related structures on silicon bulk and other materials

The conventional MOSFETs built with gate oxides thicker than 10 nm and polysilicon gates, show electrical performance limitations as shown in the previous section. Such a limitations are a large threshold voltage V_t, which inhibits the use of low-voltage supplies, a large subthreshold slope S, which makes transistor for high-speed digital electronics unsuitable. The small transconductance g_m is also another limitation for high-speed electronics. The polysilicon depletion and the series source/drain resistance are also two additional mechanisms, which negatively impact the electrical performance. A way to circumvent all these limitations is through the reduction of the channel length L and gate oxide thickness T_{ox}. However, as the channel length and the gate oxide are reduced, the energy of the carriers increases giving rise to hot carrier effects, such as impact ionization measured as a

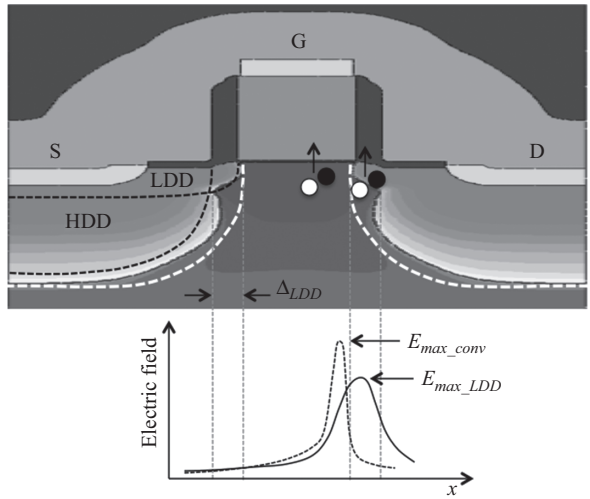

Figure 2.15 LDD MOSFET structure and electric field distribution for a single implanted conventional structure (dashed line), and for an LDD structure (continuous line)

bulk current, oxide tunneling measured as gate leakage current, channel self-heating measured as an increase of the local temperature, drain-induced barrier lowering (DIBL) [2.26] measured as a reduction of the threshold voltage, or increase of the channel leakage current.

The first approach to alleviate hot carrier effects has been the introduction of the lightly doped drain/source (LDD) MOSFET structure [2.27]. The LDD structure is shown in Figure 2.15. The structure is composed of a double implantation with a highly doped region (HDD) and a lightly doped section (LDD). A conventional single implanted S/D MOSFET structure is represented by the thick white dashed contour. The combination of the HDD and the LDD doping profiles results in a buffer region Δ_{LDD}, where the electric field reduces in magnitude and its maximum peak value E_{max_LDD} moves away from the active channel region. In the case of a single S/D implanted conventional structure, the electric field E_{max_conv} is larger than for the LDD and peaks in the active channel region. As the hot carrier generation is exponentially dependent on the electric field, a drastic reduction of hot carriers happens for the LDD structure. Moreover, as the electric field peaks, in the case of the LDD structure, outside the active channel region, thus the amount of hot carriers injected into the gate oxide diminishes, which minimizes degradation of the threshold voltage and improves gate oxide reliability.

The reduction of hot carrier generation by the use of a LDD structure is not for free, it comes with a bias-dependent series resistance effect [2.28]. Because of the light doping level at the Δ_{LDD} region, the charges at the gate-to-source/drain overlapping regions ΔL becomes modulated by the gate voltage, which results in a gate voltage-dependent series resistance as shown in Figure 2.16. The extracted gate

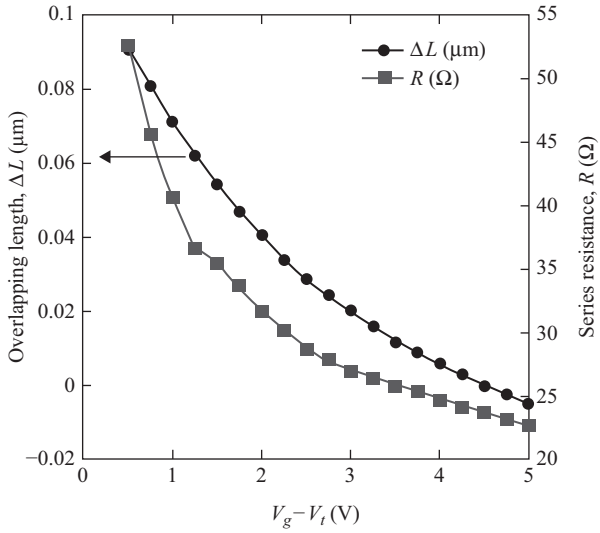

Figure 2.16 Measured overlapping length ΔL and series resistance R as a function of the gate voltage, for a 0.7 μm n-type MOSFET

overlapping length ΔL becomes also gate voltage dependent. At high gate voltages ΔL becomes even negative, which means the fringe gate electric field extends beyond the gate edge, controlling not only the charges under the gate-source/drain overlap but also the charges beyond the gate edge. Despite the LDD structure has been the workhorse for the MOSFET-based electronics for a long period of time since its inception in the late 1970s when used for a 5-mm MOSFET generation [2.29]. The reduction of the supply voltage and the contact resistance [2.30], has required a modification to its structure in order to be ready for a further miniaturization down to the 0.1 μm generation [2.31]. The 0.1 μm generation is a 1.5 V power supply technology with dual n^+/p^+ polysilicon gates on a 3.5 nm gate SiO_2 oxide.

This 0.1 μm technology still makes use of local oxidation (LOCOS) as an insulator between n- and p-type MOSFETs. The realized 50 nm shallow source/drain junctions in this 0.1 μm technology implies the consumption of silicon during the silicidation process, a problem avoided using the source-drain extension, a modification to the original LDD structure. A counter doping pocket implant (halo) is used to increase the doping level at the extensions, which further helps in suppressing short-channel effects. The halo doping allows for heavier channel doping, which in turn results in shallower source/drain junctions and thus in a reduced gate length. However, transistors with a high uniform doping level, from the surface through the bulk, this results in a degradation of carrier mobility due to combined action of Coulombic and phonon scattering. Thus the incorporation of super-steep retrograde channel doping profiles mitigates the carrier mobility degradation [2.32], and helps keeping a threshold voltage V_t with low variability from device to device. Gate oxides thinner than 10 nm brought the need to modify once again the

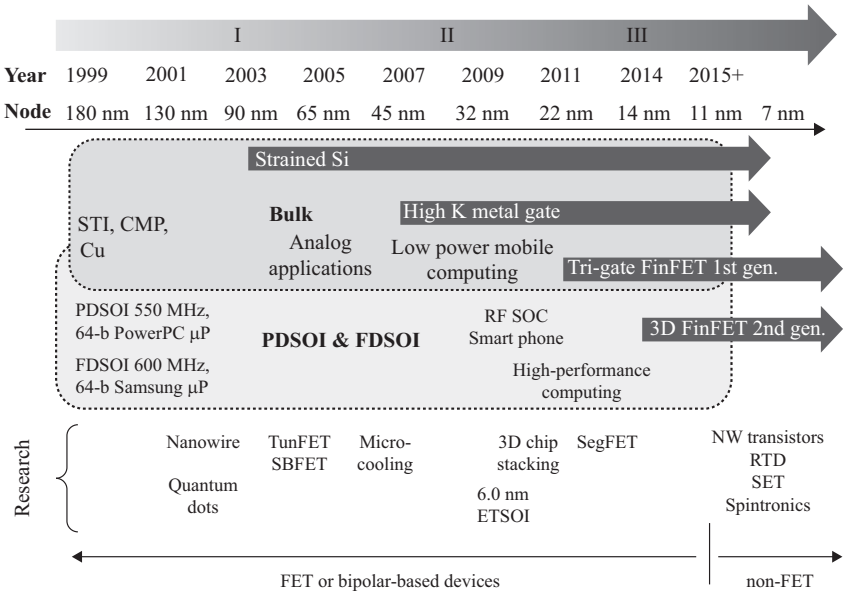

Figure 2.17 Technology evolution for Si- and FET-based devices. The two upper blocks Bulk and PDSOI and FDSOI shows the technologies already introduced for production. The lower part shows some of the alternative research approaches. The upper part shows the node definition and yearly progress

original LDD structure by making use of nitrided oxide films in place of pure SiO_2 [2.33]. The use of stacked nitride films prevents the boron penetration through the gate oxide into the channel, which in turn, alleviates the threshold voltage variation caused by the boron penetration into the channel.

In general the evolution of the FET-based IC technology can be split into three stages and three blocks as shown in Figure 2.17.

Stage I goes from the 180 nm to approximately the 65 nm technology node, where the LDD device structure incorporates many fabrication processes changes, such as mechanical strain to boost carrier mobility, retrograde channel doping, elevated source/drain regions [2.34] with shallow junctions and silicide contacts. Shallow trench isolation (STI) is introduced as a way to prevent current leakage between adjacent devices [2.35]. Chemical mechanical planarization (CMP) together with Cooper interconnects are introduced as a way to flat and smooth the inter-level dielectric layers in ICs [2.36]. In this first stage two popular microprocessor for computing application, the 550 MHz 64-b Power PC and the 600 MHz 64-b Samsung microprocessors, technologies are commercially introduced on Silicon-on-insulator (SOI) technologies [2.37, 2.38]. These microprocessors are based on partially depleted (PDSOI) or fully depleted (FDSOI) SOI technologies [2.39]. Alternative structures, such as nanowires (NWs) [2.40] and quantum dots [2.41], are researched and for the

first time envisioned as potential alternative for semiconductor device applications. Other alternative structures, such as the tunnel FET (TunFet) [2.42] and the Schottky Barrier FET (SBFet) [2.43], are also explored at the end of this first stage.

The second stage (Stage II) is dominated by the introduction of high-k gate oxide dielectrics and metal gates. Low Power Mobile computing has been proved to work in a 20 nm bulk planar CMOS technology. This technology features an advanced high-k metal gate process, strain engineering. A fully functional high density (0.081 μm^2 bit-cell) SRAM is reported at 0.9 V voltage supply [2.44]. Radio frequency (RF) System-On-Chip (SoC) for wireless and smart phone applications are also proven to work on either bulk- or SOI-FET-based technologies [2.45, 2.46]. These RF SoC applications have been developed on 32 and 28 nm technologies, which have resulted on 4G/LTE (long-term evolution) mobile SoC chips suitable for integration with multicore processors as well as analog and audio mixed-signal front ends [2.47]. With increasing levels of integration the need for 3D silicon chip stacking has increased. The 3D silicon chip stacking is required to meet the demand for high-density interconnection at medium and high frequencies [2.48]. This approach is explored in this second stage. As a result of the high-density integration high heat flux removal becomes a major consideration. An alternative to dissipate the heat flux out of an IC chip is the use of multiple drainage micro-trenches as proposed in Reference 2.49. Extremely Thin SOI (ETSOI) devices, with low GIDL and low V_t variability, are researched as candidates for low power applications. These ETSOI devices are built on 6 nm SOI layers [2.50].

Finally at the third stage comes the commercial introduction of both bulk and SOI FinFETs for high-performance computing, which marks an evident transition from the evolved planar MOSFET toward a 3D FinFET structure. In 2012 a 22 nm generation featuring a fully depleted (FD) tri-gate transistor is first introduced for SRAM and microprocessor applications [2.51]. Later in 2014 the second-generation 14 nm FinFET technology featuring with air-gapped interconnects is introduced for mass production of high-performance microprocessors and high-density SRAM [2.52]. Also in 2014 IBM introduced a 14 nm SOI FinFET technology with 0.0174 μm^2 embedded DRAM and 15 levels of Cu metallization [2.53]. An alternative to FinFET devices, called Segmented-Channel MOSFET (SegFET), is researched as an option to enhance electrostatic integrity and reduce short-channel effects using a still planar-silicon substrate [2.54]. This device structure has the advantage of a simplified planar MOSFET fabrication process with electrical performance as good as that of thin-body SOI devices.

In an exploratory stage there are various devices among them a vertically stacked gate-all-around silicon NW FET [2.55], which enables dynamic configuration of the device polarity to be n- or p-type. Si NW transistors with gate lengths in the range of 20 nm have been shown a high I_{on}/I_{off} ratio larger than 10^6. This NW transistor is fabricated with a simpler process without junctions [2.56], which results in improved short-channel characteristics compared to the inversion-mode devices. A more advanced option is the silicon single-electron quantum-dot transistor, based on the Coulomb blockade effect, which has been demonstrated to

work at room temperature for a silicon dot of about 12 nm of diameter [2.57]. Another option for the post-CMOS or post-FET era is the control of spin transport in Silicon [2.58]. Spin-based devices are non-volatile information by nature. So they are highly efficient in storing and processing information. They are also quite efficient in transferring information as well, which in addition to other outstanding features such as injection of spin-polarized currents into silicon makes them very attractive for a CMOS-spin circuit combination [2.59].

Another option for high-speed electronics is the Resonant Tunneling Diode (RTD) device [2.60]. Maximum frequencies of up to 2.2 THz have been demonstrated with RTDs, which outperform that of Si-based FET devices [2.61]. The RTDs may found application in different areas, such as high-resolution imaging systems or wide-band secure communication systems.

Other than Silicon materials such as graphene, have been also researched as a material with excellent electrical transport properties. Graphene can be grown as a dimensional mono-atomic layer with excellent semimetal properties, such as concentrations as high as 10^{13} cm^2 with room-temperature mobilities of around 1×10^4 cm^2/Vs [2.62].

The advanced semiconductor devices, such as FinFETs, SOIs, TunFets, NWs, quantum dots, and spin-based devices, will be treated in detail in the subsequent sections.

2.2 Advanced FET-related devices

2.2.1 Introduction

Power-Performance-Area-Cost (PPAC) trade-off relationship is the "*leitmotif*" that moves today's semiconductor industry. Since early 1960s, the reduction of MOSFET dimensions with some punctual modifications to control short channel effects (SCEs) has been enough to fulfill the above balance equation while following Moore's Law (the number of devices in an IC will double every 18 months) [2.63]. Meanwhile, the power consumption has been kept under control, at the same time that the drain current and therefore the performance were largely increased. Finally, the cost-per-device of each node was smaller than that in the just previous one, or equivalently, the number of transistors that can be bought per dollar was monotonically increasing node after node (Figure 2.18).

The major factors that control the drain current and therefore the performance of a MOSFET transistor are the channel length, the carrier mobility, and gate capacitance. Although the reduction of channel length would theoretically increase the drain current and reduce the switching times of the device making it faster, when this length approaches nanometric dimensions, the arising of physical and essential limitations makes this picture much more complicated. These limitations are related to SCEs, degradation of carrier transport, and increase of leakage current and/or power consumption. SCEs (i.e., charge sharing between source/drain depletion regions and the channel) [2.64] mean the lack of electrostatic control of

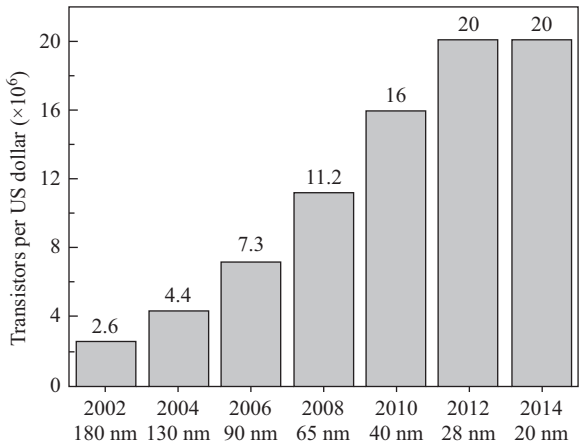

Figure 2.18 Transistors that can be bought per dollar at each technological node
© 2014 Semiconductor Engineering. Adapted with permission from Brian Bailey http://semiemgineering.com/the-tail-of-moores-law-nolonger-wagging-the-dog/

the channel by the gate, and the degradation of the proper switching capabilities of the transistor. To avoid SCEs, substrate doping level has to be increased. However, there is a limit to how much the doping level can be increased before junction breakdown becomes a problem. In addition, the increase in the substrate doping produces an increase in the transversal electric field and a degradation of the carrier mobility [2.65, 2.66], and also degradation in the gate-to-channel capacitance, both facts producing a reduction of the on-current.

Keeping the gate-to-channel capacitance, while downsizing the gate length, requires an equal factor of decrease in the gate oxide thickness. In the 65 nm technology node with gate length of 32 nm, the thickness of the silicon oxide should be about 0.9 nm, which is very close to the theoretical limit (around 0.7nm) for bulk silicon dioxide [2.67]. Further device downsizing is only possible by introducing high-dielectric constant (high-k) materials [2.68, 2.69]. By using gate insulators with higher permittivity a larger value of the gate capacitance can be achieved with a thicker film, thus not only resolving the physical constraint of the oxide thickness for further downsizing but also helping to suppress the leakage tunnel current through the gate.

Degradation of mobility because of high doping substrates can be compensated by mobility or transport boosters [2.70]. The most straightforward way to improve the carrier transport in MOSFETs is to induce uniaxial or biaxial tensile strain in NMOSFETs and uniaxial compressive strain in PMOSFET channels [2.71]. Tensile strain produces an energy band splitting of the silicon conduction band, and a repopulation of the carriers, which originates a decrease of the transport effective mass and a reduction of the phonon scattering. Biaxial strain can be induced by substrate engineering, i.e., from epitaxial growth of tensile silicon on relaxed SiGe layers, and uniaxial tensile or compressive strain can be obtained from Contact

Table 2.1 Mobility boosters for CMOS VLSI technology

	Electrons	**Holes**
Channel direction	<100>	<100> on (100) <110> on (110)
Surface orientation	(100)	(110)
Strain	biaxial tensile	biaxial tensile uniaxial compressive
Materials	(III–V)	SiGe/Ge

Etch Stop Layer (CESL) approach. Another efficient way to improve the carrier mobility is to choose the appropriate crystalline orientation and the transport direction (Table 2.1). Finally, other materials presenting higher electron and/or hole mobilities, such as III-Vs, SiGe, or Ge, can be used to improve the transport in the channel.

For very short channel devices, the resistance of the source/drain and the extension regions can be comparable to that of the channel, thus becoming in a showstopper limiting the performance enhancement obtained by the channel length reduction. The source/drain engineering is therefore another technology booster that implies the optimal design of source impurity profiles and Schottky metal source structures.

But, performance is only one term in the equation. Power dissipation is also an important ingredient. The power dissipation of a MOSFET is due to static and dynamic contributions. Static power consumption is the product of the supply voltage times the off-state current. Therefore, the reduction of static power consumption requires an excellent control of the off-state current (including leakage currents), and a low value of the threshold voltage, which would allow the scaling down of supply voltage. However, a minimum value of the threshold voltage is required due to subthreshold swing degradation, short channel threshold voltage roll-off, and DIBL [2.72]. Another important effect of scaling is related to the increased current that flows through the device in its off state. In addition to the subthreshold current, several parasitic currents can contribute to the static power consumption: (i) first, for nanometer size gate dielectrics, the probability for carriers to tunnel between the gate and the channel is non-negligible [2.73]. An efficient way to reduce the gate leakage is to increase the physical dielectric thickness, while keeping a sufficient potential barrier height between the channel and the dielectric. In order to keep at the same time a large capacitive coupling between the gate and the channel high-k materials have to be used, as mentioned earlier. Another source of current leakage is the junction leakage current between source/drain to body current of the PN junction. In addition to this reverse PN junction current, a drain to body leakage can be induced when a high gate to drain voltage is applied, as a consequence of the band-to-band tunneling (BTBT) of electrons between the conduction band in the drain region and the valence band in the accumulated region below the gate oxide. Finally, for channel lengths below 10 nm, a significant amount of carriers can tunnel directly from source-to-drain through the barrier potential [2.74].

With regard to dynamic power consumption, it can be kept under control by reducing parasitic capacitances as much as possible [2.75].

In summary, so far PPAC trade-off condition has been achieved by geometrically scaling the gate length of the transistors to nanometric dimensions, without involving any major change in the bulk MOSFET structure except a complexity increase in the fabrication process using technology boosters which can be classified into three categories: (i) gate-stack engineering with the use of high-k insulators and metal gate electrodes; (ii) source-drain engineering which includes Schottky barrier source structures and optimal design of source impurity profiles; and (iii) channel engineering, which includes the use of strain (global or local) and the use of alternative high-mobility channel materials.

Thus channel lengths in the 30 nm range have been achieved using classical bulk-Si MOSFETs [2.76]. However, a scaling limit for this classical CMOS bulk structures beyond $L_g = 30$ nm is now evident. The complex doping profiles required to control SCEs, and the variability issues arising by the randomness of the dopant atoms, stop bulk-Si MOSFETs from being scaled with reliable results further than 30 nm.

The increasing variability in the device characteristics is among the major challenges to scaling and integration for the present and next generation of nano-CMOS transistors and circuits [2.77]. The statistical variability of transistor characteristics, which has been previously concern only in the analog design domain, has become a major concern associated with CMOS transistors scaling and integration [2.78, 2.79]. It already critically affects SRAM scaling [2.80] and introduces leakage and timing issues in digital logic circuits [2.81]. The statistical variability in modern CMOS transistors is introduced by the inevitable discreteness of charge and matter, the atomic scale non-uniformity of the interfaces and the granularity of the materials used in the fabrication of ICs. The granularity introduces significant variability when the characteristic size of the grains and irregularities become comparable to the transistor dimensions. For conventional bulk MOSFETs Random discrete dopants (RDD) is the main source of statistical variability [2.82]. Random dopants are introduced predominantly by ion implantation and redistributed during high temperature annealing. Apart from special correlation in the dopant distribution imposed by the silicon crystal lattice, there may be also correlations introduced by the Coulomb interactions during the diffusion process. For a complete study of variability consider the work of Prof Asenov's group [2.77, 2.83, 2.84].

No additional performance "boosters," such as strained-Si channels and metal gate stacks [2.76, 2.85], will enable a reliable classical technology beyond channel lengths shorter than 30 nm. As the channel area underneath the gate is getting very short, the gate is no longer powerful enough to control it properly. It could control the top part of the channel but the further from the gate the less the control. In particular, when the gate is off there are paths between source and drain that remain on and so there is very high leakage. It is clear that new transistor architectures are required.

The basic constraint is that the entire channel needs to be close to the gate so that it can be controlled properly. Therefore, if a thin channel is put on top of an insulator, and the gate is built on top of that then there is once again good control and low leakage (Figure 2.19). There are simply no paths through the channel that

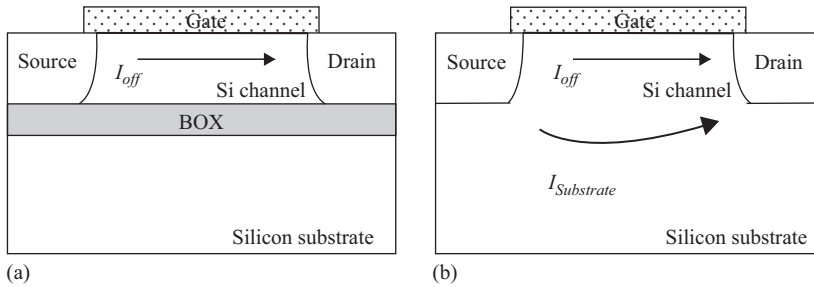

Figure 2.19 Schematic of (a) a SOI MOSFET transistor and (b) a bulk MOSFET showing different components of the off-current

are far from the gate and so poorly controlled because the insulator isolates the source and drain from the substrate. These devices are called SOI transistors. That is thick-box SOI (box just stands for buried oxide, the insulator underneath the channel). If, however, the box is very thin then the substrate itself becomes a sort of second back gate and can further be used to control the channel, not to turn it on and off but to affect its performance.

Another alternative to do this is to make the channel into a thin vertical fin and wrap the gate around it. This structure is known as FinFET. Since the fin is thin, it is never far from the gate and control is good and leakage is low. The following parts of this chapter are devoted to review these interesting devices.

2.2.2 Silicon-on-insulator FET technology

Typical silicon wafers have a total thickness of less than 1 mm (usually 775 μm for 300 mm wafers [2.86]). Only a tiny slice of several micrometers at the top is used for fabricating nanoelectronic devices, Figure 2.20. The unused bottom region of monocrystalline silicon is necessary to ensure the structural feasibility of the wafer and the devices, providing strength and avoiding breaks [2.87].

But using a semiconductor substrate also contributes to some undesirable parasitic effects such as:

- Implicit electrical connection between different devices. It is usually solved using lateral isolation techniques like STI, or channel stop implantations. These techniques consume area and require more fabrication steps.
- Appearance of parasitic capacitances and devices. An NPN parasite BJT can appear using the N^+ diffusion of the source or drain of a N-MOSFET as emitter, the P-type well acts as the base and the N-type well as collector. A PNP BJT can also appear the same way next to a P-MOSFET.
- Lower control over SCEs. The gate looses the electrostatic control over the channel due to source and drain region influence. This limits the minimum channel length of the device that can be fabricated. To overcome this problem, high body doping to reduce the depletion regions has been used. However, this increase in the body doping has a negative effect on mobility, threshold voltage, transconductance, and device variability.

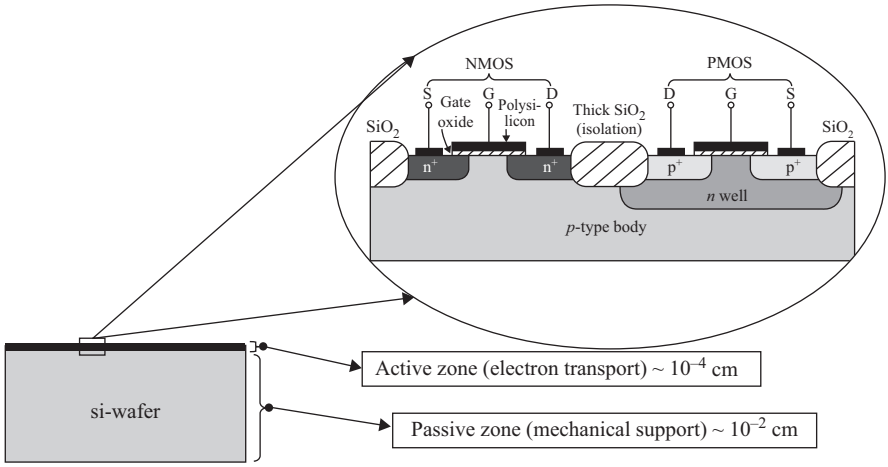

Figure 2.20 Details of the useful layer thickness on a bulk Silicon wafer. Only the top region is used for fabricating devices, while the thick bottom region remains unused providing mechanical strength and avoiding breaks

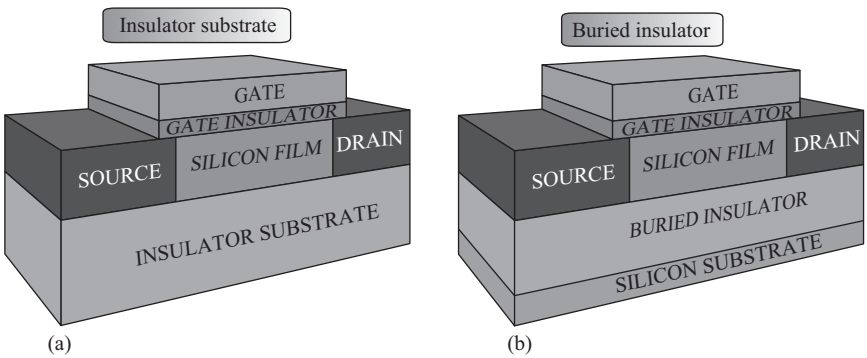

Figure 2.21 Different SOI wafer configuration depending on the buried oxide thickness. (a) In the panel A, a thin Si-film layer is grown or deposited on top of an insulator substrate. (b) In the panel B, only a buried thin layer of insulator separates the active area to the silicon substrate

In order to solve these problems, the SOI technology proposes the use of a new film made of dielectric. This insulator layer isolates the active region where devices will be fabricated from the silicon substrate. There are two different alternatives: using a thin insulator layer buried in the silicon wafer or using a wafer made of an insulator material and growing a thin layer of silicon on its top. Both types of approaches are depicted in Figure 2.21.

The most common option is to use the buried layer called BOX (Buried OXide). This enables substrate biasing when the insulator layer is not very thick, less than 200 nm. Nevertheless, to achieve a useful SOI wafer is very challenging.

A thin monocrystalline layer of silicon needs to be grown on top of the insulator. The Si-film must feature the same quality and properties as those grown in volume:

- low density of interface states
- uniform thin layers
- good performance of the dielectric

Figure 2.22 summarizes the main techniques for fabrication of SOI wafers.

Among all of them, the most important and used today is the Unibond technique or *Smart-Cut*. This is one of the most effective processes to produce commercial SOI wafers. The Smart-Cut technique combines an ion implantation and wafer bonding to transfer a thin slice of one wafer to another wafer or insulator substrate. It was first developed in 1992 at CEA-LETI [2.88]. The main steps are illustrated in Figure 2.23 and summarized below:

1. Initially, two bulk silicon wafers, "A" and "B," are used. The surface of one of them should be completely oxidized, for example, wafer "A." This wafer will be used for the active layer on top of the BOX. The next step consists on implanting positively charged hydrogen ions (protons) on the wafer "A." The implantation's energy will define the silicon film thickness.
2. After this, the wafer is cleaned and then bonded onto wafer "B" using the SiO_2 previously grown to maintain them together.
3. Then, a first heat treatment is performed at around 400–600 ºC. With this, the micro-cavities produced by the implantation of protons split up the wafer into two pieces, one of them a bulk wafer, "A," and the other an SOI wafer, "B." After this, a second heat treatment to improve the connection between the BOX layer and the wafer itself is carried out.

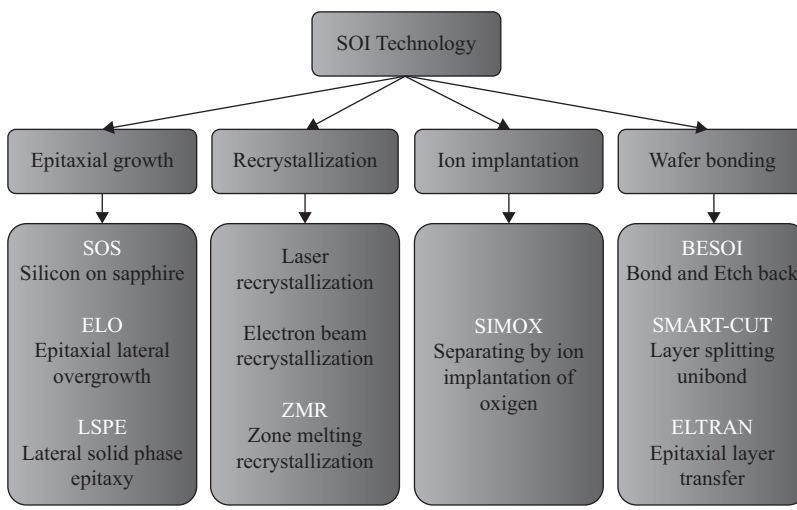

Figure 2.22 Main techniques for SOI wafers fabrication

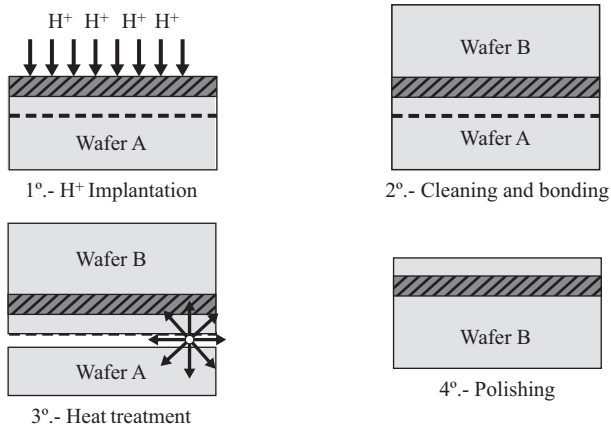

Figure 2.23 Smart-Cut SOI wafer fabrication technique based on wafer bonding

4. Finally a chemical mechanical polishing (CMP) process is performed to achieve a uniform wafer surface and also to thin the Si-film to the desired final thickness.

The advantages that SOI technology provides compared to bulk are numerous. Some of the improvements are [2.89]

- Avoid the connection between device and substrate:
  - area consumption reduction
  - avoid the latch-up
  - lower power consumption
  - better subthreshold swing
  - lower leakage currents
  - better transconductance
  - improve the control of SCEs
  - lower power voltage
  - better immunity to ionizing radiation
- No need of body doping: lower Random Dopant Fluctuation (RDFs), decreasing variability on threshold voltage, and other parameters.
- Capability of integrating different devices on the same wafer such as, CMOS, power devices, bulk designs, and optoelectronics.
- Possibility to stack more than one layer of devices (the drawbacks are the interconnection issues that appear and also self-heating-related problems [2.89]).

The main disadvantage of SOI technology seems to be the higher price of the wafers due to the extra fabrication steps needed. However, it is worth noting that the final cost of an IC in SOI technology may be lower due to a simpler fabrication process with less manufacturing steps. Together with the extra price, there is another

important drawback of SOI. The self-heating effect (SHE) is more remarkable in SOI wafers since the SiO_2 is about two orders of magnitude less thermal conductive than silicon. Thin-film SOI MOSFETs are therefore prone to accumulate heat because it cannot be dissipated rapidly through the BOX. However, recent studies show that the SHE is present but it does not represent a limiting factor for the reliability in ultra-thin silicon films transistors, especially for fast switch operations [2.90]. Other constraints that SOI wafers may include are [2.91–2.93]:

(i) The uniformity of the BOX and silicon layers is crucial to avoid high variability.
(ii) Floating-body effects (FBE) [2.94–2.96]. Although this is not always a drawback, it may lead to an abnormal behavior.
(iii) Inter-gate coupling effects between front and back-channels. As the FBE, it may be also an advantage.
(iv) Large series resistance in thin film devices. This is normally reduced by raising the source and drain regions, RSD (raised source drain also known as ESD, elevated source drain) technique [2.97, 2.98].

2.2.2.1 Partially depleted SOI MOSFETs

SOl CMOS involves building more or less conventional MOSFETs on a thin layer of crystalline silicon, as illustrated in Figure 2.24. The thin layer of silicon is separated from the substrate by a thick layer (typically 100 nm or more) of buried SiO_2 film, thus electrically isolating the devices from the underlying silicon substrate and from each other. SOl CMOS process can be readily developed due to the compatibility with established bulk processing technology.

SOl MOSFETs are often distinguished as partially depleted (PD) and fully depleted (FD) [2.99, 2.100].

In case of PD transistors, the silicon film under the gate is not completely depleted of mobile charges. In contrast, for FD MOSFETs no charge accumulation or storage can be achieved without biasing the gates: there is no quasi-neutral region, which serves as a potential well to store majority carriers. In general, the thickness of the silicon film that determines whether it is PD or FD depends mainly

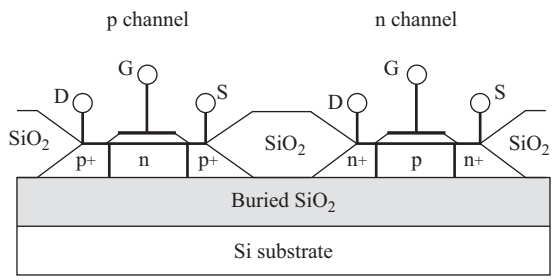

Figure 2.24 Schematics of p-channel and n-channel transistors in SOI CMOS technology

on the body doping concentration, $N_{A,D}$. The following equation indicates the depletion depth for one interface with no lateral influence (1D model):

$$x_D = \sqrt{\frac{2\epsilon_0\epsilon_{Si}\Phi_s}{qN_{A,D}}} \tag{2.19}$$

where ε_0 and ε_{Si} are the permittivity of vacuum-free space and silicon relative permittivity, respectively, q is the electron charge, and Φ_S is the surface potential at the interface. The maximum depletion width, $X_{D,max}$, corresponds to $\Phi_S = 2\Phi_F$, where Φ_F is the Fermi potential, equal to $\frac{kT}{q} ln(\frac{N_{A,D}}{n_i})$.

Typically, commercial silicon film thicknesses, t_{Si}, larger than 70 nm correspond to PD, and below 40 nm to FD [2.101]. The main differences between both types of transistors are resumed in Table 2.2 and Figure 2.25 [2.102–2.105].

In a PDSOI device there is no interaction between the front and the back depletion zones because $t_{Si} > X_{D,max}$. Therefore, the threshold voltage in a PDSOI transistor is the same as in a bulk MOSFET:

$$V_{TH} = V_{FB} + 2\Phi_F + \frac{qN_A x_{D,max}}{C_{ox}} \tag{2.20}$$

where $V_{FB} = \Phi_{MS} - \frac{Q_{ox}}{C_{ox}}$ is the flatband voltage.

As previously mentioned, in a PDSOI device, the body is thick enough such that only part of the body region is depleted across the bias range of operation. This means that part of the silicon film remains neutral, populated with mobile majority carriers and surrounded by the buried oxide at the bottom, and laterally by source/body and drain/body PN junctions. Therefore, this neutral area remains isolated from any contact, as observed in Figure 2.26, i.e., the body of the transistor remains floating and its potential is determined by capacitive coupling through the gate oxide, C_g, the sidewall source and drain junctions, C_s and C_d, the BOX interface C_b, and the leakage current through the junctions and the oxides. In Si-bulk devices, if majority carriers are created during the operation of the transistor, they can be evacuated through the substrate since this is directly connected to the substrate

Table 2.2 Partially depleted, fully depleted SOI, and bulk transistors comparison

Parameter	Partially depleted	Fully depleted	Bulk
Silicon thickness	>70 nm (typ.)	<40 nm (typ.)	—
Source/drain resistance	Moderate	High	Low
I_{on}	Moderate	High	High
I_{off}	Very low	Low	Moderate
DIBL	Low	Very low	Moderate
Subthreshold swing	Moderate	Very low	High
Floating-body effects	✓	✖	✖
Kink effect	✓	✖	✖
History effect	✓	✖	✖
Coupling channel	✖	✓	✖

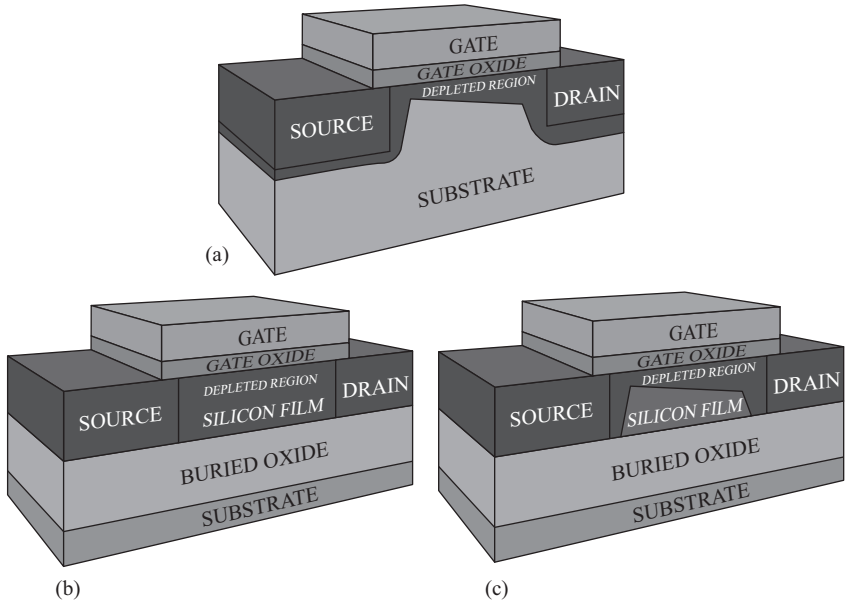

Figure 2.25 Depleted region comparison between (a) bulk MOSFET, (b) fully depleted SOI transistor, and (c) partially depleted SOI transistor. The depletion region induced by the back-gate is not represented

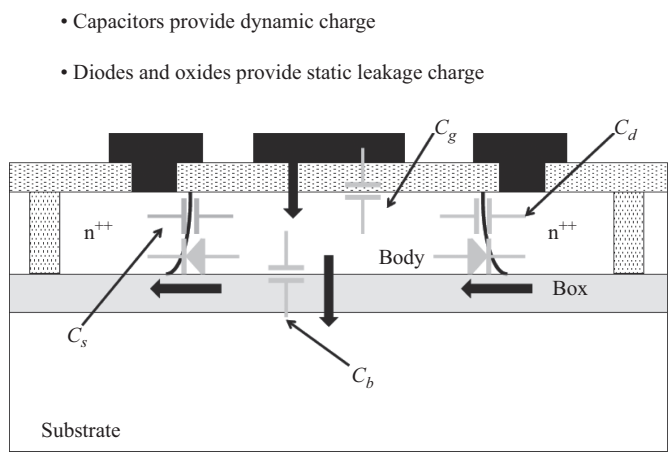

Figure 2.26 Schematic cross-section of a partially depleted SOI transistor showing the capacitive coupling of the neutral body of the transistor through the gate oxide, C_g, the sidewall source and drain junctions, C_s and C_d, the BOX interface C_b, and the leakages current through the junctions and the oxides

contact. On the contrary, in the case of a PDSOI transistor, the excess of majority carriers accumulates in the body of the device, changing its potential, which therefore is not fixed but depends on the history of the device. This fact is the origin of a set of effects named FBE [2.89]. All these effects have their origin in the charging-discharging of the floating-body by currents coming from the source or the drain and in the capacitive coupling between the gate and the floating-body.

Although these effects may be detrimental, it also allows the MOSFET to exhibit very interesting properties such as memory capabilities, the so-called floating-body memory [2.106–2.108]. Some of the most important aspects of FBEs are summarized below [2.89, 2.109]:

1. **History effect and threshold voltage variability**
   The most prominent electrical property of the PDSOI device is the history effect. The *I–V* characteristics (and the threshold voltage) of the transistor are no longer constant, but dependent on the amount of charge contained in the body of the device at any given time. The charge content of the body and the distribution of that charge caused by gate, source, and drain potentials determine the final behavior of the device. The magnitude of charge contained in the body depends on several factors that include:

   - the previous state of the transistor
   - the device architecture (length, width, Si-film thickness, etc.)
   - the applied biases
   - the frequency of operation
   - the temperature

   Figure 2.27 shows an example of history effect in a PDSOI transistor. To do so, we have considered a PDSOI transistor with a channel length of $L_{ch} = 1$ μm. Initially a voltage ramp is applied to the gate of the transistor during 10 ns. During this time, the drain to source voltage is set to $V_{DS} = 0.1$ V. Figure 2.27c shows the hole concentration in the body of the transistor at the end of the gate voltage ramp ($t = 10$ ns). At that moment, a high voltage pulse is applied to the drain ($V_{DS} = 3$ V) during 5 ns, while the gate voltage is kept at the value reached at the end of the ramp. In these conditions, a high value of the electric field and a high value of drain current occur near the drain edge of the channel; impact ionization mechanism [2.98] produces electron–hole pairs near the drain. While electrons are drifted to the drain, holes are stored in the neutral body of the transistor, producing the concentration increase shown in Figure 2.27d at the end of the pulse. The increase of hole concentration in the body of the transistor produces a decrease of the threshold voltage. This is the reason why the same gate voltage ramp is now applied to the transistor, the measured I_D is higher (Figure 2.27b). At the end of the new voltage ramp the hole concentration in the body of the transistor is shown in Figure 2.27e. At $t = 35$ ns, a negative voltage pulse is applied to the drain ($V_{DS} = -1.5$ V) while the gate is kept grounded. In these conditions, the body-drain junction is forward-biased, allowing the holes to escape through the drain. At the end of the negative pulse, the concentration of

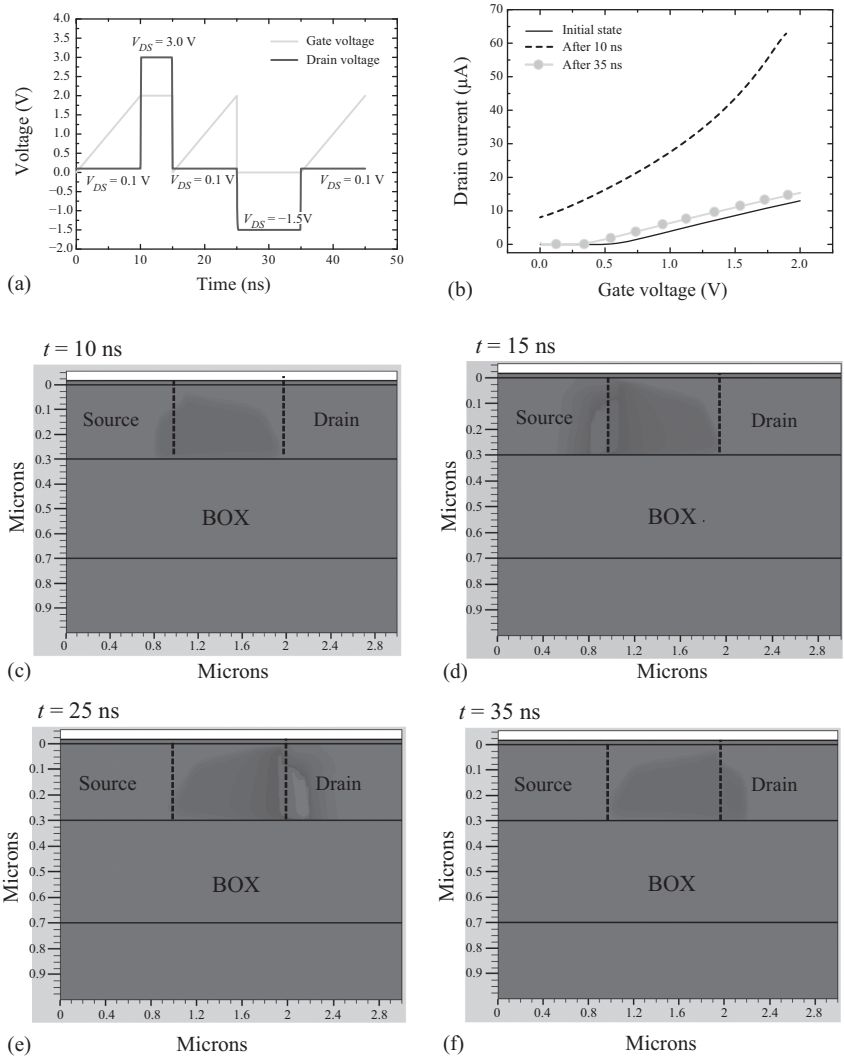

Figure 2.27 History effect in a PDSOI transistor. (a) Voltage patterns applied to the gate and drain of the transistor. (b) I_D–V_{GS} characteristics measured at different times. (c)–(f) Hole concentration in the transistor at different times

holes in the body (Figure 2.27f) is now similar to the one at $t = 0$ s. Therefore, the threshold voltage has returned to almost its initial value and when the I_D–V_{GS} characteristic is measured again, a similar curve to the first one is obtained.

The pronounced hysteresis effect observed in PDSOI transistors has been an intense matter of investigation [2.110–2.113]. Since any kind of hysteresis in a transistor entails a memory effect, much attention started to be paid to the design

and fabrication of new memory cells on SOI substrates [2.114, 2.115]. The research of the FBE in PDSOI devices rose exponentially when at the beginning of the last decade the start-up company, Innovative Silicon, introduced the Z-RAM memory cell [2.94]. The basic principle of operation of the cell was the shift induced in the threshold voltage of the PDSOI MOSFET, caused by the injection of holes in the floating-body (a transient overpopulation of holes in the floating-body) [2.116]. This transitory shift of the threshold voltage leads to two different current levels at a given bias point [2.94]. At equilibrium (stable state), the floating-body of the transistor remains neutral; this situation defines the "0" state. The "1" state is forced by charging the body with holes produced by impact ionization mechanism [2.93] that occurs when a large current flows through the device. The consequence of the stored charge is an increase in the potential of the body of the device and a decrease in the threshold voltage: for the same bias a larger current is then obtained. Figure 2.28 presents simulation results obtained, under the drift-diffusion approximation, with calibrated models for impact ionization. The top-side of the figure shows an example of the bias pattern used to demonstrate the 1T-DRAM functionality of the PDSOI MOSFET. In the bottom side, the driven current is monitored. Initially, the holes are injected in the floating-body by impact ionization due to the large current driven by the device ($V_{DS} = 1.6$ V while $V_{GS} > V_{TH}$, W "1" in Figure 2.28): the highly energetic electrons knock electrons out of their bound state and promote them to a state in the conduction band, creating electron–hole pairs. Electrons are

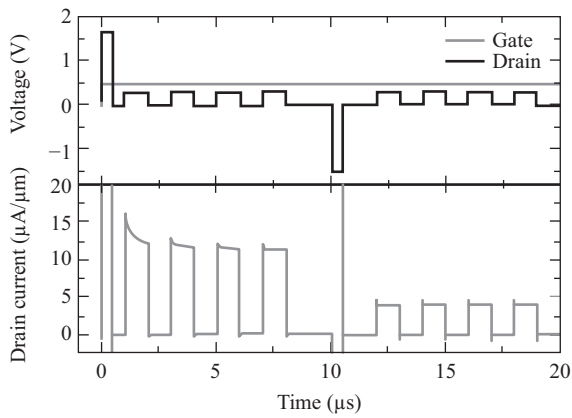

Figure 2.28 Simulation results for the operation of a PD 1T-RAM based on the Z-RAM approach. The picture shows the bias pattern (top) and the driven current (bottom). For simplicity the gate bias is maintained constant ($V_{GS} > V_{TH}$). The floating-body is initially charged with holes generated by impact ionization (W "1"), and the cell state is read four times by using a small drain bias. At $t = 10$ μs, the cell is purged (write "0" state: W "0"), and read again four times reflecting the difference with respect to the previous "1" states. $L = 1$ μm, $t_{Si} = 300$ nm, $t_{ox} = 3$nm, $t_{BOX} = 400$ nm, $N_A = 10^{17}$ cm^{-3}

evacuated through the drain, while holes are trapped into the neutral body of the silicon film. The hole overpopulation of the body of the device leads to a decrease in the threshold voltage and therefore a transitory increase of the drain current. The cell can be purged of charge by forward biasing the drain-to-body junction (negative drain bias, W "0" in Figure 2.28).

In this process, holes are evacuated from the floating-body through the channel-to-drain p–n junction. If the cell state is read again, the current level remains in the stable level (lower current). For simplicity, the gate bias has been maintained constant and larger than the threshold voltage ($V_{GS} > V_{TH}$) during the whole simulation period in order to have always a conductive channel.

2. Kink effect

The kink effect is a direct consequence of the FBE. It makes the drain current, I_{DS}, to show overshoot when applying a large V_{DS} voltage [2.89]. The charge stored in the body modifies the potential (increases in case of N-MOS), reducing therefore the threshold voltage and leading to a sudden increase in the drain current. This effect tends to appear for a high drain bias where the charge is injected in the body by impact ionization. If the large drain bias is hold for a long time, more impact ionization would be obtained leading at the end to a higher increase in drain current (positive feedback effect). An example of this effect is represented in Figure 2.29. I_D–V_{DS} curves have been calculated with Silvaco Atlas [2.117] in a PDSOI transistor for different values of the gate voltage. For the sake of comparison, dashed lines show the drain current data when impact ionization is ignored in the simulation. Solid lines (with impact ionization taken into account) show an overshoot in the drain current produced

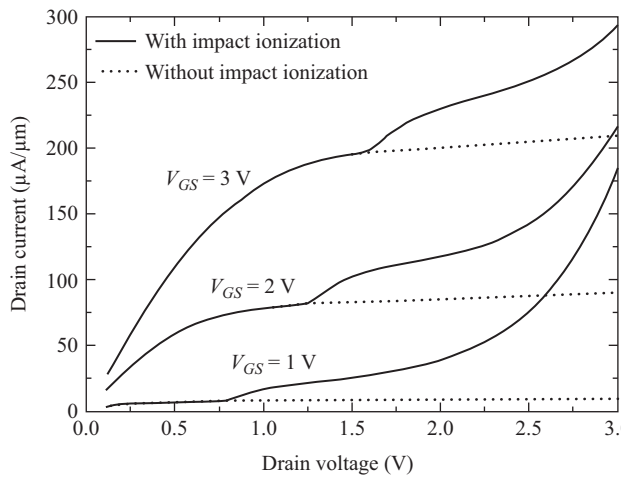

Figure 2.29 Simulated drain current versus drain voltage for different values of the gate voltage in a PDSOI transistor showing kink effect when impact ionization is considered (solid line). Kink effect disappears when impact ionization is ignored (dashed lines): $L_{ch} = 0.8$ μm, $t_{Si} = 300$ nm, $t_{ox} = 17$ nm, $t_{BOX} = 400$ nm, $N_A = 10^{17} cm^{-3}$

by the hole accumulation in the body of the transistor. This effect disappears when impact ionization is ignored (dashed lines).

If the minority carrier lifetime in the silicon film is high enough, the kink effect can be reinforced by the NPN bipolar parasitic transistor structure present in the device (second kink).

3. Transient effects

Due to the existence of the floating-body in PDSOI devices, transient effects are significant when the body is not tied to a fixed voltage [2.118].

The drain current experiences a long transient delay before reaching a stable value, thus influencing the drain current just after gate switching and in steady state. This subsequently causes different subthreshold slope and threshold voltage. When the gate is switched on, majority carriers are expelled from the depletion region (instantly formed by capacitive coupling, Figure 2.26) and collected in the neutral body, giving rise to a drain current "overshoot." The drain current decreases gradually with time during electron–hole recombination. A reciprocal "undershoot" occurs when the gate is switched from strong to weak inversion: the drain current increases with time as the majority carriers are generated and allow the depletion depth to shrink. The amplitude of current overshoot or undershoot is proportional to the difference between the final and initial body charges, and the transient duration depends on the generation-recombination rate in the film volume, at interfaces and on the edges. Figure 2.30 shows the turn-on and turn-off transients of drain current in a PD body SOI device, showing the corresponding transient effects.

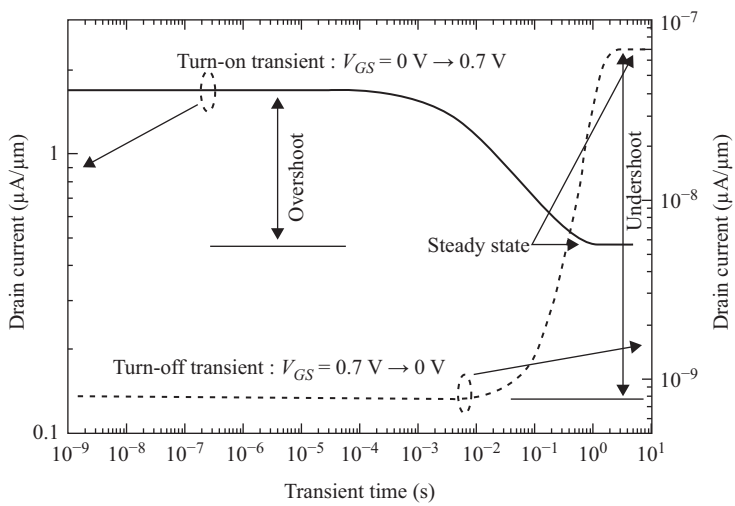

Figure 2.30 Turn-on (solid line) and turn-off (dashed line) in a PDSOI transistor. At $t = 0$ s the gate voltage is switched from 0 to 0.7 V (resp. 0.7 to 0 V) while $V_{DS} = 0.1$ V. Drain current is calculated using Silvaco Atlas until the steady state is reached. $L_{ch} = 0.8$ μm, $t_{Si} = 300$ nm, $t_{ox} = 17$ nm, $t_{BOX} = 400$ nm, $N_A = 10^{17}$ cm^{-3}

Due to the capacitance coupling between the front gate and the floating-body, switching of the front gate voltage changes the body potential momentarily. If the body of a PDSOI device is not tied to a fixed potential, carriers need to be generated or recombine through the front and back interfaces as well as through the PN junctions in order to reach steady state. This may take several seconds. Before carriers are generated or recombine, the potential is lower or higher than its final value, resulting in a change of threshold voltage and drain current. As time elapses during the turn-off transient, holes are generated and the potential in the device rises. The drain current, therefore, will also rise from a low value to its final, stable value. During the turn-on transient, holes recombine, and the potential is high initially and then returns to its final, stable value. Thus the drain current experiences a high to low transition, as shown in Figure 2.30.

These drain current transients in a PD floating-body SOI device can affect the circuit operation in various ways. The circuit may not behave similarly under different frequencies [2.119–2.121].

4. **Parasitic bipolar transistor**

If we consider an n-channel PDSOI device, the N^+-source, the P-type body, and the N^+-drain also form the emitter, the base, and the collector of an NPN bipolar transistor. As in a PDSOI transistor the body is floating (unless a contact is provided) the accumulation of the majority carriers in the body of the transistor produced by impact ionization or BTBT at the drain edge of the channel makes the body potential become high enough so that the PN (body-source) junction turns on. The NPN (Source/film/Drain) bipolar transistor is activated. The parasitic bipolar transistor (PBT) is responsible for different effects; for example, it can amplify impact ionization current and produce a reinforcement of kink effect as mentioned earlier, or also can trigger an extremely low inverse subthreshold slope and reduce the drain breakdown voltage [2.93].

Anomalous subthreshold slope, hysteresis, and single transistor latch

As mentioned in the explanation of kink effect, the generation of majority carriers by impact ionization near the drain can give rise to an increase of the body potential and a related decrease of the threshold voltage. Sometimes, a similar effect can occur at gate voltages lower than the threshold voltage. If the drain voltage is high enough, impact ionization can occur in the subthreshold region, even though the drain current is very small [2.93]. Body charging is particularly effective in weak inversion, where the current depends exponentially on potential. Figure 2.31 compares the drain current versus the gate voltage in a PDSOI MOSFET when impact ionization is considered (solid) and when impact ionization is ignored (dashed). As observed, impact ionization (solid) helps to improve the subthreshold behavior of the device. When the device is turned off, there is no impact ionization (both curves coincide) and the body potential is equal to zero. When the gate voltage is increased the weak inversion current can induce impact ionization in the high electric field region near the drain (if V_{DS} is high enough), holes are generated, the body potential increases, and the threshold voltage is reduced. Consequently, the whole

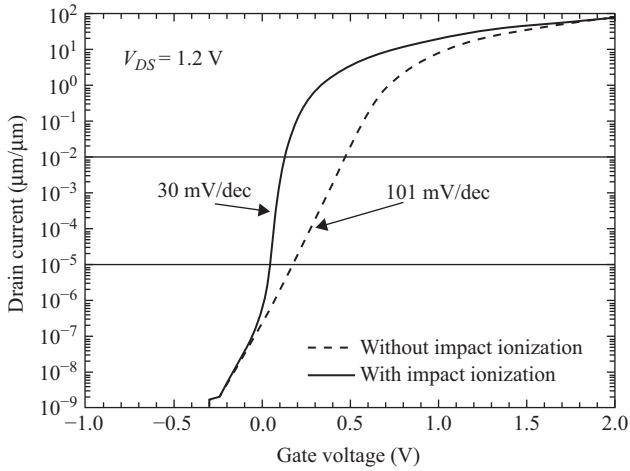

Figure 2.31 Simulated I_D–V_{GS} characteristics of a PDSOI n-channel transistor taking into account impact ionization (solid line) and ignoring impact ionization (dashed line). An anomalous subthreshold slope lower than the theoretical limit of 60 mV/dec can be observed. $L_{ch} = 0.8$ μm, $t_{Si} = 300$ nm, $t_{ox} = 17$ nm, $t_{BOX} = 400$ nm, $N_A = 10^{17}$ cm^{-3}

I_D/V_{GS} curve shifts to the left and the current can increase with gate voltage at a rate larger than 60 mV/decade, i.e., an anomalous subthreshold slope lower than the theoretical limit of 60 mV/dec can be observed [2.93].

This increase of drain current in weak inversion constitute a positive feedback loop: the higher the drain current, the higher the impact ionization, the higher the body potential, the lower the threshold voltage, and the higher the drain current, which suddenly increases with a subthreshold slope equal to zero millivolt per decade (transistor latch [2.122]) (Figure 2.32).

In Figure 2.32, for $V_{DS} = 1.8$ V, the impact ionization current that is generated near the drain during the forward gate voltage scan ($V_{GS} = -1.5 \rightarrow 2$ V) raises the body potential. The increased body bias in turn reduces the threshold voltage of the SOI MOSFET leading to an increase in I_{DS} and more impact ionization current. This positive feedback, which occurs when the impact ionization current is larger than the body-to-drain diode leakage current leads to the abrupt increase of the subthreshold current and the body potential. The positive feedback is self-limiting: increased body bias also increases the drain saturation voltage which results in lower channel electric field and smaller impact ionization current. Also, as the drain current increases, the effective potential across the channel decreases due to resistive voltage drops across the source and drain regions. During the descending V_{GS} scan, the impact ionization current under the large drain bias keeps the body potential high, which in turn keeps the MOSFET threshold voltage low, to sustain the inversion layer and a high I_{DS} until this positive feedback cannot be maintained and I_{DS} and the

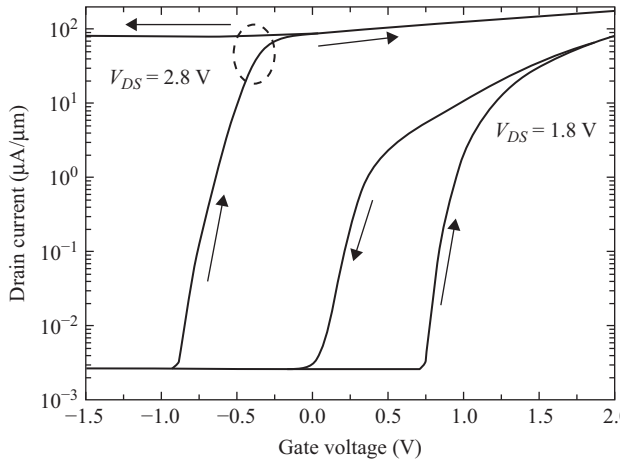

Figure 2.32 Simulated I_D current for ascending and descending scans of the gate voltage in a PDSOI transistor for two values of the drain voltage. If V_{DS} is large enough, a hysteresis cycle is observed. For even higher V_{DS} values, single transistor latch-up occurs: the inversion channel is maintained, although the gate is turned-off. $L_{ch} = 0.8$ μm, $t_{Si} = 300$ nm, $t_{ox} = 17$ nm, $t_{BOX} = 400$ nm, $N_A = 10^{17}$ cm^{-3}

body potential collapse suddenly. It can be noticed that the gate voltage at which the current suddenly raises during a forward scan is higher than the voltage at which the current suddenly falls during a reverse scan. As a consequence, hysteresis is observed in the I_D–V_{GS} curve. For $V_{DS} = 2.8$ V, the positive feedback loop cannot be turned off once it has been triggered, and the device does not turn on (at least for reasonable V_{GS} values) [2.123].

Leakage current

Another effect originated by the parasitic bipolar effect in SOI transistors is related to the subthreshold leakage current (I_{OFF}). The main involved OFF leakage currents are BTBT, impact ionization (II), and direct gate tunneling currents [2.124–2.126]. In short-channel SOI devices, these three contributions can all be amplified by the inherent PBT. When front gate is negative and drain is positive, holes are generated either by BTBT or impact ionization at the drain side and they are driven into body by the lateral electric filed. The body potential increases and turns on the source–body junction (here, playing the role of base–emitter junction); consequently electrons are injected from source and collected by the drain as collector current, I_C, which is an amplified value of the base current, I_B.

5. **Gate-induced floating-body effect**

The gate-induced floating-body effect (GIFBE) [2.127] occurs for very thin gate oxides and at strong gate voltage; the leakage currents by tunnel effect can be important, leading to body charging, a variation of the film potential (even for

low drain current) and an increase of the drain current. Experiments and simulations show that the gate-to-body current charges the body causing an unexpected "kink" effect to occur at low drain voltage. The drain current input characteristics measured at low drain voltage show a sudden increase of the drain current. This unexpected "kink" on the drain current gives rise to a second peak in transconductance, which can exceed by up to 40% the normal peak.

The classical remedy to floating-body problems is the use of a body contact in PD devices [2.93]. Using body contacts can restore the device characteristics of SOl MOSFETs back to the bulk-MOSFET-like characteristics [2.128]. Body contact, however, carries a delay penalty and loses the body effect advantage of SOl devices. Advantage can be taken of current overshoot effects and increased current drive due to the kink effect to boost switching speed and therefore, circuit performance [2.129]. However, elaborate circuit models need to be used to avoid unexpected device behavior due to FBE [2.93, 2.129].

2.2.2.2 Fully depleted SOI transistor

FBE can be largely avoided in FD SOl devices in which either the silicon film is thin enough or the doping is light enough that the entire film is depleted, i.e., there is no neutral region in the body. In fact, the entire silicon film can be undoped because FDSOl MOSFETs scale by the silicon film thickness, not by the gate depletion width (x_D) as bulk and PDSOl CMOS do. The inverse subthreshold slope of a long-channel FDSOl MOSFET can be near the ideal 60 mV/decade number at 300 K. Figure 2.33 compares the charge distribution in a PDSOI transistor (left, $T_{Si} = 400$ nm) and an FDSOI transistor (right, $T_{Si} = 100$ nm) with the same channel length. Doping concentration was fixed to $N_A = 10^{17}$ cm^{-3} and a $V_G = 1$ V is applied to the front gate.

In the case of FDSOI device, the whole channel is depleted (charged), while in the PDSOI device, there is a neutral region (dark area) under the channel. The lack of neutral region in an FDSOI transistor makes that the front and back surface

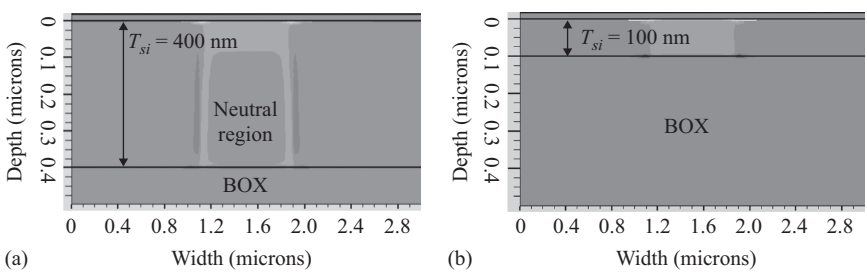

Figure 2.33 Total charge concentration in a PDSOI transistor (a) and in an FDSOI transistor (b) Dark gray indicates zero total charge. The neutral region in the body is clearly observed in the PDSOI transistor, while the body of the FDSOI transistor is FD and therefore charged

potentials become inter-related [2.87], and FDSOI technology presents numerous advantages:

- The possibility to non-dope the conduction channel enables increasing the mobility compared with a PDSOI transistor.
- Short-channel effects are largely reduced if T_{Si} is very small [2.130, 2.131].
- Lower threshold voltage compared to Si bulk technologies allows low power consumption applications.
- The subthreshold slope (S) is reduced due to the replacement of the dynamic depletion capacitance (C_{dep}) by a fixed Si film capacitance ($C_{Si} = \varepsilon_{Si}/t_{Si}$).

Interface coupling means that the electrical characteristics of one channel vary with the bias applied to the opposite gate. In FDSOI MOSFETs, two inversion channels can be activated, one at the front Si–gate oxide interface and the other at the back Si–BOX interface. A better coupling is then obtained between the gate bias and the inversion charge, leading in particular to an increase of the drain current. Because the front and back interface can either be in accumulation, depletion, or inversion, there are nine possible modes of operation in an FDSOI transistor, as a function of the front gate voltage and back gate voltage. In particular, the threshold voltage of the front gate depends on the bias of the substrate or back-gate voltage, V_{G2}.

Figure 2.34 represents I_D–V_G characteristics of an FDSOI device with $T_{Si} =$ 50nm for different conditions of the back interface: solid line corresponds to the case when the back interface is in depletion; dash-dot line corresponds to the case when the back interface is in accumulation. If a positive voltage is applied to the substrate or back gate (V_{G2}), the back interface becomes inverted (dashed line).

Figure 2.35 shows the transconductance of the FDSOI device with a $T_{Si} = 50$ nm, for different states of the back interface. In general, the transconductance of FDSOI devices is complicated function of the gate voltage because of the influence of the back interface on the front channel threshold voltage. As observed in Figure 2.18 the transconductance has its maximum value when the back channel is in depletion. When the back interface is in inversion, the transconductance curve shows a plateau, originated by the activation of the back channel before the front channel [2.132].

Threshold voltage

The threshold voltage of an FDSOI device can be obtained by solving the Poisson equation [2.93]. If ϕ_{S1} and ϕ_{S2} are the surface potential at both interfaces (front and back) (Figure 2.36), the front and back gate voltages, V_{G1} and V_{G2}, respectively, can be expressed as

$$V_{G1} = \phi_{s1} + \phi_{ox1} + \phi_{MS1} \tag{2.21}$$

$$V_{G2} = \phi_{s2} + \phi_{ox2} + \phi_{MS2} \tag{2.22}$$

where ϕ_{oxi} and ϕ_{MSi} are the potential drop across the front (resp. back) gate oxide and the front (resp. back) workfunction differences.

Figure 2.36 shows the potential distribution in an FDSOI device with $t_{Si} = 50$ nm for two conditions of the back interface, inversion (solid line), and accumulation (dashed line). Electron and hole concentrations in the direction perpendicular to the channel are also shown in Figure 2.37.

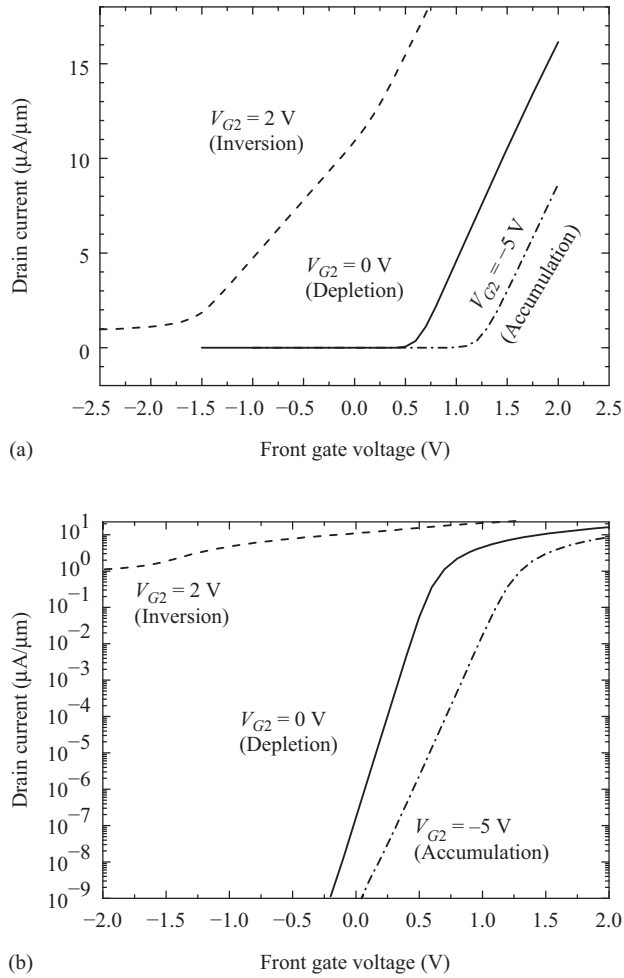

Figure 2.34 Calculated I_D–V_{GS} characteristics of an FDSOI device with $T_{Si} = 50$ nm for different conditions of the back interface (a) linear scale, (b) log scale

We can obtain a relationship between the front gate voltage and the surface potentials [2.91, 2.93]:

$$V_{G1} = \phi_{MS1} - \frac{Q_{ox1}}{C_{ox1}} + \left(1 + \frac{C_{Si}}{C_{ox1}}\right)\phi_{s1} - \frac{C_{Si}}{C_{ox1}}\phi_{s2} - \frac{\frac{1}{2}Q_{depl} + Q_{inv1}}{C_{ox1}} \tag{2.23}$$

$$V_{TH1,depl2} = V_{TH1,acc2} - \frac{C_{Si}C_{ox2}}{C_{ox1}(C_{Si} + C_{ox2})}\left(V_{G2} - V_{G2,acc}\right) \tag{2.24}$$

$$V_{TH1,inv2} = \phi_{MS1} - \frac{Q_{ox1}}{C_{ox1}} + 2\phi_F - \frac{Q_{depl}}{2C_{ox1}} \tag{2.25}$$

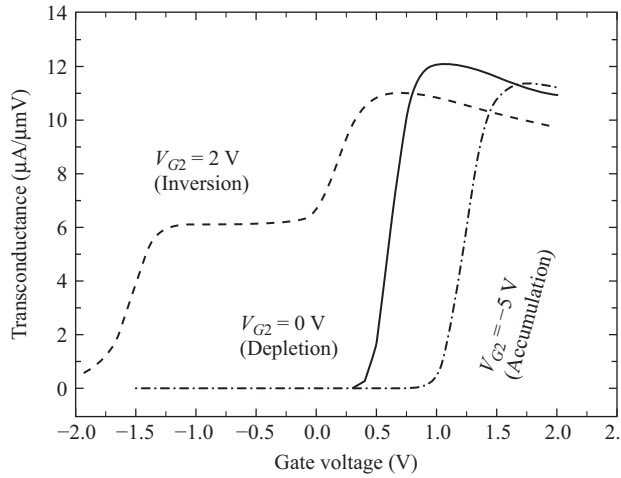

Figure 2.35 Calculated transconductance for the device of Figure 2.34 in different conditions of the back interface (accumulation, depletion, and inversion)

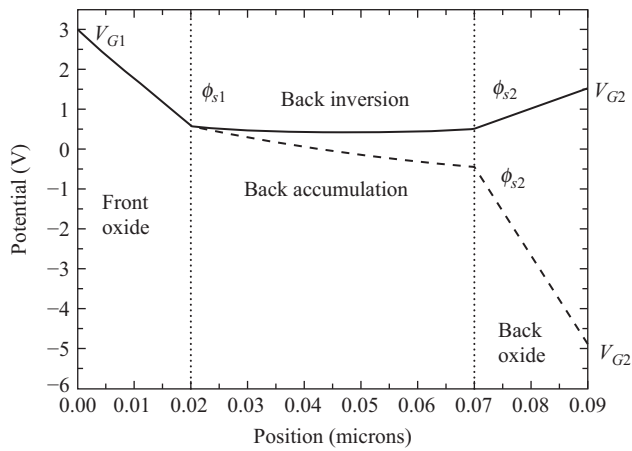

Figure 2.36 Potential distribution in an FDSOI device with $t_{Si} = 50$ nm for two conditions of the back interface: inversion (solid line) and accumulation (dashed line)

where Φ_F is the Fermi potential, equal to $\frac{kT}{q} ln(\frac{N_A}{n_i})$, and $V_{G2,acc}$ is the value of the back gate voltage for which the back interface reaches accumulation and is given by

$$V_{G2,acc} = \phi_{MS2} - \frac{Q_{ox2}}{C_{ox2}} + 2\left(1 + \frac{C_{Si}}{C_{ox1}}\right)\phi_F - \frac{Q_{depl}}{2C_{ox2}} \tag{2.26}$$

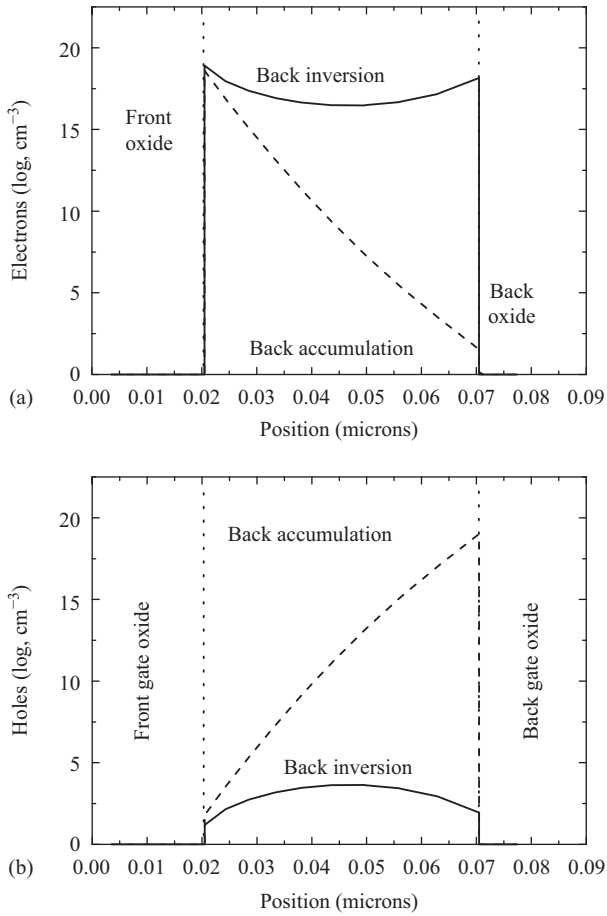

Figure 2.37 (a) and (b) Electron and hole concentrations in an FDSOI device with $t_{Si} = 50$ nm for two conditions of the back interface: inversion (solid line) and accumulation (dashed line)

Figure 2.38 shows the evolution of the front gate threshold voltage with the back gate voltage. When the back interface is in accumulation (or inversion), the front threshold voltage slightly increases (or decreases).

The dependence of the threshold voltage with the silicon thickness has been studied by different authors [2.133, 2.134]. If the device is PD, the threshold voltage does not depend on the silicon thickness. In an FD transistor, the threshold voltage decreases with the silicon thickness. This is due to the reduction of the depletion charge as the silicon thickness decreases (Figure 2.39). When the film thickness is below 10 nm, a threshold voltage rebound is observed: the conduction band splits into subbands and the minimum energy of the conduction band increases as the film thickness decreases [2.134].

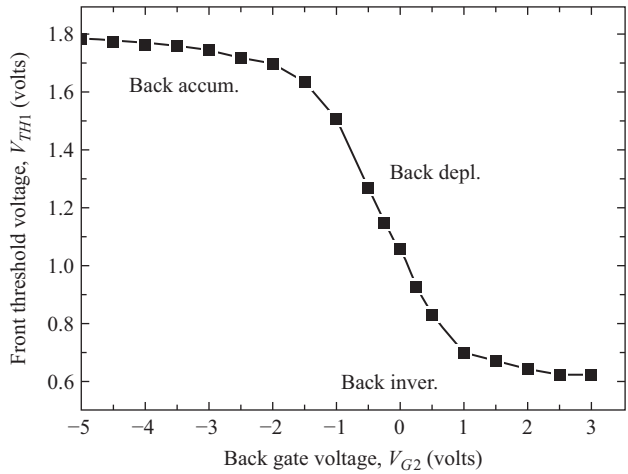

Figure 2.38 Dependence of the threshold voltage with the back gate bias in an FDSOI transistor

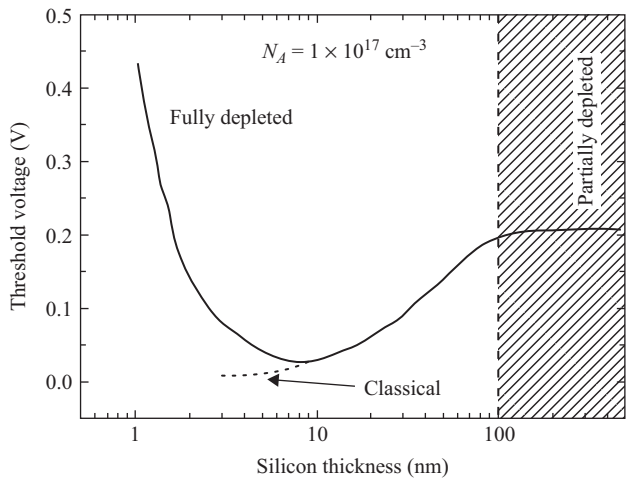

Figure 2.39 Evolution of the threshold voltage of a SOI transistor with the silicon thickness. When the device is PD, threshold voltage does not depend on the silicon thickness. As the silicon thickness decreases and the device become FDSOI, V_{TH} decreases. Below 10 nm, quantum effects make V_{TH} to increase

Subthreshold slope

The fact that the depletion region is constant in an FDSOI device improves the subthreshold slope when comparing with PDSOI devices as shown in Figure 2.40:

The subthreshold slope S is defined as

$$S = \frac{dV_G}{dlog(I_D)} \tag{2.27}$$

which in the case of a bulk MOSFET or a PDSOI transistor can be written as

$$S = \frac{kT}{q} ln(10)\left(1 + \frac{C_D + C_{it}}{C_{ox}}\right) \tag{2.28}$$

where C_D is the depletion capacitance, $C_D = \mathrm{d}Q_D/\mathrm{d}\phi_s$, and C_{it} is the capacitance related to the interface traps. In an FD transistor with depleted back interface, the subthreshold slope can be expressed as [2.135]

$$S^{dep} = \frac{kT}{q}\ln(10)\left(1 + \frac{C_{it1}}{C_{ox1}} + \alpha_1 \frac{C_{Si}}{C_{ox1}}\right) \tag{2.29}$$

α_1 is the interface coupling coefficient, given by

$$\alpha_1 = \frac{C_{ox2} + C_{it2}}{C_{Si} + C_{ox2} + C_{it2}} \tag{2.30}$$

which accounts for the influence of the back interface traps and the buried oxide (BOX) thickness, and it is always smaller than 1.

The comparison between (2.28) and (2.29) shows that the inverse subthreshold slope of an FDSOI device is smaller than that of a PDSOI transistor, with the same parameters, as observed in Figure 2.40. By accumulating the back channel, the

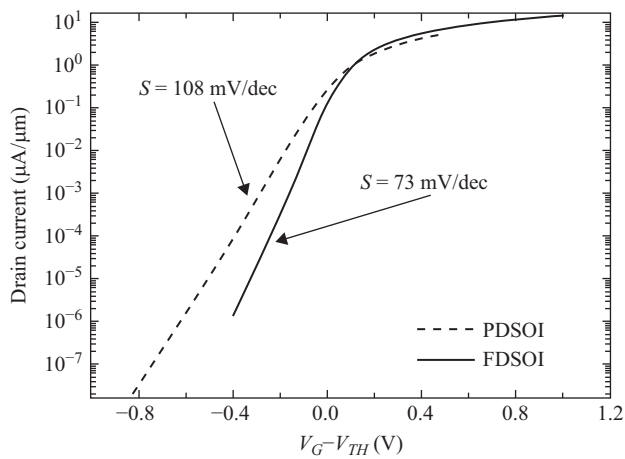

Figure 2.40 Comparison of subthreshold characteristics of PDSOI and FDSOI transistors

front inversion channel becomes decoupled from the defects in the back interface and α_1 tends to 1 [2.135], causing an overall degradation of the subthreshold slope, as shown in Figure 2.40. As a result, S has the lowest value in an FD device, it is larger in the bulk of PDSOI device, and even larger in the FD device with back accumulation.

The subthreshold slope normally improves for thinner silicon films and thicker BOXs, only in the case of few states at the silicon layer/BOX interface [2.133]. On the contrary, a high concentration of interface traps at the buried interface strongly degrades the subthreshold swing.

Short-channel effects in FDSOI devices

In a bulk MOSFET, the reduction of the channel length produces numerous effects so-called short channel effects and whose last origin is the loss of control by the gate of the depletion zone below it, i.e., the depletion charge under the gate it is not totally controlled by the gate because of the encroachment from the source and drain. This results in a roll-off of the threshold voltage as the channel length decreases [2.76] [2.76]. In bulk-Si MOSFETs, increasing the substrate doping and forming shallow junctions enable length scaling. However, ultra-large doping degrades the carrier mobility and promotes BTBT current thus increasing leakage currents.

In FDSOI devices, the fraction of depletion charge controlled by the gate is larger than that in a bulk MOSFET for the same channel length, and the situation improves as the silicon thickness decreases. Figure 2.41 shows the threshold voltage roll-off in bulk and SOI devices for different values of the silicon thickness, t_{Si}.

DIBL is another SCE also due to charge sharing between the gate and the source/drain junctions. It occurs in both bulk and SOI devices, although as in the case of threshold voltage roll-off, in SOI, it is better controlled by reducing the film thickness [2.100]. However, the major SCE in SOI is due to the penetration of the electric field from the drain into the BOX and the substrate (Figure 2.42) [2.135].

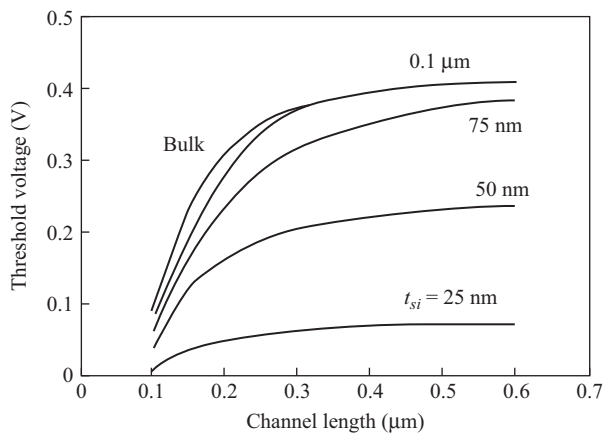

Figure 2.41 Variation of the threshold voltage as a function of the channel length for different values of the silicon thickness in a SOI transistor

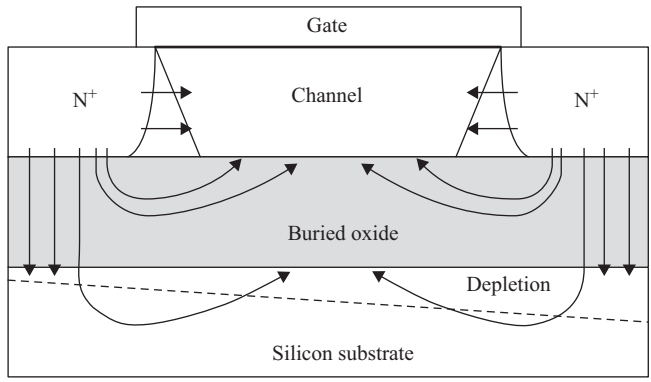

Figure 2.42 Drain-induced virtual substrate biasing (DIVSB) effect

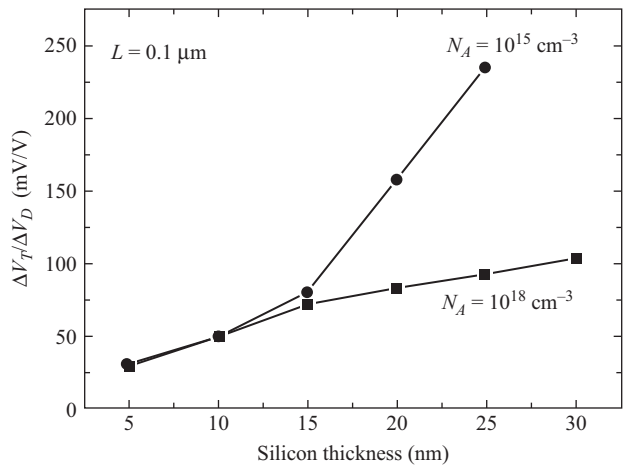

Figure 2.43 Threshold voltage lowering induced by DIBL and DIVSB in highly doped and undoped SOI MOSFET as a function of the silicon thickness

The fringing field tends to increase the surface potential at the film–BOX interface. As mentioned earlier, front and back interfaces are coupled in FDSOI devices; therefore the front-channel properties become degraded. For example, the threshold voltage is lowered with increasing drain bias, as in DIBL, but caused by a different effect.

Figure 2.43 compares the threshold voltage lowering induced by DIBL and DIVSB in highly doped and undoped SOI MOSFETs as a function of the silicon thickness. For silicon thicknesses below 15 nm, ΔV_T becomes very small even for undoped substrates. It is concluded that an undoped and ultra-thin silicon layer is extremely robust to SCEs. Further improvements of SCEs could be obtained

reducing the effect of the fringing field, for example, using thinner BOX, multigate devices, or using a ground plane (GP) or back plane (BP), i.e., a highly doped region or metal layer underneath the BOX [2.137].

Self-heating

SOI transistors are thermally insulated from the substrate by the buried insulator. As a result, the heat generated inside the device is not efficiently removed and the temperature of the device increases up to more than 150 ºC, and a mobility reduction is observed [2.138, 2.139]. Due to self-heating and the mobility degradation as V_{DS} increases, a negative resistance can be seen in the output characteristics of SOI MOSFETs.

Figure 2.44 shows the output characteristics of a SOI transistor with a channel length of 1 μm calculated with Silvaco ATLAS [2.117] under continuous conditions (solid line) and under pulsed conditions (symbols, 0.1% duty cycle, 1 ms period). When the device is measured under continuous conditions, the effect of self-heating is evident. Drain current decreases as drain voltage increases because of the increase of the lattice temperature that produces mobility degradation.

Figure 2.45(a) shows the lattice temperature in the device at $V_{GS} = 5$ V and $V_{DS} = 3.5$ V calculated in DC conditions. The lattice temperature highly increases in the body of the SOI transistor, which produces a strong degradation in the mobility. The poor heat conductivity of SiO_2 prevents the sink of the heat generated

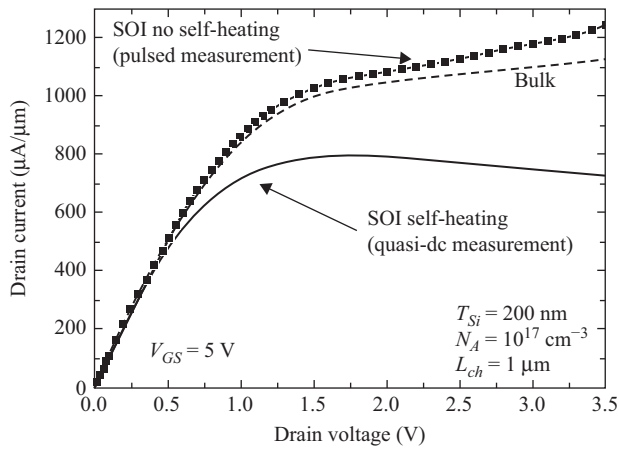

Figure 2.44 Calculated output characteristics of a SOI transistor: (a) under quasi-DC conditions (solid line) the effect of self-heating and the negative resistance can be observed, (b) under pulsed-conditions (symbols) (0.1% duty cycle, 1 ms period) no self-heating effect is observed. (c) For the sake of comparison, the output characteristics of a bulk transistor with the same parameters as the SOI transistor have been simulated (dashed line). No degradation of the output conductance is observed

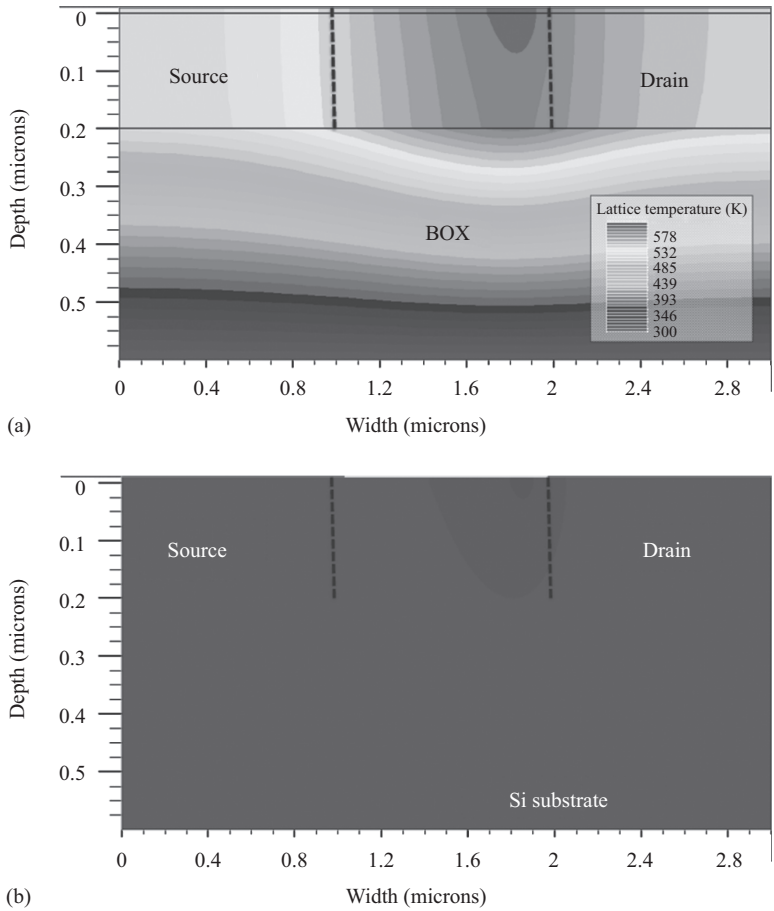

Figure 2.45 (a) Lattice temperature in the SOI device of Figure 2.44 for $V_{GS} = 5$ V and $V_{DS} = 3.5$ V calculated under DC conditions. (b) Lattice temperature in a bulk device with the same characteristics and calculated in the same conditions

in the device. For the sake of comparison a similar bulk device has been considered working in the same conditions as the SOI transistor. Figure 2.45(b) shows that the increase of the temperature is much lower in the case of the bulk device, and therefore the degradation of the mobility because the increase of the temperature is very weak. The output characteristics for the bulk device calculated for the same conditions as the SOI device are shown in dashed line in Figure 2.44.

As the silicon layer is made thinner, self-heating is accentuated [2.100]; this is why FD SOI MOSFETs are more affected. The channel temperature is also raised with increasing the BOX thickness and the channel-to-contact separation. Fortunately, self-heating is highly reduced under dynamic and/or low-voltage operation. As discussed in Reference 2.93, self-heating takes place as power is

dissipated in the device, as is the case when the device is measured in quasi-DC mode, but not in operating digital CMOS circuits, since there is virtually no current flowing through the devices in the standby mode, and power is dissipated in the devices only during switching for short periods of time normally. However, if the duty cycle or the frequency are large, although the negative resistance would not be a problem for digital circuits, the increase of the overall local temperature should be taken into consideration, since mobility could be modified [2.90].

For analog circuits, heating effects are more serious: the output conductance of a transistor becomes frequency dependent because of self-heating. Analog designers must take into account self-heating and use circuit simulation models in which this effect is included [2.140, 2.141].

2.2.3 Ultra-thin FDSOI MOSFETs

As discussed previously, for ultimate scaling, FDSOI devices consist of an undoped ultra-thin silicon layer ($T_{Si} < 15$ nm) sandwiched between two oxide layers. In this situation, electrons are quantized in the direction perpendicular to both Si/SiO_2 interfaces, but they can move freely in the plane parallel to them [2.142]. This confinement of the carriers in the direction perpendicular to the channel greatly modifies their transport behavior, and as a consequence, in addition to the advantages mentioned earlier, ultra-thin SOI devices specifically present other benefits, as highlighted below.

2.2.3.1 Electron distribution and quantum effects

In these ultra-thin devices, the maximum extension of the electrons in the direction perpendicular to both Si/SiO_2 interfaces is limited by the silicon thickness that is comparable to the De Broglie wavelength of the carriers. As a consequence, to accurately evaluate the electron distribution in these structures we must self-consistently solve the 1D-Schrödinger and Poisson equations in the direction perpendicular to both Si/SiO_2 interfaces [2.143, 2.144]. The reduction of the silicon film thickness sandwiched between the two oxide layers causes important effects on electron distribution and on electron transport properties, such as the *subband modulation effect*.

The size quantization in the silicon inversion layer produces a redistribution of the carriers between the two subband ladders, which arise from the split of the degeneracy of the six equivalent valleys of bulk silicon [2.142, 2.145]. In SOI inversion layers, the redistribution of the inversion electrons is more acute as the silicon layer shrinks and the following consequences are observed [2.146]:

1. A reduction in the conduction effective mass of electrons in the inversion layers as T_{Si} is reduced. A lower effective conduction mass means a greater electron velocity for the same drift field value, and thus a greater mobility [2.144]. The reduction of the conduction effective mass of electrons as the silicon layer thickness decreases can clearly be observed in Figure 2.46, where the average conduction effective mass versus the total electron concentration for different silicon layer thicknesses is shown.

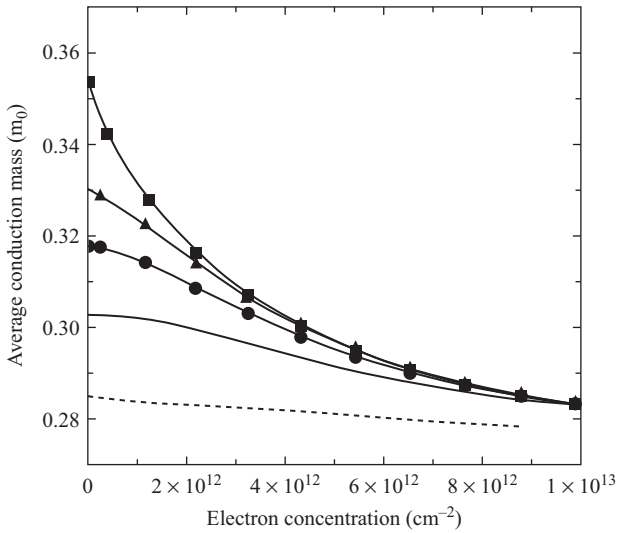

Figure 2.46 Average conduction effective mass versus the inversion charge concentration for different silicon layer thicknesses in a SGSOI inversion layer. (■ $T_{Si} = 50$ nm, ▲ $T_{Si} = 25$ nm, ●$T_{Si} = 15$ nm, (solid) $T_{Si} = 10$ nm, (dashed)$T_{Si} = 5$ nm)

2. A reduction of the intervalley scattering rate between non-equivalent valleys (f-scattering, [2.144, 2.146]) due to the greater separation of the energy levels related to prime subbands with respect to the non-prime ones as the silicon film thickness is reduced.

Both effects, 1 and 2, simultaneously contribute to an electron mobility increase.

Phonon-scattering increase

Another important effect that appears in SOI-inversion layers as the silicon layer thickness is reduced is an increase in the phonon-scattering rate [2.147]. The electron confinement in ultra-thin SOI-inversion layers is greater than in bulk-inversion layers [2.144, 2.146]. Thus, the uncertainty concerning the location of the electrons in the direction perpendicular to the interface is less in SOI samples than in bulk samples. In accordance with the uncertainty principle, there is a wider distribution of the electron's momentum perpendicular to the interface. In other words, due to size quantization, the electrons interface-directed momentum does not have a single value (as in 3D electrons), but a distribution of possible values that expands as the silicon layer thickness is reduced. Taking into account the momentum conservation principle, there are more bulk phonons available that can assist in transitions between electron states, and therefore an increase in the phonon-scattering rate is expected. As a consequence, for the same inversion-charge concentration, the phonon-scattering

rate is greater in thinner films than in thicker ones (since the confinement is greater), and therefore a mobility reduction can be expected [2.146].

Subband modulation effect and phonon-scattering increase, discussed earlier, indicate that two opposing trends appear in electron mobility as the silicon layer thickness is reduced. However, the contribution of these two trends varies depending on the considered structure and on the temperature. It would be interesting to know which of these trends, if either, is dominant, and whether there is a critical silicon layer thickness at which a change in mobility behavior is observed: in other words, if a change is produced in the trend of electron mobility as the silicon layer thickness is reduced.

2.2.3.2 Electron mobility in ultra-thin FDSOI transistors

Electron mobility behavior in ultra-thin SOI inversion layers has been calculated using a one-electron MC simulator. Phonon and surface-roughness scattering have been taken into account. In ultra-thin FDSOI structures, the silicon layer is usually left undoped, and if, in addition, the Si/SiO2 interfaces are of good quality (which is desirable), the interface charge concentration is also quite small. As a consequence, Coulomb scattering is much less important than phonon and surface-roughness scattering, especially at intermediate and high inversion charge concentrations. Bulk electron–phonon scattering models considering acoustic deformation potential scattering and intervalley scattering (between both equivalent and non-equivalent valleys [2.143, 2.148]) have been considered. If the scattering mechanisms related to the presence of the Si/SiO_2 interface significantly affect the electron transport properties in bulk silicon inversion layers, one can easily understand that this effect should, at least a priori, be taken into account in those physical systems where electrons are simultaneously affected by two such $Si–SiO_2$ interfaces. This is the case of the ultra-thin SOI inversion layers: the presence of a second interface plays a very important role, both by modifying the surface-roughness scattering rate due to the gate interface, and by itself providing a non-negligible scattering rate. In addition, we have shown that the usual surface-roughness scattering model in bulk silicon inversion layers overestimates the effect of surface-roughness scattering arising from one of the interfaces as a consequence of the presence of the other [2.145, 2.149]. Therefore, it was necessary to improve the surface-roughness model in order to calculate the scattering rate due to both interfaces (which are assumed not to be correlated) [2.143, 2.145, 2.148].

Figure 2.47a shows mobility curves versus the electron concentration for different values of silicon layer thicknesses, t_{Si}, at room temperature. Phonon scattering and surface-roughness scattering were taken into account.

The following surface-roughness parameters were assumed: $\Delta_{m1} = \Delta_{m2} = 0.1$ nm, $L_1 = L_2 = 1.5$ nm, where Δ_{mi} and L_i are the rms value and the autocovariance length of the roughness fluctuations, respectively. The effect of surface-roughness scattering is more acute at high inversion charge concentrations and in the thinnest samples. In the latter case, the effect of surface-roughness scattering is noticeable even at very low transverse effective fields. There is more than one trend in the electron mobility as the silicon thickness is reduced, and this behavior strongly depends on the electron concentration. To see this more clearly, the evolution of

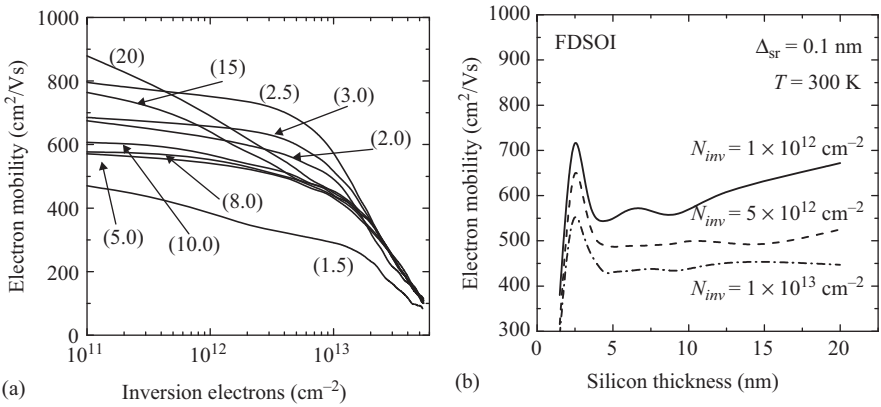

Figure 2.47 *(a) Electron mobility curves in an ultra-thin FDSOI MOSFET at room temperature versus the inversion electron concentration for different values of the silicon layer thickness (T_{Si}). Phonon scattering and surface-roughness scattering due to both interfaces ($\Delta_{m1} = \Delta_{m2} = 0.1$ nm), ($L_1 = L_2 = 1.5$ nm) have been considered. The thickness of the silicon layer is expressed in nanometers between parentheses. (b) Evolution of electron mobility in an FDSOI MOSFET with the silicon layer thickness for different values of the inversion charge concentration at room temperature*

electron mobility with the silicon layer thickness for different values of the transverse effective field is shown in Figure 2.47b. Three regions can be distinguished:

1. For high silicon thickness values, electron mobility tends toward the mobility value in bulk inversion layers.
2. As T_{Si} decreases, electron mobility gradually decreases until a minimum is reached around 5 nm.
3. Then it quickly increases until a maximum at 3 nm is reached, and then abruptly falls.

This behavior is a direct consequence of the opposing trends mentioned earlier.

2.2.3.3 Ultra-thin BOX

From the point of view of the control of SCEs, ultra-thin SOI technology presents another important advantage compared to standard bulk devices: the addition of new degrees of freedom in the definition of the device geometry, i.e., the thicknesses of the silicon and buried oxide layers. In this way, the scaling is carried out thanks to a channel thickness reduction instead of the implantation of complicated doping profiles with very high doping densities. Following the classical scaling

rules for bulk MOSFETS, the maximum depth for source and drain implants must be close to $L_G/5$ [2.150]. Therefore, the fabrication of decanano bulk devices demands an important reduction in the implant depth of source and drain regions with the subsequent challenge of obtaining higher doping densities stopping the dopant diffusion to reach the targeted depth. This issue disappears in ultra-thin SOI technology since the BOX constitutes a natural barrier to dopant diffusion. The scaling rules stand also different for bulk and SOI devices. In the case of FDSOI devices, the silicon thickness plays the role of the implant depth, however the conventional design rule can be modified to a less restrictive $L_G/T_{Si} = 4$ [2.151]. In this way, a 4 nm silicon slab would be necessary for a 16 nm channel-length device. However, for T_{Si} smaller than 5 nm two effects limit the use of FDSOI devices: On the one hand, it is very difficult to keep good enough thickness uniformity at wafer level to avoid V_{TH} fluctuations. On the other hand, electron mobility is dramatically reduced as a consequence of confinement effects [2.152].

The condition $L_G/4$ can be relaxed for Multiple-Gate FET devices (as will be discussed later) where the recommended T_{Si} to minimize SCEs follows $N_G L_G/4$ being N_G the effective number of gates [2.153]. Therefore, if we use a double gate structure ($N_G = 2$), the necessary thickness of the silicon slab in the previous example will be increased to 8 nm; if we use a three-gates structure, the necessary silicon thickness will be 12 nm. In both cases, the thickness of the silicon layer is large enough to avoid the above problems of degradation of the mobility and variability. In most cases, the use of multiple-gate devices means the use of 3D architectures whose mass production implies important efforts from an economical and technological point of view.

Therefore, it is necessary to relax the channel length to thickness constraint to extend the use of ultra-thin single-gate FDSOI (SGSOI) transistors to the future nodes. There is still an unexploited way to improve SCEs control for SGSOI devices and, thus, to extend the use of FDSOI devices beyond the limit given by standard design rules considering a thick BOX, as it has been the standard up to now. The use of ultra-thin BOX (UTBOX) and the addition of a GP, i.e., a highly doped region underneath the BOX, can improve the behavior of the device. This fact has been already experimentally demonstrated for gate lengths of 33 nm as shown in Reference 2.154.

Different authors have studied the possibilities that the combined use of UTBOX + GP offers to determine whether the scaling of planar FDSOI devices makes possible to fulfil the requirements of sub-32 nm nodes reducing the impact of thickness fluctuation effects [2.154–2.157]. As the channel length is reduced, the control of DIBL and V_{TH} roll-off is one of the biggest challenges from the point of view of device optimization. Figure 2.48 shows I_D–V_{GS} curves for an FDSOI transistor with a channel of 18 nm with different BOX configurations. These current curves have been calculated using a multi-subband MC simulator described elsewhere [2.158–2.160].

The gate stack structure includes a midgap metal and an HfO_2/SiO_2 dielectric bilayer with an EOT of 1.2 nm, which is in the order of the recommended for a well-tempered decanano device [2.161]. For all the cases T_{Si} is fixed to 6 nm, which

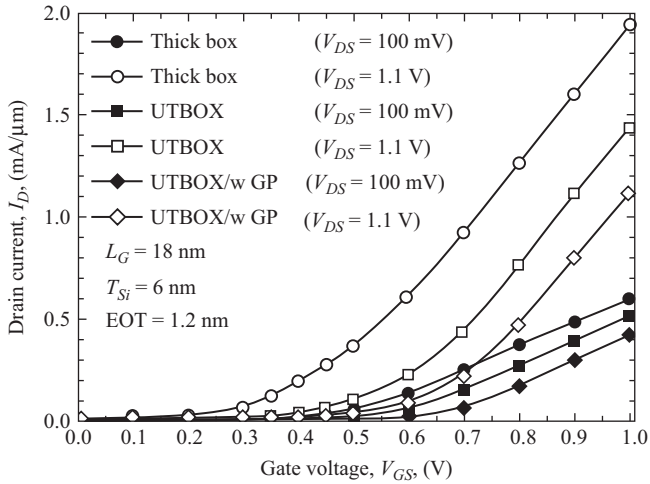

Figure 2.48 *I_D versus V_{GS} curves for the 18 nm FDSOI devices calculated at $V_{DS} = 100$ mV (closed symbols) and $V_{DS} = 1.1$ V (open symbols). It can be observed the important variation of the characteristics for the standard thick BOX devices demonstrating that the scaling for such architecture cannot be extended beyond the standard rules*

fits the requirements for a 24 nm channel length following the standard rule [2.151]. Concerning the BOX, three configurations were studied:

1. a standard thick BOX ($T_{BOX} = 145$ nm),
2. an Ultra-thin BOX (UTBOX, $T_{BOX} = 10$ nm),
3. the same UTBOX ($T_{BOX} = 10$ nm) but including a GP contact with $N_A = 3.0 \times 10^{18}$ cm^{-3}.

In all the cases, source and drain regions are doped with $N_D = 5.2 \times 10^{19}$ cm^{-3}, where a Gaussian transition profile is considered into the channel with no variation of the doping in the transversal direction.

As can be observed in Figure 2.48, the different BOX configurations have a considerable impact especially on the threshold voltage at both high and moderate drain bias. From the results it can be inferred that the use of thick BOX is not recommended due to the important variation on the V_{TH} requiring a channel thinner than 5 nm in order to fulfill the scaling rules. However, this will not make things much better since the aforementioned problems from the point of view of performance and variability will start to play an important role. Focusing on UTBOX options, the variation of the characteristics from high to moderate V_{DS} remains under control and a closest study is necessary to determine whether UTBOX or UTBOX + GP could meet the minimum requirements on SCEs

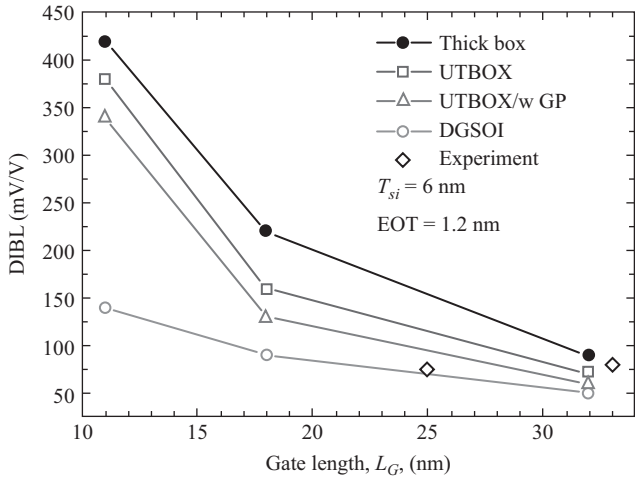

Figure 2.49 DIBL as a function of the gate length including the different BOX configurations for FDSOI, and the corresponding DGSOI device (open circles). For the sake of comparison, experimental results obtained for $L_G = 33$ nm and $L_G = 25$ nm are also shown (diamonds)

control. Figure 2.49 shows the channel length dependence of the DIBL for the different devices under study.

As expected, there is an important increase of DIBL as L_G is reduced; however, the UTBOX + GP device keeps it under control (130 mV/V) for the 18 nm device (triangles). For the sake of comparison, results corresponding to a Double-Gate SOI transistor (discussed later) with $T_{Si} = 6$ nm are also shown. DGSOI devices show smaller values of DIBL as a consequence of the higher electrostatic control as will be discussed later. Diamond symbols represent experimental results for $L_G = 33$ nm [2.154] and $L_G = 25$ nm [2.162] ultra-thin FDSOI devices.

Concerning another important consequence of scaling, V_{TH} roll-off as a function of the gate length, Figure 2.50a shows the evolution of threshold voltage as a function of L_G for the three considered BOX configurations. As the gate length is decreased, a reduction of V_{TH} is observed for all the cases; however the smallest variation among the FDSOI devices occurs again for the UTBOX configurations (triangles and squares). The use of UTBOX also increases V_{TH} respect to the standard thick BOX case for a given length due to the electrostatic influence of the BOX. This fact allows keeping a single metal gate for both p and n devices, which is not possible if V_{TH} becomes very small since the noise margins are dramatically reduced. The impact of channel thickness in UTBOX devices has been also studied. Figure 2.50b shows I_D–V_{GS} curves for $V_{DS} = 1.1$ V (open symbols) and $V_{DS} = 100$ mV (closed symbols) corresponding to the 18 nm device and silicon thickness ranging

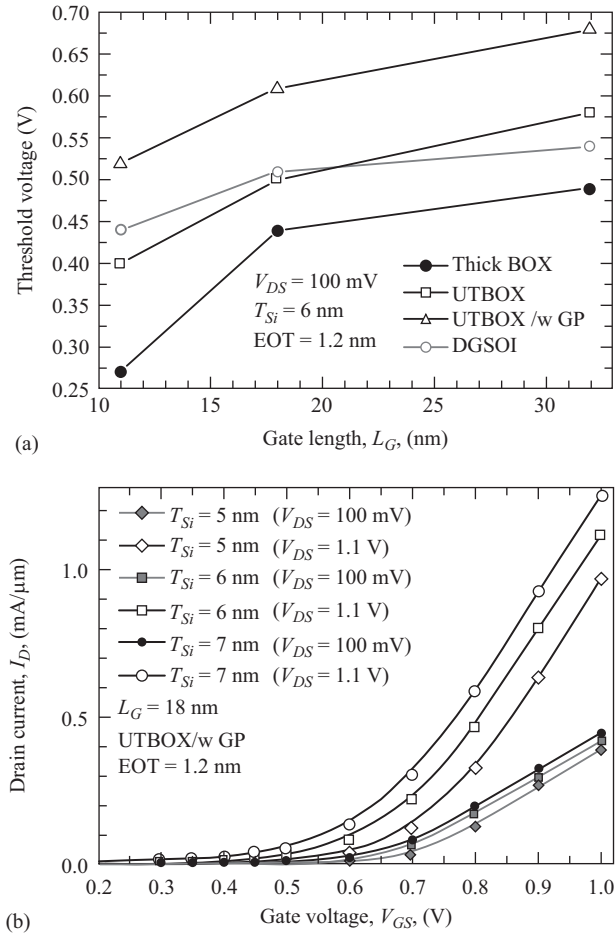

Figure 2.50 (a) Threshold voltage as a function of the gate length for all the BOX configurations and the DGSOI reference device (open circles). For all the cases the same midgap metal gate is used. (b) I_D versus V_{GS} curves for the 18 nm FDSOI devices calculated at $V_{DS} = 100$ mV (closed symbols) and $V_{DS} = 1.1$ V (open symbols) and T_{Si} ranging from 5 to 7 nm. The variation of the characteristics can be specially noticed for saturation bias conditions

from 5 to 7 nm. As observed, there is a V_{TH} increase as the T_{Si} is reduced especially for the case of saturation bias conditions. As a consequence, there is an important variation in the DIBL value specially between the $T_{Si} = 6$ nm and the $T_{Si} = 7$ nm thick devices: $DIBL_{(@TSi=6nm)} = 130$ mV/V and $DIBL_{(@TSi=7nm)} = 210$ mV/V.

However there is a small variation (only 10 mV/V) when the channel thickness is reduced to $T_{Si} = 5$ nm: $DIBL_{(@TSi=5nm)} = 120$ mV/V. Therefore, there could be an important influence of the thickness fluctuations on the SCEs control that cannot be neglected when extremely thin film devices are used.

All these features obtained from the use of FDSOI devices combined with UTBOX + GP allow extending the use of SGSOI transistors for sub-32 nm nodes. The simulations show that 18 nm gate length devices with a channel thickness of 6 nm present good performance and excellent SCEs control. Therefore, the standard design rule which relates gate length and channel thickness can be relaxed to give an extra technological node for a given T_{Si} and delaying the aforementioned end of the scaling capabilities based on channel thickness. Following the considerations presented in Reference 2.153, the proposed design rule corresponds to $N_G \approx 1.5$, giving an idea of the extra electrostatic control obtained from the UTBOX + GP which could be represented as an additional half-gate. The main advantage of this configuration in between of single and double gate structures is the compatibility with the standard ultra-thin FDSOI fabrication flow. However, further studies are necessary in order to evaluate the impact of channel thickness variability on the performance of sub-32 nm node devices.

2.2.3.4 Multi-V_T ultra-thin body and buried oxide FDSOI platform

Multi-V_T CMOS design platforms are commonly used to continue increasing the speed of low-power (LP) applications while keeping adequate static power consumption. High-V_T (HVT) (500 mV $\leq$ HVT $\leq$ 650 mV) transistors are used in noncritical paths to keep low leakage currents, whereas standard-VT (SVT) (350 mV $\leq$ SVT $\leq$ 500 mV) and low-VT (LVT) (200 mV $\leq$ LVT $\leq$ 350 mV) transistors are used in critical paths to meet timing constraints [2.163, 2.164].

In contrast to bulk technology, V_{TH} is primarily set by the gate material work function (WF) in FDSOI devices. Therefore, setting up multi-V_{TH} devices in FDSOI technology is then very challenging. Although today, the cointegration of two gate materials has been demonstrated [2.165–2.168], cointegrating more than two gate materials prohibitively complicates the process. Researchers from LETI and STMicroelectronics have demonstrated recently that using undoped ultra-thin body and ultra-thin BOX (UTBB) devices it is possible to develop a multiple threshold voltage VT platform for digital circuits compatible with bulk CMOS. To do so, various technology options, such as gate materials, buried oxide thickness, BP doping type, and back biasing, were conveniently combined in order to achieve a technology platform that offers at least three distinct VT options (high-VT, standard-VT, and low-VT). In References 2.169 and 2.170, it has been shown that integrating a doped BP below an ultra-thin buried oxide (BOX) (<30 nm) allows setting up three distinct VT options with a single metal gate. Figure 2.51 summarizes the different BP and back bias (V_b) configurations needed to achieve three different VT values in an n-channel UTBB device.

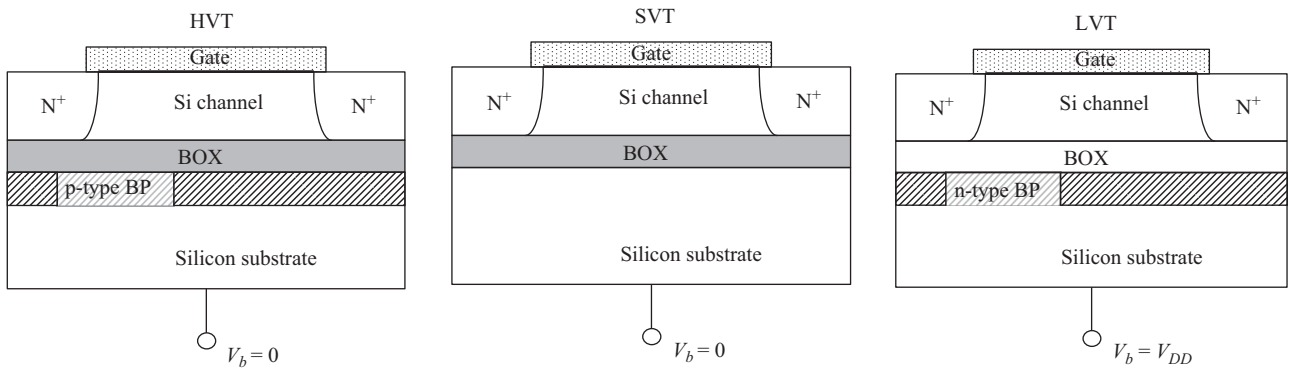

Figure 2.51 NMOS FDSOI multi-V_T devices

Table 2.3 Threshold voltages for UTBB SOI devices with different back plane (BP) and back gate (V_B) configurations

	NMOS			PMOS		
	HVT p-type BP, $V_B = 0$	SVT No BP $V_B = 0$	LVT n-type BP, $V_B = V_{DD}$	HVT n-type BP, $V_B = 0$	SVT No BP $V_B = 0$	LVT n-type BP $V_B = -V_{DD}$
V_{TH}(mV) @ $V_D = 0.1$ V	604	506	253	−427	−302	−153

1. For standard-VT (350 mV < SVT < 500 mV), no BP is necessary and the back bias is set to zero.
2. Low-VT option (200 mV < LVT <350 mV) is obtained with an n-type BP set to a back bias of $V_b = V_{DD}$.
3. High-VT option (500 mV < HVT < 650 mV) is obtained with a p-type BP biased to $V_b = 0$ V.

For p-type devices, complementary BP doping type and biasing are applied.

Using $T_{Si} = 8$ nm, $T_{BOX} = 10$ nm, and a nominal gate length of $L_G = 40$ nm, the values obtained for the threshold voltage are shown in Table 2.3 [2.171].

2.2.4 Double-gate and FinFETs

As shown in the previous section, the use of UTBB devices together with BPs/GPs and back biases allows a better electrostatic control of the channel, and therefore a better control of SCEs in ultra-thin FDSOI transistors. This fact suggests that addition of more than one gate to the transistors will enhance their performance and functionality. Several versions of multigate device are discussed extensively in the literature [2.87, 2.100, 2.93, 2.151]. There are two varieties: planar and vertical structures [2.87] (Figure 2.52). The former group contains GP and back-gate devices, which are derivatives of the SOI device [2.93]. The vertical structures contain the FinFET [2.172–2.174], the Omega FET [2.175], the Tri-Gate [2.176], the Gate-All-Around FET [2.177], and the junctionless FET [2.178].

The main difficulty with multiple-gate transistors is the realistic fabrication of such devices. Manufacturing a self-aligned double-gate MOSFET has been the goal of device engineers and researchers ever since it was proposed by Sekigawa and Hayashi in 1984 [2.179]. Different approaches for the fabrication of DGSOI transistors have been discussed since then.

(i) The planar solution (Figure 2.52a) is suitable but it does not guarantee the self-alignment of the two gates [2.180–2.182], although some advantages can still be obtained using asymmetrical and misaligned DGSOI devices [2.181].

(ii) A totally different approach is to adopt a non-planar technology. In fully vertical DG-MOSFET (Figure 2.52b), the source-body-drain stack, and therefore the current is perpendicular to the Si-wafer. These devices are attractive because the channel length (source-to-drain distance) is controlled by epitaxy, instead of lithography. They suffer, however, from the

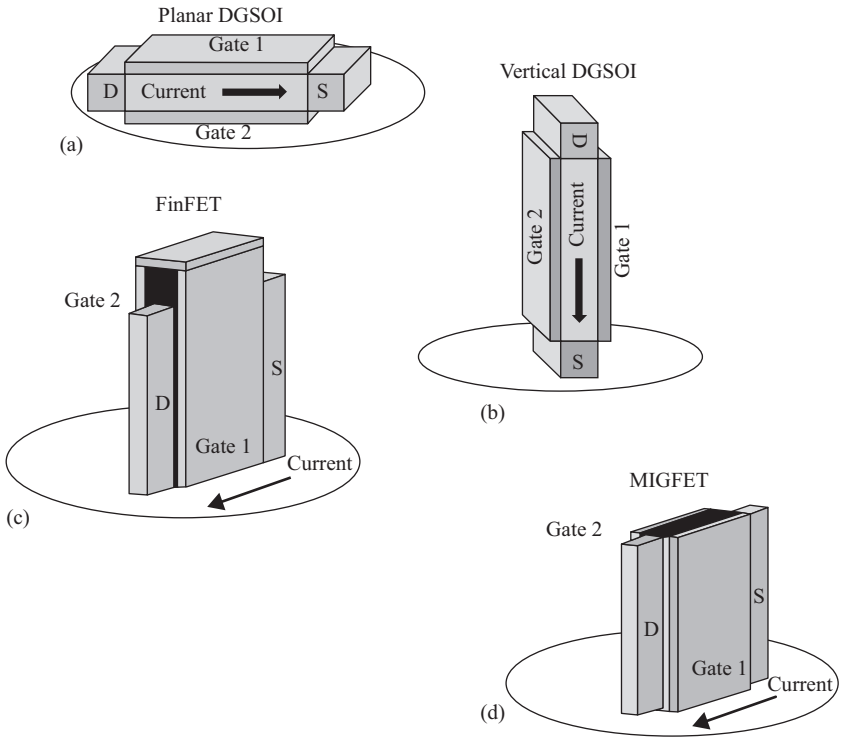

Figure 2.52 (a) Planar DGSOI (b) Vertical DGSOI (c) FinFET (d) Multiple Independent Gate FET

asymmetry of the source and drain terminals and from the difficulty of achieving tiny pillars with ultra-small integrate distances [2.183].

(iii) The third option is the FinFET. In this case, source and drain are set at both edges of the silicon fin (Figure 2.52c). The current is controlled by the two vertical gates and flows horizontally along the body sidewalls. On top of the silicon fin, a dielectric layer called "hard mask" deactivate the formation of an inversion channel at the top corners of the device. Another alternative of the FinFET is the MIGFET (Multiple Independent Gate FET). In this device, the top gate is etched, thus the lateral gates become independent, and therefore they can play different roles (Figure 2.52d).

(iv) If the top gate is made active by reducing the top dielectric layer, the device is named triple-gate MOSFET, or tri-gate MOSFET, although in fact one single gate controls three different sections of the channel: two vertical and one horizontal (Figure 2.53). The addition of the third gate improves the electrostatical integrity of the device. This electrostatical integrity can be improved still more by extending the sidewall portions of the gate electrode to some extent inside the buried oxide (Pi-Gate transistor) or/and underneath the channel region (Omega-Gate transistor). In fact, these devices will behave, from the electrostatic point of view, as having a number of gates between 3 and 4 [2.151, 2.184,–2.186].

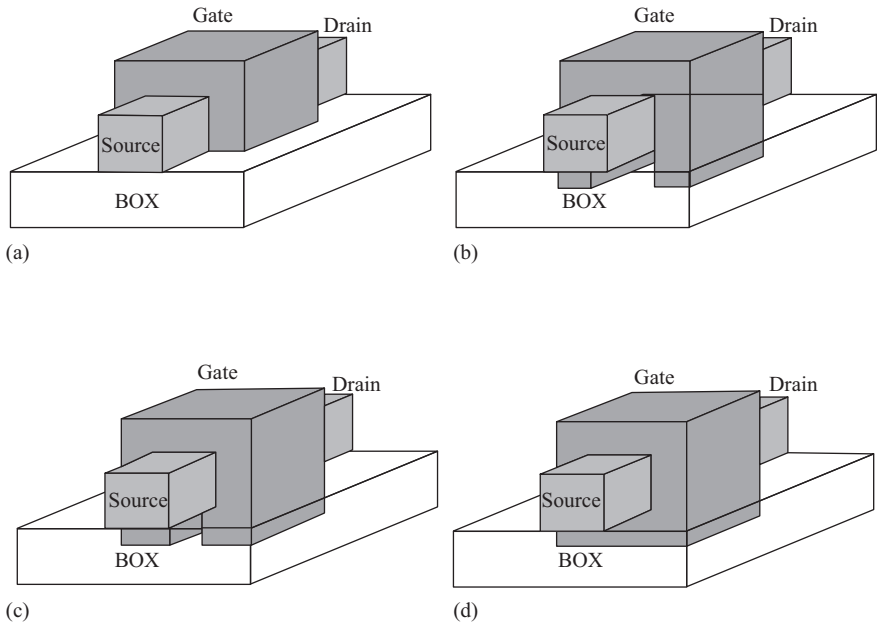

Figure 2.53 Multigate transistors. (a) Tri-gate FET, (b) Pi-gate FET, (c) Omega-gate FET, and (d) GAA-FET

(v) The device with better control of the channel region by the gate is the surrounding gate MOSFET, or Gate-all-around (GAA) MOSFET [2.187]. In these devices, the gate electrode is wrapped around all sides of the channel region.

2.2.4.1 Fabrication technology for multigate transistors

The first modern self-aligned vertical multigate MOSFET was called DELTA (DEpleted Lean channel TrAnsistor). This device was proposed by D. Hisamoto *et al*. in 1989 [2.173]. Figure 2.54 shows a cross section of the DELTA MOSFET.

The critical fabrication steps in the front-end processing of a multigate MOSFET include, sequentially: (1) fin formation, (2) gate stack formation, (3) source and drain extension implant, (4) spacer formation, (5) epitaxial raised source/drain formation, and (6) deep source/drain implantation and activation anneal. The fabrication flow of a tri-gate MOSFET on a SOI substrate is shown in Figure 2.55:

(a) The SOI silicon top layer (T_{Si}) thickness defines the fin height (FinHEIGHT).
(b) The fin pattern and the critical dimension of fin width (FinWIDTH) can be defined by optical lithography or by spacer image transfer (SIT) [2.189, 2.190], followed by plasma etching. After fin etch, the fin sidewall surfaces are rough. Therefore, oxidation and H_2 annealing are often used to smooth the sidewalls [2.191, 2.192].
(c) Next, the gate dielectric is grown and metal gate is deposited. It is suitable to tune the threshold voltage (V_{TH}) of the MOSFET by using a gate material that has the appropriate effective workfunction rather than by doping the channel,

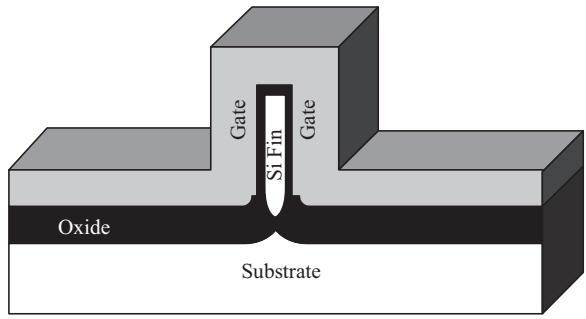

Figure 2.54 DELTA MOSFET. The oxide under the Si fin was formed through LOCOS oxidation, while the Si fin was protected by the nitride hard mask and a nitride spacer prior to the oxidation process

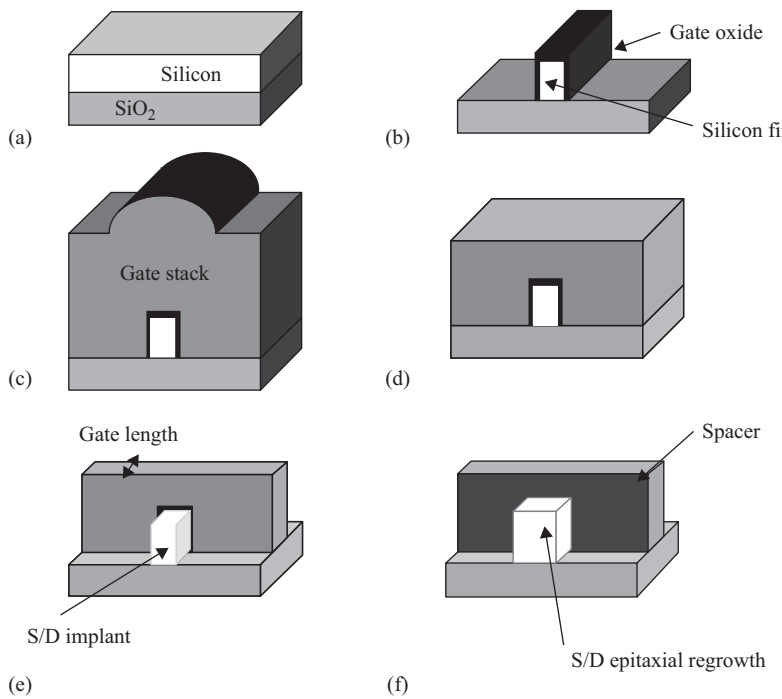

Figure 2.55 Fabrication sequence of a FinFET transistor

since as mentioned earlier, it is highly desirable to have intrinsic or lightly doped channels.

(d) Since the gate stack is over the fin topography, a planarization step is desirable to flatten the gate surface, which reduces the burden on photolithography and gate etch. Significant overetch of the gate material is required to clear the

bottom of the fins. As a result, the gate etch must have a high selectivity to the gate dielectric on top of the fin, if one wants to avoid damage to the fin during gate etch.

(e) Source and drain (S/D) extensions are formed after gate patterning using low-energy and large-tilt angled implants [2.193–2.195]. Next, S/D offset spacers are formed along the sidewalls of the gate and fin.

(f) The sidewall spacers on the fins are subsequently removed to expose the fin to grow raised source and drain using selective epitaxy [2.193–2.195]. The raised source and drain structure helps to reduce the parasitic resistance associated with thin fins [2.193].

For a complete treatment of multigate MOSFET technology, the reader can follow Reference 2.188.

2.2.4.2 Multigate transistors and short channel effects

Starting from Poisson equation, Yan and coworkers [2.196] and Lee and coworkers [2.186] introduced a powerful concept, the "natural length," λ, which is a measure of SCEs in multigate transistors. It represents the distance of penetration of the drain electric field into the channel [2.185, 2.186]. A device will be free of SCEs if the channel length is at least six times the natural length [2.186]. The natural length depends on the gate oxide thickness, the silicon film thickness, and the geometry of the gate, i.e., the number of gates. Table 2.4 summarizes the expression of λ, for different device geometries.

Suzuki *et al*. [2.198] proposed an accurate expression for the natural length in a double-gate device:

$$\lambda_2 = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}}{4\varepsilon_{Si}}\frac{t_{Si}}{t_{ox}}\right)t_{Si}t_{ox}} \tag{2.31}$$

Table 2.4 Natural length for different multigate FETs

Device	Natural length	Ref.
Single gate	$\lambda_1 = \sqrt{\frac{\varepsilon_{Si}}{1\varepsilon_{ox}}t_{Si}t_{ox}}$	[2.185]
Double gate	$\lambda_2 = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{ox}}t_{Si}t_{ox}}$	[2.186]
Triple gate	$\lambda_3 = \sqrt{\frac{\varepsilon_{Si}}{3\varepsilon_{ox}}t_{Si}t_{ox}}$	[2.186]
Surrounding gate (square cross-section)	$\lambda_4 = \sqrt{\frac{\varepsilon_{Si}}{4\varepsilon_{ox}}t_{Si}t_{ox}}$	[2.186]
Surrounding gate (circular cross-section)	$\lambda_o = \sqrt{\frac{2\varepsilon_{Si}t_{Si}^2\ln\left(1+\frac{2t_{ox}}{t_{Si}}\right)+\varepsilon_{ox}t_{Si}^2}{16\varepsilon_{ox}}}$	[2.197]

Colinge and coworkers [2.184] also introduced the concept of effective gate number, N, to generalize the expression of the natural length to an arbitrary number of gates.

$$\lambda_N = \sqrt{\frac{\varepsilon_{Si}}{N\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}}{4\varepsilon_{Si}}\frac{t_{Si}}{t_{ox}}\right)t_{Si}t_{ox}} \tag{2.32}$$

The value of N can be extracted experimentally from the dependence of threshold voltage on the silicon film thickness, which in a multigate device is given by

$$V_{TH,N} = V_{FB} + 2\phi_F + \frac{qN_A}{C_{ox}}\frac{t_{Si}}{N} \tag{2.33}$$

Thus, for a Pi-gate transistor, N takes the value of 3.14, and for an Omega-gate FET, N is between 3 and 4, depending on the penetration of the fourth gate underneath the channel [2.186].

The natural length depends on the silicon thickness, the oxide thickness, and the number of gates. Based on the "natural length" concept, Suzuki *et al*. [2.198] defined a scaling parameter, α_n, which allows one to estimate the short-channel sensitivity of devices with different gate structures.

$$\alpha_N = \frac{L_{eff}}{2\lambda_N} \tag{2.34}$$

Given a silicon thickness, t_{Si}, and oxide thickness t_{ox}, the minimum gate length avoiding SCE can be estimated imposing a value of $\alpha \approx 2.2$ [2.186].

2.2.4.3 Corner effects

Despite their benefits controlling SCEs, when multiple gate devices are considered, new coupling effects appear due to their 3D architecture. Design studies of multiple gate SOI MOSFETs have revealed that the corners of the silicon body can significantly affect their *I–V* characteristics [2.176, 2.199–2.201]. This phenomenon is commonly referred to as corner effects, and they are due to the formation of independent channels with different threshold voltages next to the corners as compared to the top or the sidewall gates. The corner components of the total current reflect a lower threshold voltage than in the rest of the device, giving rise to a higher I_{off}, which degrades the I_{on}/I_{off} ratio [2.202, 2.203]. In addition, the radius of curvature of the corners has a significant impact on the device electrical characteristics and can determine if the corner sections of the channel and the planar interfaces of the channel will have a different threshold voltage. A comprehensive study of corner effects in Pi-gate SOI transistors was performed in Reference 2.201. It was observed that the extension of corner regions has an inverse dependence on doping concentration. Thus, a reduction of doping density would help to prevent the presence of undesirable double threshold voltages. However, it has also been demonstrated that, even when highly doped substrates are used, corner effects can be suppressed as long as the device dimensions are small enough. Moreover, the influence of corner rounding and

the reduction of the gate oxide thickness were also analyzed. For these cases, the elimination of the corner effects is based on the reduction of electrostatically favorable regions and, therefore, of potential variations along the Si–oxide interface. This would avoid the possibility that different regions of the device become inverted at different gate voltages. Therefore, in accordance with these results, corner effects are not expected to play an important role in ultra-small structures. These conclusions, reached from the study of Pi-gate MOSFETs, can be extended to similar structures, such as tri-gate FETs, Ω-gate FETS, or GAA SOI MOSFETs.

2.2.4.4 Bulk FinFETs

The multigate devices described so far are fabricated on SOI wafers. However, multiple gate devices can also be made on bulk silicon wafers [2.204, 2.205]. Indeed, Intel introduced bulk FinFETs in their 22 nm CMOS technology [2.206] (Figure 2.56)

The main advantages of using bulk silicon over SOI substrates are basically two:

1. lower wafer cost, and
2. better substrate heat transfer rate.

The disadvantages seem to be much more numerous:

1. Bulk multigate FETs require for the fabrication additional isolation steps, which increase the number of steps in the fabrication process and therefore the final cost per device. Figure 2.57 compares the fabrication processes for a bulk tri-gate transistor and for a SOI tri-gate transistor (see for instance soiconsortium.org).

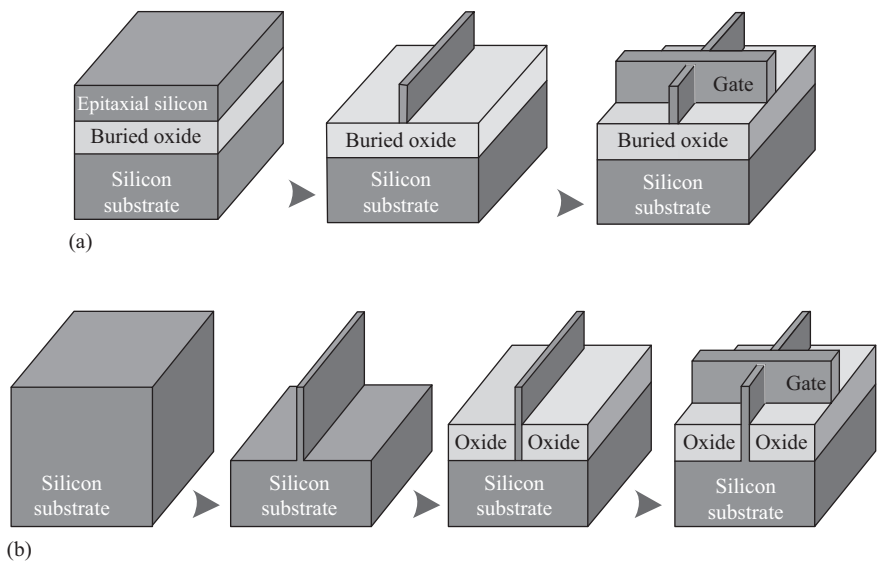

Figure 2.56 Comparison of (a) SOI FinFET and (b) bulk FinFET

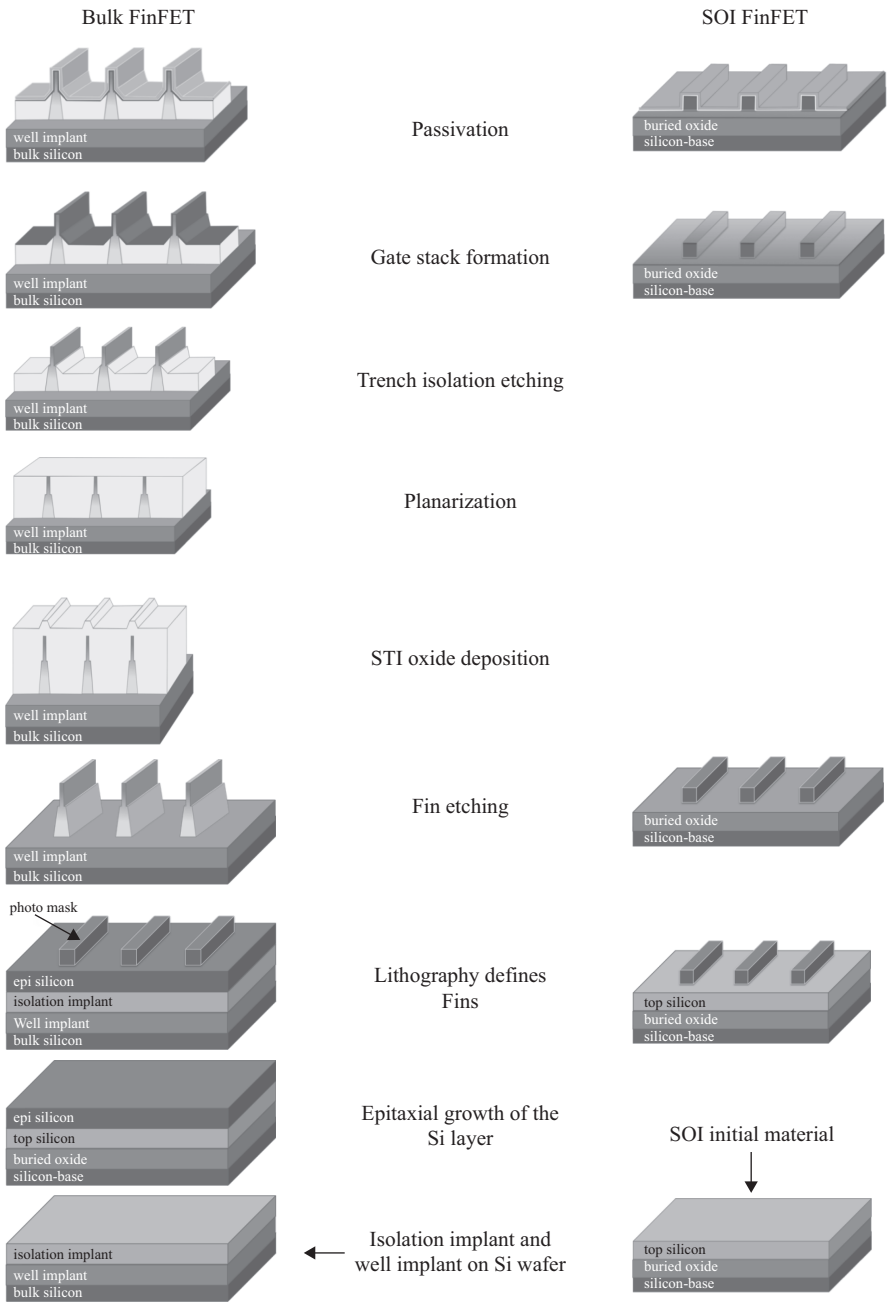

Figure 2.57 Comparison of fabrication processes for bulk and SOI multigate transistors. Adapted from soiconsortium.org

2. There are in addition some issues related to geometrical variability that are better solved in SOI FinFETs than in bulk FinFETs. The fin height in a bulk FinFET is entirely determined by the fin etch step (not by the Si layer thickness as in the case of SOI FinFET). This puts more pressure on etch variation control, since any fin height variation translates into transistor width variation.
3. Although the control of the electrostatics of the channel by the gate in bulk FinFETs is as good as in their SOI counterparts, underneath the fin, in bulk devices, the source and drain have to be separated by heavy channel stop implants to prevent sub-surface punch through.
4. The bulk silicon under the fin can be accessed by a body contact. But the body factor of a bulk FinFET is very low, since the electrostatic potential inside the fins is dominate by the gate, not by the body. Therefore, body bias is no effective in changing the threshold voltage of a multigate bulk transistor.

Asenov's group at University of Glasgow performed a comprehensive simulation study comparing the performance of bulk multigate transistors and SOI-based devices [2.84]. This study indicates that for a tri-gate FinFET, following the normal design practice, the SOI device can introduce more than 6% performance and I_{on}/I_{off} ratio advantage compared to bulk FinFET, or can provide more than two times reduction in leakage current at the same drive current. This is thanks to the BOX isolation compared to the junction isolation which depletes the bottom part of the bulk fin. For a DG FinFET, the advantage of SOI FinFET over its bulk counterpart will be more pronounced: over 10% improvement on drive current and I_{on}/I_{off} ratio can be expected in SOI architecture for devices with the same leakage current, and more than five times reduction of leakage current in SOI can be achieved if both devices have the same drive current.

Although SOI FinFETs have slightly worse SCEs compared to bulk FinFETs, to some extent it can be mitigated by BOX and substrate doping optimization. SOI technology can efficiently help to reduce the process-induced FinFET variability. In SOI FinFETs, there is no obvious degradation on statistical variability performance compared to bulk FinFETs that have the best possible RDD performance. Considering the larger process variation associated with the fin formation in bulk technology, the SOI FinFETs can have better overall variability performance compared to bulk FinFETs.

For a comprehensive discussion about bulk Si versus SOI FinFETs, the reader can follow the work by Fossum *et al*. [2.85].

2.2.4.5 Quantum effects in quantum-well-based multigate transistors

The thickness and/or width of the multigate transistors have to be reduced to values below 10 nm in order to control SCEs as discussed previously. Under these conditions, the carriers in the channel become quantized in one dimension (in quantum-well-based devices, as DGSOI and FinFETs) or even in two dimensions (in quantum wire-based devices as tri-gate, four-gate, or GAA devices). This results in the formation of energy subbands and in electron distributions in the silicon film

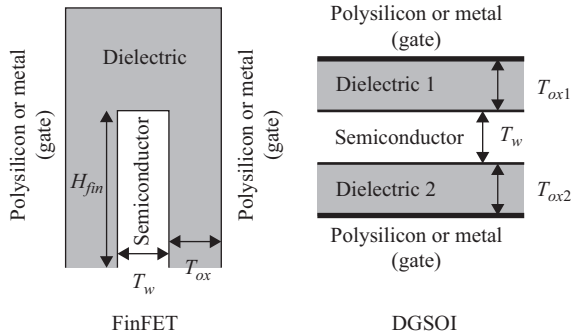

Figure 2.58 Schematic representation of a FinFET (left) and a Double-Gate transistor (right)

that can be significantly different from what is predicted by the classical theory. The confinement of carriers is responsible for different behavior of carrier mobility and threshold voltage.

We will start analyzing quantum effects and electron mobility in quantum-well-based devices, i.e., those devices as planar DGSOI and FinFETs in which carriers are confined only in the direction perpendicular to both gates (2DEG). We will consider the case of quantum wire based devices (1DEG) in a next section of this chapter.

In a planar DGSOI structure the silicon slab is sandwiched between two oxide layers. A metal or a polysilicon film contacts each oxide (Figure 2.58). Each of these films acts as a gate electrode (front and back gate), which can generate an inversion region near the $Si–SiO_2$ interfaces if an appropriate bias is applied. Thus, we would have two MOSFETs sharing the substrate, source and drain. The outstanding feature of these structures lies in the concept of *volume inversion*, introduced by Balestra *et al*. [2.206] if the Si film is thicker than the sum of the depletion regions induced by the two gates, no interaction is produced between the two inversion layers. The operation of this device is similar to that of two conventional MOSFETs connected in parallel (Figure 2.59b).

However, if the Si thickness is reduced, the whole silicon film is depleted and an important interaction occurs between the two potential wells. In such conditions the inversion layer is formed not only at the top and bottom of the silicon slab (i.e., near the two silicon–oxide interfaces) but throughout the entire silicon film thickness. It is then said that the device operates in "*volume inversion*," i.e., carriers are no longer confined at one interface, but distributed throughout the entire silicon volume (Figure 2.59a).

Several authors have claimed that *volume inversion* presents a significant number of advantages, such as: (i) enhancement of the number of minority carriers; (ii) increase in carrier mobility and velocity due to the reduced influence of scattering associated with oxide and interface charges and surface roughness; (iii) as a consequence of the latter, an increase in drain current and transconductance; (iv) a decrease in low-frequency noise; and (v) a large reduction in hot carrier effects [2.206].

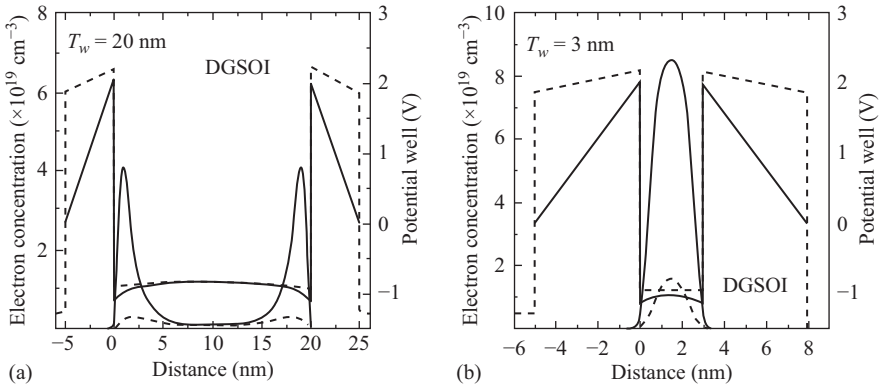

Figure 2.59 Electron distribution and potential well for two DGSOI devices with different silicon-layer thicknesses and (a) and (b) two values of the inversion charge concentration. Dashed lines correspond to $N_{inv} = 1 \times 10^{12}$ cm^{-2}, and solid lines correspond to $N_{inv} = 8 \times 10^{12}$ cm^{-2}

To evaluate accurately the electron distribution in a DGSOI structure we must self-consistently solve the Schrödinger and Poisson equations [2.146, 2.208–2.211]. Figure 2.59 shows the potential distribution in the structure and the electron concentration for two silicon thicknesses $T_{Si} = 20$ nm (a) and $T_{Si} = 3$ nm (b) and for two electron concentrations (solid line: $N_{inv} = 1 \times 10^{12}$ cm^{-2}; and dashed line: $N_{inv} = 8 \times 10^{12}$ cm^{-2}). In this case, N_{inv} is defined as

$$N_{inv} = \int_0^{\frac{t_{Si}}{2}} n(x)dx \tag{2.35}$$

where $n(x)$ is the electron distribution.

From the self-consistent solution of the Poisson and Schrodinger equations, the following conclusion can be drawn:

1. As in ultra-thin FDSOI discussed earlier, the subband modulation effect is an important effect caused by the reduction of the silicon film thickness [2.210, 2.211]. This effect is related to the redistribution of the carriers among the different electric subbands originated by the size quantization. The direct consequence of a decrease of the conduction effective mass as the silicon thickness decreases. Although the picture in DGSOI devices is slightly more complicated than that observed in FDSOI structures, Figure 2.60a shows that, also in DGSOI devices, the average conduction effective mass decreases as the silicon layer thickness is reduced.
2. Another important quantum effect that appears in ultra-thin FDSOI inversion as silicon thickness decreases is an increase of the phonon-scattering rate, i.e., the uncertainty in the location of the electrons in the direction perpendicular to

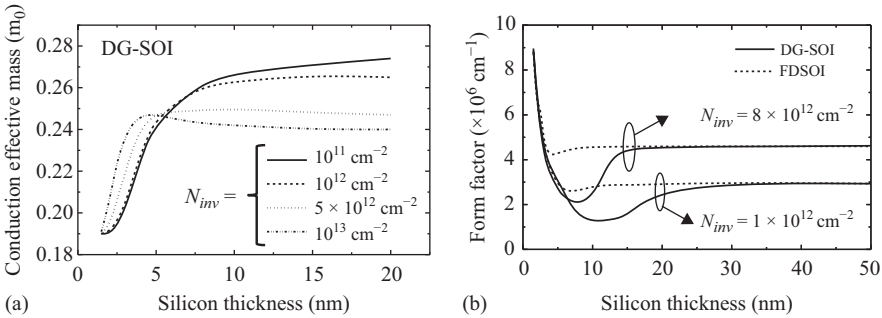

Figure 2.60 (a) Evolution of the average conduction effective mass with the silicon slab thickness, for different inversion charge concentrations. (b) Evolution of phonon-scattering rate for the ground subband as a function of the silicon thickness for two values of the inversion charge concentration. Solid line: for a DGSOI inversion layer; dashed line: for an ultra-thin FDSOI inversion layer

the interface is lower as T_{Si} decreases. By the uncertainty principle, there is a wider distribution of the electron's momentum perpendicular to the interface. In other words, due to size quantization, the electron's interface-directed momentum does not have a single value (as in three-dimensional electrons), but rather a distribution of likely values that expands as the silicon layer thickness is reduced. Taking into account momentum conservation, there are more phonons available that can assist the transitions between electronic states, and therefore the phonon-scattering increases. Thus for the same inversion charge concentration, the phonon-scattering rate is greater in thinner films than in thicker ones (since the confinement is greater), and therefore we expect a reduction of the mobility. Phonon-scattering rate is proportional to the form factor displayed in Figure 2.60b. The form factor corresponding to ultra-thin FDSOI inversion layers is also shown (dashed line). For thinner samples the form factor is very large due to the geometrical confinement of electrons in a very narrow space (no differences are observed between DGSOI and FDSOI). As the silicon slab thickness increases, the form factor is quickly reduced, until a minimum is reached in the region between 5 and 15 nm. Then, it increases to approach, for thick samples ($T_{Si} \sim 20$ nm), the value presented in ultra-thin FDSOI inversion layers and in bulk inversion layers. As can be seen in the figure, in the range $T_{Si} = 5$–15 nm the phonon-scattering rate for DGSOI is lower than the one corresponding to FDSOI for the same thicknesses, and even lower than the one corresponding to bulk inversion layers. Consequently, in intermediate ranges of the silicon thickness (which depend on the inversion charge concentration) the phonon-scattering rate in the DGSOI inversion layer decreases, instead of increasing as expected. This is an important result, a direct consequence of the volume inversion effect. This fact is important in explaining the behavior of the transport properties.

2.2.4.6 Electron mobility in quantum-well-based transistors

Phonon scattering is not the only scattering mechanism present in multigate devices. Although other scattering mechanisms (namely, those associated with the Coulomb interaction with oxide and interface charges and with the roughness of the silicon–oxide interfaces) are likely to be weakened by a volume inversion operation [2.212–2.216], their contribution has to be taken into account. The weakness of these scattering mechanisms is justified, at least a priori, by the spread of the electrons throughout the whole silicon region. Nevertheless, we must not forget that in order to achieve volume inversion, both channels must interact strongly, and this only happens in the medium-high transverse electric field range when the silicon slab between the two oxides is thin enough (below 20 nm as pointed out by [2.144, 2.212–2.216]). In these thin devices, although electrons are certainly spread along the whole silicon layer, they may not be far enough from the interfaces and may therefore be significantly affected by surface scattering mechanisms; much more so, in fact, than in bulk MOSFETs, since they are now interacting with two interfaces. This means that scattering mechanisms may play a very important role in the electron mobility in ultra-thin DGMOSFETs, contrary to what was previously believed. This imposes a serious limitation on the minimum silicon thicknesses that can be used in these devices, in addition to the limitations already presented by other physical and technological issues, as detailed elsewhere [2.208, 2.212].

Using a one-electron MC method the stationary electron transport properties in DGSOI and FinFET inversion layers have been evaluated. Electron quantization in the inversion layer was taken into account in an appropriate manner, self-consistently solving Poisson's and Schrödinger's equations assuming a simple non-parabolic band model for the silicon. Once the electron distribution in the silicon layer was determined, the Boltzmann transport equation was solved by the MC method, simultaneously taking into account phonon, surface-roughness, and Coulomb scattering. To do this, it was necessary to improve on existing scattering models. The presence of two close silicon–oxide interfaces in a DGMOSFET makes it significantly different from its standard-bulk counterparts. Figure 2.61 shows the total electron mobility for two values of the total inversion charge as a function of the silicon thickness in a planar DGSOI transistor. For the sake of comparison, the electron mobility in an ultra-thin FDSOI transistor with the same parameters is also shown.

Figure 2.61 reveals the existence of three regions with different behavior in the DGSOI electron mobility:

(i) The first region corresponds to thick silicon slabs. In DGSOI inversion layers the two channels are sufficiently separated and no interaction appears between them. This situation corresponds to two conventional inversion layers in parallel, separated by a large potential barrier. The behavior of electrons in each of these inversion layers is the same as that observed in a bulk silicon inversion layer. As the silicon thickness is reduced, the interaction between the two inversion layers causes the electrons to occupy the entire silicon volume. This is the beginning of the second region, which

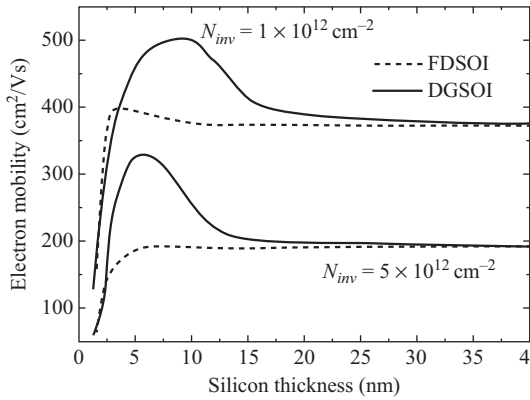

Figure 2.61 Evolution of electron mobility in DGSOI and FDSOI with the silicon thickness

strongly depends on the value of the transverse effective field, since for high electric fields a potential barrier, which obstructs the mutual influence of the two channels, is formed in the middle of the silicon slab.

(ii) In the second region, the electron mobility in DGSOI inversion layers is up to 20% larger than the mobility in FDSOI inversion layers. The limits of this region and the values of the mobility depend on the inversion charge concentration. This is the region in which volume inversion occurs. In this region of silicon thickness, both subband energy levels and wave functions vary significantly as a consequence of the two channels interacting. It is for this reason that the phonon-scattering rate decreases [2.146] compared to its value in conventional bulk. This happens down to a certain value of silicon thickness. For lower thicknesses, although the electrons are distributed throughout the entire silicon layer, their confinement is greater (due to the geometrical confinement), and therefore, the phonon-scattering rate increases, as shown in Figure 2.61. This marks the beginning of the third region.

(iii) In the third and last region ($t_{Si} < 4$ nm), the mobility for DGSOI falls abruptly. In this zone, mobility is limited by the thickness of the silicon slab, and therefore electron mobility falls abruptly.

For a complete and comprehensive study of the electron mobility in multigate devices, the reader can follow Reference 2.217.

2.2.5 Silicon multigate nanowires

Multiple-gate FETs provide a good electrostatic control of the channel and therefore the possibility of a higher reduction of the channel length compared to traditional bulk MOSFETs. It has been demonstrated that for DGSOI transistors to operate correctly is necessary silicon thicknesses t_{Si} lower than half of the channel length $L_{ch}/2$. The use of several gates can relax this condition without degradation

of the device performance. Therefore, since the characteristic dimensions for the next node generations is well below 100 nm, the silicon fin cross-section will reach the nanometer scale, confining the carriers in the two directions perpendicular to the transport one. As a consequence, the 2D electron gas is transformed in a 1D one. The density of states experiences an important transformation due to their different energy dependence. Under these circumstances, it has been experimentally observed a change of fundamental electrical parameters such as the threshold voltage [2.218].

The need to scale the active channel region below 30 nm requires a silicon body width and thickness of the same dimensions or even lower in order to maintain an acceptable gate electrostatic control of the channel potential. For these reduced dimensions, carriers are confined in the directions perpendicular to the transport, such devices being called NWs. The potential application of semiconductor NW field- FETs as potential building blocks for highly downscaled electronic devices with superior performance is attracting considerable attention [2.219, 2.220].

With regard to their manufacturing process, it is possible to establish two different approaches, bottom-up and top-down:

(i) The bottom-up approach refers to the methodology that employs chemistry to promote the self-assembly of complex mesoscopic architectures. One of the most important discoveries in recent years has been the growth of single-crystal nanostructured materials at low temperatures using different nanometer-sized metallic nanoparticles (e.g., Ni, Au, Fe) as catalysts [2.221]. A wide variety of semiconductor materials such as Si, Ge, GaAs, GaN, and InP can be synthesized employing this technique [2.222, 2.223]. Different applications, such as laser action, photoluminescence, sensing, p-n junction, and FETs, have already been demonstrated. Currently, the FETs fabricated from Vapor-Liquid-Solid (VLS) grown NWs may offer better size uniformity than etching for very small diameters (<5 nm) due to controlled chemical synthesis.

(ii) The top-down approach refers to those devices with dimensions in the nanometer range, fabricated using the standard techniques employed for CMOS processing, namely, photolithography, thin-film deposition, etching, and metallization, to obtain multigate SOI FETs with very small dimensions [2.224, 2.225].

As has been established previously in this chapter, Multiple-Gate SOI MOSFETs are considered an attractive alternative to traditional bulk MOSFETs since they have proved to give better electrostatic control of the channel, allowing a greater reduction of the channel length (L_g) while the SCEs are kept under control. Moreover, the use of two, three, or even four gates allows a relaxation of the width (W_{Si}) and height (H_{Si}) of the silicon fin compared with L_g. When the dimensions of the semiconductor fin, W_{Si} and H_{Si} (see Figure 2.62), reach the nanometer scale, the carriers are confined in two dimensions, in the plane perpendicular to the transport direction. Therefore, the bulk crystal symmetry is not preserved and fundamental magnitudes, such as the density of states, and the band structure, experience

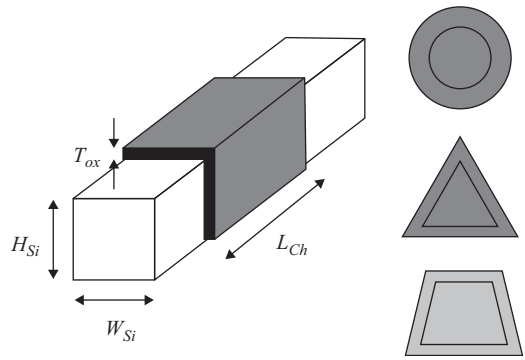

Figure 2.62 Representation of a SiNW where W_{Si} and H_{Si} represent the semiconductor fin width and height respectively, L_g the gate length, and T_{ox} the gate oxide thickness. Different cross-sections, such as triangular, circular, or trapezoidal can be considered in addition to the rectangular one

important modifications, which will influence the carrier transport properties of these new devices.

2.2.5.1 Quantum effects in Si nanowires

It has been demonstrated that band structure effects begin to manifest in silicon NWs with diameters below 5 nm. For higher dimensions, the simple parabolic effective-mass approach with bulk effective-masses is the optimum solution due to its reduced computational cost. Moreover, with very small dimensions (<5 nm) this method can be still used when appropriate tuning parameters are employed [2.226]. Therefore, the modified semiconductor band structure should be taken into account when the device dimensions are below the limit of 5 nm since other important parameters, such as the threshold voltage and the gate-channel capacitance, suffer considerable modifications [2.227]. In order to understand in depth the transport properties of these one-dimensional (1D) devices, detailed knowledge of the electron density and the electrostatic potential is necessary. Obviously this requires the solution of the Poisson equation. Two different approximations can be carried out to achieve this goal. On the one hand, whether or not the whole device is considered, the solution of the three-dimensional (3D) Poisson equation for the electrostatic potential has to be carried out [2.228–2.230].

On the other hand, if a very long device is considered, this equation can be restricted to a plane perpendicular to the transport direction and the influence of the source and drain contacts neglected. In this case, a 2D Poisson equation must be solved:

$$\nabla(\varepsilon\nabla\phi) = -q\left(p - n + N_D^+ - N_A^-\right) \tag{2.36}$$

where ϕ is the electrostatic potential, ε is the dielectric constant, q is the electric unit, n and p are the electron and hole concentrations, and $N_D{}^+$ and $N_A{}^-$ are the ionized donor and acceptor concentrations. Use of the finite element method allows

the simulation of different geometries, such as triangular, cylindrical, or rectangular cross-sections. Due to the reduced dimensions of the devices under study, it is mandatory to include the quantum effects in the simulation, through the self-consistent solution of the Schrödinger equation. The most common approximation is the solution of the equation in two dimensions in the channel cross-section. If the whole device is studied, this solution is carried out in an arbitrary number of slices along the device length and then coupled with the corresponding transport equation [2.228, 2.229].

It can be assumed that confinement is produced in the *y*- and *z*-directions and transport in the *x*-direction and, as a first approximation, the effect of source and drain contacts can be neglected. Therefore, the 2D Schrödinger equation can be written as

$$-\frac{\hbar^2}{2}\frac{\partial}{\partial y}\left(\frac{1}{m_y}\frac{\partial \Psi_v}{\partial y}\right)-\frac{\hbar^2}{2}\frac{\partial}{\partial z}\left(\frac{1}{m_z}\frac{\partial \Psi_v}{\partial z}\right)+V(y,z)\Psi_v=E_v\Psi_v \tag{2.37}$$

where m_y and m_z are the effective electron masses along the *y*- and *z*-axis, respectively, and Ψ_v the wave function belonging to energy level E_v.

In order to self-consistently solve the two equations, different algorithms can be employed. However, the predictor-corrector scheme proposed by Trellakis *et al*. [2.231] has been tested by several authors [2.232, 2.233] on different semiconductor structures with excellent results in every case. In order to show the correct operation of the above procedure, it has been applied to a silicon Gate All-Around (GAA) MOSFET, where the semiconductor is completely surrounded by the insulator and the gate contact. In all the calculations, we assumed a square cross-section ($W_{Si} = H_{Si}$), substrate doping of 10^{15} cm^{-3}, $T_{ox} = 1$ nm, and a midgap workfunction metal gate ($\phi_m = 4.61$ eV).

Figure 2.63a,c represents the electron distribution in a silicon GAA with $W_{Si} = H_{Si} = 15$ nm while Figure 2.63b corresponds to a 4 nm lateral size. Figure 2.63d was calculated using a classical solution of the structure and an applied gate voltage (V_G) equal to 1 V. The maximum electron density is located at the Si–SiO_2 interface, right in the corners, and its value is clearly overestimated when compared with the corresponding quantum simulation shown in Figure 2.63c. Figure 2.63a was calculated for the same device shown in Figure 2.63c but with a gate voltage reduced to 0.25 V. It shows how the electrons are spread throughout the whole silicon body with a peak density at the centre of the structure due to the so-called volume inversion effect [2.207]. Figure 2.63b corresponds to a device with reduced silicon fin dimensions ($W_{Si} = H_{Si} = 4$ nm) and shows that for the same gate voltage as Figure 2.63c ($V_G = 1$ V), the maxima of the electron density are again located at the center of the semiconductor due to the volume inversion effect.

2.2.5.2 Electron transport in Si nanowires

The electron transport properties in Si NWs can be studied from different approximations such as the Kubo-Greenwood formula [2.234, 2.235] modified for 1D transport, the nonequilibrium Green's function (NEGF) formalism [2.236, 2.237] or an MC simulation where the quantum effects have been taken into account

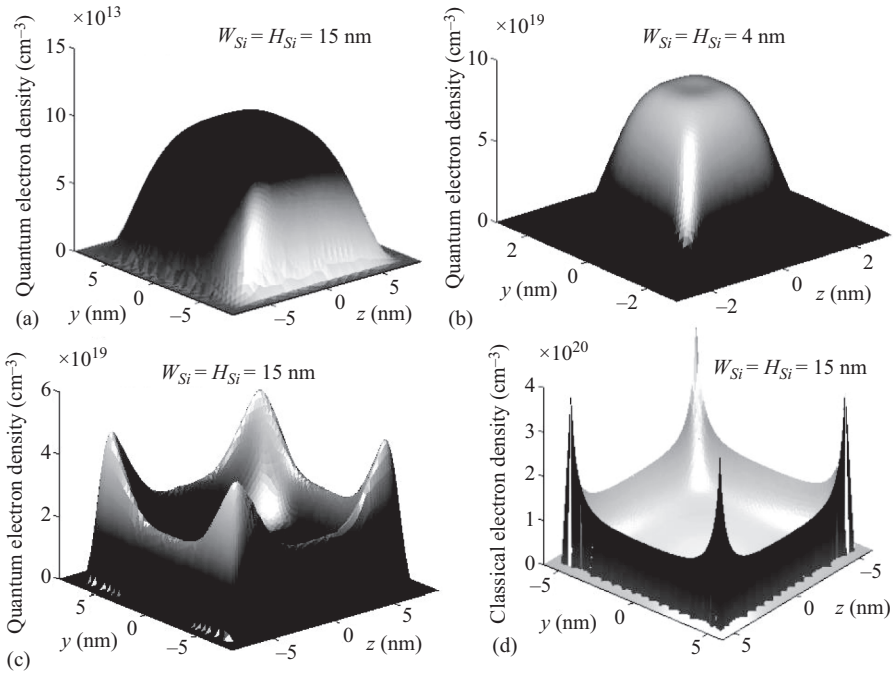

Figure 2.63 (a)–(c) Calculated quantum electron distributions in a silicon GAA nanowire with $W_{Si} = H_{Si} = 15$ nm (a) and (c), and $W_{Si} = H_{Si} = 4$ nm (b). (d) Calculated classical electron distribution in a silicon GAA nanowire with $W_{Si} = H_{Si} = 15$ nm and the same gate bias as (c)

[2.238, 2.239]. The MC procedure has been quite popular in recent decades and the scattering models have been tested in a large number of semiconductor structures [2.240]. However, the MC algorithm normally used to calculate the electron transport properties in silicon inversion layers has to be modified to take into account the special characteristics of carrier confinement in two dimensions. Among the different scattering mechanisms, which can influence carrier mobility in a SiNW, it has been demonstrated that phonon scattering is the dominant mechanism in mobility degradation in a Si MOSFET under operating conditions at room temperature. Therefore, phonon mobility is dominant in low effective fields and its value is determined by the acoustic and intervalley scattering rates. The results obtained from MC simulation are shown in Figure 2.64 where the calculated values of phonon-limited mobility are depicted as a function of the gate voltage for three different values of the square cross-section ($W_{Si} = H_{Si} = 15$ nm; 10 nm; 5 nm). As can be observed, phonon-limited mobility is quite similar for the larger cross-sections (15 and 10 nm of lateral size). However, if the silicon fin is reduced to 5 nm, a significant degradation is found [2.239, 2.241].

Electron mobility in multigate NWs based in III–V materials have been widely studied in References 2.242–2.246.

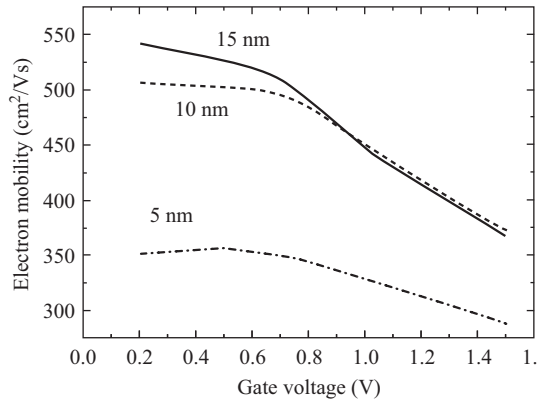

Figure 2.64 Phonon-limited electron mobility in a silicon GAA as a function of the gate voltage. Three different cross-sections are considered ($W_{Si} = H_{Si}$), 15 nm, 10 nm, and 5 nm

Different research groups are currently working on the manufacture and characterization of Si NWs and a wide variety of experimental results have been presented. As an example, we could mention the studies published by Lieber's group [2.247, 2.248], which have shown that the average transconductance and mobility show substantial advantages for SiNWs obtained from vapour-liquid-solid (VLS) synthesis compared with more conventional multigate FETs. However, a number of issues including device performance, reproducibility, and high-quality ohmic contacts must be addressed if such systems are to be implemented in the future. More recently, electron mobility as high as ≈1,000 cm^2/Vs has been reported for n-channel SiNW FETs made following conventional semiconductor manufacturing techniques, from a p-type SOI wafer with n^+ source and drain. Moreover, the authors of this work conclude that as the channel width decreases, the inversion layer mobility of the SiNW increases to approximately twice the mobility of the larger channel-width FETs [2.249].

Singh *et al*. [2.225] reported the fabrication of GAA n- and p-FETs on a SOI wafer with a diameter smaller than 5 nm and lengths around 1,000 nm where the estimated electron and hole mobilities are ∼750 and ∼325 cm^2/Vs at high fields. These experimental results cover a wide range of mobility values and, to date, a clear explanation is not available for all of them. Various reasons have been put forward to justify these discrepancies, such as strain in the semiconductor due to the oxidation process or the possible suppression of intervalley phonon scattering, volume inversion, and reduced surface roughness at high fields [2.225].

The unique properties observed in 1D electron gases can be appreciated only when lateral dimensions are well below 10 nm since otherwise their behavior much more closely resembles that found in traditional silicon inversion layers. This conclusion can be relaxed when very low temperatures are applied, as was demonstrated by Colinge *et al*. [2.250].

2.2.6 Junctionless transistors

All the devices presented so far along this chapter are based on the formation of junctions. Junctions are capable of both blocking current and allowing it to flow, depending on an applied bias. For example, the MOSFET transistors are made using two p–n junctions: the source junction and the drain junction. Therefore, an n-channel MOSFET transistor is an N-P-N structure, while a p-channel transistor is a P-N-P structure. As detailed in previous sections, trends in the electronic industry require smaller and smaller components resulting in transistor sizes down to the nanoscale. This is starting to pose significant manufacturing problems. In classical very small transistors one has to form two junctions, since source and drain regions are separated by channel area with opposite doping polarity. The diffusion of source and drain doping atoms is difficult to control in very short-channel transistors. In all transistors, the scattering and diffusion of source and drain impurities into the channel region becomes a bottleneck to the fabrication of very short channel devices, and very low thermal budget processing techniques must be used [2.251]. Very costly techniques are used to minimize this diffusion, but even in the absence of diffusion the statistical variation of the impurity concentration due to ion implantation or other doping techniques can cause device parameter variation problems. To overcome these problems, in 2010 J. P. Colinge proposed [2.252] the junctionless transistors (JNTs). These devices are fabricated without source and drain formation process, as the doping type and concentration in the channel region is essentially equal to that in the source and drain, or at least to that in the source and drain extensions [2.253–2.255]. A JNT is basically an FD accumulation-mode device, consisting of a heavily doped SOI NW resistor with an MOS gate to control current flow. Doping concentration is constant and uniform throughout the device and typically ranges from 10^{18} and $10^{20}\,\mathrm{cm}^{-3}$. The JNT device can be tuned to normal-off state when the gate workfunction is properly chosen and the highly doped channel can be FD with no gate bias. As gate voltage is increased, the JNT enters into partially depletion state, and current conducts in the centre of the NW when V_D is supplied, and then at flatband voltage, the depletion region is completely gone. The accumulation starts at the NW surface when further raises the V_G, which additionally offers an accumulation current, in spite of the bulk current.

Figure 2.65 shows calculated I_D–V_G curves for a cylindrical GAA JNT with a gate length of $L_{ch} = 20$ nm and a radius, $R_i = 3$ nm. Doping concentration was set to $N_D = 8 \times 10^{19}\,\mathrm{cm}^{-3}$. The metal gate was assumed to have a workfunction of 5.5 eV and the oxide thickness is set to $t_{ox} = 2$ nm. The curves were calculated by self-consistently solving Poisson equation and drift-diffusion and continuity equations. In this device, the subthreshold slope results to be $S = 70$ mV/dec.

In subthreshold operation ($V_G = -0.2$ V in Figure 2.66), the silicon is FD. Threshold voltage is reached when a portion of the silicon becomes neutral. At that point the device is PD. The bulk current flows in this neutral channel (that is not depleted silicon). Therefore carriers in a JNT transistors see a zero electric field in the directions perpendicular to the current flow. This is a big difference with inversion mode GAA or tri-gate transistors. As gate voltage increases, depletion decreases and the diameter of the neutral channel increases. When the gate voltage reaches flatband

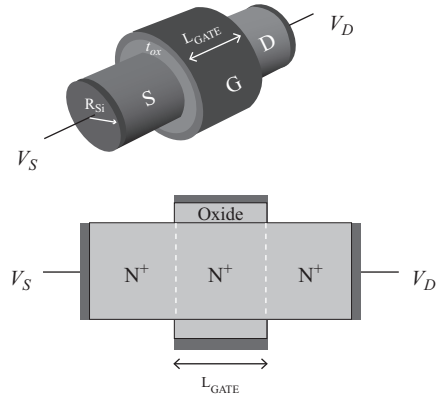

Figure 2.65 Schematics of a cylindrical GAA junctionless nanowire

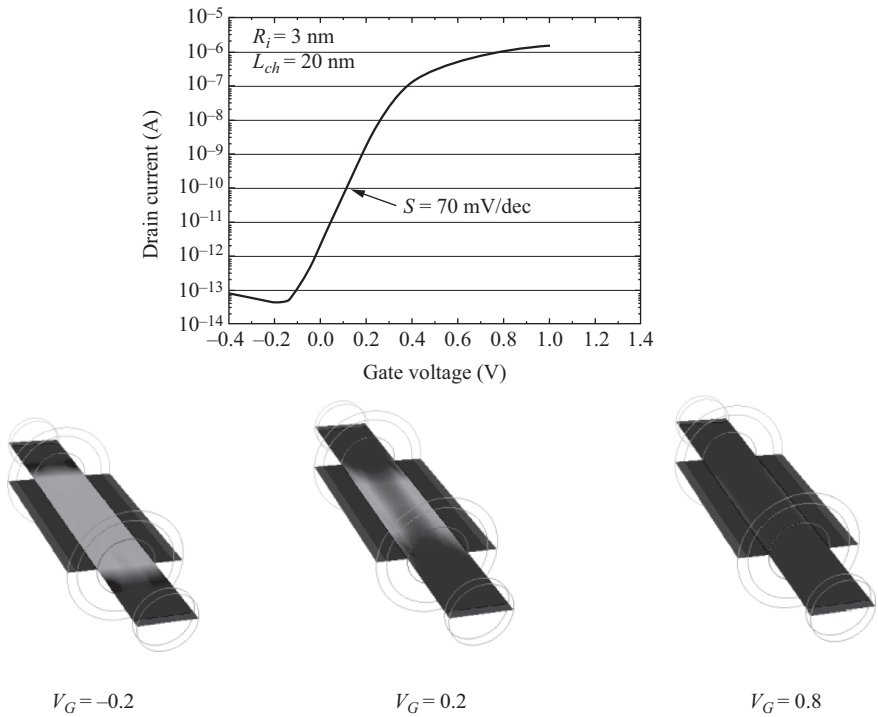

Figure 2.66 I_D–V_G curve for a cylindrical junctionless transistor. $V_{DS} = 50$ mV. Electron concentration contour plots for different gate voltage V_G. $V_G = -0.2$ V (below threshold): the channel is completely depleted of electrons; $V_G = 0.2$ V: the channel starts to be populated with electrons and the current starts to increase; $V_G = 0.8$ V (above threshold): the channel is almost completely populated with electrons

voltage the entire channel region becomes neutral (assuming low V_{DS}). Further increasing the gate voltage brings about the formation of an accumulation layer.

In conclusion, JNTs are unipolar, thin-film, heavily doped (typically in the 10^{19} cm^{-3} range) MOS transistors. Because of its simple design, the JNT architecture has been adapted to semiconductor materials other than silicon. In the off-state the channel is FD owing to the workfunction difference between the semiconductor and the gate material. When the device is turned on, a substantial part of the current is carried in the bulk of the thin film, and is usually augmented by an accumulation current contribution. JNTs are characterized by reduced SCEs and present excellent subthreshold slope and low DIBL [2.256]. As a result, CMOS junctionless devices with outstanding short-channel characteristics have been demonstrated for gate lengths down to 13 nm. The JNT is probably the most scalable of all FET structures, as demonstrated by both ab initio simulations and experimental devices with gate lengths as small as 3 nm.

2.2.7 Tunnel field-effect transistor

Tunnel Field-Effect Transistors (TFETs) are one of the most promising devices to replace conventional MOSFETs. Their low off-current and steeper subthreshold slope overcoming the 60 mV/dec limit of MOS transistors, make them enormously attractive for low-power applications. One of the main problems arising in MOSFETs is that when they are scaled down, so as to do their power supply voltage in order to reduce power density. The subthreshold swing limit of 60 mV/dec present in conventional MOSFETs, imposes a severe roadblock to reduce the supply voltage plateau of 1 V and maintain high ON-state currents along with low OFF-state leakages. TFETs, on the other hand, are based in the so-called BTBT mechanism which makes the carrier injection into the channel essentially dependent on the quantum process of tunneling across an energy barrier. This fact allows extremely low subthreshold swings when the device turns on due to the quasi-exponential dependence of the current on the barrier width. Likewise, when the transistor is off, the tunneling barrier keeps the leakage current extremely low. In MOSFET scaling, tunneling phenomena from heavily doped junctions resulted in parasitic leakage currents. However, as this process is precisely the working principle of TFETs, it is no longer an unwanted parasitic effect. Furthermore, since tunneling only takes place in a very small region of these devices, this may allow significant gate scaling up to the distance of BTBT which in silicon represents less than 10 nm. As source-to-drain DT is negligible for channel lengths greater than that value [2.257], TFETs could in principle be scaled to very small dimensions without relevant leakage current degradation.

Since the discovery of BTBT in 1957 by Esaki [2.258] when studying very narrow germanium p–n junctions, this phenomenon based on the tunneling injection of carriers from occupied states in the valence (conduction) band to empty states in the conduction (valence) band has been demonstrated in many devices. As indicated earlier, such a mechanism has been shown, for example, in MOSFETs (both lateral and vertical). The first gated p-i-n structure was proposed in 1978 at Brown University [2.259] suggesting it for spectroscopy. Transistors based on it (like

B2T–MOSFETs [2.260] or others replacing the i-region under the gate by a p^--region [2.261]) were investigated, showing the lack of V_{TH} roll-off and temperature dependence of the device characteristics when scaling. However, the first gated p-i-n diodes operating as Surface Tunnel Transistors were proposed on III–V compounds [2.262]. Similar tunneling transistor operation was developed in silicon at Cambridge [2.263], and later at Toshiba [2.264]. The interest of these first results was limited until the experimental results presented in 2000 by W. Hansch and I. Eisele on vertical p-i-n diodes [2.265–2.267]. In 2004, a lateral gated p–n junction diode (without intrinsic region) on silicon-on-insulator was fabricated [2.268] at Brown University. In this last case, the lack of intrinsic region reduced gate capacitance but did not significantly improved ON-current – which was still very low – and also produced an increase in leakage current. Also in 2004, Appenzeller *et al*. [2.269] reported for the first time a subthreshold swing under 60 mV/dec in carbon nanotube FETs (CNFET). A back gate and a top gate were employed to achieve the necessary band configuration to trigger BTBT. In 2005, the same authors [2.270] compared several CNFETs concluding that the single gate configuration presented the best performance. Despite the obtained results for CNFETs, the research on silicon-based FETs offered in principle a more immediate possibility to industrial applications due to the greater development of this technology [2.271, 2.272].

2.2.7.1 Structure and operation

The device structure of a TFET essentially differs from that of the MOSFET in the nature of the dopants used in the source and the drain. While MOSFETs have the same type of dopants, in TFETs, source and drain are of opposite types. The basic constituent of TFETs is thus a gated p-i-n diode, or less frequently – as previously mentioned – a gated p–n diode [2.268]. The name of the terminals is chosen to resemble the MOSFET biasing. To switch the device ON, the diode has to be reverse biased and a voltage applied to the gate. Therefore, an n-type TFET would require a positive voltage in the gate and also in the n-doped region, which would play the role of the drain if one recalls the analogy with the NMOS. The other p^+ region would act as the source and the intrinsic region as the channel. Figure 2.67 shows a schematic of a lateral single gate n-type silicon TFET where the dielectric

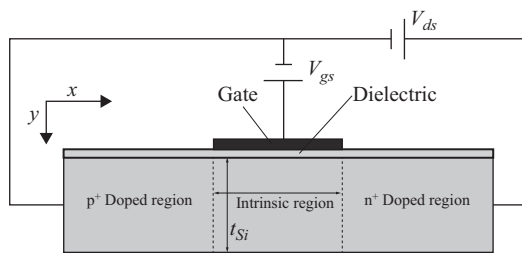

Figure 2.67 Single gate n-type TFET. The p^+-region acts as the source and the n^+-region as the drain

covers the source, the drain and the channel. In a p-type TFET, the dopings would be the opposite: the source would be n^+ and the drain, p^+.

Prior to study the operation regimes of these transistors, and in order to better understand them, it may result very useful to analyze the qualitative behavior of the p–n tunnel diodes, in which p–i and n–i junctions of the TFET are based. Tunnel diodes consist of a p–n junction in which both p and n sides are degenerate (i.e., very heavily doped).

To illustrate this, let us consider the tunnel diode configurations depicted in Figure 2.68 along with their corresponding points in the $I-V$ curve, and discuss the

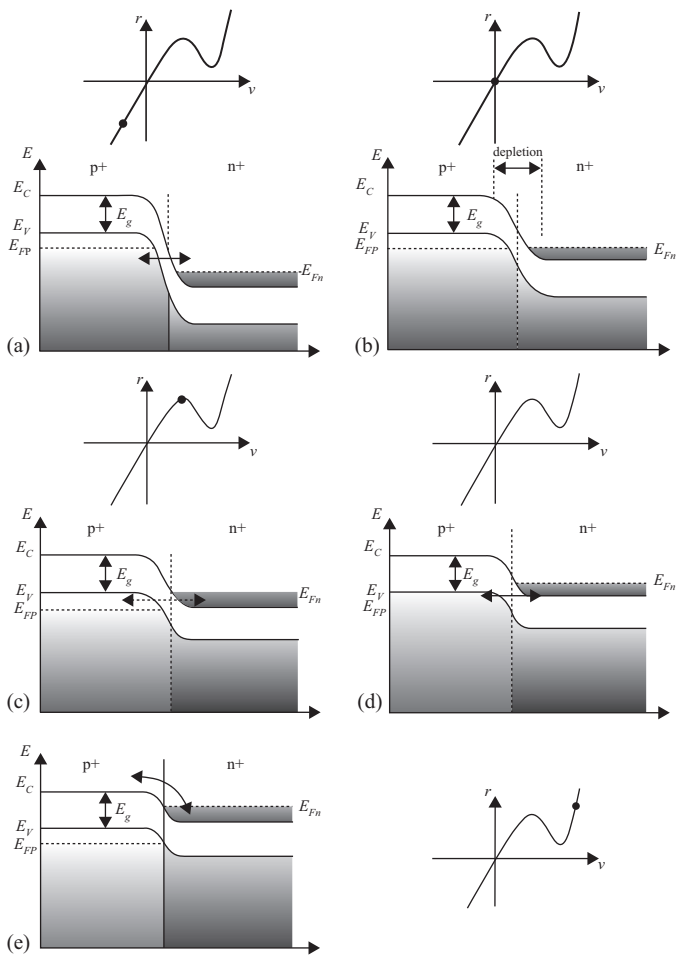

Figure 2.68 Energy band diagrams and I−V characteristics of a tunnel diode at (a) reverse bias with increasing tunneling current; (b) thermal equilibrium, zero bias; (c) forward bias V such that peak current is obtained; (d) forward bias approaching valley current; and (e) forward bias with diffusion current and no tunneling

different processes taking place in them at absolute zero temperature. Each of the different figures corresponds to:

(a) When the tunnel diode is reverse biased (p-side negative bias with respect to n-side), the BTBT current increases monotonically and indefinitely.
(b) At thermal equilibrium, no voltage is applied and the Fermi levels are aligned. That means that above the Fermi level there are almost no filled states on either side of the junction, and below it there are almost no empty states available on either side of the junction. Hence, net tunneling current at zero bias is zero.
(c) In the forward direction (positive voltage at the p-side with respect to n-side), the current first increases to a maximum because electrons can tunnel from the conduction band to the valence band. Tunneling is possible as there is a common band of energies with filled states on the n-side and unoccupied states on the p-side.
(d) If forward voltage is further increased, this range of common energies decreases and so does the current until the bands are uncrossed and there are no available states aligned with filled states.
(e) Once tunneling current becomes zero, normal diffusion current begins to dominate and current increases again exponentially.

However, in Figure 2.68e there also exists another type of current contribution called excess current. The excess current arises from a BTBT process that takes place indirectly through energy states within the forbidden gap. Several possible routes followed by carriers can be seen in Figure 2.69 [2.273]. As an example, an electron could drop down from A to an empty level at B, decreasing its energy, from which it might tunnel to the final state D in the valence band. Alternative trajectories would be ACD, or even a staircase route formed by several tunneling transitions followed by vertical losses of energy. This last one is by far less probable and requires a sufficiently high concentration of intermediate states.

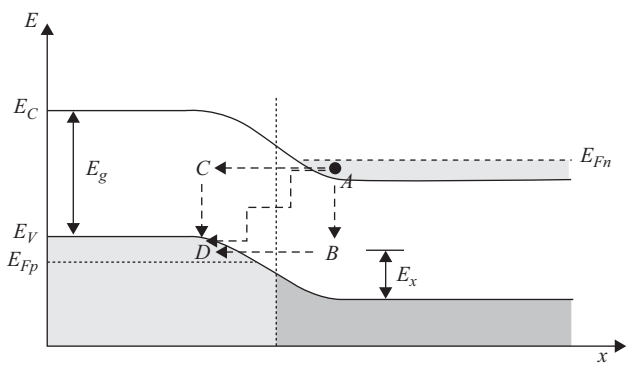

Figure 2.69 Example of different BTBT trajectories through intermediate states in the forbidden gap. E_x is the energy through which the electron must tunnel in B

2.2.7.2 Operating regimes of the TFET

In Figure 2.70, we show the band diagrams for the OFF and ON states of the TFET. There are two configurations that correspond to the OFF state. The first is when the band structure is in equilibrium and no bias applied, Figure 2.70a, which corresponds to a situation as that shown in Figure 2.68b. In this initial state, the built-in potentials of the p–i and n–i junctions determine the characteristic staircase-like profile that can be observed. When we only apply a positive voltage to the drain, $V_{DS} > 0$, the current flow is not allowed through the device in absence of gate bias because electron and hole currents are blocked by the built-in barriers (Figure 2.70b with $V_{GS} = 0$). In this situation, only reverse biased p-i-n diode leakage current flows between the source and the drain. This leakage current is extremely low (may result of order fA/μm).

When we apply positive voltage to the gate, $V_{GS} > 0$, the conduction band inside the channel is pushed down until it is aligned with the top of the valence band of the source. From that point onward, BTBT begins to be possible and carriers (in this case, electrons) are injected from the source into the channel (Figure 2.70b with $V_{GS} > 0$). This operating mode is the n-channel ON-state with source/channel junction resembling that of Figure 2.68a. We clearly see how the gate controls the band bending inside the channel and, consequently, the BTBT mechanism. TFETs designed with symmetry between the p- and n-doped regions, may show ambipolar behavior provided that adequate voltages are applied to the terminals. In our case, if we change the sign of the voltage applied to the gate,

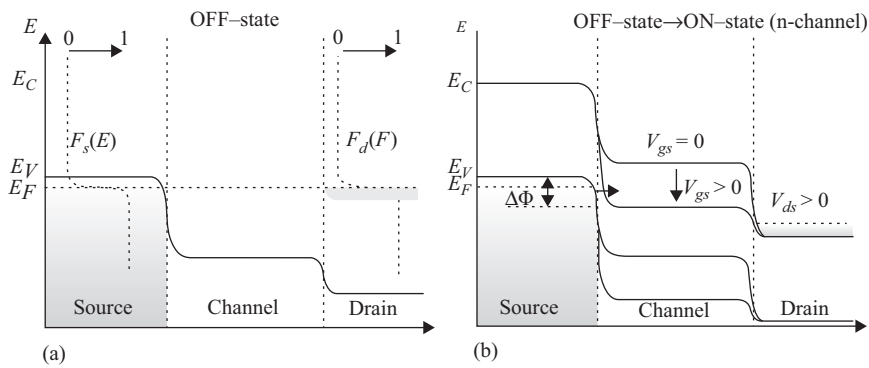

Figure 2.70 Energy band diagrams of the TFET taken horizontally along the channel close to the dielectric interface. (a) OFF-state showing the equilibrium configuration of energy bands when no bias is applied at the gate and the drain. (b) Combined ON- and OFF-states. When $V_{GS} = 0$, BTBT cannot take place and only p-i-n diode leakage current exists: OFF-state. If a big enough $V_{GS} > 0$ is applied, the conduction band in the channel is pushed down and BTBT may appear: ON-state. $\Delta\Phi$ represents the difference between the top of the valence band in the source and the bottom of the conduction band in the channel

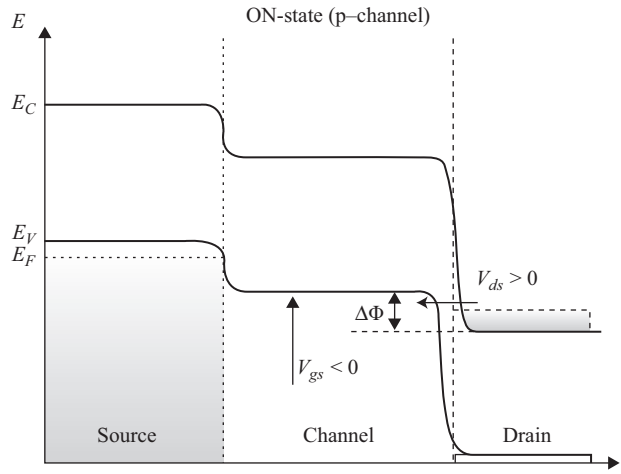

Figure 2.71 Band diagram configuration of the p-channel ON-state of the TFET. Carriers are injected from the drain into the channel once the top of the valence band inside the channel is raised over the bottom of the conduction band in the drain

$V_{GS} < 0$ – while keeping $V_{DS} > 0$ – the bands inside the channel move up and carriers can tunnel through the drain/channel junction as soon as the valence band inside the channel is lifted above the bottom of the conduction band in the drain. This can be seen in Figure 2.71. In this case, we again recall the situation of Figure 2.68a, but now between the drain and the channel. Obviously, this ambipolar behavior would imply a reassignation of "source" and "drain" labels for the p-channel ON-state if one wants to keep the analogy with the MOSFET operation.

To complete the description of the operating modes of the n-type TFET, let us consider $V_{DS} < 0$ and sufficiently large. In that case, the p-i-n structure is forward biased which means that carriers can flow with $V_{GS} = 0$ and results in exponential diode characteristics. The application of gate bias may block either the electrons or the holes by means of a potential barrier but not both. This configuration is not appropriate for switching purposes. Hence, while the drain bias switches the device characteristics from that of a forward-biased p-i-n diode to that of a TFET, the gate bias switches the TFET characteristics from an n-channel to a p-channel mode of operation, when the diode is reverse-biased.

TFETs are essentially based on tunneling rather than thermal emission. In this sense, they clearly differ from the normal operation pattern of conventional MOSFETs. In the subthreshold regime, we can use the following expressions [2.274] to describe the BTBT current in a tunnel diode assuming DT where the momentum is conserved in direct bandgap

$$I_{BTBT} = C_1 \int_{E_{Cn}}^{E_{Vp}} [f_C(E) - f_V(E)] T(E) N_C(E) N_V(E) dE \tag{2.38}$$

C_1 is a constant, $N_{C,V}(E)$ are the density of states in the conduction and valence bands respectively, $T(E)$ is the transmission probability across the energy tunneling barrier width – which is assumed to be equal for both directions – and $f_{C,V}(E)$ are the occupation probabilities of the bands described by the Fermi distribution functions.

Let us focus now on the tunneling process that happens at the source/channel junction in the n-channel mode. The bands profile is similar to that shown in Figure 2.68a. An accurate way to describe the transmission probabilities through the barrier was developed by Sze [2.275] using the WKB approximation and a triangularly shaped potential barrier, as depicted in Figure 2.72.

The 1D expression for the tunneling transmission probability is given by

$$T(E) \approx exp\left[-2\int_{x_{start}}^{x_{end}} k(x)dx\right] \tag{2.39}$$

with *k(x)* the wave vector of the electron inside the barrier, which, using the parabolic band approximation is given by

$$k(x) = \sqrt{\frac{2m^*}{\hbar^2}(U(x) - E)} \tag{2.40}$$

where m^* is the electron effective mass. If we assume that, according to Figure 2.71, the electron approaches the barrier at the bottom of the triangle, then $E = 0$ for it. The linear equation for the potential energy reads as

$$U(x) = \frac{E_g}{2} - qF(x)x \tag{2.41}$$

With these assumptions, the transmission probability reads as

$$T(E) \approx exp\left[\frac{4}{3}\frac{\sqrt{2m^*}}{qF\hbar}\left(\frac{E_g}{2} - qFx\right)^{\frac{3}{2}}\right]\Bigg|_{x_{start}}^{x_{end}} = exp\left(-\frac{4\sqrt{2m^*}E_g^{\frac{3}{2}}}{3qF\hbar}\right) \tag{2.42}$$

To perform the integration we have assumed that the electric field, $F(x)$, is uniform along the integration path ($F(x) = F$) which is consistent with the approximated shape of the barrier of Figure 2.72. This assumption is made in the so–called

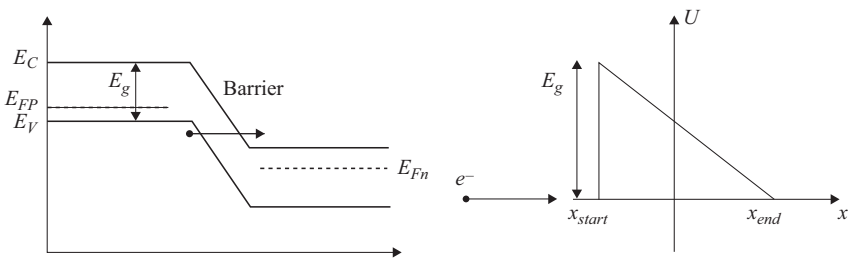

Figure 2.72 BTBT process approximated by a triangular barrier with the electron tunneling at the base of the triangle

semiclassical local models and allows obtain an analytical expression for the transmission probability. A more realistic approximation is incorporated in non-local models, which explicitly regard F as a function of x given its dependence on the band bending at every point inside the barrier. As a consequence, in non-local models, $T(E)$ is more accurately described. Nonetheless, unlike what happens in local models, the integration cannot be solved analytically but only numerically. The electric field may be replaced by $F = \frac{E_g}{qw}$ in the case of the situation shown in Figure 2.72 (with $w = x_{end} - x_{start}$), thus leaving $T(E)$ as a function of the width and height of the barrier

$$T(E) \approx exp\left(-\frac{4w\sqrt{2m^*E_g}}{3\hbar}\right) \tag{2.43}$$

Finally the BTBT current can be expressed as

$$I_{BTBT} = \frac{Aq^2}{36\pi\hbar^2}\sqrt{\frac{2m^*}{E_g}}Dexp\left(-\frac{4\sqrt{2m^*}E_g^{\frac{3}{2}}}{3qF\hbar}\right) \tag{2.44}$$

where the integral D is

$$D = \int [f_C(E) - f_V(E)]\left[1 - exp\left(-\frac{2E_S}{\overline{E}}\right)\right]dE \tag{2.45}$$

with $\overline{E}$ and E_S given by

$$\overline{E} = \frac{\sqrt{2}q\hbar F}{\pi\sqrt{m^*E_g}} \tag{2.46}$$

$$E_S = min\left(E_{Vp} - E, E - E_{Cn}\right) \tag{2.47}$$

The BTBT current is finally given by

$$I_{btbt} \propto exp\left[-\frac{4\lambda\sqrt{2m^*}E_g^{\frac{3}{2}}}{3\hbar\left(E_g + \Delta\Phi\left(V_{gs}\right)\right)}\right]\Delta\Phi\left(V_{gs}\right) \tag{2.48}$$

Here, λ is the screening tunneling length and describes the spatial extent of the transition region at the source–channel interface; it depends on the specific device geometry. In a TFET, at constant drain voltage, V_{DS}, the V_{GS} increase reduces λ and increases the energetic difference between the conduction band in the source and the valence band in the channel ($\Delta\Phi$), so that in a first approximation the drain current is a super-exponential function of V_{GS}. As a result, in contrast to the MOSFET, the point subthreshold swing of the TFET is no longer a constant but strongly depends on V_{GS}. This behavior clearly differs from that of conventional MOSFETs, in which SS is a constant and does not vary with V_{GS}.

Figure 2.73 compares the subthreshold characteristics of a TFET and an ideal MOSFET transistor (SS = 60 mV/dec). Swing is smallest at the lowest V_{GS} for which BTBT occurs, and increases as V_{GS} does likewise. As a consequence of this

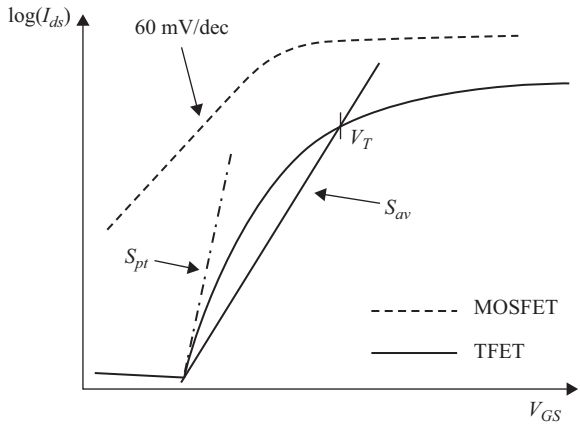

Figure 2.73 Qualitative comparison between and ideal MOSFET and TFET subthreshold characteristics. S_{pt} and S_{av} are depicted for TFETs showing the nonuniformity of subthreshold slope (SS)

variation, two different SS are defined in TFETs: the point swing, S_{pt}, and the average swing, S_{av}. S_{pt} is the smallest swing anywhere in the I_{DS}–V_{GS} curve, and in most cases coincides with the point where BTBT starts. On the other hand, S_{av} is the swing taken from the point where BTBT begins, up to the threshold voltage. There is not a unified definition of the threshold voltage in TFETs. Some authors use the constant current technique (usually 10^{-7} A/μm). Other authors choose a more physically based definition and regard the threshold voltage as the voltage at which the control that the corresponding electrode exerts over the current changes from quasi-exponential to linear.

These two swings are qualitatively shown in Figure 2.73 along with the conventional MOSFET characteristics. Note that typically the TFET has a lower ON-state and OFF-state current. S_{av} is the most important swing for switch performance. Unlike conventional MOSFETs where SS is a function of the thermal factor kT/q, SS does not depend on temperature to a first approximation in TFETs. This fact is not surprising since tunneling currents are weakly dependent on temperature. However, this does not imply that there is no degradation in S_{pt} or S_{av}. Degradation with T indeed exists given that rising temperatures clearly affect leakage current by increasing it, and making the steepest region of the curves disappear. Figure 2.74 shows simulated I_{ds}–V_{gs} curves for a single gate and a double gate n-channel TFETs (schematically shown in Figure 2.75).

Today TFETs represent the most promising steep-slope switch candidate, having the potential to use a supply voltage significantly below 0.5 V and thereby offering significant power dissipation savings. Because of their low off currents, they are ideally suited for low-power and low-standby-power logic applications operating at moderate frequencies (several hundred MHz). Other promising applications of TFETs include ultra-low-power specialized analog ICs with improved temperature stability and low-power SRAM.

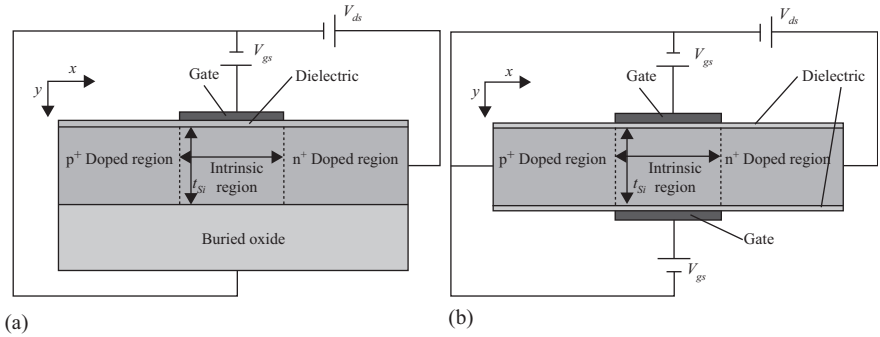

Figure 2.74 Schematic cross-section (not to scale) of the single gate (a) and double gate (b) n-channel TFETs considered. Dopings: p^+ region: 10^{20} cm^{-3}; intrinsic/lightly doped region: 10^{17} cm^{-3} (n-type); n^+ region: 10^{20} cm^{-3}; $t_{ox} = 1$ nm; $L_{source} = L_{drain} = 100$ nm; $L_g = 20$ nm; $t_{Si} = 3$ nm

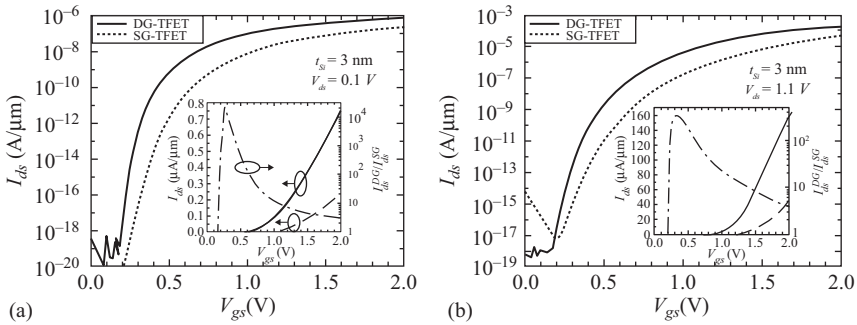

Figure 2.75 Transfer characteristics for (a) single gate and (b) double gate TFETs with $t_{Si} = 3$ nm for $V_{DS} = 0.1$ and 1.1 V. The inset shows the current on linear scale (left axis) and the ratio $\frac{I_{ds}^{DG}}{I_{ds}^{SG}}$ (right axis)

The biggest challenge is to achieve high performance (high I_{ON}) without degrading I_{OFF}, combined with an SS of less than 60 mV per decade over more than 4 decades of drain current. This requires the additive combination of the many technology boosters specific to complementary heterostructure TFETs, which are available or under research on advanced SOI CMOS platforms.

2.3 Different approaches for semiconductor device modeling and simulation

2.3.1 TCAD tools: technological motivation and general outlook

The IC plays a key role in our modern digital information society. Sophisticated technology computer-aided design (TCAD) tools are currently used to assist in IC

development and engineering at practically all stages from process design and definition to circuit development and optimization. The level of success which microelectronics has achieved by now was predestined and enabled by the extensive smart TCAD use providing and supporting an appropriate level of mathematical abstraction necessary to design elements and circuits containing billions of interconnected devices. At present, TCAD tools allow to reduce research and development costs by approximately 35%–40% [2.276]. Superior performance is achieved by making transistors smaller, faster, cheaper, and more energy efficient and by assembling more elements on a die. Thanks to the unique MOSFET scalability, the minimum feature size of a transistor has been successfully reduced for more than four decades, allowing to effectively double the number of transistors on a chip by every second year. Today, with the 14 nm CMOS technology introduced [2.59, 2.66], the physical transistor gate length is shorter than 20 nm. Nowadays, this trend which is institutionalized as the famous Moore's law is showing signs of saturation as Intel has recently announced a delay in bringing to the market the next generation of devices manufactured within the 10 nm technology node [2.315]. However, supported by a demonstration of MOSFETs with a gate length as short as 6 nm already in 2002 [2.290], the International Technology Roadmap for Semiconductors [2.276] predicts further scaling beyond the10 nm node in the coming decade. This demands extension and possibly a redesign of the known TCAD tools for modeling the transport behavior in a given device down to sub-10 nm scale. Many new aspects must be taken into consideration at these dimensions. For example, the famous three-dimensional tri-gate architecture [2.341] employed by Intel for the 22 nm and 14 nm technology nodes require fully three-dimensional device modeling. The cutting-edge devices fabricated with the 14 nm process are so small that the fluctuations of the number of dopants inside the channel alter their characteristics significantly [2.282]. Even more, a particular positioning of an impurity in the channel affects the current thus demanding TCAD to take this randomness into account.

The first suggestion of a fully numerical transport description in a one-dimensional bipolar transistor was available already in 1964 [2.311]. The approach was further developed and extended to describe the carrier transport in *PN*-junctions [2.288] and impact ionization avalanche diodes by Scharfetter and Gummel in 1969 [2.354]. The first application of a solution of the two-dimensional Poisson equation to address electrostatics of metal-oxide-semiconductor (MOS) structures was performed by Loeb [2.335] and Schroeder and Muller [2.355]. A simultaneous solution of the coupled continuity and Poisson equations to describe the transport in junction gate field effect [2.325] and bipolar transistors [2.361] goes back to 1969.

Since the pioneering work on transport modeling numerical approaches have been successfully developed and applied to practically all important devices prompting the number of papers in the field to grow exponentially. Today modeling of transport in modern ICs has matured into a well-established field with vast commercial applications and intense software development. Numerous textbooks, monographs, and reviews devoted to theoretical and computational aspects of transport modeling in ICs are available. Not pretending to cover all the literature we

would like to mention one of the first monographs [2.356], which addresses practically all aspects from modeling and discretization to applications, the textbooks describing various semiclassical transport models [2.336] and modern quantum mechanics-based approaches to electron transport [2.287], and a monograph [2.363] investigating the role of mechanical stress to boost the performance of modern MOSFETs.

As the development and maintenance costs of modern sophisticated TCAD have increased significantly, only large semiconductor companies can afford to support their own TCAD development team. Fortunately, there exist a fairly large number of commercial TCAD software products available on the market, e.g., [2.360, 2.366], which serve most of the industrial demands. Numerous TCAD tools developed at the universities have an advantage of being open-source licensed software [2.316, 2.345, 2.368]. These tools gain their popularity due to the need of multiscale approaches to simulations combining different levels of complexity and precision. It makes these tools valuable not only for pure educational or research purposes but also satisfies the demand from semiconductor manufacturing companies for more refined simulations of complex phenomena. This urges a creation of new successful spin-off companies, e.g., [2.26, 2.78], focusing on the development and commercialization of specialized tools.

Regardless of the small transistor size, even today most TCAD tools are based on semi-classical macroscopic transport models. The celebrated drift-diffusion transport model has enjoyed an amazing success due to its relative simplicity, numerical robustness, and an ability to perform two- and three-dimensional simulations on large unstructured meshes [2.356]. However, with device size dramatically reduced and new technology elements and materials introduced, the TCAD tools based on the standard semi-classical transport description are becoming less accurate.

From the viewpoint of transport modeling in nanoscale transistors, the problem is two-fold. First, with downscaling the driving field and its gradient increase dramatically inside the short channel. As a result, the carrier distribution along the channel can no longer be described by even a heated shifted Maxwellian distribution typically assumed in current and energy transport. In order to properly account for the hot carrier and non-local high-field effects, the drift-diffusion and even the energy transport model have to be improved to incorporate higher-order corrections beyond the heated Maxwellian in the carrier distribution function. This leads to a more complicated and computationally involved macroscopic transport model equations set.

The second reason for semi-classical modeling tools to become inadequate is a growing importance of quantum-mechanical effects, especially the under-the-barrier tunneling which increases the leakage and causes parasitic power dissipation in the off-state. The band-to-band quantum-mechanical tunneling is the phenomenon, which defines the functionality of a TFET, the device with a potentially very steep subthreshold characteristic. Although less pronounced in the on-state current due to the averaging over many states at different energies involved in transport, the quantum-mechanical effects are believed to play a role in determining the current as the device size is getting comparable to the De Broglie electron wave length, where the transport is becoming more ballistic. However, since the devices operate

at room temperature, the carrier scattering in silicon-based FETs is still important [2.348] and a crossover from diffusive to ballistic transport may occur at much shorter channel lengths [2.300]. Therefore, an adequate transport model of an ultra-scaled MOSFET must account for both quantum-mechanical effects and scattering simultaneously.

In the direction perpendicular to transport the most important quantum-mechanical effect is the quantization of carrier motion in the potential well. This results in the formation of subbands described with the corresponding wave functions. The subband wave functions nearly do not penetrate in the gate dielectric, which results in the rapid decay of the corresponding subband charge densities close to the gate–oxide interface. Classically, however, the charge density is characterized by the maximum value at the interface. As a consequence, the transport can no longer be accurately described by the classical three-dimensional equations, and a new description based on two- or even one-dimensional subbands in tri-gate structures and FinFETs must be adopted. In addition, the subbands are characterized by the transport effective masses which, apart from strain, depend strongly on the channel orientation, and, most importantly, on the confinement strength.

Modern TCAD tools must be flexible enough to address challenges of the upcoming technological changes due to the use of new materials and structures. They have to describe properly transport in silicon and new channel materials depending on strain and confinement and must be prepared to adequately address the quantum-mechanical phenomena which are expected to determine the transport properties in ultra-scaled CMOS and post-CMOS devices.

The electron spin attracts at present much attention as a possible candidate for complementing or even replacing the charge degree of freedom in future devices. The electron spin state is characterized by one of two of its possible projections on a given axis and could be potentially used in digital information processing. In addition, it takes an amazingly small amount of energy to invert the spin orientation, which is necessary for low power applications. The electron spin may also point in any direction on a unit Bloch sphere, which opens new directions in storing and processing information by initializing, manipulating, and detecting the spin orientation. Therefore, the TCAD tools must be ready to help foreseeing and guiding the future device development based on new principles of operation.

Without pretending to cover the large field of transport modeling research here, we present several important examples and outline some difficulties and challenges regarding the transport description in modern MOSFETs. We begin with the semi-classical description of carrier dynamics inside the device and outline methods to solve the Boltzmann equation. A particular emphasis will be put on the inclusion of strain effects into the transport simulations. We also demonstrate how the spin lifetime can be evaluated by methods similar to those employed for the low-field mobility calculations. In ultra-scaled devices quantum-mechanical effects start playing an important role. Different types of quantum potential and density gradient corrections can be introduced. We conclude with briefly mentioning fully quantum-mechanical approaches dealing with the dissipative quantum transport in ultra-scaled devices.

2.3.2 Drift-diffusion transport model

In order to analyze a semiconductor device under general operating conditions, a mathematical model has to be formulated first. Regardless of the complexity of carrier dynamics inside the semiconductor, two equations are the most important ingredients of any particular model. These are the Poisson equation and the current continuity equation [2.356]. The Poisson equation relates the carrier charge density ρ to the electrostatic potential V as

$$\nabla\varepsilon\nabla V = -\rho \tag{2.49}$$

where ε is the dielectric permittivity. The charge density is related to the electron n and hole p via

$$\rho = q(p - n + C) \tag{2.50}$$

where q is the electron charge value and C is the concentration of fixed ionized charges.

The continuity equation relates the charge current density

$$\vec{j}(\vec{r},t) = \vec{j}_n(\vec{r},t) + \vec{j}_p(\vec{r},t) \tag{2.51}$$

to the time derivative of the charge density $q(p–n)$

$$\frac{\partial(n-p)}{\partial t} = \frac{1}{q}\nabla\vec{j} \tag{2.52}$$

In case $\frac{\partial C}{\partial t} = 0$ the electron and hole contributions are described by two separate equations.

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla\vec{j}_n + R \tag{2.53}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla\vec{j}_p + R \tag{2.54}$$

Here R is the electron–hole generation-recombination rate.

In order to complete the formulation of the mathematical model at this level, the system of these two equations must be supplemented with the current density expressed via the electron and hole concentrations and the electric field. By assuming a constant temperature in the device, the electron $\vec{j}_n$ and hole $\vec{j}_p$ current densities can be, in the simplest form, written as

$$\vec{j}_n = qn\mu_n\vec{E} + qD_n\nabla n \tag{2.55}$$

$$\vec{j}_p = qp\mu_p\vec{E} - qD_p\nabla p \tag{2.56}$$

$\mu_{n(p)}$ is the electron (hole) mobility and $D_{n(p)}$ is the electron (hole) diffusion coefficient.

The electron mobility and diffusion coefficient are material dependent. In order to calculate their values an accurate description of the carrier dynamics in the material is required.

Equations (2.49–2.56) form the framework of the transport description in the drift-diffusion approximation. Although more accurate transport models have been extensively developed, implemented, and used, the drift-diffusion-based simulations continue to be mainstay. One reason is the relative simplicity of the model, which allows obtaining timely yet accurate results [2.337]. Another reason is that the drift-diffusion simulations are surprisingly predictive even in situations, where they are not expected to work at all. Several examples [2.337], for which the drift-diffusion provides amazingly good results, include the diffusion through a thin base of a bipolar transistor near the ballistic limit and an emission-diffusion theory through the Schottky barrier, which reproduces the Landauer theory. Even a quasi-ballistic transient heat phonon transport can be well modeled with the drift-diffusion model [2.337].

Although the drift-diffusion formalism can be applied to describe a wide range of phenomena, it is instructive to understand the formal limitations of the approach and ways to go beyond the approximations. We demonstrate the common generalizations of the drift-diffusion approximation by considering first the semi-classical transport model and then transport models including higher moments of the carrier distribution function.

2.3.3 *Semi-classical transport and higher moments transport models*

An ensemble of classical particles is conveniently described by the single-particle distribution function $f(\vec{r}, \vec{k}, t)$ in phase space. The distribution function satisfies the Boltzmann equation.

$$\frac{\partial f}{\partial t} + \vec{v} \cdot \nabla_r f + \frac{S_v q}{\hbar} \vec{E} \cdot \nabla_{\vec{k}} f = \left(\frac{\partial f}{\partial t}\right)_{coll} \tag{2.57}$$

$\vec{v} = \nabla_{\vec{k}} E(\vec{k})$ is the carrier velocity.

The sign function s_v distinguishes between negatively charged electrons, $s_n = -1$, and positively charged holes, $s_p = 1$. The right-hand side in (2.57) represents the collision operator due to phonons, impurities, interfaces, and other scattering sources.

For realistic structures, a direct numerical solution of this equation by discretization of the phase space is computationally expensive. Therefore, the Boltzmann transport equation is not solved directly in the TCAD tools. Usually an approximate solution is obtained by using the method of moments of the distribution function. By defining the moments of the distribution function $f(\vec{r}, \vec{k}, t)$, one consecutively obtains the drift-diffusion model [2.311], the energy transport model [2.362], or the six-moments transport model [2.305].

The drift-diffusion mode has several shortcomings, when it is applied to miniaturized devices. Hot carrier effects can be partly addressed by a mobility dependence on the driving field. However, non-local effects such as velocity overshoot are completely neglected within the drift-diffusion approach. Higher-order transport hydrodynamic model [2.285] and the energy transport model [2.362] are designed to overcome some of these shortcomings. However, the energy transport model tends to overestimate the non-local effects and thus the on-current in a device. This also results in unacceptable errors in the hot carrier induced gate tunneling current [2.299]. Another example is a particularly poor description of transport in partially depleted SOI devices, where, because of the overestimated hot carrier diffusion into the floating-body of the device, the energy transport model fails completely in predicting the device characteristics [2.308–2.310], and the application of transport models including higher-order moments is required. The six-moments transport model includes additional information about the shape of the distribution function and is predestine to overcome the above-mentioned limitations [2.305, 2.307, 2.308, 2.329].

The derivation of the transport models is based on equations of the moments-statistical averages as

$$\langle\vec{\Phi}\rangle = \frac{1}{4\pi^3}\int \vec{\Phi}\left(\vec{k}\right) f\left(\vec{r},\vec{k},t\right) d^3k \tag{2.58}$$

where $\langle\vec{\Phi}\rangle$ is a weight function in $\vec{k}$ space. In order to derive a particular model, the following weight functions are considered.

$$\begin{aligned} &\Phi_0 = 1, \quad \Phi_2 = E\left(\vec{k}\right), \quad \Phi_4 = E^2\left(\vec{k}\right) \\ &\vec{\Phi}_1 = \hbar\vec{k}, \quad \vec{\Phi}_3 = \vec{v}E\left(\vec{k}\right), \quad \vec{\Phi}_5 = \vec{v}E^2\left(\vec{k}\right) \end{aligned} \tag{2.59}$$

Here an isotropic parabolic dispersion $E(\vec{k}) = \frac{\vec{k}^2}{m_v}$ with the effective mass m_v is assumed; however, a generalization to non-parabolic energy band dispersions is straightforward [2.303]. Taking the moment of the Boltzmann equation gives the following general moment equation

$$\frac{\partial\langle\vec{\Phi}_j\rangle}{\partial t} + \nabla_{\vec{r}}\cdot\langle\vec{v}\otimes\vec{\Phi}_j\rangle - s_v q\vec{E}\cdot\langle\nabla_p\otimes\vec{\Phi}_j\rangle = \int d^3k\vec{\Phi}_j\left(\frac{\partial f}{\partial t}\right)_{coll} \tag{2.60}$$

where $\otimes$ denotes the tensor product. In order to obtain a closed set of equations for moments several approximations have to be introduced. One is concerned with the moments of the scattering integral, which are frequently approximated using a macroscopic relaxation time expression.

$$\int d^3k\vec{\Phi}_j\left(\frac{\partial f}{\partial t}\right)_{coll} \cong -\frac{\langle\vec{\Phi}_j\rangle - \langle\vec{\Phi}_j\rangle_0}{\tau_\Phi} \tag{2.61}$$

The distribution function can be split into a symmetric and an antisymmetric part, where the symmetric part of the distribution function depends only on the absolute value of $\vec{k}$.

$$f\left(\vec{k}\right) = f_S\left(\left|\vec{k}\right|\right) + f_A\left(\vec{k}\right) \tag{2.62}$$

The carrier concentration v, the carrier temperature T_v, the current density $\vec{J}$, the energy flux density $\vec{S}$, the "second-order" temperature Θ_v, the moment of the sixth order M_6, and the flux $\vec{K}_v$ (related to the kurtosis of the distribution) are defined by

$$\nabla \cdot \vec{J}_v = -s_v q\left(\frac{\partial v}{\partial t} + R_v\right) \tag{2.63}$$

$$\nabla \cdot \vec{S}_v = -C_4 \frac{\partial (vT_v)}{\partial t} + \vec{E} \cdot \vec{J}_v - C_4 v \frac{T_v - T_L}{\tau_{E(k)}} + G_{E(k)v} \tag{2.64}$$

$$\nabla \cdot \vec{K}_v = -C_5 \frac{\partial (vT_v\Theta_v)}{\partial t} + 2s_v q\vec{E} \cdot \vec{S}_v - C_5 v \frac{T_v\Theta_v - T_L^2}{\tau_\Theta} + G_{\Theta_v} \tag{2.65}$$

$$C_4 = \frac{3}{2}k_B, C_5 = \frac{15}{4}k_B^2 \tag{2.66}$$

The system of balance equations for the densities is completed with the equations for fluxes

$$\vec{J}_v = -C_1\left(\nabla(vT_v) - s_v \frac{q}{k_B}\vec{E}_v\right), C_1 = s_v k_B \mu_v \tag{2.67}$$

$$\vec{S}_v = -C_2\left(\nabla(vT_v\Theta_v) - s_v \frac{q}{k_B}\vec{E}_v T_v\right), C_2 = \frac{5}{2}\frac{k_B^2}{q}\frac{\tau_S}{\tau_m}\mu_v \tag{2.68}$$

$$\vec{K}_v = -C_3\left(\nabla(vM_6) - s_v \frac{q}{k_B}\vec{E}vT_v\Theta_v\right), C_3 = \frac{35}{4}\frac{k_B^3}{q}\frac{\tau_K}{\tau_m}\mu_v \tag{2.69}$$

where the mobility μ_v is defined as

$$\mu_v = \frac{q\tau_m}{m_v} \tag{2.70}$$

We note that generation-recombination terms may depend on both electron and hole distribution functions in an integral, non-local manner [2.356], which makes the task of solving the corresponding equations extremely difficult. Therefore, generation-recombination terms have to be modeled carefully using knowledge from solid-state physics of semiconductors, which may represent a significant challenge [2.306].

Let us now derive the hierarchy of TCAD transport models. The drift-diffusion transport model consists of the continuity equations (2.63) and the current relations

(2.67). The latter is decoupled from the higher-order equation by introducing a closure assumption for the second order moment

$$T_v = T_L \tag{2.71}$$

The physical meaning of this assumption is that the carrier gas is in equilibrium with the lattice. The energy transport model additionally takes into account the carrier energy balance equation (2.64) and the energy flux equation (2.68). To close the system of equations, an assumption on the fourth-order moment has to be introduced. The assumption of a heated Maxwellian distribution for the symmetric part of the distribution function gives the closure relation

$$\Theta_v = T_v \tag{2.72}$$

Going one step further in the model hierarchy, the balance equation for the average squared energy (1.16) and the related flux equation (2.69) are added. To close the equation system, the moment of sixth-order M_6 has to be approximated using the lower-order moments. An empirical closure relation that accounts for the "second-order" temperature Θ_v is the best choice [2.304].

$$M_6 = T_v^3 \left(\frac{\Theta_v}{T_v}\right)^c \tag{2.73}$$

From MC simulations, which are an accurate reference, the value of $c = 2.7$ has been estimated [2.302] for the simulation of miniaturized MOSFETs. Compared to the energy transport models, the six-moments model requires two additional relaxation times, namely, the relaxation time of the second-order temperature τ_Θ and the kurtosis flux relaxation time τ_K. Since analytical models for these new parameters are not available, tabulated values obtained from bulk MC simulations [2.302] can be used.

2.3.3.1 Deterministic solution of the Boltzmann transport equation

In order to evaluate the accuracy of the transport models the solution of the Boltzmann transport equation for the distribution function with subsequent calculations for the moments and the current density is required. The current density obtained with this method, as an integral of the velocity with the distribution function, is free from the assumptions used to close the set of the equations for the moments and fluxes, and can be used for benchmarking the transport models.

With computers getting more powerful, a deterministic numerical solution of the Boltzmann equation for the distribution function can be found by expanding the angular dependence of the distribution function $f(\vec{r}, \vec{k})$ on $\vec{k}$ using a complete set of spherical harmonics $Y_{lm}(\theta, \phi)$.

$$f\left(\vec{r}, \vec{k}\right) = \sum\nolimits_{lm} f_{lm}\left(\vec{r}, \vec{k}\right) Y_{lm}(\theta, \phi) \tag{2.74}$$

θ and ϕ are the polar angles between the electric field $\vec{E}$ and $\vec{k}$. In the low-field limit one can truncate the expansion (2.74) after the terms with $l = 1$. Importantly, this truncation results in a drift-diffusion transport model for the current under the

assumptions of parabolic isotropic bands and randomizing elastic scattering. It turns out that in silicon, where the valleys are anisotropic, this approximation gives good results [2.313] in the limit of a weak electric field.

For general scattering processes and realistic band structures as well as at higher driving fields, more terms in the expansion (2.74) are required [2.349]; however, a limited number (less or around ten) of spherical harmonics is needed to achieve good accuracy. Because the angular dependence is accounted for by a small number of harmonics, the number of discretization points in momentum space is reduced with respect to the full three-dimensional discretization procedure. This speeds up the computation significantly.

The knowledge of the distribution function allows evaluate numerically all the moments and fluxes needed for the formulation of the TCAD transport models. Although typically requiring more computer resources and longer simulation time than corresponding TCAD simulations, the deterministic solution of the Boltzmann equation by using the spherical harmonics expansion is essential in verifying the accuracy of the TCAD transport models.

Current–voltage characteristics computed with the spherical harmonic expansion method and using the macroscopic transport models based on the moments of the distribution function are shown in Figure 2.76. It is demonstrated that for a short-channel device the drift-diffusion model underestimates the current. Indeed, since the carrier temperature is assumed constant, the drift-diffusion model cannot

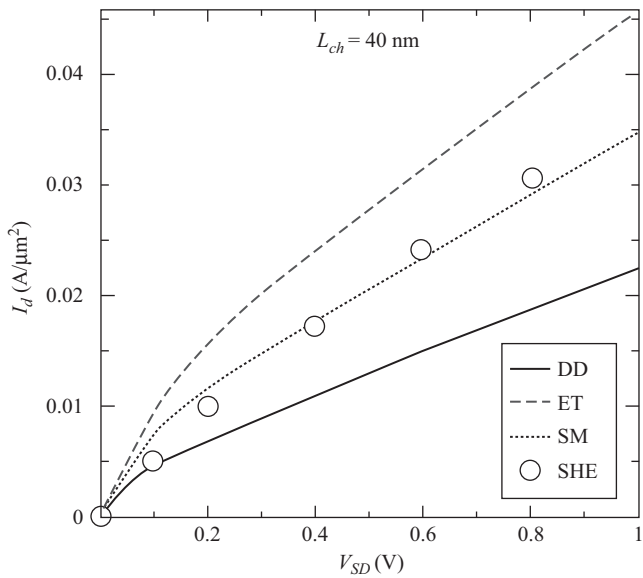

Figure 2.76 I–V characteristics computed with the drift-diffusion (DD), energy transport (ET), six moments (SM) transport models, and with the spherical harmonic expansion method. The six-moments model gives results closest to the results of the spherical harmonic expansion method

account for the non-local effects inside the short-channel device properly. Thus, for short devices the restriction of constant carrier temperature must be relaxed.

When the temperature is not constant, a temperature gradient causes heat flow and thermal diffusion appears. The drift-diffusion transport model must be augmented to allow the energy flow. The energy transport model additionally takes into account the energy flux and the carrier energy balance. The model, however, overestimates the drive current. Figure 2.77 illustrates the average velocity profile in a 40 nm long channel. The drift-diffusion model underestimates the average velocity, while the energy transport model overestimates it. In order to reduce this spurious velocity overshoot effect the next moments should be included for devices with L_{ch} shorter than about 40 nm. This is accomplished by introducing a transport model of sixth order. Balance equations for the average squared energy and the related flux are added. To close the equation system, the moment of sixth order has to be approximated by using the lower order moments (2.73).

The inclusion of higher moments improves the quality of the transport model significantly. The current–voltage characteristics are reproduced fairly well even for a short device as shown in Figure 2.76, because of the more accurate results for the averaged velocity (Figure 2.77). The solution of the Boltzmann equation is required in describing transport and hot carriers effects in power devices at very

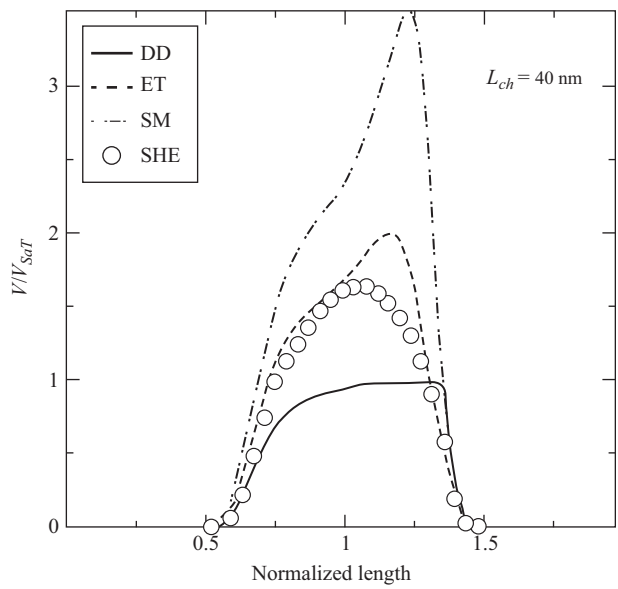

Figure 2.77 Average velocity along a device with 40 nm channel length computed with the macroscopic transport models and with the spherical harmonic expansion method. While the drift-diffusion model underestimates the velocity and current, the energy transport model overestimates the velocity in short-channel devices. The six-moments model gives best results as compared to the velocity obtained by the spherical harmonic expansion method

high-applied voltages, when even the use of the six-moments transport model may become insufficient.

The energy transport model requires knowing the mobilities for the current density and the energy flux, for each carrier type, one relaxation time, and the non-parabolicity factor for non-parabolic bands as the material parameters. The six-moments model requires two additional relaxation times for the second order temperature and the kurtosis flux. Having too many adjustable parameters is a particular inconvenience of the six-moments model. Solving the Boltzmann transport equation using the spherical harmonics expansion method or an MC algorithm usually tabulates these parameters. The parameter dependences on temperature, doping, and the electric field are determined from the conditions that the six-moments transport model mimics exactly all the moments obtained from the MC simulator under homogeneous conditions. The full-band MC method of the solution of the Boltzmann equation is required, when the band structure is strongly non-parabolic and is known only numerically.

We present an example of the mobility evaluation in stressed silicon where the band structure depends on strain in a complex manner. Alternatively, a Kubo-Greenwood approach can be applied to find the low-field mobility [2.298] as we show later on an example of ultra-thin silicon films with stress. The Kubo-Greenwood method can also be used to evaluate the electron spin lifetime and its dependence on strain.

2.3.3.2 Monte Carlo methods for the Boltzmann equation solution

Methods based on MC techniques are well established for studying transport in semiconductors [2.317]. The motion of charge carriers is simulated in the appropriate phase space formed by position and momentum. In the presence of external fields, the carriers which are considered as point-like objects with well-defined positions and momentum move according to Newton's law on classical trajectories. A dispersion relation expressing the carrier energy dependence on the crystal momentum is determined by the band structure. The free flight of carriers along the trajectory is interrupted by scattering events, which are assumed local in space and instantaneous in time. Scattering is modeled as a random process. The duration of a free flight, the type of scattering mechanism, and the state after the scattering are selected randomly from the given probability distributions characteristic to the microscopic scattering processes [2.314, 2.320, 2.339, 2.352]. The method of generating sequences of free flights and scattering events appears to be so intuitively transparent that it is frequently interpreted as a direct emulation of the physical transport process rather than a numerical method. For these reasons the MC methods of transport evaluations are quite time consuming. Being statistical by nature, the method provides an error inversely proportional to the square root of the total number of scattering events. The MC method for solving the Boltzmann transport equation can be useful when the deterministic solution is too expensive, as in strained silicon.

Mathematically one can reformulate the transport equation as an integral equation and then develop an MC algorithm for its solution [2.319, 2.343]. When the Boltzmann equation is transformed to an integral equation, which is then iteratively solved [2.319], the iteration series results in the MC backward technique. This

algorithm is useful, if rare events have to be simulated or the distribution function is needed only in a small phase space domain [2.328]. If the Boltzmann equation is reformulated in an adjoin integral form [2.326], a link between the physically based MC method and the iterative procedure of the solution of the integral equation is established.

Already in 1966 Kurosawa [2.332] applied the MC method to high-field transport in semiconductors. In References 2.292 and 2.293 GaAs and Ge were studied, correspondingly. In the mid-1970s a physical model capable of explaining the major macroscopic transport characteristics in silicon was developed [2.286, 2.318]. Considerable improvement of the method and application to a variety of materials was reported in Reference 2.317.

With an increase of the carrier energy the need of an accurate energy band structure description has been realized [2.297, 2.331, 2.358, 2.372]. For electrons in silicon, the most thoroughly investigated case, the "standard model" [2.295], provides a description of all scattering mechanisms. Transport analyzes considering the accurate band structure were performed in [2.296, 2.298, 2.323].

2.3.4 Stress- and orientation-dependent mobility in silicon

To compute the low-field electron mobility in strained Si, one can use the VMC simulator [2.369]. It includes a comprehensive set of scattering models with phonons, ionized impurities, alloy scattering, as well as impact ionization for both electrons and holes.

For electrons in n-silicon, a phonon-scattering model based on Jacoboni and Reggiani [2.320] is used. The model takes into account long-wavelength acoustic phonons causing intravalley transitions as well as optical phonons triggering intervalley transitions. Intravalley scattering is treated as an elastic process. Following [2.289] we adjusted the original values for the coupling constants for intervalley phonon scattering to achieve a bulk mobility enhancement factor of 70% in biaxially strained silicon layers. The coupling constants for acoustic and optical intervalley phonons, as well as the phonon energies are listed in Table 2.5. In full-band simulations the scattering rates are proportional to the density of states calculated from the band structure [2.323].

Figure 2.78 demonstrates the orientation-dependent electron mobility enhancement factor for tensile stress applied in [111] direction obtained from the full-band MC simulations.

Table 2.5 Modes, coupling constants, phonon energies, and selection rule of inelastic phonon scattering

Mode	Δ (MeV/cm)	$\hbar\omega$ (meV)	Selection rule
Transverse acoustic	47.2	12.1	f
Longitudinal acoustic	75.5	18.5	f
Longitudinal optical	1042.0	62.0	f
Transversal acoustic	34.8	19.0	g
Longitudinal acoustic	232.0	47.4	g
Transversal optical	232.0	58.6	g

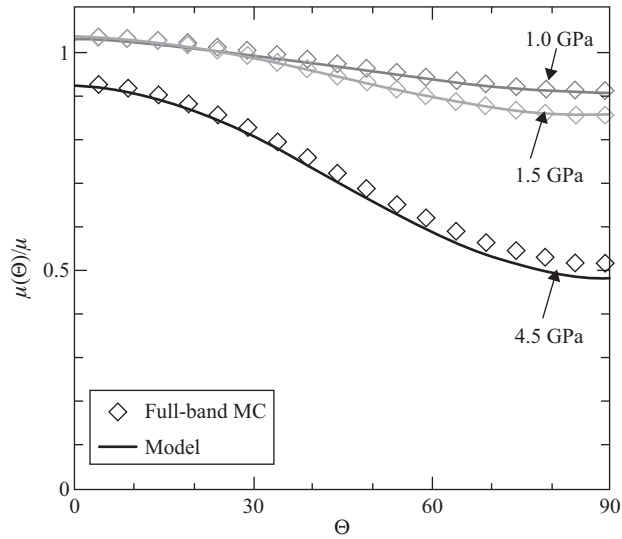

Figure 2.78 Orientation-dependent electron mobility variation in silicon under tensile stress along [111] direction, for several stress values. Results of full-band MC are well explained by the dependence of the effective masses on shear strain. Note the mobility degradation at high stress values caused by an increase of scattering due to the stress-dependent increase of the density-of-states mass

The current direction is defined by the unity vector $\hat{n}$.

$$\hat{n} = \left[\frac{cos(\Theta + \Phi_0)}{\sqrt{2}}, \frac{cos(\Theta + \Phi_0)}{\sqrt{2}}, sin(\Theta + \Phi_0)\right] \tag{2.75}$$

where $\Phi_0 \approx 36^o$ is the angle between [111] and [110] directions. The angle Θ determines the current direction in the plane defined by the [111] and [110] axes and is counted from the [111] direction. Results of the full-band simulations coincide well with an analytical model for the mobility described below.

Stress along the [111] direction does not produce a relative energy shift between the valleys and thus affects all six valleys in a similar way. The mobility of an ellipsoidal valley in an arbitrary orientation $\hat{n}$ with respect to the crystallographic coordinate system is determined by the inverse of the conductivity mass $1/m_{\mathbf{n}}$ along this direction computed as

$$m_n^{-1} = \hat{n}^T \hat{m}^{-1}(\eta)\hat{n} \tag{2.76}$$

where $m^{-1}(\eta)$ is the inverse effective mass tensor for the valley in the crystallographic system. $\eta = 2D\varepsilon_{xy}/\Delta$ is a dimensionless strain with $D = 14$ eV being the shear strain deformation potential, ε_{xy} the shear strain component, and $\Delta = 0.5$ eV [2.363].

Taking into account the dependence of the density-of-state effective mass $m_{dos}(\eta) = [m_l(\eta) \times m_{t1}(\eta) m_{t2}(\eta)]^{\frac{1}{3}}$ on dimensionless strain η, the mobility dependence on [111] strain in a direction $\hat{n}$ is obtained as

$$\frac{\mu(\eta, \hat{n})}{\mu_0} = \frac{m_c}{m_n} \left[\frac{m_{dos}}{m_{dos}(\eta)} \right]^{\frac{3}{2}} \tag{2.77}$$

μ_0 is the mobility of relaxed silicon, $m_c = 3\left(\frac{1}{m_l} + \frac{2}{m_t}\right)^{-1}$, and $m_l = 0.91 m_0$ and $m_t = 0.19 m_0$ are the longitudinal and transversal effective masses. The analytical curves for the mobility dependence on $\hat{n}$ in silicon in Figure 2.78 are obtained by substituting in (2.77) the strain-dependent longitudinal and transversal masses $m_{t1}(\eta)$, $m_{t2}(\eta)$, and $m_l(\eta)$. For the [001] oriented valleys the dependences are [2.363]

$$\frac{m_t}{m_{t1}(\eta)} = \begin{cases} \left(1 - \eta \dfrac{m_t}{M}\right), |\eta| < 1 \\ \left(1 - sgn(\eta) \dfrac{m_t}{M}\right), |\eta| > 1 \end{cases} \tag{2.78}$$

$$\frac{m_t}{m_{t2}(\eta)} = \begin{cases} \left(1 + \eta \dfrac{m_t}{M}\right), |\eta| < 1 \\ \left(1 + sgn(\eta) \dfrac{m_t}{M}\right), |\eta| > 1 \end{cases} \tag{2.79}$$

$$\frac{m_l(\eta)}{m_l} = \begin{cases} (1 - \eta^2)^{-1}, |\eta| < 1 \\ \left(1 - \dfrac{1}{|\eta|}\right)^{-1}, |\eta| > 1 \end{cases} \tag{2.80}$$

$sgn(\eta)$ denotes the sign function.

2.3.5 *Mobility in ultra-thin body of strained SOI transistors*

In thin silicon films the three-dimensional band structure splits into a number of two-dimensional subbands. A special subband MC method has to be implemented in order to evaluate the transport properties. Fortunately, to find the low-field mobility it is not necessary to run the MC simulations. Instead, following the Kubo-Greenwood approach [2.298], one can linearize the Boltzmann transport equation with respect to the proportionally small electric field and perturbation to the distribution function and obtain an approximate expression for the mobility

$$\mu = \frac{q}{4\pi^2 \hbar^2 k_B T n_S} \sum_i \int_0^{2\pi} d\phi \int_{E_1^{(0)}}^{\infty} dE \frac{\left|\vec{k}_i\right|}{\left|\frac{\partial E\left(\vec{k}_i\right)}{\partial \vec{k}_i}\right|} \times \left(\frac{\partial E\left(\vec{k}_i\right)}{\partial \vec{k}_i} \right)^2_{\varphi = \frac{\pi}{4}, \frac{\pi}{2}} \tau^{(i)} f(E)(1 - f(E)) \tag{2.81}$$

$n_s = \sum_i n_i$, n_i is the population of the subband i, and $\tau^{(i)}$ is the scattering rate in the *i-th* subband. It turns out that the mobility value evaluated in this simplified way coincides well with the one computed with the help of full quantum-mechanical non-equilibrium Green's function-based solvers employed to study transport in 14 nm FDSOI structures [2.366].

Scattering mechanisms are the most important physics ingredients determining the relaxation rates. The interface between silicon and oxide plays an important role in determining carrier transport. Small perturbations at the interface contribute to scattering. In ultra-thin films the importance of surface-roughness scattering increases due to the presence of two interfaces. The surface-roughness momentum relaxation rate is calculated after [2.298] as

$$\frac{1}{\tau_i^{SR}\left(\vec{k}_i\right)} = \frac{2\pi}{\hbar(2\pi)^2}\sum_j \int_0^{2\pi} \pi\Delta^2 L^2 \frac{1}{\varepsilon_{ij}^2\left(\vec{k}_i - \vec{k}_j\right)} \frac{\hbar^4}{4m_l^2} \frac{\left|\vec{k}_j\right|}{\left|\frac{\partial E\left(\vec{k}_j\right)}{\partial \vec{k}_j}\right|}$$

$$\times \left[\left(\frac{d\Psi_{i\vec{k}_i\sigma}}{dz}\right)^* \left(\frac{d\Psi_{j\vec{k}_j\sigma}}{dz}\right)\right]^2_{z=\pm\frac{7}{2}} exp\left(\frac{-\left(\vec{k}_j - \vec{k}_i\right)L^2}{4}\right) d\varphi \qquad (2.82)$$

$\vec{k}_i$ and $\vec{k}_j$ are the in-plane wave vectors before and after scattering, φ is the angle between $\vec{k}_i$ and $\vec{k}_j$, ε is the dielectric permittivity, L is the autocorrelation length, Δ is the mean square value of the surface-roughness fluctuations, $\Psi_{i\vec{k}_i}$ and $\Psi_{j\vec{k}_j}$ are the wave functions, $f\left(\vec{E}\right)$ is the Fermi function, and $\sigma = +/-1$ is the spin projection to the [001] axis.

The momentum scattering relaxation rate is calculated as

$$\frac{1}{\tau_i^{PH}\left(\vec{k}_i\right)} = \frac{2\pi k_B T}{\hbar\rho v_{PH}^2}\sum_j \int_0^{2\pi} \frac{d\phi}{2\pi} \frac{1}{(2\pi)^2} \frac{\vec{k}_j}{\left|\frac{\partial \vec{E}_j}{\partial \vec{k}_j}\right|} \left[1 - \frac{\left|\frac{\partial E\left(\vec{k}_j\right)}{\partial \vec{k}_j}\right| f\left(E\left(\vec{k}_j\right)\right)}{\left|\frac{\partial E\left(\vec{k}_i\right)}{\partial \vec{k}_i}\right| f\left(E\left(\vec{k}_i\right)\right)}\right]$$

$$\times 2\pi \int_0^t \left[\Psi^\dagger_{j\vec{k}_{j\sigma}}(z) M^{PH} \Psi_{i\vec{k}_{i\sigma}}(z)\right]\left[\Psi^\dagger_{j\vec{k}_{j\sigma}}(z) M^{PH} \Psi_{i\vec{k}_{i\sigma}}(z)\right] dz \times \theta\left(\vec{E}_i - \vec{E}_j\right) \qquad (2.83)$$

where the phonon velocity $v_{PH} = \frac{2v_{TA}+2v_{LA}}{3}$ [2.320], and the deformation potential $M^{PH} = 12$ eV [2.346].

The electron mobility enhancement along tensile stress in [110] direction is shown in Figure 2.79 as a function of the shear strain component. The mobility in

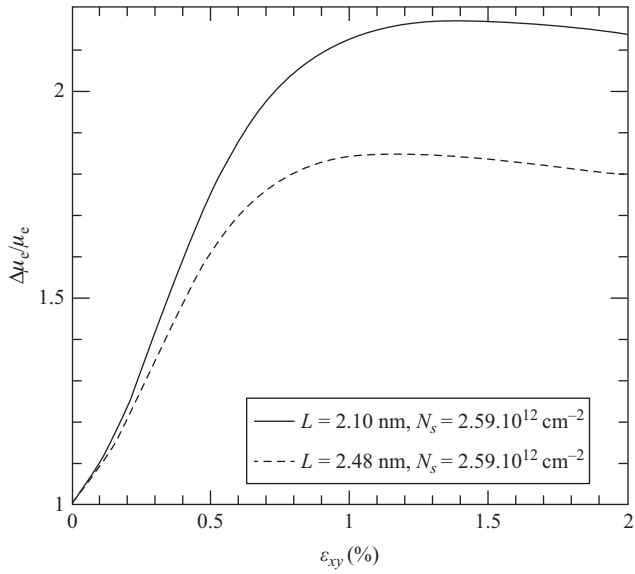

Figure 2.79 Electron mobility enhancement as a function of shear strain for two different film thicknesses at 300 K

thin silicon films at high stress increases by a factor of two as compared to its value in relaxed structures. The increase depends on the electron concentration and the film thickness. A strong mobility increase is observed up to 0.5% shear strain with a further saturation at higher strain value.

The mobility enhancement in silicon was previously explained by the effective mass reduction. However, the effective mass decrease only accounts for roughly one half of the mobility enhancement and cannot explain the two-fold mobility enhancement. Another contribution is the usually ignored dependence of the scattering matrix elements on strain. The electron–phonon scattering matrix elements do not display any substantial dependence on strain. On the other hand, the surface-roughness scattering matrix elements decrease strongly at higher strain values and account for the missing part in the mobility enhancement. As the total mobility is due to a combination of the surface-roughness and electron–phonon scattering limited mobilities, with the surface-roughness contribution becoming more pronounced in narrow structures, the total mobility enhancement is stronger in thinner films, in complete agreement with the simulations in Figure 2.79.

2.3.5.1 Spin lifetime enhancement in strained silicon films

The electron spin is another intrinsic physical characteristic of charge carriers in semiconductors. When injected into a non-magnetic material, the electron spin diffuses away from the spin accumulation region. In contrast to the electron charge, while diffusing the electron spin also relaxes toward its equilibrium value, which is

zero. The spin relaxation is characterized by the characteristic spin lifetime. In silicon the spin-flip scattering processes cause the spin relaxation. The small but finite probability to flip the spin after scattering is due to the fact that the wave function of an injected electron with a fixed spin projection is not the eigenfunction of the Hamiltonian because of the presence of the spin–orbit interaction. Therefore, to describe spin relaxation, it is necessary to know the spin-flip scattering rates and the spin–orbit interaction or, to be more specific, the wave functions in the presence of the spin–orbit interaction.

The spin-flip scattering rates due to the surface roughness and the electron–phonon interaction scattering are obtained in a way similar to the relaxation rates (2.82, 2.83) in the previous section [2.346]. The wave functions needed for the evaluation of the scattering matrix elements are obtained within the $\vec{k}\cdot\vec{p}$ formalism [2.364]. For the conduction band valleys along [001] direction relevant to describe the properties in (001) silicon films, the corresponding Hamiltonian written in the vicinity of the *X*-point at the Brillouin zoned edge is

$$\mathcal{H} = \begin{bmatrix} H_1 & H_3 \\ H_3^{\dagger} & H_2 \end{bmatrix} \tag{2.84}$$

where H_1, H_2, and H_3 are written as

$$H_1 = \begin{bmatrix} \dfrac{\hbar^2 k_z^2}{2m_l} + \dfrac{\hbar^2\left(k_x^2+k_y^2\right)}{2m_t} - \dfrac{\hbar^2 k_0 k_z}{m_l} + U(z) & 0 \\ 0 & \dfrac{\hbar^2 k_z^2}{2m_l} + \dfrac{\hbar^2\left(k_x^2+k_y^2\right)}{2m_t} - \dfrac{\hbar^2 k_0 k_z}{m_l} + U(z) \end{bmatrix} \tag{2.85}$$

$$H_2 = \begin{bmatrix} \dfrac{\hbar^2 k_z^2}{2m_l} + \dfrac{\hbar^2\left(k_x^2+k_y^2\right)}{2m_t} + \dfrac{\hbar^2 k_0 k_z}{m_l} + U(z) & 0 \\ 0 & \dfrac{\hbar^2 k_z^2}{2m_l} + \dfrac{\hbar^2\left(k_x^2+k_y^2\right)}{2m_t} + \dfrac{\hbar^2 k_0 k_z}{m_l} + U(z) \end{bmatrix} \tag{2.86}$$

$$H_3 = \begin{bmatrix} D\varepsilon_{xy} - \dfrac{\hbar^2 k_x k_y}{M} & \left(k_y - k_x i\right)\Delta_{SO} \\ \left(-k_y - k_x i\right)\Delta_{SO} & D\varepsilon_{xy} - \dfrac{\hbar^2 k_x k_y}{M} \end{bmatrix} \tag{2.87}$$

Here, ε_{xy} denotes the shear strain component, $M^{-1} \approx m_t^{-1} - m_0^{-1}$, $D = 14$ eV is the shear strain deformation potential, m_t and m_l are the transversal and the longitudinal silicon effective masses, $k_0 = 0.15X2\pi/a$ is the position of the valley minimum relative to the *X*-point in unstrained silicon, and $U(z)$ is the confinement potential.

The spin–orbit term $\tau_y \otimes \Delta_{SO}\left(k_x\sigma_x - k_y\sigma_y\right)$ with [2.333]

$$\Delta_{SO} = \frac{\hbar^2}{c^2 2m_0^3}\left|\sum_n \frac{\langle X_1|p_j|n\rangle\langle n|[\nabla V \times \vec{p}]_j|X_{2'}\rangle}{E_n - E_X}\right| \tag{2.88}$$

couples the states with the opposite spin projections from the opposite valleys. In the perturbation theory expression for Δ_{SO} E_n is the energy of the nth band at the X-point, E_X is the energy of the two lowest conduction bands X_1 and X_2' degenerate at the X-point, $\vec{p}$ is the momentum operator, V is the bulk crystal potential, σ_x, σ_y, and σ_z are the spin Pauli matrices, τ_y is the y-Pauli matrix in the valley degree of freedom, and c is the speed of light.

Strain and confinement are lifting the four-fold degeneracy of the nth unprimed subband by forming an n^+ and n^- subladder (the valley splitting). The degeneracy of the eigen states with the opposite spin projections $n \pm \Uparrow$ and $n \pm \Downarrow$within each subladder is preserved so that the wave function with an arbitrary spin projection can be constructed. When the spin injection direction is fixed, the degenerate states satisfy

$$\langle \Uparrow n \pm |f| n \pm \Downarrow\rangle = 0 \tag{2.89}$$

with the operators defined as

$$f = cos(\theta)\sigma_z + sin(\theta)\left[cos\,(\varphi)\sigma_x + sin(\varphi)\sigma_y\right] \tag{2.90}$$

where θ is the polar and φ is the azimuthal angle defining the orientation of the injected spin. Due to the spin–orbit interaction, the expectation value of the operator f computed between the wave functions from different subladders is non-zero

$$\bar{\bar{f}} = \langle \Uparrow n \pm |f| n \pm \Downarrow\rangle \neq 0 \tag{2.91}$$

In the two valleys' plus two spin projections' basis the subband wave functions possess four components. These wave functions are written as ($k_x = 0$)

$$|n - \Downarrow\rangle = \begin{pmatrix} \Psi_{1,1} \\ \Psi_{1,2} \\ \Psi^*_{1,1} \\ -\Psi^*_{1,2} \end{pmatrix} |n - \Uparrow\rangle = \begin{pmatrix} -\Psi_{1,2} \\ \Psi_{1,1} \\ \Psi^*_{1,2} \\ \Psi^*_{1,1} \end{pmatrix} |n + \Downarrow\rangle = \begin{pmatrix} \Psi_{2,2} \\ \Psi_{2,1} \\ -\Psi^*_{2,2} \\ \Psi^*_{2,1} \end{pmatrix} |n + \Uparrow\rangle = \begin{pmatrix} -\Psi_{2,1} \\ \Psi_{2,2} \\ -\Psi^*_{2,1} \\ -\Psi^*_{2,2} \end{pmatrix} \tag{2.92}$$

$|n \pm \Downarrow$ and $|n \pm \Uparrow$ are the up- and down-spin wave functions for the first (second) subband. Wave functions with opposite spin in the same valley are orthogonal.

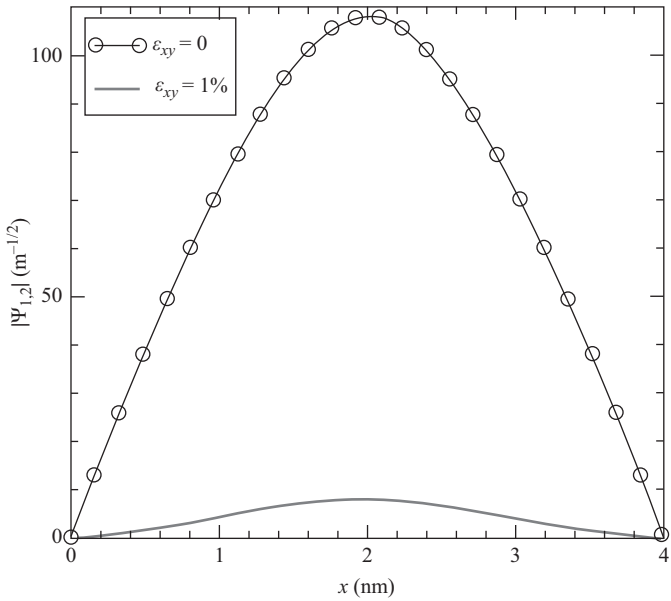

Figure 2.80 Spin–orbit interaction induced components of the wave function in relaxed film and in a film with 1% shear strain. The components are significantly reduced with strain

When the spin is injected along [001] direction, the dominant components are $\Psi_{1,1}$ and $\Psi_{2,2}$ for $|n \pm \Downarrow$ and $|n \pm \Uparrow$, respectively.

The small components of the wave functions are due to the spin–orbit interaction and thus proportional to the spin–orbit interaction strength. Shear strain ε_{xy} considerably suppresses these components as shown in Figure 2.80. Indeed, $\Psi_{1,2}$ for a strain value of 1% has almost vanished. Vanishing values of the small components reduce the spin mixing between the states with opposite spin projections, which results in longer spin lifetime. A significant spin lifetime increase in a silicon film under strain is shown in Figure 2.81. In contrast to the mobility, which is only enhanced by a factor of two, the spin lifetime increases almost exponentially by orders of magnitude. This makes silicon films perfectly suited for spin interconnects as uniaxial stress is now routinely used by the semiconductor industries to boost the MOSFET performance.

2.3.6 Quantum and quantum-corrected transport models

Quantum-mechanical effects influence the characteristics of modern semiconductor devices. Due to this fact, purely classical device simulation may not be sufficient to accurately reproduce all the details of transport. Size quantization of carrier motion in the confining potential of an inversion layer is the most investigated quantum-mechanical effect in modern MOSFETs. Because of the size quantization, the energy spectrum becomes discrete in the confinement direction, while it is still continuous

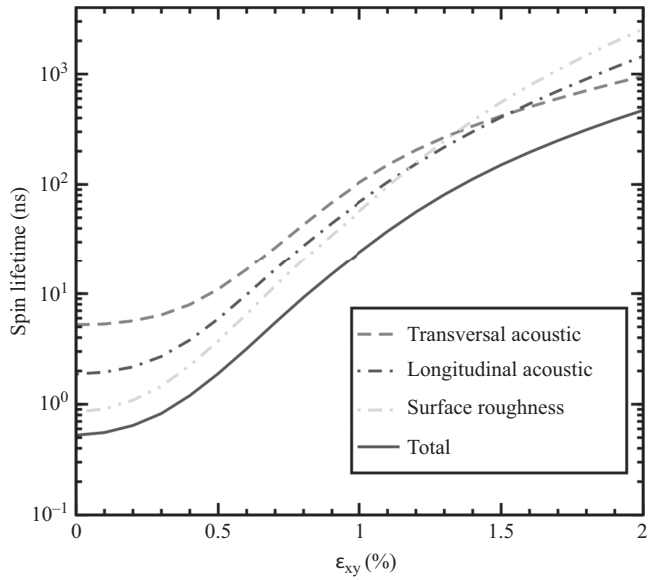

Figure 2.81 Spin lifetime enhancement by shear strain for $T = 300$ K, the film thickness $t = 2.1$ nm

along the transport direction. The three-dimensional energy band structure is partitioned into a set of two-dimensional subbands. In order to find the subband energy levels and the corresponding wave function, the Schrödinger equation has to be solved.

The potential entering the Schrödinger equation depends on the charge carrier density in the inversion layer. By knowing the wave functions and occupations of the subbands, the charge carrier concentration in the inversion layer can be obtained. Therefore, the potential has to be determined self-consistently by solving the Schrödinger equation and the Poisson equation simultaneously. This procedure is time-consuming and should be avoided whenever timely results must be obtained. One option is to exploit the well-established semi-classical transport models, while correcting them in such a way that they mimic the quantum-mechanical behavior [2.291, 2.312, 2.324, 2.344, 2.347].

The quantum correction that mimics the local density of states close to the interface can be interpreted as an additional quantum potential [2.294], which has to be added to the classical self-consistent potential in order to describe the decrease of carrier concentration at the interface correctly. Because this additional quantum potential enters into the current relations, it opens an opportunity to introduce quantum-mechanical effects into the drift-diffusion- and higher moments-based transport models. In fact, the appearance of the quantum potential can be easily illustrated, if one just substitutes the wave function represented as the product of the real amplitude and the exponent containing the phase factor

$$\psi(\vec{r},t) = A(\vec{r},t)exp(i\phi(\vec{r},t)) \tag{2.93}$$

into the Schrödinger equation. The density $n(\vec{r},t) = A^2(\vec{r},t)$, the velocity $v = \hbar\nabla\frac{\phi(\vec{r},t)}{m}$, and the current $\vec{j} = n\vec{v}$ are introduced and one obtains the following two equations [2.368]:

$$\frac{\partial n(\vec{r},t)}{\partial t} + \nabla[n(\vec{r},t)\vec{v}] = 0 \tag{2.94}$$

$$\frac{\partial \vec{v}}{\partial t} = \nabla\left(-\frac{v^2}{2} + \frac{q}{m}V(\vec{r},t) + V_{QC}(\vec{r},t)\right) \tag{2.95}$$

Here, the additional quantum correction potential $V_{QC}(\vec{r},t)$ is given by the following expression

$$V_{QC}(\vec{r},t) = \frac{\hbar^2}{2m^2}\frac{\Delta\sqrt{n}}{\sqrt{n}} \tag{2.96}$$

The form of the quantum potential (2.96) is commonly referred to as the density gradient correction and is extensively used in quantum hydrodynamic calculations [2.278, 2.281]. The expression for the current density including the quantum correction reads [2.283]:

$$\vec{J} = q\mu n\vec{E} + qD\nabla n - \mu n\frac{\hbar^2}{2mr}\nabla\frac{\Delta\sqrt{n}}{\sqrt{n}} \tag{2.97}$$

Here an additional parameter $r \geq 1$ is introduced.

Substitution of the current relation (2.97) into the continuity equation (1.41) results in a differential equation for the particle concentration n of fourth order. Such an equation needs two boundary conditions. If one considers the interface between the semiconductor and the dielectric, the first boundary condition is the standard one to set on the normal derivative of the concentration to zero required by the absence of the normal current component at the interface. The second boundary condition allows set the carrier concentration to zero at the interface simultaneously. Thus, the quantum drift-diffusion theory based on (2.97) supplemented with the corresponding boundary conditions automatically reproduces the concentration decrease at the interface, mimicking the quantum-mechanical behavior. A review of quantum hydrodynamic models is given in, e.g., Reference 2.322.

For numerical transport calculations it is convenient to avoid the discretization of the fourth order equation and to include the quantum potential correction term into a generalized electro-chemical potential [2.283]. After a careful calibration of the resulting density gradient model the transport calculations including source-drain tunneling in ultra-scaled MOSFETs becomes possible [2.283]. The density gradient formalism is successfully used for handling discrete charges in drift diffusion "atomistic" simulations [2.301]. It enables the comprehensive statistical investigation of the effects associated with charge trapping on the defects in a wide range of doping values for 20 nm CMOS bulk and 14 nm FinFET transistors

[2.277]. To justify the approach, an accurate calibration to the experimental data is required. A comparison with more sophisticated transport models is also needed.

An approach capable of handling both the quantum coherent propagation and dissipative scattering is based on the Wigner function formalism. The Wigner function is defined as the density matrix in a mixed coordinate/momentum representation [2.330, 2.371]. A practically used approximation to incorporate realistic scattering processes into the Wigner equation is to utilize a properly adapted Boltzmann scattering operator [2.327]. In this way well-established scattering models already calibrated within semi-classical transport approaches can be employed in quantum transport calculations. The inclusion of dissipation through the Boltzmann scattering operator, although intuitively appealing, raises some concerns about the validity of such a procedure. The Boltzmann scattering operator is semi-classical by its nature and represents a good approximation for sufficiently smooth device potentials.

The kinetic equation for the Wigner function is similar to the semi-classical Boltzmann equation, except for a non-local quantum potential term. In the case of a slowly varying potential this non-local term reduces to the local classical force term, and the semi-classical description given by the Boltzmann equation is obtained from the Wigner equation. This semi-classical limit of the Wigner transport equation allows link a semi-classical description of the extended contact regions with the quantum-mechanical description of the active region of a device using the same formalism [2.327].

Implementations of MC methods for solving the Wigner equation have been reported, e.g., [2.342, 2.359]. Recent advances in solving the Wigner transport equation by MC methods are reviewed in Reference 2.357.

To account for scattering more rigorously, spectral information has to be included in the Wigner function formalism, resulting in energy dependence in addition to the momentum dependence [2.338]. The non-equilibrium Green's function method addresses the quantum transport problem in a most consistent and complete way. However, the method is computationally complex. Scattering requires the knowledge of the corresponding self-energies and thus complicates computations significantly [2.364]. The self-consistent Born approximation for the self-energy is an extremely time consuming but necessary step, because it guarantees current continuity. The convergence of the self-consistent iteration is a critical issue, where fine resonances at some energies have to be resolved accurately [2.321, 2.351]. For that purpose an adaptive method for selecting the energy grid is essential [2.321, 2.351].

Nowadays atomistic quantum transport simulators designed for ultra-scaled CMOS and beyond CMOS device simulations are available, e.g., [2.340, 2.353]. They allow not only to compute the electron transport by using the material-dependent atomic parameters and scattering but even to obtain the parameters and currents from the first-principle density-functional calculations with specially designed exchange correlations [2.284]. Being able to accurately study realistic ultra-scaled devices these methods, however, are computationally demanding, as they require using several interacting complex simulation tools.

2.4 Alternative materials and device structures

2.4.1 Introduction

At the beginning of the twenty-first century, the International Technology Roadmap for Semiconductors has been accelerating the introduction of new and diverse technologies to extend the CMOS fabrication technology into nanoscale MOSFET structures [2.373]. Since then, rather than replacing CMOS the new materials and devices have been combined with a CMOS platform to extend microelectronics to new applications domains not accessible at that time to CMOS technology alone [2.374]. However, device cost and performance will continue to be strongly correlated to dimensional and functional scaling of CMOS as information processing technology is driving the semiconductor industry into a broadening spectrum of new applications according to 2013 ITRS [2.375]. Not only the continuation of the Moore's Law is the driver for the search of new materials, in the early 2000s was invented the term More than Moore (MtM) to stress the fact that the value of a packaged system doesn't rely only on the performance of the CMOS technology for the digital information processing, but also on diversified technologies which doesn't necessarily perform better through a dimensional scaling. MtM is the other facet of the microelectronic products complementing the digital part of the integrated systems. More specifically the MtM approach allows for the non-digital functionalities of a product – which do not necessarily scale according to Moore's Law, but provide additional value in different ways – to migrate from the system board-level into the package (SiP) or onto the chip (SoC) [2.376]. As it is pointed in the 2013 ITRS, because the More than Moore domain is multidisciplinary, involving expertise from many different areas, such as electrical and mechanical engineering, materials science, biology and medical science, the search of new and compatible materials with the silicon fabrication technology is now a short-term goal that needs to be fulfilled.

Strained silicon, high-k dielectrics, metal gate, multigate transistors, Ge, SiSe, and II-V semiconductors are now used in IC manufacturing based on the promise of high mobility. All of these triggered the emerging research on completely new transistor operating and new materials. Nanoelectronics is now the common place for the future of the ICs. With a mix of chemistry, physics, biology, and engineering, nanoelectronics may provide a solution to increasing fabrication cost and may allow ICs to be scaled beyond the limits of modern transistors [2.377]. However, the fabrication methods that this approach requires are still waiting for a breakthrough for its implementation in mass production. Nevertheless, the devices that that will be used in the nanoelectronic circuits as well as the new materials to build them are being developed and, among the most popular proposals we can mention the following:

Carbon nanotube (CNT). Are cylindrical carbon molecules that exhibit unique and interesting physical properties including current carrying ability, long ballistic transport length, high thermal conductivity, and mechanical strength [2.378]. The carbon nanotube field-effect transistor (CNFET) is one possible candidate for future high-performance nanoelectronics, because it has near ballistic

transport at room temperature, tight electrostatic control on its 1D channel, which provides superior speed and reduced SCEs, as a consequence, it may enable further downscaling [2.379]. By developing noise and manufacturing process variability to the Stanford CNFET compact model in reference the authors predicted that the CNFET devices would outperform Si-CMOS in RF applications in terms of the requirements of the International Technology Roadmap for Semiconductors. However, the current fabrication technology for CNFET are still affected by several shortcomings, it is not possible to provide exact control over CNT diameter and doping, or the removal of tubes with metallic behavior [2.380].

Graphene. Since its discovery in 2004 [2.381], it has been proposed as replacement for silicon in MOSFET for high-frequency applications mainly because its high field effect mobility (close to 10,000 cm^2/Vs at room temperature) [2.382]. Graphene is a two-dimensional material with sp^2 structure that has many excellent physical properties such as extremely high intrinsic carrier mobility, ultra-thin body, long mean-free-path, great thermoelectric property and stability. An excellent summary of the physics, chemistry and engineering of this marvelous material may be found in Reference 2.383. Graphene also suffers from major drawbacks; the most prominent is that is a zero band gap material, which results in small on/off current ratio and no stable saturation region in the output characteristics of transistors made on this material [2.384]. Nevertheless, the search of a graphene FET has not ended but up to this time, they appear with a high off-state leakage current and lack of drive current as a consequence of the gapless band structure. Among all the strategies for producing Graphene, CVD on transition metals substrates seems to be the most promising approach to produce large area and inexpensive materials. In spite of all the developments in the deposition of graphene, there still important challenges to be solved [2.385]: First of all, synthesizing graphene with large and controlled grain size would be very important for various electronic applications. For instance, is it possible to grow single-grain graphene of centimeter or even wafer scale size? Second, controlling the number of layers and stacking order of graphene is also very important, as bilayer and trilayer graphene may offer functions and properties different from monolayer graphene. In addition, growing graphene directly on insulating substrates such as Si/SiO_2 and h-BN would help to overcome the quality degradation caused by the transfer process. Furthermore, low temperature graphene growth will be attractive to reduce the cost and may enable the direct growth on flexible polymer-based substrates. From the aforementioned, one of the possible route for graphene devices is to complementarily integrate them with the CMOS ICs or systems in order to supply more functionality to the silicon technology as an active element in the MtM area. In this respect Huang [2.386] has demonstrated the integration of a graphene Hall sensor with the CMOS amplifier in a silicon chip. So far this is tone of the approaches for incorporating graphene to the silicon mainstream technology and for building system in package.

Nanowires (NW). Semiconductor NWs have attracted considerable attention because its improved electrostatic control in the cylindrical geometry by using wraps gates [2.387], and because they offer the possibility have including heterostructures in transistor design [2.388]. Although many different types of semiconductor NW

have been investigated, silicon NWs have become prototypical NWs because they can be readily prepared, the Si/SiO2 interface is chemically stable, and Si NWs are utilized in a number of device demonstrations that have well-known silicon-technology-based counterparts [2.389]. The Si nanowire FET (SiNWFET) has already been demonstrated in continuing with the scaling of the transistor and, seems to be a better alternative than the CNFET because it always is a semiconductor independently of the diameter. When used for FET fabrication they have demonstrated, by comparing it with a SOI FET scaled to the NW dimensions that the SiNWFET has larger on-state current and the average subthreshold slope approaches the theoretical limit and the average transconductance is up to ten times larger [2.390]. In particular epitaxially grown silicon (Si) NWs are considered as promising candidates for post-CMOS logic elements owing to their potential compatibility with existing CMOS technology. One major advantage of vapor-liquid-solid (VLS) grown NWs compared to top-down fabricated devices is that they have well-defined surfaces. This reduces surface scattering, an issue that becomes important for devices on the nanoscale. Moreover, epitaxially grown NWs circumvent the problem of handling and positioning nanometer-sized objects that arise in the conventional pick-and-place approach, where devices are fabricated by manipulating horizontally lying VLS-grown NWs. In this respect, a generic process flow to fabricate silicon NW vertical surround-gate FETs has been demonstrated; the intrinsic advantage of the process developed is that no chemical or mechanical polishing steps, which are difficult to control at this length scale, are needed [2.391].

Because the growth of NWs is a bottom-up self-assembly process, it brings an additional benefit to all of the aforementioned: then freedom in materials design where highly perfect heterostructures like In/InP, InAs/InSb, and Si/Ge may be formed [2.388], combination of materials that cannot be realized by the conventional top down techniques because the constraint of lattice matching. The incorporation of vertically integrated NWFET may enable the implementation of 3D CMOS ICs.

Gallium Nitride (GaN). The excitement generated about GaN stems from its unique material and electronic properties. GaN devices offer five key characteristics: high dielectric strength, high operating temperature, high current density, high speed switching, and low on-resistance. These characteristics are due to the properties of GaN, which, compared to silicon, offers ten times higher electrical breakdown characteristics, three times the bandgap, and exceptional carrier mobility. But this material offers yet more advantages, the high electron mobility and charge density possible in AlGaN/GaN and InAlN/GaN heterostructures has enabled the demonstration of power amplifiers with at least one order of magnitude higher output power density than in their GaAs or Si-based counterparts. However, in spite of this excellent performance, nitride-based devices cannot compete with Si CMOS electronics in terms of cost, scalability, and circuit complexity. The seamless integration of these two semiconductor families would give the circuit and system designer unprecedented flexibility to use the best material and devices for each function [2.392]. A fabrication technique for the manufacturing GaN on Si power devices and the heterogeneous integration with Si devices has been demonstrated for 4” Si wafer [2.392] and for 8” wafer substrates [2.393].

So far, we have dealt with the materials that the main stream of research has considered for increasing the performance of the Si technology, but recently and offering new functionality to this technology the polymers and small molecular thin films have emerged refreshing the materials catalog. The main advantage that makes these materials very attractive is their low deposition temperature. In addition to that, the possibility of tailoring the properties of the films by using multicomponents organic semiconductors [2.394] is a new area of research for obtaining new functionalities in the Si technology. For instance, light emission to the Si technology has already been demonstrated [2.395] and is only an example of all the new functionalities that can be added to CMOS chips.

2.4.2 Nanostructured materials, amorphous and SiGe alloys, and its applications

We all are used to the SiGe in the HBT fabrication and as a strained layer in the CMOS technology. HBT fabricated with SiGe heterojunction in the BiCMOS technology show a performance that is superior to its III–V counterparts. The addition of Carbon to SiGe opened new capabilities to the HBT performance and is very important step in the strained-layer epitaxy for this application. An excellent review of these applications can be found in the books edited by John D. Cressler [2.396]. However, the use of amorphous SiGe alloys or nanostructured materials that are obtained from Plasma Enhanced Chemical Vapor Deposition (PECVD) are "structure sensitive" amorphous material because a perplexing diversity of structures and properties can result depending upon the preparative processes and conditions [2.397]. But, what are the advantages or novelty in incorporating amorphous or nanostructured materials obtained from PECVD? In answering the question we will follow the discussion given by Street [2.398]:

> The disorder is the main feature that distinguishes amorphous from crystalline materials. This is of special significance in semiconductors, because periodicity of the atomic structure is central to the theory of crystalline semiconductors. Bloch's theorem is a direct consequence of the periodicity and properly describes the electrons and holes by wave functions, which are extended in space with quantum states defined by the momentum. The theory of lattice vibrations has similar basis in the lattice symmetry. The description of amorphous materials is developed instead from the chemical bonding between atoms, with emphasis on the short range bonding – that is in the bond length and bonding angle – rather than in the long-range order (periodicity). This structural disorder influences the electronic properties in several different ways are summarized in the following text.

Bonding disorder. The disorder represented by deviations in the bond lengths and bond angles broadens the electron distribution of states and causes electron and hole localization as well as strong scattering on the carriers.

Structural defects. Such as broken bonds have corresponding electronic states which lie in the band gap, here the emphasis on the local bonding rather than the long range translational symmetry leads to a strong interaction between the electronic and structural states and causes the phenomenon of metastability.

Electronic properties. The wave functions of the electronic states are the solutions to the Schrödinger equation, the periodic potential of the ordered crystal leads to the familiar Bloch solutions. The wave function has a well-defined momentum that extends through the entire crystal. The energy bands are described by energy-momentum dispersion relations, which, in turn, determine the effective mass, electronic excitations, etc. The aforementioned solutions to Schrödinger equations do not apply to an amorphous semiconductor because the potential is not periodic. A weak disorder potential results in only a small perturbation of the wave function and has the effect of scattering the electron form one Block state to another. The disordering effect of an amorphous semiconductor is strong enough to cause such frequent scattering that the wave function loses phase coherence over a distance of one or two atomic spacing. This strong scattering causes a large uncertainty in the electron momentum trough the uncertainty principle; the uncertainty in the moment is similar to the magnitude of the moment and therefore is not a good quantum number and is not conserved in electronic transitions. The loss of momentum conservation is one of the most important results of disorder and changes much of the basis description of the electronic states. Some consequences of the loss of momentum conservation are listed as follows.

- The dispersion relations do not longer describe the energy bands, but instead also a density of states distribution must redefine the electron and hole effective masses redefined as they are usually expressed as the curvature of the dispersion relations.
- The conservation of momentum selection rules does not apply to optical transitions in amorphous semiconductors. Consequently, the distinction is lost between a direct and an indirect band gap, the later being those transitions which are forbidden by momentum conservation. Instead transitions occur between states that overlap in real space. This distinction is most obvious in Si, which has, and indirect band gap in its crystalline phase but not in the amorphous phase.
- The disorder reduces the carrier mobility because of frequent scattering and causes the much more profound effect of localizing the wave function.

If we try to do a balance of the opportunities offered from amorphous materials, we will be tempted to refuse its incorporation to the CMOS technology. But, looking carefully we find that because the deposition method a perplexing diversity of structures and properties can result depending upon the preparative processes and conditions. We are actually, by changing the depositing conditions, tailoring the density of defects, the band gap and therefore creating new materials from the same components. Additionally, the lack of conservation of the momentum also brings the benefit of not influence of the lattice constant, which results in that all possible ratios among elements of a compound can be achieved.

As an example of the above asseveration, the properties of a-SiGe:H are presented below and we will see the influence of the depositing conditions on the properties of the deposited semiconductor [2.399–2.401]. The samples of amorphous silicon germanium films were prepared by LF PECVD decomposition using a PECVD system from Applied Materials Inc. (Santa Clara, CA), Model 3300. Silane,

SiH_4, and germane, GeH_4, were used as the feed gases and hydrogen and argon as the dilution gases. Two different substrates were used: Corning 1737 glass for the conductivity measurements and crystalline silicon (c-Si) for the measurements of infrared (IR) spectra. The films were deposited at substrate temperature $T_s = 300$ °C. The deposition parameters were as follows: pressure, $P = 0.6$ Torr; power, $W = 350$ W; and frequency $f = 110$ kHz. The total flow of silane and germanium $Q_{SiH4,GeH4}$ was 50 sccm for all depositions. Three types of the samples were fabricated: 20:1 hydrogen dilution (H-dilution), 10:1 argon dilution (Ar-dilution), and undiluted.

Depending on the gas dilutor the growth rate of the films changes for X ranging from 0 (pure Si) to 1 (pure Ge). As is depicted in Figure 2.82, the growth rate increases monotonically with X for dilution, while for dilution at low X values the growth rate suffers changes in opposite direction.

But not only the growth rate depends on the depositing conditions, the spectral dependence of the optical absorption coefficient $\alpha(h\nu)$ is shown in Figure 2.83a for all the samples studied along with that for a-Si for comparison. As can be seen, $\alpha(h\nu)$ curves shift to lower photon energy with increasing Ge content in the feed gas. The total shift is about 0.9 eV when Y changes from 0 to 1. The shift is not proportional to Y; nearly half of the total shift occurs in the low Y region between $Y = 0$ and $Y = 0.42$. The effect of dilution is rather pronounced for $Y = 0.23$ to 0.6; the films deposited with H-dilution are shifted more than the others. Also the

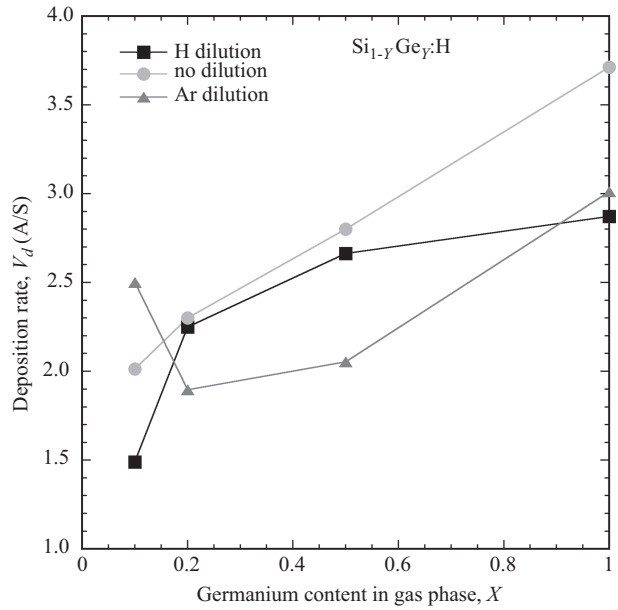

Figure 2.82 Deposition rate as a function of X, the Ge content in the feed gas, defined as the flow gas ratio $X = Q_{GeH4}/Q_{SiH4+GeH4}$

optical gap decreases linearly with Ge content to as small E_g in the range 0.95–0.95 eV for a-Ge as it is shown in Figure 2.83b.

The temperature dependence of the conductivity in the films $\sigma(T)$ is described by an activation dependence

$$\sigma(T) = \sigma_0 \exp\left(-\frac{E_a}{kT}\right) \tag{2.98}$$

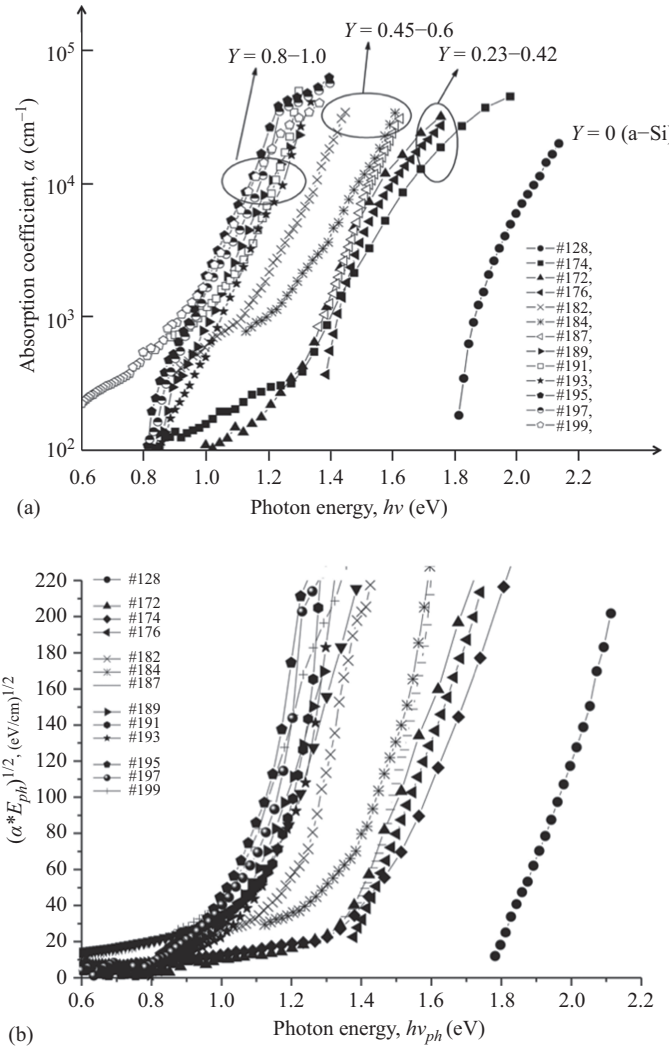

Figure 2.83 Spectral dependence of optical absorption coefficient: (a) α(hv) and (b) Tauc plots of the $Si_{1-Y}Ge_Y$:H films deposited from the gas mixtures with different Ge-content Y and different dilutions

where E_a is the activation energy determined from the slope of the experimental curves logs versus $1/T$. Figure 2.84 shows the measured conductivity of the films; we can see that Ge incorporation significantly changes conductivity of the films. Room temperature (RT) conductivity increases from $s_{RT} = 2 \times 10^{-8}$ at $Y = 0$ to $2 \times 10^{-1}\ \Omega^{-1}\text{cm}^{-1}$ at $Y = 1$, i.e., by seven orders of magnitude while for the same range of change in Y, the E_a changes from 0.60 to 0.22.

Also de deposition parameters influence the surface morphology and grain-like structures are observed trough an Atomic Force Microscope. Average height roughness, $<H>$, height distribution $F(H)$, lateral correlation length, L_c, and kurtosis, γ, were calculated from the AFM images and studied as a function of the Y content of Ge in the films. Figure 2.85 shows the average height $<H>$ for the different gas dilutions. As it can be observed, the average roughness increases from no dilution to hydrogen dilution and the highest roughness is obtained from Ar dilution. By increasing the hydrogen dilution rate the deposited films result in micro- and nano-crystallites [2.374]

By changing the dilution rate in the SiGe film deposition there is also a change in the structure and electronic properties of the deposited material. Defining the Hydrogen dilution parameter as $R = (Q_{\text{H2}})/(Q_{\text{SiH4}} + Q_{\text{GeH4}})$, where the flows $Q_{\text{SiH4}} = 25$ sccm and $Q_{\text{GeH4}} = 25$. The depositing conditions in addition of maintaining these flows constant are: pressure $P = 0.6$ Torr, RF Power = 300 W, discharge frequency $f = 110$ kHz, and a substrate temperature $T_s = 300\ ^{\text{o}}\text{C}$. R was varied from 20 to 80 and in order to characterize optical properties an optical gap E_{04}, a characteristic energy E_{03} determined as the photon energy at which absorption $\alpha(E_{04}) = 10^4\ \text{cm}^{-1}$ and $\alpha(E_{03}) = 10^3\ \text{cm}^{-1}$, respectively, are used, in addition to $\Delta E = E_{04} - E_{03}$ which reflects the density of band tail states, a plot of the optical

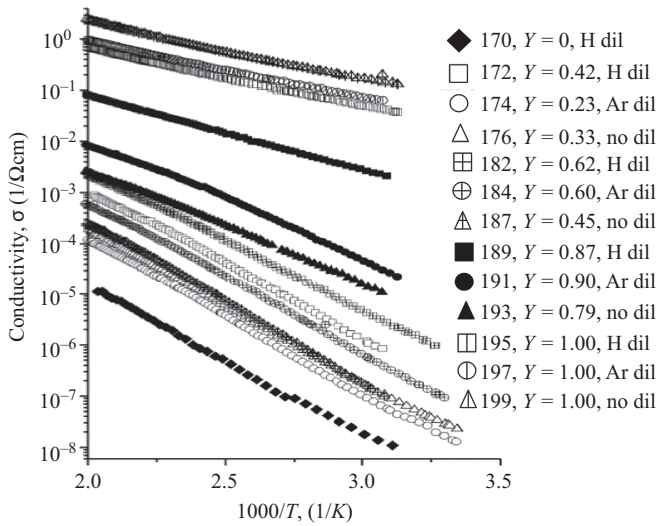

Figure 2.84 Temperature dependence of conductivity σ(T) for the SiGe films deposited with the various Ge content Y and dilutions

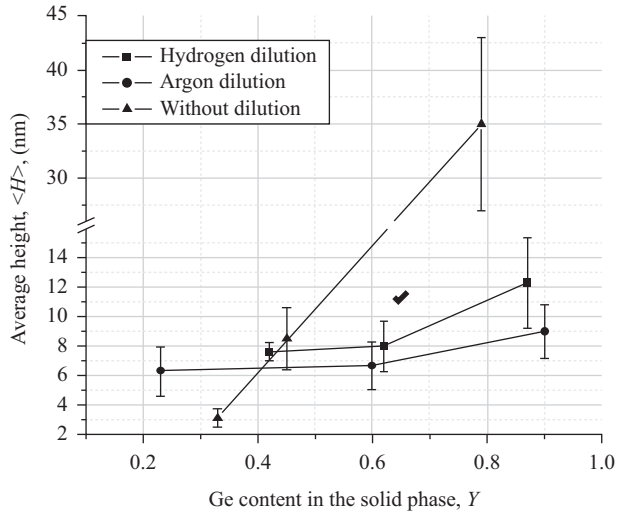

Figure 2.85 Average height as a function of Ge content, <H> for different gas dilutions. The films were deposited on Si substrates. Solid lines are just guides for the eye

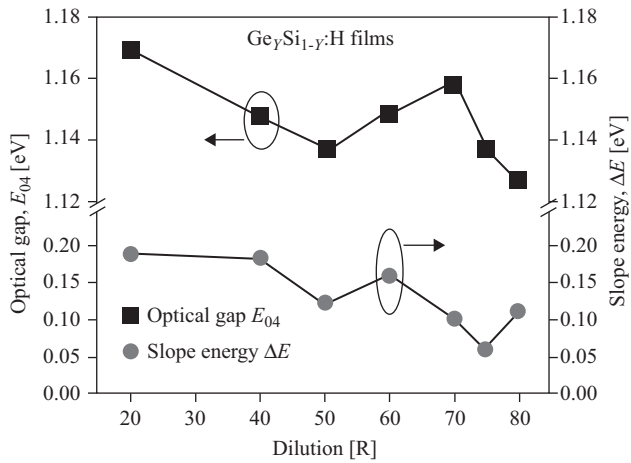

Figure 2.86 Optical gap, E_{04}, and slope energy, ΔE, as a function of hydrogen dilution in Ge_YSi_{1-Y}:H (b) films

gap versus dilution rate R is built and we can see this dependence and its corresponding change in ΔE. Figure 2.86 shows this dependence.

So far we have shown how the depositing conditions can produce a great variety of materials, here the case of SiGe:H alloys was used, but still many other

aspects in which the same alloy may be deposited by PECVD resulting in a material that gives new and surprising properties [2.402].

2.4.3 Photodetectors and micro-machined bolometers

The major factor limiting the properties of amorphous semiconductors is the density of defects in the energy gap. But we have seen in the precedent paragraph that it is possible by controlling the depositing conditions, to control the density of defects and, therefore, controlling the semiconductor properties. In the following text, we will show how the SiGe:H alloy by just changing the depositing conditions, it can be used in a variety of devices with an excellent advantage, that it can be added by post-processing to the CMOS fabrication technology without affecting the performance of the CMOS ICs.

A planar amorphous SiGe:H SAMAPD [2.403, 2.404]. For optical fiber communications, the Separated Absorption and Multiplication Avalanche Photodetector (SAMAPD) is fabricated on III–V semiconductor because the useful wavelength lies in the range of 0.9–1.55 nm. The quantum efficiency of these devices is determined by the properties of the absorption layer and the hetero-interface, while the avalanche multiplication process in the wide bandgap semiconductor determines the multiplication and excess noise properties. When the SAMAPD idea is exported to silicon, two major facts make this highly attractive: (1) the ionization coefficient ratio in Si is largely different from unity, which will result in low excess noise factor, and (2) the absorption coefficient of amorphous Si is very large compared to its crystalline counterpart. For the absorption layer of the SAMAPD, amorphous silicon (a-Si) and its alloys (a-SiGe) are a good option because they show at least one order of magnitude higher absorption coefficient with respect to crystalline material. Additionally amorphous materials have a very low deposition temperature (when PECVD is used), and do not contain any materials harmful to Si IC's fabrication processing. a-Si and a-SiGe alloys, used as absorption layers in a SAMAPD structure, do not need to have smaller band gap than the crystalline silicon, as in III–V-based APDs. Because a-Si and its alloys have optical absorption coefficients larger than 10^4 cm^{-1} (for energies 0.2 eV larger than the optical gap), for most optoelectronic applications, only a 1 mm thick absorption layer is sufficient which is two to three orders of magnitude thinner than that needed in crystalline silicon. One of the important characteristics of amorphous materials is that materials of arbitrary composition can be obtained.

A cross-section of the a-SiGe SAMAPD, fabricated in an n-type Si wafer (100), $r = 3$–5 Ω-cm of the INAOE 10-μm-CMOS IC's process, is shown in Figure 2.87. Only one extra p implantation step is required to prepare the substrate for the SAMAPD fabrication, and the IC's fabrication process is not altered. The p implantation is done with a dose of 2×10^{12} cm^{-2} at 150 keV. With this implantation the p-region of the p–n multiplication-junction is formed. The n^+ contact as well as the p region described earlier, are activated with the same heat treatment used in the formation of the source and drain regions. An a-SiGe:H from SiH_4 and GeF_4 as sources and doped with boron was deposited at 250 °C and a pressure of 0.8 Torr. The deposited film resulted a-$Si_{0.67}Ge_{0.33}$:H,F with an optical bandgap = 1.33 eV, a

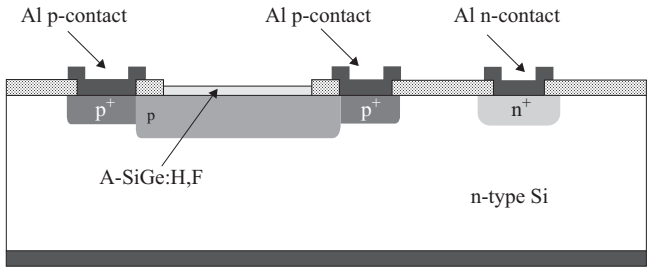

Figure 2.87 Cross-section of the a-SiGe:H,F SAMAPD and the surface n^+ contact to the n-type substrate. The junction depth of the n^+ and p^+ regions is 1.5 mm. The active window of the a-SiGe regions is 100 × 100 μm²

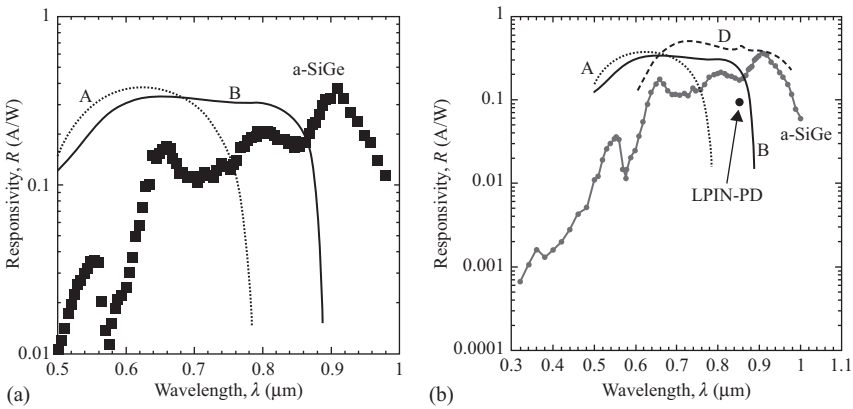

Figure 2.88 (a) Experimental responsivity R of the a-SiGe:H,F SAMAPD versus wavelength at $V_d = 0$ V, with a-SiGe:H,F thickness layer of 0.065 mm. The experimental results of a super lattice GaAs-$Al_{0.4}Ga_{0.6}As$ photo diode are also shown by the continuous lines. Curve A corresponds to 30 GaAs/AlGaAs periods of 46/48 angstroms thick, and curve B is for 30 GaAs/AlGaAs periods of 139/84 angstroms thick. A spectrophotometer is used to sweep the device from 0.3 to 0.9 mm, and a coherent ring laser is used on the 0.9–1.0 μm wavelength range. (b) Device response with AR coating (D)

diffusion length of 0.08 mm and a lifetime of 769.6 μs. Therefore a film thickness of 0.08 will avoid the risk of recombination inside the absorption layer. The addition of an antireflective (AR) coating helps to increase the performance of the device. The AR films Spin on Glass cured at 200°C in order to maintain the properties of the absorber material. Figure 2.88 shows (a) the device responsivity plotted as function of the incident wavelength and (b) with the AR deposited.

So far, an IC-compatible a-SiGe planar SAMAPD, suitable for optical communications when AlGaAs laser source is used, has been demonstrated. Its simple fabrication technology, the gain that can be obtained when operated in avalanche and the ability of tailoring the absorption layer characteristics, makes this device very attractive for Si optoelectronic IC fabrication.

MSM thin film high speed photodetector [2.405]. For the development of low-cost optical receivers for optical communications, the silicon technology has emerged as the best choice because its maturity, very well-developed fabrication process and lower fabrication cost for mass production. In order to obtain the proper absorption coefficient for the second and third fiber spectral windows (1.3–1.55 μm), the use of thin films of materials with the proper characteristics have been used. For operation at the wavelengths of 1.3 and 1.55 μm, it is proposed in this work the use of a-SiGe:H,F. On this material a MSM photo detector is constructed, and this structure was chosen because its inherent lower parasitic capacitance, hence a lower RC delay time and very simple fabrication process, because only a single mask is required. For operation at high speed the use of the transient photocurrent in amorphous hydrogenated semiconductors [2.406] is proposed. The transient photocurrent mechanism can be understood in terms of the large density of localized band tail and midgap states of the amorphous semiconductors. Therefore, the transport of carriers involves the frequent trapping, detrapping, and motion (transport in extended sates). When a photoconductive detector is built on such material, and then is illuminated by a light pulse, a photocurrent is generated. Two factors can reduce the free carrier density and cause photocurrent decay. If recombination happens, then a free carrier is lost, thus the photocurrent will be reduced, which happens when the carrier falls in a deep trap. However, when the carrier falls into a shallow trap it is reemitted soon after capture and a rapid decay is observed in the short period time of picoseconds. Physically this decay corresponds to the initial thermallization of the electrons in shallow states (tail states). Since the density of tails state is high near the band gap, the transient photocurrent decay is very fast. After this initial decay, the photocurrent decays gradually for a time, until deep trapping causes another sharp drop. Therefore, the initial thermallization or the deep trapping decay can be used to achieve a short response time of a device. The response time of the device can be adjusted between 1 and 100 ps for the initial thermallization decay. A material with a high density of midgap sates should be used for a short response time, and this condition can be achieved easily by adjusting the depositing conditions of an amorphous semiconductor. The fabrication process of an MSM is described as follows: As a starting material Si wafers of 2 in diameter were used as a mechanical support. After standard cleaning procedures were performed on the wafers, a SiN_x film was deposited by means of a PECVD system under the following deposition conditions: RF power 250 W, 0.6 Torr of pressure, deposition temperature of 260°C. Gases used are SiH_4, NH_3, and N_2. Thickness measured 105 nm. Without opening the deposition chamber, the temperature of the PECVD system was raised to 300°C to perform the a-SiGe:H deposition. GeF_4, SiH_4, and H_2 were used as the reactive gasses. An RF power of 200W was applied and the pressure of the system was 0.5 Torr.

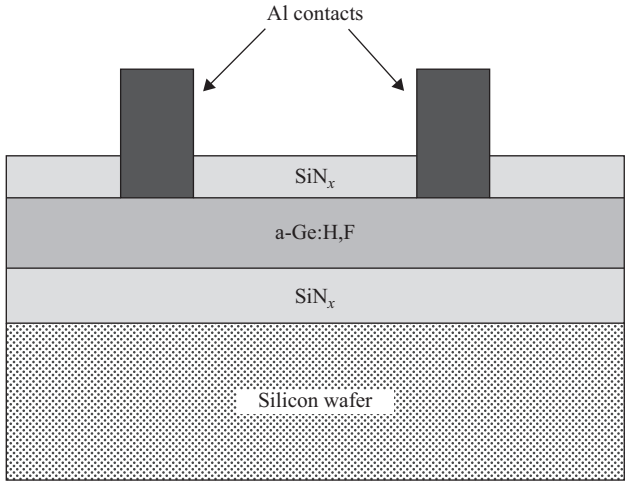

Figure 2.89 Cross-section of the fabricated device

The resulting thickness was 0.3 μm. Then, a second SiN_x layer of the same thickness as the first isolation layer is deposited on top of the a-Ge to act as an anti-reflecting layer. A finger mask containing different sizes and arrays of fingers is then placed on top of the system SiN_x/a-Ge:H,F/SiN_x, using positive photoresist, then the uncovered SiN_x is removed and a layer of Al is evaporated on the photoresist. By removing the photoresist, the finger pattern is placed on top of the a-SiGe. No alloying process for the metal contact to the amorphous layer was performed. A cross-section of the fabricated structure is depicted in Figure 2.89.

The devices were measured under DC bias in the range of ± 3 V under dark and illuminated conditions. The highest dark current measured at 3 V was 2.4×10^{-8} A, for the device with dimensions for the interdigitated area as 260 μm long, separation between fingers 40 μm and finger width 22 μm. When the device is illuminated with different monochromatic sources, it is noticed that as the wavelength increases, the photo generated current also increases. Figure 2.90 shows this behavior. It is seen that for a $\lambda = 0.94$ μm there is almost 2 orders of magnitude in current increase with respect to the dark case, and up to 3 orders of magnitude in the increase of the photo generated current when $\lambda = 1.06$ μm. The observed behavior is in agreement with the transmittance measurements performed on a sample of the system SiN_x/a-Ge:H,F/SiN_x in which no metal deposition was done. Figure 2.91 shows the measured transmittance.

In order to have an idea of the temporal response of the fabricated detector, the device was illuminated by means of a pulsed laser that delivers light pulses of 10 ns at 1060 nm of wavelength. An incident power of 4 mW was used to shine the detector without any bias that is in photovoltaic mode. The generated voltage across the detector was measured by means of an oscilloscope. The load for the probes was 50 W. The time scale that is shown in Figure 2.92 is not related to the pulse duration;

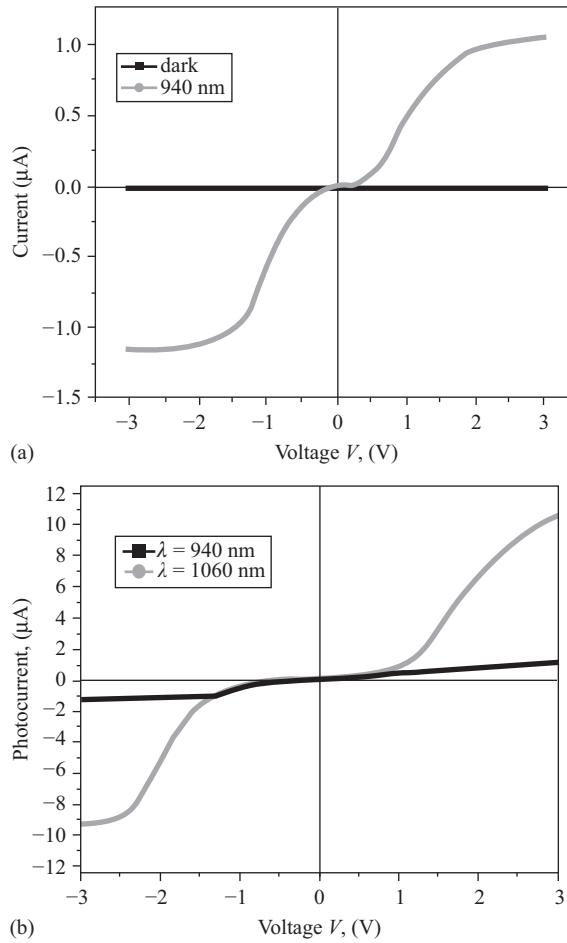

Figure 2.90 Dark and illuminated behavior of the MSM, (a) for illumination at $\lambda = 940$ nm, (b) for illumination at $\lambda = 940$ and 1060 nm

instead it represents the time-scale for the sampling rate (1.54 G samples/s). The measured characteristics under dark and illuminated conditions show that at only 3 V is necessary for the proper performance of the devices. Bias that agrees with the low power consumption requirements of the modern ICs. The device here presented has shown a good response for light pulses of 10 ns of duration.

Microbolometers. For IR imaging the thermal detector that has allowed the fabrication of cameras and video cameras of large format is the microbolometer. The operation of a microbolometer is based on the temperature rise of the thermo-sensing material by the absorption of the incident IR radiation. The change in temperature causes a change on its electrical resistance, which is measured by an external circuit. Microbolometers based on amorphous semiconductors have

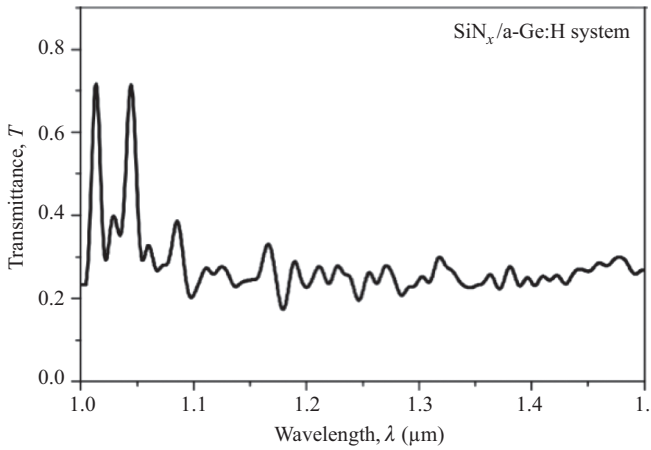

Figure 2.91 Transmittance measured on the system SiN_x/a-Ge:H,F/SiN_x in the range of 1–1.5 mm

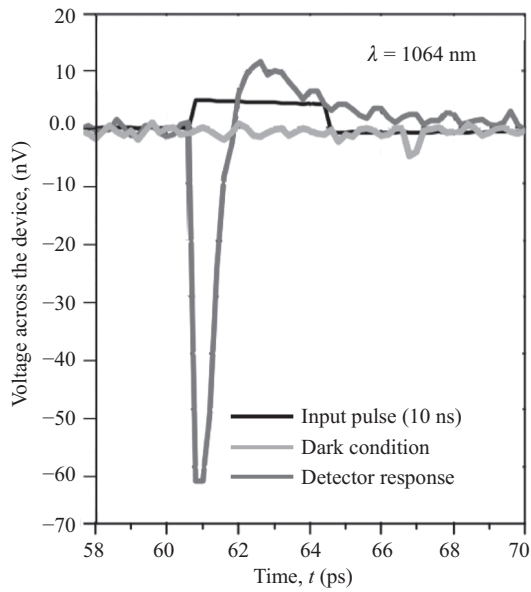

Figure 2.92 Response of the MSM to a 10 ns pulse of λ = 1.064 mm

advantages over other types of thermal detectors, including microbolometers that use other kind of thermo-sensing materials. The advantages are mainly technological, since these microbolometers are fully compatible with silicon CMOS fabrication technology, and there is no need of additional fabrication equipment in

an IC production line as they are relatively of simple fabrication and can be processed at relatively low temperature by PECVD. The latter makes them ideal for a post-process fabrication over a CMOS read-out circuit. At INAOE we have been working on the materials for application of these devices from wavelengths ranging from 10 to 1 mm. But regardless of the wavelength of interest, the key parameter that determines the responsivity is the temperature coefficient of resistance (TCR). The TCR is commonly represented by $\alpha(T)$, which is defined as

$$\alpha(T) = \left(\frac{1}{R}\right)\left(\frac{dR}{dt}\right) \approx \frac{E_a}{kT^2} \tag{2.99}$$

where E_a is the activation energy, k the Boltzmann constant, and T. A large TRC value means that a small temperature change will result in a large change in the resistance of the material. a-Si:H and a-SiGe:H happen to be the set of materials that, by the proper depositing conditions, are able to cover the range of the IR spectra aforementioned.

Uncooled microbolometer. The device is a temperature-dependent resistor working at room temperature, which contains an IR absorbing film deposited on a thermosensing element. Those films are supported by a suspended membrane, which provides thermal isolation. The devices may be fabricated by using bulk micromachinining or through surface micromachining; the former is used for obtaining a better thermal isolation by placing the device on a floating thermal isolator. The later is used when an array of devices is required for getting the larger number of devices for a giver area of silicon, besides that this configuration allows to fabricate under it the conditioning circuitry for every pixel in a focal plane array [2.407]. These two configurations are illustrated in Figure 2.93.

For room temperature operation a-SiGe:H was studied, and resulted in a very attractive thermosensing material. It resulted in a high TCR when deposited from SiH_4 and GeH_4 in a Low Frequency PECVD system at 110 kHz, pressure of 0.6 Torr, and at substrate temperature of 573 K. The TCR measured on the device resulted dependent on the structure fabricated, for the bulk micromachined structure the film showed a TCR = 0.051 K^{-1} and for the surface micromachined structure TCR = 0.037 K^{-1} evidencing the better thermal isolation of the bulk micromachined device [2.407]. Nevertheless, the measured TCR on the fabricated devices resulted much larger than that reported for other devices; for instance Syllaios [2.408] reported a TCR measured on a device of 0.028 K^{-1}. Liang *et al*. [2.409] for poly-SiGe thermosensing film on uncooled microbolometers measured a TCR in the range of 0.014–0.022 K^{-1}.

In order of improving the performance of the surface micromachined bolometers, the position of the electrodes was also varied and two different structures resulted. These devices were named as planar and sandwich structures, in reference to the relative positioning of the electrodes, this is illustrated in Figure 2.94.

As a result the measured TCR on the devices is the same for both with a value of 0.043 K^{-1}, but because electrodes in the sandwich structure resulted in a very high field and a diode like behavior a high current is observed when the bolometer in this structure is illuminated under IR radiation and a gain in the photocurrent is observed

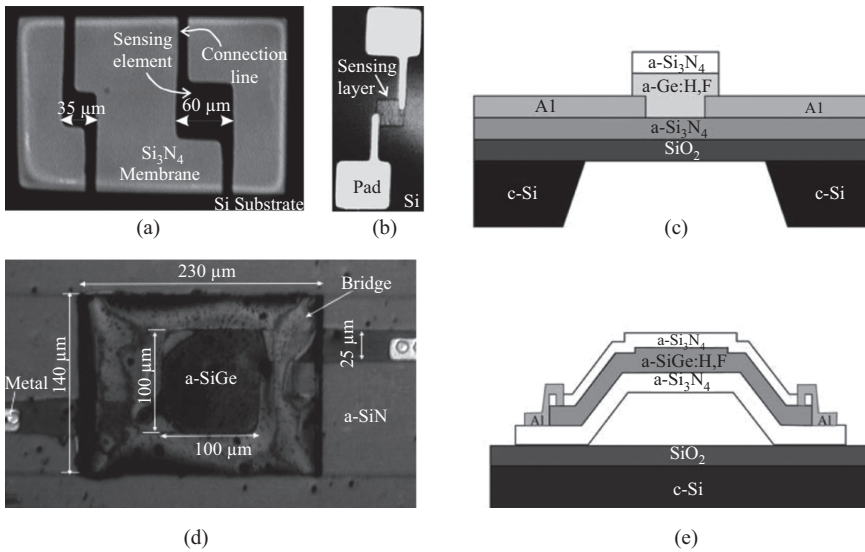

Figure 2.93 Membrane supported bolometer (a) backside view through SiO_2 membrane on a Si substrate. There are two structures of different size on the diaphragm. (b) Top view of a device. (c) Cross-section of the membrane supported microbolometer. (d) Top view of a surface micromachined bolometer. (e) Cross-section of the surface micromachined device

[2.410]. Most of the figures of merit are the same for both structures, the responsivity resulted to be 2×10^{-3} A/W for the planar structure and for the sandwich structure a responsivity dependent on the bias is observed and goes from 0.3 to 14 A/W. Also the thermal constant time for both devices is quite different being 0.1 ms and 125 ms for the planar and sandwich structures respectively [2.410].

Recently, it has been found that by varying the deposition parameters of a-Si:H, it is possible to form nanocrystals (of diameter of ~2–4 nm) distributed along the amorphous matrix. Such a material is commonly referred to as polymorphous silicon (pm-Si:H) [2.411]. The presence of nanocrystals impacts on the properties of the material by reducing the density of states (defects) and improving the transport properties (larger μe) and stability of the films. For a-Si:H thin-film solar cells, where degradation is an issue, pm-Si:H has been used instead of a-Si:H, and it has been demonstrated that this kind of cells suffer less of degradation due to light radiation (light soaking), such improvement is related to the presence of nanocrystals in the films [2.412].

For IR detectors and specifically for microbolometers, polymorphous semiconductors have not been reported, and we believe that its use as IR sensing films may represent a technological improvement, since those materials still preserve the characteristics of their amorphous counterpart, as a direct optical bandgap, large E_a,

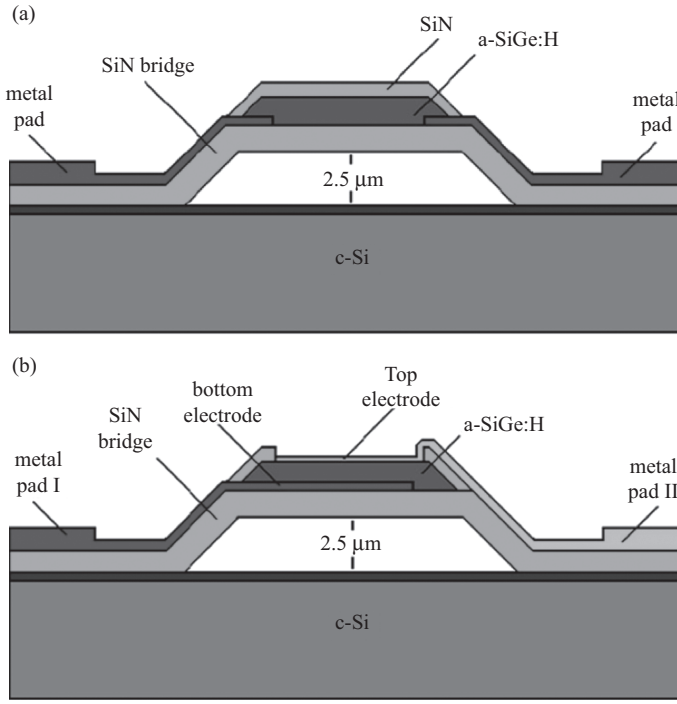

Figure 2.94 Microbolometer structure (a) planar and (b) sandwich contacts

and large TCR. In this aspect, we have studied the IR sensing properties of polymorphous silicon–germanium (pm-Si_xGe_y:H) thin films and have obtained promising results in terms of high E_a and TCR values with an improved σRT [2.413].

The pm-Si_xGe_y:H films were deposited from a SiH_4 (10% in H_2), GeH_4 (10% in H_2), and H_2 gas mixture, at a substrate temperature (T_s) of 200°C, in a capacitively coupled low-frequency PECVD reactor, working at 110 kHz, with an RF power density of 90 mW/cm^2. The films were characterized using high-resolution transmission electron microscopy (HRTEM), Figure 2.95 shows an HRTEM cross-sectional image of a pm-Si_x Ge_y:H film and as one can see, several nanocrystals of diameters in the range of 2–4 nm are distributed in the amorphous film. The presence of nanocrystals reduces the stress in the amorphous matrix, and consequently improves the stability of the Films.

The microbolometer fabricated with pm-Si_xGe_y:H resulted with the following advantages: a large TCR of -6.6% K^{-1}, resulting in devices with high-performance characteristics, the voltage Responsivity R_u (9.2×10^5 V/W) and a specific detectivity D^* (2×10^9 cmHz$^{1/2}$/W) with relatively low electrical resistance (1×10^6 Ω). Coupled with the above, the presence of small nanocrystals in the IR sensing films impacts on a reduction of defects, and improves the stability of the films against radiation [2.414].

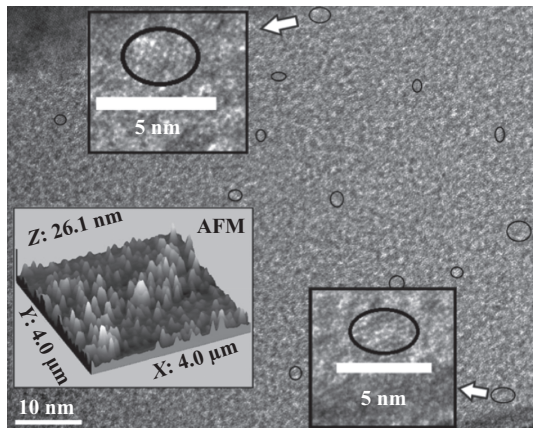

Figure 2.95 HRTEM image of a cross-section of a pm-Si_xGe_y:H film. Inset: 4 μm × 4 μm AFM image of the surface morphology of a pm-Si_xGe_y:H film, and two amplified images of nanocrystals of diameter of 4 nm

Terahertz and millimeter wavelength microbolometer. Sensing and imaging using pulsed terahertz (THz) radiation have been widely recognized for reconstructing three-dimensional (3D) images of objects [2.415, 2.416]. Recently published works show implemented systems that operate at frequencies below 1 THz. There are two reasons for this: first, humidity interferes with the image due to its high absorption above 1 THz, and second, the ability to find something covered by cloths. THz falls between the RF and IR bands, and is a largely unexplored region of the electromagnetic spectrum with wavelengths ranging from 100 GHz to 10 THz. The technology for this frequency range has been used recently in biology, medicine, and non-destructive control of materials. One key issue for obtaining low-cost detectors using monolithic construction is their easy integration and compatibility with the CMOS technology, therefore we use a-Si-B:H as material sensor. The amorphous silicon boron doped was deposited at a substrate temperature of 250 K by using SiH_4 and B_2H_6 as source gases. The TRC measured at 150K is 0.085 K^{-1}. The current responsivity measured at 77 K is 1.17×10^{-2} A/W at 7 V DC bias, enough for resolution at THz frequencies [2.417]. The same thermosensing material is used in millimeter wavelength microbolometers, here the pixel size is 4 mm because this is the size recommended for avoiding diffraction losses operating in the single mode regime [2.418]. An array of 96 microbolometers was built in a 2 inches Si wafer and is shown in Figure 2.96 mounted in a Cu plate and bonded for testing and waiting for characterization at 4.2 K.

So far we have showed how an amorphous alloy of SiGe is used for very different applications, the depositing conditions were adjusted for obtaining the properties that best fit for the particular application. Additionally the versatility offered for the PECVD system is demonstrated and all the devices are designed for being incorporated to CMOS silicon technology.

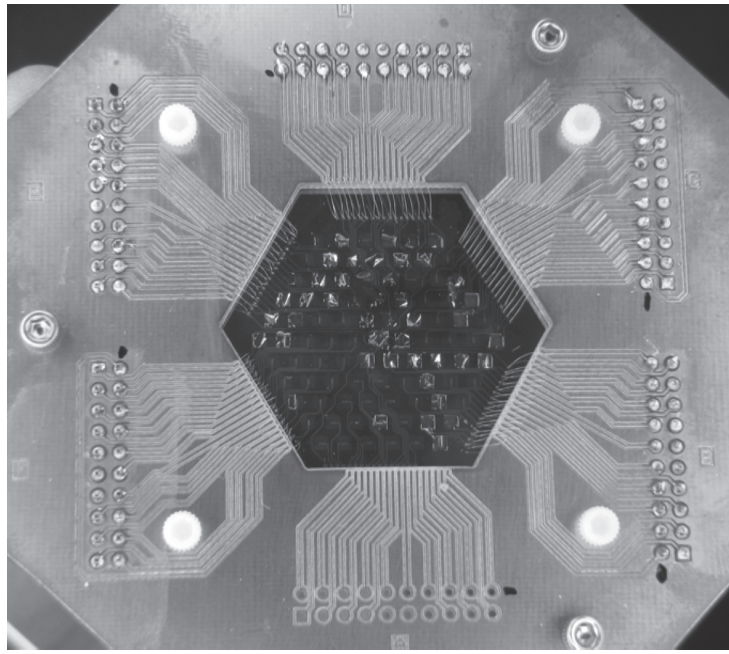

Figure 2.96 Array of 98 microbolometers placed on the Cu plate for testing at 4.2 K

2.4.4 CMOS process-compatible silicon-in-package (SiP)

System integration has shifted from a computational, PC-centric approach to a highly diversified mobile communication approach. The heterogeneous integration of multiple technologies in a limited space (e.g., GPS, phone, tablet, mobile phones) has truly revolutionized the semiconductor industry by shifting the main goal of any design from a performance driven approach to a reduced power driven approach. In few words, in the past performance was the one and only goal; today minimization of power consumption drives IC design.

This is demonstrated by the fact that SOC and SIP products have become the main drivers of the semiconductor industry as total volume of smart phones and tablets has surpassed production volumes of microprocessors in the past few years. The foundation of heterogeneous integration relies on the integration of "More Moore" (MM) devices with "More than Moore" (MtM) elements that add new functionalities (non-CMOS) that do not typically scale or behave according to "Moore's Law" [2.419]. At this point it is necessary to make the distinction between SOC and SIP.

System in Package uses the abbreviation SiP to differentiate itself from the old Single In-line Package (SIP). It is also sometimes called System in a Package. In its most simple definition, a SiP consists of active devices (one or multiple ICs), passive components and discrete devices designed and assembled into a standard or

custom package to achieve a modular function previous accomplished by using several separated single chip packages. The SiP forms a functional block or module that can be used for board level manufacturing. The objectives of using SiPs are therefore to [2.420]

- Provide alternate and cheaper solution for SOC, as SOC sometimes take longer to fabricate and reach the market.
- Provide higher levels of integration and better electrical performance.
- Reduce overall assembly size and weight and achieve cost effectiveness.

No doubt SiPs are currently used most widely in portable consumer electronic devices such as digital still camera, music player, video recorders, and mobile phones where size and weight are premium and hence the main drivers for miniaturization.

SoC (IC integration to system-on-a-chip) continues to be the dream of all semiconductor companies. Computer and communication companies have driven this trend for decades through finer lithography, better materials, and larger chips and wafers, all leading to higher clock frequency. Cost was not a factor. But the world has changed, and the primary focus today is more functionality at an affordable cost. Even personal computer companies have moved on to dual – and multi-core processors that perform multiple functions on a single chip – spreadsheet on one quarter of the screen, photograph editing on another, watching a movie on the third, and video-conferencing on the fourth. The key challenges to SoC progress, however, are formidable, and include design and design verification, manufacturability, intellectual property (IP) and legal issues, time-to-market, and cost [2.421].

For achieving the objective of high-level interconnection, size reduction and high packing density, there are four essential enabling technologies that support the progress of SiP. These four technologies are [2.420]: Wafer thinning, Substrate technology, Interconnection, and Embedded Passives. Here the Substrate technology is the topic of discussion, and a very good evaluation of materials for SOP substrates is found in reference [2.422]. In this work, the authors state that the next-generation packaging involves dramatic reduction in size and cost, coupled with higher performance. This can be accomplished with increased integration of passives, RF, and optoelectronics components within the package. For achieving all of this an appropriate choice or design of materials is important, because the major building block for the SOP technology is ultra-high-density wiring within the dielectric layers using single-sided build-up. This high-density interconnection is typically fabricated by a sequential deposition of alternate layers of copper metallization and polymer dielectric on the baseboard. The coefficient of thermal expansion (CTE) mismatch between the dielectric layers and the baseboard, coupled with the curing strain, the sequencing and asymmetry of the building layers etc., induce severe stresses and warpage in the board during or after the process. Results derived from analytical and finite element modeling show that a board with sufficient stiffness is needed to prevent the warpage and hence enable the fineline wiring and microvia build-up process.

The other building block for the SOP concept is a reliable flip-chip technology involving interconnection of unpackaged ICs directly to low-cost boards for

increasing the Si efficiency (area of Si within a package) and system level performance further. A chief concern is the CTE mismatch between the silicon die and the board. A silicon die has an approximate CTE of 2–3 ppm/°C, while conventional organic boards such as FR4 have a CTE ranging from 18 to 20 ppm/°C. The expansion mismatch induces plastic strain in the solder joint during operation resulting in low-cycle fatigue. All the materials chosen for the study are composite materials or ceramics, but nevertheless the conclusions of the comparison are challenging and can be summarized as follows:

- Matched CTE with Si die to prevent solder joint cracking without underfill.
- High enough elastic modulus to prevent cracking from cyclic warpage during heat cycle resulting from the CTE mismatch between the board and build-up dielectric layer. High elastic modulus is also necessary to reduce warpage during sequential build up process enabling ultra-high-density wiring of SOP.
- A dielectric material with low CTE, close to that of the board, and low modulus to minimize the dielectric stress and warpage caused by CTE mismatch between the base board and the dielectric. This can be another option to enhance SOP reliability performance from dielectric material design or selection standpoint.

Researchers at INAOE are proposing Teflon as the material for SiP because it offers all the advantages needed for this purpose, is a single component material, and has a very low tangent loss. The latter makes Teflon ideal for high-frequency applications because of its low dielectric constant and the offering of very low dielectric looses. Additionally if the Teflon surface is polished and an adherence to metals like Cu is improved, it also will result in low loss of the metal.

In order to proof our concept, a microstrip is going to be used [2.423]. The ohmic losses for a microstrip depend on DC resistance, AC resistance, and the real part of the impedance, Metal conductivity, frequency, and the average of roughness at the interface between metal and dielectric. In a conventional PCB fabrication process, the roughness is used for promoting adhesion of metals to the substrate. The roughness is an important factor in the ohmic losses especially in low-losses PCBs, it can enhance the AC resistance up to twice its value, and AC resistance is the most contributing part of the ohmic losses. Thus by reducing the roughness it can be reduced the ohmic losses. In our experiment we ended up a final roughness measured is of 30 nm, an argon plasma treatment on PTFE surface for Cu adherence was made and free bonds are created in the Teflon surface. Following 25 mm of electrodeposited Cu, the test of Copper Peel Strength was done with XLW (PC) Auto Tensile Tester and the result was 3.93 lbs/in, which is as good as some commercial PCB's or better. From S-parameters measurements we obtained for the microstrip fabricated an attenuation of only 2 Np/m at 20 GHz. One of the lowest values reported up to date.

Currently, researchers at INAOE are working on the fabrication of passive components as capacitors, inductors, and resistances on up to seven levels of metal using BCB as interdielectric metal. In the near future Teflon may be an optional material for SiP for very high frequency applications.

2.5 Conclusions

The silicon-based Field-Effect-device technology has evolved from the classical bulk approach based on SiO_2 gate dielectric, toward the most advanced and experimental devices, such as junctionless, tunnel-FET, NWs, SOI-FET, and Fin-FETs, where the FinFET being the mature device already in industry production for the most advanced 14 nm microprocessors. This chapter went through a review of these advanced FET-related devices, analyzing quantum effects.

The maturity of the FinFET technology has enabled a drastic reduction of the cost-per-device, or equivalently, the number of transistors that can be bought per dollar, to a number of 20 million transistors per dollar. However, this amazing evolution brought by the transistor size reduction, which increases the current drive capability and reduce the switching times making the device more functional and faster, is not for free. It comes with physical limitations due to the nanoscale quantum nature and fabrication technology limits, such as metal grain granularity, line edge roughness, RDFs. The electrical operation of advanced FET-related devices brought second-order undesirable effects, such as lack of electrostatic channel charge control, leakage currents, self-heating, that ultimately lead to device degradation reducing the performance and lifetime of electronic systems. The most common advanced FET-related device structures, its fabrication process, and operation characteristics have been reviewed in the first two sections of this chapter. The different approaches for fundamental physic-based device modeling and simulation have been introduced in Section 2.3.

Transport modeling for TCAD applications is a mature field of research with vast applications. Models of different complexity, precision, and accuracy are offered and implemented in various commercial and academic TCAD tools. Depending on parameter values and device scales, either a semi-classical or a quantum-mechanical transport description can be adopted. An MC method requires significant CPU resources and is now relatively rarely used for TCAD applications, when timely but perhaps less accurate results are of primary importance. MC methods can easily be extended and generalized to incorporate strain-induced modifications in the band structure and scattering rates, thus providing valuable input about the carrier mobility and other material parameters dependences on technological parameters and driving electric fields. These newly calibrated parameters can be used again in the drift-diffusion-based transport calculations extending their range of applicability. Spin transport in silicon can also be addressed with a diffusion-like equation with the spin relaxation term properly added.

In modern microelectronic devices quantum-mechanical effects become important and sometimes even dominant, which prompts for the development and use of quantum atomistic transport approaches. With shrinking device dimensions, the demand for fully three-dimensional accurate solvers for the coupled transport/Poisson equations and atomistic based simulations has grown significantly. With the advances in computer architectures, increased computational power and memory capabilities, state-of-the art software, development of fast numerical algorithms

and conceptually new generic simulation platforms a fundamental breakthrough in speed, reliability, and accuracy of multi-scale three-dimensional TCAD simulation tools is anticipated. However, with quantum corrections carefully added, the drift-diffusion based "atomistic" simulations provide often sufficiently accurate and timely statistical results for cutting edge ultra-scaled three-dimensional devices with fluctuation parameters including random dopant distribution. This extends the applicability of the drift-diffusion transport approach proving it again to be amazingly efficient even outside of its formal region of validity.

Finally Section 2.4 showed that the introduction of new materials and device structures has extended the CMOS platform to new applications domains, such as metrology for instance, where there is a plethora of radiation sensors that can benefit from amorphous Si and SiGe alloys, such as photodetectors and micro-machined bolometers that can be built into large arrays for high-resolution IR surveillance or detection. Nanostructured materials based on amorphous and SiGe alloys obtained from Plasma Enhanced Chemical Vapor Deposition (PECVD) are "Structure sensitive," which result in some advantages based on their short range bonding, rather than in the long-range order periodicity of crystalline materials. The structural "disorder" of amorphous materials influence the fundamental electronic properties. The strong scattering causes a large uncertainty in the electron momentum. The loss of momentum conservation implies that the E-k dispersion relations do not longer describe the energy bands. There is also no distinction between a direct and indirect band gap transition. These characteristics can be used to built CMOS-compatible high-efficient IR detectors, as the bolometer mentioned earlier.

Other materials, such as carbon for the fabrication of nanotubes have been considered due to its near ballistic transport properties at room temperature, that with a tight electrostatic control of its 1D channel may enable further downscaling beyond 10 nm. Graphene with its high carrier mobility close to 1×10^4 cm^2/Vs may be a good candidate for high frequency applications. However, graphene suffers from a major drawback; its zero bandgap, which results in small on/off current ratio and no stable saturation region in the output transistor characteristics. An option devised for graphene is its integration as a Hall sensor with a CMOS amplifier, for instance. The incorporation of graphene for building system-in-package is also another attractive route for graphene.

Gallium Nitride (GaN) is another attractive material with unique electronic properties, such as: high dielectric strength, high operating temperature, high current density, high speed switching and low on-resistance. These characteristics are due to the properties of GaN, which, compared to silicon, offers ten times higher electrical breakdown characteristics, three times the bandgap, and exceptional carrier mobility. But this material offers yet more advantages, the high electron mobility and charge density possible in AlGaN/GaN and InAlN/GaN heterostructures has enabled the demonstration of power amplifiers with at least one order of magnitude higher output power density than in their GaAs or Si-based counterparts. However, in spite of this excellent performance, nitride-based devices cannot compete with Si CMOS electronics in terms of cost, scalability, and circuit complexity. The seamless integration of these two semiconductor families would

give the circuit and system designer unprecedented flexibility to use the best material and devices for each function.

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