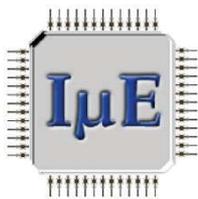


2016 Joint International EUROSOI Workshop
and International Conference on
Ultimate Integration on Silicon

EUROSOI-ULIS 2016



Book of Abstracts



Institute for Microelectronics
TU Wien, Vienna, Austria



January 25-27, 2016

2016 Joint International EUROSIOI Workshop
and International Conference on
Ultimate Integration on Silicon

EUROSIOI-ULIS 2016

Book of Abstracts

Edited by

Viktor Sverdlov
Sorin Cristoloveanu
Francisco Gámiz
Siegfried Selberherr

Institute for Microelectronics
TU Wien, Vienna, Austria

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The Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS) is a three days meeting bringing together the experts from Industry and Academia in technology, physics, modeling, simulation, and characterization of advanced nano-scale semiconductor-on-insulator and silicon-compatible devices from Europe and all over the world. For more than ten years the EUROSOI Workshop and the ULIS Conference provided a platform for the European micro- and nanoelectronic community to share the most recent advances, discuss the hottest topics in the field and outline current trends defining the future progress. As the future of microelectronics is believed to be determined by fully depleted SOI and FinFET devices enabling new functionalities, the two sister conferences were merged in 2015 in order to further boost their importance and scientific impact. Encouraged by the great success of the first joint EUROSOI-ULIS event, the second joint EUROSOI-ULIS 2016 Conference is hosted by the Institute for Microelectronics, TU Wien, Austria. The aim of the EUROSOI-ULIS Conference is to provide an open forum for the presentation and discussion of recent advances in the fields of More Moore, More than Moore, and Beyond CMOS applications. The hot topics introduced by outstanding international invited speakers will further be discussed at the sessions with a particular focus on modern SOI technology and advanced nanoscale devices. The Conference Committees and organizers hope you will enjoy the conference and the social program.

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January 25th (Monday)

9:30-10:00 Registration

10:00-10:20 Opening

SOI for Low Power and Sensors (Siegfried Selberherr, IµE, TU Wien)

- 10:20-11:00 Hans Stork** (On Semiconductor, Phoenix, USA): Invited 1
“SOI Technology for Power Management in Automotive and Industrial Applications”
- 11:00-11:20 Tim Baldauf (TU Dresden, Germany) 2
“Stress-Engineering for Improved Tunneling in Reconfigurable Silicon Nanowire Transistors”
- 11:20-11:40 Carlos Navarro (CEA-LETI, MINATEC, Grenoble, France) 4
“Reconfigurable Field Effect Transistors for Advanced CMOS: a Comparison with FDSOI Devices”
- 11:40-12:00 Yossi Rosenwaks (Tel-Aviv University, Israel) 6
“Sensors, and Multiple State Transistors Based on Electrostatically Formed Nanowire Transistors”

12:00-13:20 Lunch

Tunnel FETs (Sorin Cristoloveanu, IMEP-INP Grenoble)

- 13:20-14:00 Andreas Schenk** (ETH Zurich., Switzerland): Invited 8
“III-V-based Hetero Tunnel FETs: A Simulation Study with Focus on Non-ideality Effects”
- 14:00-14:20 Paula Agopian (University of São Paulo, Brazil) 10
“Intrinsic Voltage Gain of Line-TFETs and Comparison with Other TFET and MOSFET Architectures”
- 14:20-14:40 Elena Gnani (University of Bologna, Italy) 12
“Optimization of GaSb/InAs TFET Exploiting Different Strain Configurations”
- 14:40-15:00 José Luis Padilla (EPFL, Switzerland) 14
“Assessment of Confinement-induced Band-to-band Tunneling Leakage in the FINEHBTFET”

15:00-15:20 Coffee Break

January 25th (Monday) continued

Semiconductor Processing (Mikael Östling, KTH, Stockholm)

- 15:20-15:40 Christian Schulte-Braucks (Forschungszentrum Juelich, Germany) 16
“Process Modules for GeSn Nanoelectronics with High Sn Contents”
- 15:40-16:00 Andrew Shaw (University of Liverpool, UK) 18
“Controlling the Physical and Electrical Properties of ALD Grown ZnO
using Nb as a Dopant”
- 16:00-16:20 Alexei Orlov (University of Notre-Dame, USA) 20
“Study of Ultrathin Si₃N₄ Tunnel Barriers Prepared by Atomic Layer
Deposition using Single-electron Transistors”
- 16:20-16:40 Hei Wong (City University of Hong Kong) 22
“Challenges of MOS Gate Dielectric Scaling
in the Subnanometer EOT Range”
- 17:00-19:00 **Poster Session (Denis Flandre, Catholic University of Louvain)** and
Reception

January 26th (Tuesday)

Frequency Phenomena and Noise (Andrei Vladimirescu, MINARC – ISEP, Paris)

- | | | |
|-------------|---|----|
| 9:00-9:20 | Dimitri Boudier (University of Caen Normandie, France) | 24 |
| | “Low-frequency Noise Assessment in n- and p-channel Sub-10nm Triple-gate FinFETs” | |
| 9:20-9:40 | Carlos Márquez (University of Granada, Spain) | 26 |
| | “Electrical Characterization of Random Telegraph Noise in Back-Biased Ultrathin Silicon-On-Insulator MOSFETs” | |
| 9:40-10:00 | Sindhuri Vodapally (Kyungpook National University, Daegu, Korea) | 28 |
| | “1/f -Noise Characteristics of Omega-shaped AlGaIn/GaN Nanowire FETs” | |
| 10:00-10:20 | Christoph Jungemann (RWTH Aachen University, Germany) | 30 |
| | “Simulation of Plasma Resonances in MOSFETs for THz-Signal Detection” | |
| 10:20-10:40 | Coffee Break | |

Modeling 1 (Francisco Gamiz, University of Granada)

- | | | |
|-------------|--|----|
| 10:40-11:00 | Karol Kalna (Swansea University, UK) | 32 |
| | “Scaling/LER Study of Si GAA Nanowire FET using 3D Finite Element Monte Carlo Simulations” | |
| 11:00-11:20 | Liping Wang (University of Glasgow, UK) | 34 |
| | “Simulation Analysis of the Electro-Thermal Performance of SOI FinFETs” | |
| 11:20-11:40 | Nobuyuki Sano (University of Tsukuba, Japan) | 36 |
| | “Space-Average Impurity-Limited Resistance and Self-Averaging in Quasi-1D Nanowires” | |
| 11:40-12:00 | Michael Graef (Technische Hochschule Mittelhessen, Giessen, Germany) | 38 |
| | “Numerical Analysis and Analytical Modeling of RDF in DG Tunnel-FETs” | |
| 12:00-13:20 | Lunch | |

January 26th (Tuesday) continued

Advanced Memory (Maryline Bawedin, IMEP-INP Grenoble)

- 13:20-14:00 **Francisco Gamiz** (University of Granada, Spain): Invited 41
“Capacitor-less Memory: Advances and Challenges”
- 14:00-14:20 Yota Takamura (Tokyo Tech, Yokohama, Japan) 42
“Inverse-magnetostriction-induced Switching Current Reduction of STT-MTJs and its Application for Low-voltage Operation MRAMs”
- 14:20-14:40 Francesco Maria Puglisi (University of Modena, Italy) 44
“A Consistent Picture of Cycling Dispersion of Resistive States in HfO_x RRAM”
- 14:40-15:00 Alessandro Grossi (University of Ferrara, Italy) 46
“Performance and Reliability comparison of 1T-1R RRAM arrays with amorphous and polycrystalline HfO₂”
- 15:00-15:20 Alberto Crespo-Yepes (University Autonoma of Barcelona, Spain) 48
“Intra-device Statistical Parameters in Variability-aware Modelling of Resistive Switching Devices”
- 15:20-15:40 Coffee Break

Design, Characterization and Performance (Pierpaolo Palestri, University Udine)

- 15:40-16:00 Remy Berthelon (STMicroelectronics, Crolles, France) 50
“Impact of the Design Layout on Threshold Voltage in SiGe Channel UTBB-FDSOI pMOSFETs”
- 16:00-16:20 Theano Karatsori (IMEP-LAHC, MINATEC, Grenoble, France) 52
“Drain Current Local Variability from Linear to Saturation Region in 28nm Bulk NMOSFETs”
- 16:20-16:40 Chika Tanaka (Toshiba, Kawasaki, Japan) 54
“Investigation of BSIM4 Parameter Extraction and Characterization for Multi Gate Oxide-Dual Work Function (MGO-DWF)-MOSFET”
- 16:40-17:00 Carlos Sampedro (University of Granada, Spain) 56
“Confinement Orientation Effects in S/D Tunneling”
- 17:00-17:20 Luca Pirro (Univ. Grenoble Alpes, France) 58
“Volume and Interface Conduction in InGaAs Junctionless Transistors”
- 17:20-17:40 Alberto Oliveira (IMEC, Leuven, Belgium) 60
“Effective Hole Mobility and Low-frequency Noise Characterization of Ge pFinFETs”
- 19:00-22:30 Gala Dinner

January 27th (Wednesday)

Modeling 2 (Elena Gnani, University of Bologna)

- 9:00-9:20 Corentin Grillet (IMEP-LAHC, MINATEC, Grenoble, France) 62
“V_{DD} Scaling of Ultra-thin InAs MOSFETs: A Full-Quantum Study”
- 9:20-9:40 François Triozon (Univ. Grenoble Alpes, France) 64
“Contact Resistances in Trigate Devices
in a Non-Equilibrium Green’s Functions Framework”
- 9:00-10:00 Arienne Soares Pereira (Catholic University of Louvain, Belgium) 66
“Analysis and Modelling of Temperature Effect on DIBL
in UTBB FD SOI MOSFETs”
- 10:00-10:20 Paul Manstetten (Institute for Microelectronics, TU Wien, Austria) 68
“Modeling Neutral Particle Flux in High Aspect Ratio Holes
using a One-Dimensional Radiosity Approach”
- 10:20-10:40 Coffee Break

Advanced Devices and 3D Integration (Francis Balestra, Minatec)

- 10:40-11:20 **Silvano De Franceschi** (CEA-INAC, Univ. Grenoble Alpes, France): 71
Invited “CMOS Platform for Silicon Spin Qubits”
- 11:20-11:40 Veeresh Deshpande (IBM Research, Zurich, Switzerland) 72
“First RF Characterization of InGaAs RMG nFETs
on SiGe-OI FinFETs Fabricated by 3D Monolithic Integration”
- 11:40-12:00 Hassan El Dirani (STMicroelectronics, Crolles, France) 74
“A Sharp-Switching Gateless Device (Z³-FET)
in 14 nm FDSOI Technology”
- 12:00-13:20 Lunch

January 27th (Wednesday) continued

End of Scaling and Beyond CMOS (Siegfried Mantl, Forschungszentrum Juelich)

- 13:20-14:00 Hiroshi Iwai (Tokio Tech, Yokohama, Japan): Invited 76
“End of Scaling Theory and Moore’s Law”
- 14:00-14:20 Blend Mohamad (CEA-LETI, MINATEC, Grenoble, France) 78
“Robust EOT and Effective Work Function Extraction
for 14nm Node FDSOI Technology”
- 14:20-14:40 Sebastiano Strangio (Università degli Studi di Udine, Italy) 80
“Benchmarks of a III-V TFET Technology Platform against
the 10-nm CMOS Technology Node Considering 28T Full-Adders
- 14:40-15:00 Himadri Pandey (University of Siegen, Germany) 82
“Improved Voltage Gain in Mechanically Stacked Bilayer Graphene Field
Effect Transistors”
- 15:00-15:20 Zlatan Stanojevic (Global TCAD Solutions, Austria) 84
“Simulation Study on the Feasibility of Si as Material
for Ultra-Scaled Nanowire Field-Effect Transistors”

15:20-15:40 Coffee Break

Advanced Devices (Benjamin Iñiguez, Universitat Rovira I Virgili, Tarragona)

- 15:40-16:00 Sotirios Athanasiou (STMicroelectronics, Crolles, France) 86
“GDNMOS: A New High Voltage Device for ESD Protection
in 28nm UTBB FD-SOI Technology”
- 16:00-16:20 Guoli Li (Catholic University of Louvain, Belgium) 88
“Operation of Suspended Lateral SOI PIN Photodiode
with Aluminum Back Gate”
- 16:20-16:40 Babak Kazemi Esfeh (Catholic University of Louvain, Belgium) 90
“RF SOI CMOS Technology on 1st and 2nd Generation Trap-Rich High
Resistivity SOI Wafers”

16:40-17:00 Closing

Posters

P1	Matteo Vignetti (Université de Lyon, France) “A Novel 3D Pixel Concept for Geiger-Mode Detection in SOI Technology”	92
P2	Bruna Cardoso Paz (Centro Universitário da FEI, São Bernardo do Campo, Brazil) “Analog Performance of n- and p-FET SOI Nanowires Including Channel Length and Temperature Influence”	94
P3	Mischa Thesberg (Institute for Microelectronics, TU Wien, Austria) “Full Quantum Mechanical Electronic Transport Simulations in Si Quantum Wells and Superlattices for Thermoelectric Applications”	96
P4	Katia Sasaki (LSI/PSI/USP, University of São Paulo, Brazil) “Body Factor Scaling in UTBB SOI with Supercoupling Effect”	98
P5	Keyvan Narimani (PGI 9-IT and JARA-FIT Juelich, Germany) “Current Mirrors with Strained Si Single Nanowire Gate All Around Schottky Barrier MOSFETs”	100
P6	Daniel Tomaszewski (Instytut Technologii Elektronowej, Warsaw, Poland) “A Method for Combined Characterization of MOSFET Threshold Voltage and Junction Capacitance Eliminating Channel Current Effect”	102
P7	Eunjung Ko (Department of Materials Science and Engineering, Yonsei University, Korea) “Improvement of Silicide Resistivity for nMOSFET using In-situ Heavily Doped Si:P Epitaxial Growth”	104
P8	Rudolf Bühler (Department of Electrical Engineering, São Bernardo do Campo, Brazil) “Gated SiGe PIN Diodes Exposed to Visible Light Spectrum and Heavy-Ion Radiation”	106
P9	Romuald Beck (Institute of Microelectronics and Optoelectronics, Warsaw University of Technology, Poland) “Recrystallization and Oxidation - Competing Processes during PECVD Ultrathin Silicon Layer High Temperature Annealing”	108
P10	Andrzej Mazurak (Institute of Microelectronics and Optoelectronics, Warsaw University of Technology, Poland) “Effect of Inner Interface Traps on High-K Gate Stack Devices Admittance Characteristics”	110
P11	Joao Martino (LSI/PSI/USP, University of São Paulo, Brazil) “Comparative Study of Vertical GAA TFETs and GAA MOSFETs in Function of the Inversion Coefficient”	112

P12	Konstantinos Garidis (KTH Royal Institute of Technology, School of ICT, Kista, Sweden)	114
	“Integration of Epitaxially Grown in situ Doped SiGe Layers in Monolithic 3D CMOS Fabrication”	
P13	Viktor Sverdlov (Institute for Microelectronics, TU Wien, Austria)	116
	“Spin-dependent Resonant Tunneling in Ferromagnet-Oxide-Silicon Structures”	
P14	George P. Hosey (ON Semiconductor, East Greenwich, USA)	118
	“Finite Element Analysis at Semiconductor Die Level Modeling Heat Dissipation in an SOI Device”	
P15	Ashkhen Yesayan (Inst. of Radiophysics and Electronics, Armenia)	120
	“Conductivity Type Switching in Semiconductor Nanowires”	
P16	Lucas Czornomaz (IBM Switzerland)	122
	“Fabrication and Characterization of InGaAs-on-insulator Lateral N+/n/N+ Structures”	
P17	El-Hajjam Khalil (Institut des Nanotechnologies de Lyon, France)	124
	“Enhancing Electrical Performances of Metallic DG-SET Based Circuits by Tunnel Junction Engineering”	
P18	Dimitrios Damianos (IMEP-LAHC, Univ. de Grenoble Alpes, France)	126
	“Transient Second Harmonic Generation and Correlation with Ψ -MOSFET in SOI Wafers”	
P19	Vito Šimonka (Institute for Microelectronics, TU Wien, Austria)	128
	“Geometrical Aspects of Three-Dimensional Silicon Carbide Oxidation Growth Rate Modeling”	
P20	Andrés Godoy (Departamento de Electrónica y Tecnología de los Computadores, Universidad de Granada, Spain)	130
	“On the Influence of the Back-Gate Bias on InGaAs Trigate MOSFETs”	
P21	Vihar Georgiev (School of Engineering, University of Glasgow, UK)	132
	“Influence of Quantum Confinement Effects and Device Electrostatic Driven Performance in Ultra-scaled $\text{Si}_x\text{Ge}_{1-x}$ Nanowire Transistors”	
P22	Loukas Michalas (National Research Council, Institute for Microelectronics and Microsystems, Rome, Italy)	134
	“Scanning Microwave Microscopy for Non-Destructive Characterization of SOI Wafers”	
P23	Caio Bordallo (LSI/PSI/USP, University of São Paulo, Brazil)	136
	“Influence of the Ge Amount at the Source on Transistor Efficiency of Vertical Gate All Around TFETs for Different Conduction Regimes”	

P24	Marcio Dalla Valle Martino (LSI/PSI/USP, University of São Paulo, Brazil) “Analysis of TFET and FinFET Differential Pairs with Active Load from 300K to 450K”	138
P25	Sung-Min Hong (Gwangju Institute of Science and Tech., Korea) “Numerical Simulation of Gunn Oscillation in AlGaAs/InGaAs High-Electron Mobility Transistor”	140
P26	Aleksei Nazarov (National Technical University of Ukraine “KPI”, Dep. of General and Solid State Physics, Kyiv, Ukraine) “Metal-Graphene Contact Capacitance”	142

Session Schedule

	January 25 th	January 26 th	January 27 th
09.30 – 10.10	Registration	Frequency Phenomena and Noise	Modeling 2
10.10 – 10.20	Opening		
10.20 – 10.40	SOI for Low Power and Sensors	Coffee Break	Coffee Break
10.40 – 12.00		Modeling 1	Advanced Devices and 3D Integration
12.00 – 13.20	Lunch	Lunch	Lunch
13.20 – 15.00	Tunnel FETs	Advanced Memory	End of Scaling and Beyond CMOS
15.00 – 15.20	Coffee Break		
15.20 – 15.40	Semiconductor Processing	Coffee Break	Coffee Break
15.40 – 16.40		Design, Characterization and Performance	Advanced Devices
16.40 – 17.00			Closing
17.00 – 17.40	Poster Session and Reception (Gußhausstraße 27-29)		
17.40 – 19.00			
19.00 – 22.30	Committees' Meeting	Gala Dinner (Palais Todesco, Kärntner Straße 51)	

SOI Technology for Power Management in Automotive and Industrial Applications

Hans Stork

ON Semiconductor, 5005 East McDowell Road, Phoenix, AZ 85008, USA

With nearly three decades of experience in technology and product development, Dr. Stork has held various leadership positions including Group Vice President and CTO of the Si Systems Group at Applied Materials, and Senior Vice President and CTO of Texas Instruments and director of Si Technology Development at TI. During his career, Dr. Stork has worked with some of the semiconductor industry's leading innovators including Hewlett Packard and IBM Research.

Dr. Stork holds a PhD in Electrical Engineering from Stanford University, and an Electrical Engineering Ingenieur (Cum Laude) from Delft University in the Netherlands. He has authored numerous scientific articles and papers, and served as a board director for Sematech and the Semiconductor Research Corporation (SRC) and is a member of the Scientific Advisory Board for IMEC.

Dr. Hans Stork joined ON Semiconductor in 2011 as Senior Vice President and Chief Technology Officer (CTO) responsible for the company's product research and development.

Stress-Engineering for Improved Tunneling in Reconfigurable Silicon Nanowire Transistors

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Thomas Mikolajick^{1,2,3}, *Senior Member IEEE*, and Walter Michael Weber^{2,3}

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1. Introduction

As an alternative to multigate metal oxide semiconductor field effect transistors (MOSFETs) which will be ultimately limited in scaling, reconfigurable nanowire (NW) transistors (RFETs) provide an increased functionality of highly scaled integrated circuits [1] -[3]. With its two independently gated Schottky junctions (SJ) (Si NiSi₂) at source and drain side the RFET is able to work as a unipolar n- or p-FET with the same physical structure [3] (Fig.1) and allows multifunctional and reprogrammable logic circuits [5]. Nevertheless, the drain currents of unstrained n- and p-RFETs with Si-NiSi₂ junctions (barrier for electrons ~0.66 eV, for holes ~0.46 eV) are not symmetric and thus do not satisfy the requirements for complementary circuit operation. In this work we employ mechanical stress to modify the band structure of the semiconductor nanowire channel yielding an effective mechanism to finely adjust the symmetry between n- and p-RFET without the need of doping or altering the electrode material composition [6]. TCAD process and device simulations in combination with experimental work are employed here.

Different methods to induce the mechanical stress are considered: compressive stress from oxide shell, epitaxial stress from the silicidation of source/drain contacts, stressed metal gates and stressed top layers over the device (Fig.2). The results are also relevant for other type of devices encompassing a tunneling barrier in the on-state.

2. Mechanical Stress of Oxidized Silicon NW

A 220 nm long and 20 nm thick undoped silicon NW with <110> channel direction and six facets (two times (100), four times (111)) was oxidized with 875°C and 10 slm O₂ capturing the experimental structure. Note that the reaction rate for (111) surfaces are 30 % to 100 % higher than for (100) resulting in an oval NW cross section. The appearing oxide is approx. twice the thickness vs. the consumed silicon leading to a radial compressive stress in the NW (Fig.3). In addition, stress modulated reaction rate at Si-SiO₂ interfaces and stress dependent oxygen diffusion in the tensile oxide shell cause a self-limitation of oxidation.

3. Stressed Schottky Barrier Devices

The asymmetric transfer characteristics of n- and p-type NW-RFETs based on unstrained Si-NiSi₂ Schottky junctions arise mainly from dissimilar tunneling probabilities of electrons and holes (Fig.4). There are two important parameters influencing the tunneling

probability which are also depending on mechanical stress. One is the effective band edges E_c and E_v and the other is the average effective tunneling masses of electrons (m_{t,e}) and holes (m_{t,h}). The band edges and the NiSi₂ workfunction fixed at ~4.73 eV related to the vacuum level determine the barrier heights $\Phi_{B,e}$ and $\Phi_{B,h}$. For the tunneling case at the Schottky barriers the conduction or valance band edge is so strongly bent that the width of the barrier becomes smaller than the tunneling distance of the carriers. The compressive radial stress lowers the electron barrier and thus the barrier width increasing the tunneling probability (Fig.5). Conversely, the hole barrier increases and the hole tunneling probability decreases. In our simulations this stress dependent band structure is taken into account by the deformation potential theory of the multi-valley band structure [7].

The effective tunneling masses of electrons and holes are derived from the band bending simulated with the empirical pseudopotential method and have a direct influence of the tunneling probability which is calculated by the Wentzel-Kramers-Brillouin (WKB) approximation. Mechanical stress modulates the band bending and therefore the effective mass near the conduction and valance band edge where the most carriers are located. The radial compressive stress decreases and increases the effective mass of electrons and holes, respectively. With the impact of both mechanisms we achieved symmetric transfer characteristics of n- and p-type NW-RFETs (n/p ration of 1.05) matching the experimental results [3].

Table 1 summarizes the impact of the different stress sources on effective masses, barrier heights and finally the n/p ratio. Oxidation shows the strongest influence on device performance. The other stress sources show a weaker impact in their configuration, but offer potential for improvement and can be additionally superimposed on each other.

4. Conclusion

Mechanical stress provides a flexible dopant-free method to adjust drain currents in energy barrier based transistors. It is applicable to scalable arbitrary structural composition of silicon based RFETs as well as TFETs to finely tune the n/p ratio.

This work is supported by “Deutsche Forschungsgemeinschaft (DFG)” in the project ReproNano (MI 1247/6-2 and WE 4853/1-2) and was carried out in collaboration with the Cluster of Excellence ‘CfAED’

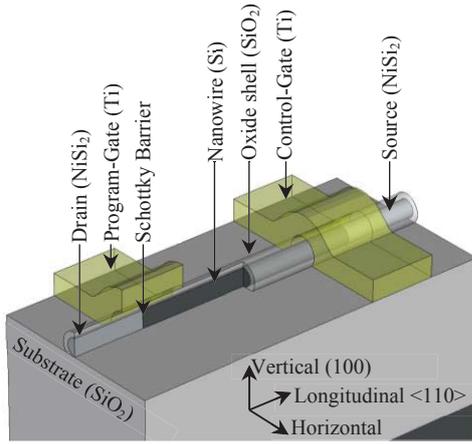


Fig.1: Schematic view of reconfigurable silicon NW-FET with two independently gated Schottky junctions at source and drain side, respectively.

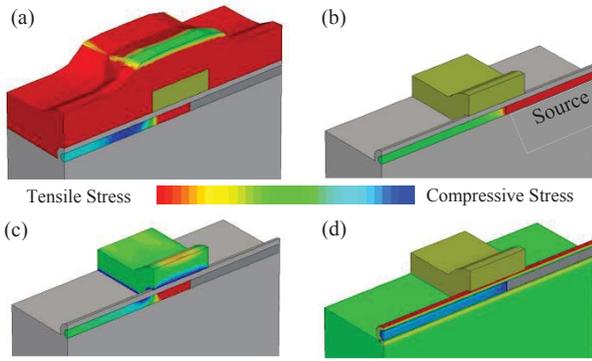


Fig.2: Simulated stress profiles of silicon nanowire induced by several stress sources: (a) tensile stressed top layers over the device, (b) stress from the silicidation of source/drain contacts (tensile), (c) compressive stressed metal gates and (d) compressive stress from oxide shell.

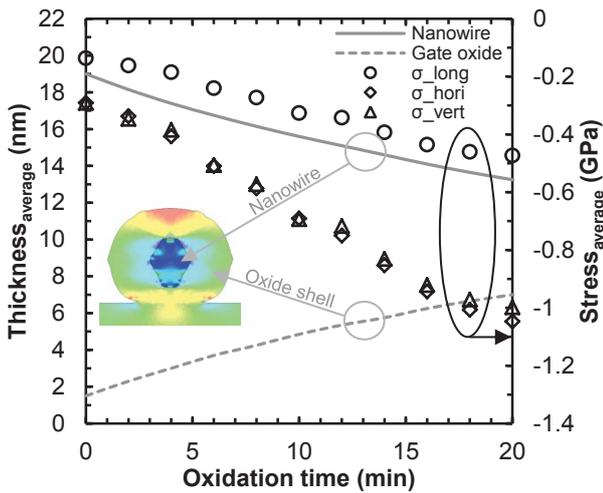


Fig.3: Simulated thickness (average) of the Si NW t_{si} , gate oxide t_{ox} (left) and average stress values near the Schottky junction (right) versus oxidation time (875 °C, O₂ = 10 slm). Initial values were $t_{si} = 19$ nm and $t_{ox} = 1.5$ nm (native oxide).

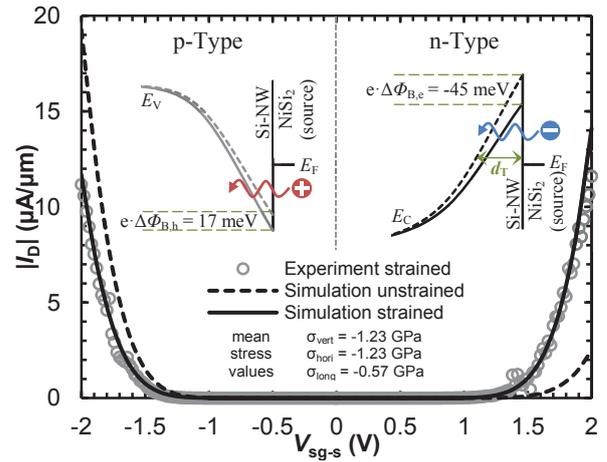


Fig.4: Transfer characteristic normalized to NW diameter for unstrained n- and p-type (dashed) and including the simulated stress profile after 25 minutes oxidation (solid). The operating point was set to $V_{dg-s} = 2$ V, $V_{d-s} = 2$ V (n-Type) and $V_{dg-s} = -2$ V, $V_{d-s} = -2$ V (p-Type). The inset shows a schematic view of strained and unstrained electron barrier (left) and hole barrier (right) at the SJ on the source side.

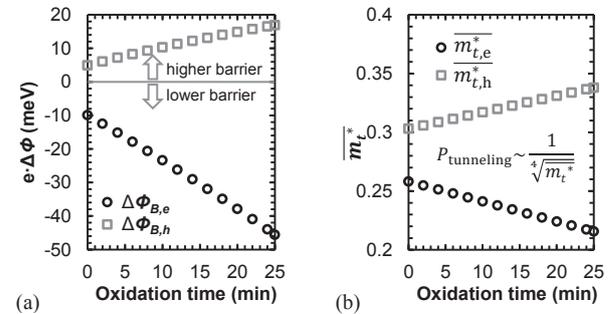


Fig.5: Stress dependent tunneling parameter as function of oxidation time (considering the native oxide of 1.5 nm): (a) change of barrier height and (b) effective electron and hole mass averaged over the corresponding subbands.

Tab.1: Overview of the simulated imprinted stress values, stress dependent effective masses and change of barrier height as well as n/p ratio (unstrained 0.13) for the four investigated stress sources.

	Oxide (compressive)	NiSi ₂ (tensile)	Metal-Gate (compressive)	Overlayer (tensile)
σ_{long} (GPa)	-0.57	0.12	0.59	0.37
σ_{hori} (GPa)	-1.23	-0.09	-0.24	0.08
σ_{vert} (GPa)	-1.23	-0.08	0.41	-0.30
$\overline{m}_{t,e}^* / \overline{m}_{t,h}^*$	0.22/0.34	0.25/0.31	0.28/0.52	0.21/0.27
$e \cdot \Delta\Phi_{B,e} / e \cdot \Delta\Phi_{B,h}$ (meV)	-45/17	0/-1	8/-13	-8/-8
n/p	1.05	0.19	0.31	0.25

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Reconfigurable Field Effect Transistors for Advanced CMOS: A Comparison with FDSOI Devices

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Abstract

The optimization of Reconfigurable FET devices is carried out in planar SOI technology. The electrostatic behavior, drive current and logic inverter operation are then compared with planar 28nm FDSOI devices.

1. Introduction

Much attention is being paid nowadays to alternative devices for future electronics. Among all the possible candidates (Trigate FETs [1], Tunneling FETs [2], stacked nanowires [3]...), Reconfigurable FETs, RFETs [4], stand as an interesting path to achieve reprogrammable logic in future circuits.

RFETs feature metallic source and drain (S/D) regions. Additional polarity gates (PGs) control the S/D schottky barriers. This allows to in-situ switch from N to P-like FETs by selecting which carrier is injected by tunneling. The RFET advantages are: i) no doping required for S/D regions (no random dopant fluctuations), ii) fewer fabrications steps and lower thermal budget (no S/D implantation, dopant activation or epitaxy), iii) possible reduction of device number for similar logic functions and iv) reversible operation.

In this work we optimized the RFET structure (Fig. 1a) and we realize a native benchmark with FDSOI (Fig. 1b) using identical 28 nm planar technology at device and single stage circuit level.

2. Simulation Setup

Preliminary simulations, using Synopsys TCAD [5], were carried out to optimize the planar RFET structure in terms of electrostatics (DIBL, subthreshold Swing (SS) and driven current, I_{ON}/I_{OFF}). The computation of the tunneling probabilities is based on the WKB approximation by using non-local tunneling between silicide and silicon [5]. In order to achieve symmetrical drive current between N- and P-RFET, the S/D silicide workfunction is set close to mid-gap while the relative electron effective masses are $m_e^* = 0.3$ and $m_h^* = 0.2$ as in [6]. The carrier mobility fits experimental 28 nm FDSOI results at similar gate length [7] (constant mobility fixed at $227/60 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ for electrons/holes). Several structures featuring distinct number of top gates were considered. The 3-gate (3G) RFET was finally selected due to the enhanced electrostatics and better control of the ambipolar current. A detailed analysis of a similar device may be found in [8]. The final structure features $t_{Si} = 6.5 \text{ nm}$, $t_{BOX} = 25 \text{ nm}$ and $EOT = 1.55 \text{ nm}$. The gates length is fixed to 20 nm while their spacing is 15 nm. The overlapping of PGs with the body is 10 nm leading to a final silicon film length of $L_{Si} = 70 \text{ nm}$.

3. RFET vs. FDSOI

The FDSOI structure used to benchmark the RFETs presents a 27 nm control gate with the same film architecture than RFETs. A 15 nm epitaxy is performed

to raise the S/D regions and reduce the series resistance.

Fig. 2 presents the drain current comparison between the RFETs and FDSOI. Table 1 summarizes the I_{ON}/I_{OFF} currents and the main electrostatic results at minimum and equivalent effective gate length for FDSOI. The RFETs ON current is about 15-50 times lower. This reduction of drain current is related to: i) the low efficiency of the carrier injection mechanism by tunneling (at silicide/silicon interface), ii) to the additional resistance between PG and CG contacts and iii) to the reduced lateral electric field. Fig. 3 illustrates the top-interface energy bands for similar biasing conditions and effective gate length. The lateral electric field (slope of the energy) is weaker in RFETs than in FDSOI. The equipotential lateral PGs prevent the development of an intense lateral field to accelerate carriers leading to a lower drain current.

-		SS mV/dec	DIBL mV/V	I_{ON} $\mu\text{A}/\mu\text{m}$	I_{OFF} nA/ μm	I_{ON}/I_{OFF} $\cdot 10^5 \text{ A/A}$
RFET	P	84	98	24.5	0.19	1.27
	N	84	94	22.2	0.20	1.11
27 nm FDSOI	P	95	148	447	1.19	3.77
	N	94	136	1160	0.88	13.1
60 nm FDSOI	P	71	37	309	0.03	117
	N	70	30	1020	0.02	518

Table 1: RFET vs. FDSOI benchmark in planar 28-FDSOI. $V_{BG}=0 \text{ V}$ and $V_{DS}=\pm 1 \text{ V}$. $V_{PG}=2\text{V}$ (N-RFET) and $V_{PG}=-2\text{V}$ (P-RFET). $I_{ON}=I_{DS}(V_{CG}=V_T\pm 0.65\text{V})$. $I_{OFF}=I_{DS}(V_{CG}=V_T\pm 0.35\text{V})$.

The capacitance comparison is showed in Fig. 4 for $V_{DS} = 0 \text{ V}$. Despite the smaller RFET control gate capacitance due to the thicker spacers, the additional PGs yield a larger load capacitance when driving all top gates simultaneously to reprogram the device. Fig. 5a depicts the voltage-transfer characteristics (VTC) of logic inverters made with FDSOI and RFET devices. The RFET VTC is degraded since the drain current at high/low (N/P-RFET) V_{CG} is determined by the tunneling barrier thickness rather than by the control gate-induced energy barrier. Fig. 5b illustrates how the FDSOI inverter response outraces the RFET. A 0.3 fF capacitance was included at the output to account for parasitic as in [9]. The rise, t_{LH} , and fall, t_{HL} , times are calculated as the crossing points at 50% of V_{DD} and averaged to extract the inverter propagation delay [10], τ_p , in Fig. 6a. RFETs feature, at least, 70 times larger delay than FDSOI. These delay differences contrast with the inverter logical effort, g , stated in [11]. The modest RFET currents, Fig. 6b, yield high equivalent resistances, thus longer τ_p (proportional to $R \cdot C_L$). Fig. 6b also demonstrates the symmetric current curves for N- and P-RFETs and how RFETs are not suitable for low-power applications ($< 1\text{V}$). As the power supply, V_{DD} , is reduced, the current dramatically drops. The energy-bands bending is small resulting in thick energy barriers

and low tunneling efficiency. To compute the energy per transition, E , the total inverter load capacitance, C_L , was approximated through the propagation delay and maximum current. $C_L = 2.2$ and 2.0 fF were obtained for FDSOI and RFET inverters, respectively. These capacitance values agree with results in Fig. 4a. The energy and energy delay product (EDP) are represented in Fig. 7. The optimum V_{DD} , minimizing the performance-power consumption, is 1 V for FDSOI while for RFETs is larger than the maximum V_{DD} considered, 2 V. In any case, we find a much lower EDP for FDSOI than for RFETs.

4. Conclusions and Perspectives

We have shown that RFETs turn to be not competitive at device or single logic gate level as compared to 28 nm FDSOI technology. Their limited current leads to much larger delays and EDP. Nevertheless, the advantages are expected to arise from a wise, but challenging, circuit conception where the reprogrammable logic can be useful to reduce the number of devices required.

Acknowledgements

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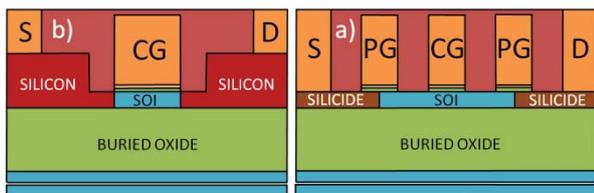


Fig. 1: a) Optimized RFET and b) 28 nm FDSOI structures with same gate-stack and films thicknesses. S/D regions are metallic in RFETs while highly doped Si is used in FDSOI.

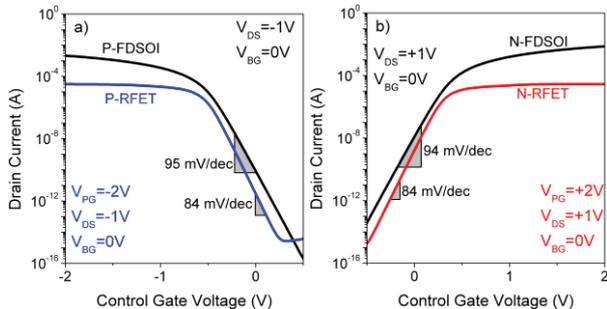


Fig. 2: (a) P- and (b) N-type current comparison. RFET $L_{Si}=70\text{nm}$. FDSOI $L_{Si}=27\text{nm}$. $V_{BG}=0\text{V}$.

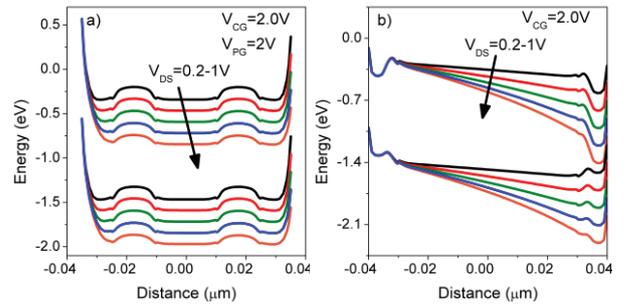


Fig. 3: Horizontal (≈ 0.5 nm from top-interface) N-MOS energy bands for (a) RFET and (b) FDSOI at similar length. $V_{BG}=0\text{V}$.

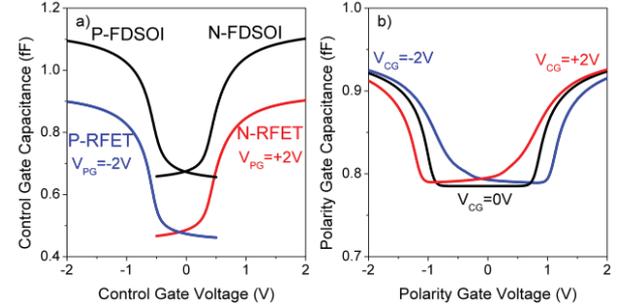


Fig. 4: Capacitance benchmark for (a) control gate in RFETs and FDSOI. (b) Single RFET polarity-gate capacitance at different control gate biases. $V_{DS}=0\text{V}$ and $V_{BG}=0\text{V}$.

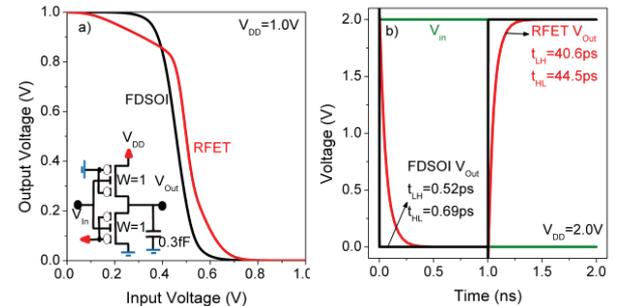


Fig. 5: Mixed mode a) Voltage-Transfer Characteristics and b) transient response to square signal. Inset: RFET inverter with 0.3fF output capacitance. FDSOI $W_P=2 \cdot W_N$. RFET $W_P=W_N$.

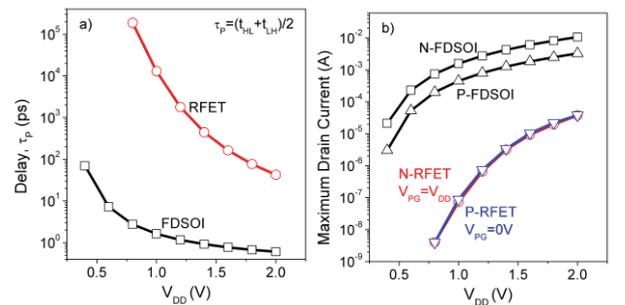


Fig. 6: a) Delay and b) maximum drain current benchmark. The RFET delay is much larger than in FDSOI due to the low tunneling current.

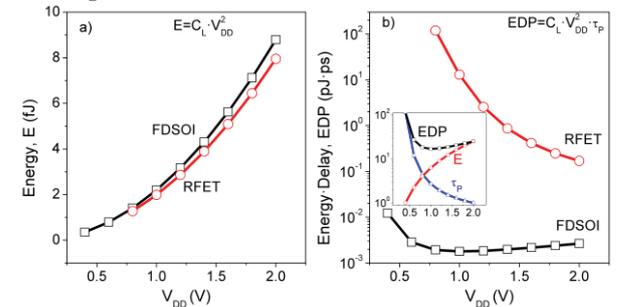


Fig. 7: a) Energy per transition and b) EDP comparison. The inset shows the normalized energy, delay and EDP for FDSOI.

Sensors and Multiple State Transistors Based on Electrostatically Formed Nanowire Transistors

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1. Introduction

As transistors dimensions are to reach their fundamental limit in around 2025, new design concepts are a subject of utmost importance. We present here a new paradigm in nanowire transistors termed Electrostatically Formed Nanowire (EFN) transistors. We demonstrate its application as a gas sensor, and multiple state transistor.

The EFN device is based on the silicon-on-insulator (SOI) four gate field-effect transistor (G^4 -FET) developed in 2002 [1], [2] which emerged from the volume inversion SOI MOSFET. The G^4 -FET combines MOSFET and junction gate field-effect transistor (JFET) principles as it consists of a top MOS gate (V_{TG}), a bottom substrate gate (V_{BG}) and is enclaved between by two lateral junction gates (V_{JG1} , V_{JG2}), as shown in Figure 1. The four gate transistor can be naturally adapted to CMOS technology scaling and manufactured in conventional silicon-on-insulator (SOI) processes with a low cost and high volume manufacturing.

The EFN device can function as an extremely sensitive molecular sensor, if the top gate is removed in order to allow functionalization of the top dielectric surface. Adsorbed polar molecules modify the surface charge distribution and consequently induce a change in the source-drain current. When a reverse bias is applied to the side junction gates, the area around them becomes depleted and the conduction band electrons between the gates are confined to a well-defined area forming a narrow channel, the electrostatically-formed nanowire, shown as a blue circle in Fig. 1(b) [3]. The sensitivity of the EFN device for ethanol detection is demonstrated in Fig. 2 and quantified through the drain current change defined here as $\Delta I/I_0 = (I_0 - I_{eth})/I_0$, where I_0 and I_{eth} are the drain currents in pure nitrogen and ethanol with nitrogen as carrier gas, respectively. The Figure shows the sensitivity of the device as a function of ethanol concentrations for side-gate voltages, $V_{JG12} = 0$ V, -0.9 V, -1.2 V, and -1.5 V and a backgate voltage of $V_{BG} = -6$ V. These side-gate voltages correspond to an effective EFN diameter varied from 46 nm to 16 nm, as represented by the schematic NW cross-sections to the right of Fig. 2. The sensitivity increases with the concentration for all curves (for each V_{JG12}). Furthermore, at each concentration, the sensitivity increases with decreasing V_{JG12} , corresponding to a narrower channel. It is evident from Fig. 2 that the EFN device is sensitive to ethanol concentrations as low as 100 ppm when $V_{JG12} < -0.9$ V and $V_{BG} = -6$ V. Adsorbed ethanol molecules modify the surface charge distribution and consequently induce a change in the surface potential; the smaller the EFN, the more it is affected by such a surface potential change. Hence, the increase in the sensitivity is a direct result of a smaller conducting channel when V_{JG12} is decreased.

Since the EFN geometry and size are electrostatically controlled, its lateral position and magnitude can be easily modified by the gates voltages. We propose here a Multiple-State EFN Transistor (MSET) that exploits the EFN lateral movement in order to form a single transistor multiplexer. In these devices the drain (or source) is split into several isolated drains (or sources) as shown schematically in Fig. 3. As a result, by tuning the position of the EFN, some of the drains can be connected to the source while the others are isolated from it realizing a multiplexer functionality. The basic MSET configuration closely resembles a split gate JFET with one important difference: the drain is split into several drain inputs isolated from each other by a dielectric buffer layer. Fig 3 shows such a two-drain MSET device embedded in a circuit which allows definition of voltage based states.

The device bulk is n type, the source and drains are n^+ , while the gates regions are p^+ doped. The light blue region between the drains is a dielectric (SiO_2) buffer. When a negative bias is applied to one of the gates, the area around it becomes depleted from charge carriers. The magnitude of the depleted region is determined by the gate voltage. Since the electric field within the depleted regions reflects the majority carriers in the device bulk, the charge carriers in the bulk are confined to the non-depleted regions. As a result, the size and position of the conduction path between the source and the drains can be controlled by tuning the gates voltages. For example in device as in Fig 3, if a high negative bias is applied to gate 1 (SG_1) while the other gate (SG_2) is grounded, the region between the biased gate and the dielectric buffer is will be completely depleted and the drain next to the biased gate will be isolated from the device bulk. Hence, there will be a single conduction path between the source and the drain next to the grounded gate (dark red line in Fig 3).

In order to obtain additional degrees of freedom a three dimensional architecture is proposed. The basic mode of operation is a two dimensional movement of the channel, where the conduction path is determined by 4 independent gates, termed here JG_N , JG_S , JG_E and JG_W . The drains are 'islands', isolated from each other and located between the gates. The source is located beneath the drains. An illustration of a three dimensional MSET with four gates and four drains is shown in Fig 3(b). In this case the conductance column is determined by the voltage on JG_W and JG_E , and the conducted row is determined by the voltages on JG_N and JG_S . The advantages of the MSET is demonstrated by realizing a 2 control, 4 inputs multiplexer shown in Fig. 3(b). Here the inputs a_0 and a_1 are binary signals that determine the voltage on JG_W and JG_N . Two CMOS inverters are used to transfer the complementary signal to the two opposite gates. As a result, for each combination of a_0 and a_1 there

will be a single conduction path between one of the drains and the output. It should be noted that while this configuration consists of a single MSET and 4 MOSFETs, a similar none-restoring multiplexer realized in CMOS consists of 16 transistors [4].

This proposed class of devices is a proof of concept aimed to demonstrate their basic functionality. Wide spread implementation of MSET based circuits in ASIC and FPGA chips will rely on the ability to fabricate them in appropriate lateral dimensions with low power consumption at sufficient frequency.

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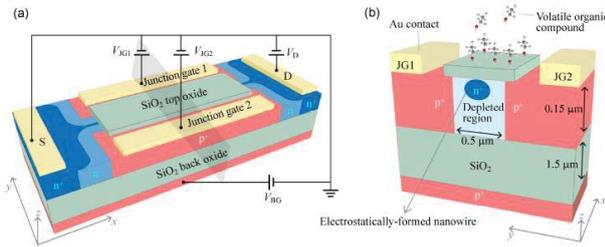


Figure 1: Schematic illustration of an EFN device. (a) Different contact regions and the channel region are defined by specific doping implants, assigned with n^+ , n , and p^+ . A thermal SiO_2 layer with a thickness of 6 nm covers the active sensing area. The EFN device is biased according to the electrical circuit. (b) Schematic cross-section along the y -axis of the device showing one possible configuration of the electrostatically shaped nanowire with a volatile organic compound (ethanol) bound to the active area of the device.

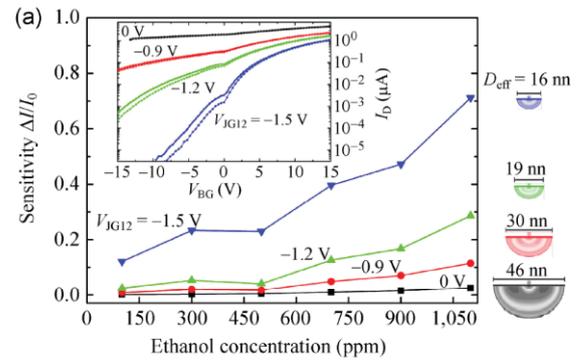
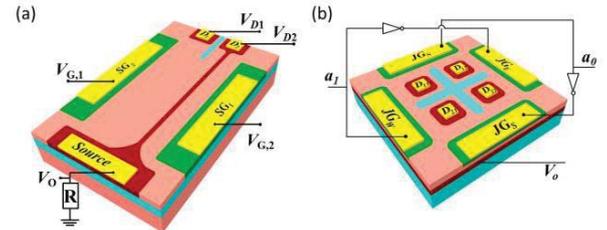


Fig.2: Sensitivity plot as a function of ethanol concentration in ppm range at $V_{BG} = -6$ V and $V_D = 1$ V. Different curves correspond to $V_{JG12} = 0$ V, -0.9 V, -1.2 V, and -1.5 V. Each voltage is equivalent to a different effective diameter represented by the semispherical cross sections on the right. The Inset shows the logarithmic plot of the I_D - V_{BG} characteristics for different V_{JG12} . Dotted curves correspond to the N_2 atmosphere and solid curves correspond to 1,100 ppm ethanol exposure on the EFN device.

Figure 3: (a) Two drains MSET device in device in an exemplary circuit which allows definition of voltage based



states. (b) An exemplary realization of a 2 control 4 inputs multiplexer based on a four gates, four drains MSET.

III-V-based Hetero Tunnel FETs: A Simulation Study with Focus on Non-ideality Effects

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We present semi-classical simulations of Gate-overlapped-Source Tunnel Field Effect Transistors (GoS-TFETs) taking into account the effects of channel quantization, surface roughness, and density-of-state (DOS) tails.

In a TFET, band-to-band tunneling (BTBT) takes place along two kinds of tunnel paths - parallel to the gate (point tunneling paths) and perpendicular to the gate (line tunneling paths, see Fig. 1). Line tunneling starts when the transistor channel becomes strongly inverted. Under such conditions, the triangular-like potential well of the channel quantizes the electronic states and a 2DEG forms. This shifts the onset voltage of line tunneling to a higher value when compared with the 3DEG case [1]. Besides, the nature of the wave functions changes from Airy functions to “quantized” Airy functions, which modifies the tunnel generation rate. These effects are not covered by the default “dynamic nonlocal path BTBT model” based on Kane’s treatment of BTBT [2], available in the semi-classical TCAD simulator Sentaurus-Device [3]. A method to model the quantization effect within a semi-classical framework has been proposed by Vandenberghe et al. [4]: Tunneling paths with energies above the lowest sub-band level are accepted while those with a lower energy are rejected, as illustrated in Fig. 3(a). We incorporated such a model in Sentaurus-Device by developing our own code for the “dynamic non-local path BTBT model” using the so-called Physical Model Interface (PMI) for “nonlocal recombination”. The implemented algorithm detects a line tunneling path at a proper energy by checking whether the extension of this path intersects the oxide interface. If not, it is not considered to be affected by channel quantization. As an alternative to this rather involved approach, a much simpler method was developed making use of the Quantum Potential Correction available in Sentaurus-Device [2]. A special TFET geometry which favors vertical tunneling (see Fig. 1) was simulated to compare both quantization correction methods. The results are plotted in Fig. 2. The good agreement between the two models suggests that the simpler model for quantum correction is as effective as the elaborate model.

In addition to the above-described quantization effects, there are various non-idealities present in a TFET which are often neglected in TCAD-based or quantum-transport simulations of BTBT. They include surface roughness, roughness at material interfaces (for a heterojunction TFET), interface traps, bulk traps, and others. In this work, we present ways to model the effect of DOS tails and surface roughness within a semi-classical framework.

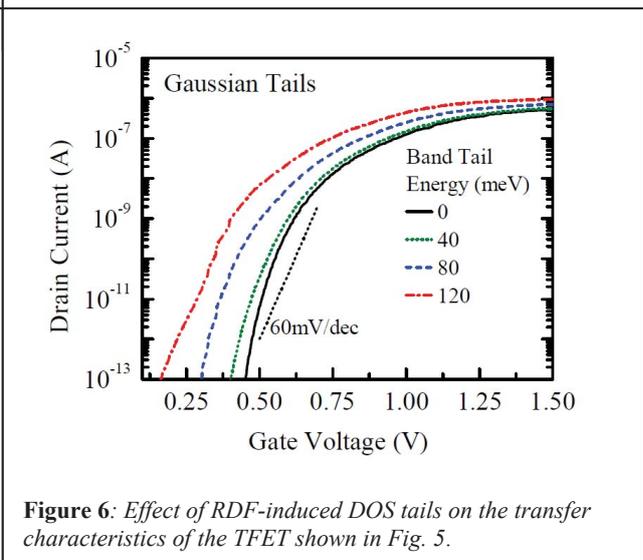
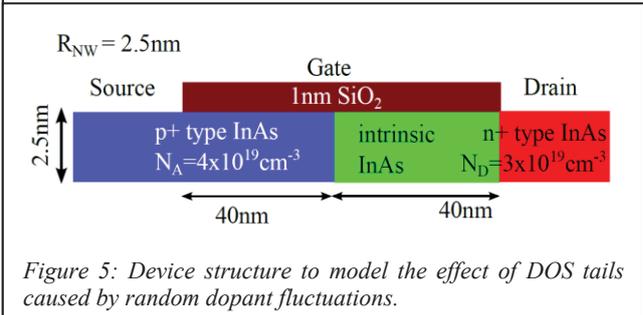
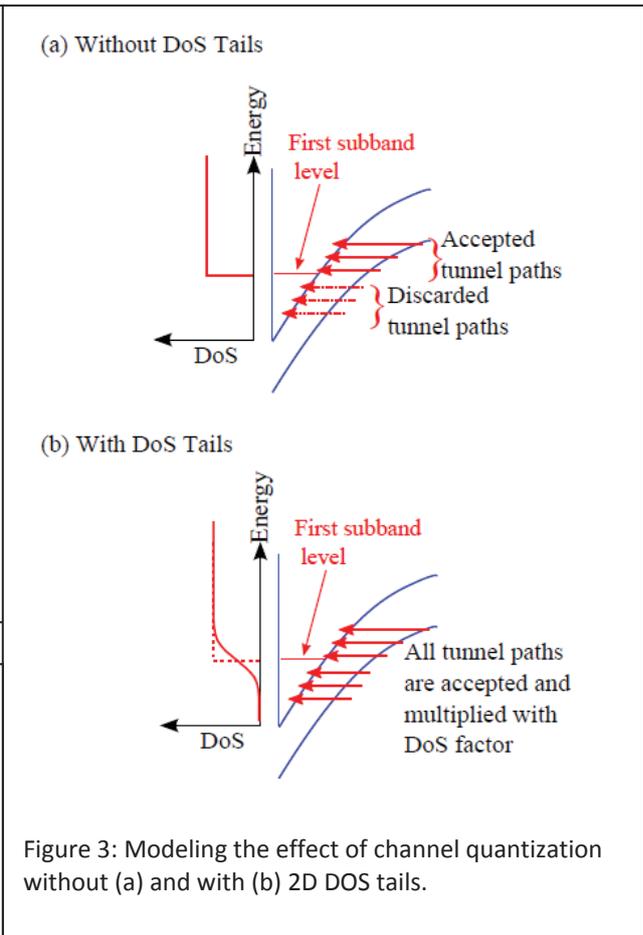
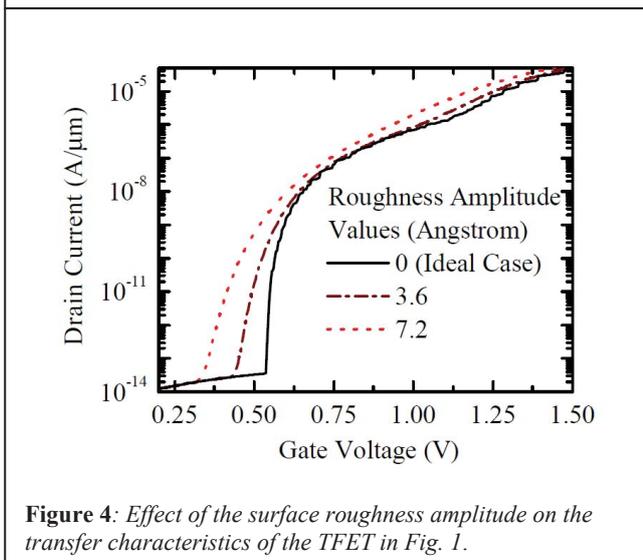
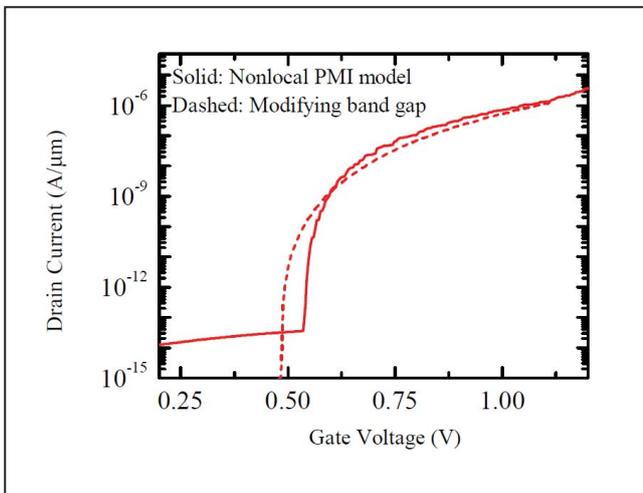
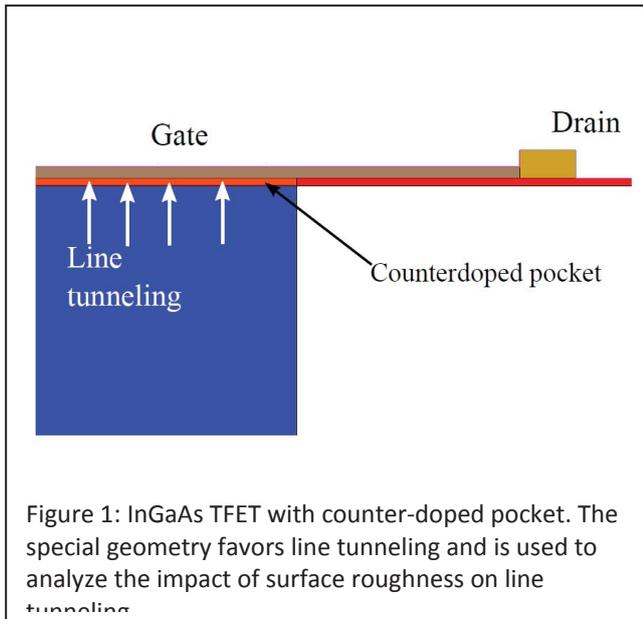
In the absence of surface roughness, the sub-band levels are well defined and the 2D DOS has the well-known staircase form. A rough oxide-semiconductor interface causes random fluctuations of the boundary wall of the triangular-like potential well. As a consequence, the step-like DOS smears out to form tail states as shown in Fig. 3(b). A simplified model for 2D DOS tails originating from an arbitrary random field has been derived by Quang and Tung [5]. Here, we apply their model to the case of a random potential due to surface roughness. Instead of rejecting the tunnel paths below the lowest sub-band energy, the energy of the tunnel path relative to the ideal sub-band level is determined and the DOS factor is calculated for this relative energy. The spectral tunnel rate from the “dynamic nonlocal path BTBT model” is then multiplied with the 2D DOS to obtain the integrated tunnel rate. This approach has been made available in Sentaurus-Device by modifying the code for the PMI model of channel quantization. The same “vertical” TFET as shown in Fig. 1 was simulated using the above model. Its transfer characteristics without and with the inclusion of 2D DOS tails due to surface roughness are presented in Fig. 4.

Kane’s model of DOS tails [6] includes the effect of random dopant fluctuations (RDF) [6]. Following his tail-state description, we derived a semi-analytical expression of the generation rate to model the effect of RDF-induced DOS tails in the frame of trap-assisted tunneling. This model was implemented in Sentaurus-Device using the PMI for “nonlocal recombination”. To analyze the impact of RDF-induced tail states on TFETs, we simulated a gate-all-around InAs nanowire TFET (see Fig. 5). The transfer characteristics of this device with and without RDF-induced DOS tails are presented in Fig. 6. One observes an earlier onset of tunneling and a degradation of the sub-threshold swing (SS) as consequence of the tail states.

The impact of bulk and interface traps (material interface and gate oxide) on the SS will be demonstrated in comparison to experimental data on InAs/Si nanowire hetero TFETs fabricated at IBM Research-Zurich [7].

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Intrinsic Voltage Gain of Line-TFETs and Comparison with Other TFET and MOSFET Architectures

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The intrinsic voltage gain (A_V) is for the first time experimentally analyzed for a planar Line-TFETs and its performance is compared with different MOSFET and point TFET architectures (FinFET and GAA:Gate-All-Around) at both room and high temperatures. The Line-TFET shows a much better intrinsic voltage gain than all studied MOSFET devices (FinFET and GAA). However, when it is compared to other TFET structures, Line-TFETs show a worse A_V . Besides the A_V , a higher on-state current was obtained for Line-TFETs, which leads to a good compromise for analog application.

1. Introduction

Tunnel-FETs have drawn the attention of the international community, as an alternative for MOSFETs, when focusing on extremely small technology nodes, due to their high speed switching capability [1]. However, some recent work has also pointed out the great potential of these devices for analog applications [2-4].

In this work the planar heterojunction Line-nTFET is analyzed experimentally through the basic analog parameters, focusing mainly on intrinsic voltage gain. The intrinsic voltage gain of this Line-TFET is compared with different architectures like FinFET (MOS and TFET) [2] and Gate-all-around (MOS and TFET) [5], for temperatures ranging from room temperature to 150°C.

2. Device Characteristics

The Si/SiGe heterojunction Line-nTFET devices were fabricated in imec/Belgium. The highly doped ($1 \times 10^{20} \text{ cm}^{-3}$) $\text{Si}_{0.55}\text{Ge}_{0.45}$ source extends under the gate and is capped with a thin intrinsic silicon pocket layer. The source and the drain regions are separated by a nominally undoped Si channel.

The gate stack is composed by a 1nm interfacial SiO_2 layer followed by 1.8nm of HfO_2 and 2nm of TiN. The channel width (W) ranges from 110nm to 200nm and two different gate lengths were evaluated (1 μm and 130nm).

Figure 1 presents a schematic structure of a Line-TFET and more details on this structure/fabrication can be found in [6].

3. Results and Analysis

In Line-TFETs the source extends under the gate region increasing the tunneling junction area where tunneling occurs in the same gate electric field direction because the gate does not overlap the channel region (intrinsic region between source and drain) avoiding point tunneling. This architecture results in a high on-state current (figure 2). It is also possible to observe from the transfer characteristics that the smaller the drain bias (V_{DS}) the steeper is the drain current (I_{DS}) in the subthreshold region. The SS improvement becomes

even more pronounced with increasing gate length and consequently the tunneling area as reported in [6]. However, evaluating the I_{DS} as a function of V_{DS} (figure 3), it is clear that at low gate bias the output characteristic is degraded and becomes inappropriate for analog applications.

Considering that the intrinsic voltage gain (A_V) is an important figure of merit for analog analysis of the transistors, the transconductance (g_m) and output conductance (g_D) were evaluated for different bias, channel lengths and channel widths, aiming to optimize the Line-TFET A_V performance.

Besides that the g_m increases with V_{GS} (due to the higher overlap between bands), the Line-TFETs present a larger tunneling current and also a higher g_m for longer channel length due to the larger tunneling junction area underneath the gate as shown in figure 4 (source / Si pocket). Evaluating the g_D parameters (figure 5), a smaller gate length dependence is observed but a high dependency on drain bias and for high V_{DS} the TFET devices operate more in the “saturation like” region, resulting in a better g_D .

The g_D and g_m parameters were also evaluated for different channel widths (W) at high V_{GS} (1.5V) as a function of drain bias (figure 6). Although the drain bias does almost not affect the transconductance, g_m increases with the channel width as expected. On the other hand, the output conductance (g_D) depends on both the drain bias and the channel width. While the channel width increases, the drain current also increases which degrades the output conductance. The higher drain bias contributes to the g_D improvement as previously observed (the TFET operates more in “saturation like” region).

Since the A_V corresponds to the g_m over g_D ratio, the output characteristic improvement associated with a V_{DS} increase leads to an optimization of the bias operation point for the analog performance of Line-TFETs. Although the dispersion of the A_V values among different channel widths and lengths is not that high, the best A_V values were obtained for the device with $W=130\text{nm}$ and $L=1\mu\text{m}$ in the studied temperature range (figure 7). Taking this device as a reference, a comparison of this planar Line-TFET among different devices (MOS and TFET) architectures (FinFET and GAA) was performed.

The first comparison, shown in figure 8, is focused on the A_V performance among the planar Line-TFET and transistors fabricated with the FinFET structure (tunnel-FET and MOSFET) for temperatures ranging from 25°C to 150°C. From this comparison it is possible to see that although the Line-TFETs A_V is smaller than

the one obtained for the TFET with the FinFET structure, a Line-TFET presents an improvement of at least 30 dB when compared with the conventional FinFET (MOSFET technology), for the temperature range considered.

The same comparison was performed considering Line-TFETs and vertical GAA structures (TFETs with different source compositions and Si-MOSFETs) as can be seen in figure 9. Independent of the source composition, the GAA-TFETs present higher A_V values than the Line TFETs. However when the Line-TFET is compared with a GAA MOSFET, the Line TFET seems to be better again.

Although Line-TFETs do not reach A_V values as high as for GAA-TFETs and Fin-TFETs, when a high on-state current is required, planar Line-TFETs can be considered as an alternative, since it reaches on-state currents much higher than the other TFET structures studied in this paper.

4. Conclusions

This paper presents for the first time the intrinsic voltage gain of Line-TFETs and shows that although this planar TFET architecture does not present the highest A_V values when compared with the two other

vertical TFET architectures (FinFET-TFET and GAA-TFET), the Line-TFET can be a good alternative to replace MOSFETs since it reaches high on-state currents and a better intrinsic voltage gain than the advanced MOSFET architectures (at least 30dB higher than FinFETs and 10dB higher when compared with GAA-MOSFETs).

5. Acknowledgements

The authors would like to thank CNPq, FWO and FAPESP for the financial support during the execution of this work and the support from the imec's Logic Device Program and its Core Partners.

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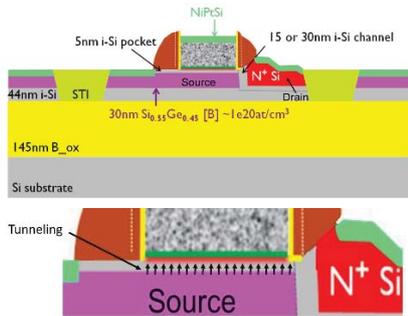


Fig.1 – Line-TFET structure.

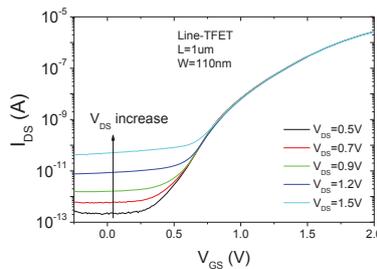


Fig. 2 – The transfer curves of a Line-TFET for different drain bias.

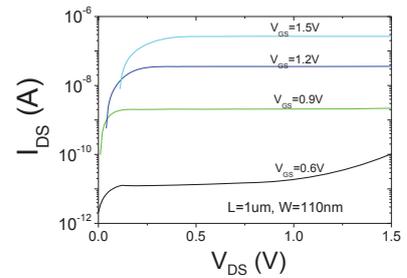


Fig. 3 – Output characteristic of a Line-TFET for different drain bias.

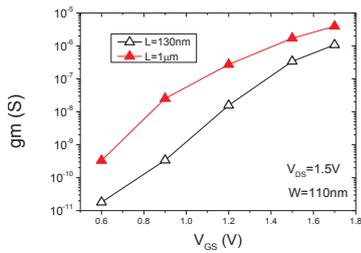


Fig. 4 – Transconductance as a function of gate bias for different channel lengths.

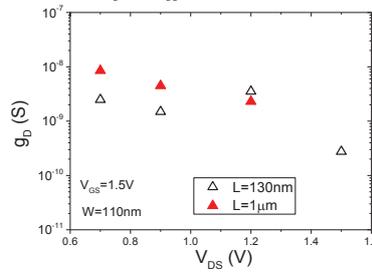


Fig. 5 – g_m as a function of drain bias for different channel lengths.

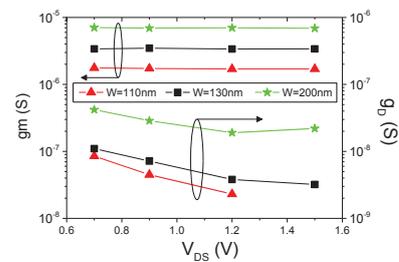


Fig. 6 – g_m and g_D as a function of drain bias for different channel widths.

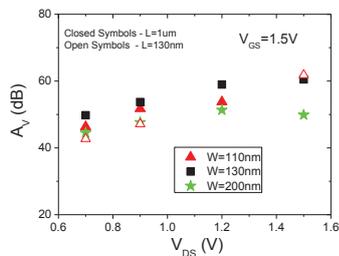


Fig. 7 – A_V behavior as a function of V_{DS} for Line-TFETs with different channel widths and lengths.

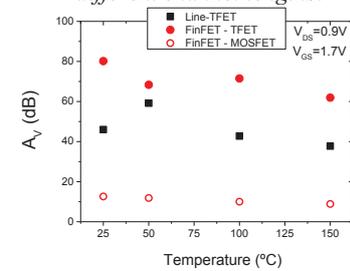


Fig. 8 - Experimental comparison of A_V as a function of temperature among Line-TFET, FinFET-TFET and FinFET MOSFET.

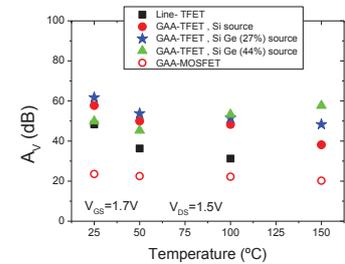


Fig. 9 – Experimental comparison of A_V as a function of temperature among Line-TFET, GAA-TFET (with different source compositions) and GAA-MOSFET.

Optimization of GaSb/InAs TFET Exploiting Different Strain Configurations

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A simulation study of heterojunction TFETs, exploring the possibility of performance improvements related with the application of appropriate stress conditions, is performed. It is shown that biaxial tensile strain induces a remarkable enhancement of the on-state current due to bandgap reduction. However, a careful optimization of the device geometry and strain level must be carried out, in order to preserve the device subthreshold swing and leakage current.

1. Introduction

There is wide consensus on the use of heterostructures with staggered or broken-gap lineups to boost the TFET on-state current. However, a careful optimization of the device geometry, doping levels, and gate-stack is required to improve their output performance.

Process-induced strain is normally used in Si-based CMOS devices to maintain the historical performance trend over different technology generations. This is due to the stress capability to increase the average carrier mobility and the injection velocity into the channel [1]. Recently, it has been asserted that a substantial performance improvement of homojunction InAs nanowire (NW) TFETs can be achieved by using appropriate stress conditions [2]. Stress, however, introduces an additional degree of freedom with a strong impact on a number of physical parameters, such as bandgap, effective mass, and, thus, density of states and degeneracy level in the source and drain regions. Therefore, identifying stress conditions able to boost the on-state current with no appreciable degradation of the off-state current and subthreshold swing, is a challenging goal. In this work, we carry out a global performance optimization of a heterojunction NW TFET, accounting for appropriate stress conditions.

2. Device under study

The investigated device is a GaSb/InAs heterojunction NW TFET, widely studied in the last few years [3]. The starting device, sketched in fig.1, has a square cross section with $T_{\text{side}} = 5$ nm, $EOT = 1$ nm, $L_G = 17$ nm, $N_S = 5 \times 10^{19}$ cm⁻³, $N_D = 1 \times 10^{18}$ cm⁻³, and is similar to the TFET investigated in [2].

The in-house simulator employed for the present investigation is based on a 8-band $\mathbf{k}\cdot\mathbf{p}$ Hamiltonian [3], to accurately model multiband effects and the complex device band structure. The Hamiltonian is extended to take into account strain, using the Pikus-Bir formalism [4].

The energy dispersion relationships of an InAs NW with $T_{\text{side}} = 5$ nm and [100] transport direction are shown in figs. 2 and 3 for the unstrained and strained conditions: biaxial tensile ($e_{yy} = e_{zz} = 2$ GPa), biaxial compressive ($e_{yy} = e_{zz} = -2$ GPa), uniaxial compressive ($e_{xx} = -2$ GPa), uniaxial tensile ($e_{xx} = 2$ GPa). Both biaxial tensile and uniaxial compressive

stress shift up the valence band, but biaxial tensile stress also lowers the conduction band, and thus obtains the largest reduction of the energy gap and of the imaginary wave-vector in the gap. A similar trend is obtained for GaSb (not shown). Another important strain effect is the alignment between the source valence and channel conduction bands at the heterojunction (ΔE_C). This parameter is strictly related to the tunnelling probability at the source/channel junction and, thus, to the device on-state current. Fig. 4 compares the I-V curves of a 5×5 nm² GaSb/InAs heterojunction NW TFET for different stress conditions. The biaxial tensile stress reduces the transistor V_T and increases the on-state current, while the uniaxial compressive stress has a smaller impact on the I-V curve.

A careful optimization of the applied strain level and the device geometry (i.e. cross section size and channel length) must be carried out to optimize the device performance. For example, the effect of the channel length and of device width are shown in Figs. 5 and 6, respectively. For an unstrained 10×10 nm² device, an I_{ON} improvement of 160% is achieved at $V_{\text{DD}} = 0.3$ V with respect to the smaller device; however, ambipolarity causes an unacceptable performance degradation when stress is applied, because of the large bandgap reduction ($\sim 70\%$). For zero source and drain degeneracy, a V_{DD} lower than the bandgap should in principle be applied to prevent ambipolarity [5]. Therefore, a moderate strain is preferable (1 GPa instead of 2 GPa) and drain engineering is required. At the end, the optimization leads to a device with $L_G = 40$ nm, $T_{\text{side}} = 7$ nm subject to a biaxial tensile stress of 1 GPa (see Fig. 7).

3. Conclusions

A TFET optimization study under appropriate stress conditions is carried out, using an 8-band $\mathbf{k}\cdot\mathbf{p}$ simulator, suitably extended to take into account strain. The investigation shows that biaxial tensile strain induces a remarkable I_{ON} enhancement, due to bandgap reduction and a more favorable band lineup at the heterojunction. However, in order to take advantage of stress, a very tight control of the fabrication processes is required, due to the strong interaction among bandgap narrowing, ambipolarity effects, DOS and tunnel-mass variation. This involves a global device optimization addressing cross section and length, as well as strain conditions and intensity.

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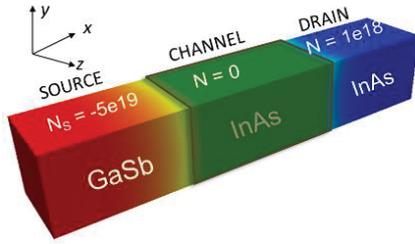


Fig. 1: Schematic view of the device under investigation.

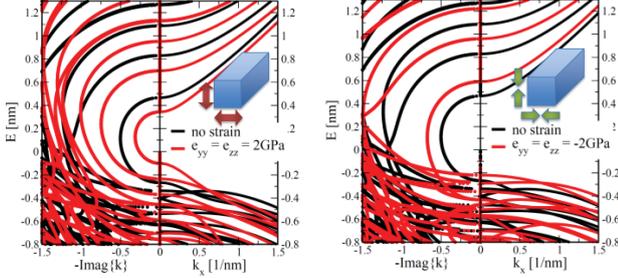


Fig. 2: Subband configuration of an InAs nanowire with $T_{side} = 5$ nm and $[100]$ transport direction. Left: biaxial tensile ($e_{yy} = e_{zz} = 2$ GPa). Right: biaxial compressive ($e_{yy} = e_{zz} = -2$ GPa). Biaxial tensile shifts up the valence band and lowers the conduction band, thus obtaining the largest reduction of the energy gap ($\sim 40\%$) and of the imaginary wave-vector in the gap. Instead, the bandgap increases for biaxial compressive stress.

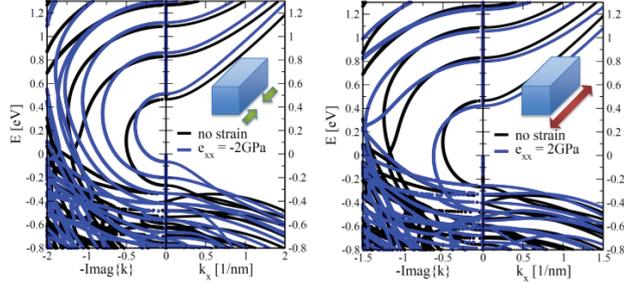


Fig. 3: Subband configuration of an InAs nanowire with $T_{side} = 5$ nm and $[100]$ transport direction. Left: uniaxial tensile ($e_{yy} = e_{zz} = 2$ GPa). Right: uniaxial compressive ($e_{yy} = e_{zz} = -2$ GPa). Uniaxial compressive stress shifts up the valence band, providing a bandgap reduction of 24% , whereas the gap reduction is modest for uniaxial tensile ($\sim 8\%$).

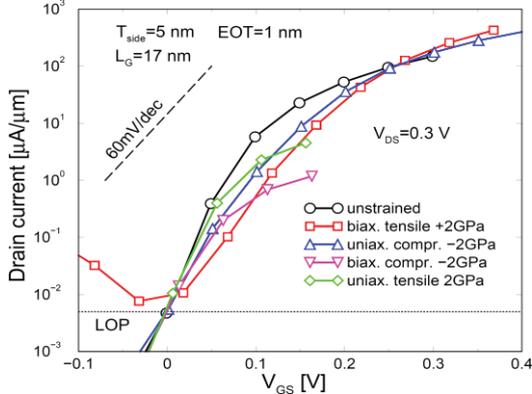


Fig. 4: Turn-on characteristics of a 5×5 nm² GaSb/InAs NW TFET for different stress conditions. The current is normalized by device side and the curves are shifted to match the I_{off} target of the LOP application (5 nA/ μ m). $V_{DS} = 0.3$ V. The biaxial tensile stress increases the on-state current, whereas the uniaxial compressive stress has a smaller impact on the I-V curve.

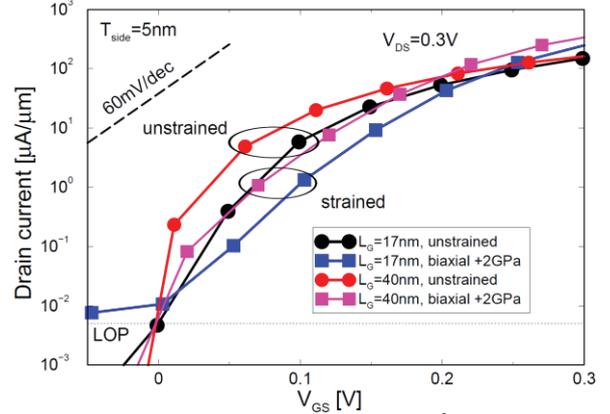


Fig. 5: Turn-on characteristics of a 5×5 nm² GaSb/InAs NW TFET for $L_G = 17$ and 40 nm for different stress conditions. The current is normalized to the cross-section side and the curves are shifted to match the I_{off} target of the LOP application (5 nA/ μ m). $V_{DS} = 0.3$ V. The increase of L_G from 17 nm to 40 nm provides a decrease of the leakage current, a slope improvement, and a higher on-state current. For the biaxial tensile stress condition a 37% increase in I_{ON} ($V_{GS} = V_{DD}$, $V_{DS} = V_{DD}$) can be achieved.

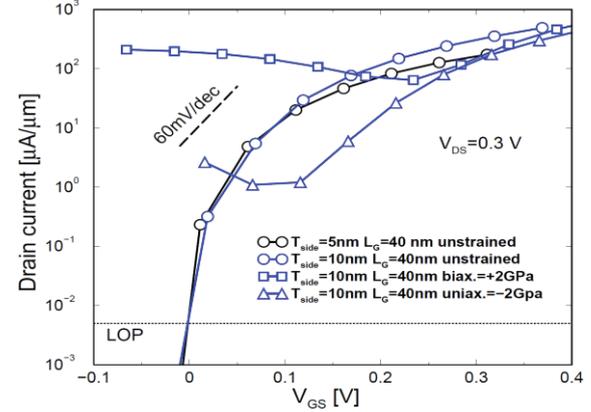


Fig. 6: Comparison of the turnon curves of a 10×10 nm² GaSb/InAs NW TFET for different stress conditions (2 GPa). The current is normalized to the cross section side and the curves are shifted to match the I_{off} target of the LOP application (5 nA/ μ m). $V_{DS} = 0.3$ V. The I-V curve of the unstrained 5×5 nm² is also shown for comparison.

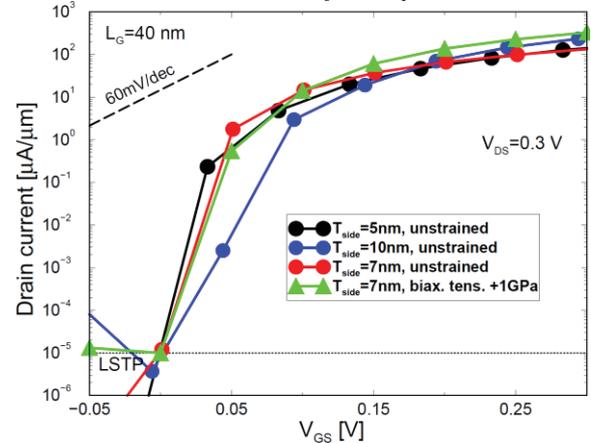


Fig. 7: The current is normalized to the cross section side and the curves are shifted to match the I_{off} target of the LSTP application (10 pA/ μ m). For $V_{DS} = 0.3$ V the largest on-current is achieved with $T_{side} = 7$ nm, $L_G = 40$ nm and applying a biaxial tensile stress of 1 GPa.

Assessment of Confinement-Induced Band-to-Band Tunneling Leakage in the FinEHBTFET

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1. Introduction

The novel FinEHBTFET [1] proves to be a promising structure for its scalability potential compared to conventional planar EHBTFETs, which are devices that exploit band-to-band tunneling (BTBT) phenomena between 2D electron and hole gases. The drive current in planar EHBTFETs is due to vertical BTBT in the central part of the channel where top and bottom gates overlap [2]. Therefore, the tunneling area is proportional to the overlapping length. The FinEHBTFET changes this conception by inserting a narrow gated fin on top of a $n^+ - i - p^+$ diode as depicted in Fig.1. This structure allows to increase the tunneling area by using higher fins without impacting the required wafer area and preserving the device density.

However, when quantum mechanical confinement is taken into account in the FinEHBTFET, a series of harmful parasitic lateral tunneling processes arise besides the so far expected effective bandgap widening phenomena. In this work, we analyze the origin of these deleterious parasitic contributions and show how to get rid of them, restoring the abruptness of the $I_{DS} - V_{FG}$ curves.

2. Device structure and simulation approach

The FinEHBTFET of Fig.1 is made of germanium and features a source p^+ region (10^{20} atoms/cm³); an intrinsic channel region (10^{15} atoms/cm³) with a central overlap between the gates inside the fin, and side underlaps at the bottom; and a drain n^+ region (10^{20} atoms/cm³). The body and fin thickness, t_{body} and t_{fin} , respectively, are chosen to be 10nm. Front and back gate dielectrics are 3nm-thick HfO₂ layers. Gate workfunctions are engineered for every polarization so that subband alignment in the fin is attained at very low front gate voltage, V_{FG} . Namely, we choose $V_{FG,align}$ to be 0.04V. In the case of germanium, optimized workfunctions turn out to be $\phi_{fg,ol}=3.06$ eV, $\phi_{fg,ul}=4.50$ eV and $\phi_{bg}=5.05$ eV. Back gate voltage, V_{BG} , will be set to 0V and V_{DS} fixed to 0.3V. The simulation approach that we follow has been extensively tested [3,4,5] and consists of a hybrid integration of ATLAS and Sentaurus TCAD simulators that allows to account for field-induced quantum confinement by segmenting each simulation run into two consecutive steps: (i) derivation of the electrostatics through selfconsistent resolution of Schrödinger-Poisson equations, and (ii) postprocessing computation of BTBT injection.

3. Results and discussion

Apart from the expected bandgap increase induced by confinement, a series of leakage lateral tunneling processes entailing a significant degradation of the potential abrupt switching performance are found to show up in the FinEHBTFET before the triggering of BTBT inside the fin at $V_{FG}=V_{FG,align}=0.04$ V. Analogous parasitic tunneling currents are known to appear in planar EHBTFETs [3,6,7].

First, as a result of scaling down the device compared to conventional EHBTFETs, direct S/D BTBT (Fig.2 top) arises. Its suppression is carried out by replacing the body material with another featuring higher bandgap. In our case, we replace Ge by Si_{0.6}Ge_{0.4} (Fig.2 bottom). Second, if we arranged $\phi_{fg,ol}$ and $\phi_{fg,ul}$ to be the same, we would get parasitic lateral tunneling from the bottom of the fin to the front gate underlap (Fig.3) due to the different strength of quantization effects inside and outside the fin. A heterogate solution (Fig.1) proves to be very effective in eliminating this parasitic current flow. Third, as a result of the push-up effect that subbands undergo inside the fin as we approach its bottom side (Fig.4), diagonal alignment between E_{el} and E_{hh1} is favored at $V_{FG}<0.04$ V and, therefore, well before the appearance of horizontal BTBT responsible for the drive current of the device. Fig.5 confirms the presence of a certain BTBT generation rate following these diagonal paths inside the fin. In order to remove this leakage current, we insert a n-doped buffer (3×10^{18} cm⁻³) of 10nm at the bottom of the fin so that E_{hh1} would be lowered in that region (Fig.6) and diagonal BTBT prevented for $V_{FG}<V_{FG,align}=0.04$ V. The resulting $I_{DS} - V_{FG}$ curves from implementing the different solutions proposed above are displayed in Fig.7. It can be seen the crucial role of our proposal for making the FinEHBTFET become an appealing steep slope switch for very low power operation. We report for the best characteristic of Fig.7 a point swing of $SS_{pt}=1.6$ mV/dec at the onset of BTBT; and an average swing of $SS_{av}=40.5$ mV/dec estimated between $V_{FG}=V_{FG,align}$ and $V_{FG}=V_{DD}=0.3$ V. Reduced bandgap materials with direct BTBT like InAs are expected to provide enhanced I_{ON} levels.

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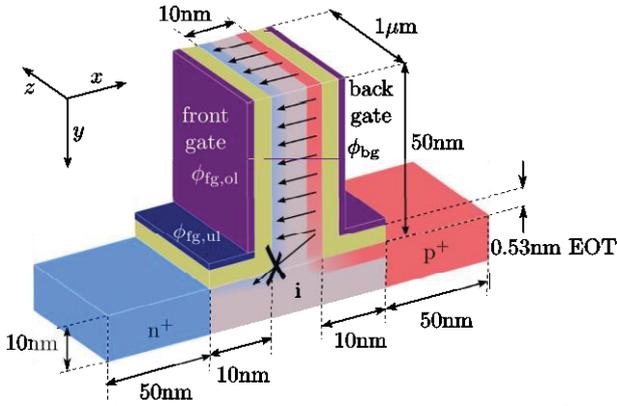


Fig.1: Schematic representation (not to scale) of the FinEHBT FET. This setup decouples the occupied wafer area from the BTBT area responsible for the ON-state current level. Parasitic lateral tunneling to the front gate underlap is suppressed by means of a heterogate configuration.

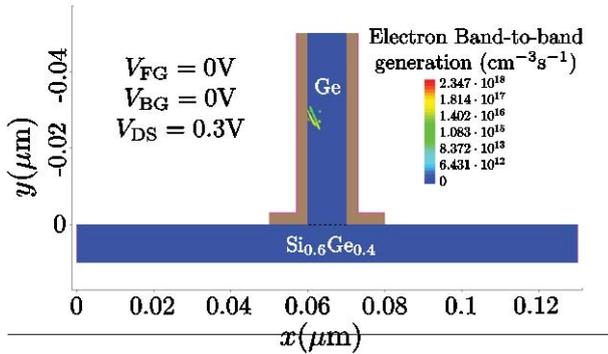
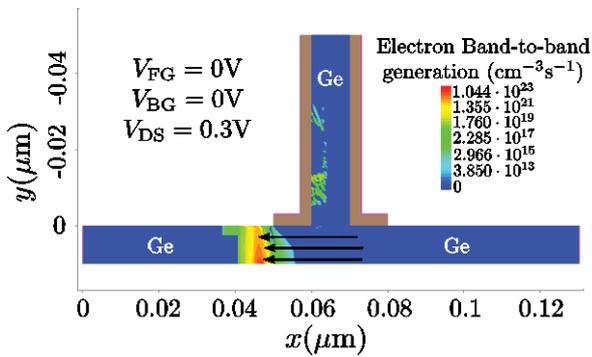


Fig.2: (Top) Electron BTBT generation rate due to direct S/D tunneling. (Bottom) Direct S/D BTBT is suppressed when we replace Ge by $\text{Si}_{0.6}\text{Ge}_{0.4}$ everywhere except in the fin.

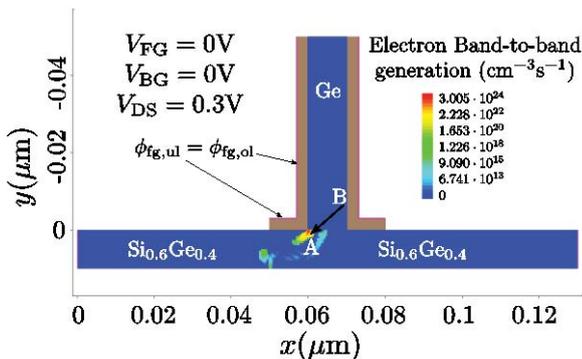


Fig.3: Parasitic lateral BTBT from the bottom of the fin to the front gate underlap at $V_{FG}=0V$ when $\phi_{fg,ol} = \phi_{fg,ul}$.

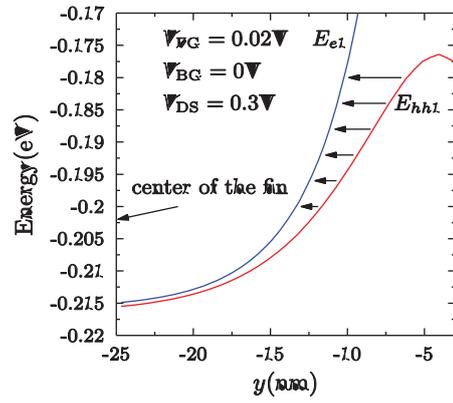


Fig.4: Subband profiles along vertical cuts taken at 1nm from the gate interfaces demonstrating parasitic lateral BTBT paths from the bottom to the center of the fin at $V_{FG}=0.02V$.

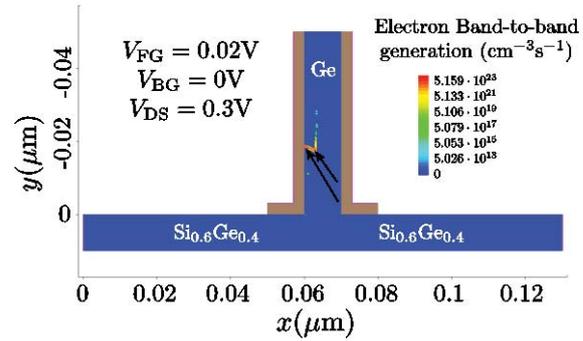


Fig.5: 2D map of the electron BTBT generation rates at $V_{FG}=0.02V$.

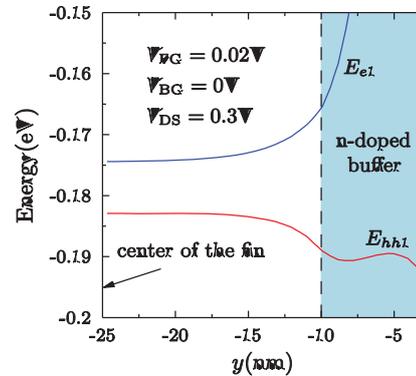


Fig.6: Vertical E_{hh1} and E_{e1} cuts at $V_{FG}=0.02V$ resulting from the inclusion of the buffer.

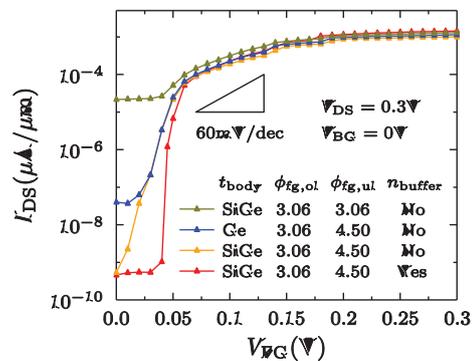


Fig.7: $I_{DS}-V_G$ curves resulting from the different optimization solutions for the FinEHBT FET leading to the removal of parasitic lateral tunneling contributions.

Process Modules for GeSn Nanoelectronics with High Sn Contents

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1. Introduction

GeSn is a group IV alloy that rapidly evolved within the last years. The availability of high-Sn content and strain relaxed layers allowed the proof of a fundamental direct bandgap (DBG) in a group IV alloy grown on Si [1]. The direct gap GeSn is not only beneficial for photonic applications but it might also serve as performance booster for electronics due to increased mobility of Γ -electrons (small effective mass & reduced scattering) and by enabling direct band-to-band tunneling in tunnel field effect transistors (TFETs).

Theoretical k.p-calculations predict a significant mobility enhancement as soon as the population of Γ -valley increases. For indirect GeSn alloys till a Sn content of 9% the total mobility is given by the electrons occupying the L-valley. For larger Sn contents with direct gap GeSn, the Γ -valley becomes populated and the boost in electron mobility becomes significant. The calculated Sn-dependent Γ -valley population and mobility is presented in Fig. 1.

Preliminary works on p- and n-MOSFETs [2], [3] and even TFETs [4] based on GeSn alloys have been reported, however, with Sn-contents and strain values far below the indirect to direct transition. The low solid solubility of Sn in Ge <1at.% and the far non-equilibrium growth results in a very limited thermal budget < 350°C for Sn-contents above 10at.% making process integration challenging.

In this work we discuss advances on low-Temperature process modules (Fig.10) for GeSn-FET devices with Sn-contents up to 13at.% including high-k/metal gate stacks with densities of interface traps in the 10^{12} eV⁻¹cm⁻²-regime and low resistive NiGeSn contacts with ultra-low Schottky barrier heights. Emphases is put on the fabrication and characterization of tunneling diodes with 13at.% as well as first steps toward DBG GeSn n-FETs.

2. Experimental

As a first key module MOS-capacitors (MOSCaps) with high-k metal gate stacks on GeSn have been investigated. MOSCaps with Sn-contents between 0% (Ge-substrate) and 12.5% have been fabricated applying low temperature high-k and metal gate deposition. A set of Capacitance-Voltage (CV)-curves for different frequencies measured on TiN/HfO₂/Ge_{0.915}Sn_{0.085} is depicted in Fig.2. As a characteristic of low bandgap semiconductors the CV-curves feature strong minority carrier inversion response hindering a reliable extraction of interface trap density (D_{it}) at room temperature. By applying the low-T conductance method D_{it} values of

2×10^{12} cm⁻²eV⁻¹ have been extracted for GeSn capacitors with different Sn contents (Fig.3).

Metal-semiconductor-metal diodes based on NiGeSn/ Ge_{0.875}Sn_{0.125} Schottky contacts have been analyzed. The lowest sheet resistance was obtained by stano-germanidation at 325°C [5]. From Arrhenius plots of the current characteristics for different voltages (Fig.4) the Schottky-barrier height (SBH) was extracted by fitting the linear region and extrapolation to 0V (Fig.5). A SBH of 0.08 eV has been extracted for NiGeSn/Ge_{0.875}Sn_{0.125} (p-type). Sheet resistance of NiGeSn is shown in Fig.6 for several Sn-contents.

Having processing technology at hand as well as the possibility of *in-situ* doping we have fabricated GeSn tunneling diodes as an important step towards advanced GeSn based TFETs. We could push the Sn-content up to 13at.% as follow up to previous results with a stack of 9at.% and 11 at.% [6] enabling an even lower bandgap and higher directness of the GeSn. As proof of band-to-band tunneling negative differential resistance (NDR) is observed at low-T (Fig.9).

Combining all process modules GeSn n-FETs have been fabricated with Sn contents of 0%, 7% and 12.5% using ion implanted S/D contacts. The transfer curves of the GeSn-nFETs for a series of Temperatures and for 80 K are shown in Fig.7 and 8, respectively. The rather poor I_{on}/I_{off} ratio of the 12.5%Sn sample is associated with ion implantation damage. The limited thermal budget used in order to avoid Sn diffusion, here 350°C, was not sufficient to recrystallize the regions amorphized by ion implantation, leading to very poor junctions. The solution for maintaining crystalline GeSn is the use of *in-situ* doping and selective growth of S/D region.

3. Conclusion

We present process modules developments for GeSn-FET-devices with Sn-contents >10%. Challenges due to the metastability of GeSn can be solved by in-situ doping.

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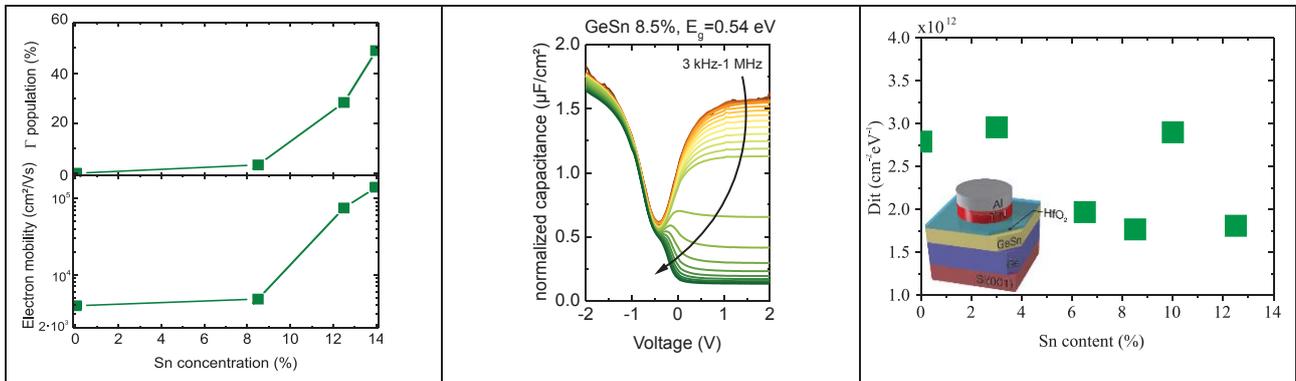


Fig. 1.: Calculated Γ -valley population (top) and the electron mobility vs Sn-content (bottom) as obtained by k.p-theory.

Fig. 2 : CV-characteristics of a TiN/ 6 nm $\text{HfO}_2/\text{Ge}_{0.915}\text{Sn}_{0.085}$ MOSCap for a set of frequencies.

Fig.3: Dit at midgap for several Sn-contents.

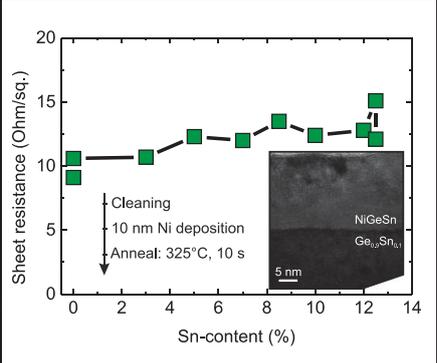
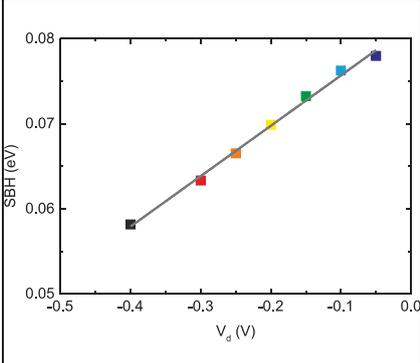
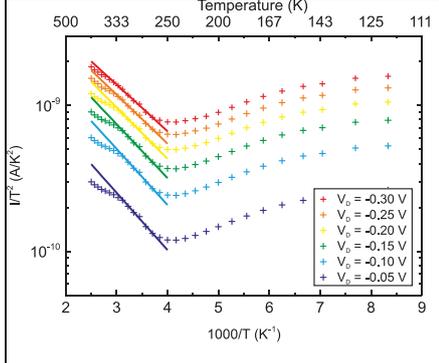


Fig.4: I - V characteristics of NiGeSn-GeSn-NiGeSn Schottky-contacts for different Temperatures.

Fig.5: Extraction of SBH by extrapolation to 0 V.

Fig 6.: Sheet resistance of NiGeSn for several Sn-contents. The inset shows a TEM-micrograph of NiGeSn on $\text{Ge}_{0.9}\text{Sn}_{0.1}$.

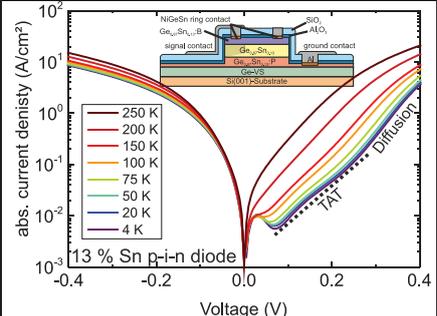
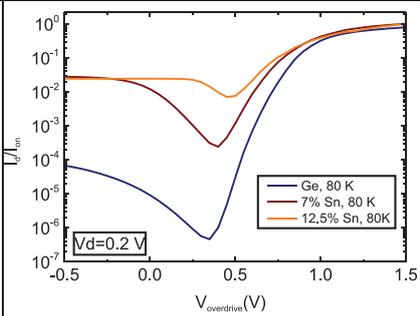
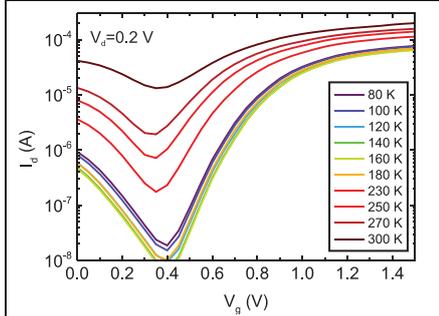


Fig. 7: Transfer characteristics of $\text{Ge}_{0.93}\text{Sn}_{0.07}$ n-FETs for several temperatures.

Fig. 8: I_d/I_{on} ratio at 80 K for several Sn-contents.

Fig.9: Temperature dependence of a $\text{Ge}_{0.87}\text{Sn}_{0.13}$ -pin-diode. The I - V -characteristic shows clear NDR for low- T .

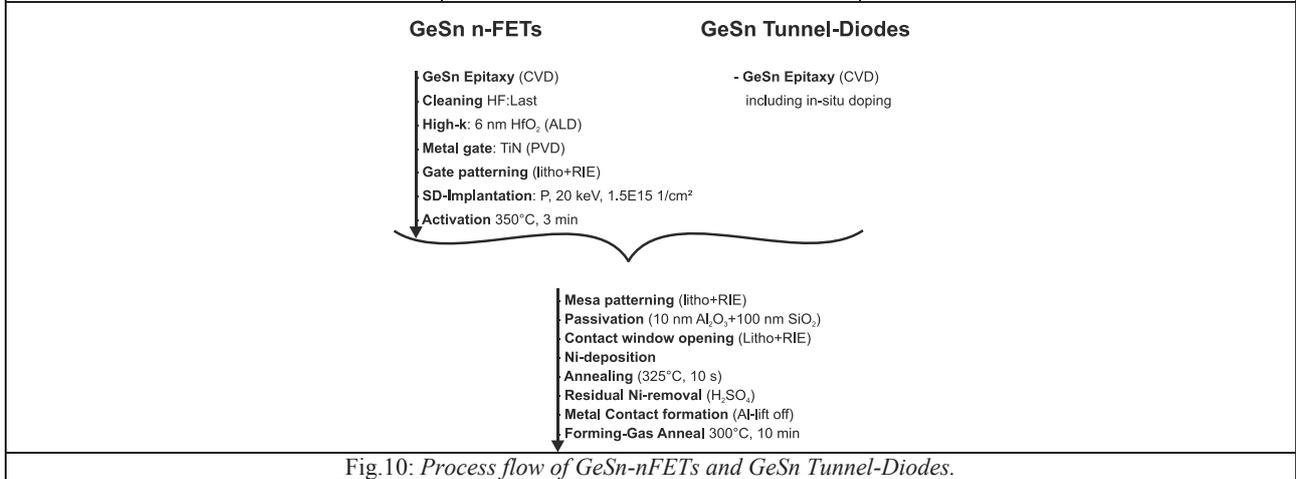


Fig.10: Process flow of GeSn-nFETs and GeSn Tunnel-Diodes.

Controlling the Physical and Electrical Properties of ALD Grown ZnO using Nb as a Dopant

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Over recent years transparent conducting oxides (TCOs) have gathered considerable interest due to their ease of fabrication, low cost, relatively high mobility, conductivity and optical transparency. This has allowed for the possibility of fully transparent electronics being integrated into such applications as heads-up display on windscreens, active matrix displays and local environmental control. For active matrix displays, zinc oxide (ZnO) based materials have been the favourable choice in thin film transistors (TFTs). As-grown ZnO suffers from a large number of defects giving rise to unacceptably high conductivity, hence the requirement of materials such as indium and gallium (IGZO). The gallium serves to stabilise the structure and hence the threshold voltage and the indium to increase the mobility [1]. However, indium suffers from large fluctuations in cost and has a low level of abundance which makes it not viable for long-term mass production. Currently extensive research into non-indium based materials is being conducted for ZnO based TFTs including; gallium [2], silicon [3] and our own work on magnesium [4]. Niobium is an attractive dopant candidate for ZnO, as its high valency (Nb^{5+}) offers the prospect of requiring lower concentrations as a substitutional dopant for Zn^{2+} and consequently reduced disorder and carrier scattering. Nb-doping has been explored previously in pulse laser deposited NbZnO TCO's, but not via atomic layer deposition (ALD) using the approach reported here. Here we report fabrication and performance of TFTs using ALD grown NbZnO as an active n-channel layer. Furthermore, the multiple trapping and release (MTR) model is applied to fit the TFT experimental data.

The films were grown via ALD at 200 °C using precursors diethylzinc and niobium pentaethoxide for ZnO and Nb respectively on an oxidised Si wafer (50 nm SiO_2) with 10 nm of ALD Al_2O_3 to act as a capping layer. The films were annealed at 300 °C in air for 1 hour. Fig.1(a) shows a Tauc plot derived from variable angle spectro-ellipsometry measurements where NbZnO and ZnO films are compared. There is an evident shift of the absorption edge for NbZnO towards higher energy, being indicative of a band gap energy increase of about 0.1 eV in comparison to the ZnO sample for a low cycle ratio of Nb cycle percentage of 3.8%. Fig.1(b) shows the effect on the band gap of increasing cycle percentages of Nb where at 12.5% the band gap is 3.48 eV, an increase of 0.2 eV.

Simple back-gated TFTs were fabricated on oxidised n^{++} Si wafers (50 nm oxide) with a thin buffer layer of alumina. The TFTs were isolated by wet-etching and

lift-off was used to form Al electrodes. Fig.2 shows a comparison between ZnO and 3.8% NbZnO TFT characteristics. The transfer characteristics in Fig.2(c) illustrate that the addition of a small concentration of Nb effectively reduces the conductivity of the film and in turn drastically reduces the off-current by from 10^{-8} to 10^{-12} A: 4 orders of magnitude. Furthermore, good current saturation, relatively low threshold voltage (V_T) and a low sub-threshold swing (SS) of 0.51 V/dec are seen. The addition of Nb results in an increase of the saturation mobility (μ_{sat}) from 1.41 to 5.13 cm^2/Vs . Table 1 summarises and compares TFT characteristics of varying amounts of Nb content. Higher Nb contents cause reduction of the μ_{sat} and SS (related to interface states and disorder in the film), whilst the *On/Off* ratio remains within reasonable levels. The aforementioned extracted parameters assume the validity of standard Si MOSFET theory in these accumulation mode devices; a commonly used assumption in the literature which allows for easy comparison of technologies. However, it is evident from the transfer characteristics in Fig.2(c), that the TFT does not follow distinct sub-threshold and quadratic regions. The transport mechanism MTR is employed to explain the characteristics [5,6]. An exponential density of defect states, $g(E) \sim \exp\left(\frac{E-E_c}{kT_o}\right)$ is assumed, where T_o is a characteristic temperature related to the degree of disorder in the film (E_c is the conduction band edge). This treatment leads to a power-law dependence of the transfer characteristics. Using this model, a good fit is observed in Fig.3 for both transfer and output characteristics, where a lower level of disorder within the film is evident from the value $T_o = 656$ K, compared to 710 K for our MgZnO films [7].

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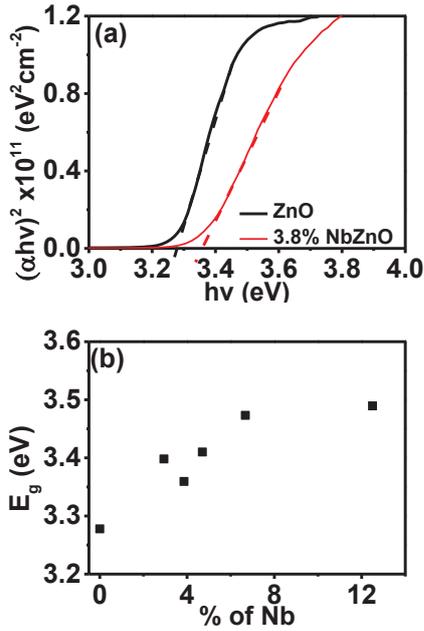


Fig 1:(a) Tauc plot for ZnO and NbZnO where α is the absorption coefficient and $h\nu$ is the photon energy (b) Summary of band gap (E_g) increase with increase cycle percentage of Nb from 0% to 12.5%

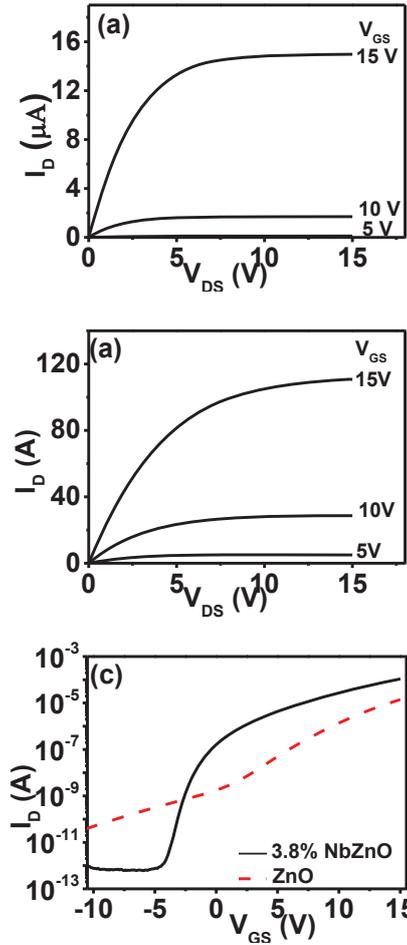


Fig 2: Output characteristics for the (a) ZnO and (b) 3.8% NbZnO and (c) transfer characteristics of 3.8 % NbZnO and ZnO, where $V_{DS}=15\text{ V}$

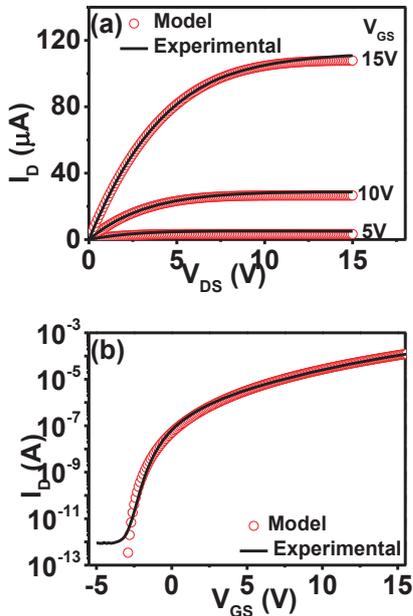


Fig 3: (a) output and (b) transfer fittings of the 3.8% NbZnO TFT using the MTR model. The fitting parameters are; $V_{FB}=-3.12\text{ V}$, $T_o=656\text{ k}$, $\beta=3\times 10^{-11}$ and $R_D=R_S=70\ \Omega$ (model parameters are defined in [5])

Table 1: Comparison of TFT characteristics for NbZnO with varying cycle fraction from 0 to 9.1%

Nb cycle fraction (%)	On/Off ratio	V_T (V)	μ_{sat} (cm^2/Vs)	SS (V/dec)
0	1.0×10^4	9.32	1.41	2.97
3.8	1.4×10^8	7.06	5.13	0.51
4.8	1.5×10^7	4.1	0.88	0.39
9.1	3.2×10^7	3.69	0.36	0.33

Study of Ultrathin Si₃N₄ Tunnel Barriers Prepared by Atomic Layer Deposition using Single-electron Transistors

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1. Introduction

The downscaling of electronic device dimensions to a few atomic layers requires a good understanding of underlying physical and chemical processes that enable precise control of nanofabrication. In single electron transistors (SETs) [1] charge transfer through the device is controlled by the Coulomb charging energy of a nano-scaled “island”, tunnel-coupled to the source and drain electrodes and electrostatically coupled to the gate. The gate-controlled charging energy barrier, $E_C = e^2/2C$, where e is an elementary charge, is inversely proportional to the total device capacitance, C . To achieve satisfactory performance in a SET, the source and drain tunnel barriers must be only a few atomic layers thick which makes them crucially dependent on the quality of the dielectric barriers. For example, the presence of defects in the dielectric will affect noise characteristics of the SETs and non-homogeneous dielectric deposition leads to drastic changes in the SET performance. This unique sensitivity of SETs to even single charge defects in the tunnel dielectric makes them ideal for evaluating the quality of ultrathin dielectrics with “princess and the pea” sensitivity.

2. Fabrication and Experimental results

Here we present the results of experimental investigation of metal-insulator-metal (MIM) SETs where Ni source, drain and the island are fabricated by using a combination of high resolution e-beam lithography, nanodamascene process, and Si₃N₄ tunnel barrier dielectric created using plasma-enhanced atomic layer deposition (PEALD). Using a Vistec EBPG 5200 100-keV electron beam lithography (EBL) system, the pattern of the island is first defined in polymethylglutarimide (PMGI) spun on the thermal SiO₂ substrate. PMGI can be used as a mask for SiO₂ etch due to its higher etch resistance than polymethylmethacrylate (PMMA). The pattern of the island is then etched into the oxide using Ar, C₄F₈, CHF₃, and CF₄ chemistry in an inductively coupled plasma (ICP) etcher. Next, Ni is deposited by e-beam evaporation at the base pressure of $<8 \times 10^{-7}$ Torr to fill the trench in SiO₂, while the field is still covered by the PMGI mask. The evaporated metal on the field along with the underlying PMGI is then lifted off by MR-Rem 400 stripper from Micro Resist Technology, heated to 70°C. Chemical mechanical polishing (CMP) is then used to remove any residual Ni on the oxide field, while leaving the island trench filled with Ni. Next, 21 cycles of Si₃N₄ PEALD process, with Bisdiethylaminosilane (BDEAS) and N₂ plasma, is performed to form a dielectric barrier covering the island (expected thickness of 1.05 nm). Finally, Ni source and drain are defined by a second EBL and liftoff. As a last step, the die was subjected to H₂ plasma treatment to ensure reduction of NiO potentially formed during exposure of the junctions

to the ambient. Finished devices (Fig. 1a) were bonded to the chip carrier and electrically tested from 300K down to 0.3K in the closed cycle ³He refrigerator. Coulomb blockade oscillations (CBOs) were observed at $T < 3.5K$; temperature dependence of CBOs is presented in Fig. 1b. As expected for MIM SETs at $T \sim E_C/k_B$ the conductance in the peaks of CBOs reaches $G_0/2$ where G_0 is high temperature approximation of conductance through the device when Coulomb blockade is suppressed, indicating a very insignificant contribution of potential in-series NiO surface oxide in the junctions[4]. The conductance in the valleys of the CBOs is exponentially suppressed with lowering T with activation energy E_C . The analysis of SET charge stability (“Coulomb diamonds”) plot, Fig. 2a, allows evaluation of the homogeneity of tunnel barriers confirmed by simulations Fig. 2b: it reveals very similar parameters for both of the junctions. The thickness of the barrier evaluated from measurements is about 10% smaller than expected, likely due to a nucleation delay. In addition to that, the Coulomb diamonds plot also reveals very large level of excess “random telegraph signal” noise, typical for trapping/detrapping processes where conductance vs. time is strongly modulated by random trapping events [2,3].

3. Discussion and summary

MIM SETs featuring ALD Si₃N₄ as barrier dielectric were fabricated for the first time, to the best of our knowledge. Analysis of temperature dependence of conductance confirm the formation of MIM junctions with negligible in-series contribution of native surface oxide, in contrast with observations for MIM Ni-SiO₂-Ni[4] and experimentally obtained value of barrier thickness matches the calculated from the deposition rate reasonably well. However, very large magnitude of observed RTS noise indicates a large density of traps inside the tunnel junctions. Our results indicate the strong influence of interface states and surface preparation on performance of the SETs fabricated by using ALD technique. As we recently demonstrated [5], by choosing optimal treatments of the ALD layers the noise characteristics can be greatly improved. The optimization of ALD process for SiN is currently in progress.

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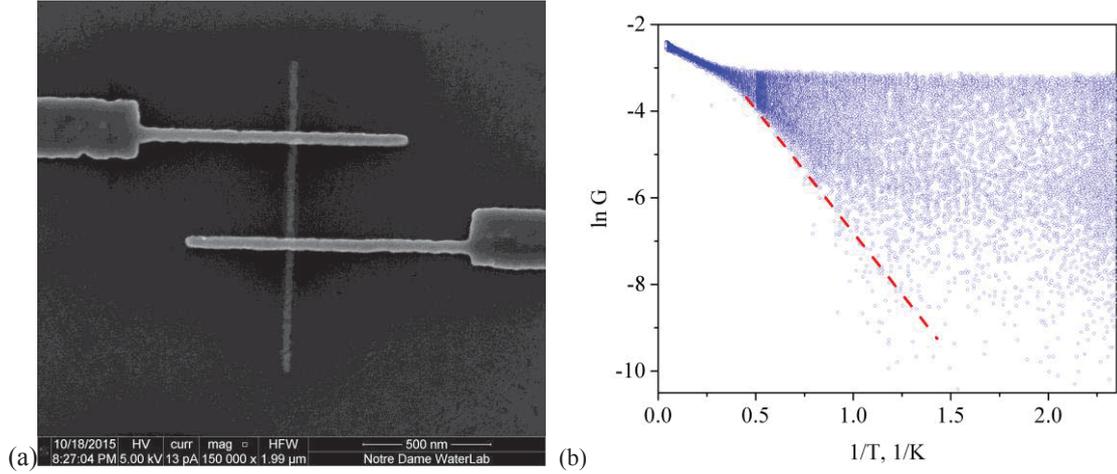


Fig.1: (a) SEM image of a fabricated SET with an island inlaid in the substrate and Si₃N₄ deposited on the island as the tunnel barrier. (b) Temperature dependence of conductance in the SET at $V_{ds}=0$. Gate voltage was continuously ramped over the range of several oscillations. The resulting plot illustrates development of both minima and maxima of CB oscillations as the temperature is lowered. Red line is a fitting of CBO minima, that corresponds to activation of the Coulomb barrier. $E_C/k_B=5.3K$ calculated from this slope matches well the value obtained from Fig 2 a(5.5K). As expected for an MIM SET conductance in the CBO peaks does not change with temperature.

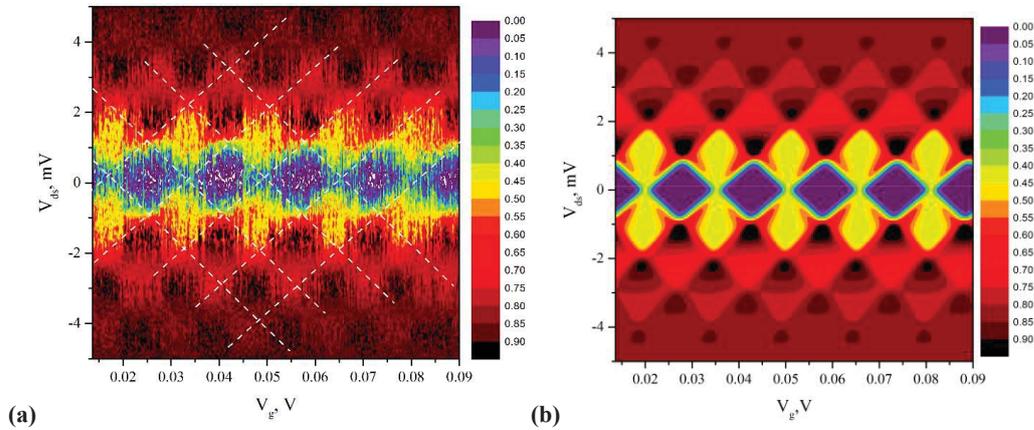


Fig.2: Charging diagrams ("Coulomb diamonds") for the SET featuring Ni-SiN-Ni tunnel junctions. Color scale represents conductance in μS (a) Experiment (b) Simulations using orthodox theory [reff] for $T=0.4K$. The values of capacitances are extracted from experimental plot: $\alpha=C_g/(C_s+C_g)=0.121$; $\beta=C_g/C_d=-0.132$ $C_g=10.5$ aF $C_d=80$ aF $C_s=77$ aF $E_C/k_B=5.5K$. The values of junction conductances are chosen to match the experiment: $G_s=G_d=0.18$ μS

Challenges of MOS Gate Dielectric Scaling in the Subnanometer EOT Range

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1. Introduction

In downsizing the CMOS gate dielectric film, the reduction rate is far slower than that suggested by the constant field scaling rule and the technology roadmap prediction even in the sense of equivalent (silicon) oxide thickness (EOT) in the last decade [1]. The slow downsizing rate was first due to the physical thickness limit of bulk silicon dioxide and the less controllable atomic layer uniformity of ultrathin film in mass production. These issues were overcome by introducing much thicker high-k metal oxide films. However, the EOT reduction could only proceed by a couple tenths of a nanometer. The much poorer properties and less thermal stability of the metal oxides hindered the further EOT downsizing. The ideal gate oxide EOT for 14 nm gate length technology should be less than half nanometer but the actual EOT used was still around 0.8 nm. We need to produce thinner EOT for maintaining further device downsizing, boosting the device characteristics, and suppressing the “off current”. When scaling towards the subnanometer range, especially around half nanometer, it is an issue of whether technologically feasible rather than the issues related to characteristic, reliability or variability degradation. The less scalable silicon/high-k and the metal gate/high-k interfaces pose the ultimate technology constraint on further EOT scaling. In this paper, we shall discuss, taking lanthanum oxide (La₂O₃) as an example, the issues and challenges of fabricating subnanometer EOT. We shall discuss the material interaction at the Si/La₂O₃ and W/La₂O₃ interfaces that leading to the EOT degradation.

2. High-k Dielectrics in Nanometer Scale

When the high-k dielectric is scaled down to a couple nanometers, its challenge will be much severer than the silicon oxide and silicon nitride of the same physical thickness. High-k oxides are often found to have much higher bulk trap (mainly the oxygen vacancies, and some cases the grain boundary states of high-k nanocrystallites)[1] than the silicon oxide ones, as a result the high-k film has much larger leakage current. The advantage of “physically thicker” will be dismissed when the physical thickness of the high-k film is reduced to a couple nanometers. In addition, direct tunneling will take place for high-k film with thickness in this range as high-k materials have much smaller band offsets with silicon and sometimes have heavier carrier effective masses [2]. Fig. 1 lists the estimated thicknesses for direct tunneling to occur for HfO₂ and La₂O₃ films. In principle, half nanometer EOT could be achieved with 3.5 nm thick La₂O₃, this

thickness is far thinner than the direct tunneling limit of La₂O₃. Significantly enhancement in gate leakage is expected.

3. Interfacing with High-k

3.1 Lanthanum oxide/silicon interface

Most high-k oxides can readily react with the interfacial silicon oxide or the silicon substrate. Depending on the process temperature, partial pressure of oxygen, several different chemical reactions may take place (see Fig.2). The reactions can lead to the formation of a silicate layer with much smaller k value. It becomes the critical constraint for half-nanometer EOT. For HfO₂ film, this interface layer was suppressed with a scavenging process [3-4]. By introducing some metals with positive Gibbs free energies and treated at sufficient high temperature, the interfacial SiO₂ can be scavenged and thus improves the EOT. The scavenging process requires a high temperature (e.g. > 800 °C) which may cause some instability issues [1]. In La₂O₃, the high-temperature treatment results in silicates formation via the calcinations process (see Figs.3 and 4). It still causes significant EOT degradation.

3.2 Lanthanum oxide/metal gate interface

The interfacial layer at the high-k/metal gate interface may also cause the EOT degradation. The metal/high-k interface layer can be either an insulating or conducting layer. Yet W/La₂O₃ stack is a good option in the sense of smaller EOT. The TEM picture shown in Fig. 3(b) also reveals the existence of transition layer at W/La₂O₃ interface. XPS study on the W bonding states in this region indicates the major bonding states are oxidized tungsten phases (WO_x) (see Fig.5). As WO_x are in d² configuration and are conductive, it can be considered as part of W electrode and should not cause EOT degradation [1]. However, when the sample was subjected to thermal annealing at 600 °C, W-O-La bonding was found (see Fig.6) which may cause the EOT degradation and needs to be taken care in half nanometer EOT requirement.

This work is supported by the National Natural Science Foundation of China under the grant No. 61376111.

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EOT (nm) (SiO ₂ Thickness)	1.0	0.7	0.5
La ₂ O ₃ Physical Thickness (nm)	6.9	4.8	3.5

Parameter	SiO ₂	La ₂ O ₃	HfO ₂
κ	3.9	27	24
ΔE_C (eV)	3.5	2.30	1.5
ΔE_V (eV)	4.4	2.6	3.4
m_e^*	0.4	0.26	0.68
m_h^*	0.33	0.5	0.29
t_{DT} (nm)	3.0	4.6	3.5

$$EOT = \frac{\kappa_{ox}}{\kappa_{high-k}} t_{high-k}$$

$$t_{DT,high-k} = t_{DT,ox} \sqrt{\frac{m_{e,ox}^* \Phi_{B,ox}}{m_{e,high-k}^* \Phi_{B,high-k}}}$$

Fig.1: Scaling high-k to subnanometer EOT will push the gate dielectric film to direct tunneling limit again as high-k metal oxide has much smaller band offsets with silicon.

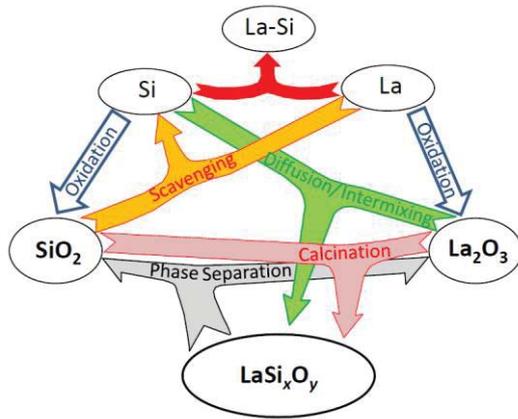


Fig.2: Possible chemical reactions amongst Si, La, SiO₂, La₂O₃, and LaSi_xO_y. Direct reaction between La₂O₃ and Si, interface oxidation, and SiO₂/La₂O₃ calcination can lead to the formation of a complex oxide layer with a smaller k value. It becomes the lower bound for minimum EOT to be achieved. Adopted from [1].

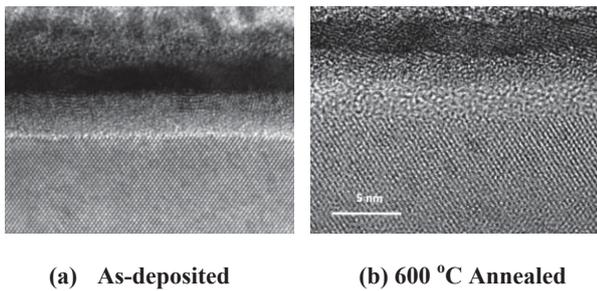


Fig.3: A thick silicate layer at the La₂O₃/Si interface make the resulting film to have a much large EOT. TEM picture showing the layered structure of cross-section view of the W/La₂O₃/Si stack: (a) as-deposited sample with sharp interfaces; (b) annealed sample with a thick silicate layer at the La₂O₃/Si interface.

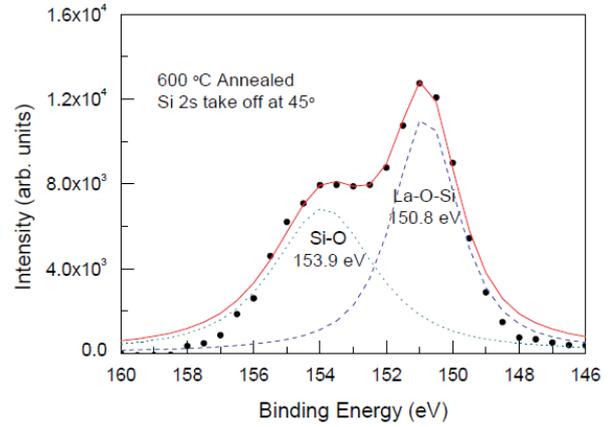


Fig.4: Angle-resolved Si 2s XPS taken at La₂O₃/Si interface showing significant amount of silicate bonding.

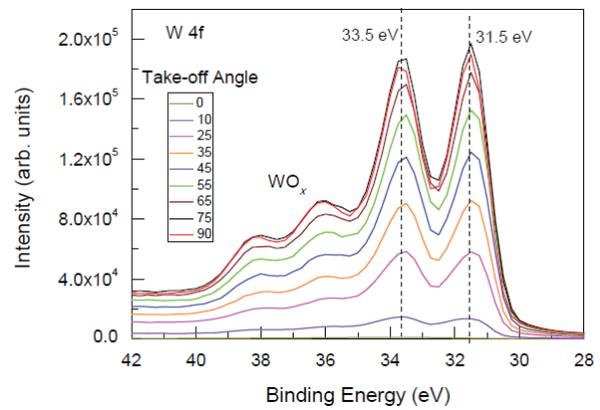


Fig.5: Typical W 4f XPS spectra at different depths showing strong WO_x peaks at the W/La₂O₃ interface. The sample was thermally annealed at 600 °C for 30 min.

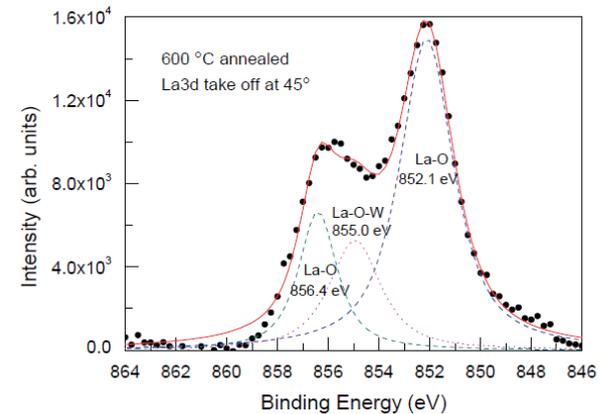


Fig.6: Gaussian decomposition of the La 3d XPS near the W/La₂O₃ interface reveals the La-O-W bonding. The sample was annealed at 600 °C for 30 min.

Low-frequency Noise Assessment in n- and p-channel Sub-10nm Triple-gate FinFETs

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In this work, static characteristics and low-frequency noise have been investigated on silicon triple-gate FinFETs. The principal static parameters have been extracted. Low-frequency noise studies showed that the origin of the $1/f$ noise in both n-channel and p-channel transistors seems to be due to carrier number fluctuations in moderate inversion.

1. Introduction

Triple-gate FinFETs are known for their good electrostatic performances and their compatibility with CMOS processes as a continuation of Moore's law [1].

The tested devices have been processed at imec (Belgium) for sub-10 nm technological nodes, in the framework of a comparative study between triple-gate FinFETs and gate-all-around (GAA) nanowire (NW) FETs [2]. The gate stack consists in a high- κ dielectric (HfO_2) on top of a SiO_2 interfacial layer, leading to an equivalent oxide thickness $EOT = 1.9\text{ nm}$. Each transistor has 5 fingers of $22 - 23\text{ nm}$ height; the finger width varies from 5 nm to 40 nm , which gives a total gate width going from $W_m = 245\text{ nm}$ to 420 nm . The gate length varies from $L_m = 45\text{ nm}$ to $10\text{ }\mu\text{m}$.

2. Results and discussion

The transistors have been studied in linear operation ($V_{DS} = 20\text{ mV}$) at room temperature. Good behavior of the transfer DC characteristics $I_D(V_{GS})$ and $g_m(V_{GS})$ is observed for both n- and p-channels, as shown on Fig.1.

Static parameters extraction has been further processed using the Y function method ($Y = I_D / \sqrt{g_m}$ [3]), which gives access to the threshold voltage V_t and the transconductance parameter $G_M = \mu_0 C_{ox} W/L$. Then the low-field mobility μ_0 and the access resistances R_{access} can also be extracted. The values of the access resistances have been confirmed using the linear variations of the total resistance for various gate overdrive voltage V_{GT} against the gate mask length L_m [4]. The value of the access resistance is determined at the common intersection of all lines, as shown on Fig.2.

A synthesis of the estimated static parameters is showed in Table 1. It can be observed that the threshold voltage V_t is higher (in absolute value) for n-channel transistors than for p-channel transistors. The charge sharing effect is more pronounced for p-channel devices, in particular for smaller finger widths. Higher values of the low-field mobility μ_0 can be observed for thinner fingers in both n- and p-channel transistors; this could be related to the effective values of the gate width. The access resistances are higher for p-channel FinFETs compared to the n-channel ones. The increase of the access resistance with the finger width decrease from 30 nm to 20 nm , observed for p-FinFETs, could be related to the effective values of the gate width.

Low-frequency noise measurements can be used as a diagnostic tool that leads to the identification of traps in the Si film and the gate oxide, thus giving information on the quality of the transistors fabrication. The low-frequency noise measurements have been performed from 1 Hz to 100 kHz at $T = 300\text{ K}$. An example of gate voltage noise power spectral densities (PSDs) S_{V_G} of an n-FinFET for different gate voltages V_{GS} can be observed in Fig.3.

All the PSDs can be modelled using a combination of three noise sources: white noise (of level K_w), $1/f$ noise (of level K_f) and generation-recombination noise, following the equation of the inset of Fig.4. The gate voltage noise PSDs show that n-channel transistors are more subject to generation-recombination contributions on the total noise compared to the p-channel ones.

The evolution of the $1/f$ noise level K_f with respect to the gate overdrive voltage V_{GT} leads to the identification of the $1/f$ noise origin. Fig.5 shows that n-FinFETs follow the carrier number fluctuations correlated to mobility fluctuations ($\Delta N + \Delta\mu$), while p-FinFETs trend to follow the number fluctuations model (ΔN) in moderate inversion [4]. For p-channel transistors in strong inversion, the total $1/f$ noise seems to originate from the access resistances noise contribution [5]. The extraction of the flat-band voltage spectral densities $S_{V_{fb}}$ values leads to an estimation of the oxide traps densities N_T , from $6.5 \cdot 10^{18}$ to $12 \cdot 10^{18}\text{ eV}^{-1} \cdot \text{cm}^{-3}$ for n-channel and from $0.8 \cdot 10^{18}$ to $4.6 \cdot 10^{18}\text{ eV}^{-1} \cdot \text{cm}^{-3}$ for p-channel, as shown in Table 2.

Finally, an example of the evolution of the Lorentzians characteristic frequency with respect to the gate overdrive voltage V_{GT} is shown on Fig.6. For the n-FinFET in this figure, it can be observed that the characteristic frequency of some Lorentzians is constant with the applied gate voltage (may be related to traps in the Si film), while the characteristic frequency of the other Lorentzians increases with V_{GT} (may be related to traps located in the gate oxide) [6]. This will be confirmed by performing a noise spectroscopic analysis.

3. Conclusion

The static parameters extracted in this work corroborates with other studies carried out at imec on these devices [2].

Low-frequency noise studies show that the $1/f$ noise in these FinFETs originates from the carrier number fluctuations. Oxide traps densities, around $10^{18}\text{ eV}^{-1} \cdot \text{cm}^{-3}$, show a good quality of the oxidation process. Further noise studies (e.g. noise spectroscopy) will give more detailed information about traps in the silicon film and the gate oxide.

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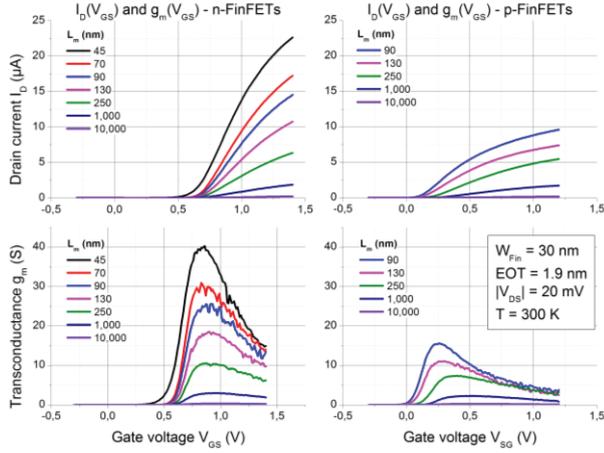


Fig.1: Typical $I_D(V_{GS})$ and $g_m(V_{GS})$ characteristics of *n*- and *p*-FinFET for various gate lengths.

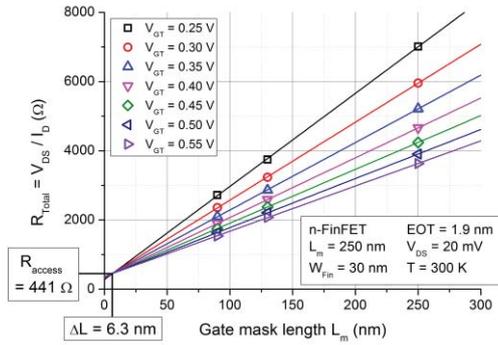


Fig.2: Example of DC parameters extraction, giving the value of the access resistance R_{access} .

	W_{Fin} / W_m	L_m	V_t	μ_0	R_{access}
	nm / nm	nm	mV	$cm^2 / V \cdot s$	Ω
n-FinFETs	20 / 320	70	732	338	375
	20 / 320	250	793		
	20 / 320	1000	752		
	30 / 370	70	727	256	441
	30 / 370	250	726		
	30 / 370	1000	740		
p-FinFETs	20 / 320	70	-69	190	1210
	20 / 320	250	-131		
	20 / 320	1000	-235		
	30 / 370	70	-144	167	594
	30 / 370	250	-232		
	30 / 370	1000	-295		

Table 1: Synthesis of DC parameters of several *n*-FinFETs and *p*-FinFETs.

	W_{Fin} / W_m	L_m	S_{fb}	N_T	
	nm / nm	nm	V^2 / Hz	$eV^{-1} \cdot cm^{-3}$	
n-Fin	20 / 320	70	$6 \cdot 10^{-9}$	$6.5 \cdot 10^{18}$	$S_{V_{fb}} = \frac{q^2 k T \lambda N_T}{f \gamma W L C_{ox}}$
	20 / 320	250	$8 \cdot 10^{-9}$	$10 \cdot 10^{18}$	
	30 / 370	70	$3 \cdot 10^{-9}$	$12 \cdot 10^{18}$	
	30 / 370	250	$2 \cdot 10^{-9}$	$8.9 \cdot 10^{18}$	
p-Fin	20 / 320	70	$2.2 \cdot 10^{-9}$	$2.4 \cdot 10^{18}$	
	20 / 320	250	$0.6 \cdot 10^{-9}$	$0.75 \cdot 10^{18}$	
	30 / 370	70	$1.2 \cdot 10^{-9}$	$4.6 \cdot 10^{18}$	

Table 2: Synthesis of flat-band voltage spectral densities $S_{V_{fb}}$ and oxide trap densities N_T of several *n*- and *p*-FinFETs.

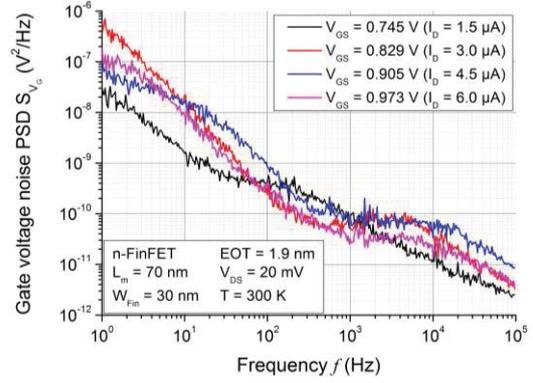


Fig.3: Gate voltage noise PSDs at different gate voltages V_{GS} (corresponding drain currents I_D are shown) of an *n*-FinFET.

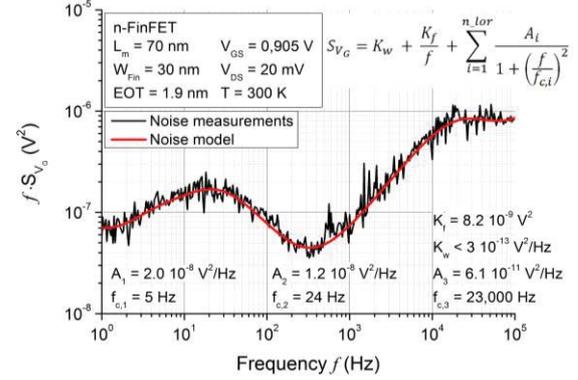


Fig.4: Example of low-frequency noise normalized by the frequency, leading to a low-frequency noise model.

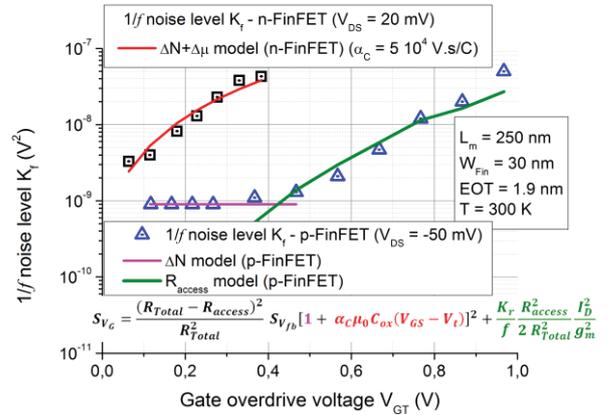


Fig.5: Evolution of the $1/f$ noise level K_f with respect to V_{GT} , for a *n*- and a *p*-FinFET with the same gate dimensions.

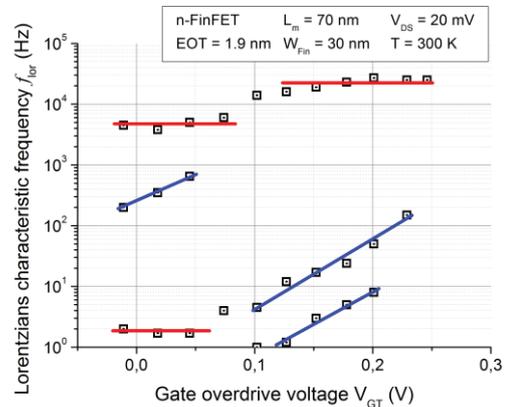


Fig.6: Evolution of the Lorentzians characteristic frequency with respect to the gate overdrive voltage V_{GT} .

Electrical Characterization of Random Telegraph Noise in Back-Biased Ultrathin Silicon-On-Insulator MOSFETs

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1. Introduction

Random Telegraph Noise (RTN) is remaining as a critical constrain when the characteristic dimensions of the semiconductor devices are shrunk to the decanometer range. Paired with the decrease of the signal levels, the introduction of Ultrathin Silicon-On-Insulator substrates also entails the appearance of additional effects related with the electrostatic coupling between the top-channel and the Si-film/BOX interfaces. Substrate bias is one of the more relevant applications of interface coupling (great importance for mobility boosting, V_T tuning...), but its role on the RTN characteristics has not been fully studied yet [1]. A systematic measuring protocol has been introduced based on a modified Weighted Time Lag Plot (WTLP) approach, combined with the Spectral Scanning by Gate Bias (SSGB) to select single traps and to identify the best operation region to characterize the RTN signature under substrate bias conditions.

2. Characterization Method

The characterization setup is based on an Agilent B1517A high resolution Source-Measurement-Unit (SMU) monitoring repeatedly the drain current during periods of 400s at a 2ms sampling-rate (the schematic is shown in Figure 1). The $1/f$ noise is characterized by using a low noise current amplifier connected to a software-based spectrum analyzer through a high resolution A/D converter.

High- k metal-gate SOI n-MOSFETs, fabricated at CEA-LETI in a 22nm process, were selected for the experiments [2]. The devices feature an ultrathin body of $t_{Si}=7\text{nm}$, Buried-Oxide (BOX) thickness of $t_{BOX}=145\text{nm}$, gate length of $L=100\text{nm}$ and width of $W=80\text{nm}$. The hafnium-based gate oxide has an equivalent oxide thickness (EOT) of $t_{EOT}=1.3\text{nm}$.

3. Experiments and Discussion

Identifying the RTN signals corresponding to single traps is one of the most challenging task during its electrical characterization. Examples of drain current, affected by RTN, measured as a function of time are shown in Figure 2 for different devices. When two current levels are clearly detected (revealing the existence of a single active trap, Figure 2.a), the time at the high- and low-current states, in average, corresponds to the capture (τ_c) and emission (τ_e) time respectively. However the selection of single traps is not straight forward in cases as the one shown in Figure 2.b. The determination of the traps of interest can be carried out unambiguously by a modified version of the Time Lag Plot method (TLP) partially based on the approach described in [3]. The sample-weighted approach of the conventional Time Lag Plot method allows to identify

the RTN levels clearly as populated regions in the diagonal of the TLP space, while populated regions outside the diagonal are related to the transitions between states. In Figure 3, we show results of the application of the method. Two lobes indicate the presence of a single trap (Figure 3.a) whereas the results in Figure 3.b) reveal the existence of three predominant current levels (two traps).

Identifying single trap RTN also requires the proper selection of the gate bias range where the characteristic times of the trap (τ_c , τ_e) are similar enough to each other so the transition events between states can be observed. This can be facilitated by obtaining the $1/f$ curve for a given bias (preferentially close to the threshold voltage) (Figure 4. Inset). The corner frequency is determined by the sum of the inverse of the characteristic times ($f_c=1/\tau_c+1/\tau_e$) [4]. Once the corner frequency is located, the spectral density of the current noise, S_i , is measured while V_G is swept leading to a S_i-V_G curve as shown in Figure 4 (Spectral Scanning by Gate Bias, SSGB). The bell shaped characteristic identifies the bias range where the RTN will be easily observable ($V_G \in [0.42\text{V}, 0.56\text{V}]$ for this particular case).

Figure 5 shows typical τ_c/τ_e ratios used to extract the physical parameters of the traps [5] for two different samples when a substrate bias is applied; the front gate overdrive voltage range is selected with the SSGB procedure previously described. As observed, although the curves are presented as a function of the overdrive voltage (note that V_T will be modified by V_{SUB} when the back interface is in depletion), the τ_c/τ_e ratio depends on the particular value of V_{SUB} (despite that the inversion charge is the same in all cases). Note also that this dependence on V_{SUB} , for a given inversion charge, is different for the particular trap considered (Figure 5.a) vs. 5.b)). Figure 6 shows the values of τ_c and τ_e as a function of the overdrive voltage for the previous devices. From the analysis of this plot we can appreciate that for a given overdrive voltage, the capture time (τ_c) decreases whereas the emission time (τ_e) increases as V_{SUB} increases. From Figure 6 one may also notice that this behavior is observed both for attractive (linear dependences of τ_c and τ_e with the gate bias, Figure 6.a) or neutral traps (linear dependence of τ_c and constant value τ_e with the gate bias Figure 6.b) [6]. This effect is contrary from the one we may expect considering *classical* RTN models relying on the inversion charge and the possible intensification of the role of the electric field in the Si-film while increasing the substrate bias [7]. In contrast, these results are compatible with the fact that the trap is escaping to the metal gate contact [8].

4. Conclusions

We have introduced an exhaustive method to identify experimentally, single-trap Random Telegraph Noise by combining the modified Weighted Time Lag Plot method with the $1/f$ Spectral Scanning by Gate Bias technique. The characterization procedure has been implemented in ultrathin SOI MOSFETs when a substrate bias is applied. The results show a non-intuitive tendency leading to an increase of the emission time (decrease of capture time) when the electric field in the film is relaxed for a given inversion charge. However this behavior could be explained by the trap escaping to the gate metal contact.

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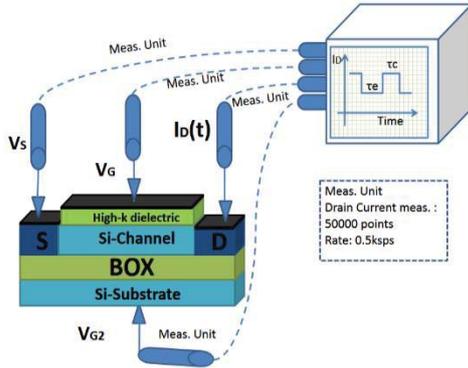


Fig.1: Schematic of the experimental setup developed for the RTN measurements. Each transistor terminal is monitored by an Agilent B1517A SMU at a rate of 500 samples per second.

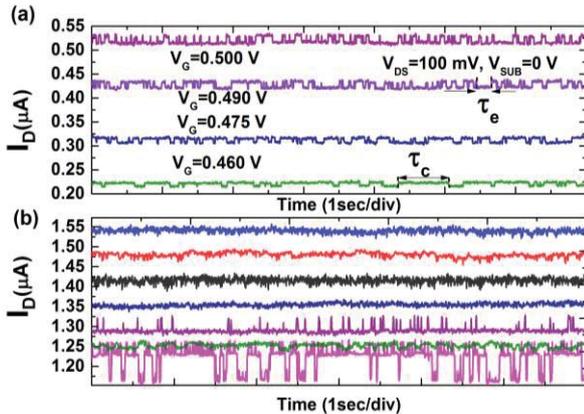


Fig.2: Drain current signal presenting RTN as a function of time for different gate voltages. a) Device with clear single active trap. b) Devices with possible multi-trap situation.

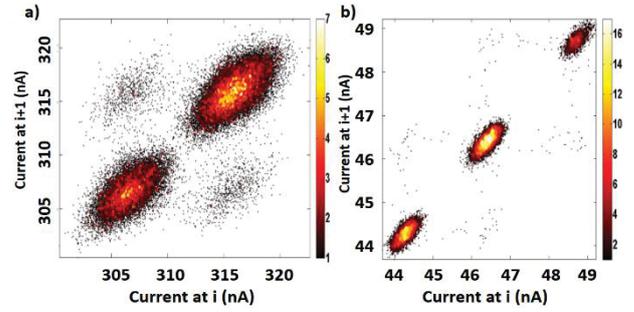


Fig.3: Weighted TLP of the drain current signal: a) transistor of Fig. 2a) with $V_G=0.475$ V where two lobes (states) result of the single active trap are clearly shown. b) Three lobes identifying the characteristic signature of three traps.

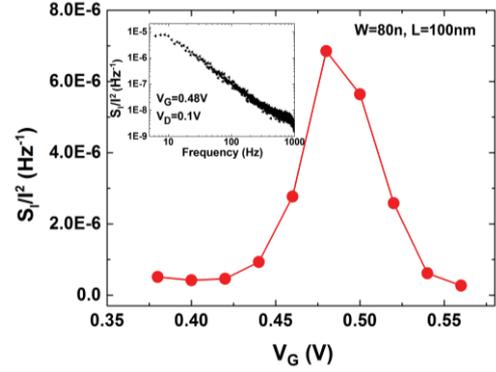


Fig.4: Normalized current noise power S_i dependence with the V_G (SSGB) for the transistor shown in Figure 2.a). Inset: S_i vs. frequency for the same device at a given bias point.

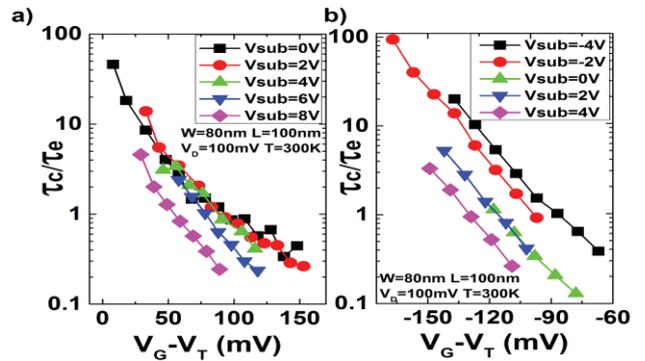


Fig.5: τ_c/τ_e ratios respect to the gate overdrive bias for different negative and positive substrate biases. Results from two different devices a) and b).

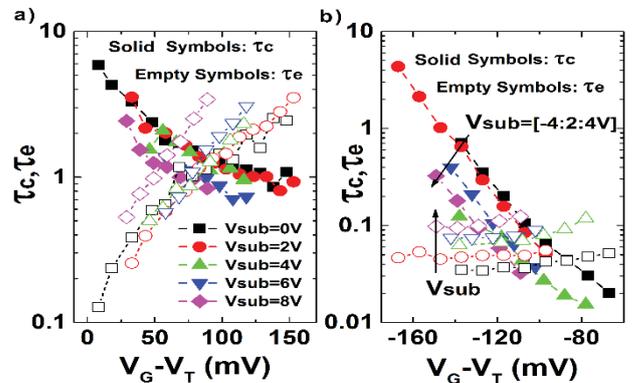


Fig.6 τ_c and τ_e ratios respect to the gate overdrive for different substrates biases in the same devices than in Fig. 5.

1/f -Noise Characteristics of Omega-shaped AlGaIn/GaN Nanowire FETs

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1. Abstract

The low frequency noise (LFN) characteristics of the omega-shaped AlGaIn/GaN nanowire FETs with different nanowire widths (W) have been investigated. It was found that the noise characteristics of the device with narrow W are dominated by the mobility fluctuation due to the accumulation of electrons in the volume of the nanowire which constricts the electron trapping in GaN layer. Whereas, width increases the LFN characteristics tended to be dominated by the carrier number fluctuation because the fin is too wide for volume accumulation and are subjected to the bulk trapping.

2. Introduction

AlGaIn/GaN fin-shaped field-effect transistors (FinFETs) benefit from enhanced gate control of the channel, which results in remarkable on-state and off-state performances [1]: low off-state leakage, high on-state current, low subthreshold swing (SS), and high linearity operation. We have recently demonstrated omega-shaped AlGaIn/GaN FinFETs exhibiting superior off-state characteristics [2] which features 2DEG conduction at the AlGaIn/GaN interface and sidewall MOS conduction along the fin sidewalls. In this work, omega-shaped AlGaIn/GaN FinFETs with different fin widths (W) have been fabricated and their 1/f noise characteristics have been analyzed. We show and explain the transition from carrier mobility fluctuations to carrier number fluctuations LFN as the fin width increases.

3. Results and Discussion

The growth of AlGaIn/GaN heterostructure and the fabrication of omega-shaped FinFETs was described elsewhere [2]. The schematic configuration and cross-sectional TEM image of AlGaIn/GaN omega-shaped FinFETs are shown in Fig. 1(a) and (b), respectively. Typical transfer I_d - V_{gs} characteristics are shown in Fig. 2. All devices exhibit extremely low off-state leakage current (10^{-11} mA), low subthreshold swing (SS \approx 60 mV/decade), and high I_{ON}/I_{OFF} ratio ($\sim 10^{10}$). These excellent performance results from full depletion operation and, more importantly, the active channel was

almost completely separated from the underlying thick GaN buffer layer [2].

The study of low-frequency characteristics based on carrier number fluctuation (CNF) and carrier mobility fluctuation (CMF) models in AlGaIn/GaN FinFETs devices has been reported in reference [3]. The normalized drain-current noise spectral density (S_{I_d}/I_d^2) as a function of nanowire width (W), measured at $V_{ds} = 0.1$ V (ohmic region) at $f = 10$ Hz is shown in Fig. 3. It was found that the noise magnitude (S_{I_d}/I_d^2) increases as the W increases, where the number of traps are higher [4]. In addition, more informative results were obtained by plotting (S_{I_d}/I_d^2) versus I_d as shown in Figure 4. It is noticed that the $(g_m/I_d)^2$ is much higher than S_{I_d}/I_d^2 (which means $S_{V_{fb}} < 1$) and essentially varies proportionally with $1/I_d$ for the device with narrow W . These facts act against the CNF model and it follows that the dominant source of noise is unequivocally the carrier mobility fluctuation [5]. In narrow device, the electron distribution spreads, from the sidewalls into the central region of the fin, similar to the volume inversion concept observed in Si-based devices [6]. This volume accumulation of electrons in the body can fill the traps, thus 2DEG electrons are less subject to bulk-trapping and the screening effect by volume electrons is responsible for the mobility fluctuation. On the other hand, the two curves, S_{I_d}/I_d^2 and $(g_m/I_d)^2$, are well matched ($S_{V_{fb}} \approx 1$) for $W = 200$ nm. The LFN varies as $1/I_d^2$, and the noise saturation in weak accumulation is clearly visible. This explicitly points out that the noise is due to carrier number fluctuation. Here, the fin is too wide for volume accumulation to take place, thus the 2DEG electrons have higher probability of being captured in bulk traps that are typically located in the GaN layer. From $W = 200$ nm, we note that $S_{V_{fb}} \approx 1$ and deduce the trap density ($N_t = 2.9 \times 10^{20} \text{ cm}^{-3} \text{ eV}^{-1}$).

4. Conclusion

The low-frequency noise (LFN) characteristics of AlGaIn/GaN FinFETs with omega-gate FinFETs were investigated. It was observed that as the fin width is shrunk, volume accumulation in the body masks the GaN traps and the noise essentially originates from CMF, whereas, the fin is too wide for volume accumulation in wider devices.

Acknowledgement

This work was supported by the BK21 Plus funded by the Ministry of Education (21A20131600011), the IT R&D program of MOTIE/KEIT (10048931), and the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No.2011-0016222, 2013R1A6A3A04057719).

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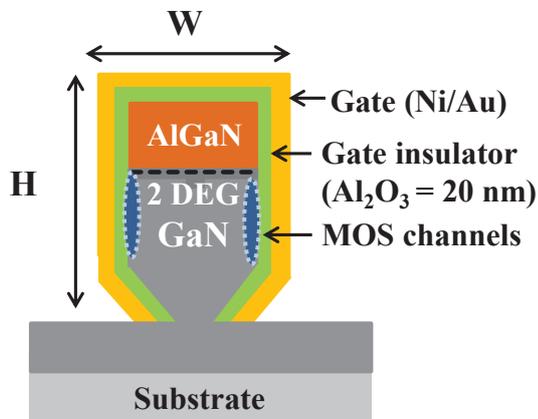


Fig.1 (a) : Schematic illustration of the omega-shaped FinFETs.

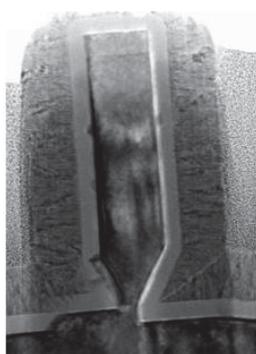


Fig.1 (b) : Cross-sectional TEM image of the omega-shaped FinFETs.

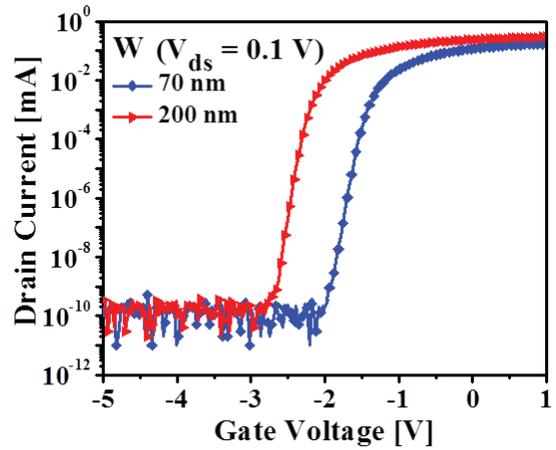


Fig.2: $I_d - V_{gs}$ characteristics according to width of the Fin.

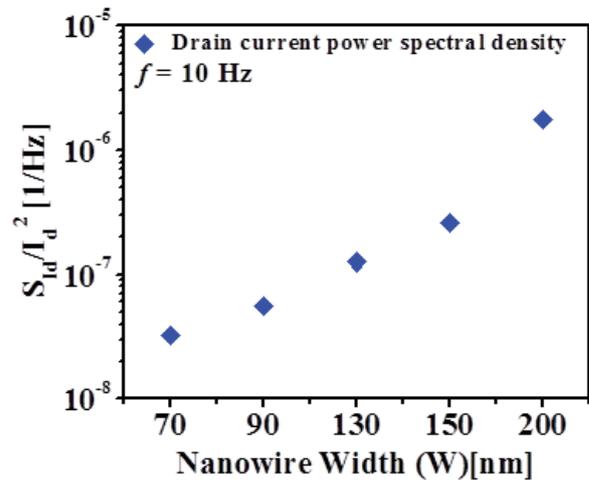


Fig.3: Normalized drain current spectral density (S_{Id}/I_d^2) versus frequency in the fabricated AlGaN/GaN omega-FET with different in widths (W) at $V_{ds} = 0.1$ V, $V_{gs} - V_{th} = 0.4$ V.

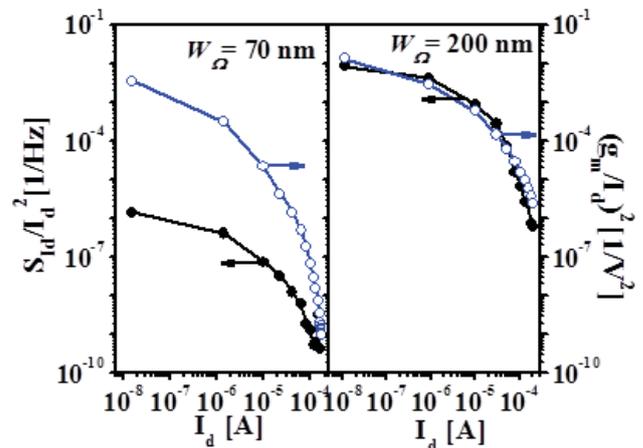


Fig.4: Averaged noise spectral density (S_{Id}/I_d^2) (black circle) and $(g_m/I_d)^2$ (blue circle) versus I_d at $V_{ds} = 0.1$ V and $f = 10$ Hz

Simulation of Plasma Resonances in MOSFETs for THz-Signal Detection

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1. Introduction

Generation and detection of electromagnetic radiation in the THz range is required for many applications. Due to the high frequencies of more than 300GHz (mm waves) the performance of semiconductor devices is very poor in this frequency range. By exploitation of plasma waves it might be possible to boost their performance [1]. In this work we present a new approach for the simulation of plasma waves in semiconductor devices beyond the usual transmission line approaches (e.g. [2]). Since in Ref. [3] quarter-micron NMOSFETs are used for detection of THz signals, we investigate the impact of plasma effects in such a device.

2. Simulation Approach

We solve in 2D the drift-diffusion (DD) model for electrons and holes together with the Poisson equation for the quasi-static potential [4]. In order to capture plasma waves, we include in the constitutive equation for the electron current density its time derivative:

$$\tau_n \frac{\partial \vec{j}_n}{\partial t} + \vec{j}_n = -q\mu_n(n\nabla\varphi - V_T\nabla n)$$

τ_n is the electron relaxation time with $\mu_n = q\tau_n/m_n$, where m_n is the electron conductivity mass. The hole case is similar. This derivative is usually neglected in TCAD simulators to avoid numerical stability problems and issues with efficiency. If the time derivative is included, the current density cannot be eliminated from the DD model and in addition to the potential and electron and hole densities we have to solve for the vector-valued electron and hole current densities. The right-hand side of the above equation is stabilized with the Scharfetter-Gummel scheme [4]. We have implemented three methods for time integration: the backward Euler (BE) scheme, the backward differentiation formula of second order (BDF2) and a modified BDF2 scheme (MBDF2) based on trigonometric functions instead of polynomials [5]. The latter scheme is only used in the case of a periodic steady-state simulation.

3. Results

In Fig. 1 the current of an abruptly turned-on pn junction is shown, where the simulations are performed with and without the time derivative of the current density. The plasma oscillations occur only in the case with the derivative and are similar to the full-band Monte Carlo result.

In Fig. 2 the basic circuit with an NMOSFET is shown, where the device is used as a passive mixer to rectify the AC signal applied to the source. The output signal is the DC drain current and the quantity of interest is the responsivity, which is given by the ratio

of the DC drain current and the AC input power at the source: $R_I = I_D^{DC}/P_S^{AC}$. In Fig. 3 a typical drain current is shown for a sinusoidal AC voltage at the source calculated with the BDF2 scheme. A few periods are required to reach the periodic steady-state. In all following simulations a sufficient number of periods is used (depending on the frequency 50 to 200 periods).

In Fig. 4 the responsivity of the MOSFET is shown for the different time integration schemes as a function of the time steps per period. The BE scheme shows the usual over-damping and requires a very large number of time steps. The standard BDF2 is more efficient than BE, and the modified one (MBDF2) requires only 8 steps for a negligible error. A smaller number of steps is not possible due to numerical instabilities.

The responsivity as a function of the frequency is shown in Fig. 5 for different electron mobilities. For low mobilities no impact of the plasma waves is seen. On the other hand, for the highest mobility a strong plasma effect occurs, which vanishes, if the time derivative of the current density is neglected. These results show, that plasma effects play no role in silicon devices with mobilities around $300\text{cm}^2/\text{Vs}$. In III-V or graphene devices the mobility might be sufficiently high for plasma effects and the responsivity might be higher than in silicon at high frequencies. At low frequencies the responsivity does not depend on the mobility.

The dependence on the gate bias and thus on the electron density is shown in Fig. 6 for a frequency of 1THz . The lower the gate bias, the lower is the resonance frequency. This leads to the minima in the responsivity for the highest mobility as a function of the gate bias. For low mobilities the peak responsivity is found near the threshold voltage, whereas at high mobilities it moves to higher voltages.

3. Conclusions

We have demonstrated that inclusion of the time derivatives of the current densities in constitutive equations of the DD model allows simulating plasma effects in semiconductor devices. Under periodic steady-state conditions the backward differentiation formula of the second order based on trigonometric functions (MBDF2) yields the best performance.

Due to the strong over-damping of the plasma waves by the low mobility (high scattering) plasma effects play no role in silicon devices. On the other hand, in high mobility materials plasma resonances might occur and the responsivity of such devices is largely enhanced at high frequencies.

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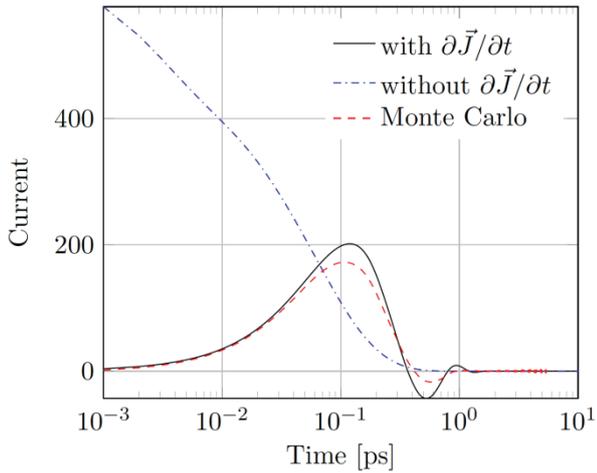


Fig.1: Current of a pn junction with an abrupt change in bias from 0 to 0.7V at zero time with and without $\partial\vec{J}/\partial t$, and corresponding Monte Carlo results.

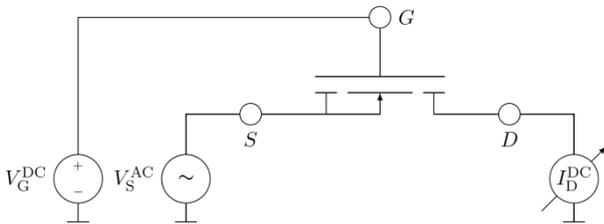


Fig.2: NMOSFET as a passive mixer.

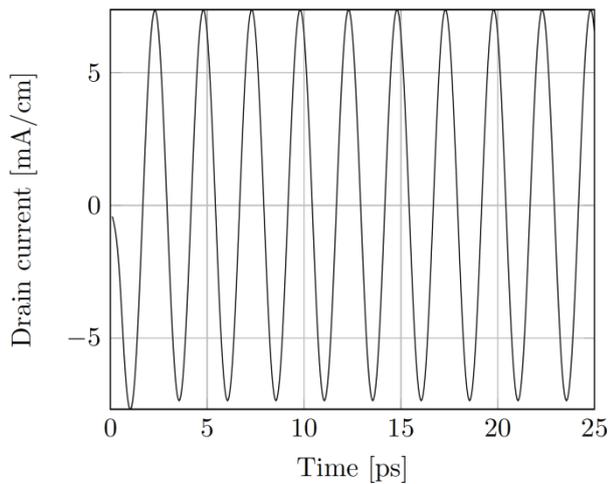


Fig.3: Drain current at $V_S^{AC} = 1\text{mV}$, $f=400\text{GHz}$, $V_G^{DC} = 1\text{V}$ and $\mu_n = 300\text{cm}^2/\text{Vs}$ evaluated with the BDF2 scheme.

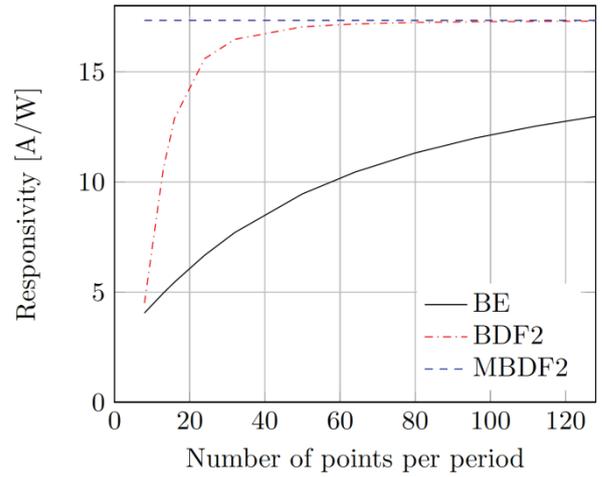


Fig.4: Responsivity at $V_S^{AC} = 1\text{mV}$, $f=1\text{THz}$, $V_G^{DC} = 1\text{V}$ and $\mu_n = 10000\text{cm}^2/\text{Vs}$.

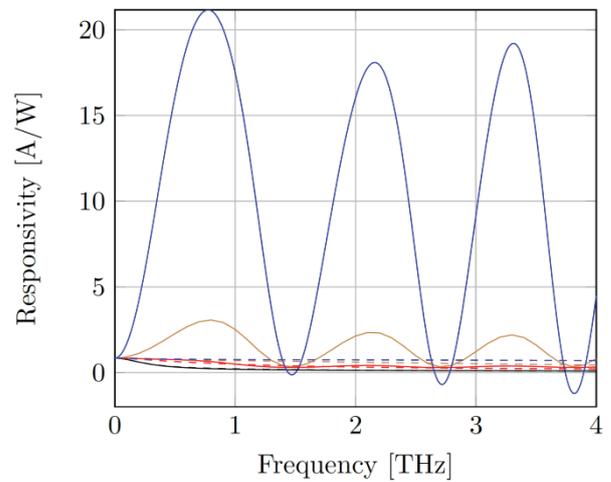


Fig.5: Responsivity at $V_S^{AC} = 1\text{mV}$, $V_G^{DC} = 1\text{V}$ with (solid lines) and without (dashed lines) $\partial\vec{J}/\partial t$. Black: 300, red: 1000, brown: 3000, blue: $10000\text{cm}^2/\text{Vs}$.

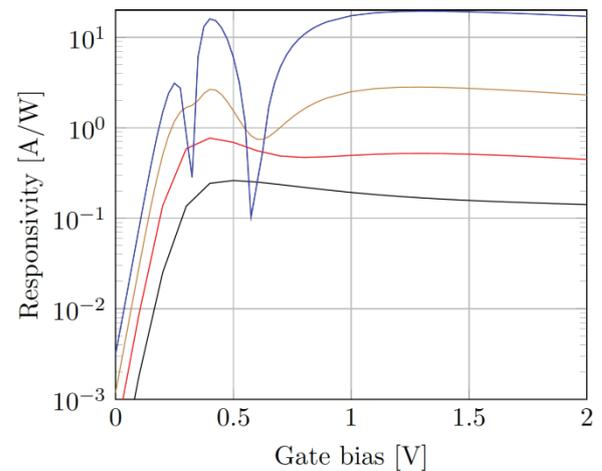


Fig.6: Responsivity at $V_S^{AC} = 1\text{mV}$ and $f = 1\text{THz}$. Black: 300, red: 1000, brown: 3000, blue: $10000\text{cm}^2/\text{Vs}$.

Scaling/LER Study of Si GAA Nanowire FET using 3D Finite Element Monte Carlo Simulations

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1. Introduction

Gate-All-Around (GAA) nanowire (NW) FETs are considered to be excellent candidates for future CMOS integration for sub-10 nm digital technology to continue transistor downscaling. The GAA NW FETs have superior electrostatics and immunity to short channel effects while still delivering a large on-current [1–3]. However, variability of transistor characteristics induced by material properties and by fabrication process can affect their performance in circuits. Line-edge roughness (LER) is one of such sources with a major impact on variability in NW/FinFETs [2, 4, 5].

In this work, we report on performance, scaling and variability induced by line-edge roughness (LER) [2, 4, 5] of GAA NW FETs. We use an in-house 3D Finite Element (FE) Monte Carlo (MC) toolbox which includes newly developed integrated calibration-free FE anisotropic Schrödinger equation based quantum corrections (SEQC). More details on the 3D FE MC toolbox are in Refs. [6–8].

2. 3D Monte Carlo Simulations

We start by comparing results from our 3D SEQC MC toolbox against experimental data of 22 nm gate length GAA Si NW [1] and <110> channel orientation. The NW has elliptical cross-section (Fig. 1) with a shorter/longer diameter of 11.3/14.22 nm; with an effective diameter (elliptical circumference/ π) of 12.8 nm), and EOT = 1.5 nm. The 3D FE quantum corrected (QC) drift-diffusion (DD) simulations were used to reverse engineer a doping profile in the sub-threshold region at $V_D=0.05$ V and $V_D=1.0$ V as shown in Fig. 2. Fig. 3 shows examples of this engineering process from a sub-threshold region which achieved excellent agreement with a max. doping of $5 \times 10^{19} \text{cm}^{-3}$, a work function of 4.492 eV, and a S/D size of 30.8 nm. We then simulate the I_D - V_G characteristics of the 22 nm gate GAA Si NW at low and high drain biases using the 3D SEQC MC toolbox without any free parameter achieving an excellent agreement seen in Fig. 4. Fig. 5 shows the potential profile in the device and Fig. 6 shows the average electron velocity along the channel at $V_D=1.0$ V and $V_G=0.8$ V. We then scale the Si GAA NW according to the ITRS specifications to a gate length of 10 nm and EOT of 0.8 nm. Fig. 7 compares the first wavefunctions of the three Δ valleys in the middle of the channel for the 22/10 nm gate length GAA NW at $V_D=1.0/0.7$ V and $V_G=0.8$ V (note that Δ_1 and Δ_2 have the same effective mass tensor in the <110> channel orientation, so they will have the same wavefunction). Fig. 8 shows I_D - V_G characteristics for the scaled NW FET at $V_D=0.05$ V and $V_D=0.7$ V predicted by the 3D FE SEQC MC. Table 1 compares device operating

characteristics with gate lengths of 22 nm and 10 nm predicting that the scaling to the 10 nm gate will ensure superior electrostatic integrity and only a small increase in on-current (5%).

3. Line-Edge Roughness (LER)

The LER variability study in NWs is essential for predicting device behaviour in digital circuits. The effect of uncorrelated LER is studied using Fourier synthesis with Gaussian autocorrelation [9] implemented as described in [10, 11]. We simulated the 22 nm gate length NW using the 3D quantum corrected FE DD with a LER correlation length (CL) of 20 nm and three root mean square values (RMS=0.6, 0.7 and 0.85 nm), chosen to represent a RMS observed in experiments [1, 2]. Table 2 compares $V_{T,lin}$, and $I_{OFF,lin}$ variability at $V_D = 0.05$ V due to the LER for the 22 nm GAA NW as a function of the RMS height. Fig. 9 shows the scatter plots of $V_{T,lin}$ versus $V_{T,sat}$ for the 22 nm Si GAA NW with CL=20 nm and RMS=0.6 nm. The threshold voltage at low and high drain biases are strongly correlated (CC=0.997). The larger the CC value, the less sensitive the variability is to a change in the drain bias. Fig. 10 shows $I_{off,sat}$ vs. $V_{T,sat}$ at $V_D=1.0$ V for the 22 nm GAA nanowire with CL=20 nm, RMS=0.6 nm. The log of the off-current exhibits the typical linear dependence on the decreasing $V_{T,sat}$ suggesting near-to-Gaussian behaviour.

4. Conclusion

We have compared results from our 3D SEQC FE MC simulation toolbox, which accurately describes the nanoscale geometry of multi-scale transistors using a completely parameter-free model of carrier transport, to the I-V characteristics of the 22 nm gate length GAA Si NW FET with exceptional agreement. We have scaled GAA NW FET to the 10 nm gate length and predicted that the scaled device will deliver on-current of 1196 $\mu\text{A}/\mu\text{m}$. Finally, we have found that the LER induced variability for the 22 nm GAA NW exhibits σV_T in order of 10 mV and $\sigma \text{Log}_{10}(I_{OFF})$ is 0.2–0.3 A.

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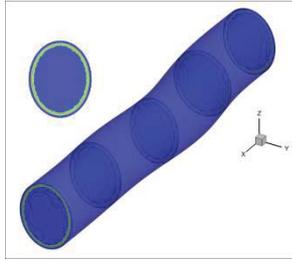


Fig. 1: Schematic of the 22 nm gate length n-channel Si GAA nanowire, showing LER and examples of 2D slices.

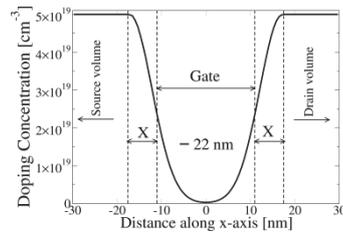


Fig. 2: Cross-section of Gaussian-like doping profile along the transport x -direction for the 22 nm gate length GAA NW FET.

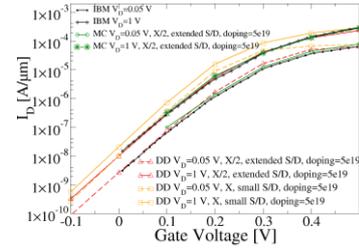


Fig. 3: Devising doping profile for the 22 nm GAA NW FET at $V_D=0.05/1.0$ V via DD sim. by size of the S/D region and the doping spread X (open red triangles and orange squares). Final MC sim. (green open circles and stars) compared to experimental data (black full circles and stars).

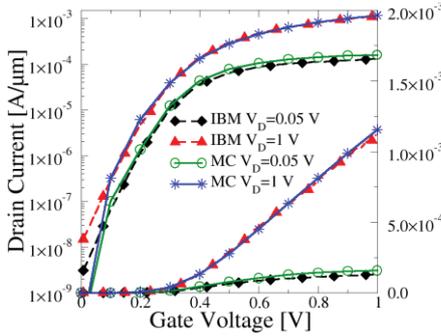


Fig. 4: I_D - V_G characteristics for the 22 nm GAA NW at $V_D=0.05/1.0$ V from the 3D FE MC with anisotropic Schrödinger quantum corrections with no free parameter (full lines) compared against experimental data (dashed lines) [1].

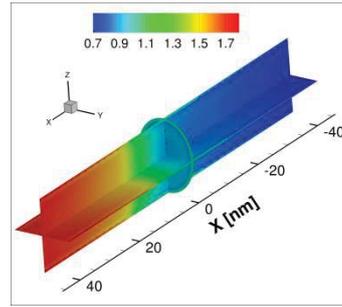


Fig. 5: Potential profile at $V_D=1.0$ V and $V_G=0.8$ V for the 22 nm gate length GAA nanowire, from drain (+ x) to source (- x).

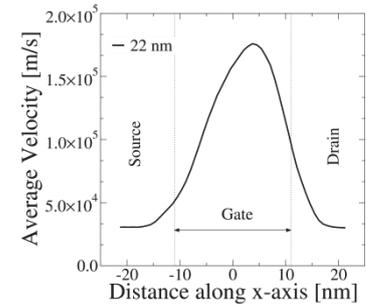


Fig. 6: Average electron velocity at $V_D=1.0$ V and $V_G=0.8$ V along the 22 nm GAA nanowire (3D MC). The zero is set in the middle of the channel.

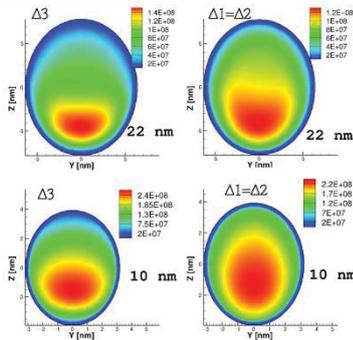


Fig. 7: The first wavefunctions of the three Δ valleys, in the middle of the $\langle 110 \rangle$ channel for the 22 nm (top, at $V_D=1.0$ V) and 10 nm (bottom, at $V_D=0.7$ V) Si GAA NWs at $V_G=0.8$ V.

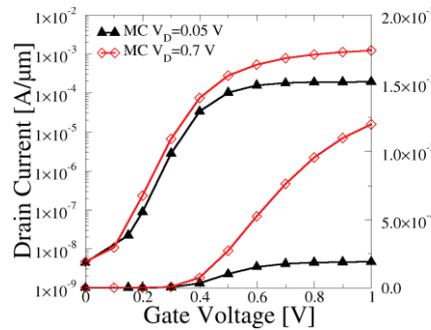


Fig. 8: I_D - V_G characteristics for the scaled 10 nm gate length GAA nanowire at $V_D=0.05$ V and $V_D=0.7$ V predicted by the 3D SEQC FE MC.

Gate length [nm]	22	10
V_T [V]	0.3	0.3
SS_{LOW} [mV/dec]	74	66
SS_{HIGH} [mV/dec]	77	67
DIBL [mV/V]	48	35
DIBL _{MC} [mV/V]	64	39
I_{MC} [$\mu A/\mu m$]	1150	1196

TABLE 1: V_T and SS for drain biases of 0.05 V (low) and 1.0/0.7 V (high) from the DD, DIBL from the DD and from the MC, and drive currents (I_{MC}) at $V_G=1.0$ V comparing the 22 nm and the 10 nm gate length GAA NWs.

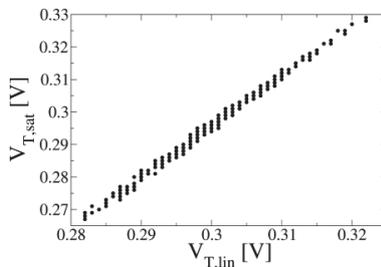


Fig. 9: Threshold voltages at low drain bias ($V_{T,lin}$) against at high drain bias ($V_{T,sat}$) for the 22 nm GAA nanowire with LER (CL=20 nm, RMS=0.6 nm).

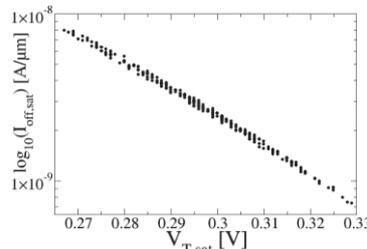


Fig. 10: $\log_{10}(I_{OFF,SAT})$ vs. $V_{T,sat}$ at $V_D=1.0$ V for the 22 nm GAA nanowire with LER (CL=20 nm, RMS=0.6 nm).

RMS [nm]	0.6	0.7	0.85
avg. V_T [mV]	300.54	302.13	302.47
σV_T [mV]	8.61	10.12	12.1
avg. $\log_{10}(I_{OFF})$ [A]	-10.02	-10.06	-10.07
$\sigma \log_{10}(I_{OFF})$ [A]	0.219	0.259	0.312

TABLE 2: Comparison of the $V_{T,lin}$ and $I_{OFF,lin}$ variability ($V_D = 0.05$ V) due to the LER for the 22 nm GAA nanowire as a function of the RMS height.

Simulation Analysis of the Electro-Thermal Performance of SOI FinFETs

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1. Introduction

FinFETs, with their superior electrostatic integrity, performance and variability, are replacing the traditional planar MOSFETs [1]. However, because of their 3D architecture, the FinFETs' thermal properties are significantly degraded. Self-heating effects will be exacerbated in SOI FinFETs (a schematic of an SOI FinFET is shown in Fig. 1), due to the low thermal conductivity of the buried oxide layer beneath the fin. To maximise the benefits of FinFET technology, an enhancement of TCAD tools is required, to allow accurate analysis and modelling of self-heating in FinFETs and its influence on device performance [2]. A progressive electro-thermal FinFET simulation study has been presented [3]. Recently, the thermal simulation module in the GSS 'atomistic' simulator GARAND [4] has been enhanced to capture accurately the fin geometry dependence of the thermal conductivity [5]. In this paper, GARAND is used to investigate the electro-thermal performance of SOI FinFETs under different external thermal resistances connected to the gate.

2. Simulation Methodology

Our electro-thermal simulation module, as used in this work, is based on the solution of the coupled Heat Flow, Poisson and Current Continuity Equations. A special thermal conductivity model is developed considering the effects of thermal confinement in FinFETs, where the thickness and width of the fin is less than 100 nm. The thermal conductivity in the fin can be significantly reduced compared to bulk Si, due to phonon-boundary scattering. The new approximate formula generalises a previous 1D paradigm [6] to 2D confined structures by assuming a similar integral dependency in the second direction [3]. The thermal environment, where heat is dissipated, is a large domain including transistors, the substrate, the interconnect layers, the die, the heat sink and packaging. The usual electrical simulation domain is typically restricted to the active region of the device in order to minimise simulation time. The inclusion of external thermal resistances is crucial for thermal simulations. In FinFETs the heat dissipation through the gate is more complicated because the shape and materials of the gate stack and surrounding region are much more complex. At thermally conducting interfaces, nonhomogeneous Neumann boundary conditions can be imposed.

3. SOI FinFET example

An SOI FinFET designed to meet the specifications for the 14/16nm CMOS technology generation is used in this study. Its channel length is 25 nm with spacers of 6nm on both sides of the gate, while the fin width and

height are 12nm and 30nm respectively. A high- κ metal gate stack is employed. Three external resistances are used to account for heat dissipation through the top of the gate, the front and the back of the gate. By employing GARAND with the coupled thermal simulation module, five different cases with various external thermal resistances connected to the gate of the SOI FinFET example are simulated, as summarised in Table I. The external thermal resistances are user-specified parameters for the electro-thermal simulation module. The values used here demonstrate the effect and importance of the choice of relevant thermal resistances.

Joule heat distribution at high drain and high gate biases resulting from the 3D coupled electro-thermal simulations for "Case 1" are illustrated in Fig. 2. Lattice temperature distributions at high drain and high gate biases for five cases are illustrated in Fig.3, as well as the temperature variation according to the gate voltage at high drain bias. The Id-Vg characteristics at high drain bias from the 3D electro-thermal simulations are illustrated in Fig.4.

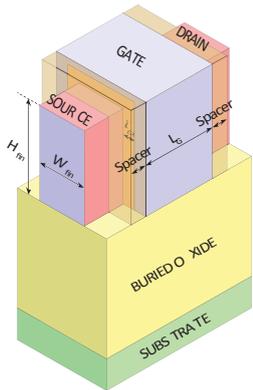
4. Conclusions

Using GARAND with enhanced 3D coupled electro-thermal simulation capabilities, the electro-thermal performance for an SOI FinFET example, aiming for the 14/16nm CMOS technology generation, has been simulated. The lattice temperature profiles under different external thermal resistances and the corresponding Id-Vg characteristics are investigated and analysed. The results show a significant hot spot generated near the drain because of the much lower thermal conductivity of the fin, as the peak lattice temperature exceeds 420 K for all five cases in this study, and strong temperature gradients are also generated in this region. The impact of external thermal resistances at different places connected to the gate is different, consequently affecting the electrical performance of the SOI FinFET.

The research leading to these results has received funding from the European Union Seventh Framework Programme (FP7/2007 – 2013) under grant agreement no. 318458 SUPERTHEME.

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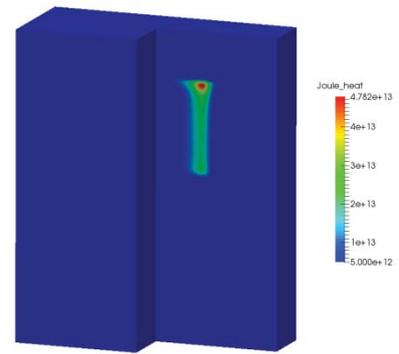
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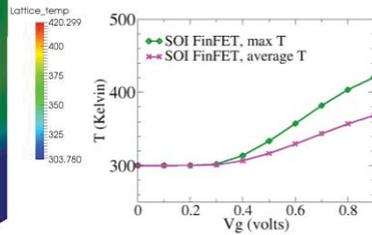
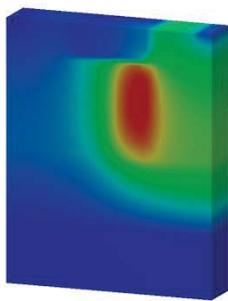
Schematics of SOI FinFET.

FIVE DIFFERENT CASES WITH VARIOUS EXTERNAL THERMAL RESISTANCES FOR 3D COUPLED ELECTRO-THERMAL SIMULATION

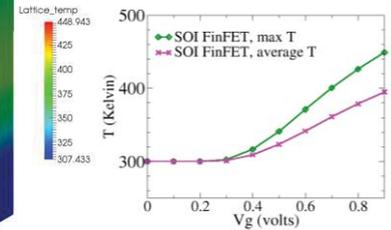
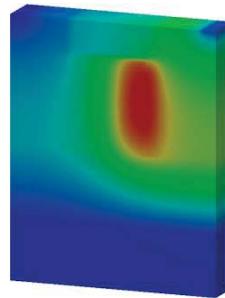
	External thermal resistance connected to		
	Top gate	Front gate	Back gate
Case 1	4800	32	32
Case 2	4800	320	320
Case 3	4800	3200	3200
Case 4	480	32	32
Case 5	480	320	320



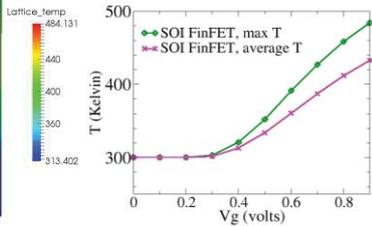
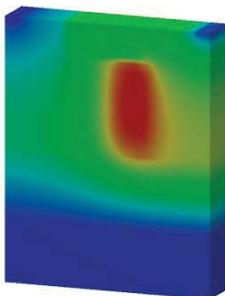
Joule heat distribution at high drain and high gate biases resulted from the 3D coupled electro-thermal simulations for "Case 1".



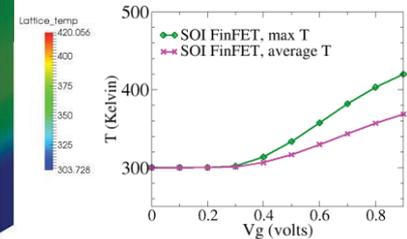
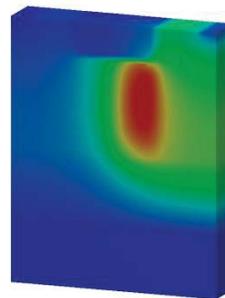
(a) Case 1



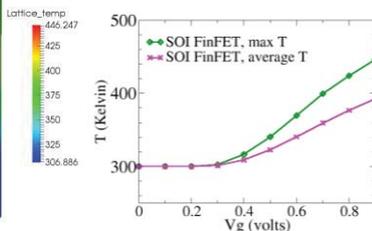
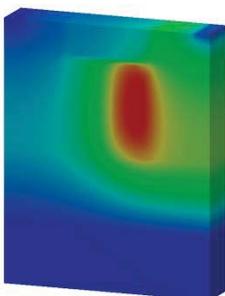
(b) Case 2



(c) Case 3

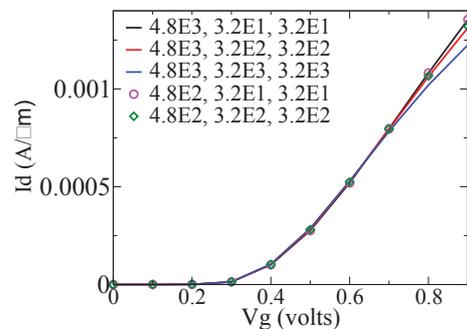


(d) Case 4



(e) Case 5

Lattice temperature distributions at high drain and high gate biases (left) and the temperature variation according to gate voltage at high drain (right), resulting from the 3D coupled electro-thermal simulations for five cases.



I_d - V_g characteristics at high drain bias from the 3D electro-thermal simulations, comparing five cases.

Space-Average Impurity-Limited Resistance and Self-Averaging in Quasi-1D Nanowires

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1. Introduction

Si nanowires have been receiving great attention in the past decades because of their possible application of future electronic and photonic devices as well as other novel applications like chemical sensors [1]. The device performance, however, greatly fluctuates, depending on the configuration of localized impurities in the channel region. So far, theoretical studies are limited with large-scale numerical simulations [2-3] and the physical mechanism behind such variability is still not clear. In particular, almost no study has been done on the interference effects among multiple impurities. In this report, we study those effects on the impurity-limited resistance in the quasi-1D nanowires based on the scattering theory and clarify the physical origin of the “self-averaging” emerged in the average resistances under the fully coherent circumstances.

2. Theoretical Methodology

We derive the exact theoretical expressions of the impurity-limited resistance due to localized impurities in the nanowire from the Landauer formula under the linear response regime. The nanowire has the spherical cross-section with radius 2 nm and the doping density of the substrate is set at $2 \times 10^{19} \text{ cm}^{-3}$. We assume that the scattering potential of ionized impurities is short-ranged and the channel potential is flat along the wire axis direction by applying a proper gate voltage. We would like to stress that the entire potential modulation in the channel is treated as a *single* scattering potential under the framework of scattering theory (Fig. 1). The exact transmission and reflection probabilities are derived from the Lipmann-Schwinger equation. The formulas are applied to the cases where two impurities are doped in the channel so that the resistance due to correlated impurities is calculated (Fig. 2). The resistance is then space-averaged under the uniform distribution of impurities inside the channel.

3. Results and Discussion

The impurity-limited resistance of 1000 different configurations of two impurities are calculated and the results are shown in Fig. 3 as a function of the impurity separation Δ . R_s 's are scattered over great ranges and this is due to both the variation of the scattering strength and phase interference of electron's wave propagation among impurities. In particular, large R_s 's at small Δ are attributed to the constructive phase interference [4]. R_s 's obtained from more elaborate tight-binding NEGF calculations for acceptor impurities whose potential are described by the screened Coulomb potential are also shown with solid symbols in Fig. 3. There are some distinct features between the two results, which result mainly from the long-range part of the screened Coulomb potential of impurity in the NEGF calculations.

Nevertheless, an essential feature is common in these results: The constructive interference dominates for small Δ , whereas R_s becomes close to the value of the series resistance of two impurities. Figure 4 shows the *space-average* resistance of two correlated impurities at $T = 300$ and 30 K as a function of the scattering potential energy v_c . It is clear that the two approximations greatly deviate from the exact result and, thus, the multiple-impurity cannot be properly described by the weak-scattering approximations unless the coupling strength is extremely small. This implies that the non-perturbative treatment of impurity scattering is inevitable for multiple impurities in the channel. As temperature is lowered, however, the average R_s under the Born approximation becomes much better. Figure 5 shows the space-average R_s of two-impurity systems at $T = 300$ and 30 K as a function of the scattering potential energy v_c along with $2R_{\text{single}}$, R_{single} being the average resistance of the single-impurity systems. The two results at $T = 300$ K agree quite well up to large v_c where the weak-scattering approximation breaks down. Since $2R_{\text{single}}$ represents the uncorrelated series resistance of two impurities, each impurity could be regarded as independent scattering center and phase interference among the impurities almost diminishes at room temperature. As is evident from Fig. 5 for $T = 30$ K, this phase randomization results from the broadness of the energy spectrum of the in-coming electrons from the reservoirs. This is the physical origin of the “self-averaging” emerged in the average resistances under the fully coherent circumstances.

4. Conclusion

We have investigated the phase interference effects on the impurity-limited resistance due to localized impurities under the quasi-1D nanowires. We have found that the *space-average* resistance of multiple impurities is very close to the value of the series resistance of the single-impurity resistance at room temperature and each impurity could be regarded as an independent scattering center. This phase randomization is induced by the in-coming electrons from the reservoirs with broad energy spectrum.

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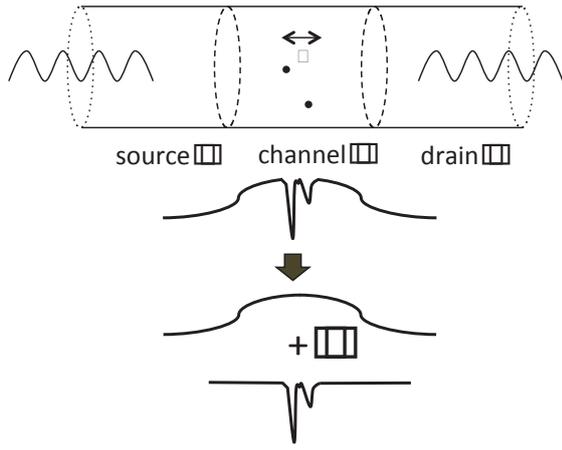


Fig.1: Schematic drawings of the nanowire with two impurities doped in the channel and the corresponding potential profile under the applied gate voltage. The whole potential modulation is treated as a single scattering potential in the scattering theory.

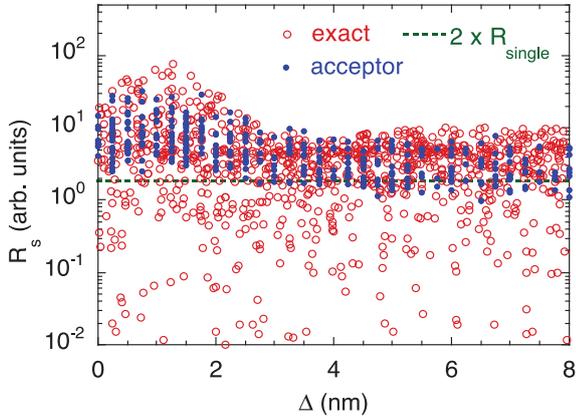


Fig.3: Impurity-limited resistances for two correlated impurities as a function of impurity separation Δ along the wire axis. Resistances for 1000 different configurations are shown. The horizontal dashed line represents $2R_{\text{single}}$. The resistances from the NEGF simulations for acceptors with realistic screened potentials are shown with solid symbols.

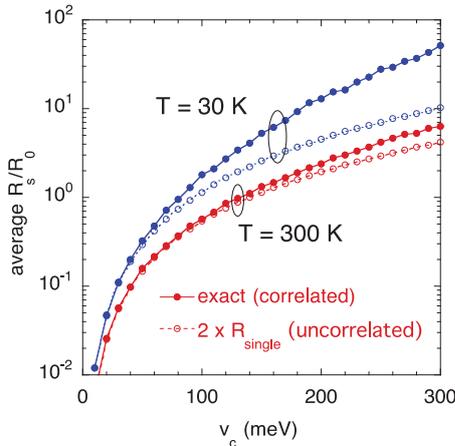


Fig.5: Space-average resistance of two correlated-impurity systems and $2R_{\text{single}}$ at $T = 300$ and 30 K as a function of the scattering potential energy v_c . R_{single} is the space-average resistance of the single-impurity systems.

Impurity-limited Resistances

exact

$$R_s(\mathbf{r}_{01}, \mathbf{r}_{02}, \Delta) = \frac{\pi \hbar}{e^2} \frac{\langle R_A(E) \rangle}{\langle 1 - R_A(E) \rangle} = \frac{\pi \hbar}{e^2} \left\{ \langle R_A(E) \rangle + \langle R_A(E) \rangle^2 + \dots \right\}$$

weak-scattering limit, non-perturbative scattering

$$R_{s,\text{weak}}(\mathbf{r}_{01}, \mathbf{r}_{02}, \Delta) = \frac{\pi \hbar}{e^2} \langle R_A(E) \rangle$$

weak-scattering limit, perturbative scattering (Born approx.)

$$R_{s,\text{weak}}^B(\mathbf{r}_{01}, \mathbf{r}_{02}, \Delta) = \frac{\pi \hbar}{e^2} \langle \Gamma_A(E) \rangle$$

$$\gamma_i(\epsilon_{k_i}, \mathbf{r}_{0i}) = v_c \frac{a}{\hbar} \sqrt{\frac{m}{2\epsilon_{k_i}}} S_{i,d}^2(\mathbf{r}_{0i})^2$$

$$R_A(E) = \frac{\gamma_1^2 + \gamma_2^2 + 2\gamma_1^2\gamma_2^2 + 2\gamma_1\gamma_2\{(1-\gamma_1\gamma_2)\cos(2k\Delta) + (\gamma_1 + \gamma_2)\sin(2k\Delta)\}}{1 + \gamma_1^2 + \gamma_2^2 + 2\gamma_1^2\gamma_2^2 + 2\gamma_1\gamma_2\{(1-\gamma_1\gamma_2)\cos(2k\Delta) + (\gamma_1 + \gamma_2)\sin(2k\Delta)\}}$$

$$\Gamma_A(E) = \gamma_1^2 + \gamma_2^2 + 2\gamma_1^2\gamma_2^2 + 2\gamma_1\gamma_2\{(1-\gamma_1\gamma_2)\cos(2k\Delta) + (\gamma_1 + \gamma_2)\sin(2k\Delta)\}$$

Fig.2: Expressions of impurity-limited resistance for two correlated impurities derived from the Landauer formula: The exact and two approximate (non-perturbative and perturbative impurity scattering under weak-scattering limit) expressions. The last expression is the conventional Born approximation.

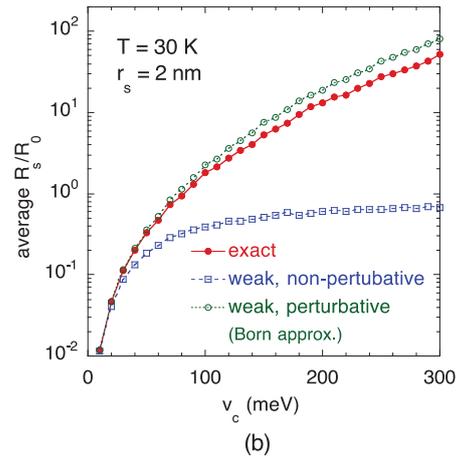
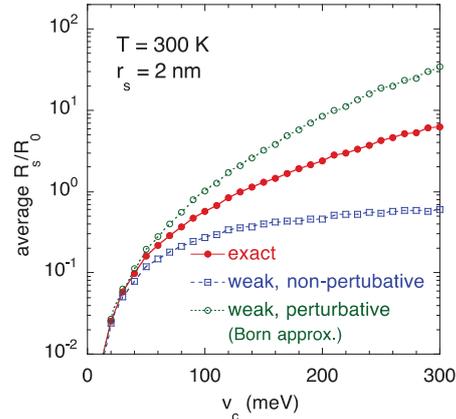


Fig.4: Space-average impurity-limited resistances of two correlated impurities as a function of the scattering potential energy v_c for (a) $T = 300$ K and (b) 30 K. The average resistances from the exact formula (red solid lines) and two approximations, $R_{s,\text{weak}}$ (blue dashed lines) and $R_{s,\text{weak}}^B$ (green dotted lines), are shown.

Numerical Analysis and Analytical Modeling of RDF in DG Tunnel-FETs

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1. Introduction

The combination of high doping concentrations in the source (s) and drain (d) region of Tunnel-FETs with an intrinsic channel leads to a diffusion of dopants from s/d towards the channel region (see Fig. 1). This greatly affects the subthreshold slope (ss) as well as the maximum ON-current of the device [1]. One of the downsides of the miniaturization of transistors nowadays is that doping concentrations are not constant within specific regions but have to be considered at discrete locations. Therefore, these discrete dopants have an increased influence on the electrostatic potential in the device. Random dopant fluctuation (RDF) hereby describes the statical variation of discrete dopants within the channel region. The model presented in this paper captures this RDF effect on MOSFET electrostatics by an equivalent variation of the gate voltage (V_g). The model can be applied on different double-gate (DG) transistor structures and in this case it is specifically applied to the DG Tunnel-FET.

2. TCAD Simulation

For the simulation with TCAD Sentaurus the following setup was chosen: Silicon device, HfO₂ oxide, $t_{ox} = 2$ nm, $t = 10$ nm, $l_{ch} = 22$ nm, $l_{sd} = 20$ nm, $N_s = 10^{20}$ cm⁻³, $N_d = 10^{19}$ cm⁻³, $N_{ch} = \text{intrinsic}$. Gaussian shaped doping profiles are applied at the channel junctions (see Fig. 1) with a standard deviation $\sigma = 1,2,3$ nm.

At first RDF was simulated in 2D using the impedance field method (IFM) [2]. Figure 2 shows the simulation results of the device. Another method of simulating RDF is with the use of randomized profiles. Therefore, the device is extended in the 3rd dimension ($w = 30$ nm) and discrete dopants are used for the simulation. In figure 3 the results are shown for 8 random samples. One can see that the gate voltage deviation σ_{V_g} is much higher in the ambipolar-state of the device in comparison to the ON-state. The reduced drain doping leads to less discrete dopants, which makes their distribution much more sensitive on the device electrostatics and especially on the tunneling distance (see Fig. 7). The high σ_{V_g} in the OFF-state is caused by the almost flat current and is not captured in the model.

3. Modelling Approach

The aim of the model is to capture the influence of random dopants in the channel region on the gate charge. Therefore, for every dopant, the associated gate charge is calculated, followed by an estimation of the equivalent change in V_g using the oxide capacitance C_{ox} . This can be done discretely for every dopant or in general, using the expected dopants in a small area of the channel region. Considering the variation of the doping concentration in the discrete volume this directly

leads to the variation of V_g .

At first the channel region has to be meshed (see Fig. 4). The expected total number of dopants can be calculated for every central point of a mesh element:

$$N = \Delta y \int_{-\frac{\Delta x}{2}}^{\frac{\Delta x}{2}} \left(N_s \cdot e^{-\frac{x^2}{\sqrt{2}\sigma^2}} + N_d \cdot e^{-\frac{(x-l_{ch})^2}{\sqrt{2}\sigma^2}} + N_{ch} \right) \cdot dx$$

Assuming a Poisson distribution for the dopants, the expected value N equals the variance of the dopants σ_N^2 [2]. Considering a point charge without boundaries, the electric field variance of these charges is given through:

$$|\sigma_E^2(\vec{r} - \vec{r}_0)| = \frac{q \cdot \sigma_N^2}{2\pi\epsilon|\vec{r} - \vec{r}_0|}$$

In order to get the equivalent charge variance σ_Q^2 , the D-field variance ($\sigma_D^2 = \epsilon \cdot \sigma_E^2$) orthogonal to the gate oxides has to be integrated (see Fig. 4) [3].

$$\sigma_Q^2(x_0, y_0) = \int_1^2 |\sigma_D^2(x_0, y_0)| \cdot \cos(\alpha) \cdot dx + \int_3^4 |\sigma_D^2(x_0, y_0)| \cdot \cos(\alpha) \cdot dx$$

For the calculation of the gate voltage variance $\sigma_{V_g}^2$ of the device follows

$$\sigma_{V_g}^2 = \int_{t_{inv}}^{t_{ch}-t_{inv}} \int_0^{l_{ch}} Q_{fit} \frac{\sigma_Q^2(x, y)}{C_{ox}} dx \cdot dy,$$

with $C_{ox} = \epsilon_{ox}/t_{ox} \cdot 2l_{ch}$, the assumed inversion layer thickness t_{inv} and a fit factor Q_{fit} , which compensates the assumed point charge without boundaries. The standard deviation of the gate voltage is then given through

$\sigma_{V_g} = \sqrt{\sigma_{V_g}^2}$. The width of the device can be considered with [2] $\sigma_{V_g}^{3D} = \sigma_{V_g}^{2D} \sqrt{1\text{cm}/w}$.

3. Results

The model is compared to the TCAD simulation data for different standard deviations of the doping profiles σ . Figure 5 shows the comparison of the model with the IFM simulation data. In Figure 6 the model, IFM and the randomized profiles are compared. Due to single dopant sensitivity at the drain-to-channel junction σ_{V_g} of the random samples is increased in the ambipolar region (see Fig. 7). This is a typical effect special to TFETs.

This work is supported by the German Federal Ministry of Education and Research under contract No.03FH001I3.

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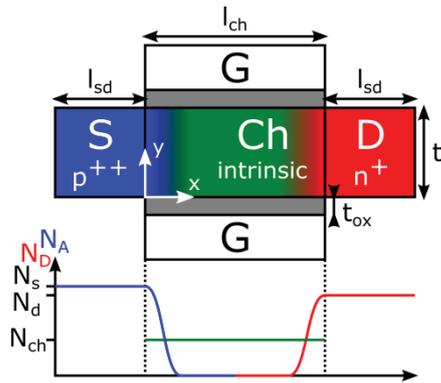


Fig.1: Geometry of a DG-n-Tunnel-FET, showing the doping profiles at the channel junctions.

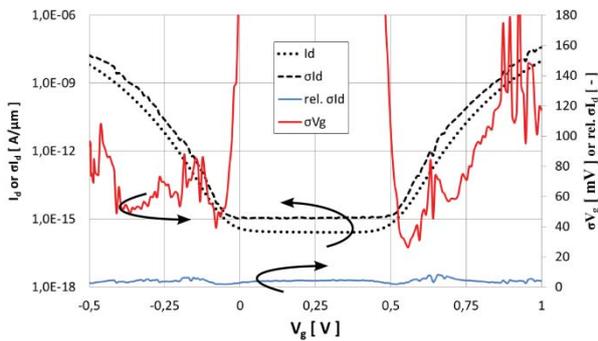


Fig.2: TCAD results for a DG n-Tunnel-FET using IFM for $\sigma = 2 \text{ nm}$, $w = 30 \text{ nm}$ and $V_d = 0.5 \text{ V}$.

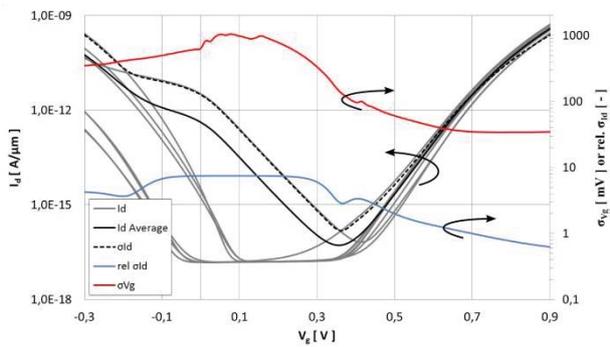


Fig.2: TCAD results for a DG n-Tunnel-FET using randomized doping profiles with $w = 30 \text{ nm}$, $\sigma = 1 \text{ nm}$ and $V_d = 0.5 \text{ V}$.

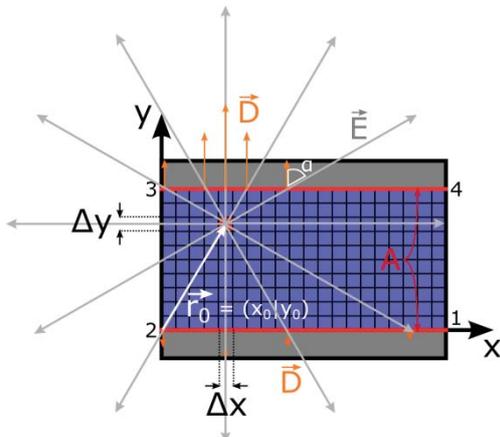


Fig.4: Meshing of the channel region and calculation of the \vec{D} -field components below the gate oxides for a specific position in the channel.

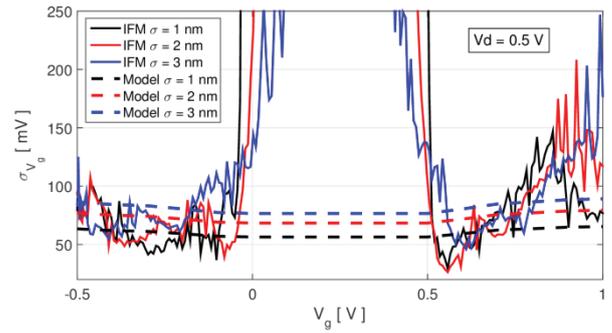


Fig.5: Comparison of the IFM TCAD Simulation data for the standard deviation of V_g with the model.

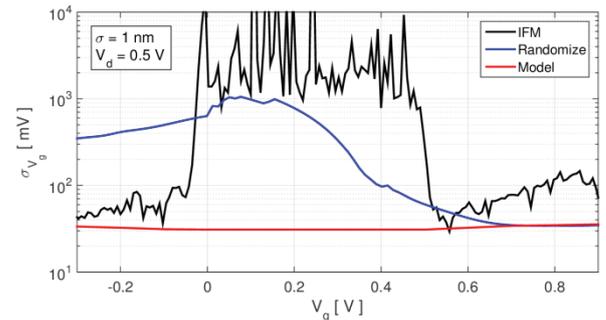


Fig.6: Comparison of the Model, IFM- and Randomize data.

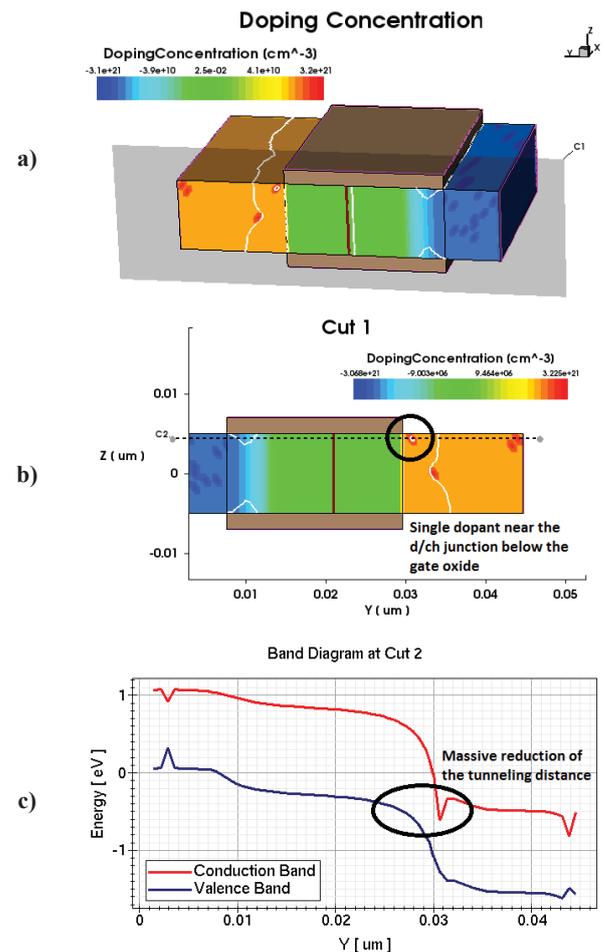


Fig.7: Influence of single dopants on the band structure.

Capacitor-less Memory: Advances and Challenges

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Several types of floating-body capacitorless 1T-DRAM memory cells with planar SOI or multi-gate 3D configurations are reviewed and compared. We focus on the recently proposed concepts (MSDRAM, A2RAM and Z²-FET), by addressing the device architecture and fabrication, operating mechanisms, and scaling issues. Experimental results together with numerical simulations indicate the directions for performance optimization, and their implementation in FDSOI 28nm (FD28) and FDSOI 14nm (FD14) technological nodes. These memory cells are the basis for the recently started European Project REMINDER “Revolutionary Embedded Memory for INternet of Things Devices and Energy Reduction”. REMINDER aims to develop an embedded DRAM solution optimized for ultra-low-power consumption and variability immunity, specifically focused on Internet of Things (IoT) cut-edge devices. REMINDER is based on three pillars:

- i) Investigation (concept, design, characterization, simulation, modelling), selection and optimization of a Floating-Body memory bit cell in terms of low power and low voltage, high reliability, robustness (variability), speed, reduced footprint and cost. Fabrication of selected bit cells with FDSOI and III-V technologies.
- ii) Design and fabrication in FD28 and FD14 technology nodes of a memory matrix based on the optimized bit-cells developed in the first pillar. Matrix memory subcircuits, blocks and architectures will be carefully analysed from the power-consumption point of view. In addition variability tolerant design techniques underpinned by variability analysis and statistical simulation technology will be considered.
- iii) Demonstration of a system on chip (SoC) application using the developed memory solution and benchmarking with alternative embedded memory blocks.

The eventual replacement of Si by strained Si/SiGe and III-V materials in future CMOS circuits would also require the redesign of different applications, including memory cells, and therefore we also propose the evaluation of the optimized bit cells developed in pillar i) in FD28 and FD14 technology nodes using these alternative materials. In order to achieve these goals, we adopt a multiscale approach that enables us to determine the band structures and the memory mechanisms (Band-to-Band Tunnelling, carrier transport and generation-recombination) in semiconductor NWs with different materials and geometries (Si, sSi, Si/Si-Ge core-shell, and III-V). We will employ numerical tools at different levels from atomic-detail (DFT) to the effective mass approximation.

We will summarize the state-of-the-art, the objectives, challenges, risks, and the proposed tasks to fulfill the goal of REMINDER Project.

Inverse-magnetostriction-induced Switching Current Reduction of STT-MTJs and its Application for Low-voltage Operation MRAMs

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1. Introduction

Low-voltage (or near-threshold voltage) operations of CMOS logic systems have attracted considerable attention owing to the ability of dramatic reduction of dynamic and static power dissipation [1]. In particular, low-voltage (~0.3-0.4V) operations can minimize the energy dissipation (or maximize the energy efficiency) of logic systems [1], and thus this operation mode is promising for always-on applications such as various wearable devices [2]. Nonvolatile data retention adaptable to low-voltage operations is highly requested for these applications. Spin-transfer torque (STT) magnetic tunnel junctions (MTJs) are expected to be a promising nonvolatile memory element for low-voltage operations owing to the current-driven operation behavior of the MTJs, i.e., as far as the critical current density (J_C) for their current-induced magnetization switching (CIMS) can be obtained at a desired low-voltage, there is no limitation for the (write-) operation voltage. Various efforts including perpendicular magnetic anisotropy electrodes have been paid to reduce J_C [3]. However, the reduction of J_C still is not enough to operate at a low-voltage for minimizing energy dissipation. J_C can be reduced by lowering the energy barrier (Δ) of MTJs. However, this degrades the thermal stability. Energy barrier reduction techniques applied only during CIMS would be promising for managing low J_C and high thermal stability. Saito et al. [4] proposed a switching field reduction technique based on the inverse magnetostriction (IMS) effect for field-induced magnetization switching of MTJs using a super magnetostriction material for the free layer. This technique would also be applied to J_C reduction for CIMS of STT MTJs. Note that pressures (<1 GPa) required for energy barrier deformation of the IMS layer of such MTJs would be obtained using a piezoelectric (PE) material with a low voltage bias (discussed later). In this paper, we propose a new STT MTJ using an IMS material for the free layer (hereafter, referred to as an IMS-MTJ) and computationally investigate IMS-induced switching current reduction of the IMS-MTJ. Energy performance of a low-voltage MRAM cell using the proposed IMS-MTJ and a high performance FinFET is also demonstrated.

2. Proposed IMS-MTJ

Fig. 1 shows a schematic device structure of the proposed STT MTJ using an IMS material for the free layer. The device is comprised of ferromagnetic electrodes (pinned and free layers), a tunnel barrier (TB), and a piezoelectric (PE) gate surrounding the MTJ part. The free layer consists of the IMS layer and high spin-polarization interfacial layer facing the TB. These two layers are magnetically coupled, i.e., the magnetization direction of the interfacial layer is governed by that of the IMS layer. The PE gate acts as a stressor to the free layer, which applies a compress pressure (P) in the free layer plane. The PE gate electrodes that apply an electric field to the PE material are also placed. In this study, SmFe_2 [5] is adopted as the IMS material, and a device structure consisting of a $\text{CoFeB}/\text{MgO}/\text{CoFeB}/\text{SmFe}_2$ MTJ part and a PMN-PT [6] gate surrounding it is employed.

3. Modelling and calculation procedure

Calculations for IMS-induced MTJ behaviour were carried out using the LLG (Landau-Lifshits-Gilbert) equation with Slonczewski's STT term [10,11]. We developed a model representing the STT term as an effective energy. The IMS effect was also treated as a magnetoelastic energy. These energies were incorporated in the LLG equation. Critical current densities for magnetization switching without/with thermally excitation [12,13] were analysed. The material constants and device parameters used in this study are shown in Table 1, which were determined by reference to reported data of IMS materials, perpendicular $\text{CoFeB}/\text{MgO}/\text{CoFeB}$ MTJs, and piezoelectronic devices [5-9]. Operations of proposed MRAM cells (shown later) were analysed by HSPICE with a 20-nm-technology FinFET PTM [14] and our developed MTJ macromodel [15]. This macromodel can closely fit experimentally observed electrical characteristics of ordinary MTJs within an error of 1.5% [15]. The device and circuit parameters used in the circuit simulations are shown in Table 2.

4. IMS-MTJ characteristics

Fig. 2 shows the calculated effective energy barrier for the IMS free layer as a function of tilt angle θ of the magnetization (also see Fig. 1 (a)). The

energy barrier can be reduced by P applying to the free layer owing to the IMS effect (Fig. 2). The STT magnetization switching (CIMS) occurs when the energy barrier disappears, and thus the IMS-induced barrier lowering is effective at reducing the critical current of the CIMS, as shown in Fig. 2(b). Here, the critical current density J_{C0} is defined by a switching current just when the energy barrier becomes zero. Note that when $P = 0$, this quantity is completely identical with Slonczewski's J_{C0} [11]. The effective barrier decreases with J depending on P , and J_{C0} can be reduced with increasing P , as shown in Fig. 3. J_{C0} also decreases with decreasing Δ . Although this phenomenon is qualitatively the same as the case of ordinary STT MTJs, J_{C0} can be diminished by P without reducing Δ for the proposed IMS-MTJ. To clarify the impact of the switching error rate of the IMS-MTJ on the critical current, the thermal excitation effect is included in our calculations using a model proposed by Koch *et al.* [12]. Fig. 4 shows the bit error rate (BER) as a function of J at room temperature, in which P is varied and the pulse width t_p for J and P are fixed at 30 ns. The BER rapidly increases with decreasing J for each P condition, when J is lower than J_{C0} . Therefore, the critical current density J_{CT} determined by a given BER is important in practice and used for the following discussion. Fig. 5 shows J_{CT} as a function of P , in which BER is varied. J_{CT} decreases with increasing P depending on BER. Fig. 6 shows J_{CT} as a function of t_p for $\text{BER} = 10^{-6}$. The non-linear behaviour of the J_{CT} - t_p curve appears for all the pressure conditions and J_{CT} increases with decreasing t_p . The magnetization switching with $J_{CT} = 0.1 \text{ MA/cm}^2$ and $\text{BER} = 10^{-6}$ can be achieved for a moderate t_p (several tens of nanoseconds).

5. Low-voltage MRAM application

Fig. 7 shows two types of MRAM cells using an IMS-MTJ. The cell shown in Fig. 7(a) is the same configuration as conventional MRAM cells, i.e. the cell configuration with the drain-side MTJ connection (DSM cell). The cell shown in Fig. 7(b) has a configuration with the source-side MTJ connection (SSM cell), in which the connected MTJ feeds back its voltage drop to the gate of the MOSFET. Since the degree of this negative feedback depends on the resistance states of the MTJ, the cell currents of the SSM cell can effectively controlled by the magnetization configuration of the MTJ (shown later). In this study, a FinFET is used for both the cells. Table 3 shows operation architecture of these cells. The IMS effect is not induced during the read operation, and it is employed only during the write operation. Fig. 8 shows P as a function of V_{PE} (that is a bias voltage of the PE gate; see Fig. 1(b)). P required for the IMS-induced switching current reduction described above (several hundreds of MPa) can easily be yielded by $V_{PE} = 0.2 \text{ V}$ or less. Figs. 9(a) and (b) show cell currents as a function of V_{DD} for the DSM and SSM cells, respectively, during the read operation, in which V_{PE} and V_G are set to zero and V_{DD} , respectively. Although the cell currents of the SSM cell is lower than those of the DSM cell, its magnetocurrent ratio (that is a ratio of the cell currents in the parallel and antiparallel configurations) is sufficiently high to distinguish the parallel and antiparallel states even at $V_{DD} = 0.3 \text{ V}$. In addition, the magnetocurrent ratio can be enhanced by the number of the fin channel of the FinFET, as shown in Fig. 10. On the other hand, the magnetocurrent ratio of the DSM cell is severely degraded for lower V_{DD} operations. Note that when V_{DD} is less than 0.4 V, the magnetization switching does not occur during the read operation (since the cell currents do not exceed J_{CT} for $V_{PE} = 0 \text{ V}$; see Table 2). Fig. 11 shows cell currents during the write operation for the SSM cell (in which V_{PE} is applied). The cell current can exceed J_{CT} for the IMS-induced switching when $V_{DD} \geq 0.2 \text{ V}$. Fig. 12 shows the write energy of the SSM cell. By reducing V_{DD} from 0.9 V to 0.2V, the write energy can be considerably reduced to 1/400.

6. Conclusion

We proposed a new STT MTJ using a super magnetostriction material for the free layer and computationally showed its effective switching current reduction. A low-voltage MRAM cell using the proposed MTJ can largely reduce the write energy without degradation of the thermal stability.

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Table 1: Material constants and device parameters for inverse-magnetostriction (IMS) MTJ

MTJ part											PE gate part			
K_u	M	λ	α	R	l_m	Δ	η	τ_0	Y_{MTJ}	Y_{PE}	N	ϵ_{33}^S	d_{31}	
(MJ/m ³)	(T)	(ppm)		(nm)	(nm)			(ns)	(GPa)	(GPa)			(nm/V)	
0.43, 0.56, 0.69	0.64	-1258	0.005	10	2	40, 60, 80	1	1	40	60	0.3	741	-0.852	

K_u : Uniaxial magnetic anisotropic energy density, M : Saturation magnetization, λ : Magnetostrictive constant, α : Damping constant, R : Radius of the MTJ pillar, l_m : thickness of the IMS layer, η : Spin transfer efficiency, τ_0 : Attempt time, Y_{MTJ} , Y_{PE} : Young modules of the MTJ and PE parts, v : Poisson's ratio, ϵ_{33}^S : Relative permittivity, d_{31} : Piezoelectric strain constant.

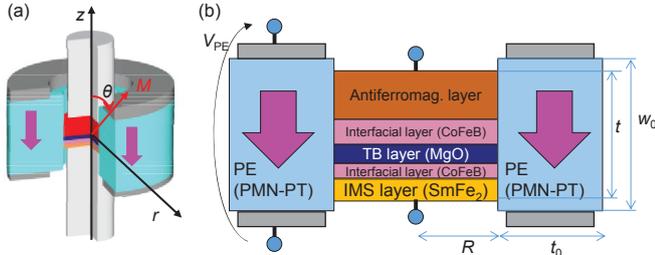


Fig. 1: (a) Schematic device structure and (b) cross section of a proposed IMS-MTJ. The dielectric polarization of the piezoelectric (PE) gate is parallel to the z axis. One of possible structures consists of a CoFeB/MgO/CoFeB/SmFe₂ MTJ and a surrounding PMN-PT gate.

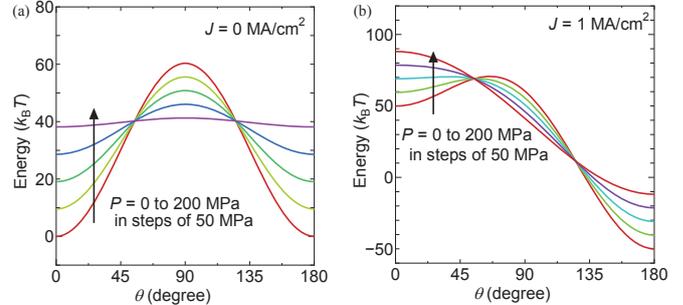


Fig. 2: Energy curves for the IMS free layer of the IMS-MTJ, in which (a) P is varied with $J=0$, and (b) P is varied with $J=1$ MA/cm². J and P represent current density passing through the device and pressure applied to the IMS layer, respectively.

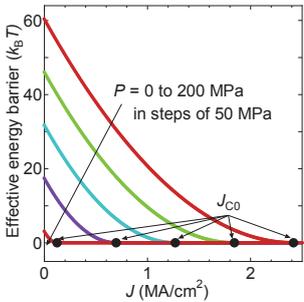


Fig. 3: Energy barrier as a function of J , in which P is varied from 0 to 200 MPa in steps of 50 MPa.

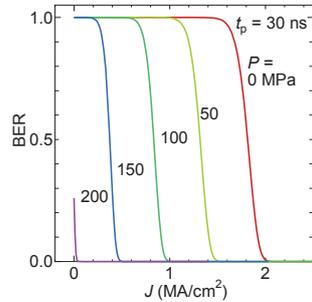


Fig. 4: BER as a function of J , in which P is varied from 0 to 200 MPa in steps of 50 MPa.

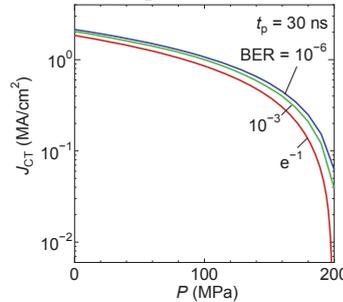


Fig. 5: J_{CT} as a function of P for (a) various BERs. The definition of J_{CT} is described in the text.

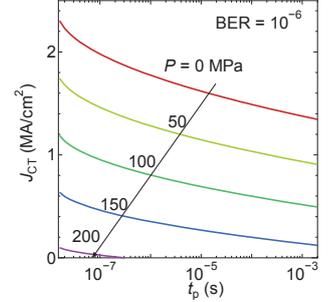


Fig. 6: J_{CT} as a function of t_p for BER = 10⁻⁶, in which P is varied from 0 to 200 MPa in steps of 50 MPa.

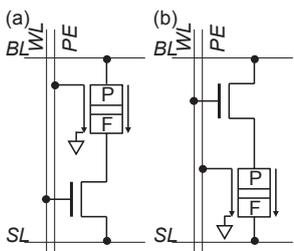


Fig. 7: Low-voltage MRAM cells using an IMS-MTJ with (a) drain-side MTJ connection (DSM) and (b) source-side MTJ connection (SSM) configurations.

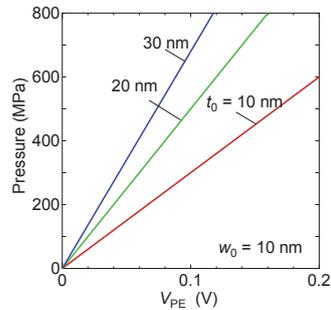


Fig. 8: P as a function of V_{PE} . V_{PE} represents a bias voltage of the PE gate (see Fig.1 (b)).

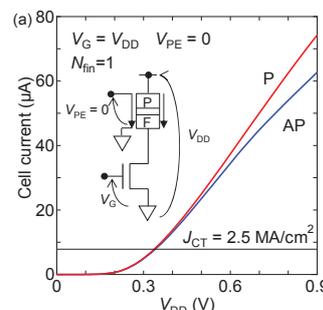


Fig. 9: Cell currents as a function of V_{DD} for (a) the DSM cell and (b) the SSM cell during the read operation mode.

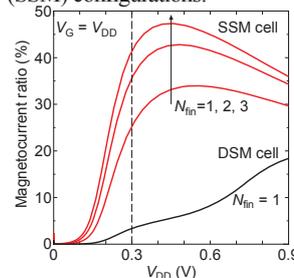
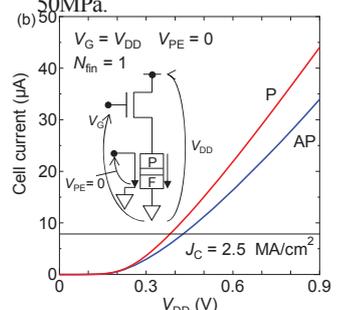


Fig. 10: Magnetocurrent ratio as a function of V_{DD} for the DSM and SSM cells during the read operation mode.

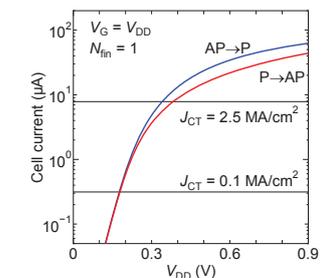


Fig. 11: Cell currents as a function of V_{DD} for the SSM cell during the write operation mode.

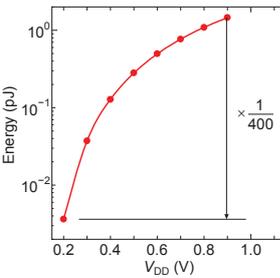


Fig. 12: Write energy as a function of V_{DD} for the SSM cell.

Table 2: Simulation parameters for low-voltage MRAM

MTJ	Tunneling magnetoresistance: TMR	100%
	Resistance-area product: RA	2 $\Omega \cdot \mu\text{m}^2$
	Voltage at half-maximum TMR: V_{half}	0.5 V
	J_{CT} without the IMS effect	2.5×10^6 A/cm ²
	J_{CT} with the IMS effect	0.1×10^6 A/cm ²
	Resistance: $R_P(0)$ (Parallel mag.)	6.36 k Ω
	$R_{AP}(0)$ (Antiparallel mag.)	12.7 k Ω
FinFET	Channel length: L	20 nm
	Fin width	15 nm
	Fin height	28 nm

Table 3: Read/write operation architecture.

	Read	Write(AP→P)	Write(P→AP)
BL	H	L	H
SL	L	H	L
WL	H	H	H
PE	L	H	H

A Consistent Picture of Cycling Dispersion of Resistive States in HfO_x RRAM

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Introduction. As RRAM technology is approaching the industrial stage, the evaluation of cycling dispersion [1] is essential to evaluate the technology potential. Dispersion is a critical concern for HfO_x RRAM applications, such as low-power non-volatile memory [1], and neuromorphic computing [2]. In this paper, we systematically analyze a wide set of experimental data to perform a thorough investigation of cycling dispersion. A RRAM compact model [3] is used to link the device electrical response to its physical characteristics, providing a clear picture of dispersion implications on the device reliability. Results are exploited to evidence a trade-off between power dissipation and device reliability.

Devices and Experiments. TiN/5nm-Ti/3.4nm- HfO_2 /TiN RRAM devices in 1T1R configuration are measured under different operating conditions (temperature - T , reset voltage - V_{RESET} , current compliance - I_C), Fig. 1a. Initially, devices are formed using different I_C . This creates a conductive filament (CF) composed of oxygen vacancies, Vo [4-5]. The CF cross-section, S (and so R_{LRS}), is controlled by I_C [6]. After forming, each device is cycled 50 times and I-V curves are measured, Fig. 1a. Each cycle includes a reset operation, driving the device from low- (LRS) to high-resistive state (HRS), and a set operation, driving the cell in LRS. Particularly, the reset operation drives the oxygen ions around the CF towards its bottom end, where they recombine with the Vo in the CF leading to the re-oxidation of its bottom tip [5]. This forms a dielectric barrier [3-5] with cross-section S and thickness x (see Fig. 2c), which can be modulated using different V_{RESET} [1-8]. So R_{HRS} depends on both S and x [1-8]. The set operation, performed with the same I_C as in forming, causes the barrier breakdown, restoring the full CF [3-8].

HRS and LRS Statistics. Data are used to extract the device resistance in HRS and LRS, i.e. R_{HRS} and R_{LRS} , at the read voltage $V_{\text{READ}}=0.1\text{V}$, Fig. 1a. The corresponding distributions reveal two different behaviors: while R_{LRS} follows a normal distribution, R_{HRS} is log-normally distributed, Fig. 1b, in agreement with previous studies [1] and other reports [4,7-8]. The R_{LRS} and R_{HRS} dispersion is attributed to the randomness of the physical mechanisms involved in reset and set operations [5,7]. The transition to the HRS during reset results from random recombination events, which cause variations of the barrier thickness at each cycle [7]. Similarly, the transition to the LRS during set is determined by random Hf-O bond breakage events [5] resulting in variations of S at each cycle [7].

Results and Discussion. We exploit our compact model [3] to link the electrical dispersion of R_{HRS} and R_{LRS} to the physical variations of x and S , Fig. 2. Interestingly, the normal R_{LRS} distribution corresponds to a normal S distribution, while the log-normal R_{HRS} distribution arises from a normal x distribution [1], Fig. 2d. Dealing only with normal distributions can be helpful, as normal distributions are completely described by the mean μ and the standard deviation σ . This allows discussing physical variability by using four simple physical indicators, namely μ_x , σ_x , μ_S , and σ_S . We systematically study dispersion at different operating conditions reporting the “ 6σ distributions”, i.e. $\mu \pm 3\sigma$, required by the industry to completely evaluate the technology potential and to determine circuit design constraints. We start the analysis discussing the influence of V_{RESET} on both x and S . Fig. 3a shows the trends of μ_x and σ_x vs. V_{RESET} . μ_x is increased by higher V_{RESET} , in agreement with the evidence [1-8] that a higher V_{RESET} results in a higher R_{HRS} . σ_x is instead constant, which suggests that x dispersion is related to

the O ions availability during the reset operation [5], independently of the applied voltage. Fig. 3b shows the relative x immunity to variations, described by μ_x/σ_x . Clearly, higher V_{RESET} result in higher relative x immunity. Nevertheless higher V_{RESET} does not translate in higher relative R_{HRS} immunity, due to the non-linear relation between x and R_{HRS} [1,3-7]. Fig. 4 shows the trends of μ_S , σ_S , and μ_S/σ_S as a function of V_{RESET} . Conceivably, they show no dependence on V_{RESET} confirming that the reset operation has no influence on the CF size, S . The analysis of dispersion at different switching temperatures, T , reveals a similar portrait, Fig. 5a. The compact model has also been proved to correctly include temperature effects [8]. A higher T during reset provides a thicker average dielectric barrier [8], while its variance is constant, Fig. 5a. A higher T implies indeed a more effective diffusion of the O ions during reset, leading to a thicker barrier. Still this has no effect on the O ions availability, which is consistent with σ_x trend. Fig. 6 shows that a higher switching temperature has a negligible effect on R_{LRS} and its dispersion, confirming that S is controlled solely by I_C . The analysis of the impact of I_C on x and S dispersion reveals interesting details. Results in Fig. 7a show that I_C controls μ_S , as reported in the literature [3-6]. However, an I_C reduction also produces an increased S (and R_{LRS}) dispersion, σ_S . This means that scaling I_C critically lowers the relative S immunity to variations, μ_S/σ_S , Fig. 7b. Moreover, I_C scaling dramatically affects also x dispersion, Fig. 8a. While μ_x is not affected by the choice of I_C (as expected), results in Fig. 8a clearly show a significant increase of σ_x at low I_C . We attribute this behavior to the small S at low I_C , which enhances the effects of reset operation randomness. The recombination of each individual Vo has indeed a strong impact on the formation of the barrier when the CF is composed of few Vo 's. So, small variations in the number of recombination events may induce relatively large variations of the barrier thickness, x . Conversely, at high I_C the CF encompasses many Vo 's and the relative effect of an individual recombination event on x is much weaker. This highlights the critical role played by I_C . Its reduction is largely chased by designers for low-power applications. However, reducing I_C may result in a critical increase of cycling dispersion of both x and S . Notably, I_C scaling affects the average values of both R_{HRS} and R_{LRS} (i.e. $R_{\text{HRS,AVG}}$ and $R_{\text{LRS,AVG}}$, respectively) leaving the median memory window (i.e. $R_{\text{HRS,MED}}/R_{\text{LRS,MED}}$) unaltered, Fig. 9. However, it also determines a severe degradation of the worst-case read window (i.e. $R_{\text{HRS,MIN}}/R_{\text{LRS,MAX}}$), which is the true margin between HRS and LRS through the device lifetime to be considered in circuit design, Fig. 9.

Conclusions. This systematic study of cycling dispersion delivers a clear picture of its sensitivity to the operating conditions in HfO_x RRAM devices. Particularly, the dispersion of both R_{HRS} and R_{LRS} is worsened at low I_C , which reduces the worst-case read window. This shows a trade-off between reliability and power consumption.

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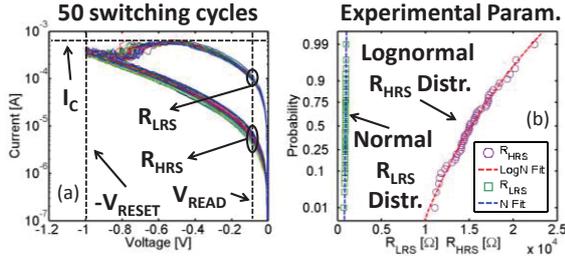


Fig. 1 – (a) Reset I-V curves of an RRAM device cycled 50 times. The current compliance, I_C , the read voltage, V_{READ} , and the reset voltage, V_{RESET} , are reported. The R_{LRS} and R_{HRS} dispersion sensed at V_{READ} is shown (black circles). (b) Corresponding R_{LRS} (normal) and R_{HRS} (log-normal) distributions and fittings.

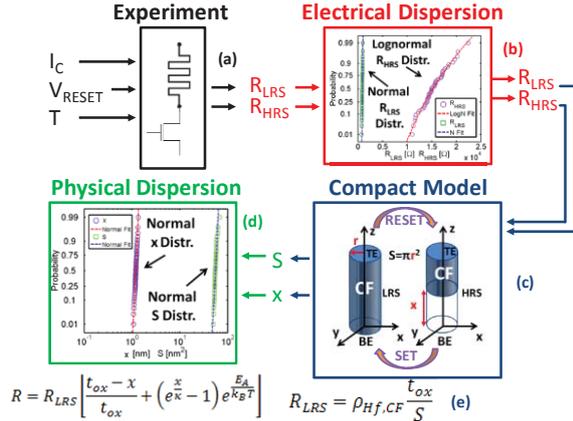


Fig. 2 – (a) Experiments are run at given operating conditions (I_C , V_{RESET} , T), returning the R_{LRS} and R_{HRS} distributions over cycling (b). These are fed to the compact model (c) translating electrical quantities to physical ones (x and S), both normally distributed (d). In (c), a 3D schematic depiction of the device in LRS and HRS is reported. (e) Compact model equations: R is the device resistance, t_{ox} (x) the oxide (barrier) thickness, κ a tunneling constant [3], E_A the activation energy, k_B the Boltzmann constant, $\rho_{Hf,CF}$ the CF resistivity, S its cross-section.

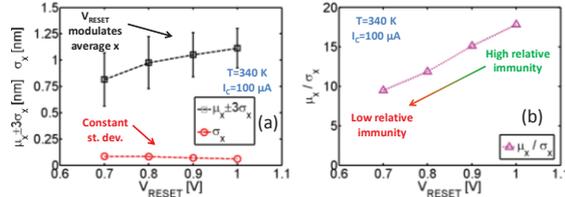


Fig. 3 – (a) Trends of μ_x (6 σ distributions) and σ_x vs. V_{RESET} for a device formed at $I_C=100\mu A$ and cycled at $T=340K$. (b) Relative x immunity to variations (μ_x/σ_x) vs. V_{RESET} for the same device.

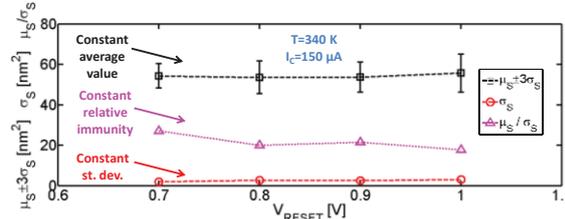


Fig. 4 – Trends of μ_S (6 σ distributions), σ_S , and μ_S/σ_S vs. V_{RESET} for a device formed at $I_C=150\mu A$ and cycled at $T=340K$.

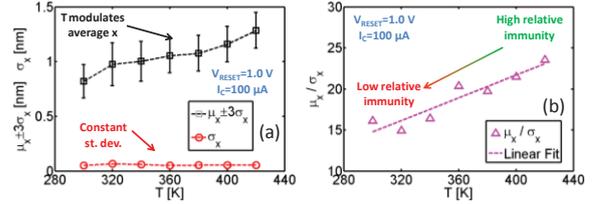


Fig. 5 – (a) Trends of μ_x (6 σ distributions) and σ_x vs. T for a device formed at $I_C=100\mu A$ and cycled with $V_{RESET}=1.0V$. (b) Relative x immunity to variations (μ_x/σ_x) vs. T for the same device along with linear fitting.

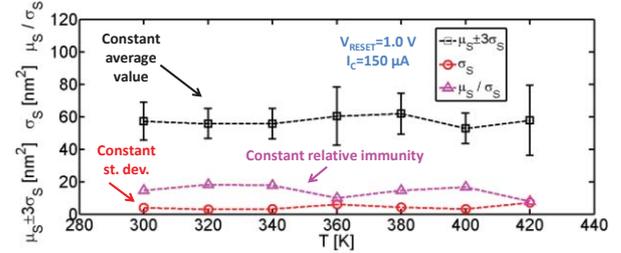


Fig. 6 – Trends of μ_S (6 σ distributions), σ_S , and μ_S/σ_S vs. T for a device formed at $I_C=150\mu A$ and reset at $V_{RESET}=1.0V$.

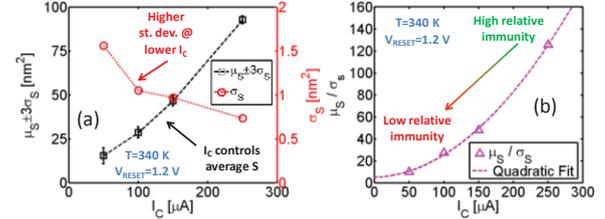


Fig. 7 – (a) Trends of μ_S (6 σ distributions) and σ_S vs. I_C . All devices are cycled at $V_{RESET}=1.2V$ and $T=340K$. (b) Relative S immunity to variations (μ_S/σ_S) vs. I_C with quadratic fitting.

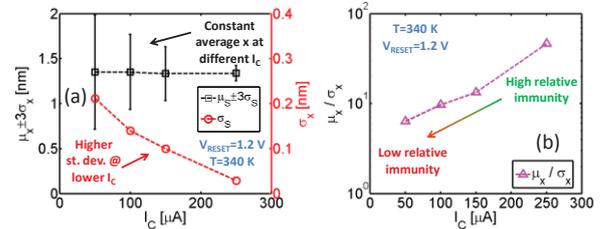


Fig. 8 – (a) Trends of μ_x (6 σ distributions) and σ_x vs. I_C . All devices (same as in Fig. 7) are cycled at $V_{RESET}=1.2V$ and $T=340K$. (b) Relative x immunity to variations (μ_x/σ_x) vs. I_C .

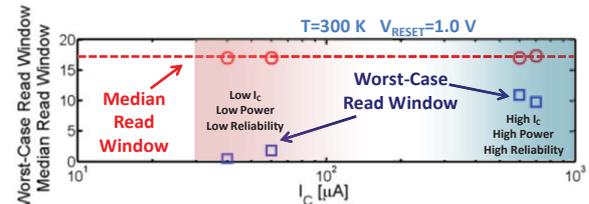


Fig. 9 – Trade-off between power consumption (proportional to I_C) and reliability. Small x and S dispersion at high I_C (blue-shaded zone) implies a small difference between the median ($R_{HRS,MED}/R_{LRS,MED}$ - red circles) and the worst-case read window ($R_{HRS,MIN}/R_{LRS,MAX}$ - blue squares). At low I_C (red-shaded zone), increased x and S dispersion causes a significant reduction of the worst-case read window.

Performance and Reliability Comparison of 1T-1R RRAM Arrays with Amorphous and Polycrystalline HfO₂

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1. Introduction

Recent advances in Resistive Random Access Memories (RRAM) technology gathered significant interest for several applications. However, the choice of proper Metal-Insulator-Metal (MIM) technology for RRAM cells exhibiting good uniformity and low switching voltages is still a key issue for array structures fabrication and reliable electrical operation [1]. Such a process step is mandatory to bring this technology to a maturity level. In this work, a comparison between 1T-1R RRAM arrays manufactured either with amorphous [2] or polycrystalline [3] HfO₂ MIM in terms of performance, reliability, intra-cell and inter-cell variability [4] is reported.

2. Experimental Setup

The 1T-1R memory cells in the 4kbits arrays (see Fig. 1) are constituted by a select NMOS transistor manufactured with a 0.25 μm BiCMOS technology, which also sets the current compliance, whose drain is in series to a MIM stack. The variable MIM resistor is composed by 150 nm TiN top and bottom electrode layers deposited by magnetron sputtering, a 7 nm Ti layer, and 8 nm HfO₂ layer deposited with two different Atomic Vapour Deposition (AVD) processes resulting either in amorphous (A) or polycrystalline (P) HfO₂ films, respectively. The resistor area is equal to 0.4 μm^2 . For amorphous films it has been integrated also a resistor with larger area that previously shown improved reliability and performance (i.e., 1 μm^2) [5]. The Forming/Set/Reset operations on the arrays were performed by using an Incremental Pulse and Verify algorithm. The bitline (BL), sourceline (SL) and wordline (WL) voltages applied during Forming, Set, Reset and Read operations are reported in Tab. 1. Reset operations were performed by applying the highest WL voltage available (2.8 V on array A and 2.5 V on array P) to maximize the cells switching yield while avoiding the breakdown of the MIM [6]. Pulses were applied during Forming by increasing V_{BL} with $\Delta V_{\text{BL}}=0.01\text{V}$, whereas during Set and Reset $\Delta V_{\text{BL}}=0.1\text{V}$ and $\Delta V_{\text{SL}}=0.1\text{V}$ have been used, respectively. Each pulse featured a duration of 10 μs , with a rise/fall time of 1 μs to avoid overshoot issues. Set operation was stopped on a cell when the read-verify current reached 20 μA , whereas Reset was stopped when 10 μA was reached. Forming, Set and Reset BL/SL voltages necessary to reach the requested read-verify current targets are extracted from the characterization data and labelled as V_{FORM} , V_{SET} and V_{RES} , respectively.

3. Experimental Results

Fig. 2 shows the average current ratios between Low Resistive State (LRS) and High Resistive State (HRS) read currents ($I_{\text{LRS}}/I_{\text{HRS}}$), calculated on the entire cells population during SET/RESET cycling at $V_{\text{read}} = 0.2\text{V}$ on arrays using A-HfO₂ (A-arrays) and P-HfO₂ (P-array), and their relative dispersion coefficient. P-array showed higher Ratio (≈ 2.8) even after 5k cycles, but also a higher dispersion coefficient [5] after Forming (i.e., cycle 1). Fig. 3 shows a comparison between I_{LRS} and I_{HRS} cumulative distributions measured at cycle 1 and after the endurance test: A-arrays show more compact distributions at cycle 1, however after the endurance test P-array shows a higher percentage of correctly switching cells reaching the Set/Reset verify targets. Fig. 4 shows the average Set and Reset switching voltages (V_{SET} , V_{RES}) and their relative dispersion coefficients: lower V_{SET} and V_{RES} are required on P-array which shows no variations during the endurance test, whereas V_{SET} , V_{RES} increase on A-arrays during cycling. V_{RES} on P-array shows the highest variability. Fig. 5 shows the cumulative distributions of Forming, Set and Reset switching voltages at cycle 1 and after the endurance test: P-array requires lower V_{FORM} , V_{SET} and V_{RES} . Since P-array shows a more compact distribution on V_{SET} and a larger V_{RES} than A-arrays, faster Set operation could be reliably used on P-array, whereas on Reset an incremental pulse with verify technique is required to ensure good reliability. Fig. 6 shows the average energy required to perform Set and Reset operations on a single cell: P-array shows lower power consumption with a lower increase during cycling. Additional details about the results and the extension of the characterizations up to 10k cycles will be provided in the full paper.

4. Conclusions

1T-1R RRAM arrays manufactured with P-HfO₂ shows several advantages compared to A-HfO₂ even considering their improved process: higher current Ratio, lower switching voltages, lower power consumption, minor endurance degradation and higher overall yield. Moreover, P-array show very low V_{SET} variability, hence faster Set operation could be reliably performed. P-array disadvantages are represented by the larger HRS distribution after Forming and the higher Reset voltage dispersion.

Acknowledgements

This work was supported by the European Union's H2020 research and innovation programme under grant agreement N°640073.

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Operation	V_{SL} [V]	V_{BL} [V]	V_{WL} [V]
Forming	0	2→3.2	1.5
Set	0	0.2→3.2	1.5
Reset	0.2→3.2	0	2.5 (A) 2.8 (P)
Read	0	0.2	1.5

Tab. 1. Forming, Set, Reset and Read Parameters.

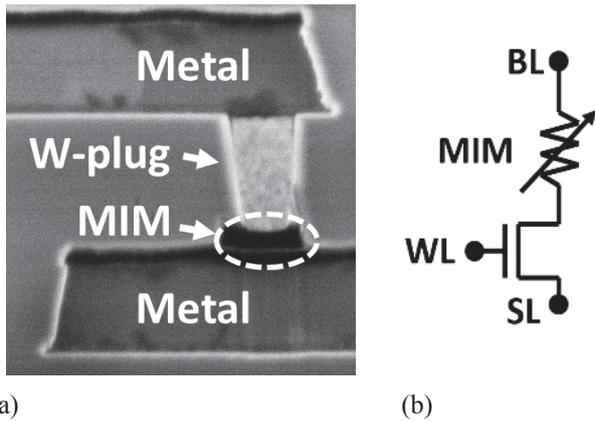


Fig. 1. Cross-sectional STEM image (a) and schematic (b) of the 1T-1R cell integrated in the arrays.

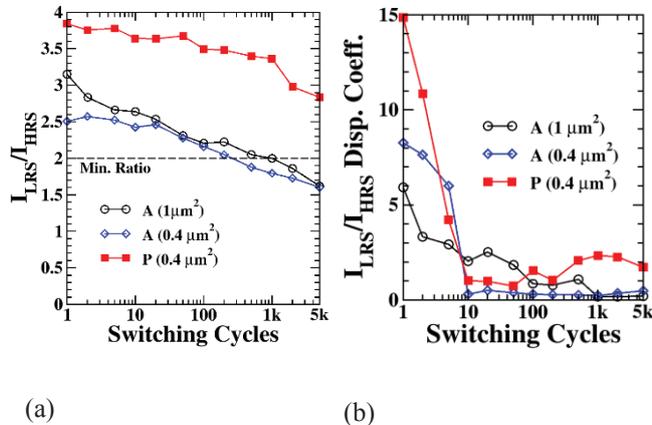


Fig. 2. I_{LRS}/I_{HRS} current ratio average values (a) and dispersion coefficients (b) calculated during cycling.

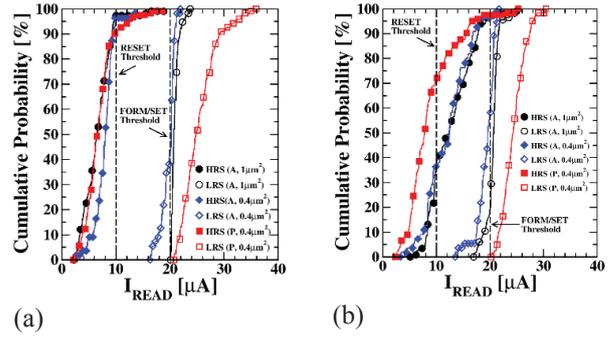


Fig. 3. I_{HRS} and I_{LRS} cumulative distributions at cycle 1 (a) and at cycle 5k (b).

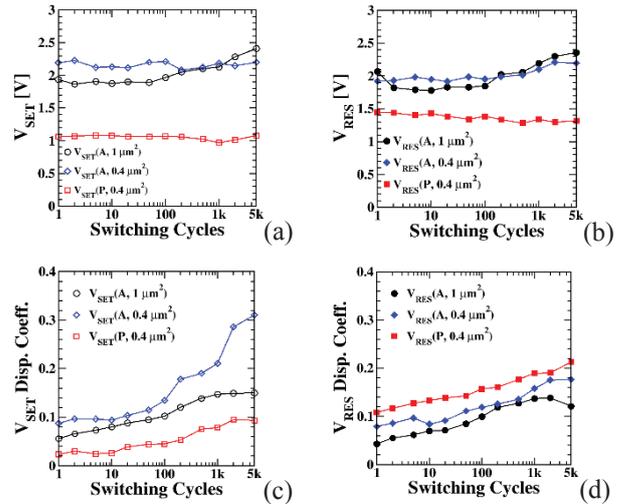


Fig. 4. V_{SET} and V_{RES} average values (a,b) and dispersion coefficients (c,d) calculated during cycling.

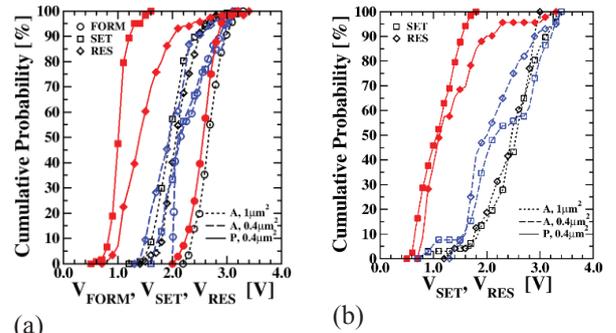


Fig. 5. V_{FORM} , V_{SET} and V_{RES} cumulative distributions at cycle 1 (a) and at cycle 5k (b).

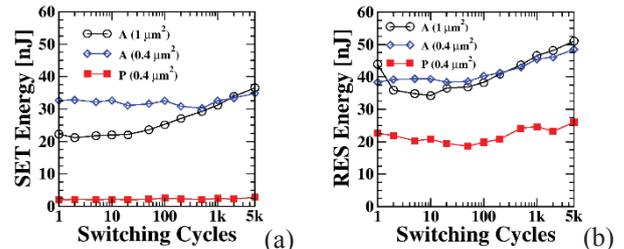


Fig. 6. Energy required to perform Set (a) and Reset (b) operations as a function of the Set/Reset cycle number.

Intra-device Statistical Parameters in Variability-aware Modelling of Resistive Switching Devices

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1. Introduction

Resistive Switching (RS) devices have become potential candidates for nonvolatile memory applications and promising basis of new computing architectures [1-3]. To explore circuit and memory designs based in RS devices, electrical models are needed, implementable in circuit simulation tools [4-6]. In this scenario, one of the challenges is to develop models that account for the large variability observed in the RS devices electrical characteristics. This work is focused on the intra-device variability. The statistical distributions of the model parameters in an equivalent circuit model are obtained from experimental data and their main properties analyzed. A procedure is developed to correctly reproduce these distributions.

2. Results.

RS devices suffer from large intra-device variability, both at low resistive state (LRS) and high resistive state (HRS), which must be properly accounted for in SPICE-like models. As example, figure 1 shows typical RS I-V curves obtained during 400 cycles on a Ni/HfO₂/n⁺Si device structure. Note the large cycle-to-cycle variability in the device electrical characteristics, especially in the HRS. To model these curves (at both LRS and HRS) we use a Resistor-Diode circuit (inset in Fig. 1) whose output is fully defined by three parameters: the resistance (R), the diode saturation current (I_s) and diode ideality factor (n) [7, 8].

An automatized fitting process has been developed to extract the three circuit parameters corresponding to each I-V curve, within operation regime ($V \leq 1$). Figure 2 shows several examples of fittings of the experimental I-V curves, where it can be observed that the circuit is able to correctly reproduce the measurements, regardless of the device state and current magnitude. The fitting of all the curves (3000 in the example shown) allows obtaining the statistical distributions of the model parameters. Dots in figure 3 a, b and c show the experimental cumulative probability distributions of the 'R', 'I_s' and 'n' parameters, for the LRS and HRS states. Clearly, two different ranges of values are obtained for the 'R' and 'I_s' parameters, ascribed to the LRS and HRS. However, the 'n' parameter distributions for the HRS and LRS overlap, being the spread larger for the HRS case. An important point is the correlation between the model parameters. Figure 4 shows a 3D plot of the complete set of parameters, for the LRS (left) and HRS (right). The projections on the three planes show that the correlation between parameters cannot be neglected, being larger for the HRS.

To accurately include the RS variability into circuit simulators, the statistical distributions of the Resistor-Diode model parameters (Fig. 3) have to be properly described. However, the complexity of these statistical distributions makes difficult to take advantage of analytical expressions. For this reason, we have used a random number generator implicit method, which correctly reproduces the statistical distributions of all the parameters (lines in Fig. 3) and also the correlation between parameters (not shown). The extrapolation of the experimental distributions to extreme percentiles allows increasing the statistical sample size

The Resistor-Diode circuit and the generated statistical parameters have been introduced into a circuit simulator, and the resulting currents have been compared to the experimental results (Fig. 5). The good agreement between the experimental and simulated current distributions allows concluding that with the presented procedure the RS variability can be properly reproduced in circuit simulators, even when complex distributions are obtained, such is the case.

3. Conclusions

A diode-resistor equivalent circuit model has been used to describe the RS electrical characteristics, for both LRS and HRS. The fitting of a large number of I-V curves (obtained during device cycling) has allowed evaluating the statistical distributions of the model parameters, which cannot be described by simple analytical expressions. A method has been proposed to correctly reproduce the experimental distributions, which accounts for the observed parameter correlation. The model (and the suitable model parameters) can be introduced into circuit simulators to analyze the impact of device variability on circuit performance.

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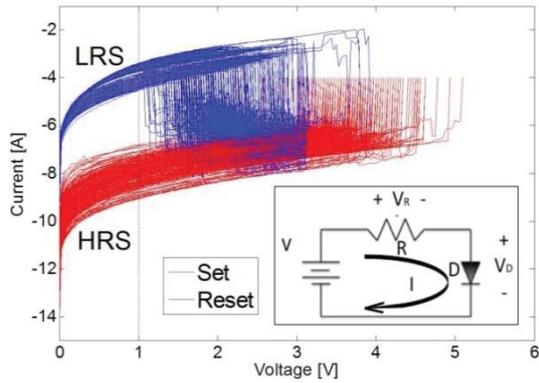


Figure 1: Typical I-V curves obtained during 400 RS cycles. A current limit of 100uA was used during Set. (Inset) Model for the RS characteristics based on a Diode-Resistance circuit. Resistance value (R), and saturation current (I_s) and ideality factor (n) of the diode are used to fit the conduction at both resistive states. Samples used were Ni/HfO₂/n⁺Si devices with 20nm HfO₂ layer and area of 5x5μm².

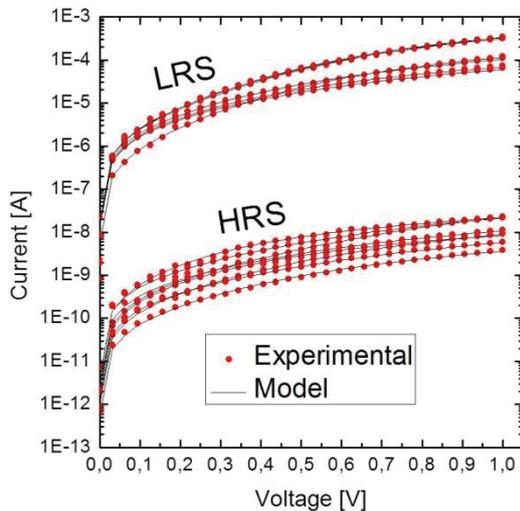


Figure 2: Examples of LRS and HRS I-V curves fittings. Circles correspond to the experimental results and lines to the model fittings. With the suitable parameter sets, the model reproduces properly the experimental curves at both states.

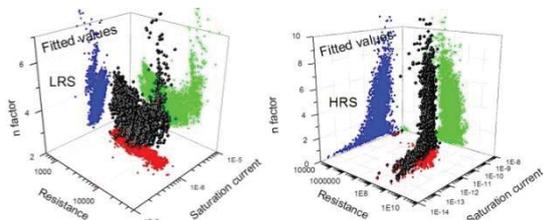


Figure 4: 3D plot of model parameter sets (black points) obtained from the fitting of the experimental curves for the LRS (left) and the HRS (right). Projections show the correlation between parameters separately. Correlation between parameters at HRS is larger than at LRS.

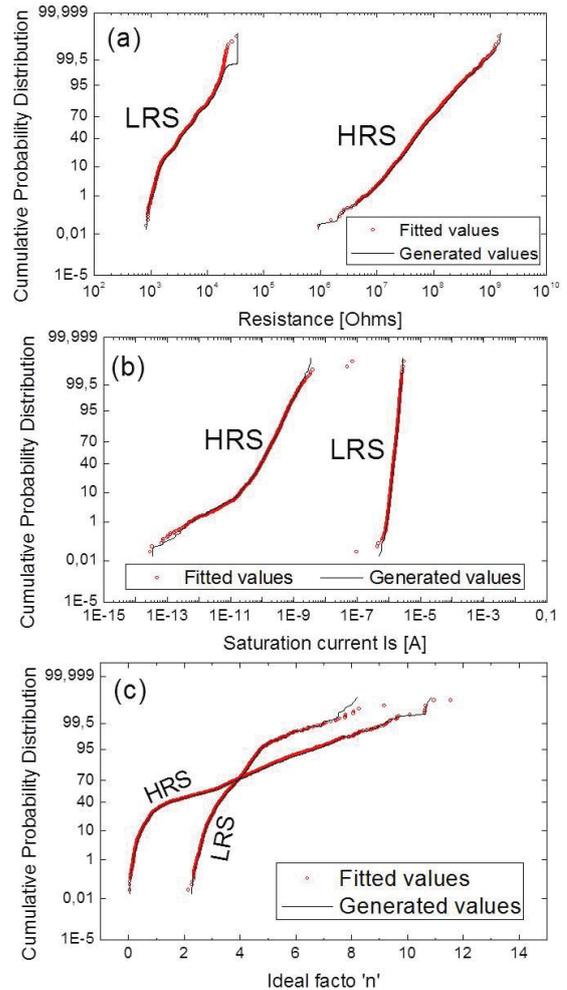


Figure 3: Statistical distributions of the circuit model parameters obtained by fitting the experimental curves (dots), a) Resistance (R), b) Saturation current (I_s) and c) Ideality factor (n) of the diode. In the HRS and LRS, two different ranges of values are obtained for R and I_s indicating a clear change of the electrical properties of the conductive filament. Line correspond to the distributions generated using the proposed method.

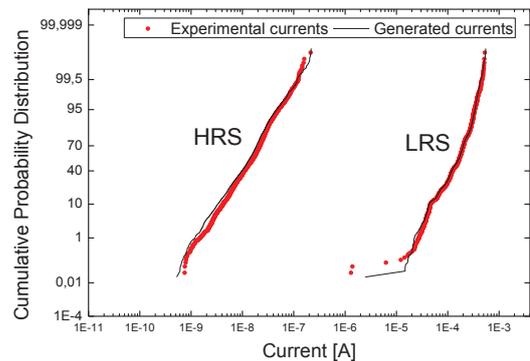


Figure 5: Cumulative probability distributions of experimental (circles) and generated (lines) LRS and HRS currents at 1V. The observed experimental variability can be properly described with the generated statistically distributed parameters sets.

Impact of the Design Layout on Threshold Voltage in SiGe Channel UTBB-FDSOI pMOSFETs

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1. Introduction

A UTBB-FDSOI (Ultra-Thin Body and Buried oxide - Fully Depleted Silicon On Insulator) technology has been developed at the 14nm node. It highlights a -34% delay (or +50% frequency) improvement along with a 100mV supply voltage reduction (0.8V vs. 0.9V) over the 28nm FDSOI technology [1]. This performance is mainly achieved thanks to the introduction of a high-k metal gate first, a 6nm thin SiGe channel and SiGe sources/drains in pMOSFETs. Even if some literature papers already evidenced layout effects induced by such a global stressor [2,3,4], no exhaustive study was reported up to now about the impact of design layouts on the electrical characteristics, whatever the shape of the active area.

For this purpose, we have extracted the threshold voltage (V_{th}) of transistors down to $L_g=20\text{nm}$ gate length as a function of several layout parameters. The length and shape of the active region, as well as the number of gate fingers have been investigated. We have developed an analytical model based on the physical mechanical behavior, which reproduces accurately the experimental data.

2. Active extension lengths

First, we have studied the effect of the active extension lengths, i.e. the gate-to-STI distances on active, called SA and SB (Figure 1 (a)). The V_{th} for both nMOS (Figure 2) and pMOS (Figure 3) have been extracted at a given current and here in the case of a symmetric layout (SA=SB). The threshold voltage of nMOS devices does not depend on SA/SB, evidencing that the channel of nMOS devices is not stressed, especially by the STI. On the other hand, the pMOS V_{th} strongly increases with the reduction of the active length, suggesting a modification of the stress in the channel of the transistor. For long and large devices, the stress is compressive biaxial, whereas it becomes highly uniaxial for short SA/SB [2]. This change of stress configuration leads to a V_{th} increase (of 88mV from SA=SB=980nm to SA=SB=80nm). We have also extracted the V_{th} for dissymmetric layouts (SA \neq SB). Figure 4 shows a similar trend for SA \neq SB as on Figure 3 for SA=SB. It demonstrates that V_{th} is directly limited by the shorter gate-to-STI distance, which is the minimum of SA, SB, in agreement with mechanical simulations.

In order to establish a model of V_{th} variation with layout, we use the stress model proposed by [5] (Eq. 1 and Figure 5). V_{th} is then derived from stress, using a first order linear longitudinal stress sensibility of $S=-113\text{mV/GPa}$, extracted from our measurements (Eq. 2). The stress value of interest is taken at the middle of the channel ($x=SA+L_g/2$), which is a relevant approximation for short channels ($L_g=20\text{nm}$). As shown in Figure 3 and Figure 4, our model well reproduces the experimental data for both symmetric and dissymmetric layouts.

3. Non-rectangular active area

Non-rectangular active areas have also been studied in symmetric or non-symmetric layouts (Figure 1 (b)). In these cases, the extension length in the X direction differs along the channel width (i.e. along the Y direction). The transistor can thus be modelled by 2 sub-transistors (T1 and T2) in parallel, whose SA/SB and width (W) are different (SA1, SB1, SA2, SB2, W1, W2). In this so-called “2-transistor model”, the weight of each sub-transistor in the total conduction is directly linked to the so-called width ratio ($W_i/(W_1+W_2)$). This model does not take into account any shear stress at T1/T2 transition. Under the assumption that V_{th} is extracted in the subthreshold regime and the subthreshold swing (SS) is independent of the stress, V_{th} can be modelled by the Equation 3.

Another approach can be used in order to get simple netlists extracted after the Layout Versus Schematics (LVS). It consists in the extraction of only one transistor of equivalent SA and SB calculated by a Matthiessen’s law (“1-transistor model”, Eq. 4). Figure 6 compares both model approaches. The “2-transistor model” allows reproducing the layout dependence with good accuracy whereas the “1-transistor” model could be a good tradeoff between model predictability and time/complexity of SPICE (Figure 7 and Figure 8).

4. Multifinger transistors

However, in a design, transistors can be built on a same active area. Especially, multifinger MOSFETs consist of different transistors in parallel and on the same active region (Figure 9). Each elementary transistor is not the same because of different extension lengths. Similar methodology as in §3 is used to model the V_{th} (Eq. 5) and well reproduces experimental data (Figure 10). This figure shows that the transistor closest to the STI impacts the V_{th} of the whole structure.

5. Conclusion

The threshold voltage of SiGe short channel FDSOI pMOSFETs with different layout parameters (active area length, shape and number of fingers) have been deeply characterized and analytically modelled. This analysis confirms the need to properly model the layout effects in order to accurately predict/assess circuit performance.

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7. Acknowledgements

This work was partly supported by the Catrene Dynamic-ULP, Places2be KETs and Nano2017 projects, through the French ministry of Industry.

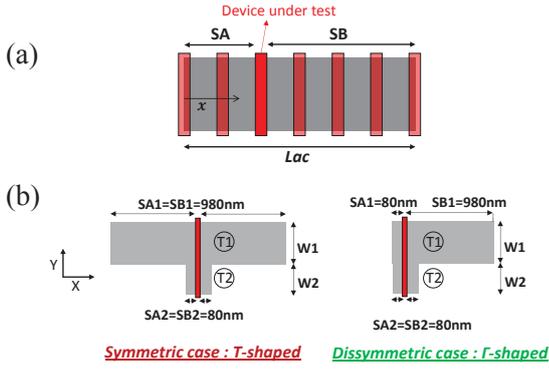


Figure 1. (a) Typical layout of tested devices. SA and SB are the distances between the gate and the active area edge on the left and right sides, respectively. (b) Scheme of non-rectangular layouts. Symmetric case (T-shaped) on the left and dissymmetric case (Γ -shaped) on the right.

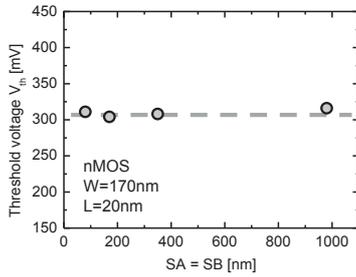


Figure 2. Threshold voltage of nMOS device as a function of SA=SB. No change of V_{th} is observed since nMOS active is made of unstrained Si.

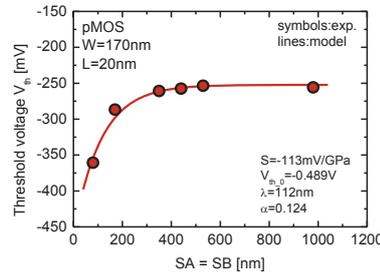


Figure 3. Threshold voltage of pMOS device as a function of SA=SB. The threshold voltage is strongly impacted by the reduction of active length.

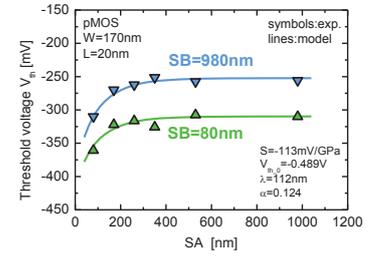


Figure 4. Threshold voltage variation vs. extension length for dissymmetric layouts (SA \neq SB). SB value is fixed at either 980nm or 80nm. The V_{th} value is limited by the shortest extension length.

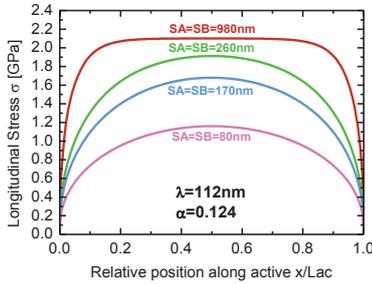


Figure 5. Stress value along the active position from the model of Eq. (1) with $\lambda=112\text{nm}$ and $\alpha=0.124$.

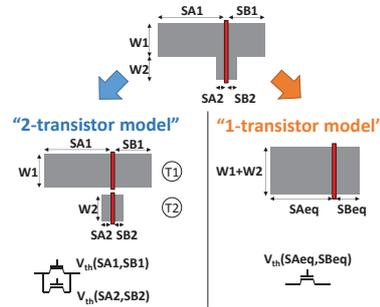


Figure 6. Illustration of the 2 approaches, the “2-transistor” and “1-transistor” models.

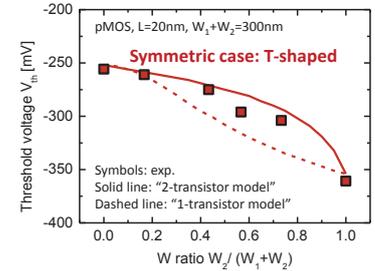


Figure 7. Threshold voltage vs. the width ratio of transistor 2 in the case of symmetric non-rectangular active (Γ -shaped). Experimental data are compared with the “2-transistor” and “1-transistor” models.

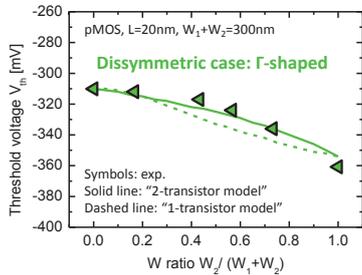


Figure 8. Threshold voltage vs. the width ratio of transistor 2 in the case of dissymmetric non-rectangular active (Γ -shaped). Experimental data are compared with “2-transistor” and “1-transistor” models.

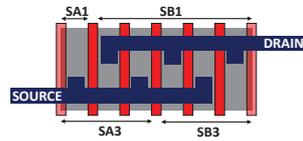


Figure 9. Illustration of multifinger transistors layout built in parallel (in this example, $N=5$).

Multifinger model (transistors in parallel)

$$V_{th}(N) = -SS \ln \left[\frac{1}{N} \sum_{i=1}^N \exp \left(-\frac{V_{th}(SA_i, SB_i)}{SS} \right) \right] \quad (5)$$

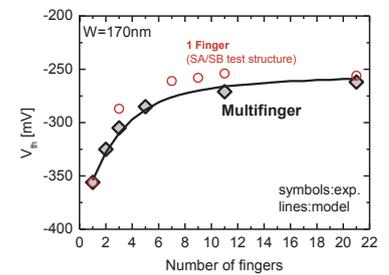


Figure 10. Threshold voltage of multifinger pMOSFETs as a function of the number of fingers. The transistor closest to the STI impacts the V_{th} of the whole structure.

Stress model

$$\sigma(x, Lac) = \sigma_0 \left[\frac{1}{2} \left(\left(1 - \exp \left(-\frac{x}{\lambda} \right) \right)^\alpha + \left(1 - \exp \left(\frac{Lac - x}{\lambda} \right) \right)^\alpha \right) \right]^{1/\alpha} \quad (1)$$

$\sigma_0=2.1\text{GPa}$ is the initial level of stress from $\text{Si}_{0.75}\text{Ge}_{0.25}$ channel and $\text{Si}_{0.7}\text{Ge}_{0.3}\text{:B}$ S/D

x the position along the active length Lac .

Threshold voltage model

$$V_{th}(SA, SB) = V_{th0} + S \cdot \sigma \left[\frac{1}{2} \left(\left(1 - \exp \left(-\frac{SA + Lg/2}{\lambda} \right) \right)^\alpha + \left(1 - \exp \left(\frac{SB + Lg/2}{\lambda} \right) \right)^\alpha \right) \right]^{1/\alpha} \quad (2)$$

“2-transistor model”

$$V_{th} = -SS \ln \left[\frac{W_1}{W_1 + W_2} \exp \left(-\frac{V_{th1}}{SS} \right) + \frac{W_2}{W_1 + W_2} \exp \left(-\frac{V_{th2}}{SS} \right) \right] \quad (3)$$

“1-transistor model”

$$SA_{eq} = \left(\frac{W_1}{W_1 + W_2} \frac{1}{SA_1} + \frac{W_2}{W_1 + W_2} \frac{1}{SA_2} \right)^{-1} \quad (4)$$

V_{th1} and V_{th2} are the threshold voltages of the transistors T1 and T2 with layout parameters SA1, SB1, W1 and SA2, SB2, W2, respectively (cf **Ошибка! Источник ссылки не найден.**)

Drain Current Local Variability from Linear to Saturation Region in 28nm Bulk NMOSFETs

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1. Introduction

A crucial issue in MOSFETs and especially in advanced nano-scaled devices is the study of drain current local variability or mismatch. The phenomenon of the source – drain (SD) series resistance mismatch was investigated in a previous work performed on FDSOI devices [1]. Indeed, it has been shown that there is a noticeable difference in the drain current mismatch, $\Delta I_D/I_D$, (Eq. 1) behavior between the small and large area devices. In the same work an expression including the SD series resistance mismatch impact was proposed for the calculation of the drain current mismatch. In this work, we studied this phenomenon on bulk NMOS transistors processed with 28nm Gate-first technology and extended the drain current local variability model to the saturation region as well.

2. Experimental

The devices measured in this work are bulk n-MOS transistors, issued from 28nm planar CMOS technology with channel width (W) varying from 10 down to 0.08 μm and channel length (L) varying from 5 down to 0.03 μm . The devices are fabricated by STM in France and present also pocket implants. A sample of 65 pairs of identical MOS transistors spaced by the minimum allowed distance and laid out in an identical environment, was necessary for matching measurements. Drain current measurements both at linear ($V_D = 30\text{mV}$) and saturation region ($V_D = 1\text{V}$) were performed with Agilent B1500 Semiconductor Device Analyzer.

3. Results

The results obtained from linear and saturation region are presented in the figures below. In Figs. 1(a) and (b) the normalized standard deviation of the drain current mismatch, $\sigma(\Delta I_D/I_D)$, is plotted as a function of the gate voltage for various geometries at the linear and saturation region, respectively. Note that, at low drain voltage, there are clearly cases at strong inversion where an increase of $\sigma(\Delta I_D/I_D)$ with V_G is observed. This increase, which is not observed in all geometries, was attributed to SD series resistance variability in FDSOI devices [1]. Therefore, it appears that this phenomenon also exists in bulk devices. On the other hand, we observe that, for the same geometries, no such behavior is clearly observed at saturation region (see Fig. 1(b)). In order to interpret these results, we extended the model described in [1] so that the saturation region can be included in the calculation of the drain current mismatch (see Eq. 2). As a result, we used Eq. 2 to fit the experimental data with 3 fitting parameters, the threshold voltage mismatch, $\sigma\Delta V_t$, the current gain factor mismatch, $\sigma\Delta\beta/\beta$ and the R_{SD} mismatch, $\sigma\Delta R_{SD}$, in all operation regions. The value of R_{SD} was extracted using the Y-Function method using several gate lengths [2]. The results are displayed in Fig. 3(a). Concerning the saturation region, we extracted nearly the same values for

$\sigma\Delta V_t$ and $\sigma\Delta\beta/\beta$, consistently with those of the linear region. As it is shown in Fig. 3(b) we achieved a good agreement between the experiment and the model. This indicates that the influence of ΔR_{SD} can be significantly attenuated in saturation region. This feature can be understood through the last term of Eq. 2, which is related to the drain current sensitivity to ΔR_{SD} and which indicates that I_D is at least twice less sensitive to R_{SD} in saturation, where $g_D=0$. This observation is confirmed in Figs. 5 (a) and (b) where the individual matching parameter $iA\Delta V_g(V_G)$ (Eq. 3) is presented for various geometries at the linear and saturation region, respectively. The plateau at low gate voltages nearly corresponds to the individual matching parameter $iA_{\Delta V_t}$ (Eq. 4). As we can see in more detail in Fig. 6, $\sigma\Delta V_t$ has almost the same value for both linear and saturation region. The difference observed between the two regions at high V_G values is because of the $\sigma\Delta R_{SD}$ difference, while the slight increase of $iA_{\Delta V_g}$ at strong inversion is due to $\sigma\Delta\beta/\beta$. From Fig.6 it is also clear that the parameter $iA_{\Delta V_g}$ is smaller at $V_D=1\text{V}$ since there is less ΔR_{SD} impact in saturation (Eq. 2). Note that this investigation was also verified by simulations (Figs. 2 & 4). Figs. 7 and 8 present the individual matching parameters $iA_{\Delta V_t}$ and $iA_{\Delta\beta/\beta}$ respectively, as a function of the gate length (Eqs 4 & 5). The values corresponding to the $iA_{\Delta V_t}$ parameter are ranging between 2 and 6.5 $\text{mV}\cdot\mu\text{m}$, in agreement with [3] and they increase slightly with the gate length. Moreover, $iA_{\Delta\beta/\beta}$ ranges from 0.4 to 0.6 $\%.\mu\text{m}$ verifying that our fitting with the gain factor mismatch was correctly done. Last but not least, the standard deviation of the SD series resistance mismatch versus the channel width is presented in Fig. 9. As can be seen, the R_{SD} and the $\sigma\Delta R_{SD}$ follow the same trend and more specifically their values decrease as the channel width increases. Furthermore, a dependence on the gate length is observed at fixed width. Finally, it was found that the normalized series resistance local variability, $\sigma\Delta R_{SD}/R_{SD}$, is around 5-15%, which is similar to FDSOI technologies [1].

4. Conclusion

The impact of the SD series resistance mismatch on the drain current variability has been investigated for 28nm Bulk MOSFETs. A mismatch model that takes into consideration the $\sigma\Delta R_{SD}$ effect was developed and used to extract all mismatch parameters, including $\sigma\Delta V_t$, $\sigma\Delta\beta/\beta$ and $\sigma\Delta R_{SD}$, in linear and saturation regions. This phenomenon was proved to be reduced in saturation region for high drain voltage values, due to lower drain current sensitivity to series resistance variation. Finally, as in FDSOI devices, the SD series resistance mismatch, $\sigma\Delta R_{SD}$, was found to scale down with gate width as R_{SD} , and the normalized series resistance local variability parameter $\sigma\Delta R_{SD}/R_{SD}$ takes similar values, demonstrating very good access resistance control in bulk technology.

$$\Delta I_D / I_D = \ln(I_{D2} / I_{D1}) \quad (1), \quad \sigma^2 \left(\frac{\Delta I_D}{I_D} \right) = \left(\frac{g_m}{I_D} \right)^2 \cdot \sigma^2(\Delta V_t) + \left((1 - g_D \cdot R_{SD})^2 \right) \cdot \sigma^2 \left(\frac{\Delta \beta}{\beta} \right) + (g_m / 2 + g_d)^2 \cdot \sigma^2(\Delta R_{SD}) \quad (2)$$

$$iA \Delta V_G = \left[\sigma \left(\frac{\Delta I_D}{I_D} \right) / \left(\frac{g_m}{I_D} \right) \right] \cdot \sqrt{W \cdot L} \quad (3), \quad iA \Delta V_t = \sigma(\Delta V_t) \cdot \sqrt{W \cdot L} \quad (4), \quad iA \left(\frac{\Delta \beta}{\beta} \right) = \sigma \left(\frac{\Delta \beta}{\beta} \right) \cdot \sqrt{W \cdot L} \quad (5)$$

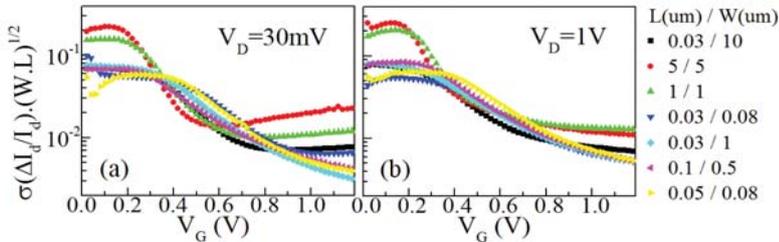


Fig. 1: Normalized standard deviation of the drain current mismatch vs V_G for different geometries in linear (a) and saturation (b) region.

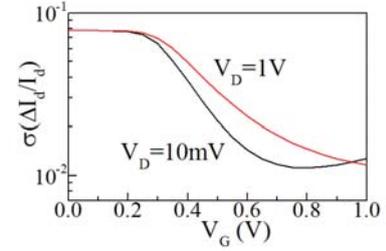


Fig. 2: Simulation results of $\sigma(\Delta I_D / I_D)$ vs V_G for nMOS devices with $L=1\mu m$ and $W=1\mu m$.

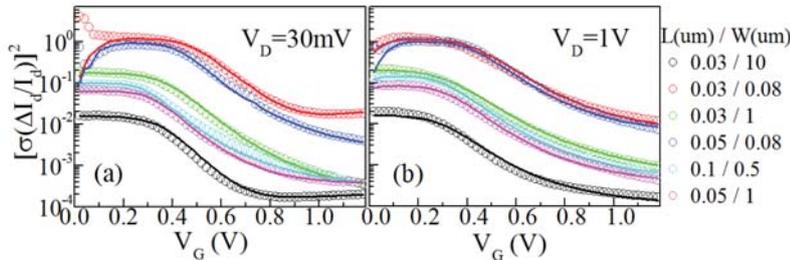


Fig. 3: Experimental results (symbols) of $\sigma^2(\Delta I_D / I_D)$ vs V_G for small and large area devices in linear (a) and saturation (b) region (symbols) and Model (lines).

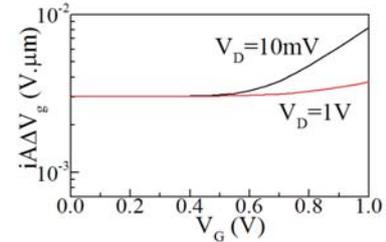


Fig. 4: Simulation results of parameter $iA \Delta V_g$ vs V_G for nMOS with $L=1\mu m$ and $W=1\mu m$.

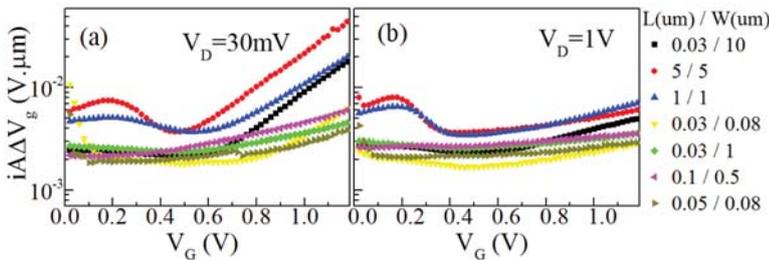


Fig. 5: Individual matching parameter $iA \Delta V_g$ vs V_G extracted by experimental data in linear (a) and saturation region (b) for different geometries.

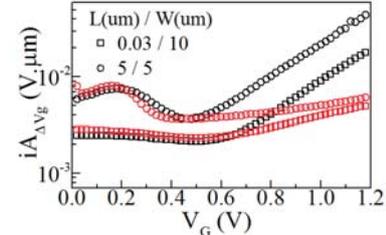


Fig. 6: Individual matching parameter $iA \Delta V_g$ vs V_G in linear (black symbols) and saturation region (red symbols).

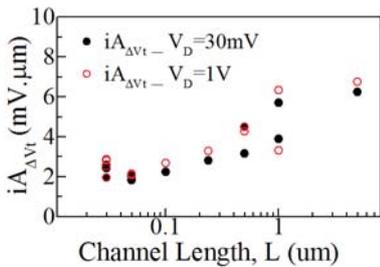


Fig. 7: $iA \Delta V_t$ vs channel length in linear (black symbols) and saturation region (red symbols) for 28nm BULK nMOSFETs.

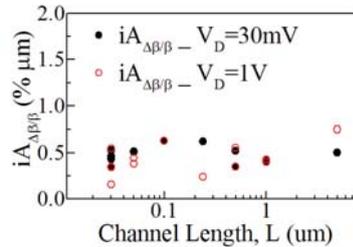


Fig. 8: $iA \Delta \beta$ vs channel length in linear (black symbols) and saturation region (red symbols) for 28nm BULK nMOSFETs.

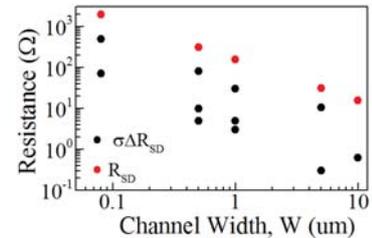


Fig. 9: SD series resistance (red symbols) and its mismatch (black symbols) vs channel width for 28nm BULK nMOSFETs.

Investigation of BSIM4 Parameter Extraction and Characterization for Multi Gate Oxide-Dual Work Function (MGO-DWF)-MOSFET

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1. Introduction

Dual Work Function (DWF)-FETs have been proposed [1,2,3] for RF/analog circuit applications, which show a larger transconductance (g_m) and a smaller drain conductance (g_d) because of work function (WF) difference in the gate electrode. We fabricated Multi Gate Oxide (MGO)-DWF-FET with LV-MOSFET in the source side region and HV-MOSFET in the drain side region and enhancement of F_{MAX} was observed in the scaled devices [4]. As for SPICE modeling, conventional MOSFET models cannot be used straightforwardly for MGO-DWF-FET due to the asymmetric source/drain (S/D) structures. In this study, we investigated BSIM4 based DC and capacitance model parameter extraction procedure for MGO-DWF-FET with different geometries on the basis of the measurement data.

2. Device Structure and Characteristics

We fabricated MGO-DWF-FET by using Toshiba's 65nm CMOS technology. Fig. 1 shows the schematic device structure and cross sectional TEM image. Gate oxide thickness of source side gate ($t_{ox,S}$) was thinner than that of drain side gate ($t_{ox,D}$), and asymmetric S/D extension was formed. Fig. 2(a) shows the measured I_d-V_g and g_m-V_g curves of n -channel MGO-DWF-FET with drain side gate length ($L_{G,D}$) of 170nm and source side gate length ($L_{G,S}$) of 30nm. Higher g_m was obtained for shorter $L_{G,D}$ devices, as shown in Fig. 2 (b). Fig. 3 shows $L_{G,D}$ dependence on drain induced barrier lowering (DIBL). Short channel effect (SCE) immunity was guaranteed to the channel length of 200nm, which corresponds to the results obtained from in-house 2D device simulation of Fig. 4.

3. DC Parameter Extraction

We applied BSIM4.6.0 [5] in order to extract the model parameter from the measurement data of MGO-DWF-FET. SPICE modeling tool, UTMOST IV [6], was used. The targeted device geometries for parameter extraction are $(L_{G,D}, L_{G,S})=(530, 30), (230, 30), (170, 30), (130, 30)$ [nm] and $W=500$ nm. P⁺ poly/SiO₂ gate stack with $t_{ox,S}=2.0$ nm and n⁺ poly/SiO₂ gate stack with $t_{ox,D}=7.4$ nm were fabricated. Before the parameter extraction, process parameter of 'L' (channel length) and 'TOXE' (gate oxide thickness) were carefully derived. Although the total channel length is a sum of $L_{G,D}$ and $L_{G,S}$, 'L' was set to be $L_{G,D}$ in this study. 'TOXE' was extracted from the maximum capacitance (C_{max}) with gate area defined by $L_{G,D} \cdot W$. As shown in Fig.5, although the total channel length is a constant value of $L_{G,S}+L_{G,D}=100$ nm for all devices, C_{max} has the $L_{G,D}$ dependence because inversion area under n⁺ gate was determined by $L_{G,D} \cdot W$. Therefore, since 'TOXE'

has the $L_{G,D}$ dependence, multiple DC parameter sets for various $L_{G,D}$ down to 130nm were obtained for n -type MGO-DWF-FET. In I_d-V_g optimization procedure, initial value of 'VTH0' was obtained from the measurement data of $L_{G,D}=500$ nm. In I_d-V_d optimization procedure, parasitic resistance (R_{sd}) was simply determined from $R_{on}-L_{G,D}$ plot in the long channel regime, as shown in Fig. 6. R_{sd} can be obtained from the y-axis intercept of the observed straight line. When 'L', 'TOXE', 'VTH0' and R_{sd} were determined, local optimization strategies and rubberband method were used for parameter extraction. Fig. 7 shows the typical results of the measured and simulated g_m-V_g , I_d-V_g and I_d-V_d curves. The behavior in g_m curves and smaller g_d characteristics were optimized to match the characteristics of MGO-DWF-FET. Good fitting with maximum error < 5% for the targeted voltage range was achieved for n -channel MGO-DWF-FET with sub-200nm gate length.

4. Parasitic Capacitance Characterization

Figure 8 shows simulated capacitance-voltage (CV) characteristics of MGO-DWF-FET. Since a capacitance coupling between the gate electrode and the drain side inversion layer, which indicates an increase of parasitic capacitance (C_{para}) in the drain side, was observed when V_g is applied, a total gate capacitance was observed before the transistor is turning on. This trend corresponds to the result obtained from measurement data (Fig. 9). $C_{gd}-V_g$ characteristics also have V_d dependence, as shown in Fig.8 (b). Therefore, we used a bias-dependent C_{para} model of BSIM4. When 'CAPMOD=1' had been selected, it was found that 'CGDO', 'CDGL' and 'CKAPPAD' were useful parameter to optimize the CV characteristics (Fig.10). In particular, 'CDGL' and 'CKAPPAD', which have bias-dependent in order to treat LDD structure for conventional MOSFET, show the C_{para} reduction at the low- V_g and V_d region.

5. Conclusion

SPICE model parameters of BSIM4 were successfully extracted for MGO-DWF-FET by using UTMOST IV. 'L' was set to be $L_{G,D}$ and 'TOXE' were carefully derived from the maximum capacitance with $L_{G,D}$ dependence. Parameter sets for $L_{G,D}$ down to 130nm were obtained, as long as process parameter are well defined. Larger g_m , smaller g_d , and C_{para} in the drain side can be observed on the extracted parameter. The extracted parameters will be a useful tool for characterizing the circuit performance of MGO-DWF-FET. Furthermore, our extraction procedure is applicable to extract the BSIM4 model parameters for MGO-DWF-FET as well as other structures (e.g. SOI, double gate) and materials (e.g. high-k) for MGO-DWF-FET.

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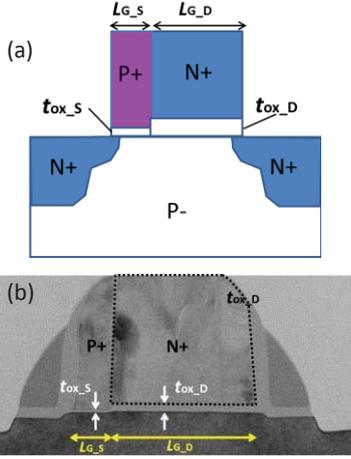


Fig.1 (a)Schematic device structure and (b)cross sectional TEM image of MGO-DWF-FET.

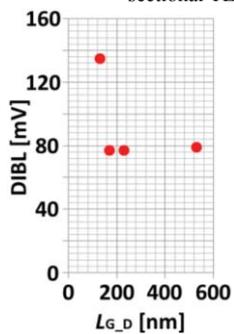


Fig.3 Measured $L_{G,D}$ dependence on DIBL. $L_{G,D}=170\text{nm}$, $L_{G,S}=30\text{nm}$, $W=500\text{nm}$. SCE immunity was guaranteed to the channel length of 200nm.

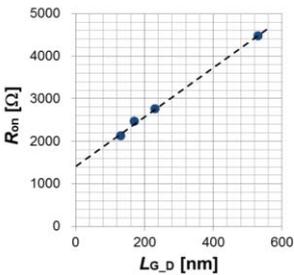


Fig.6 R_{sd} was determined from measured $R_{on}-L_{G,D}$ plot with $W=500\text{nm}$, $L_{G,S}=30\text{nm}$. R_{sd} can be obtained from the y-axis intercept of the observed straight line.

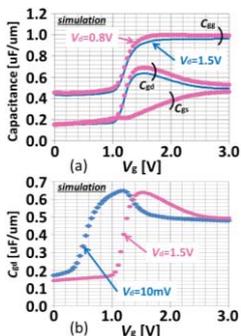


Fig.8: (a) Simulated gate capacitance (C_{gg}), gate-to-drain capacitance (C_{gd}) and gate-to-source capacitance (C_{gs}) curves with high V_d and (b) V_d dependence on C_{gd} . Unlike MOSFET, only C_{gd} was increased when V_g is applied.

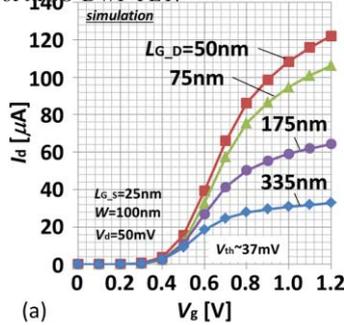


Fig.4 Simulated (a) I_d-V_g at liner region and (b) DIBL characteristics with $W=100\text{nm}$, $L_{G,S}=25\text{nm}$. In this simulation, gate work function difference was a constant condition for all devices.

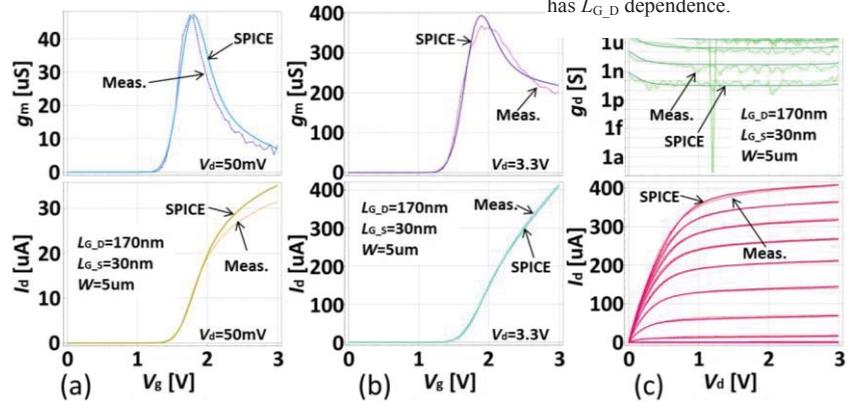


Fig.7 Typical optimization results for (a) g_m-V_g and I_d-V_g curves with $V_d=50\text{mV}$ (liner), (b) g_m-V_g and I_d-V_g curves with $V_d=3.3\text{V}$ (saturation) and (c) g_d-V_g and I_d-V_d curves. SPICE simulation was performed by using extracted parameter. Good fitting with maximum error $< 5\%$ for targeted voltage range was achieved for n -channel MGO-DWF-FET.

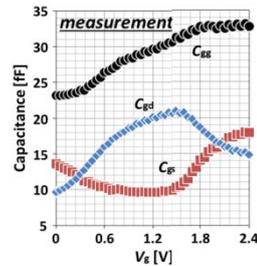


Fig.9

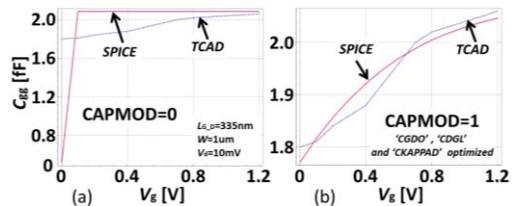


Fig.10 TCAD and SPICE simulation results for C_{gg} characteristics. (a) "CAPMOD=0" and (b) "CAPMOD=1". "CGDO", "CDGL" and "CKAPPAD" were useful parameter to optimize the CV characteristics. When "CAPMOD=1", optimized CV was obtained.

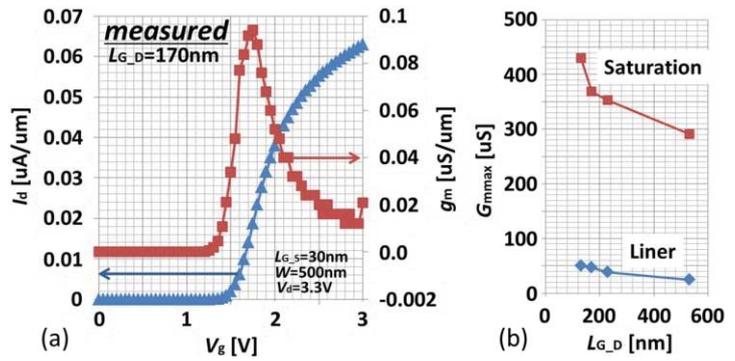


Fig.2 (a) Measured I_d-V_g and g_m-V_g characteristics of n -channel MGO-DWF-FET with $L_{G,D}=170\text{nm}$, $L_{G,S}=30\text{nm}$ and $W=500\text{nm}$. $V_d=3.3\text{V}$. (b) Extracted $L_{G,D}$

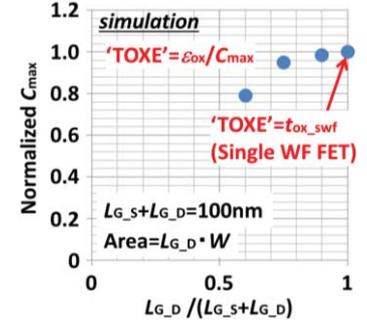


Fig.5 Normalized C_{max} extracted from simulated CV curves. The device with the data for $L_{G,D}/(L_{G,S}+L_{G,D})=1$ shows single work function MOSFET. C_{max} has $L_{G,D}$ dependence.

Confinement Orientation Effects in S/D Tunneling

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1. Introduction

The study of alternative technical approaches for electronic devices is necessary to fulfill the requirements of power consumption, delay time and scalability demanded by ITRS [1]. On the one hand, the inclusion of quantum effects in the transport description is mandatory when the dimensions of the electronic devices are reduced. In particular, Source-to-Drain tunneling (S/D tunneling) allows electrons go from the source to the drain through the potential barrier. This phenomenon is presented as a scaling limit since it increases the subthreshold current [2]. On the other hand, new transistor architectures are considered to replace standard technology. The addition of multiple gates surrounding the channel reduces the short-channel effects. If we consider a double gate device on standard wafers, the planar version, Double-Gate Silicon-On-Insulator (DGSOI), is a (100) device and the vertical one, FinFET, corresponds to the (110). This work presents a meticulous comparison between DGSOI and FinFET by means of Monte Carlo simulations when S/D tunneling mechanism is taken into account. It will be shown the influence of the orientation on the S/D tunneling and, consequently, on the device characteristics.

2. Simulation and Results

The model presented in this work is included in a Multi-Subband Ensemble Monte Carlo (MS-EMC) simulator which has already demonstrated its capabilities studying different advanced nanodevices [3-4]. This simulator is based on the quantum transport mode-space approximation [5] where the 1D Schrödinger equation is solved in the confinement direction and the 2D Boltzmann Transport Equation is solved in the transport plane as shown in Fig.1. The main advantage of this approach is its reasonable computational effort, even when scattering and quantum mechanisms are included in a detailed way.

The considered orientation of both devices changes between (100) for planar DGSOI and (0-11) for FinFET as the confinement direction, whereas the transport direction remains constant $\langle 011 \rangle$. These devices have been parameterized for gate length ranging from 5nm to 20nm. The rest of the technological parameters remains constant, channel thickness $T_{si}=3\text{nm}$, gate oxide with Equivalent Oxide Thickness, $EOT=1\text{nm}$, and work function of 4.385eV. It should be highlighted that the FinFET is a 3D structure whereas our MS-EMC simulator makes use of a 2D description. However, it was demonstrated that this simulator provides a good agreement with other 3D codes when FinFETs are thoroughly analyzed [6].

This simulation approach, which is an extension for non-local band-to-band tunneling algorithm [7], is based on the free-flight technique, commonly used in EMC simulation where the position of each electron after a

flight is calculated. If S/D tunneling is considered, an electron near the potential barrier with lower energy either will rebound from the potential barrier or will go through it. The tunneling probability is calculated by the WKB approximation:

$$T_{dt}(E) = \exp\left\{-\frac{2}{\hbar} \int_a^b \sqrt{2m_{tr}^*(E_i(x) - E)} dx\right\} \quad (1)$$

where a and b are the starting and ending points, E and m_{tr}^* are the energy and transport effective mass of the electron, respectively, and $E_i(x)$ the energy of the i -th subband. A rejection technique is used to determine whether the particle will tunnel or not. A uniform distributed random number r_{dt} is generated and compared to T_{dt} . On the one hand, if $r_{dt} > T_{dt}$, the electron will turn back. On the other hand, if $r_{dt} \leq T_{dt}$, the electron will go through the barrier. The motion inside the barrier obeys Newton mechanics considering an inverted potential profile and ballistic transport [8].

The inclusion of this effect has an important impact on I_D - V_{GS} characteristics for both DGSOI and FinFET (Fig.2). The differences in the confinement direction modify the distribution of the electrons in the subbands and, consequently, the potential profile. Also, the carrier transport effective mass is modified. Thus, in this study, m_{tr}^* is higher for the FinFET orientation than for the DGSOI orientation. As a result of these changes, T_{dt} is higher for DGSOI than for FinFET. This quantum effect produces a noticeable modification of the I_D - V_{GS} characteristic (Fig.2). As it is shown, the influence of the S/D tunneling is lower in the FinFET (Fig.2a) compared to DGSOI (Fig.2b). Due to the rejection technique explained before, higher T_{dt} implies higher probability of an electron suffering S/D tunneling. For this reason, the number of particles affected by S/D tunneling is higher for DGSOI than for FinFET (Fig.4). The same effect is also shown in Fig.3 where the impact of the S/D tunneling on the threshold voltage (ΔV_{th}) is estimated for both, the DGSOI and the FinFET. This effect is exacerbated as the dimensions of the device are reduced. The percentage of electrons affected by S/D tunneling near the potential barrier is lower for FinFET (Fig.5a) than for DGSOI (Fig.5b). In addition, there is a maximum of this percentage for the FinFET due to a reduced height of the potential barrier. Consequently, the number of electrons near the potential barrier with lower energy is also reduced. By way of contrast, this maximum percentage is shifted to higher gate voltages in DGSOI (not shown). In conclusion, our simulations show important differences fully caused by the change in the confinement directions in both DGSOI and FinFET when S/D tunneling is taken into account. Nevertheless, FinFET devices show less degradation in their subthreshold characteristics, and therefore are better candidates to implement future nodes, especially for ultra low power applications.

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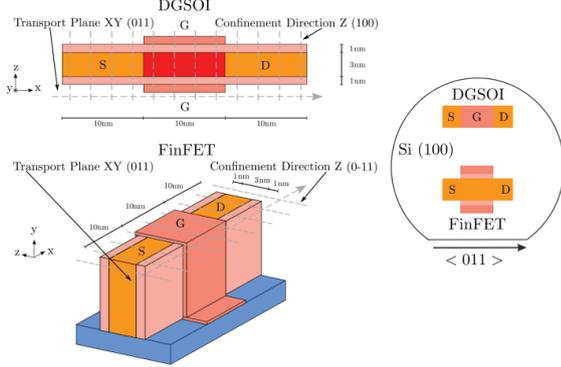


Fig.1: DGSOI and FinFET structures analyzed in this work. 1D Schrödinger equation is solved for each grid point in the transport direction and BTE is solved by the MC method in the transport plane.

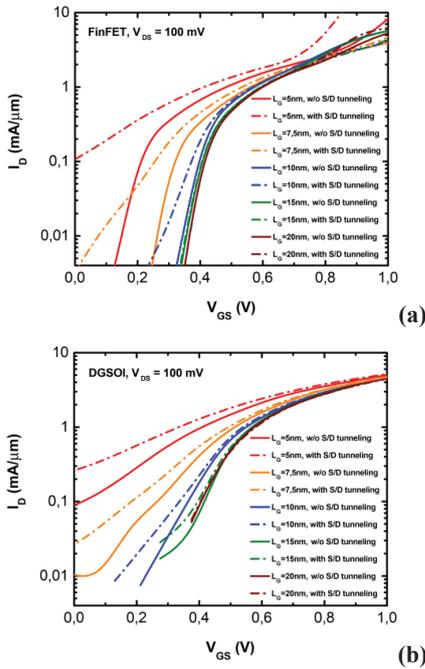


Fig.2: I_{D_S} vs. V_{G_S} as a function of L_G at low bias with and w/o considering S/D tunneling for FinFET (a) and DGSOI (b).

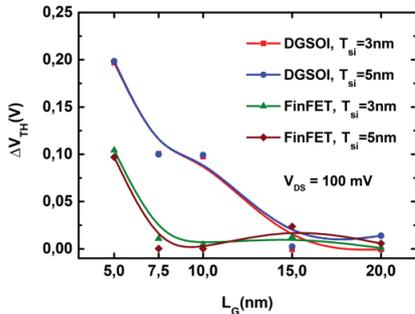


Fig.3: Difference between the threshold voltage (ΔV_{th}) of a simulation considering S/D tunneling and a simulation w/o taking it into account as a function of L_G for FinFET and DGSOI.

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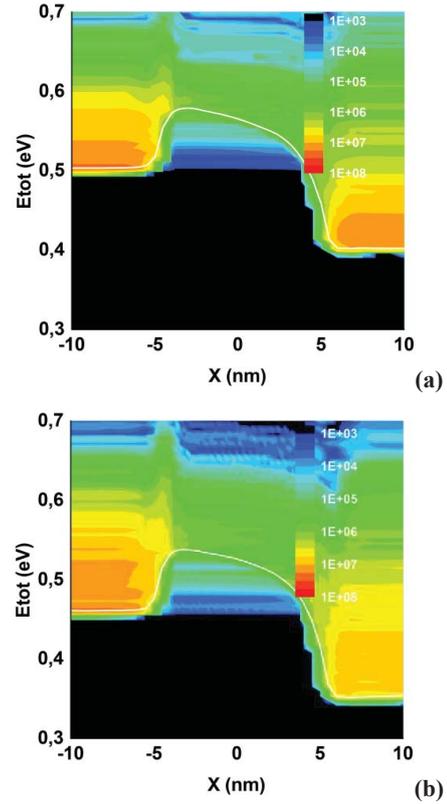


Fig.4: Electron distribution in the first subband as a function of total energy in the 10nm device including S/D tunneling for FinFET (a) and DGSOI (b) with $V_{G_S}=0.8V$ and $V_{D_S}=100mV$.

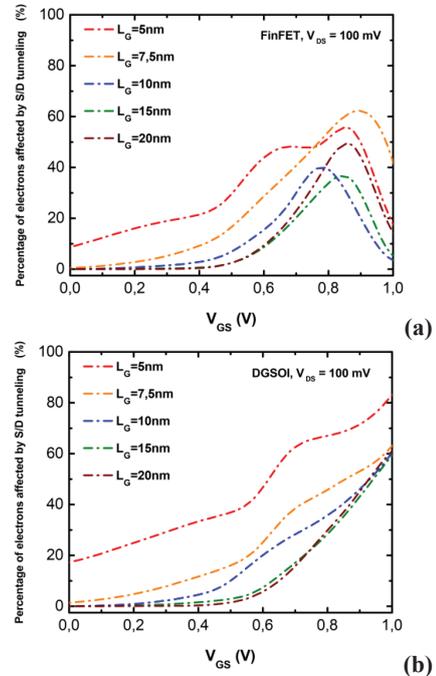


Fig.5: Percentage of electrons affected by S/D tunneling near the potential barrier as a function of L_G at low bias drain for FinFET (a) and for DGSOI (b).

Volume and Interface Conduction in InGaAs Junctionless Transistors

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Abstract – Doped InGaAs films were characterized using a revisited pseudo-MOSFET configuration. Two different conduction mechanisms were evidenced: volume and interface. The impact of film thickness, channel width and length is evaluated. Measurements at low temperatures complete the analysis.

1. Introduction

According to ITRS prediction [1], Indium-Gallium-Arsenide (InGaAs) is expected to replace silicon in n-type MOSFETs, thanks to superior electron mobility [2]. In this work, In_{0.53}Ga_{0.47}As layers transferred on oxide were characterized using a modified version of the well-known pseudo-MOSFET (Ψ -MOSFET) configuration [3]. After presenting the measurement set-up (Sec. 2), Sec. 3 shows a suitable procedure to extract the electron mobility which is further discussed in Section 4.

2. Measurement set-up

Fig. 1a shows the schematic of the tested structures. InGaAs layers with different thicknesses t_{III-V} (25 nm, 50 nm, 100 nm and 200 nm) were transferred on buried oxide (BOX composed of 10 nm Al₂O₃ over 25 nm SiO₂). The target doping of the III-V film was of $2 \cdot 10^{16} \text{ cm}^{-3}$. The technological sequence is presented elsewhere [4]. The static analysis was performed by sweeping the gate bias V_G and measuring the resulting drain current (I_D) between source and drain. Instead of the standard pressure probes of the Ψ -MOSFET, implanted metal contacts are used as source and drain. This configuration was chosen to study the material quality and avoid probe-induced defects. Fig. 1b presents the measured drain current I_D versus drain bias V_D . A linear trend is obtained, confirming the ohmic contacts between the metal and the III-V film.

Fig. 2 shows I_D (plain symbols) and associated transconductance g_m (empty symbols) versus gate bias in thick InGaAs film. A plateau is evidenced in $I_D(V_G)$ curve for $V_G \approx 0$ and double peaks appear in the $g_m(V_G)$ characteristic. These signatures are a clear evidence of double conduction mechanisms present in the III-V film. Volume conduction is possible thanks to the high doping level and is controlled by V_G via the modulation of the depletion region. Beyond flat-band voltage ($V_G > V_{FB} \approx +1.1 \text{ V}$), an accumulation channel forms at the InGaAs-BOX interface and gradually dominates the total current. The double peak tends to disappear in thinner films where the volume conduction is less pronounced.

3. Parameters extraction

Considering the doping level, the maximum depletion width [5] is $w_D \approx 197 \text{ nm}$, which means that

all films are basically fully depleted. Fig. 3 presents the measured $I_D(V_G)$ curves in devices with $t_{III-V} = 200 \text{ nm}$, same length ($L = 200 \mu\text{m}$) and different widths. Full depletion is more marked for narrow width ($W = 2.5 \mu\text{m}$), pointing on a 2D mechanism: depletion from sidewalls reinforces the vertical depletion induced by the gate.

To investigate the material quality, we used the approach proposed by Liu *et al.* [6]. In volume conduction regime, the drain current in the neutral (undepleted) region of the film can be written as:

$$I_D = \frac{W}{L} \cdot C_{BOX} \cdot \mu_{vol} \cdot V_D \cdot (V_G - V_0) \quad (1)$$

where C_{BOX} and V_0 are respectively the oxide capacitance and a characteristic voltage which enables full depletion of the channel [7]. μ_{vol} represents the volume mobility. The surface mobility μ_S at the film-BOX interface is obtained from the slope of the Y-function (Y_{fun}) in accumulation regime, after removing the contribution of the volume current I_{vol} (Fig. 4 and dashed line in Fig. 2) [7].

4. Mobility trends

The extracted μ_{vol} (Fig. 5) increases when the gate length L decreases below $100 \mu\text{m}$ for all devices tested and can exceed $1000 \text{ cm}^2/\text{Vs}$. As expected, the surface mobility (Fig. 6) is inferior. The lowest mobility is measured for $t_{III-V} = 25 \text{ nm}$, suggesting that the coupling with the top interface affects the extraction. Since charged defects exist on the free surface, the difference between the front and back surface potentials induces a vertical field, $E_{int} = (\Psi_{S1} - \Psi_{S2})/t_{III-V}$, that obviously increases in thinner films [8]. Even if the influence of the gate-induced field is removed in Y-function, the mobility is still affected by the intrinsic field. In other words, the low-field mobility is not accessible. The μ_S versus L curves obtained for thick films ($t_{III-V} = 50\text{-}200 \text{ nm}$) overlap (Fig. 6) showing less impact of the intrinsic field and comparable interface quality.

Fig. 7 presents the subthreshold swing S (plain symbols) and V_{FB} (empty symbols) for different measurement temperatures T . The device had $t_{III-V} = 25 \text{ nm}$. A strong decrease of S with temperature is found, as reported for undoped MOSFETs [5]. V_{FB} decreases for lower temperature [9].

5. Conclusions

The evidence of two conduction mechanisms (volume and interface) in InGaAs layer has been reported. Material quality was investigated for different structures (III-V thickness, device width and length) pointing out their impact on the extracted carrier mobility. Analysis at low temperature was performed to complete the study as documented in the extended paper.

Acknowledgments

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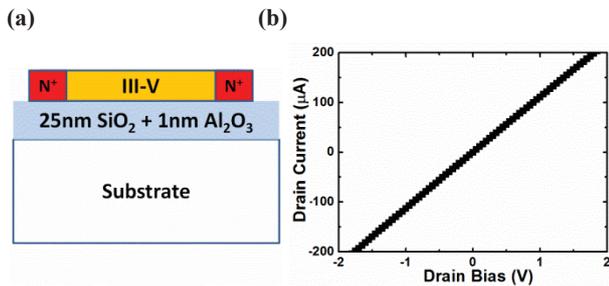


Fig. 1 : (a) Schematic view of back-biased InGaAs film on insulator, used for electrical characterization. (b) Measured I_D versus V_D .

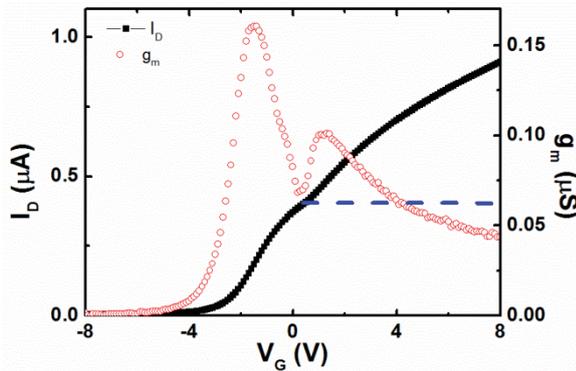


Fig. 2 : I_D (plain symbols) and g_m (empty symbols) versus gate bias. $t_{III-V} = 200 \text{ nm}$ and $W = 20 \text{ }\mu\text{m}$. The dashed line represents I_{Vol} .

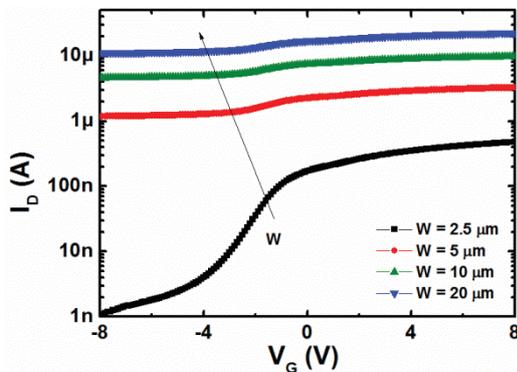


Fig. 3 : I_D versus V_G for $t_{III-V} = 200 \text{ nm}$ and $L = 200 \text{ }\mu\text{m}$. The samples had different W .

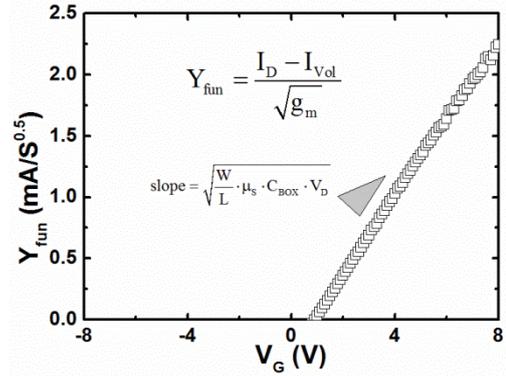


Fig. 4 : Y_{fun} as function of V_G computed from Fig. 2.

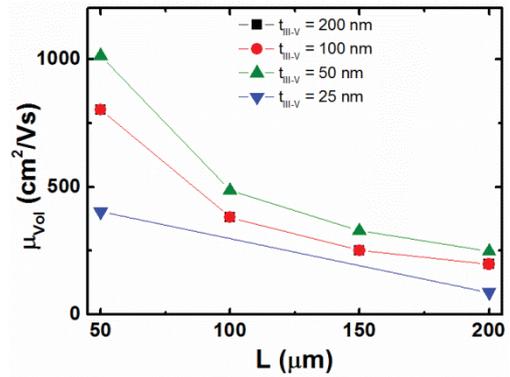


Fig. 5: μ_{Vol} (a) versus L for different t_{III-V}

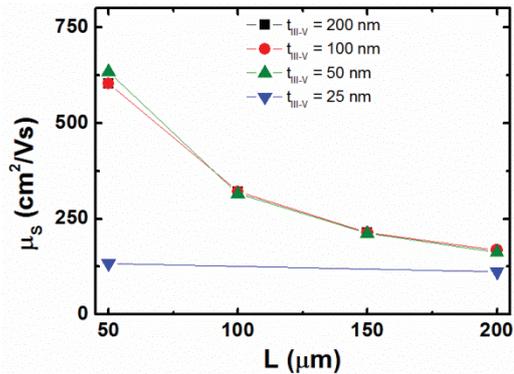


Fig. 6 : μ_S versus L for different t_{III-V} .

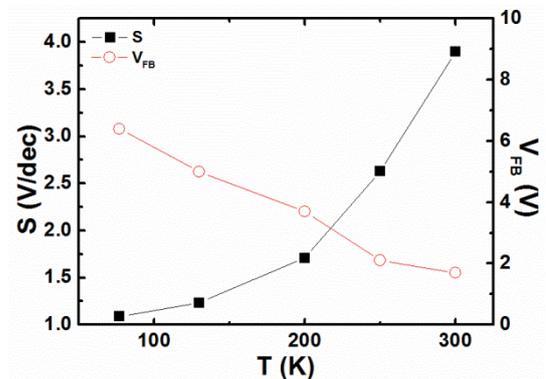


Fig. 7 : S and V_{FB} measured versus temperature T . The device had $t_{III-V} = 25 \text{ nm}$ and $W = 2.5 \text{ }\mu\text{m}$.

Effective Hole Mobility and Low-Frequency Noise Characterization of Ge pFinFETs

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Abstract

Germanium pFinFETs are evaluated from the viewpoint of effective hole mobility and low frequency noise characterization. These parameters are measured for different fin widths and backside substrate bias in order to get a better insight in the underlying scattering mechanisms. For narrow devices, it was found that the peak effective mobility and the Coulomb scattering coefficient were limited due to the charges in the gate oxide sidewalls or interface layer, resulting in similar effective mobility values for narrow and planar-like devices. On the other hand, the substrate biasing played a role only in planar-like devices, which moves the effective mobility and Coulomb scattering coefficient values toward the opposite direction.

Introduction

Many research efforts have been spent recently for alternative high-mobility materials for the channel region, regarding especially future high-performance applications, i.e., germanium (Ge) and III/V instead of silicon [1]. Ge is particularly relevant for p-channel devices thanks to the 4 times higher bulk hole mobility than Si [2]. On the other hand, there are some challenging issues that must be overcome to optimize the Ge transistor performance [2]. Apart from that, considering the fact that the main semiconductor industries have been investing in multiple gate devices, such as FinFET triple-gate (3D-transistors), [3] [4], thanks to their electrostatic improvements and short-channel effect control [5], it is very relevant evaluating the combination of a future candidate channel material with the current mainstream architecture.

Therefore, this work analyses the effective hole mobility and low frequency noise behavior for different fin widths of inversion-mode strained Ge pFinFETs, which are schematically represented in Fig. 1.

Experimental Details

The main fabrication steps are summarized in Fig. 2. The p-type strained germanium FinFET devices used in this work have been fabricated at imec/Belgium on 300 mm Si (100) wafers via the Shallow Trench Isolation (STI) first process. The main FinFET device dimensions are fin widths (W_{fin}) of 20nm; 30nm; 50nm and 100nm and geometric channel lengths (L_G) 1.03 μ m and a fin height (H_{fin}) of 20nm. The channel and n-type insitu doped relaxed buffer (Si_{1-x}Ge_x x=75%) have the doping concentration of around $1 \times 10^{17} \text{cm}^{-3}$ and $5 \times 10^{18} \text{cm}^{-3}$, respectively. The gate stack is composed by 0.7nm SiO₂, 2.5nm HfO₂ and TiN. The work is based only on experimental data, which were obtained from measurements with an HP 4146C - Semiconductor Device Parameter Analyzer, Agilent E4980 A - High frequency CV and the hardware/software systems from

ProPlusSolution for IV, CV and low frequency noise measurements, respectively.

Results and Discussion

Fig. 3 clearly reveals a W_{fin} dependency of the threshold voltage (V_T). First of all, it is a consequence of a higher leakage current underneath the channel from source to drain regions for the narrow devices. Moreover, it is associated with the negative charge in either the gate oxide or interface layer, since the V_T is shifted towards more positive values [6]. In addition, the V_T behavior is quite consistent with the frequency normalized noise Power Spectral Density (PSD), showing Lorentzian components with a V_{GS} -dependent corner frequency. This originates from V_{GS} dependent generation-recombination (GR) noise, which indicates the presence of traps in the gate dielectric, owing to a strong relation between the V_{GS} and the SHR lifetime [7].

Fig. 4 shows that the Capacitance Equivalent Thickness (CET) has a mean value around 1.5nm for the studied fin width range, taking into account five samples of the same wafer. It points out to a relative good uniformity of the gate stack dielectric for the process under evaluation.

Fig. 5 noticeably shows that the average effective hole mobility (μ_{eff}) is quite W_{fin} independent. On the other hand, the μ_{eff} should be higher for small W_{fin} compared with planar-like, since the low-field hole mobility of the FinFET <110> sidewalls is superior over the value for the top <100> plane [8] [9]. The fact that there is no W_{fin} dependence of μ_{eff} is related to a higher oxide trap density in the sidewalls, which limits the μ_{eff} for narrow devices. In addition, the dominant mobility scattering mechanism plays a role in the μ_{eff} value. In these devices, the surface roughness scattering might be dominant, since the μ_{eff} presents only a slight temperature dependence, as shown in Fig. 6.

The drain current noise power spectral density presented in Fig. 7 tells that the flicker noise ($1/f^2$) is dominant in the frequency range evaluated. Furthermore, the γ factor is around one for all W_{fin} . The observed $1/f^2$ can be modeled in terms of the carrier number and correlated mobility fluctuations [10]. From the input-referred voltage noise (S_{VG}) one can extract the Coulomb scattering coefficient (α_{SC}) and the slow oxide trap density (Nt), at flat-band voltage region [11].

Fig. 8 presents the influence of the substrate bias (V_{BS}) on α_{SC} and μ_{eff} . As the backside V_{BS} increases, the α_{SC} of the planar-like device ($W_{fin}=100\text{nm}$) decreases, demonstrating that α_{SC} is less efficient, since the distance between the interface with the gate stack and the inversion layer charge centroid becomes larger, resulting in the increase of μ_{eff} , as in planar Ge

MOSFETs [12]. On the other hand, there is no significant impact of V_{BS} on μ_{eff} and α_{SC} for narrow devices, due to the strong electrostatic coupling, which can be confirmed in Fig. 9, where the V_T for narrow devices is V_{BS} -independent for the studied channel length range.

Conclusions

An 1.5nm-CET Ge pFinFET using a conventional STI scheme was characterized and reported in this work. Instead that the effective mobility follows the expected behavior, i.e., higher for narrow devices than planar-like ones due to the higher μ_{eff} of $\langle 110 \rangle$ sidewalls, this work revealed that the μ_{eff} was limited due to the predominance of charges in the gate oxide sidewalls or interface layer, which also degraded the threshold voltage for narrow devices. Considering the low-frequency-noise behavior, it is shown that $1/f^{\gamma}$ behavior ($\gamma \sim 1$) is observed for all fin widths. Moreover, the Coulomb scattering coefficient (α_{SC}) showed to be dependent on the substrate bias (V_{BS}) only for the planar-like devices, resulting in μ_{eff} increase and α_{SC}

reduction, as a consequence of a larger distance between the interface with the gate stack and the inversion layer charge.

Acknowledgment

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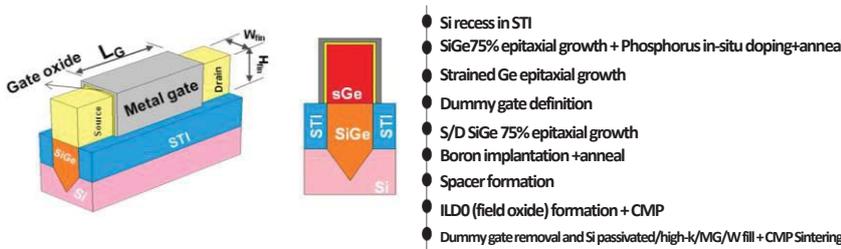


Fig. 1: Germanium FinFET structure (A), cross section in the middle of the fin (B).

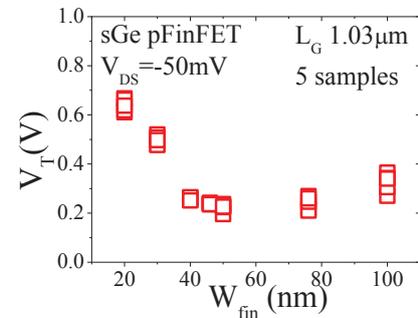


Fig. 3: Threshold voltage as a function of fin width.

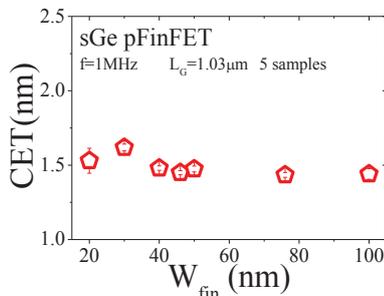


Fig. 4: Capacitance equivalent thickness as a function of fin width.

Fig. 2: Process flow description of the Ge pMOSFET studied in this work.

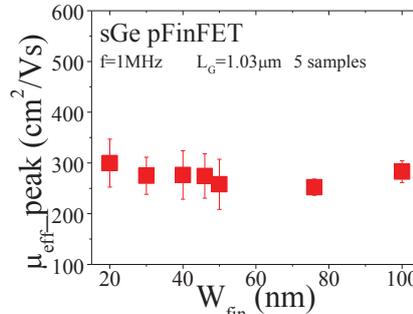


Fig. 5: Peak of effective mobility as a function of fin width.

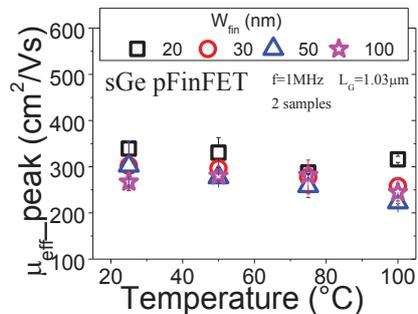


Fig. 6: Peak of effective mobility as a function of temperature for different W_{fin} .

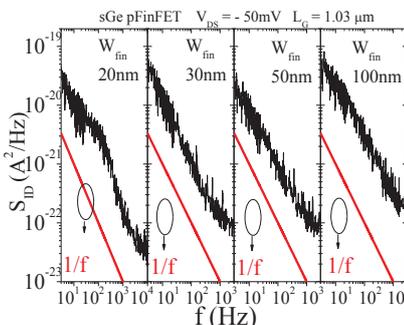


Fig. 7: Power spectral density as a function of frequency for different W_{fin} .

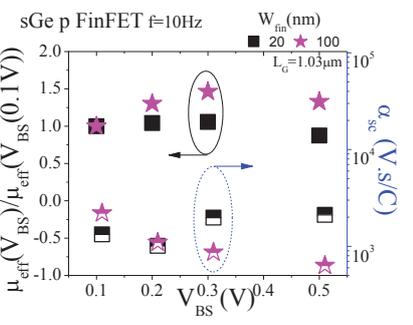


Fig. 8: Normalized effective mobility and scattering coefficient as a function of substrate bias.

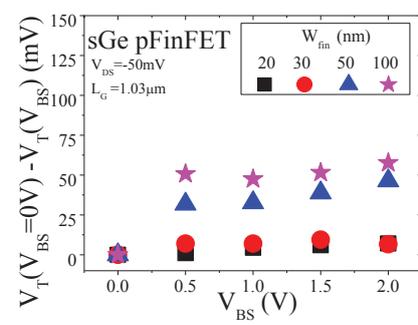


Fig. 9: Threshold voltage shift as a function of substrate voltage.

V_{DD} Scaling of Ultra-thin InAs MOSFETs: A Full-Quantum Study

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1. Introduction

High-mobility III-V compounds are nowadays extensively investigated as channel materials to replace Si and SiGe with the aim to fulfill the ITRS requirements for the sub-10nm technological nodes [1]. Recently, promising results have been reported in terms of ON-current (I_{ON}) and DIBL for InAs thin layer [2, 3]. By means of full-quantum simulations we analyze the electrical performance of InAs MOSFETs at different V_{DS} values and address a V_{DD} scaling investigation to evaluate the performance of III-V MOSFET at small supply voltages and channel lengths.

2. Model

The device under investigation is similar to that of Ref. [2]. As shown in Fig. 1, it consists of an ultra-thin InAs channel of 2.4nm thickness deposited on an InAlAs layer with the InP lattice constant. Hence, InAs is under compressive strain ($\epsilon_{||} = -0.0311$, $\epsilon_{\perp} = 0.0338$). Spacers have a length of 17nm and help to prevent source-to-drain tunneling at small gate lengths (L_G). The gate oxide is composed of 0.5nm of Al_2O_3 and 2nm of ZrO_2 .

In our study we adopted a full-quantum approach to account for any leakage mechanism and quantum effect. The devices are simulated using a self-consistent solution of the 2D Poisson and Schrödinger equations in the NEGF formalism employing an 8×8 k·p Hamiltonian [4]. Such an Hamiltonian is able to consider transport within the Γ valley, as well as strain effects on the bandstructure and transport properties. Phonon scattering is implemented via the self-consistent Born approximation and local self-energies. Acoustic phonons are treated within the elastic approximation, whereas polar optical phonons are assumed to be dispersionless. Details on the scattering parameters can be found in Ref. [5].

3. Results

Transfer characteristics for different V_{DS} values and $L_G=25$ nm are shown in Fig. 2. We note a significant increase of the OFF-current (I_{OFF}) as V_{DS} increases. To gain insight on this behavior, in Fig. 3 we plot the lowest conduction (LC) and the highest valence (HV) subband for different V_{GS} at $V_{DS}=0.7$ V. The effective gap is larger than in bulk InAs due to quantum-confinement and strain effects. It can be observed that the LC subband is energetically lower than the HV subband in a region near the channel/drain junction. This condition enhances band-to-band tunneling (BTBT) of valence electrons in the channel and conduction electrons in the drain (see the local density of states in Fig. 4(a)). However, such a BTBT does not directly contribute to the current because the HV

subband in the source is lower than the LC subband in the drain. At low values of V_{GS} , the BTBT induces a positive charge in the channel and therefore decreases the gate control on the channel barrier, resulting in a degraded sub-threshold swing (SS) when $V_{DS}>0.5$ V. As shown in Fig. 4(b) the I_{OFF} is therefore dominated by the thermionic component at energies higher than the top of the barrier (the conduction subband). However, the InAs MOSFET works properly at $V_{DS}<0.6$ V, for which the HV subband is always smaller than the LC subband for the V_{GS} of interest (see Fig. 5). Fig. 6 shows the output characteristics of a device with $L_G=25$ nm presenting an ideal linear behavior at small V_{DS} and high saturation currents. An optimal electrostatic integrity can be appreciated in Fig.7 showing the SS and the DIBL as a function of L_G . Acceptable SS and DIBL values are reported even at $L_G=8$ nm. They are due to the use of an aggressive oxide with an EOT=0.52nm and by the absence of significant interface traps, which is consistent with the characterization data in Ref. [2]. Finally, Fig. 8 shows the I_{ON} (computed as the I_{DS} at $V_{GS}=V_{DS}=V_{DD}=0.5$ V) dependence on L_G for $I_{OFF}=0.1$ uA/um, which is the ITRS specification for high-performance (HP) applications. A maximal value of $I_{ON} \sim 0.5$ mA/um compatible with the experimental value measured in Ref. [2] is found. It is worthwhile to remark that the I_{ON} decreases as L_G is reduced due to the worst electrostatic integrity and the consequent SS deterioration, whereas tunneling current is negligible even at $L_G=8$ nm, mainly because of the use of large spacer regions that suppress direct source-to-drain tunneling, which is the main source of the I_{OFF} degradation in such devices [6].

4. Conclusion

Our 2D full-quantum simulations of ultra-thin InAs channel MOSFETs have shown that for $V_{DS}<0.6$ V such devices can provide I_{ON} values compatible with the ITRS requirements even at small gate lengths, but they suffer from significant BTBT degrading their SS at larger bias voltages.

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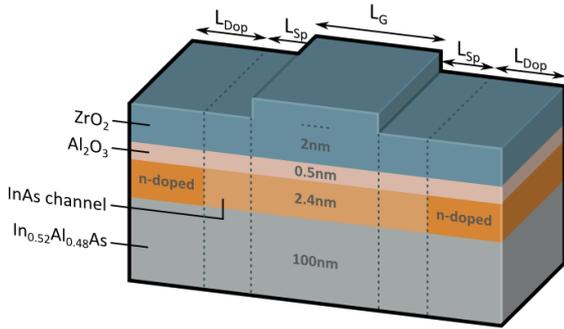


Fig. 1: Sketch of the InAs MOSFET. Doped regions have a donor concentration of $N_D=3.10^{19} \text{ cm}^{-3}$. Parameters: $L_{Dop}=20\text{nm}$, $L_{sp}=17 \text{ nm}$, $L_G = 40, 25, 15, 8 \text{ nm}$.

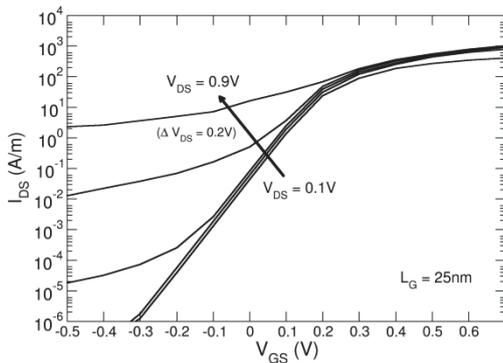


Fig. 2: Transfer characteristics at $V_{DS}=0.1, 0.3, 0.5, 0.7$ and 0.9V for a device with $L_G=25\text{nm}$. The gate work-function is chosen in order to have $I_{OFF}=0.1\mu\text{A}/\mu\text{m}$ for $V_{DS}=0.5\text{V}$.

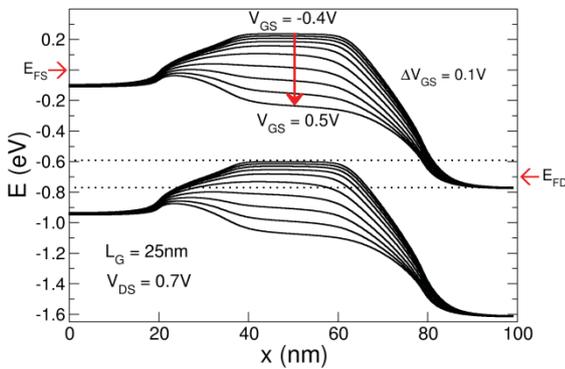


Fig. 3: Spatial profile of the highest valence subband and of the lowest conduction subband at different V_{GS} and $V_{DS}=0.7\text{V}$ for a device with $L_G=25\text{nm}$. Dashed lines indicate the energy window where BTBT occurs. E_{FS} and E_{FD} are the Fermi levels in the source and in the drain.

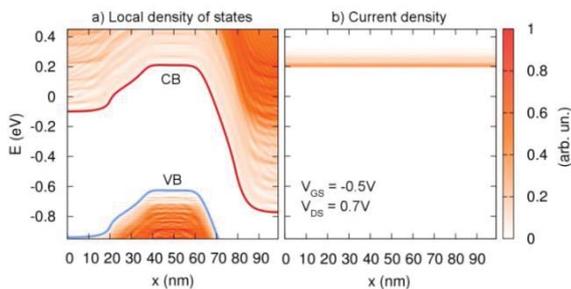


Fig. 4: (a) Local density of states and (b) spectral current density at $V_{GS}=-0.5\text{V}$ and $V_{DS}=0.7\text{V}$ for a device with $L_G=25\text{nm}$.

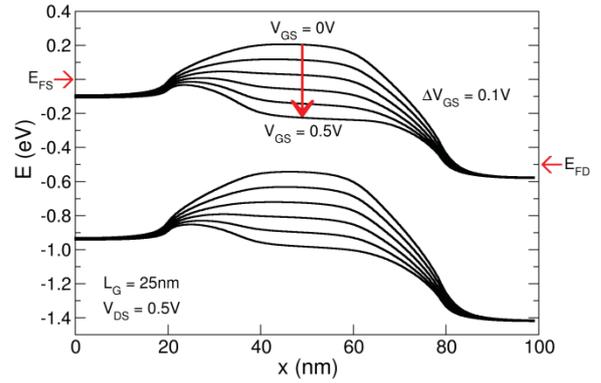


Fig. 5: Same as Fig. 3, but at $V_{DS}=0.5\text{V}$.

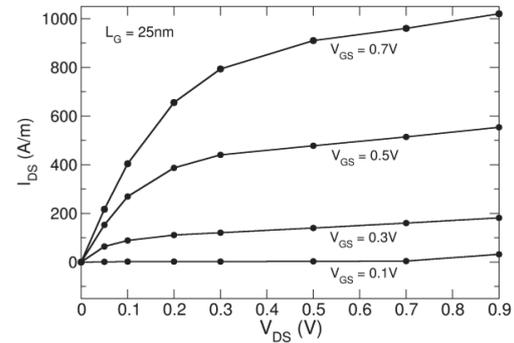


Fig. 6: Output characteristics at $V_{GS}=0.1\text{V}$ to 0.7V for a device with $L_G=25\text{nm}$.

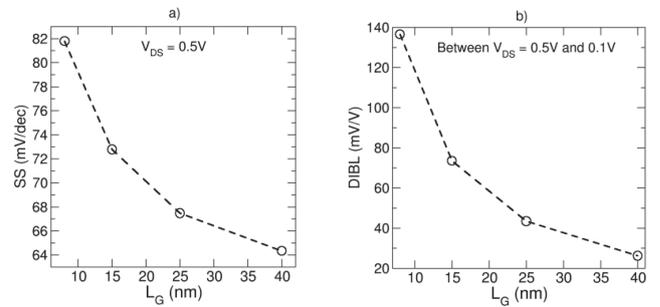


Fig. 7: (a) Sub-threshold swing (SS) evaluated at $V_{DS}=0.5\text{V}$ and (b) DIBL evaluated between $V_{DS}=0.5\text{V}$ and $V_{DS}=0.1\text{V}$ as a function of L_G .

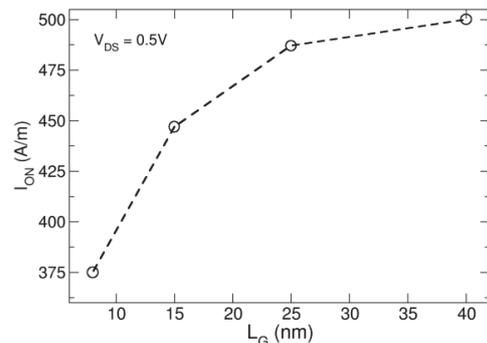


Fig. 8: On current (I_{ON}) as a function of L_G computed assuming $V_{DS}=0.5\text{V}$ and $I_{OFF}=0.1\mu\text{A}/\mu\text{m}$.

Contact Resistances in Trigate Devices in a Non-Equilibrium Green's Functions Framework

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1. Introduction

As the gate length L of field-effect transistors is reaching the sub-20 nm range, the contact resistances are increasingly limiting the electrical performances of the devices. The “apparent” contact resistance R_c can be defined as the extrapolation to zero gate length of the total resistance of the device, $R(L) = V_{ds}/I_{ds}$, where I_{ds} is the drain current and V_{ds} the source-drain voltage. In the low field (low V_{ds}) regime, this contact resistance is dominated by *i*) the quality of the metal-semiconductor contact, *ii*) the transport through the lowly doped regions of the devices such as the spacers, and *iii*) the “ballistic” resistance of the channel. Although the latter can be intrinsic to the channel, it is usually mixed into the apparent contact resistance as it is independent on the gate length. In this work, we compute components *ii*) and *iii*) of the contact resistance in Fully-Depleted Silicon-on-Insulator (FDSOI) Trigate and FinFET devices in a Non-Equilibrium Green's Functions (NEGF) framework [1]. The simulation results are compared to recent electrical measurements performed on Trigate devices fabricated at CEA-LETI.

2. Simulation methodology and devices

The channel is a rectangular [110] oriented silicon nanowire with width W and height H in the 4 to 24 nm range, etched in a (001) SOI layer [2]. The gate stack is made of 0.8 nm SiO₂ and 2.2 nm HfO₂. The channel is connected to bulk source and drain contacts by 6 nm long spacer regions (see Fig. 1). Point-like dopants are added to the source and drain according to the different target distributions plotted in Fig. 2, in order to capture impurity scattering in these regions. Surface roughness, Remote Coulomb Scattering (RCS) in the channel, and electron-phonon interactions are also included in the simulations. The current is computed with a NEGF code in the effective mass approximation.

3. Results

At low bias, the resistance $R(L)$ of the devices is linear with L in the 20-100 nm range and can therefore be extrapolated to $L = 0$ (Fig. 3). The contact resistance $R_c = R(L \rightarrow 0)$ in a 10×10 nm Trigate is plotted as a function of the carrier density in the channel in Fig. 4

(red line with dots), for the “Reference” doping profile of Fig. 2. It is compared to the ballistic resistance of the channel (no scattering), and to the contact resistance extracted in a device without surface roughness nor impurity scattering in the source/drain (continuous background dopant distributions). The contact resistance is much larger than the ballistic resistance, and is clearly limited by scattering by dopant impurities and surface roughness. It represents a significant part of the total resistance of a $L = 30$ nm long device (green line with diamonds). A careful analysis of the data shows that the lowly doped spacers are the most resistive elements. This will be discussed at the conference, together with the comparison of the total contact resistance of Fig. 4 with experimental data.

The contact resistances for the different doping profiles of Fig. 2 are plotted in Fig. 5, and for different nanowire cross sections in Fig. 6. R_c decreases when doping increases under the spacers, at the expense of a loss of electrostatic control (larger DIBL). Also, R_c increases when the cross sectional area decreases. Other results about the design of the spacers, and about the link with the apparent dependence of the mobility on gate length [3,4], will be discussed at the conference.

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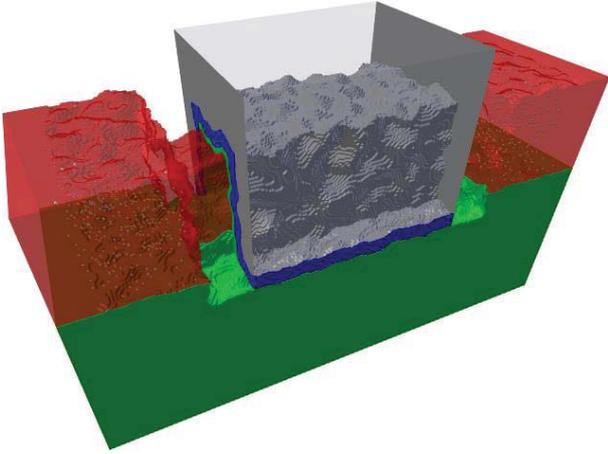


Fig.1: A $W = 10 \times H = 10$ nm Trigate device, with overgrown source and drain contacts. Silicon is in red, SiO_2 in green, HfO_2 in blue and the gate in gray. The dots in the contacts are single dopant impurities. The spacers are 6 nm long.

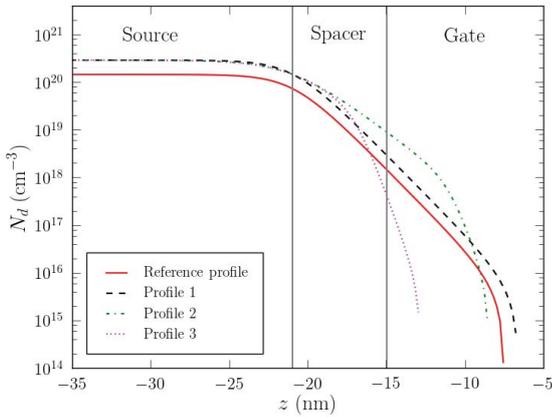


Fig.2: Target doping profiles in the source of Fig. 1 (doping profiles are symmetric in the drain). They are used to generate random dopant distributions.

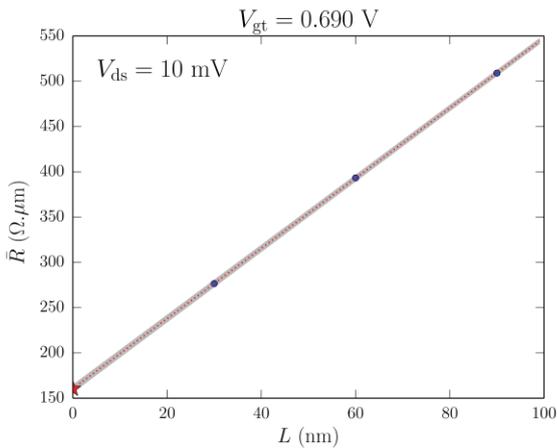


Fig.3: The resistance $R(L)$ as a function of channel length L for a particular realization of the “Reference” doping profile of Fig. 2. The carrier density in the channel is $n = 10^{13} \text{ cm}^{-2}$. The contact resistance is the extrapolated $R_c = R(L \rightarrow 0)$, while the slope gives an estimate of the carrier mobility in the channel.

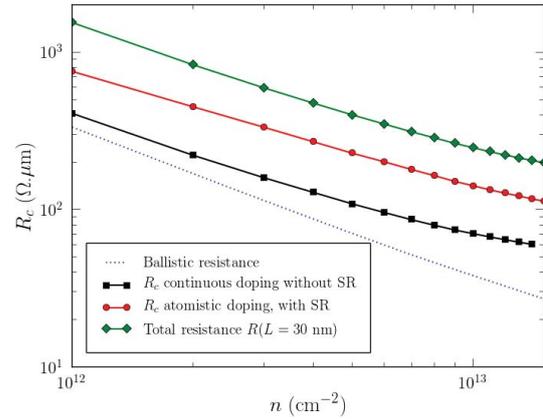


Fig.4: The contact resistance R_c extracted from Fig. 3 as a function of the carrier density n in the channel. R_c is normalized to the effective width $W+2H$ of the device. It is compared to the ballistic resistance of the channel, to the contact resistance extracted without surface roughness nor impurity scattering, and to the total resistance of a $L = 30$ nm long device.

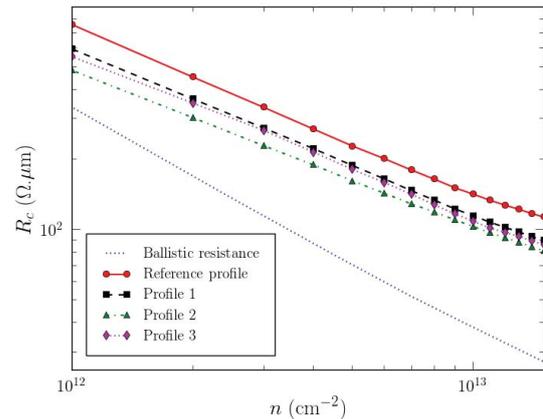


Fig.5: The contact resistance R_c as a function of n for the different doping profiles of Fig. 2.

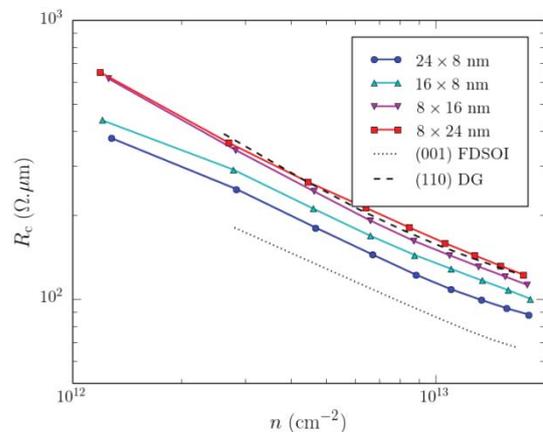


Fig.6: The contact resistance R_c as a function of n for different nanowire cross sections $W \times H$. The target doping profile is the “Reference” profile of Fig. 2. The data are compared with reference (001) FDSOI ($H = 8$ nm, $W \rightarrow \infty$) and (110) double gate devices ($W = 8$ nm, $H \rightarrow \infty$).

Analysis and Modelling of Temperature Effect on DIBL in UTBB FD SOI MOSFETs

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1. Abstract

The Drain Induced Barrier Lowering (DIBL) behavior in Ultra-Thin Body and Buried oxide (UTBB) transistors is investigated in details in the temperature range up to 150°C, for the first time to the best of our knowledge. The analysis is based on experimental data, physical device simulation, compact model (SPICE) simulation and previously published models. Contrarily to MASTAR prediction, experiments reveal DIBL increase with temperature. Physical device simulations of different thin-film fully-depleted (FD) devices outline the generality of such behavior. SPICE simulations, with UTSOI DK2.4 model, only partially adhere to experimental trends. Several analytic models available in the literature are assessed for DIBL vs. temperature prediction. Although being the closest to experiments, Fasarakis' model overestimates DIBL(T) dependence for shortest devices and underestimates it for upsized gate lengths frequently used in ULV (ultra-low-voltage) applications. This model is improved in our work, by introducing a temperature-dependent inversion charge at threshold. The improved model showed very good agreement with experimental data, with high gain in precision for the gate lengths under test.

2. Introduction

The Ultra-Thin Body and Buried oxide (UTBB) SOI MOSFET is widely considered for future technology nodes thanks to its improved electrostatic and variability control [1]. The scalability of UTBB devices can reach the 8 nm node, considering DIBL (Drain Induced Barrier Lowering) values < 100 mV/V as the electrostatic criterion [1]. Studying the temperature effects in UTBB SOI MOSFETs is important even for room-temperature applications, as these devices can be affected by self-heating with channel temperature reaching ~ 100°C under normal operation conditions [2-3]. In [4-5], the DIBL of bulk 0.4-1.5 μm -long devices showed increase with temperature and stronger dependence for shorter devices. For 28 nm long UTBB devices [6], an increase of DIBL by about 20 mV/V over 100°C was observed. However, in-depth analysis of DIBL evolution with temperature was not performed. The present work investigates the experimental DIBL behavior and compares the observed results to physical simulations (Atlas), compact modelling (SPICE) and several published analytical models. In order to reproduce the experimental DIBL dependence on temperature, an upgrade of the most adequate model to date is proposed.

3. Experimental Devices

The experimental devices were fabricated at ST Microelectronics [7], with a BOX thickness (t_{BOX}) of 25 nm and silicon body (t_{Si}) of 7 nm. The metal gate stack is composed of 2.3 nm of HfSiON with an equivalent oxide thickness (t_{OX}) of 1.3 nm. The measured devices are n-channel MOSFETs with gate lengths (L) from 34 to 500 nm and channel width (W) of 1 μm . The channel is left undoped. Both

standard V_T (STDVT) and low V_T (LVT) devices were measured up to 150°C.

4. Results and Discussion

Fig. 1 shows the experimental DIBL as a function of temperature. The DIBL values were calculated from $\Delta V_G/\Delta V_D$, where V_G is the gate voltage at the constant current value of 10^{-7} (W/L) for low V_D (V_{DL}) of 50 mV or high V_D (V_{DH}) of 1 V. The increase of DIBL with temperature can be clearly observed for both LVT and STDVT transistors. Moreover, this increase is stronger in shorter devices. DIBL values calculated using MASTAR software [8] are plotted on the same graph for the sake of comparison and are independent of temperature.

Fig. 2 presents the DIBL for different thin-film FD structures simulated with Atlas [9]. This simulation analysis aims at verifying whether some particular process feature could generate such DIBL behavior. An ideal double gate (DG) structure was also studied to remove any possible channel position and substrate depletion effects. For all structures, the trend is the same as for experimental results of Fig. 1, highlighting that this DIBL behavior is physical and not specific to the measured UTBB devices. Fig. 3 shows the DIBL variation with temperature from circuit-level simulations using UTSOI DK2.4 model from ST Microelectronics [10] compared to experimental data for devices with L of 42 and 60 nm. The UTSOI DK2.4 model qualitatively reproduces the experimental DIBL dependence on temperature for L = 60nm. However, the modeled DIBL(T) incorrectly lowers with reduced L and is underestimated for L=42nm.

We then assess the ability of different analytic models to reproduce DIBL vs. temperature increase in UTBB devices. Fig. 4 shows the DIBL as a function of L for different models published in literature, for T = 25°C (top) and T = 150°C (bottom). Three models are considered: 1°) MASTAR software [8], which is based on Voltage Drop Transformation (VDT) model [11]; 2°) Arshad's model [12] an improved version of MASTAR model, which takes into account the effective length (L_{EFF}) and the mean channel position in the thin film (Y_{MEAN}); 3°) Fasarakis' model [13] which is a threshold voltage model, defining the DIBL as the difference between the V_T for low and high V_D . Though MASTAR software can calculate the drain current and SCE (Short-Channel Effects) as a function of temperature, the DIBL equation does not include dependence on temperature (Fig. 1). Arshad's model can be adapted for different T by considering $L_{\text{EFF}}(T)$ and $Y_{\text{MEAN}}(T)$ extracted from simulations. The Y_{MEAN} shifts towards bottom interface and L_{EFF} becomes shorter with T increase. Both these trends naturally result in DIBL increase at higher T. However, incorporation of these dependences is not sufficient to reproduce actual DIBL(T) results. Fasarakis' model has a good accuracy for room temperature but deviates at higher temperature.

Fig. 5 shows the $\Delta DIBL/\Delta T$ as a function of L for measurements and Fasarakis' original model. Both experimental and model results feature enhanced DIBL vs T increase with L shortening. However, Fasarakis' model gives stronger dependence, particularly overestimating $\Delta DIBL/\Delta T$ values in shorter devices and underestimating in long ones. The reason is that the inversion charge defined at the threshold condition (Q_{TH}) in Fasarakis' model has no temperature dependence. We extracted the Q_{TH} from Atlas electron concentration taking into account the Y_{MEAN} for different T and V_D . Then, we introduced these values in Fasarakis' model. The result is shown in Fig. 5, referred as "Fasarakis et al + $Q_{TH}(T)$ dependence". It can be observed that the proposed upgraded model reproduces well the experimental data in the whole L range under consideration and can be used to estimate the temperature dependence of DIBL with temperature for UTBB devices. In some applications, especially ULV, the use of channel lengths above the minimal length of the technology is common to minimize current leakage [14] and to have better analog performance [15]. Fig. 6 shows the comparison between Fasarakis' model and its improved version for the devices with L of 38 and 120nm. The proposed improvement in model is the most accurate, with a precision gain of 35% for L=120nm, showing that the Q_{TH} is significantly temperature dependent (Fig.6 inset).

5. Conclusions

The DIBL dependence on temperature in UTBB FD SOI MOSFETs was analyzed. The experimental results revealed increase of DIBL with temperature. This trend is confirmed by both physical and SPICE simulations. The fact that physical devices simulation of different thin-film architectures provides

the same trends emphasizes generality of such DIBL temperature behavior. Existed models, however, do not allow to reproduce DIBL(T) dependence properly. We proposed a way to upgrade the voltage model of Fasarakis et al, by including inversion charge (accounting for channel position) dependence on T in order to correctly reproduce/predict DIBL variation with temperature. The obtained results show very good agreement with experimental data and significant gain of precision for both shortest devices and for longer ones with channel lengths in the range used for low leakage ULV digital or good output conductance analog applications for this technology.

Acknowledgements

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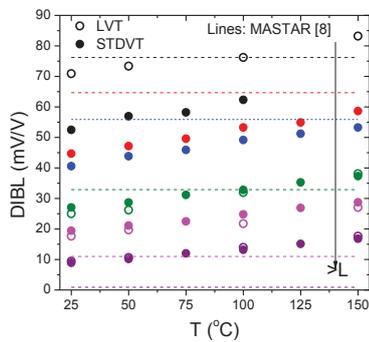


Fig.1: Measured DIBL as a function of temperature for STDVT and LVT devices of different lengths.

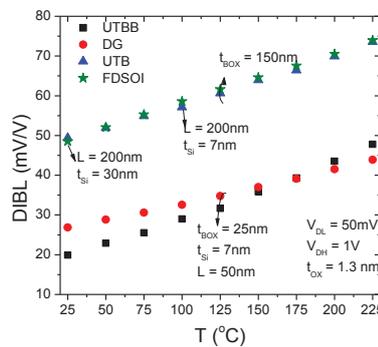


Fig.2: DIBL as a function of temperature from Atlas simulations of different SOI structures.

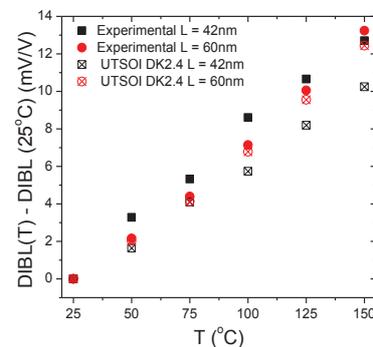


Fig.3: DIBL increase with temperature for lengths of 42 and 60 nm from measurements and SPICE simulations.

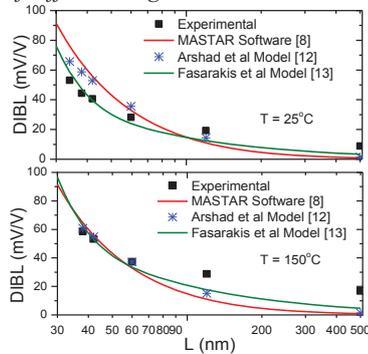


Fig.4: DIBL as a function of channel length for temperatures of 25°C (top) and 150°C (bottom).

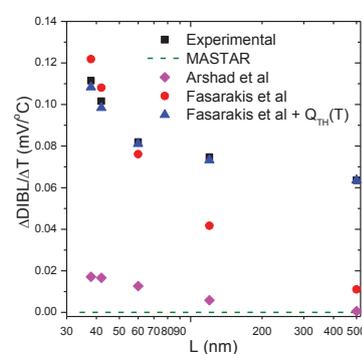


Fig.5: $\Delta DIBL/\Delta T$ up to 150°C as a function of channel length.

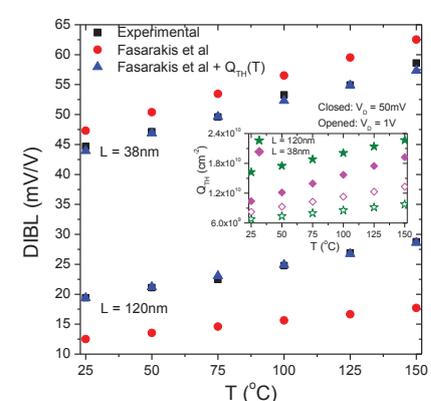


Fig.6: DIBL as a function of temperature for the devices with L=38 and 120nm. (Inset) Extracted $Q_{TH}(T)$ for the same devices.

Modeling Neutral Particle Flux in High Aspect Ratio Holes using a One-Dimensional Radiosity Approach

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1. Introduction

We propose a one-dimensional radiosity model to approximate the local flux on the wall and bottom of high aspect ratio (HAR) holes during three-dimensional plasma etching simulations. In this work we consider an ideal cylindrical shape, ideal diffuse reflections/sources, and a sticking probability s , independent of the flux; ballistic transport is assumed for the neutral particles.

The diffuse re-emission mechanism is a common assumption for neutral particles [1] and cylinder-like shapes are a key prerequisite for HAR holes in the context of, for instance, 3D NAND processing [2].

During a plasma etching simulation the local fluxes of the etching species are used to model the surface reactions. The local flux must be recalculated for each simulation time step, because the interface positions are changing due to the evolving surface. For HAR features, the local flux originating from re-emission is prominent and the local flux rates can easily vary by orders of magnitude along the feature depth.

Considering the computational costs of a three-dimensional plasma etching simulation, the calculation of the local flux is dominant. The efficient calculation of the neutral flux is therefore essential considering especially the fact that HARs further increase this dominance.

Common approaches for three-dimensional flux calculation are Monte Carlo ray tracing [3] and radiosity based [4] methods. Ray tracing supports bi-directional reflectance distribution functions, whereas radiosity inherently favors diffusely reflecting surfaces.

We propose a computationally inexpensive one-dimensional approach, which reproduces the results obtained by a three-dimensional ray tracing simulation, and can therefore be used as a drop-in replacement for cylinder-like hole structures.

2. One-Dimensional Radiosity

The simulation domain (Fig. 1) is a circular cylinder parameterized along its depth and radius. We model the source of neutral particles by an ideal diffusely-emitting disk closing the cylinder at the top without re-emission ($s=1$). The wall of the cylinder is an ideal diffuse reflector with a constant sticking probability ($s=s_w$). The bottom of the cylinder does not have any re-emission ($s=1$). This setup is a reasonable approximation for the neutral flux in a HAR plasma etching environment.

Our approach is based on rotational symmetry and a subdivision of the cylinder into surface elements (Fig. 1). By assuming a constant flux and a constant sticking probability over each surface element, the problem can be formulated using the discrete radiosity equation: For a surface element i the equation reads

$$B_i = E_i + (1 - \alpha_i) \cdot \sum_j (F_{j \rightarrow i} \cdot B_j), \quad (1)$$

where B is the radiosity (sum of emitted and reflected energy), E is the emitted energy, α is the absorptance and $F_{j \rightarrow i}$ is the view factor (proportion of the radiated energy which leaves element j and is received by element i). The radiosity B is related to the absorbed energy A by

$$A_i = (B_i - E_i) \cdot \alpha_i / (1 - \alpha_i). \quad (2)$$

We adapt Equation (2) to our problem by substituting the absorbed energy A by the flux and the absorptance α by the sticking probability s . The view factors F are derived using an analytical formula for two coaxial disks of unequal radius [5].

The solution to the resulting diagonally-dominant linear system of equations is approximated with the Jacobi method.

3. Results

The normalized flux distributions for holes with aspect ratios (ARs) 5 and 45 are shown in Fig. 2. The non-continuity of the sticking probability causes a jump at the wall-bottom interface. The flux is normalized to the flux on a surface fully exposed to an infinite source plane. Fig. 3 and Fig. 4 compare the flux distributions for $AR=5$ obtained using the proposed one-dimensional radiosity approach with results generated by a reference Monte Carlo ray tracing tool [6]; similarly, Fig. 5 and Fig. 6. compare the flux distributions for $AR=45$.

The results show a good agreement, beside the deviation at the wall-bottom interface, caused by the discretization which is used in the ray tracing simulation. The separation of the flux distributions, particularly visible for $s_w=0.2$ (Fig. 5), and the visible noise in Fig. 6, reflect the stochastic nature of the ray tracing approach.

4. Summary

We provide an approximation of the local neutral flux in three-dimensional plasma etching simulations of HAR holes using a one-dimensional radiosity approach. Comparing the results with a three-dimensional Monte Carlo ray tracing simulation shows good agreement.

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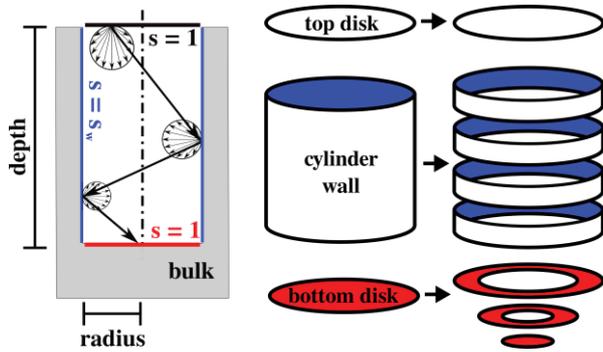


Fig. 1: *Left:* The simulation domain is decomposed into a fully adsorbing source (black), a partly adsorbing wall (blue) and a fully adsorbing bottom (red). *Right:* The wall and bottom are subdivided into ring elements; the top disk is not subdivided as the flux distribution leaving the cylinder is not of relevance.

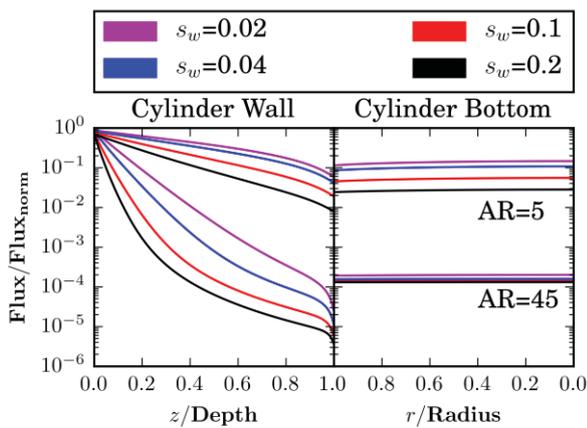


Fig. 2: *One-Dimensional Radiosity:* Normalized flux distribution along the wall (left) and the bottom (right) of holes with aspect ratios $AR=5$ (upper group) and $AR=45$ (lower group). The sticking probability of the wall s_w is varied from 0.02 to 0.2.

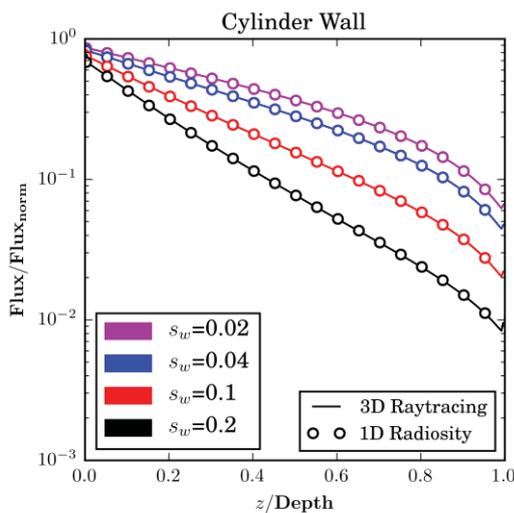


Fig. 3: *Ray Tracing vs. Radiosity ($AR=5$):* Flux along the wall for different sticking probabilities s_w . The ray tracing results show an increasing flux near the wall-bottom interface.

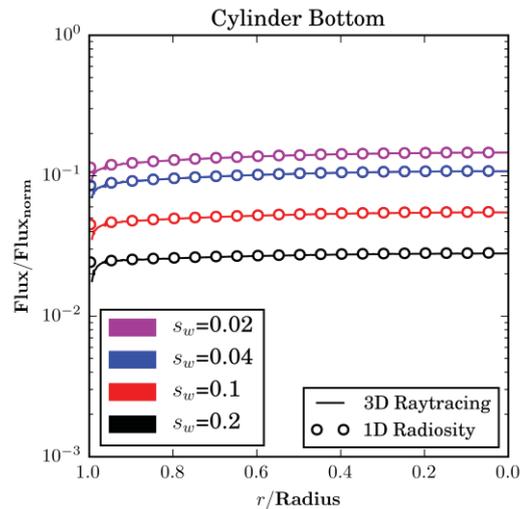


Fig. 4: *Ray Tracing vs. Radiosity ($AR=5$):* Flux along the bottom for different sticking probabilities s_w . Differences are visible near the wall-bottom interface.

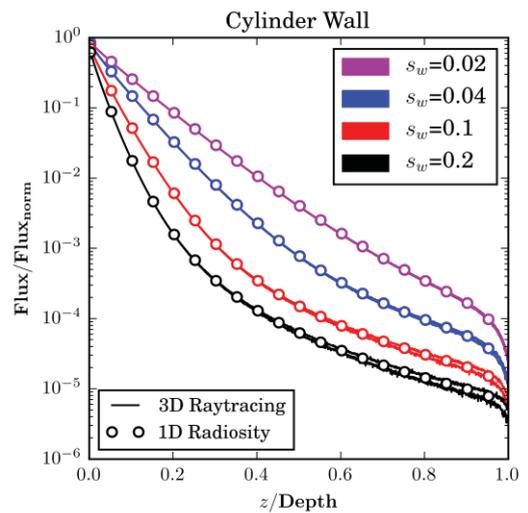


Fig. 5: *Ray Tracing vs. Radiosity ($AR=45$):* Flux along the wall for different sticking probabilities s_w . For each depth, minimum and maximum are plotted for the ray tracing results; the difference increases towards the bottom interface.

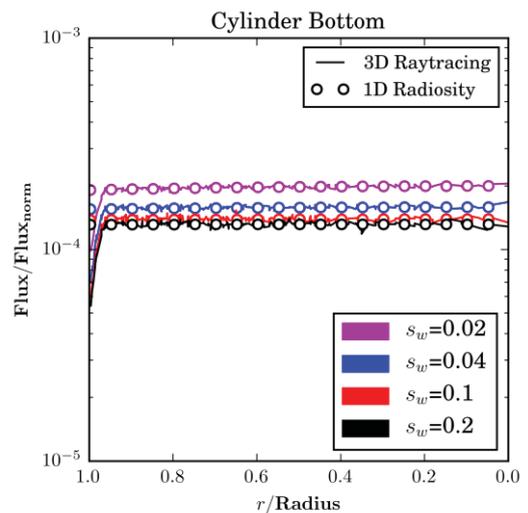


Fig. 6: *Ray Tracing vs. Radiosity ($AR=45$):* Flux along the bottom for different sticking probabilities s_w . Differences are visible near the wall-bottom interface. The ray tracing results reveal noise over the entire domain.

CMOS Platform for Silicon Spin Qubits

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Quantum computing exploits some sort of quantum-based built-in parallelism, which results in a computation power growing exponentially with the number of quantum bits (qubits). It has been theoretically shown that quantum computers could largely outperform the most powerful classical computers in the solution of certain classes of problems, such as number factorization, which is at the core of cryptographic protocols. In order to become truly competitive, however, quantum computers will need to encompass large numbers of qubits coupled to each other. Large-scale qubit integration is therefore the biggest challenge to face.

This presentation deals with the case of silicon-based qubits where quantum information is encoded in a spin degree of freedom. Such qubits were recently shown to yield outstanding performances at the one and two qubit level. The implementation of silicon spin qubits onto an industrial CMOS platform may largely facilitate their development into large-scale integrated quantum circuits. Following this idea, we are exploring a possible route to CMOS spin qubits, our approach being based on state-of-the-art 300-mm silicon-on-insulator technology. Here we provide an outline of this project and present our advances in the development of the basic building blocks for CMOS spin qubits.

First RF Characterization of InGaAs RMG nFETs on SiGe-OI FinFETs Fabricated by 3D Monolithic Integration

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Introduction

3D Monolithic (3DM) integration is attracting much attention owing to density scaling benefits and the potential to stack independently optimized multifunctional layers at transistor level [1]. However, due to the inherently high thermal budget of Si MOSFET process, Si(Ge)-on-Si 3DM integration scheme faces major challenges in top layer optimization without degrading bottom layer performance. As the InGaAs MOSFET processing thermal budget is significantly lower, it is well-suited to be used as the top layer channel material. Besides this, InGaAs also has higher mobility enabling high performance at lower voltages and is a widely used material for high-frequency devices. Here, we show RF characteristics of InGaAs nFETs fabricated with RMG process on top of SiGe-OI finFETs in a 3DM integration scheme. We demonstrate a cut-off frequency of 16.4 GHz for gate length (L_g) of 120 nm.

Device Fabrication

The 3DM process flow is shown in Fig. 1(a). Firstly, bottom layer SiGe-OI fin pFETs are fabricated with a process described in ref [2, 3]. After the silicidation step of SiGe-OI finFET process, the inter-layer oxide is deposited and CMP planarization is carried out. The InGaAs layer is transferred on to this oxide with direct wafer bonding from InP donor wafers [4]. InGaAs nFET fabrication is then performed with the RMG process described in [5]. Finally, oxide encapsulation is deposited and contact holes are opened and metallization is completed.

Electrical Characterization

Fig. 2 (a) shows the DC I_d - V_g characteristics of top InGaAs planar nFET with $L_g = 120$ nm. This device also features 10 finger gates in parallel and is so designed to enable RF characterization with coplanar waveguide pad structures. DC characteristics show competitive electrostatic control with DIBL of 100 mV/V and $SS^{\text{sat}} = 100$ mV/dec due a scaled high-k gate stack with CET of 1.6 nm [5]. Fig. 2 (b) shows the I_d - V_d characteristics for the same device. Fig. 3 shows the I_d - V_g characteristics of the bottom layer SiGe-OI finFET with $L_g = 36$ nm and fin width ~ 15 nm before (black-dash) and after (blue-solid) top nFET fabrication. Owing to the lower thermal budget of the top layer InGaAs

process, very minimal impact is observed on the bottom pFET, even for a scaled gate length. Nearly the same I_{ON} is maintained in the pFET indicating no degradation of the bottom silicide. RF characterization of the top nFET is performed on the devices with 10 parallel finger gates, each with a width of 2 μm (= total width of 20 μm), and having GSG pad configuration. LRRM calibration with a vector-network-analyzer (VNA) is first carried out to move reference plane to probe tips. Dedicated on-chip 'open' pad structures are used to de-embed the device. S-parameters are measured from 45 MHz to 40 GHz. From the measured S-parameters, current gain ($|h_{21}|$) is calculated and shown in Fig. 4 for a device with $L_g = 120$ nm. A cut-off frequency (F_t) of 16.43 GHz is obtained for $V_{ds} = 1\text{V}$. Lower F_t value is probably due to higher access resistance in the device and high parasitic capacitance between the gate-source/drain contacts due to short separation of 100nm. Cut-off frequency vs. L_g is plotted in Fig.5 shows an increase in cut-off frequencies with decreasing L_g . Scaling L_g further, along with improving access resistance could provide a way to increase the cut-off frequency.

Conclusion

We show, for the first time, RF characterization of InGaAs RMG nFETs fabricated on top of SiGe-OI finFETs in 3D monolithic integration. A cut-off frequency of 16.4 GHz is obtained for $L_g = 120$ nm nFET with negligible impact on the bottom pFET performance. The InGaAs nFETs also feature a scaled gate stack and tight pitch design (gate-contact spacing = 100 nm). Thus we demonstrate the benefit of InGaAs-on-SiGe 3D monolithic integration, showing that independently optimized multifunctional layers can be fabricated exploiting the advantages of both device layers.

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(a) Fabrication process flow:

- 1) SiGe-OI pFET fabrication [2, 3]
- 2) Oxide deposition and CMP
- 3) InGaAs direct wafer bonding and
InP donor wafer removal [4]

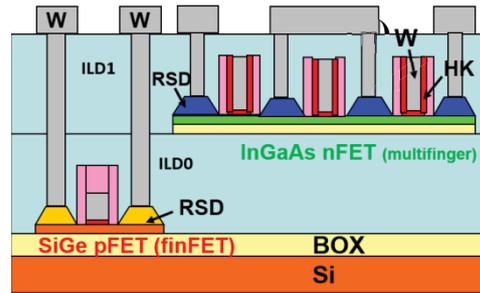


Fig. 1. (a) InGaAs-on-SiGe-OI 3D monolithic process flow with RMG process for InGaAs nFETs, (b) schematic showing the 3D monolithic stack of fabricated InGaAs RMG nFETs with multifinger gates on top of SiGe-OI pFETs

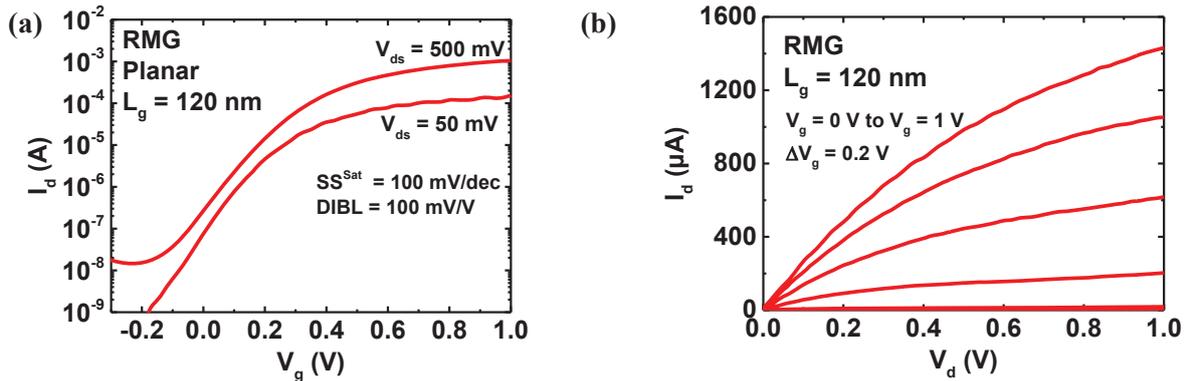


Fig. 2. (a) DC I_d - V_g characteristics of planar RMG InGaAs nFET featuring a L_g of 120 nm with 10 parallel gate fingers. (b) I_d - V_d characteristics of the same nFET with varying V_g .

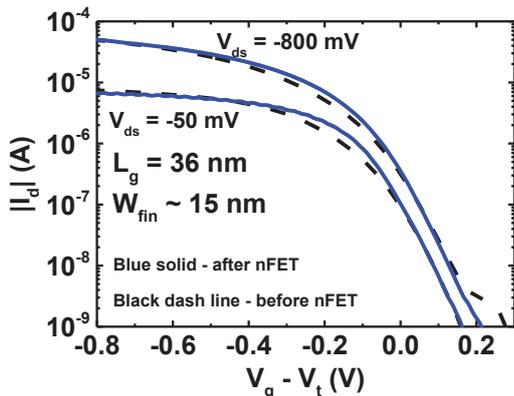


Fig. 3. Comparison of I_d - V_g characteristics for a SiGe-OI finFET at the bottom layer ($L_g = 36$ nm and fin width ~ 15 nm), before and after top nFET fabrication. Minimal impact of the nFET process is evident.

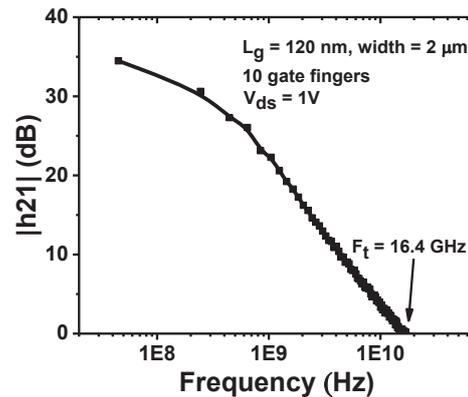


Fig. 4. Measured current gain ($|h_{21}|$) vs. frequency for an InGaAs nFET (top layer) with $L_g = 120$ nm and 10 parallel gate fingers. Cut-off frequency (F_t) of 16.4 GHz is obtained for $V_{ds} = 1$ V.

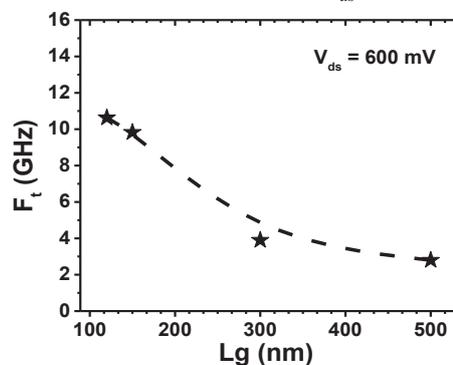


Fig. 5. Cut-off frequency vs. gate length (L_g) for top InGaAs nFETs for $V_{ds} = 600$ mV. Cut-off frequency increases with decreasing gate lengths.

A Sharp-Switching Gateless Device (Z^3 -FET) in 14nm FDSOI Technology

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1. Introduction

Devices with ultra-thin silicon film on insulator (UTSOI) attract increasing attention nowadays for RF and IoT applications. Fully Depleted Silicon On Insulator technology (FDSOI) features high electrical performance by reducing the parasitic capacitances, varying the threshold voltage with back-gate biasing, improving the leakage, mobility and subthreshold swing (SS) [1, 2]. In addition, this technology benefits from simpler (planar) manufacturing process than FinFETs, offering lower power consumption at reduced cost [3-5].

First introduced at the CMOS 28 nm node [1], the Z^3 -FET (Zero gate, Zero swing slope and Zero impact ionization) is a band-modulation device, like FED [6] and Z^2 -FET [7, 8], but without top gates. It exhibits vertical switch, low leakage current (I_{Leak}), tunable triggering voltage (V_{t1}), and high ON current (I_{ON}). In this paper, we present the performance of several types of Z^3 -FET fabricated in 14 nm [9] FDSOI node.

2. Device structure and operation principle

The Z^3 -FET is a forward biased P-I-N diode with an undoped ultra-thin silicon film ($t_{Si} = 6$ nm, Fig. 1a). The source (N^+ doped) is grounded and the drain (P^+ doped) is positively biased ($V_A > 0$ V). Sharp switching is controlled by two separated ground planes that act as back-gates (GP-N/P in Fig. 1). The heavily doped GPs are positively (GP-N) and negatively (GP-P) biased, which keeps the device in OFF state by forming potential barriers and blocking the injection of electrons (from N^+ source) and holes (from P^+ drain) into the body. The triggering is achieved by increasing the anode voltage. When V_A reaches V_{t1} , a positive feedback mechanism occurs due to the flow of carriers from the anode to the cathode and vice versa, leading to a sudden collapse of barriers. This results in remarkable transition from low to high current, enabling an I_{ON}/I_{OFF} ratio of 8 decades (Figs. 2-3). Comparing to Z^2 -FET [7], the Z^3 -FET does not have high-k metal gate stack which eliminates any issues related to high voltage reliability. Moreover, the free surface can be functionalized for various applications like bio and light sensing.

Three variants have been fabricated. The first one has an ultra-thin silicon film ($t_{Si} = 6$ nm), Fig. 1a. The second (Fig. 1b) and the third (Fig. 1c) variants feature thicker Si film ($t_{Si} = 12$ nm). The L_n part of the third variant received light doping. All structures have thin buried oxide ($t_{BOX} = 20$ nm) and fixed width (300 μ m).

3. Static and transient behavior

DC and TLP [10] measurements were performed at room temperature.

Static curves. Typical output characteristics (sharp switch, low leakage current, tunable V_{t1}) are presented in Figs. 2-3. The ultrathin device features a very low leakage current ($I_{Leak} < 10^{-11}$ A) in OFF state but no sharp switch (SS = 60 mV/dec). The switching characteristic is improved by increasing the film thickness up to 12 nm (Fig. 2b). The GPs serve in tuning the triggering voltage. In long devices ($L_p = L_n = 200$ nm) with ultrathin film, the barrier is strong enough at $V_{Gbp} = 0$ V to prevent the injection of electrons (Fig. 2a), while with thicker t_{Si} it is needed to reinforce the electron barrier by negatively biasing the GP-P ($V_{Gbp} = -2$ V), as shown in Fig. 2b. As V_{Gbn} increases, the holes injection barrier is stronger, hence a higher V_{t1} is needed to turn on the device. The evolution of triggering voltage with V_{Gbn} is presented in insets of Figs. 2a-b, showing that V_{t1} is very sensitive to the back-gate bias ($\Delta V_{t1}/\Delta V_{Gbn} = 900$ mV/V).

The I_A - V_A characteristics of the doped variant are presented in Fig. 3. Thanks to the partial channel doping, the device is blocked without back-gate bias, even in shorter devices. The triggering voltage increases and the leakage current decreases with device length due to the reinforcement of the injection barriers.

Pulsed current. The ESD behavior was investigated with transmission line pulse characterizations (TLP) for different pulse width ($t_{PW} = 5$ & 100 ns) and native rise time (~ 300 ps). Shorter devices show higher performance: easier triggering with smaller V_{t1} and higher current capability (Fig. 4). Fig. 5 shows an S-shaped negative-resistance characteristic for the partially N-doped device with no back-gate bias. Fig. 6 confirms that the triggering voltage of the device is tunable by GP bias and device length. The barrier formed by GP-N is strengthened at $V_{Gbn} = 2$ V and the higher the $|V_{Gbp}|$ bias, the larger the triggering voltage.

4. Conclusion

For the first time, a gateless band-modulation device (Z^3 -FET) was demonstrated experimentally in 14 nm FDSOI technology. Performances in terms of triggering, leakage current and failure current have been reported. The Z^3 -FET can serve as a robust ESD protection element and also as ion-sensitive, photo-sensitive and memory devices.

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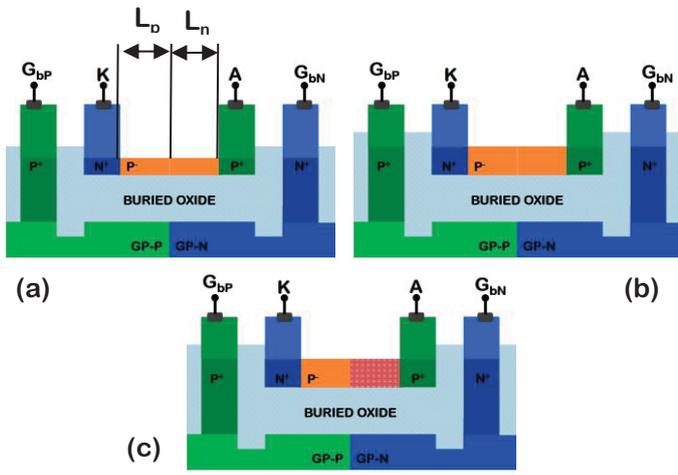


Fig.1: Schematic of Z^3 -FET architecture in 14 nm node: (a) $t_{Si} = 6$ nm, (b) $t_{Si} = 12$ nm, (c) partially N-doped channel, $t_{Si} = 12$ nm.

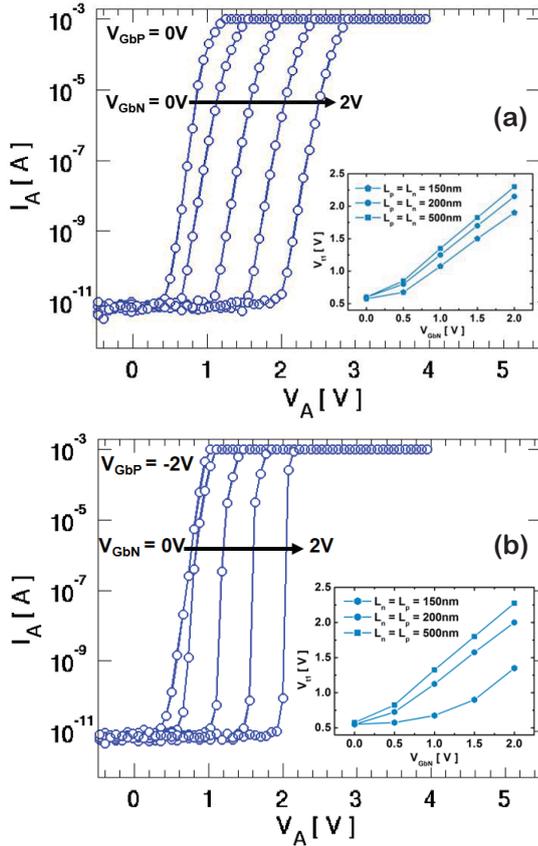


Fig.2: Experimental DC I_A - V_A characteristics for variable GP-N voltages with $V_{G_{bP}} = -2$ V. Z^3 -FET ($L_n = L_p = 200$ nm) with (a) $t_{Si} = 6$ nm and (b) $t_{Si} = 12$ nm (sharp switch). Inset: variation of V_{IL} with $V_{G_{bN}}$.

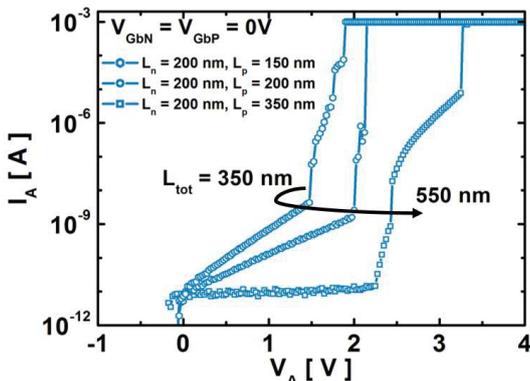


Fig.3: Current versus drain voltage measured for different geometries. Doped Z^3 -FETs with $V_{G_{bN}} = V_{G_{bP}} = 0$ V. $t_{Si} = 12$ nm

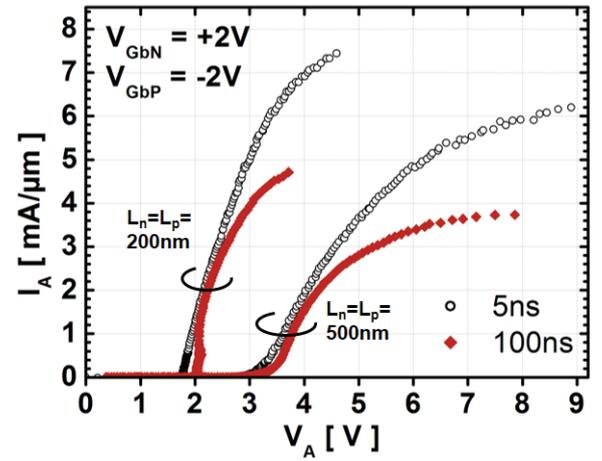


Fig.4: TLP characterization results (I_A - V_A) for 5 ns pulse width (open symbols) and 100 ns (closed symbols) with native rise time (~ 300 ps). $L_p = L_n = 200$ nm and 500 nm. $V_{G_{bN}} = 2$ V and $V_{G_{bP}} = -2$ V. $t_{Si} = 12$ nm.

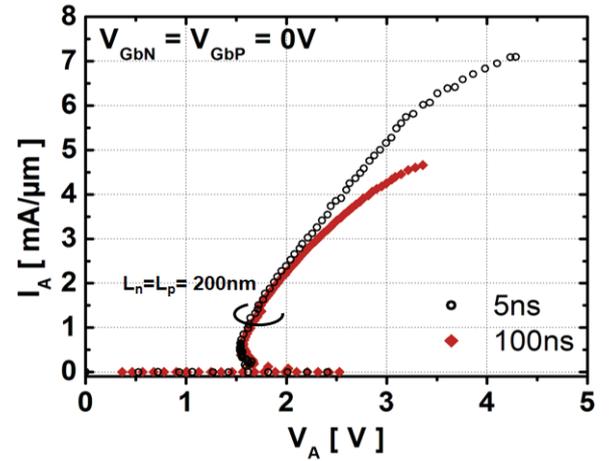


Fig.5: TLP I_A - V_A characteristics for 5 ns and 100 ns pulse width and native rise time ~ 300 ps. $L_p = L_n = 200$ nm (N-doped device) $V_{G_{bN}} = V_{G_{bP}} = 0$ V. $t_{Si} = 12$ nm.

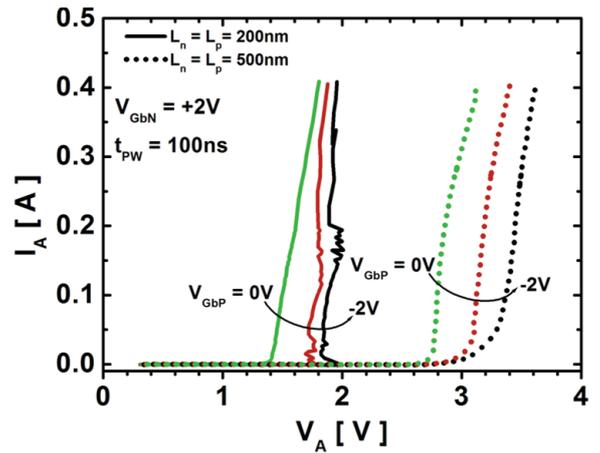


Fig.6: Non-destructive TLP measurements: I_A - V_A for $V_{G_{bN}} = 2$ V and various $V_{G_{bP}}$. $L_p = L_n = 200$ nm (solid lines) and $L_p = L_n = 500$ nm (dotted lines). $t_{Si} = 12$ nm.

End of Scaling Theory and Moore's Law

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1. Introduction

The progress of integrated circuits has been conducted by a prediction -- Moore's law [1] --, and a guideline -- scaling theory [2] (Fig.1). The continuous downsizing of MOSFETs has been accomplished for half a century long since the 1st MOSFET fabrication in order to decrease the production cost and to increase the performance. Further downsizing of the MOSFETs is strongly demanded to deal with the huge amount of information in the coming 'smart society'. However, it is predicted now that the downsizing will reach its limit within a few generations or several years. In this paper, the reasons for the limit for the downsizing is explained, and the future after reaching the limit is predicted.

2. End of the Scaling Theory and Moore's Law

So far, the downsizing of MOSFETs has been accomplished more than 40 years since the beginning of LSI's as shown in Fig.2. What would be the future? Figure 3 shows the trend of device downsizing in human history. It is tremendous that the size decreased with 10 million times in the 20th century by the development of vacuum tubes and semiconductor devices. The size is already approaching the direct-tunneling and atomic distances. Figure 4 shows the future predictions of the downsizing by ITRS 2013, published in April 2014. The downsizing will continue for future 7 generations with the shrink rate of 0.7 time every 2 years, and would reach '1.3 nm' in 2027. However, these are only for the commercial names, and real physical parameters such as the metal half pitch and gate length in 2017 are 8 and 5.6 nm, respectively. Thus, the technology in 2017 would be something like that of 8 or 6 nm in reality. Actually, the shrinking rate for one generation of physical parameters are expected to be much larger from 0.80 to 0.96 as shown in Fig.5. In fact, the physical gate lengths of 14 nm technologies are already as large as 25 nm in some semiconductor companies.

There are difficult problems waiting us to limit the downsizing. They are 1) difficulty in EUV lithography development, and cost increase for the double/triple/quadruple lithography as the alternate, 2) increase in the leakage current of MOSFETs, 3) decrease in on-current or drivability of MOSFETs, 4) increase in the capacitance and resistance of the interconnects, 5) degradation in variability, reliability and yield.

Increase in the leakage current of MOSFETs and decrease in on-current or drivability of MOSFETs are further explained. With downsizing MOSFETs, four leakage current components of the MOSFETs become problematic ; i) punch-through between S (source) and D (drain), ii) direct-tunneling between S and D, iii)

subthreshold leakage between S and D, and iv) gate oxide leakage between G (gate) and S, C (channel) and D. Punch-through can be somehow suppressed by controlling the channel potential fixed to 0V, by decreasing t_{ox} , and adopting multi-gate structure (FDSOI-, or fin-FETs) as shown Fig. 6. Direct tunneling is believed to be the fundamental limit at the gate length of 3 nm. Sub-threshold leakage is very difficult to be suppressed because we need to decrease V_{th} in the course of downsizing as shown in Fig.7. Gate oxide leakage is fortunately believed not to become the limiting factor from our experimental data as shown in Fig 8. In conclusion, the sub-threshold leakage current will limit the downsizing, much before L_g reaches 3nm, especially for mobile applications.

Another big problem is the significant decrease in the on-current of MOSFETs with decrease in t_{ox} and t_{si} as shown in Fig.9. With decrease in these thicknesses, interaction between the carriers and the interface/surface becomes extremely strong as shown in Fig.10, resulting in the significant decrease in mobility. The reduction of the carrier density under low V_{supply} , due to the decrease in the density of the state (DOS) when decreasing t_{si} , is another reason for the on-current reduction.

Even though, the downsizing of the MOSFETs will stop in some future, it is not necessary to be pessimistic. The demand and market size for the microprocessors will keep increasing in future smart society, and thus, the effort to further enhance the performance, decrease the power consumption and production cost will be and should be continued.

3. After the End of Scaling Theory

What would be the future beyond the limit. There is no scaling theory beyond that. How about the Moore's law. The number of the transistors might be increased by the three dimensional integration, but this could extend the limit only a few generations. Thus, the Moore's law will also end in near future in terms of the number of the transistors in a chip. However, in a system level, IoT network increases the number of the devices connected to the system significantly. Moore's law will be extended to hybrid integration of various kinds of devices through the network, resulting in a new value which we have not experienced. In a long term, the hybrid integration of real bio systems including neurons and sensors which are more intelligent, efficient and sensitive than the solid-state devices will extend future possibility with different scale.

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Geometry & Supply voltage	L_g, W_g, T_{ox}, V_{dd}	K	Scaling K: K=0.7 for example
Drive current in saturation	I_d	K	$I_d = v_{sat} W_g C_o (V_g - V_{th})$ C_o : gate C per unit area $\rightarrow W_g (t_{ox}^{-1})(V_g - V_{th}) = W_g t_{ox}^{-1} (V_g - V_{th}) = KK^{-1}K = K$
I_d per unit W_g	I_d/W_g	1	I_d per unit $W_g = I_d / W_g = 1$
Gate capacitance	C_g	K	$C_g = \epsilon_o \epsilon_{ox} L_g W_g / t_{ox} \rightarrow KK/K = K$
Switching speed	τ	K	$\tau = C_g V_{dd} / I_d \rightarrow KK/K = K$
Clock frequency	f	1/K	$f = 1/\tau = 1/K$
Chip area	A_{chip}	α	α : Scaling factor \rightarrow In the past, $\alpha > 1$ for most cases
Integration (# of Tr)	N	α/K^2	$N \rightarrow \alpha/K^2 = 1/K^2$, when $\alpha=1$
Power per chip	P	α	$fN C V^2 / 2 \rightarrow K^{-1}(\alpha K^{-2})K(K^1)^2 = \alpha = 1$, when $\alpha=1$

Fig.1 Scaling scheme

(1970) $10 \mu m \rightarrow 8 \mu m \rightarrow 6 \mu m \rightarrow 4 \mu m \rightarrow 3 \mu m \rightarrow 2 \mu m \rightarrow 1.2 \mu m \rightarrow$
 $0.8 \mu m \rightarrow 0.5 \mu m \rightarrow 0.35 \mu m \rightarrow 0.25 \mu m \rightarrow 180 nm \rightarrow 130 nm \rightarrow$
 $90 nm \rightarrow 65 nm \rightarrow 45 nm \rightarrow 32 nm \rightarrow (28 nm \rightarrow) 22 nm(2012)$
 $\rightarrow 14 nm (2014)$

Fig.2 Past downsizing trend

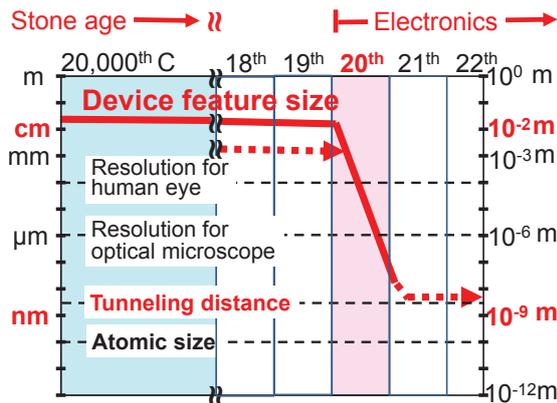


Fig.3 Device downsizing in human history

Year	2013	2015	2017	2019	2021	2023	2025	2027
Commercial name (nm)	14	10	7	5	3.5	2.5	1.8	1.3
Half pitch (HP) (nm)	40	32	25.3	20	15.9	12.6	10	8
L_g (nm)	20.2	16.8	14.0	11.7	9.7	8.1	6.7	5.6

Fig.4 Future downsizing trend by ITRS2013

		Year 2013	Year 2027
Commercial name (nm)	X 0.70 / 2 years	14 (nm)	1.3 (nm)
Metal half pitch (nm)	X 0.80 / 2 years	40 (nm)	8 (nm)
L_g (nm)	X 0.83 / 2 years	20.2 (nm)	5.6 (nm)
V_{dd} (V)	X 0.96 / 2 years	0.86 (V)	0.65 (V)
EOT (nm)	X 0.91 / 2 years	0.80 (nm)	0.43 (nm)
T_{Si} (nm)	X 0.84 / 2 years	7.4 (nm)	2.0 (nm)

Fig.5 Shrink rate of physical parameters by ITRS2013

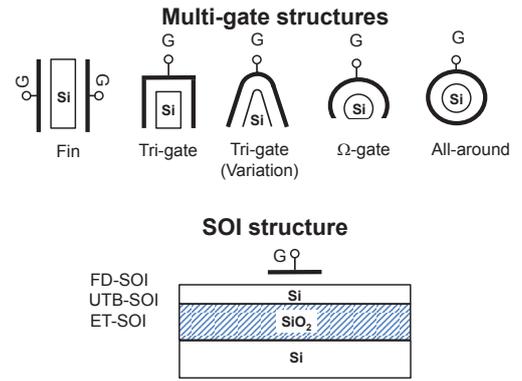


Fig.6 Structures to prevent punch through

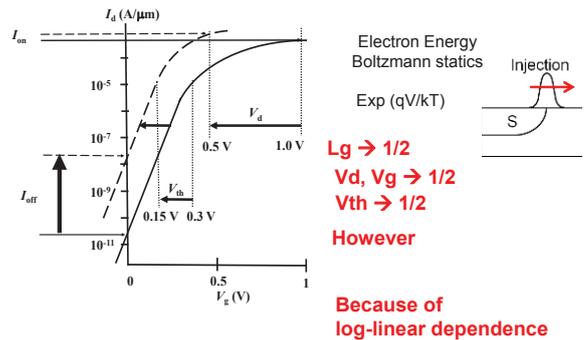


Fig.7 Subthreshold leakage increase with scaling

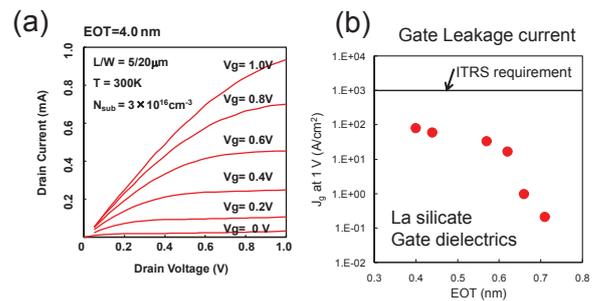


Fig.8 Characteristics of La-silicide MOSFETs

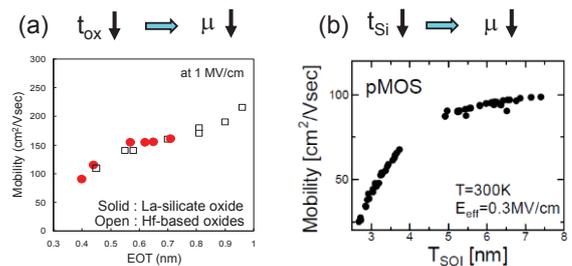


Fig.9 Mobility decrease with decrease EOT [3] and Si thickness [4]

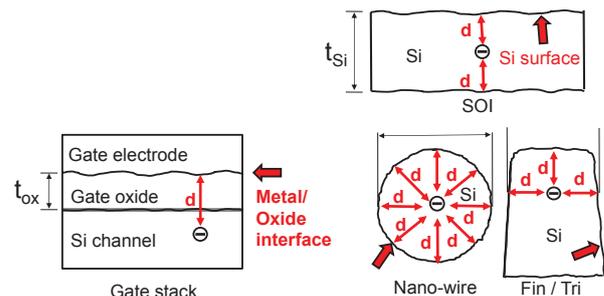


Fig.10 The mechanism of mobility degradation

Robust EOT and Effective Work Function Extraction for 14nm Node FDSOI Technology

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1. Introduction

The effective Work function (WF_{eff}) and the Equivalent Oxide thickness (EOT) are key parameters for FDSOI device characterization. They influence directly Capacitance Equivalent thickness (CET) and Threshold voltage (V_t) and therefore on-current. Both are strongly related to the process: dielectric thickness, metal gate work function and dielectric interface dipole [1]. Former methodologies [2, 3] for automatic and statistical extraction of WF_{eff} and EOT were fitted for bulk but not for FDSOI technology. The extraction difficulties come out with the complexity of the FDSOI structure (Fig. 1) and the strong influence on V_t of several technological parameters such as: channel thickness t_{si} , buried oxide (BOX) thickness t_{box} and well doping level of substrate of BOX backside. We will present a comprehensive study on numerous devices (Fig. 2) combining the process modules on metal gate, dielectric, channel (Si & SiGe) and well type (P & N doped). Reliable parameter extraction is presented by comparison between quantum simulations and experimental capacitances CV allowing the identification of the process modules that really influence EOT and WF_{eff} .

2. Results and Discussion

Fig.1 shows two standard FDSOI MOS devices (P (a) & N (b) MOS) that feature a gate stack characterized by a metal bilayer (Poly and TiN) on the top of oxide bilayer (High k dielectric HfON & SiON). The channel thickness is around 6-8 nm of Si or $\text{Si}_{0.75}\text{Ge}_{0.25}$ stacked on a 20 nm BOX with a P or N-Well with 10^{18}cm^{-3} doping level at its backside. Interlayer (SiON) dielectric thickness is set in order to have two different oxide thicknesses: EOT=1nm for GO1 and EOT=3nm for GO2. The metal bilayer (Poly and TiN), is deposited after a sacrificial metal gate process, specific to each gate type (N or P), including thermal treatment and etching to adjust dipole at oxide bilayer interface [1]. From these standard FDSOI MOS, a wide set of devices has been obtained by combining the process modules on metal gate, dielectric, channel and well type (Fig.2).

The relative gate to channel capacitances (C_{gc}) are reported in Fig. 3 for GO1 and Fig. 4 for GO2. V_t shift with respect to the reference architecture are evidenced and summarized in Fig.2. The identification of gate stack parameters (EOT and WF_{eff}) of these devices (Fig.2) is obtained by fitting Quantum Simulation to experimental capacitances CV. The simulations are based on the self-consistent solution of one dimensional Poisson and Schrodinger equations (PS) carried out by TCAD Simulator (UTOXPP [4]). However, we must notice that in FDSOI technology, adjustment between experiments and simulated CV characteristics still guarantee extraction of EOT (with precision below 0.01 nm) but an expected precision of WF_{eff} below 5mV questionable. Indeed, different set of parameters for t_{box} and t_{si} can lead to the same good fit, but variation on WF_{eff} (Fig. 5). In order to extract t_{box} , we have proposed recently a new CV

measurement with back contact as gate [5]. Adjustment with quantum simulation makes possible a reliable extraction of the box thickness independently of t_{si} and EOT [5]. Concerning t_{si} , it can be obtained by comparison between simulations and experiments on a large set of CV characteristics with back biases from 0V to large back interface inversion (fig. 7). If t_{box} and t_{si} are expected to shift V_t but also WF_{eff} , Source and Drain type as well as back substrate well should only impact V_t . It has been confirmed on a set of three different MOS devices, leading to a same EOT and WF_{eff} extraction for two different well type (Fig. 8) and two different MOS type (Fig.9), validating the reliability of the extraction.

In Fig. 10, WF_{eff} and EOT extraction for the fifteen different tested MOS devices (Figs. 2, 3 and 4) are summarized. The agreement reported on WF_{eff} & EOT in Fig. 8-9 is identified with a blue arrow, other similar agreements can be identified with green arrows. t_{box} and t_{si} are not reported on these figures. In fact, t_{box} is found at the same 20nm value for all the different MOS devices, a value corresponding to the target of this SOI substrate. Concerning t_{si} , it appears to depend only on channel and oxide type. Indeed it is equal to 6.1nm for Si and 7 nm for SiGe for all GO1 devices and 6.8nm for Si and 7.9 nm for SiGe for all GO2 devices, indicating less channel consumption with the GO2 process. EOT is reported in Fig. 10. It depends preliminarily on oxide type, but also on channel material as evidenced [6] with an interlayer oxide increase with SiGe around 0.12nm for GO1 and 0.3nm for GO2. WF_{eff} depends on gate type, channel material and oxide (GO1 and GO2). Considering first GO1, we notice an average shift of 100mV from N to P metal gate. It is the expected effect of Al dipole created at HfON/SiON interface by the sacrificial gate process [1]. With SiGe channel, WF_{eff} report an additional shift of 145mV, it is required in addition to the shift of Valence Band Energy with SiGe to account of the observed 320mV V_t shift, evidenced in Fig. 3. It has been identified as an interface dipole at SiGe/ SiON interface [6]. For GO2, both dipoles at HfON/SiON and SiGe/SiON device interfaces decrease respectively of 45 and 95 mV.

3. Conclusion

Robust EOT and WF_{eff} extractions have been proposed through a methodology which identify first t_{box} and t_{si} . It has been validated on a large set of devices. Such analysis evidence the relative impact of process modules on t_{si} , EOT and WF_{eff} with combined effects of Gate type, channel material and oxide dielectric.

Acknowledgments: Work partly supported by MINOS Laboratory of French ANR and PLACES2BE Project.

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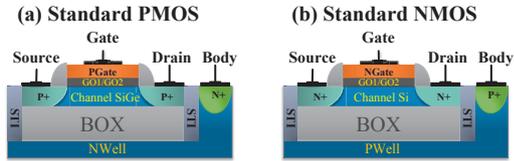


Fig.1: Standard (a) PMOS and (b) NMOS FDSOI devices: both feature a gate stack TiN+Poly on a bilayer oxide HfON+SiON but (a) with SiGe channel and NWell substrate and (b) with Si channel and PWell substrate.

	GO1				GO2			
	Channel	Metal	Well	ΔV_t [mV]	Channel	Metal	Well	ΔV_t [mV]
NMOS	Si	N	P	Ref.	Si	N	P	Ref.
	Si	N	N	45	Si	N	N	115
	Si	P	P	90	Si	P	P	45
PMOS	SiGe	P	N	Ref.	SiGe	P	N	Ref.
	SiGe	N	P	60	SiGe	N	P	90
	SiGe	N	N	100	SiGe	N	N	45
	Si	P	N	320	Si	P	N	250
	x	x	x	x	x	x	x	295

Fig.2: Set of different FDSOI devices featured by combining the process modules on metal gate, dielectric, channel (Si & SiGe) and well (P & N doped). The 4th and 8th columns report on the ΔV_t shift evidenced in Figs. 3 and 4.

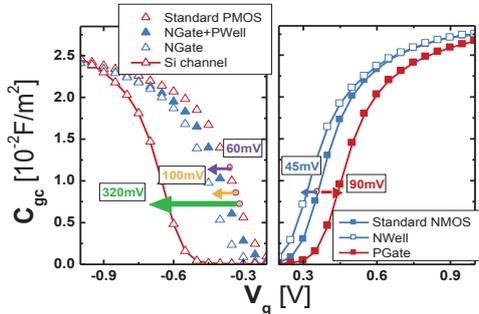


Fig.3: Gate to channel capacitance at back bias $V_b=0V$ for PMOS and NMOS FDSOI GO1 with V_t shift to reference architecture.

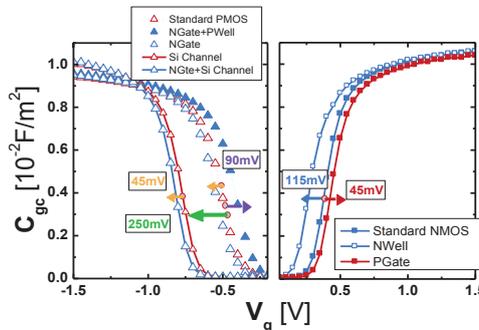


Fig.4: Gate to channel capacitance at back bias $V_b=0V$ for PMOS and NMOS FDSOI GO2 with V_t shift to reference architecture.

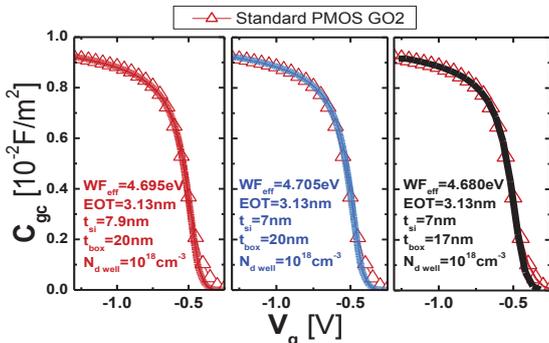


Fig.5: Standard PMOS GO2 Gate to channel capacitance and Simulation (UTOXPP) with different channel and BOX thicknesses; each fit with experimental CV leads to a Wf_{eff} and EOT extraction.

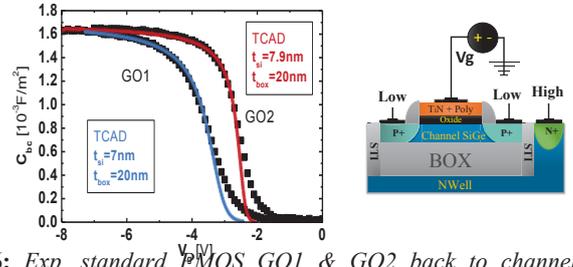


Fig.6: Exp. standard PMOS GO1 & GO2 back to channel capacitance compared to Simulation (UTOXPP) leading to t_{box} extraction.

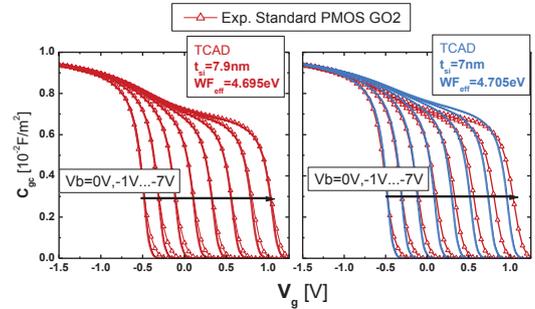


Fig.7: Standard PMOS GO2 Gate to channel capacitance vs Simulation (UTOXPP) with two different channel thicknesses. Here, 7.9nm t_{si} is mandatory for fitting all CV's.

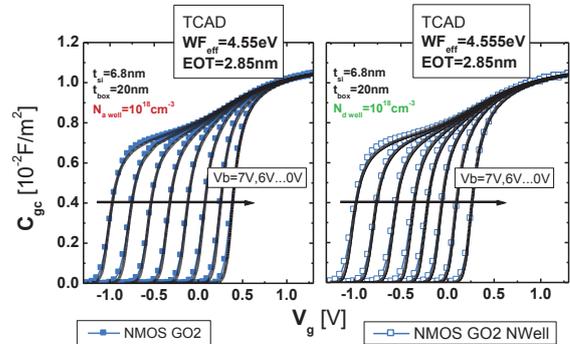


Fig.8: Fitting between simulations and experiments for two MOS devices having two different well types of back side.

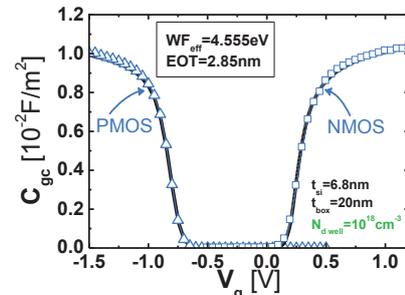


Fig.9: Fitting between simulation and experiment for same gate stack and channel and two MOS types (GO2 NMOS with NWell & GO2 PMOS with NWell and NGate metal and Si channel).

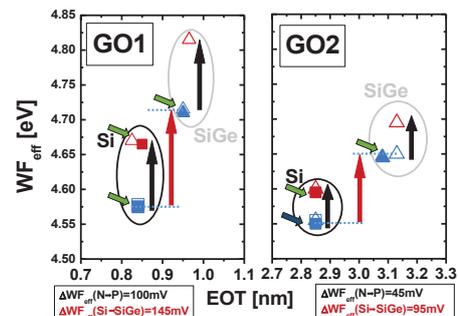


Fig.10: Wf_{eff} versus EOT for different structures PMOS and NMOS FDSOI. Impact of Ge and sacrificial Metal gate and coherence of Wf_{eff} and EOT extraction are shown.

Benchmarks of a III-V TFET Technology Platform against the 10-nm CMOS Technology Node Considering 28T Full-Adders

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I. Introduction — Tunnel field-effect-transistors (TFETs) featuring a potential sub-threshold-swing $SS < 60\text{mV/decade}$ have been proposed as an alternative to conventional MOSFETs [1-4].

A virtual design for a III-V TFET technology platform has been recently proposed by using 3D full-quantum simulations [1,2], and benchmarked against a future CMOS technology [5,6] considering inverters [2]. In this paper, we use TCAD device modeling and circuit simulations to extend such a benchmark to a standard 28T Full-Adder (FA) [7].

II. Methodology — The benchmark relies on a multi-level simulation deck, ranging from the quantum simulations in [2] to the circuit simulations presented here. *TCAD Sentaurus Device* [8] has been used to bridge these levels, in the sense that the full-quantum simulation results in [2] were used to calibrate the drift-diffusion parameters (band-diagram parameters and effective valence/conduction band density of states) as well as the dynamic band-to-band tunneling model parameters (tunneling constants) of the TCAD deck. Then, I_D - V_{GS} - V_{DS} and C - V_{GS} - V_{DS} look-up-tables (LUTs) have been extracted from the TCAD and imported as *Verilog-A* models in the *Cadence* circuit simulator.

III. Devices — The proposed TFET technology platform [2] consists of III-V N/PTFET nanowires (NW); device structures are illustrated in **Fig.1**. Regarding the CMOS counterpart, we consider FinFETs projected to the 10 nm node: *spice Predictive-Technology-Models of Multi-Gate transistors* (PTM-MG) have been presented in [5] and are available in [6]. To assure a fair comparison, the off-current (in A, not in A/ μm) of PTM-MGs have been aligned to the one of the TFETs.

A fine calibration of the TCAD models has allowed us to reproduce the I_D - V_{GS} in [2] (parameters are reported in **Table.I** [1,8,9]), as evidenced in **Fig.2** by the matching between the red/blue lines (calibrated TCAD deck) and symbols (reference simulations from [2]). The CMOS PTM-MG I_D - V_{GS} curves are also reported for comparison (grey lines). Unlike the symmetric characteristics of CMOS devices, the PTFET features a lower on-current than the NTFET (about 25% at $V_{DD} = 400\text{mV}$).

Fig.3 shows the capacitances characteristics (C_{Gx} - V_{GS}). The symbols in the plot represent the total gate capacitances reported in [2], which have been estimated as the net charge difference between the on and off states divided by V_{DD} ($C_{GG} = (Q_{ON} - Q_{OFF})/V_{DD}$). These values have been used in [2] to compute inverter rise/fall times by integrating the device I_D - V_{DS} curves. The simulations in the present paper, instead, have been performed including the full description of the devices (i.e. both current and capacitances LUTs), and thus taking into account also the actual dependence on the biasing point of the intrinsic capacitances.

IV. Full Adders — The test-bench in **Fig.4** allows to simulate a FA block (the green box is the FA under test) under normal operating condition, since it is placed in a framework including driving and loading blocks and the

input sequences are randomly generated. Although only minimum area 28T standard FAs implemented with either TFETs or CMOS PTM-MGs are discussed here, the proposed test-bench can be used to benchmark other single-ended FA topologies.

Fig.5 reports the worst case delay for sum (S) and carry-out (Co) output versus V_{DD} . The delay of the Co is calculated independently for different cases: P^1 and P^0 (propagation of 1 or 0), D (delete), G (generate). The propagation delay (t_{prop}), corresponding to the worst case delay between $Co(P^1)$ and $Co(P^0)$, is the bottleneck for a n-bit FA in the Ripple-Carry-Adder (RCA) implementation [7], since the theoretical minimum clock-period T_{bit} is given approximately by $n \times t_{prop}$. The *Energy versus Propagation Delay* computed at $T_{bit} = 100$ ns for 1-bit FA blocks is reported in **Fig.6**. Here, for simplicity T_{bit} is assumed constant over the full V_{DD} range instead of adjusting it to the minimum value fixed by t_{prop} . Taken as a single instance, the TFET FA features a much lower minimum energy point (< 10 aJ/cycle), and the CMOS FA is more energy efficient only in fast applications requiring $t_{prop} < 160$ ps.

In **Fig.7**, 1-bit FA simulation results are projected to 32-bit RCAs to compute the minimum energy necessary to complete a sum operation (E^{Op}). Such projection is performed by separating the static and dynamic energy components (SE and DE, respectively) for any V_{DD} . Then the SE is weighted relying on the minimum T_{bit} at which the 32-bit RCA can operate, whereas the DE is essentially independent of T_{bit} . In the CMOS case, there is a *Minimum Energy Point* (MEP) at $V_{DD}^{MEP,CMOS} = 250$ mV, since a further scaling of V_{DD} below V_{DD}^{MEP} results in a higher energy consumption because the SE contribution becomes dominant. At any V_{DD} , the E^{Op} is much lower in the TFET implementation (it is dominated by the DE component down to $V_{DD} = 200$ mV), basically because the increase of t_{prop} is less pronounced than the reduction of the leakage with the V_{DD} scaling. Thus, the MEP in the 32-bit TFET RCA corresponds to a lower V_{DD} ($V_{DD}^{MEP,TFET} = 150$ mV).

V. Conclusions — A III-V TFET technology platform has been benchmarked against the predictive models for 10 nm node CMOS FinFETs considering Full-Adders as test circuit. Aggressively scaled III-V based TFETs allow for much better energy efficiency at low V_{DD} .

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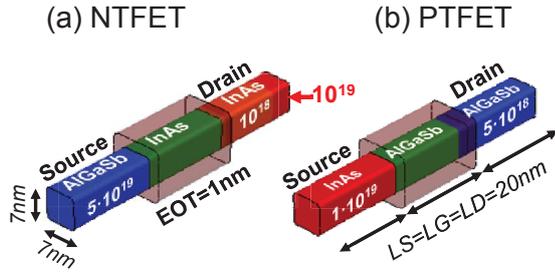


Fig.1: AlGaSb/InAs TFET structures implemented in the TCAD to reproduce the full-quantum simulations of the devices proposed in [2]. Dimensions, materials, and doping levels are the same as in [2]. Doping levels are in cm^{-3} .

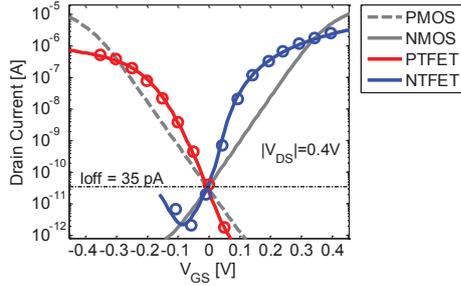


Fig.2: Simulated I_D - V_{GS} for the TFETs in Fig.1 (red and blue lines) and for the 10 nm node CMOS FinFETs of the predictive models [6] (grey). The full-quantum TFET simulations from [2] are indicated by bullets. $V_{DS}=0.4V$.

Parameter	$\text{Al}_{0.05}\text{Ga}_{0.95}\text{Sb}$	InAs
E_G (eV)	1.04	0.59
χ (eV)	4.01	4.9
$A_{\text{path}}(\text{cm}^{-3}\text{s}^{-1})$	$1.51 \cdot 10^{20}$	$1.44 \cdot 10^{20}$
$B_{\text{path}}(\text{V/cm})$	$9.54 \cdot 10^6$	$2.94 \cdot 10^6$
$N_C^{\text{DOS}}(\text{cm}^{-3})$	$1.26 \cdot 10^{18}$	$5.22 \cdot 10^{17}$
$N_V^{\text{DOS}}(\text{cm}^{-3})$	$1.8 \cdot 10^{19}$	$6.6 \cdot 10^{18}$

Table.I: Parameters used in the TCAD for the calibration of the AlGaSb/InAs hetero-junction against the full-quantum simulations in [1,2]. Energy Gap (E_G) and Electron Affinity (χ) are extracted from [1], BiBT model parameters (A_{path} and B_{path}) are computed using effective masses from [9]. Effective conduction/valence band density of states used as fitting parameters.

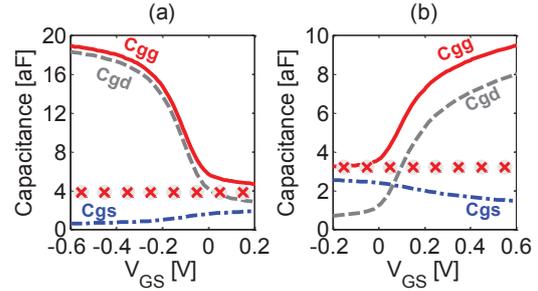


Fig.3: Simulated TFET capacitances versus V_{GS} at $V_{DS} = 0V$ for the (a) PTFET and (b) NTFET. The symbols in the plot represents the total gate capacitances (C_{GG}) reported in [2], estimated as $C_{GG} = (Q_{ON} - Q_{OFF})/V_{DD}$.

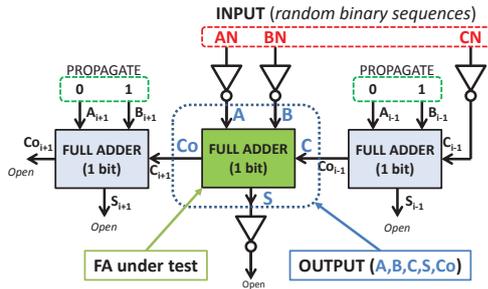


Fig.4: Test-bench for extracting the figures-of-merit of a single Full-Adder block (FA). The FA under test (green) is placed in a framework including driving and loading blocks and the input sequences are randomly generated to emulate normal operating conditions.

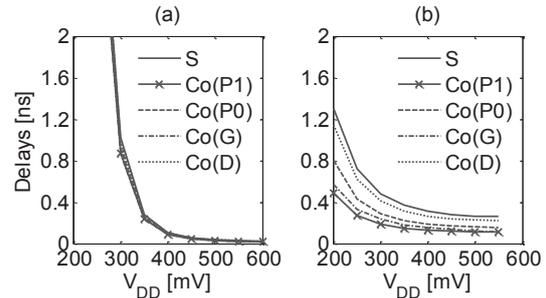


Fig.5: 28T (minimum area) standard FA (topology reported in [7]), sum (S) and carry-out (Co) delays as a function of V_{DD} . (a) CMOS, (b) TFET. The delay of the Co is reported for different cases: P1/P0 (propagation of 1/0), D (delete), G (generate).

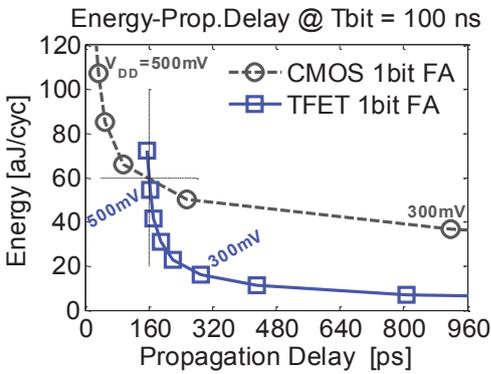


Fig.6: Average Energy-Propagation Delay plot computed at $T_{\text{bit}} = 100 \text{ ns}$ for single FA blocks. TFET FA features a much lower minimum energy point ($<10 \text{ aJ/cycle}$). The CMOS FA is more energy efficient only in fast applications requiring $t_{\text{prop.}} < 160 \text{ ps}$. Points correspond to different V_{DD} (step 50 mV).

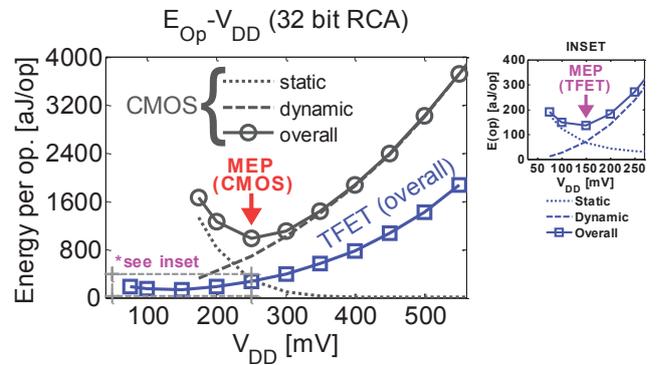


Fig.7: Minimum Energy per Operation (MEO) as a function of V_{DD} projected for 32-bit Ripple-Carry-Adders (RCAs). For the TFET implementation we report only the overall energy since it is dominated by the dynamic energy for $V_{DD} > 200 \text{ mV}$ (see the inset reporting the single components).

Improved Voltage Gain in Mechanically Stacked Bilayer Graphene Field Effect Transistors

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1. Introduction

Graphene has attracted much attention of the device research community since its earliest experimental demonstrations as graphene effective field effect transistors (GFETs) [1]. Analog circuit applications have been recently proposed for GFETs, both theoretically [2][3] as well as experimentally [4]. High voltage gain, an essential requirement in such circuits, requires good transistor output current saturation, something that is lacking in typical single layer graphene FETs. Several approaches have been proposed in literature to improve the saturation behavior, such as Bernal stacked bilayer graphene [5], which is difficult to achieve in chemical vapor deposited (CVD) graphene. In this paper, we explore the performance potential of mechanically stacked bilayer GFETs (BIGFETs) made from CVD graphene.

2. Device fabrication

Thermally oxidized (85nm, p-doped) silicon wafers were used as the starting material. The surface was cleaned and in-house grown CVD graphene monolayers were transferred using an electro-delamination method with PMMA support layer [6]. This PMMA layer was then dissolved in acetone, followed by subsequent transfer of a second monolayer graphene sheet on top of it, resulting in a randomly oriented bilayer stack. Fig. 1a shows the optical micrograph of the stacked bilayer graphene. Channels were patterned using oxygen plasma based reactive ion etching, followed by thermal deposition of 10 nm/90 nm Cr/Au contact pads. 10 nm SiO₂ was e-beam evaporated as the top gate oxide, followed by deposition of 100 nm Al gate deposition and a subsequent lift off in acetone.

3. Results & discussion

Fig. 1b shows Raman spectra in monolayer and bilayer regions. It can be seen that 2D and G bands show a distinct behavior in bilayer as compared to monolayer graphene with an enhancement in G band intensity and a broadened 2D band, without showing the typical fingerprint of Bernal stacked bilayer graphene [7]. This indicates weak electrostatic coupling between the two stacked layers. Fig. 2a shows a micrograph of a fabricated device. Electrical characterization was carried out in ambient conditions. Fig. 2b shows the output and transfer characteristics of a device at zero back gate voltage (V_{BG}). Fig. 3 compares the performance of two of our devices with literature reports of monolayer and Bernal stacked bilayer GFETs [5]. At each back gate voltage, several transfer and output characteristics were

measured and maximum DC transconductance ($g_{m,max}$) as well as minimum output conductance ($g_{d,min}$) values were extracted. The $g_{m,max}$ (Fig. 3a) values follow a trend similar to that of monolayer GFETs whereas $g_{d,min}$ (Fig. 3b) values were of lower magnitude at increasingly negative V_{BG} . This results in an improved voltage gain figure of merit, ranging between 2.5 to 28.84, with an average gain between 6 and 10, without any specific device optimization. Table 1 summarizes our observations compared to the literature data. Using the simple model proposed in [8], the carrier densities were calculated from transfer characteristics. It was found that the peak carrier density in a BIGFET channel increases with applied V_{BG} and is of the order of $\sim 10^{13}$ cm⁻² at $V_{BG} = -60$ V as compared to $\sim 10^{12}$ cm⁻² at $V_{BG} = 0$ V. An increased carrier density would mean a decrease in carrier velocity in the channel, which might be one of the possible reasons for enhanced saturation tendency observed in these devices. These preliminary results indicate that stacked bilayer graphene can be a potential candidate for analog circuits paving the way for the implementation of integrated high frequency nano-transceivers.

This work is supported by the German Research Foundation (DFG, LE 2440/1-1 and 2-1) and by the Spanish Ministry of Science & Innovation (RUE CSD2009-00046 and TEC2010-15765).

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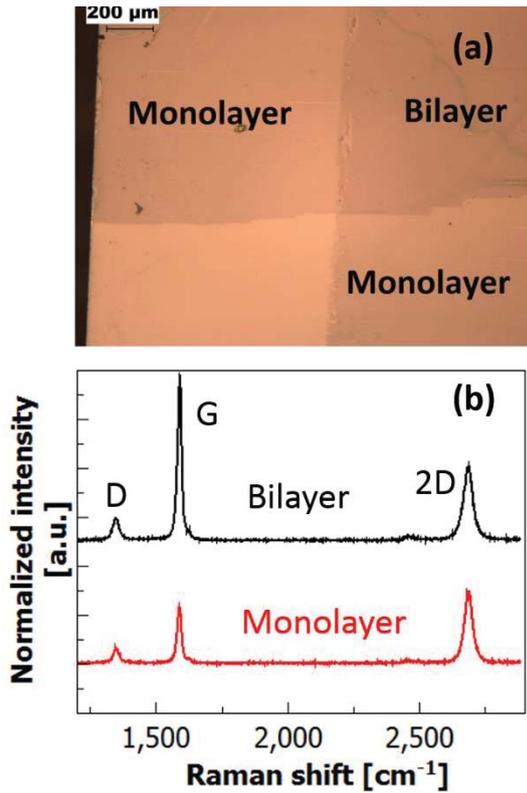


Fig.1: (a) Optical micrograph of mechanically stacked bilayer graphene. (b) Raman spectra of stacked bilayer graphene compared to monolayer graphene.

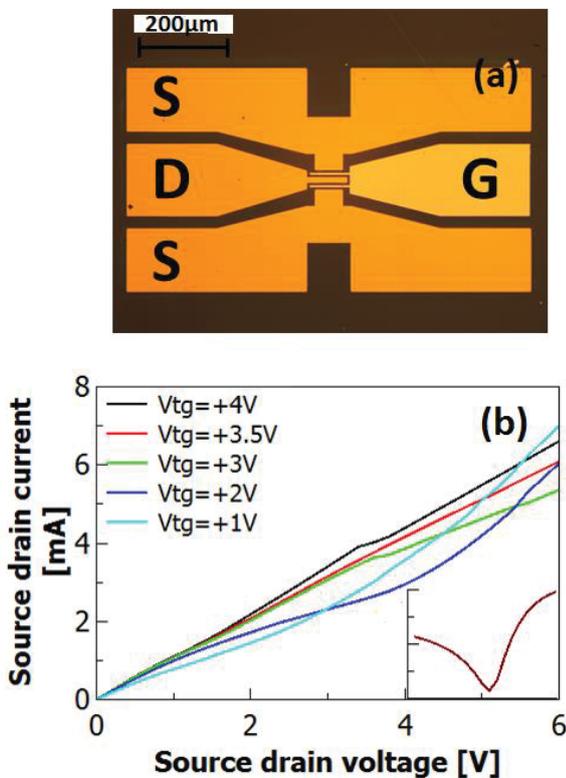


Fig.2: (a) optical micrograph of a BIGFET. (b) Output characteristics and (inset) transfer characteristics (at a source drain bias of 0.1V) of a typical device at $V_{BG}=0V$.

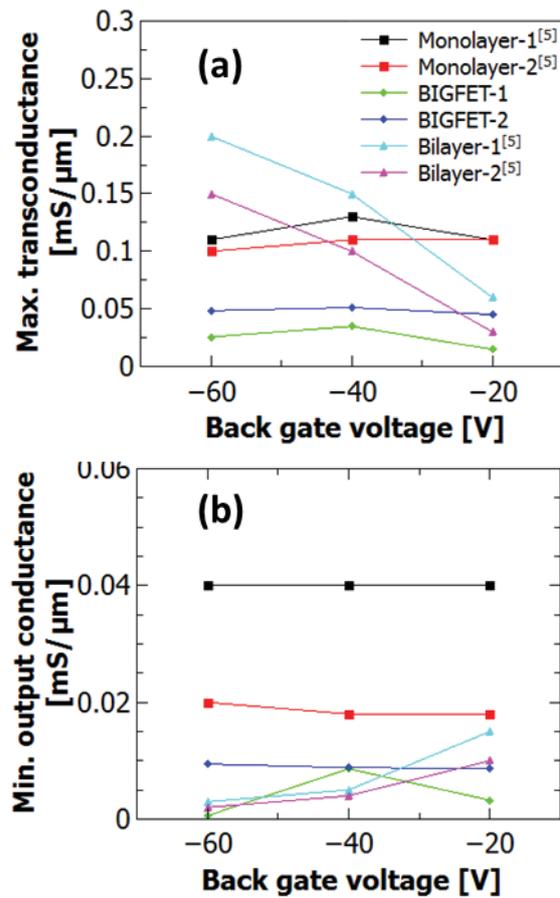


Fig.3: (a) Maximum DC transconductance and (b) minimum output conductance values measured at different back gate voltages for BIGFETs with a gate length of 12 μm and channel width of 60 μm. The data normalized to unit width is compared against monolayer and bilayer GFETs reported literature [5]. Both the monolayer and bilayer graphene in [5] were mechanically exfoliated whereas our devices were fabricated from in-house grown CVD graphene. The magnitude of minimum output conductance values was observed to be closer to Bernal stacked bilayer GFET case.

Table 1: Comparison of maximum intrinsic voltage gain figures for various device types

Device type	Maximum intrinsic gain (dB)
Monolayer GFET	6[5]
BIGFET	Between 2.5 to 28.84
Bilayer GFET	35[5]

Simulation Study on the Feasibility of Si as Material for Ultra-Scaled Nanowire Field-Effect Transistors

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1. Abstract

We present a simulation framework which allows thorough performance evaluation of ultra-scaled devices. Our simulation approach is based on the full solution of the Boltzmann transport equation (BTE) on subbands including all relevant scattering mechanisms. We employ the simulation framework to investigate the performance limits of silicon-based technology for ultra-scaled field-effect transistors in logic applications.

2. Modeling Tools

The simulation framework is based on our previous work on mobility modeling in nano-device channels [1, 2, 3, 4], where we developed the representation of the full scattering operator in \mathbf{k} -space based on either an effective-mass or a $\mathbf{k}\cdot\mathbf{p}$ subband structure. We have also extended the above methods to non-Si materials and to include entire devices using a channel-slicing technique combined with low-field coupling [5]. However, low-field coupling is not sufficient to model current at high source-drain bias and, in particular, the on-current of a device.

To enable the simulation of the high- V_{DS} characteristics of a device, one additional ingredient to the simulation framework has been developed: a subband-BTE solver. The solver operates in *phase space*, i.e. tensor product of real and \mathbf{k} -space.

The phase-space formalism allows simulation on any numerically obtained dispersion relation, such as one provided by a $\mathbf{k}\cdot\mathbf{p}$ or tight-binding subband structure tool. This accurately captures a number of band structure effects: (i) anisotropy of band structure, (ii) non-monotonicity or *subband warping* commonly occurring in valence subbands, and (iii) strain effects on subband energies and curvatures within $\mathbf{k}\cdot\mathbf{p}$ theory. Non-polar phonon scattering (acoustic and optical), polar-optical phonon scattering, remote phonon scattering, ionized impurity scattering, remote Coulomb scattering, and surface roughness scattering can be included.

All the involved components - subband structure, scattering operator, subband-BTE, self-consistent iteration - have been implemented in the simulators Minimos-NT [6] and VSP [7] as provided by GTS Framework [8].

3. Results

We examined Si nanowire transistors of both n and p-type, as depicted in Fig. 1. The channels are 4 nm wide, 8 nm long, and fitted with as $\text{SiO}_2/\text{HfO}_2$ /metal gate stack. The channel orientation was chosen to be $\langle 110 \rangle$

for both devices, as this has been reported to improve channel conductivity [9]. The transfer characteristic of both devices was computed at a source-drain bias of 0.7 V. The calculations were done self-consistently with the electrostatic potential. For both devices, the characteristic was obtained (i) for an unstrained device including scattering (non-polar phonons, impurities, surface roughness), (ii) for the ballistic limit of the unstrained device, and (iii) for a device with 1.5 GPa stress applied along the channel axis - *tensile* for nMOS, *compressive* for pMOS.

In both cases the applied stress increases the output current, although the question remains whether there is a mechanically stable way to apply compressive stress to a nanowire channel. However, even with the increase, the pMOS current is below that of the nMOS device by roughly a factor of two. To achieve a balanced CMOS circuit, two pMOS transistors are required to complement one nMOS.

4. Conclusion

We presented a novel computational framework that includes all relevant band structure, scattering, and high-field transport effects in a self-consistent simulation. The purpose of the developed framework is the predictive evaluation of device current at high source-drain biases. The capabilities of the framework have been demonstrated on the examples of next generation Si nMOS and pMOS transistors.

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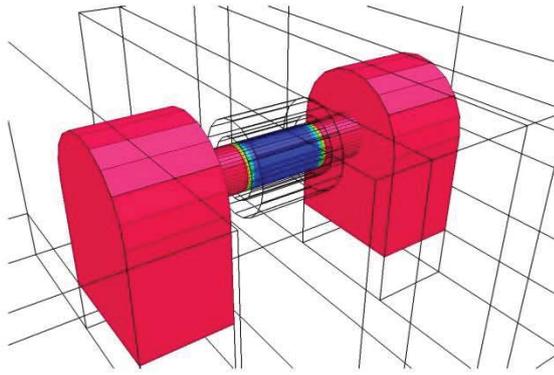


Fig. 1: Test device - a gate-all-around nanowire transistor; the gate stack is comprised of $\text{SiO}_2/\text{HfO}_2$ layers and a metal gate. The colors indicate doping which is $1 \times 10^{20} \text{ cm}^{-3}$ in the source and drain regions and $1 \times 10^{12} \text{ cm}^{-3}$ in the channel. The channel orientation is $\langle 110 \rangle$.

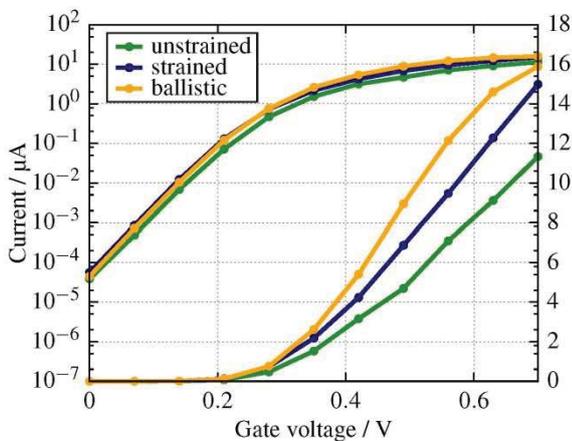


Fig. 2: Transfer characteristic of the n-type device at $V_{\text{DS}} = 0.7 \text{ V}$; applying tensile stress of 1.5 GPa along the $\langle 110 \rangle$ channel reduces the transport mass and thus increases on-current. The unstrained ballistic current is also shown for reference.

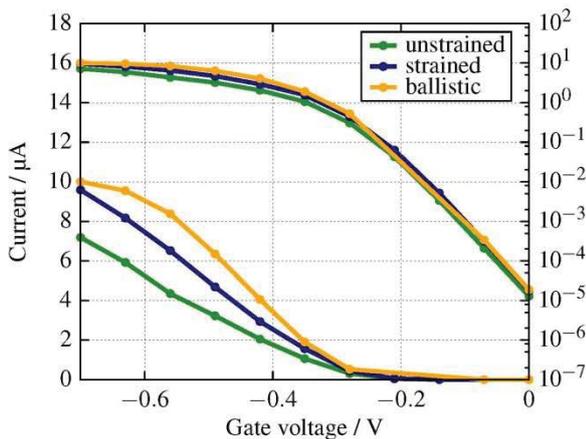


Fig. 3: Transfer characteristic of the p-type device at $V_{\text{DS}} = -0.7 \text{ V}$; applying compressive stress of 1.5 GPa along the $\langle 110 \rangle$ channel reduces the transport mass and thus increases on-current. The unstrained ballistic current is also shown for reference. Although $\langle 110 \rangle$ channel orientation improved pMOS performance, the improvement is not sufficient to match the nMOS device.

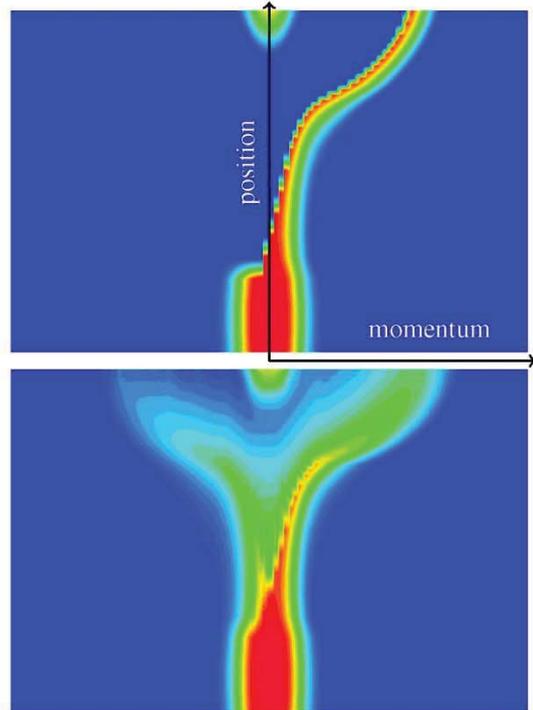


Fig. 4: Phase-space plot of the distribution function in the lowest subband for the n-type transistor; gate bias is set to 0.05 V above threshold. The ballistic (top) and dissipative (bottom) transport regimes are shown. The horizontal axis corresponds to momentum or \mathbf{k} , while the vertical axis corresponds to the position along the channel.

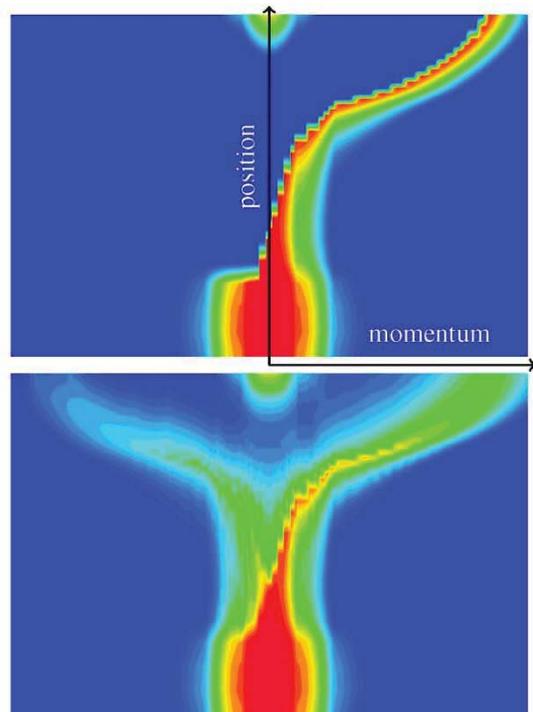


Fig. 5: Same as Fig. 4 but for the p-type device

GDNMOS: A New High Voltage Device for ESD Protection in 28nm UTBB FD-SOI Technology

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Abstract— We propose a novel device (GDNMOS: Gated Diode merged NMOS) fabricated with 28nm UTBB FD-SOI high-k metal gate technology. Variable electrostatic doping (gate-induced) in diode and transistor body enables reconfigurable operation, in particular in thyristor mode. This innovative architecture demonstrates excellent capability for high-voltage protection while maintaining a latch up free behavior.

Index Terms - Electrostatic Discharges, FD-SOI, Gated Diode, MOSFET, Thyristor, SOI, CMOS

1. Introduction

Recent advances in Fully Depleted SOI (FD-SOI) technology [1] continue to shrink the design window of ElectroStatic Discharge (ESD) protection devices, reducing supply voltage V_{dd} and decreasing breakdown voltage V_{Br} . This window is highly dependent on the type of devices to be protected, as well as on the region of operation. Our previous studies have been conducted on thin film BiMOS device for protection of circuits operating in typical voltage range for FD-SOI technology [2, 3, 4]. In this work, we present an original structure for high voltage protection that combines diode and MOSFET mechanisms. Electrical measurements prove the flexibility, functionalization and robustness of the GDNMOS. 3D TCAD simulations reveal the details of the operation mechanisms.

2. Device structure and properties

GDNMOS is composed of a typical FD-SOI nMOSFET merged with an FD-SOI p-i-n gated diode. There is a common n-type area which acts as the diode cathode and as the MOSFET drain. The ultrathin bodies of the diode and transistor can be electrostatically doped (N^+ or P^+ , by attracting different types of carriers in the ‘intrinsic’ region below the gate) via the gates or back-plane bias. Our main purpose is to take advantage of such reconfigurable behavior for emulating a PNPN thyristor structure: positively biased P^+ anode, floating N^+ drain, P MOSFET body, grounded N^+ source (Fig. 1). Test devices (Fig. 2) were fabricated with the 28nm FDSOI STMicroelectronics process featuring an ultrathin silicon film of 7nm, ultra-thin BOX of 25nm, high-k metal gate stack and p-type backplane (p-BP). The devices were fabricated with different gate stack options: Standard Gate (SG, EOT=1.1nm) and Extended Gate (EG, EOT=3.4nm). In DEV1, 2, 3 structures the MOS gate and the diode gate were interconnected, while in DEV4, 5, 6 they were independent. In the mixed gate stack devices, the gate oxide of the diode was always selected to be thick (EG), for increased robustness to the stress applied to anode. Minimum process-compliant gate dimensions were selected and compared to longer gates.

3. Simulation results

The 28nm FD-SOI GDNMOS was meshed in 3D (Fig. 1) for different gate stack configurations. We consider phonon scattering, Coulomb scattering in doped materials, and mobility degradation due to high field saturation and high temperature. Other active modules include avalanche model as well as Auger recombination model. For the simulation study, the surge is an ACS stress with 1A max current and 100ns rise time, which is equivalent to the transmission line pulse (TLP) test for human body model (HBM). Fig. 3 shows typical I-V characteristics resulting from ACS simulation. The differentiation between the mixed SG-EG gate stacks as well as EG-EG gate stacks is observed as well as the effect of floating vs grounded/biased gate terminals. At the end of the stress, current density reaches the maximum value with conduction through the whole film (volume inversion, Fig.3).

4. Measurements and discussion

The devices were tested in static and TLP modes under different conditions. TLP measurements had duration of 100ns or 10ns and native or 10ns rise time. The stress was applied on anode, while cathode was grounded. The gates were either grounded or floating. Our primary goal is to investigate the ESD behavior of the various structures and evaluate the efficiency of the floating-body (without base contact) lateral thyristor.

For the first type of devices (Fig. 4, 5) with the two gates connected, we observe clear snapback characteristics. The fluctuations on I-V response are attributed to the coupling during the transient TLP stress between the two different gate stacks. This effect is not observed in devices (Fig. 6,7) that have separate MOS and diode gates, even for identical biasing conditions. For these structures there is no systematic differentiation between 100ns and 10ns TLP I-V curves. No strong snapback behavior is observed primarily due to the lack of direct control on the Emitter-Base p-n junctions of the Lateral Bipolar Junction Transistors (LBJT between source and drain) as well as the relatively high doping of LBJT base in the merged area. The selection of gate stack affects strongly the breakdown voltage of the device (Fig. 8) with EG gate stack devices exhibiting higher breakdown voltage and lower leakage (Fig. 9). In terms of performance DEV5, 6 provide the best performance with higher I_{t2} , lower leakage and higher breakdown voltage. Additionally, by utilizing variable biasing on MOS gate (MG) we can achieve different behavior during a TLP stress as seen in Fig. 9. We show that doping calibration as well as gate and backplane biasing schemes modulate the thyristor operation leading to further improvement of the ESD stress responses. We benchmark its performance with that of alternative devices proposed for ESD protection in ultrathin FD-SOI.

In summary, the GDNMOS shows promising characteristics and remarkable versatility for adoption in the FD-SOI technology.

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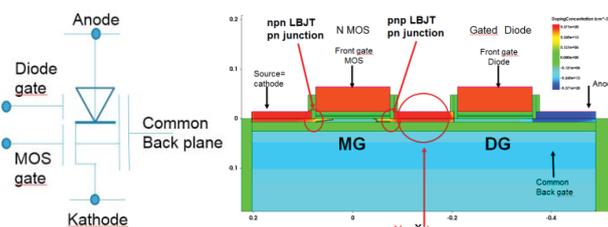
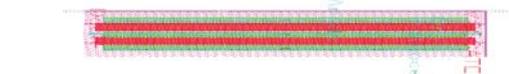


Figure 1: Schematic (left) and cross-section (right) of GDNMOS structure



	MOS Gate	Diode Gate	Lg1	Lg2	MG-DG2	Biasing
DEV1	SG	SG	5nm	5nm	conn	2V
DEV2	SG	EG	10nm	50nm	conn	4V
DEV3	EG	EG	50nm	50nm	conn	4V
DEV4	SG	SG	5nm	5nm	separ	2V
DEV5	SG	EG	10nm	50nm	separ	4V
DEV6	EG	EG	50nm	50nm	separ	4V

Figure 2: **Top:** typical GDNMOS layout. **Bottom** different device configurations fabricated.

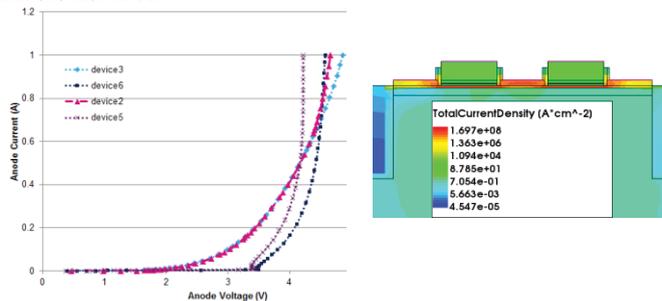


Figure 3: **Left:** ACS I-V TCAD simulation for devices 2, 3, 5 and 6. **Right:** Current density extracted at the end of ACS stress for device 6, grounded gates. Volume conduction is visible.

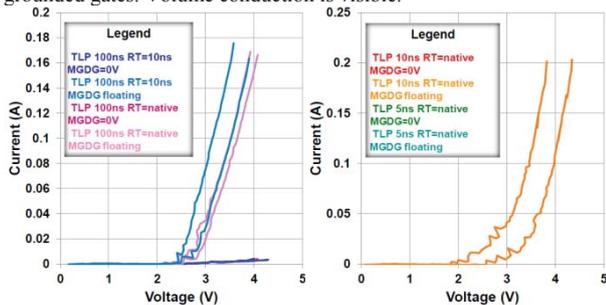


Figure 4: Device1 TLP measurements for different rise times: **Left:** 100ns duration time. **Right:** 10ns duration time.

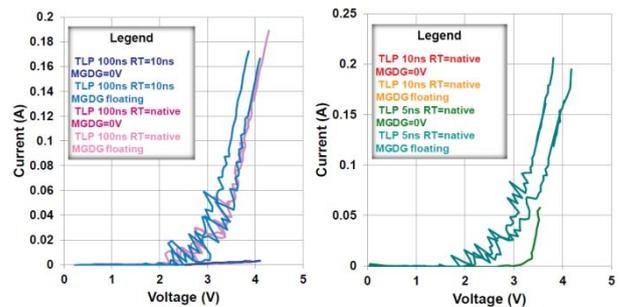


Figure 5: Device2 TLP measurements for different rise times: **Left:** 100ns duration time. **Right:** 10ns duration time.

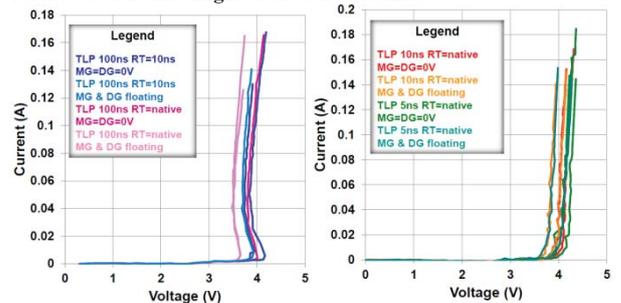


Figure 6: Device4 TLP measurements for different rise times: **Left:** 100ns duration time. **Right:** 10ns duration time.

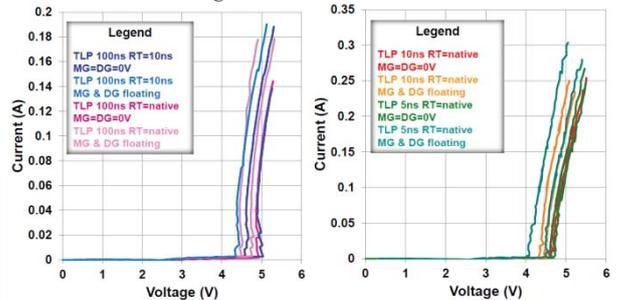


Figure 7: Device6 TLP measurements for different rise times: **Left:** 100ns duration time. **Right:** 10ns duration time.

	Vt1	It1	It2	Vhold	V _{BR}
DEV1 GND	NA	NA	<20mA	NA	3.1V
DEV1 FLT	NA	NA	<180mA	NA	NA
DEV2 GND	NA	NA	<20mA	NA	4.2V
DEV2 FLT	NA	NA	<180mA	NA	NA
DEV3 GND	NA	NA	<20mA	NA	4.8V
DEV3 FLT	NA	NA	<120mA	NA	NA
DEV4 GND	4V	NA	>160mA	4V	4.3V
DEV4 FLT	4V	NA	>140mA	4V	NA
DEV5 GND	3.5V	NA	>160mA	3.5V	4.2V
DEV5 FLT	3.5V	NA	>140mA	3.5V	NA
DEV6 GND	4.5V	NA	>160mA	4.5V	4.9V
DEV6 FLT	4.3V	NA	>140mA	4.3V	NA

Figure 8: Extracted results for different gate biasing and configurations. We observe the improved performance with last 3 implementations. These devices exhibit higher I_{C2}, improving robustness during an ESD event.

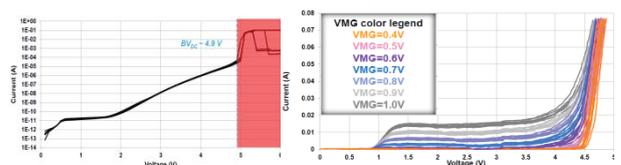


Figure 9: Device6. **Left:** DC sweep with grounded MG and DG for breakdown voltage extraction. **Right:** TLP 100ns with different MG biasing.

Operation of Suspended Lateral SOI PIN Photodiode with Aluminum Back Gate

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1. Introduction

A wide interest emerges, in environmental and biomedical monitoring systems, for high-responsivity photodetectors embedded in CMOS integrated circuits. In SOI technology, a thin-film lateral PIN photodiode suspended on a micro-hotplate platform was studied in [1]. Its intrinsic (I) region with length L_i corresponds in practice to a weakly doped P region (i.e. P⁺PN⁺).

In the present work, an additional 1- μ m thick Aluminum (Al) layer was deposited on the backside of the samples. A schematic cross-section of the suspended lateral SOI PIN photodiode with Al back gate is depicted in Fig.1. Three photodiode geometries are specified in Table I, i.e. M5, M10 and M20 with intrinsic lengths $L_i = 5, 10$ or $20 \mu\text{m}$ and 6, 4 or 2 finger PIN diodes interdigitated in parallel, respectively.

The operation of the PIN photodiode is strongly influenced by the depletion condition present in the I-region, where carriers generated by light radiation can be collected more efficiently thanks to the fully-depleted (FD) regime induced by positive back-gate voltage and reverse anode bias [2]. The Al back gate is also expected to act as a reflector and influence light absorption in the device active layer, thanks to its excellent reflection property across the visible spectrum.

In this work we investigate the performances of the suspended lateral SOI PIN photodiode influenced by Al back gate, based on measurements and simulations.

2. Experimental Measurements

Fig.2 presents the measured photocurrents, normalized for one finger of each suspended photodiode, as a function of the applied back-gate voltage (V_G), under 590 nm incident light and different reverse anode bias (V_D). V_G modifies the operation mode of the active Si film back interface, from accumulation to depletion and inversion for negative to positive bias. It is clear that the photocurrents are modulated by the vertical depletion width (to the first order, as the square root of positive V_G above flat-band voltage) and achieve a maximum under FD condition whose value is directly proportional to L_i as is expected from carrier collection over the full I-region volume.

The photocurrents also vary with V_D but only in the non-fully-depleted (NFD) intermediate regime. In this case, Fig.3 shows that at constant $V_G - V_D$, the photocurrent indeed increases with the lateral depletion width L_{zd} at the P⁺N⁺ blocked junction, i.e. roughly with the square root of $-V_D$ (as indicated by black dashed curve in Fig.3). This cannot occur anymore once FD is

achieved by increasing V_G . Similar behavior was observed at all wavelengths in the visible spectrum.

Under FD condition, responsivities of M20 at 3 different wavelengths (490, 590 and 760 nm) are 0.07, 0.1, 0.05 A/W respectively. Compared to the photodiodes lying on substrate [1], 2~3 \times higher responsivity has been achieved in the suspended photodiode with backside Al deposition, thanks to the FD condition achieved by back-gate bias and excellent optical reflection from Al as a back reflector.

3. Numerical Simulation Analysis

To further investigate and analyze our results, numerical simulations were conducted in Atlas [3] on a 2-D physical device model with $L_i = 10 \mu\text{m}$ (Fig.4). Fig.5 confirms the 1st-order interpretation of our measurements of Fig.2. Depending on biases, the I-region can indeed feature an undepleted zone (NFD) and two main depletion zones, one arising from PN⁺ junction (FD₁), one from BOX interface (FD₂): (a) negative V_G suppresses FD₂, (b) positive V_G induces FD₂ and (c) full depletion is achieved under sufficiently positive V_G . However from cases (a) and (b), we observe that V_G also influences FD₁ extension while from (b) and (d), reverse V_D modulates FD₂. 2-D modeling is thus required to fully quantify our photocurrent measurements in all operation regimes (Fig.2 and 3).

Light absorption in the thin Si film was also simulated within the 450-900 nm range, setting the optical index and thickness of all the device materials from ellipsometry measurements. Fig.6 compares the numerical results for the suspended diode with Al back mirror and for the diode lying on substrate. Compared to the on-substrate diode, light absorption in the suspended diode is boosted in specific wavelength ranges, e.g. around 500, 600 and 770 nm, leading to an abrupt responsivity increase as observed in our measurements.

4. Conclusions

With Al deposition on the backside of SOI PIN photodiodes suspended on a micro-hotplate platform, the voltage applied to the back gate can modify the depletion condition in the I-region. FD condition achieved by positive back-gate bias maximizes the device optical response. Besides, back Al acts as a reflector, which for specific wavelength ranges, can significantly boost the device responsivity. A ~3 \times improvement has been achieved at 590 nm in the measurements. Further device simulations are conducted to fully validate and optimize the device performance and potential improvement.

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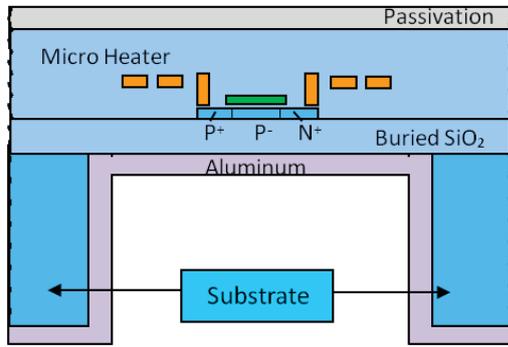


Fig.1: Cross sectional view of SOI diode suspended on a micro-hotplate platform with Al back gate.

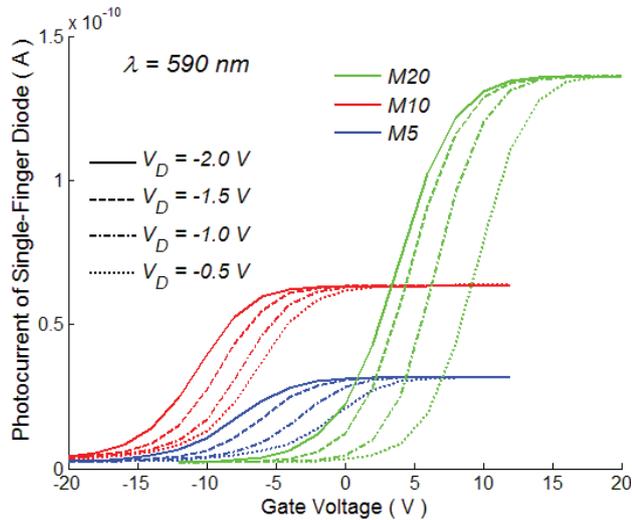


Fig.2: Normalized photocurrent for single-finger diode as a function of applied back-gate voltage with 590 nm illumination ($8.92 \times 10^{-3} \text{ W/cm}^2$), under different reverse anode bias V_D .

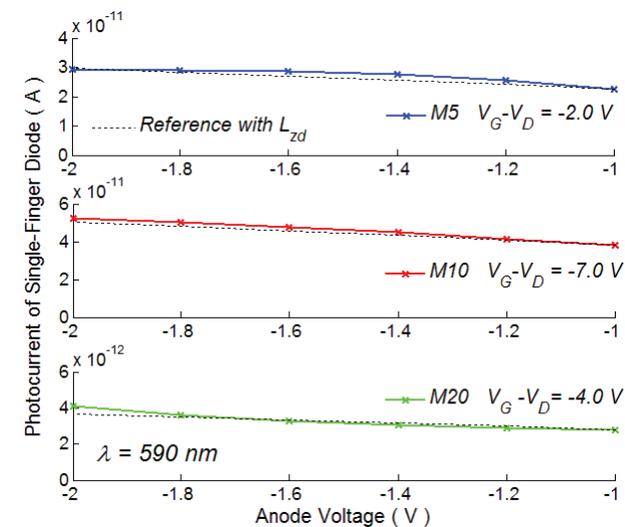


Fig.3: Photocurrent for single-finger diode as a function of reverse anode voltage, under non-fully-depleted operation at proper back-gate bias V_G .

TABLE I
PHOTODIODE GEOMETRIES

Devices	L_i (μm)	Fingers	W_{fingers} (μm)	Effective area ($\mu\text{m} \times \mu\text{m}$)	Total area ($\mu\text{m} \times \mu\text{m}$)
M5	5	6	60	30×60	58×60
M10	10	4	60	40×60	60×60
M20	20	2	60	40×60	52×60

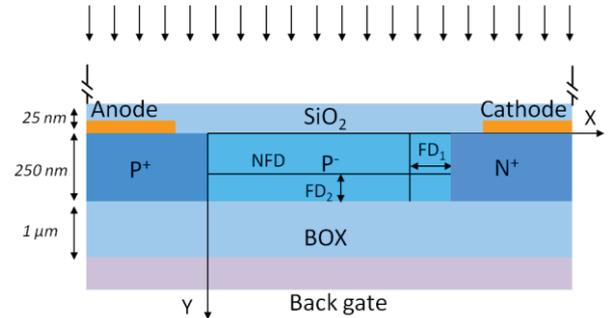
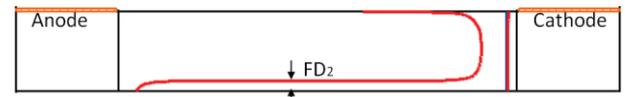


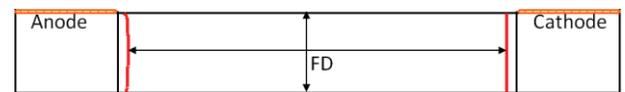
Fig.4: Schematic view of lateral SOI PIN diode under study: FD_1 = region depleted by reverse anode bias, FD_2 = region depleted by back-gate voltage, NFD = undepleted part.



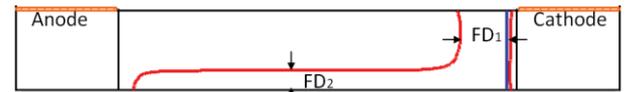
(a) $V_G < 0.0 \text{ V}$, $V_D = 0.0 \text{ V}$



(b) $V_G > 0.0 \text{ V}$, $V_D = 0.0 \text{ V}$



(c) $V_G \gg 0.0 \text{ V}$, $V_D = 0.0 \text{ V}$



(d) $V_G > 0.0 \text{ V}$, $V_D < 0.0 \text{ V}$, with the same $V_G - V_D$ as (b)

Fig.5: Depletion region edges (red curves) as a function of V_G and V_D . The blue curve denotes the P^+N^+ junction.

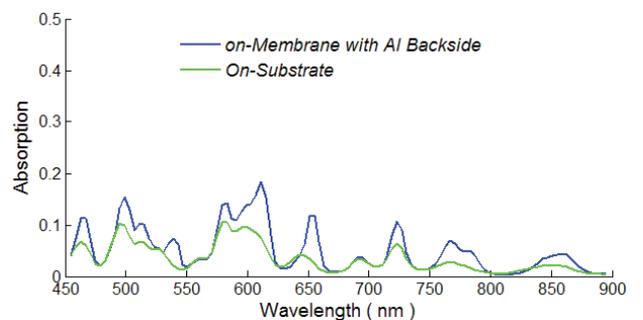


Fig.6: Light absorption average (bandwidth = 10 nm) of the suspended diode with Al deposition at backside (blue curve) and the on-substrate diode (green curve) with $L_i = 10 \mu\text{m}$.

RF SOI CMOS Technology on 1st and 2nd Generation Trap-Rich High Resistivity SOI Wafers

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1. Introduction

During last decades, CMOS technology scaling-down has enabled millimeter wavelength operation and low-cost integration of digital, analog and RF systems on the same wafer for system-on-chip or in system-in-package applications [1-3]. In this context, the most special advantage of SOI CMOS compared to bulk Si is the availability of high-resistivity silicon (HR-Si) substrate to achieve low crosstalk between passive and active devices and high-quality passive elements thanks to effective reduction of substrate coupling and losses in RF circuits [4-5]. Moreover, SOI technology has simpler fabrication process than bulk and hence is more cost-effective. However, HR-SOI substrate suffers from resistivity degradation due to the formation of parasitic surface conduction (PSC) beneath the buried oxide layer (BOX) [6-9] due to fixed oxide charges (Q_{ox}) within the oxide. One of the most efficient techniques to overcome this problem is to introduce a trap-rich layer at the Si/SiO₂ interface compatible with industrial SOI wafer production and thermal budget of standard CMOS process [8] which captures the free carriers forming the PSC and thus makes the substrate retrieving its nominal high resistivity. Since thermal resistance is proportional to the square root of the BOX thickness, BOX thinning is desired to improve thermal properties. Moreover, threshold voltage control by means of back-gate biasing voltage V_{bg} could be a useful feature provided by thin BOX in fully depleted devices [10]. Therefore, trap-rich HR-SOI with thinner BOX could be considered as a promising candidate.

2. Devices description

In this work two types of trap-rich HR-SOI substrates denoted eSi1 and eSi2 as 1st and 2nd generations with 400nm and 200nm-thick BOX respectively and one standard HR-SOI with 1 μ m BOX (all provided by SOITEC) are characterized and compared for non-linearity effects and DC/RF MOSFET behaviors. The test structure devices include 0.52 μ m-thick CPW lines and PD SOI nMOSFETs fabricated using TowerJazz 0.18 μ m SOI CMOS process. The dimensions of the CPW lines are respectively 20, 18 and 100 μ m for the central conductor, slot space and ground plane. The PD SOI MOSFETs have 145 nm of thin active silicon film of 10 Ω -cm resistivity and 5 nm of gate oxide thickness. The studied RF body-tied MOSFET has a 0.24 μ m gate length (L_g) with 16 gate fingers of 2 μ m each (W_f). The studied single finger DC MOSFET has a 0.26 μ m of gate length (L_g) with 1.5 μ m width (W_f).

3. Measurement results

A. PD SOI RF and DC MOSFETs

The DC/RF on-wafer measurements have been

done using an Agilent N5242A for high-frequency measurement from 10 MHz to 26.5 GHz and Agilent B1500 for DC measurements. As shown in Fig. 1, the I_D - V_G and g_m - V_G curves in linear regime for DC transistor on the 3 different wafers are very close. To eliminate the threshold voltage variations effect and fairly compare these results, g_m/I_D ratio versus $I_D/(W/L)$ curves for the same transistors are plotted in Fig. 2. Similar DC characteristics are obtained for all substrate types. Fig. 4 shows a good similarity of current cut-off frequency f_T as one of the main RF figures of merit as expected on all 3 wafers.

B. Substrate Effective Resistivity and Harmonic Distortion

By means of a 2100 μ m-long CPW line S-parameters measurement, the effective resistivity (ρ_{eff}) and total loss (α) on the 3 different types of substrate, plus quartz, considered as the best reference, have been extracted. Fig. 4 shows that as stated before, due to the formation of PSC, the standard HR SOI substrate loses its nominal high resistivity and shows an effective resistivity of only 200 Ω .cm, whereas in 1st and 2nd generations of trap-rich HR-SOI, the substrate has kept its high resistivity of more than 2 k Ω .cm and 3 k Ω .cm respectively, after CMOS processing. The interesting point that can be seen in this figure is that despite its thinner BOX, the eSi2 substrate shows higher ρ_{eff} and lower α compared to eSi2 which could be explained by the better process and quality of the trap-rich layer in 2nd generation. Fig. 5 illustrates the 2nd and 3rd harmonics of a 900 MHz signal at the output of the CPW line on all different wafers. Compared to HR-SOI wafer, a reduction of 24 and 35 dB is measured on both generations of trap-rich HR-SOI for respectively, 2nd and 3rd harmonics. From Fig. 4 and 5 it can be clearly seen that the level of the harmonics are reversely proportional with the substrate resistivity. Fig. 6 demonstrates the RF performance insensitivity of trap-rich HR-SOI substrates to the applied bias voltages. It can be seen that under different bias conditions, the maximum variation of 2nd harmonics in HR-SOI wafer is 3 times higher compared to second generation trap-rich substrate.

4. Conclusion

In HR SOI wafers by applying a trap-rich layer underneath the BOX, the substrate recovers its high-resistivity properties resulting in higher effective resistivity, lower losses, lower crosstalk and higher linearity (which was demonstrated by lower harmonics level), all conserved after CMOS processing. It was shown that the presence of a trap-rich layer does not change the DC and RF characteristics of the MOSFET transistors. Moreover, by applying enhanced 2nd

generation trap-rich HR SOI substrate having thinner BOX of 200 nm, improved thermal properties could be achievable. Therefore, this technology can be considered as a good candidate for SoC applications.

The authors acknowledge SOITEC for providing the wafers and TowerJazz for the fabrication of CPW lines and PD SOI CMOS devices.

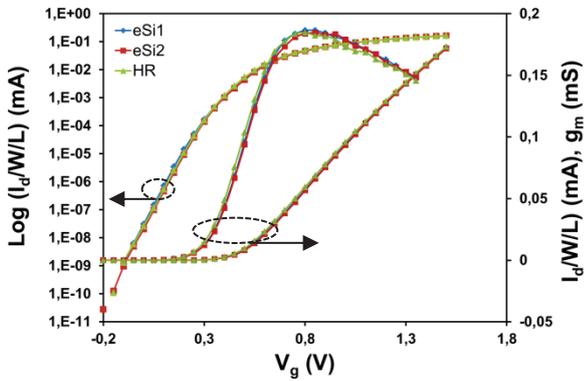


Fig.1: Normalized I_D - V_G (linear and logarithmic) and g_m - V_G characteristics in linear regime ($V_{DS} = 50mV$) of DC transistor for 3 different wafers.

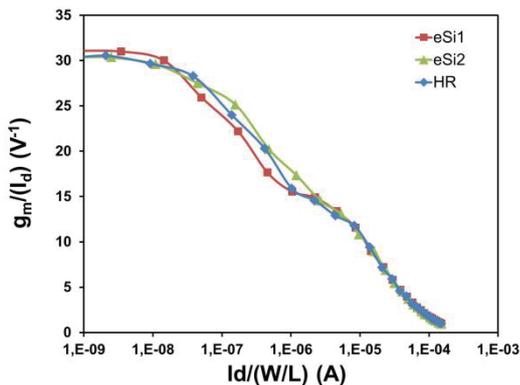


Fig.2: g_m/I_D ratio versus $I_D/(W/L)$ DC transistor on 3 different wafers.

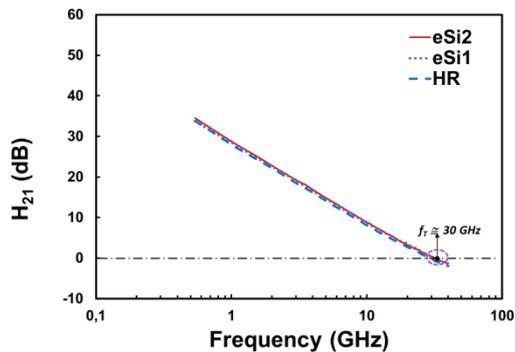


Fig.3: Current gain cutoff frequency f_T at $V_{DS} = 1.2 V$ and V_{GS} at which g_m is maximum for body-tied RF transistor

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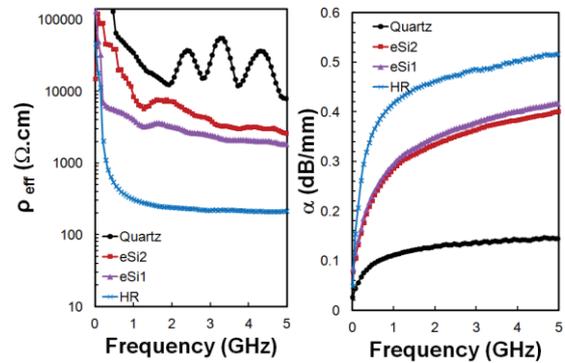


Fig.4: (a) Effective resistivity (b) Total Loss (Conductor and substrate) of 3 different substrates. Quartz has been considered as a reference.

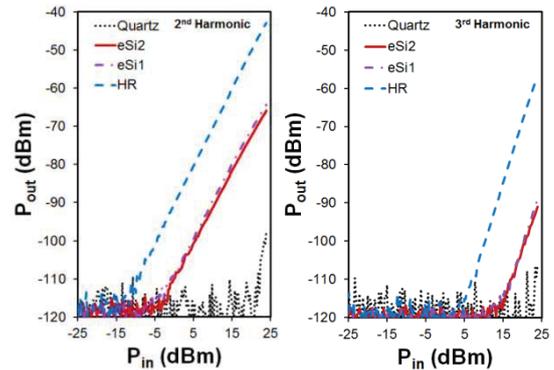


Fig.5: (a) 2nd and (b) 3rd harmonics distortion measured by CPW lines on 3 different wafers. Quartz has been considered as a reference.

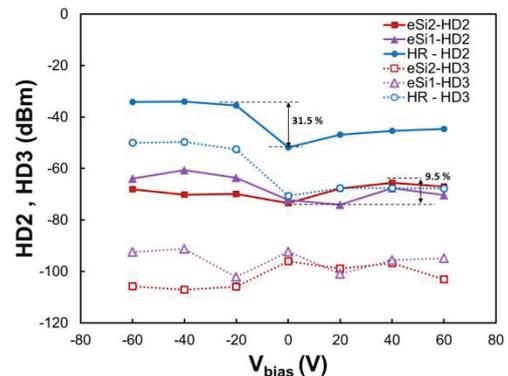


Fig.6: The variation of HD2 and HD3 with bias changing from -60V to +60 V at input power $P_{in} = 20 \text{ dBm}$ for 3 different wafers.

A Novel 3D Pixel Concept for Geiger-Mode Detection in SOI Technology

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1. Introduction

Geiger-mode avalanche diodes have been extensively studied and implemented for the detection of weak optical signals in the visible and near-infrared spectrum range [1] and, during the last few years, in the field of High Energy Physics and Medical Physics for the detection of ionizing particles in tracking applications. A Geiger-mode avalanche diode consists of a p-n junction which is reverse biased above its breakdown voltage. Under this condition, when an electron-hole pair is generated in the space charge region of the junction, a self-sustained charge multiplication process by impact ionization could be triggered, giving rise to a macroscopic electrical signal, promptly quenched by dedicated electronics. The latter are also responsible for signaling that an avalanche event has occurred [1]. In this work, we propose a novel 3D pixel architecture based on Geiger-mode avalanche diodes with associated read-out electronics, conceived for advanced Silicon-On-Insulator (SOI) CMOS technology both for backside illumination and charged particle detection.

2. Concept

Compared to SPAD architectures conceived so far in SOI technology [2-4], our pixel has a 3D structure consisting of an avalanche diode placed beneath the Buried Oxide (BOX) and dedicated pixel electronics in the SOI layer (Figure 1a). The pixel has been designed according to the features of an advanced Fully-Depleted (FD) SOI technology, by properly exploiting the available implantations and diffusions, which are normally meant to provide different back-biasing strategies for the transistors (Figure 1b). The diode sensitive region is indeed defined in the space charge region of a p-well / deep n-well (n-iso) junction. A low doped p-type guard-ring obtained thanks to the retrograde doping of the deep n-well, prevents Premature Edge Breakdown (PEB). The back-gate biasing option featured by this technology (and meant to enable threshold "tuning"), can be conveniently used to connect the SOI electronics with the anode and cathode of the avalanche diode beneath the BOX. Thanks to its 3D structure, the proposed solution is expected to allow very small pixels (down to a few μm^2) while enabling a very high fill factor. Furthermore the pixel read-out electronics can benefit of the well-known advantages brought by SOI technology such as high speed and low power consumption.

3. Very preliminary results and perspectives

TCAD simulations of the proposed 3D pixel have been carried out based on realistic process parameters provided by the foundry. The anode has been grounded in order to insulate the SOI electronics from back-gating effects. The reverse bias $I - V$ curve of the avalanche

diode is plotted in Figure 2, showing a breakdown voltage of $V_{bd} = 13.5\text{V}$. Figure 3 shows the electric field color map of the pixel when the avalanche diode is reverse biased at $V_{rev} = 16.5\text{V}$ (i.e. an excess bias of $V_{ex} = 3\text{V}$). As expected, the retrograde n-type doping in the deep n-well effectively acts as guard-ring preventing any peripheral breakdown at the p-well edges. The simulation accounted for Shockley-Read-Hall (SRH) and band-to-band tunneling generation phenomena but it is observed that tunneling is not the dominant generation mechanism, at least up to a $V_{ex} = 3\text{V}$ (Figure 4), indicating that a low dark count rate could be probably obtained with this technology. This latter has been actually extracted by implementing a numerical method derived from [5] and by considering either a doping dependent or doping independent SRH Generation mechanism (Figure 5). Compared to the doping dependent SRH model, the doping independent one provides results which are closer to what can be found in literature for avalanche diodes having similar technological features [3]. A deeper study is thus required to understand this discrepancy.

Figure 6 shows two possible matrix arrangements for the proposed pixel. Solution (a) provides shielding of the pixel electronics by grounding the p-well. The output is thus sensed at the cathode which penalizes the fill-factor as every pixel needs an independent deep n-well. Solution (b) enables $\sim 100\%$ fill factor pixels (all of them share the same deep n-well) but the electronics need to be insensitive to back-gating effects. Both solutions need an attentive study of optical and electrical cross-talk in order to establish the optimal pixel pitch minimizing those effects.

Acknowledgments

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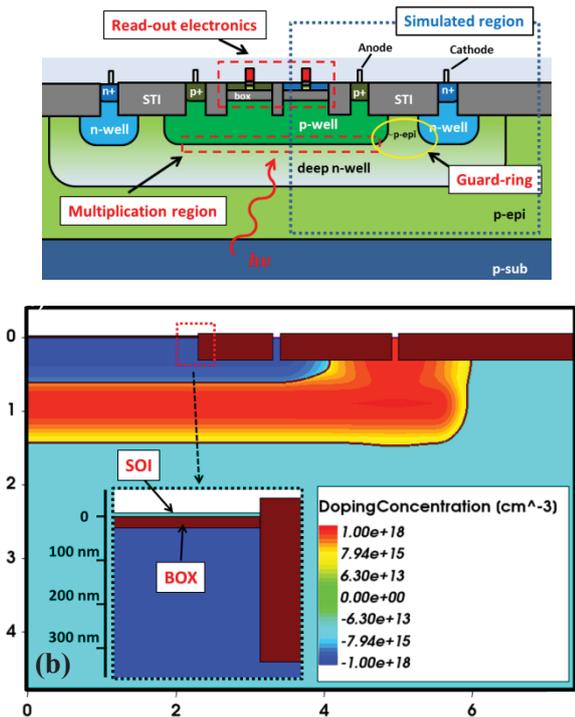


Fig. 1: Schematic representation of (a) the proposed 3D SOI pixel and (b) its associated TCAD model. (Positive values refer to n-type doping. Spatial scales are in μm).

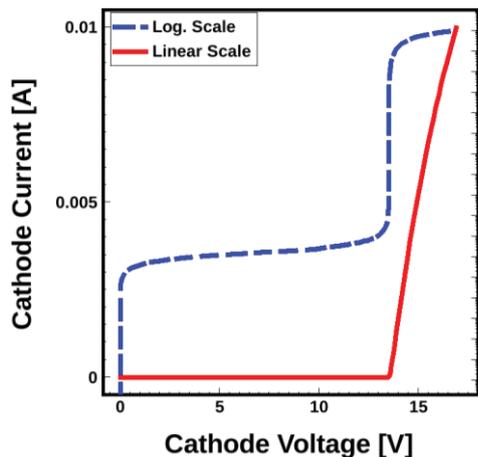


Fig. 2: TCAD Simulation: Reverse bias I-V curve of the avalanche diode. (Sensitive area diameter $D = 7\mu\text{m}$)

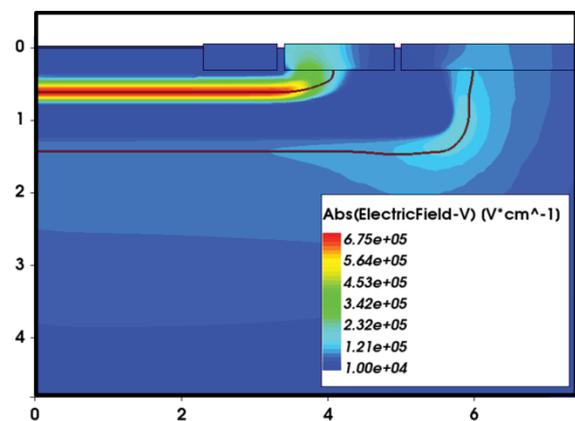


Fig. 3: TCAD Simulation: Electric field color map of the pixel, when the avalanche diode is reverse biased at $V_{rev} = 16.5\text{V}$ (Spatial scales are in μm)

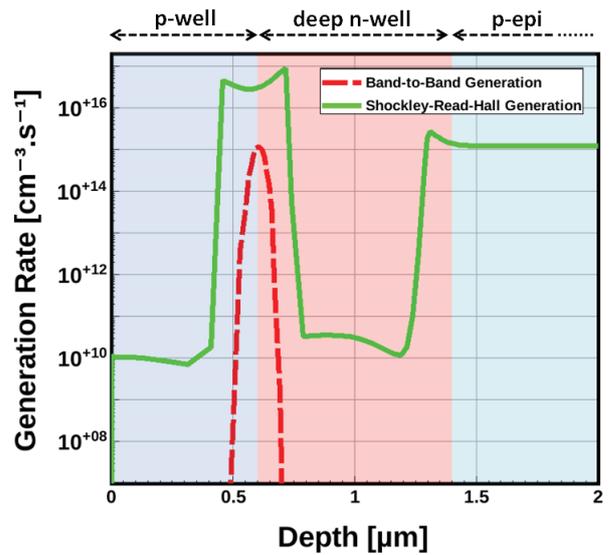


Fig. 4: TCAD Simulation: e/h pair generation mechanisms in the multiplication region of the diode at $V_{rev} = 16.5\text{V}$.

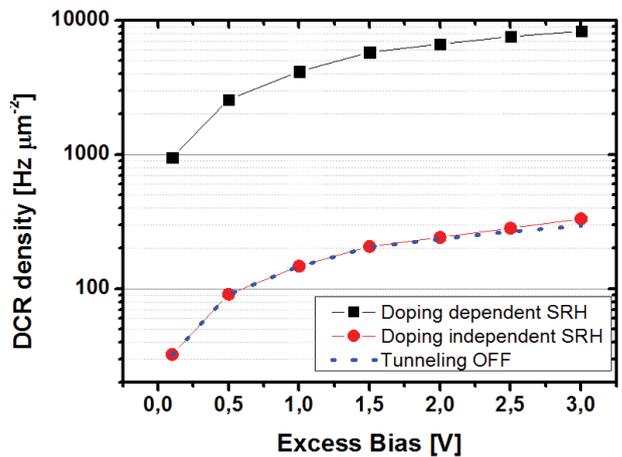


Fig. 5: Dark Count Rate per unit surface extracted by implementing a numerical method based on [5].

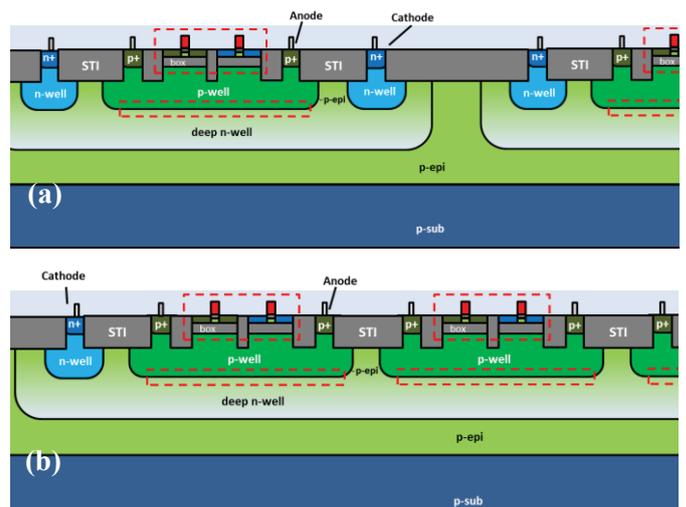


Fig. 6: Possible matrix arrangements for the proposed pixel. Solution (a): grounded anode. Solution (b): common deep n-well

Analog Performance of n- and p-FET SOI Nanowires Including Channel Length and Temperature Influence

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This work aims to present the analog performance of silicon n-type and p-MOSFET SOI nanowires (NWs). Analog parameters are shown at room temperature for both n- and p-type, long and short channel devices with different channel width (W_{FIN}). Results for long channel n-MOS NWs are investigated for the first time for low temperatures down to 100K. Moreover, an analysis is shown comparing the intrinsic voltage gain (A_V) in NWs and quasi-planar transistors.

1. Introduction

The scaling of transistors is a request for the continuity of the CMOS roadmap. Reducing the short channel effects is then a matter of necessity to allow good performances of the devices. Following this idea, multiple gate field effect transistors have been developed in order to improve the gate electrostatic control over the channel charges, allowing scaling beyond the limits imposed by usual planar devices [1]. NWs have shown to be of great interest due to their excellent performance recently reported [2] [3].

Many works have demonstrated the efficiency of NWs concerning digital applications [4], transport [5] and fabrication [3], but not much attention has been paid concerning analog applications [6], which is important for integrating such ultimate devices in mixed circuits. In this work we extend the results in [6] and present for the first time an experimental study of analog properties for both n- and p-MOS SOI NWs with long ($L=10\mu\text{m}$) and short ($L=40\text{nm}$) channel lengths as a function of W_{FIN} , where the long channel n-MOS are analyzed down to 100K. The analog performance of NWs and quasi-planar MOSFETs are compared.

2. Devices and Measurements

The studied transistors are Si [110]-oriented trigate NWs fabricated at CEA-Leti using a 145nm thick buried oxide SOI substrate. The NWs were fabricated in a multi finger structure (50 fins) with EOT of 1.4nm and silicon thickness of 11nm. Details about the fabrication of the transistors can be found in [2] and [7]. Fig. 1 presents a cross-section TEM image and a schematic of Si NW FET. The transistors present the drain current (I_{DS}) as a function of gate voltage (V_{GS}) characteristics shown in Fig. 2, at $|V_{\text{DS}}|=40\text{mV}$, n-MOS ($W_{\text{FIN}}=14.5\text{nm}$) and quasi-planar ($W_{\text{FIN}}=10\mu\text{m}$) down to 100K (a) and long and short channel p-MOS at room temperature (b). At room temperature, long channel n- and p-type devices present $S=61\text{mV/dec}$. For the narrow n-MOS, the threshold voltage variation with temperature ($\Delta V_{\text{TH}}/\Delta T$) is around 0.6mV/K and $S=28\text{mV/dec}$ at 100K. The subthreshold slope for p-MOS with $L=40\text{nm}$ and $W_{\text{FIN}}=15\text{nm}$ is slightly degraded to 71mV/dec . The measurement of carrier effective mobility (μ_{eff}), extracted through the split C-V method [8], and series resistance (R_S), extracted according to ref. [9], at $T=300\text{K}$ and 100K is reported in Table I for n-MOS.

3. Results and Discussion

Fig. 3 presents both transconductance (g_m/W_{ef}) (A) and output conductance (g_D/W_{ef}) (B) as a function of W_{FIN} , in saturation, at room T for $L=10\mu\text{m}$. From Fig. 3.A, one can note the higher values of g_m for n- than in p-MOS and a g_m degradation (resp. g_m increase) for n-MOS (resp. p-MOS) as W_{FIN} is reduced. These effects are related to the electrons and holes mobility. While holes μ_{eff} is higher in (110)/[110], electrons μ_{eff} is higher in (100)/[110]. Being (110) the surface related to the fin height and (100) related to the fin width, reducing W_{FIN} favors mobility in (110) plan in comparison to (100) plan [10]. This is why p-MOS NWs show improvements on g_m over wide planar FETs, while n-MOS show the opposite behavior. For n-MOS, g_m degradation is 19% for $V_{\text{GT}}=400\text{mV}$ and for p-MOS the improvement is 52%. Fig. 3.B shows the decreasing (improvement) of g_D as W_{FIN} decreases for both n- and p-MOS, almost reaching one order of magnitude. The behavior of g_D is mainly related to the channel modulation effect (CME), where CME is reduced in NWs due to the better electrostatic gate control over the charges.

In Fig. 4 it is presented the results for the potential at the center of n- and p-MOS with $L=40\text{nm}$ and $W_{\text{FIN}}=15\text{nm}$, obtained from tridimensional numerical simulations performed in Sentaurus, from Synopsys [11]. It is observed that the potential distribution inside the channel is similar for both n- and p-MOS, varying V_{DS} , which can explain the fact that g_D , and as a consequence, the intrinsic voltage gain behaves similarly varying W_{FIN} , comparing n- and p-MOSFETs.

The A_V (calculated through the g_m/g_D ratio) as a function of W_{FIN} is shown in Fig. 5 for $L=10\mu\text{m}$ and Fig.6 for $L=40\text{nm}$. Due to the behavior of g_m and g_D , it is observed an improvement for NWs as the width is reduced. Using NWs allows an intrinsic voltage gain 20dB higher than the wide planar device for both n- and p-MOS with $L=40\text{nm}$.

In Fig. 7, g_m/I_{DS} is presented as a function of V_{GT} (A) and μ_{eff} as a function of T (B), for long channel n-MOS. Wide and NW FETs are compared from 300K to 100K. It is observed an increase of g_m/I_{DS} as T is reduced and W_{FIN} reduces from $10\mu\text{m}$ to 14.5nm . According to [10], g_m/I_{DS} can be estimated by $\left(\frac{g_m}{I_{\text{DS}}}\right)_{\text{sat}} = \left(2/V_{\text{GT}}\right) \times \frac{1+(R_S\mu_{\text{eff}}C_{\text{ox}}W_{\text{ef}}V_{\text{GT}})/2L}{1+(R_S\mu_{\text{eff}}C_{\text{ox}}W_{\text{ef}}V_{\text{GT}})/L}$ (1). The parameters that are W_{FIN} dependent are R_S , μ_{eff} and W_{ef} . From Table I, it is observed a variation for R_S of a factor close to 10 for n-MOS, as W_{FIN} goes from $10\mu\text{m}$ down to 14.5nm . This decrease of R_S with T is associated to μ_{eff} increase [12]. The increase of μ_{eff} while increasing W_{FIN} is smaller than a factor of 2. On the other hand, W_{FIN} reduces almost 3 orders of magnitude, being the key parameter in (1), where it is observed that g_m/I_{DS} varies with the inverse of $R_S \times \mu_{\text{eff}} \times W_{\text{ef}}$. This is why NWs show higher g_m/I_{DS} than wide planar FETs, mainly in weak inversion. From Fig. 7

(B), the T dependence coefficient of μ_{eff} is found to be around 0.88 for all devices, above 100K, where phonon scattering is dominant at moderate inversion. Fig. 8 presents both g_m/W_{eff} (A) and g_D/W_{eff} (B) as a function of T, (extracted at $V_{\text{DS}}=0.9\text{V}$ and $V_{\text{GT}}=400\text{mV}$) for long channel n-MOS. By decreasing T, it is observed an increase of g_m and g_D with similar rate for both parameters, which is close to the same 0.88 factor obtained for the μ_{eff} dependence with T. As a result, in Fig. 9 we observe that the influence of T in g_m and g_D is annulated one by each other and A_V is approximately constant. Fig. 9 also shows high values of Early Voltage ($V_{\text{EA}}=I_{\text{DS}}/g_D$) for n-type NWs due to smaller CME.

4. Conclusions

This work has presented an experimental analysis of analog parameters for NWs SOI devices considering long and short channel devices, n- and p-MOS and temperature down to 100K. It was observed great improvements on the performance of NWs in comparison to wide planar transistors concerning A_V , due to improvements on g_D . Concerning T decreasing, the effects on μ_{eff} variation

change both g_m and g_D on the same rate, leading to values approximately constant for A_V . The intrinsic voltage gain is around 30dB for both n- and p-MOS with $L=40\text{nm}$ and $W_{\text{FIN}}=15\text{nm}$ at $T=300\text{K}$.

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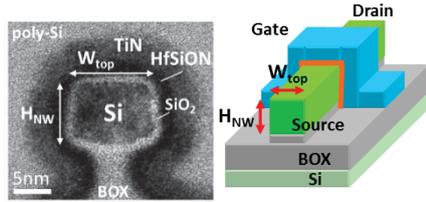


Fig. 1: Si SOI NW cross section TEM image and schematic.

Table I: Effective mobility at $N_{\text{INV}}=0.8 \times 10^{13} \text{cm}^{-2}$ and series resistance for n-MOS at 100K and 300K.

	W_{FIN}	$\mu_{\text{eff}} [\text{cm}^2/\text{V}\cdot\text{s}]$		$R_s [\text{k}\Omega]$	
		100K	300K	100K	300K
nMOS	10 μm	626	283	0.9	1.8
	14.5nm	466	216	8.7	14.8

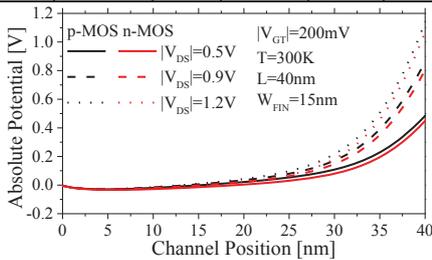


Fig. 4: Simulation results: potential along the channel length for n- & p-MOS at 300K, $L=40\text{nm}$, $W_{\text{FIN}}=15\text{nm}$, $|V_{\text{GT}}|=200\text{mV}$, $|V_{\text{DS}}|=0.5, 0.9$ and 1.2V .

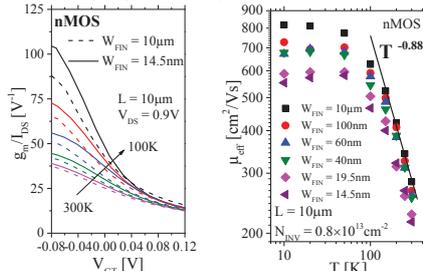


Fig. 7: n-MOS, $L=10\mu\text{m}$, results for g_m/I_{DS} vs V_{GT} at $V_{\text{DS}}=0.9\text{V}$ (A) and μ_{eff} vs T at $N_{\text{INV}}=0.8 \times 10^{13} \text{cm}^{-2}$ (B).

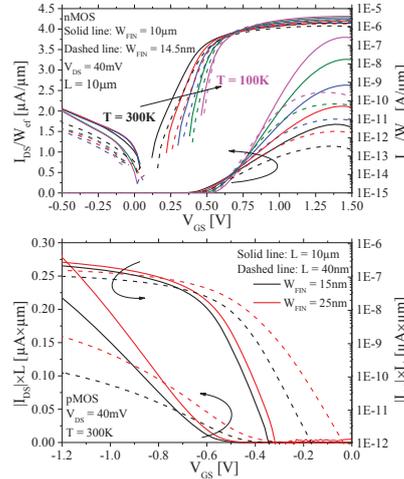


Fig. 2: $I_{\text{DS}}/W_{\text{eff}}$ and I_{DS}/L vs V_{GS} for n- (A) and p-MOS (B) at $|V_{\text{DS}}|=40\text{mV}$.

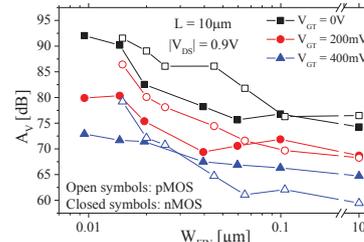


Fig. 5: A_V vs W_{FIN} for n- and p-MOS at 300K, $L=10\mu\text{m}$, $|V_{\text{DS}}|=0.9\text{V}$, $|V_{\text{GT}}|=0, 200\text{mV}$ and 400mV .

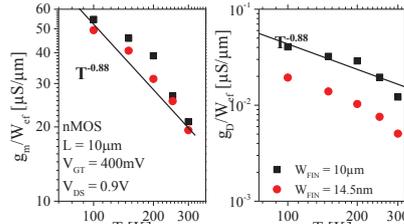


Fig. 8: g_m/W_{eff} (A) and g_D/W_{eff} vs T for n-MOS, $L=10\mu\text{m}$, at $V_{\text{DS}}=0.9\text{V}$ and $V_{\text{GT}}=400\text{mV}$.

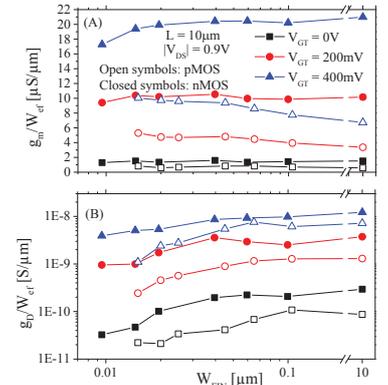


Fig. 3: g_m/W_{eff} (A) and g_D/W_{eff} vs W_{FIN} for n- and p-MOS, $L=10\mu\text{m}$, $|V_{\text{DS}}|=0.9\text{V}$, $|V_{\text{GT}}|=0, 200$ and 400mV .

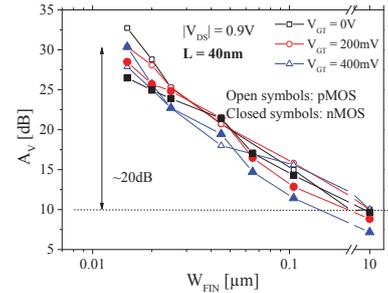


Fig. 6: A_V vs W_{FIN} for n- and p-MOS at 300K, $L=40\text{nm}$, $|V_{\text{DS}}|=0.9\text{V}$, $|V_{\text{GT}}|=0, 200\text{mV}$ and 400mV .

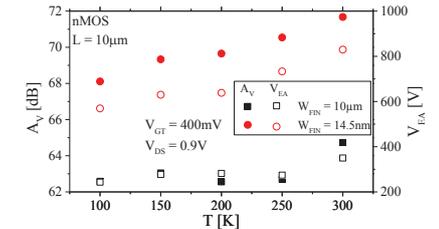


Fig. 9: A_V and V_{EA} vs T for n-MOS, $L=10\mu\text{m}$, at $V_{\text{DS}}=0.9\text{V}$ and $V_{\text{GT}}=400\text{mV}$.

Full Quantum Mechanical Electronic Transport Simulations in Si Quantum Wells and Superlattices for Thermoelectric Applications

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1. Introduction

When a temperature difference is applied across a thermoelectric material, a potential difference which can be used to drive a circuit, results. Thus, thermoelectrics have the potential to turn omnipresent waste heat into a power source. Furthermore, unlike a traditional heat engine, thermoelectric generators have no moving parts, require no or minimal maintenance, are arbitrarily scalable in size, and can also be used for cooling applications when a voltage is applied across them. The main hurdle towards wide-spread application of such technology is the stubbornly low power conversion efficiency of current materials. Recent advances in nanostructured thermoelectrics, however, and especially in Si-based low-dimensional and nanostructured materials, has the potential to uproot this state of affairs [1-4].

The thermoelectric (TE) performance of a material can be quantified by the figure of merit $ZT = \sigma S^2 / \kappa$, where σ denotes the electrical conductivity, S the Seebeck coefficient and κ the thermal conductivity. Recent improvements in ZT have been achieved through the use of nano-engineered materials with ultra-low κ , reaching values below the amorphous limit [1-3]. Attempts to improve the numerator, the so-called power factor (σS^2), have proved substantially less successful owing to the often inverse relationship between the conductivity and the Seebeck coefficient. However, the energy filtering of carriers in nanocomposite materials with embedded potential barriers (V_B) (i.e. superlattices) is a promising way to improve σS^2 via improvements in the Seebeck coefficient [4, 5]. Seebeck coefficient enhancement in nanometers-size layer superlattices has been observed in several experimental works. However, improvements over the overall power factor were not due to accompanying losses in σ . In this work, we develop a fully quantum mechanical Non-Equilibrium Green's Function (NEGF) method in 1D to explore the conditions under which σ and S^2 can be simultaneously improved. We show that optimized superlattice structures could provide up to ~30% power factor improvements.

2. Method and Discussion

We use the NEGF method in the effective mass approximation, including both acoustic and optical phonon scattering. Figure 1 illustrates the simulated 1D channel geometry, consisting of a series of potential

barriers. The colormap shows the current spectrum and how it fluctuates in energy during emission / absorption of optical phonons. Previous works have indicated that under optimal conditions the transport in the wells needs to be semi-ballistic, where carriers only lose part of their energy before they reach the next barrier [6, 7], and thus, in this work we calibrate the well size L_w , electron-phonon scattering, and barrier height V_B for these optimal conditions. We use $L_w = 20\text{nm}$ and $V_B = 0.16\text{eV}$ throughout this work.

Once the model is constructed, we then explore the space of possible superlattice configurations and calculate their corresponding power factors. Two main parameters are examined, the width of the barriers W , and the position of the Fermi level with respect to the barrier height $\eta_F = E_F - E_C$. Figure 2 shows the significance in choosing the right barrier width. Figure 2a shows that if the barriers are too thin, tunneling makes them seem transparent, and their filtering effect is lost (which is detrimental to S). Figure 2b shows that if the barriers are too thick, then carriers relax at the top of them, which increases the channel resistance. The optimal width is somewhere in the middle as shown in Fig. 2c. The influence of the barrier width on the power factor is indicated in Fig. 3. We can observe thin barriers could cause up to ~40% degradation in performance. The optimal value is $W \sim 3\text{nm}$, whereas for larger widths the resistance increases and the power factor drops again.

The behavior of the power factor versus η_F is shown in Fig. 4. As the E_F increases, the power factor increases, with an optimal value around $E_F \sim 0.14\text{eV}$, approximately $\sim k_B T$ below V_B . This allows enough hot carriers to overpass the barriers, and blocks the cold carriers, which increases energy filtering and benefits both S and σ . In comparison to the optimized power factor in a uniform material without barriers (magenta line), this is ~15% higher. An additional improvement can be achieved by relaxing the shape of the barriers from perfectly sharp to smooth, which provides power factor values up to ~30% higher compared to the uniform material. The reason behind this is the fact that sharp edges introduce quantum reflections in the transmission, which strongly reduces the conductivity.

The fact that two major performance degrading mechanisms, are of quantum mechanical nature (tunneling and reflections) justifies the choice of our

quantum mechanical model for the optimization of new generation TE materials. We also note that we are currently developing 2D quantum mechanical transport capabilities, which will be used to explore a much richer design space in terms of geometries for even larger improvements in the TE power factor.

We acknowledge the Vienna Scientific Computing Cluster for computational resources and funding from the Austrian Science Fund FWF, project code P25368-N30.

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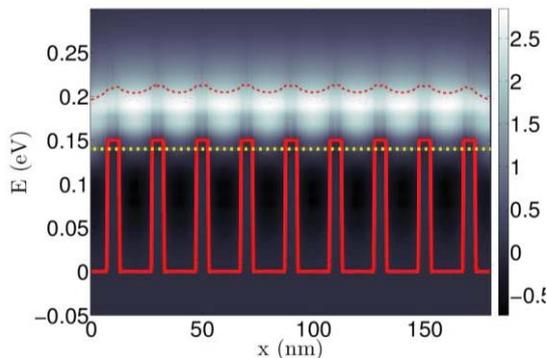


Fig. 1. The potential profile of the barriers in the channel with width of 4nm and height of 0.16 eV. The colormap shows the current density versus position. Superimposed on the image are the potential barriers and the carriers energy expectation value $\langle E \rangle$.

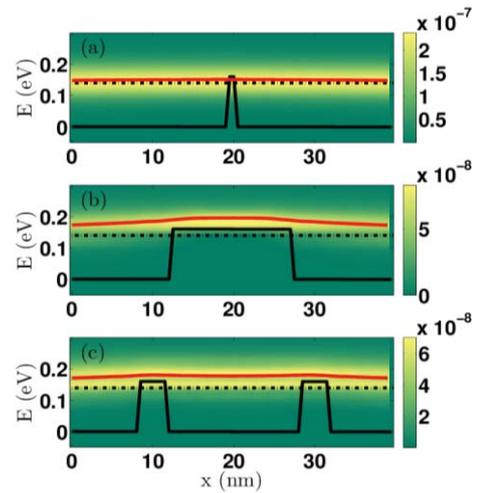


Fig. 2. (a) The case of a thin, transparent barrier, in which most current passes through the barrier. (b) The case of a thick barrier, where most of the current passes over the barrier. (c) The case of an optimal superlattice. Partial energy relaxation is observed in the wells (lowering of the red line in the well regions).

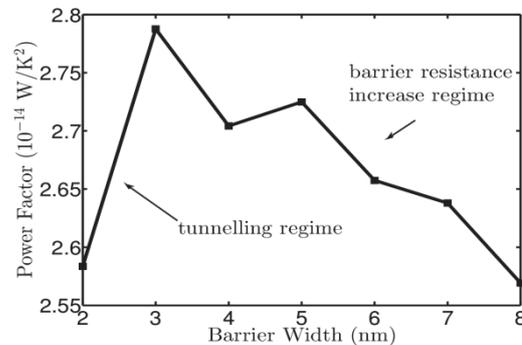


Fig. 3. Power factor versus barrier width. The optimal barrier width is ~ 3 nm, which is thick enough to prevent tunnelling, but thin enough retain the conductance high.

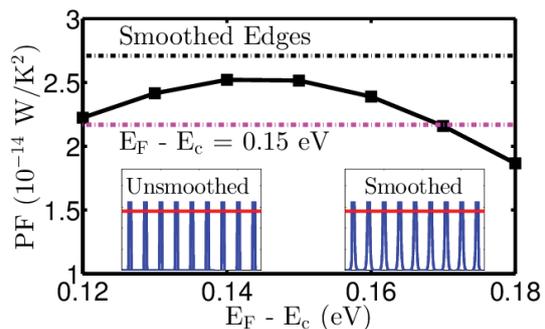


Fig. 4. The thermoelectric power factor of a superlattice material versus the position of the Fermi level E_F with respect to the conduction band edge. The barrier height is $V_B=0.16$ eV. The optimal power factor of a uniform channel is indicated by the magenta-dashed line, and the optimal power factor of a superlattice with smoothed barriers (as shown in the insets) by the black-dashed line.

Body Factor Scaling in UTBB SOI with Supercoupling Effect

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1. Abstract

Focusing on the channel length scalability, the coupling coefficient ($\alpha_1 = \Delta V_{T1}/\Delta V_{G2}$) is analyzed in thick (25nm) and thin (7nm) UTBB SOI devices. Experimental data and simulations demonstrate that the supercoupling effect further improves the device scalability and operation in thin silicon films. The impact of thinning the gate oxide and body on the inter-channel coupling is documented.

2. Introduction

UTBB (ultrathin body and buried oxide) SOI device has been considered a good candidate for the sub-28nm technology node [1-4]. The body and buried oxide (BOX) thinning, together with a ground plane (GP) implantation beneath the BOX, improves the channel control. Enhanced inter-gate coupling occurs, offering a more efficient threshold voltage tuning by the back-gate bias (V_{G2}) and reduced source- and drain- fringing field effects [5-6]. UTBB devices can also operate with lower voltage for better power efficiency [3,4,7-8].

Si-film thinning below 10 nm enables extreme inter-gate coupling effects, like the supercoupling, to develop. Supercoupling prevents the independent operation of the front and back interfaces [9,10]. Reference [10] shows the channel length impact on the critical thickness, i.e., the thickest silicon film at which the supercoupling effect is present. Differently, the following analysis investigates the dependence of the coupling coefficient with the gate length to demonstrate that supercoupling helps to mitigate short-channel effects (SCE) in UTBB devices enabling a more aggressive downscaling.

3. Device Characteristics

The UTBB SOI transistors under test were processed at LETI and STMicroelectronics. The SOI wafers have a 25nm-thick BOX. The silicon film thickness (t_{Si}), effective oxide thickness (EOT) of the high-k/metal gate stack, channel length (L) and channel doping (N_{CH}) of the measured and simulated devices are presented in Table I. The simulations parameters follow the characteristics of the measured devices, considering quantum model.

MEASURED DEVICES DETAILS

From	t_{Si} (nm)	EOT (nm)	L (nm)	N_{CH} (cm ⁻³)
LETI	25	3.1	50-1000	2×10^{17}
ST	7	1.3	30-1000	1×10^{15}
2D-Numerical	25	3	50-1000	2×10^{17}
Simulations	7	1 and 3	20-1000	1×10^{15}

4. Results and Analysis

Fig. 1 presents the experimental front-channel threshold voltage (V_{T1}) as a function of the back-gate bias (V_{G2}) for thick and thin silicon films. Fig. 2 shows the simulated front $V_{T1}(V_{G2})$ (figs. 2C and 2D) and the back $V_{T2}(V_{G1})$ (figs. 2A and 2B) coupling curves.

Experimental and simulated V_{T1} are extracted by the 2nd derivative method. The slope yields the coupling coefficients ($\alpha_1 = \Delta V_{T1}/\Delta V_{G2}$ and $\alpha_2 = \Delta V_{T2}/\Delta V_{G1}$), which are compared in figs. 3A and 3B for different channel lengths and body thicknesses. Figs. 2 and 3 show that the coefficient α_2 is higher than α_1 because of the thinner front oxide compared to the BOX.

As the device length is downscaled, a reduction in $V_{T1,2}$ and coupling coefficients is observed due to SCEs (figs.1-3). This drop is more remarkable in thick SOI devices. For ultrathin Si-films, although the roll-off is still present, the coupling coefficient remain almost constant (figs.1-3), indicating that UTBB transistors can be further scaled down. This constant body factor is a consequence of the supercoupling effect.

The lower coupling coefficient α_1 for thinner Si-film (see figs. 1-3) can be explained by fig. 4. The thinner front-gate oxide (open symbols), which is the case of the measured samples, degrades the back-gate impact on the V_{T1} . If the Si-film thickness were the only difference between the samples (half-filled and full symbols), the coupling would be stronger for thinner device. It follows that both, the front- and back-gate oxide, should be downscaled together to keep the coupling coefficient constant.

In order to analyze how the supercoupling benefits the scalability, the potential along the structure (at mid-channel from front to back gate) can be seen in fig. 5 for various channel lengths at $V_{G1}=V_{T1}$. For 25nm Si-film (fig. 5A), the potential at the back interface is enhanced in shorter channels due to the threshold voltage roll-off. The loss of the back interface control is caused by the fringing field spreading through the BOX.

On the other hand, figs. 5B and 6 show that the front-gate coupling increases in thin SOI devices and the back interface tends to follow the potential at the front one, counteracting the fringing field impact. The result are: (i) a higher back-interface potential (Φ_{S2}) than for 25nm-thick transistor, (ii) a Φ_{S2} reduction as the channel length is decreased down to 60nm and (iii) a slight increase in Φ_{S2} for channel lengths shorter than 60nm. Fig. 6 demonstrates how UTBB devices are more resilient against short-channel effects thanks to the limited source and drain charge sharing but also to the supercoupling effect.

5. Conclusions

Measurements and simulations show the supercoupling impact on the back-surface potential as well as the variation of the coupling coefficient in UTBB SOI for different gate lengths. A stronger coupling in thin Si-films was observed by maintaining the same front-gate oxide thickness.

Acknowledgments:

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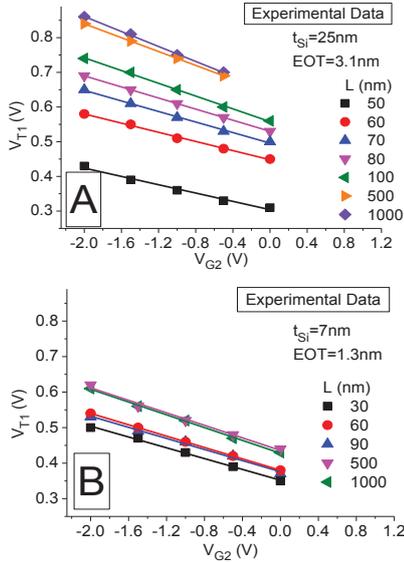


Fig.1: Measured front-gate threshold voltage as a function of the back-gate bias for various channel lengths in thick (A) and thin (B) Si-films.

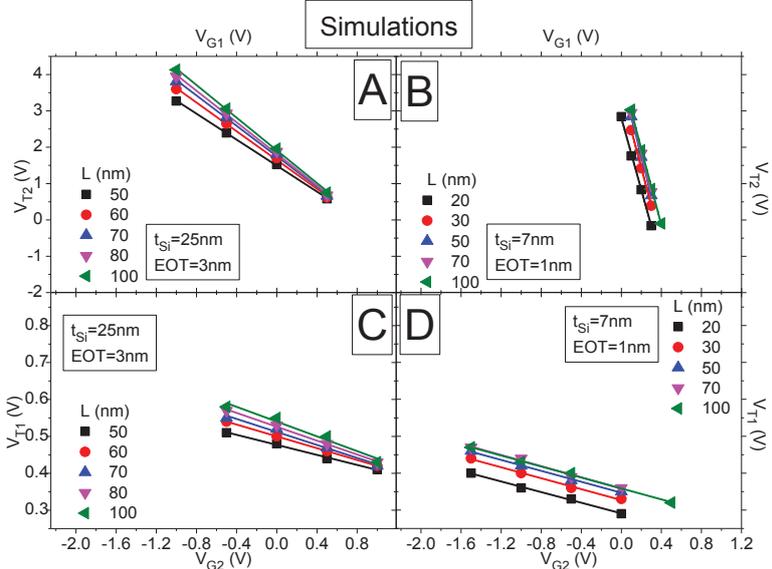


Fig.2: Simulated threshold voltage of the back (A and B) and front (C and D) channels versus front (A and B) and back (C and D) gate biases for various channel lengths in thick (A and C) and thin (B and D) films.

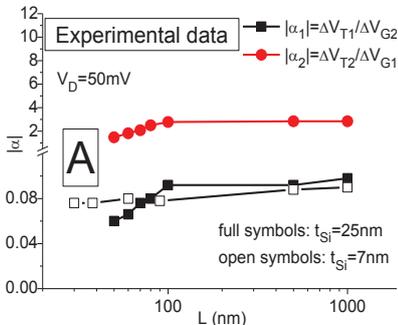


Fig.3: Front and back coupling coefficients (α_1 , α_2) versus channel length for thick ($t_{Si}=25nm$) and thin ($t_{Si}=7nm$) devices obtained by measurements (A) and simulations (B).

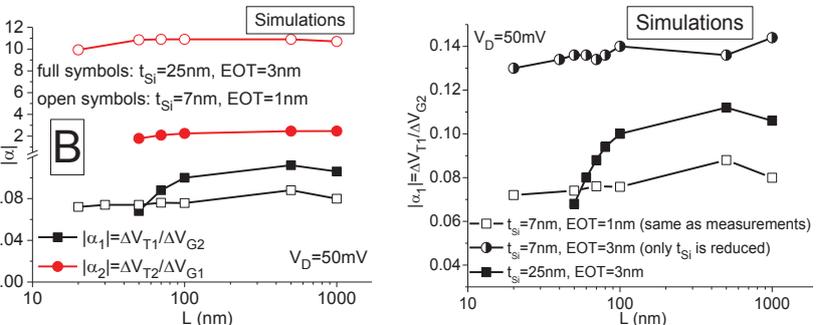


Fig.4: Simulated coupling coefficient α_1 as a function of channel length.

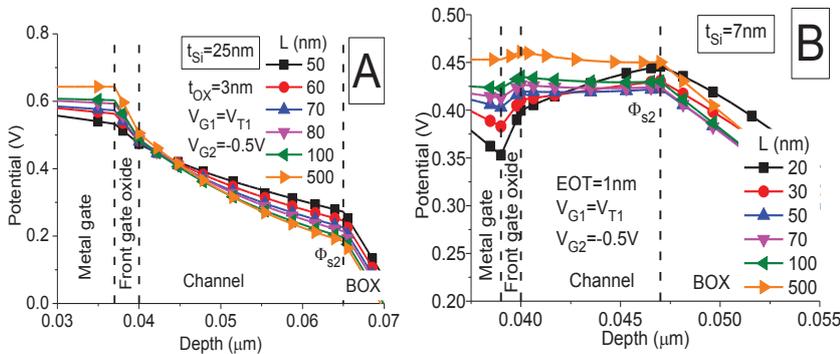


Fig.5: Simulated potential for various channel lengths in 25nm- (A) and 7nm-thick (B) Si-film at mid-channel from front to back gate.

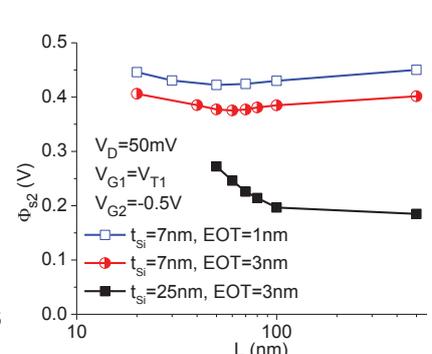


Fig.6: Simulated back surface potential versus gate length for thick (25nm) and thin (7nm) films.

Current Mirrors with Strained Si Single Nanowire Gate All Around Schottky Barrier MOSFETs

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1. Abstract

In this work, we present a simple current mirror based on two single nanowire strained silicon Schottky barrier (SB) MOSFETs with gate-all-around (GAA) structure. B⁺ implantation into NiSi₂ with dopant segregation at source and drain was used to decrease the Schottky barrier height for holes at the metal/channel junctions. The current mirror shows a very good Mirror Ratio MR = 0.99 and high output resistance of 100MΩ.

2. Introduction

As MOSFET reaches its physical scaling limit, new device concepts are required to overcome scaling problems in CMOS technology. SBMOSFETs using metallic contacts have lower parasitic source/drain (S/D) resistances with abrupt junctions at silicon/metal interfaces which overcome scaling limitations for short channel devices[1]. Moreover, replacing S/D with silicide requires low thermal budget and is silicon process compatible. Improved control over silicide/channel interface by introduction of ultra thin silicides has been exhibited [2,3]. However, large SB heights result in low on current and poor subthreshold swing. It has been shown that dopant implantation into silicide(IIS) can be used to tune Schottky barrier height(SBH)[4,5], while preventing dopant diffusion far into the channel, the so-called dopant segregation[6]. Electrical properties of SBMOSFETs fabricated with IIS for planar[3] and gate-all-around(GAA)[7] devices have been already investigated. In this work, we aim to analyze the analog circuit performance of single NW strained silicon GAA SBMOSFETs by fabricating a simple current mirror based on two connected transistors.

3. Device Fabrication

Strained single Si NWs have been fabricated by electron beam lithography and dry etching technique on biaxially strained SOI ($\epsilon_{\text{biax}} = 0.8\%$) with 15 nm top Si on 145 nm BOX. The free standing-wires were wrapped with 3nm HfO₂ and 40 nm TiN (AVD®-process). NiSi₂ was formed at the source/drain regions with a very thin Ni layer. Then B⁺ ion implantations at tilted angle of 45° and 135° were performed for both source and drain as shown in Fig.1, followed by a low temperature anneal for dopant segregation. Fig.2 shows an SEM image of the device. The NW has a width of 30nm and a thickness of 12 nm. Using this fabrication process, current mirrors with two gate fingers were fabricated as shown in Fig.3. The drain and the gate of transistor M1 are connected to each other through an aluminum contact, while the source contacts of both M1 and M2 are connected through the silicide. Fig.4 illustrates the working principle of the current mirror.

4. Device Characteristics

Fig.5 shows the transfer characteristics of the fabricated sSi GAA single NW SB MOSFETs with and without IIS at V_{ds} = 0.1 V. The minimum off current is shifted to positive V_{gs} because the Si channel is slightly p-doped (1e16 cm⁻³).

To compensate this voltage shift work function engineering is needed. It is evident from the figure that IIS increases the drain currents and lowers the inverse subthreshold slope of the device from 135mV/dec to 80mV/dec. This can be attributed to the reduction of SBH for holes using B dopant segregation. Moreover, the on-current is several orders of magnitude higher than the gate leakage which exhibits good oxide quality. The transistors were biased according to the biasing scheme shown in Fig.4. V_{DD} was connected to the source of transistors. An input current, I_{REF}, was applied to the drain of transistor M1, and the output current I_{out} was measured by sweeping the drain voltage of transistor M2. Fig.6 shows the output characteristics of the simple current mirror. V_{out} represents the V_{ds} of transistor M2. As it is shown, by increasing I_{REF}, the output current also increases and exhibits good saturation at the respective I_{REF} value. The Mirror Ratio (MR) = I_{out}/I_{REF} was calculated to be 0.99 at I_{REF} = 1uA which indicates both transistors are well matched. Moreover, the output resistance of current mirror was calculated to be as high as 100MΩ, which is considerable for simple current mirror. A high output resistance is essential to achieve stable output currents under different load conditions.

5. Conclusion

We have fabricated single NW sSi GAA SB MOSFETs with B⁺ implantation into NiSi₂ source/drain and dopant segregation. The lowered effective SBH for holes by dopant segregation increases the on-current and improves the subthreshold swing. A simple current mirror employing two transistors exhibits a good MR of 0.99 and high output resistance of 100MΩ. These properties and low operating voltages of fabricated SB MOSFETs makes them suitable for low-power analog circuit applications.

Acknowledgement

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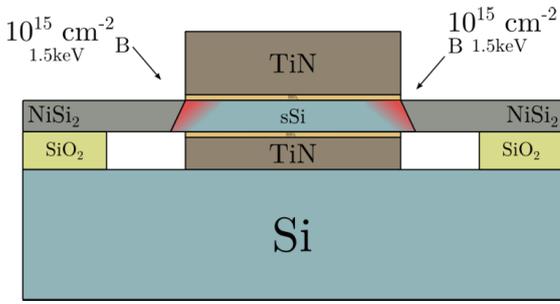


Fig.1: Schematic of the fabricated sSi NW SB MOSFET with a TiN/HfO₂ gate stack

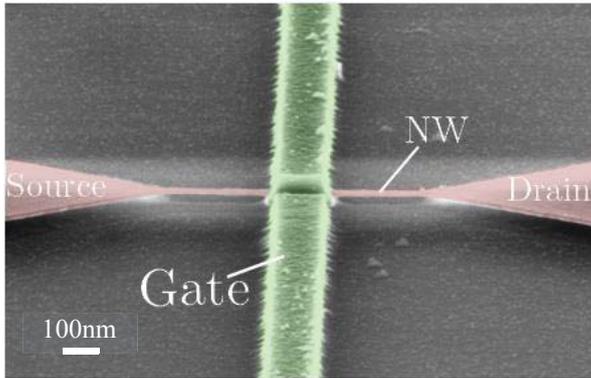


Fig.2: SEM image of a single sSi NW SB MOSFET with TiN/HfO₂ gate stack. The gate length is 150 nm

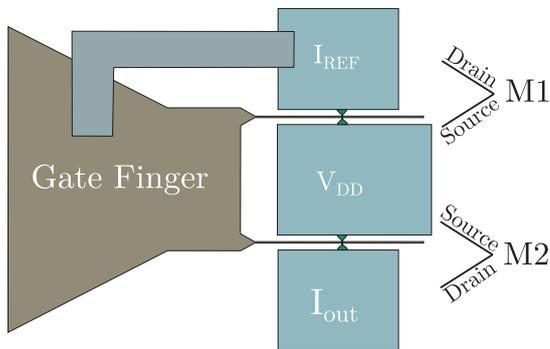


Fig.3: Circuit layout of the single sSi NW SB MOSFET current mirror. The drain and gate of M1 are connected through an Al contact.

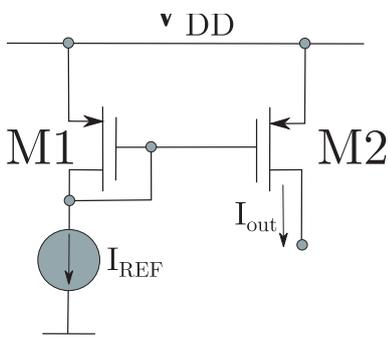


Fig.4: Biasing scheme of the p-SB MOSFET based current mirror.

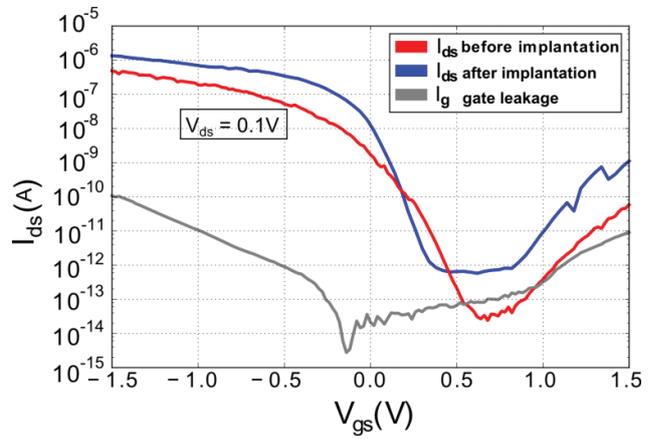


Fig.5: Transfer characteristics of a SB MOSFET before (red) and after (blue) B⁺ implantation into silicide and annealing, showing improved performance of the device by IIS and dopant segregation.

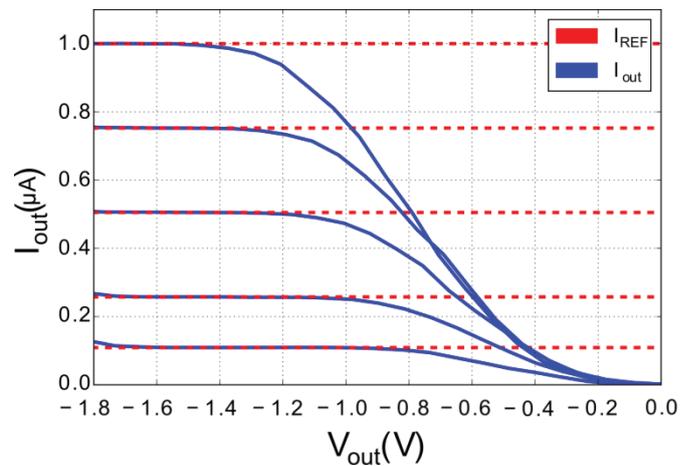


Fig.6: Output characteristics of the current mirror. The red line shows the I_{REF} value. The output current exhibits good saturation at I_{REF} values, indicating a very good match of both transistors.

A Method for Combined Characterization of MOSFET Threshold Voltage and Junction Capacitance Eliminating Channel Current Effect

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1. Introduction

MOSFET threshold voltage models are typically based on a 1D solution of a Poisson equation in the MOSFET below the gate. In this approach the current flow is neglected. Standard threshold voltage extraction methods are based on measured I-V characteristics [1]. So an electric field effect on mobility and a voltage drop at the source and drain resistances in real devices affect V_{th} extraction. Methods aimed at minimization of these effect have been proposed, e.g. in [2,3], but they do not eliminate the channel current effect on V_{th} extraction.

In the presented work we describe a method based on a measurement of the MOSFET source-bulk (SB) junction capacitance C_{bs} vs the gate-source voltage V_{GS} . The drain terminal remains open, so the channel current effect is eliminated.

2. Description of the method

A potential distribution in a space charge area of the SB junction below the gate is different than in the area outside the gate. Simulation results from Silvaco Atlas for a simplified p-channel structure are shown in Fig.1. As V_{GS} varies the potential distribution below the junction is constant, whereas below the gate changes. At the accumulation below the gate it is rather insensitive to gate bias, so C_{bs} capacitance does not change with V_{GS} . However at the onset of strong inversion a channel is formed as an expansion of the source. It is followed by a steep increase of C_{bs} capacitance. This observation is a basis of the proposed method.

The $C_{bs}(V_{BS})$ characteristics of the p-channel MOSFET measured for different V_{GS} voltages are shown in Fig.2. Based on them, $C_{bs}(V_{GS})$ curves with V_{BS} as a parameter have been constructed (Fig.3). They lead to the $V_{th}(V_{BS})$ characteristics of the MOSFET (Fig.4) where they are set together with $V_{th}(V_{BS})$ plots obtained using the current-based methods: a linear extrapolation of I_D-V_{GS} at transconductance g_m maximum, and $I_D/g_m^{0.5}$ [2]. It may be stated that the V_{th} extraction results are close. Their values for a set of substrate bias are listed in Table 1.

By applying a method of [4] to $V_{th}(V_{BS})$ data, standard parameters of V_{th} may be determined: $V_{th,0}$ – threshold voltage at $V_{BS}=0V$, γ – body factor, $2\cdot\phi_F$ – double Fermi voltage [4].

The proposed method allows for analysis of the C_{bs} capacitance in the MOSFETs. It is well known, that the MOSFET junction capacitances have plane and sidewall components. Typically they are extracted based on C-V characteristics of diode series. However, using our method it is possible to use C-V data for MOSFETs of different channel widths. In Fig.5 $C_{bs}(V_{GS})$ characteristics for three PMOSFETs are shown. Based on the PMOSFET layout (Fig.6) C_{bs} may be expressed by (1).

$$C_{bs} = W \cdot [L_S \cdot C_{bs,A}(V_{BS}) + C_{bs,SW}(V_{BS}) + C_{bs,G}(V_{GS}, V_{BS})] + 2 \cdot L_S \cdot C_{bs,SW}(V_{BS}) \quad (1)$$

$C_{bs,A}$, $C_{bs,SW}$, $C_{bs,G}$ denote respectively a plane junction capacitance per unit area, a sidewall capacitance per unit length and a sidewall capacitance below the gate per unit length. $C_{bs,SW}$ corresponds to the edges A-B-C-D in Fig.6 which coincide with a channel stop edge. $C_{bs,G}$ corresponds to the edge A-D. From (1) it follows, that a regression of C_{bs} against channel width W allows to determine $C_{bs,SW}(V_{BS})$ characteristics. Next, by assuming that in the accumulation $C_{bs,G}$ is negligible as compared to $L_S \cdot C_{bs,A}$, the $C_{bs,A}(V_{BS})$ may be determined. Finally, $C_{bs,G}(V_{GS}, V_{BS})$ characteristics in the non-accumulation range may be retrieved.

$C_{bs,A}(V_{BS})$ relation is typically described by (2)

$$C_{bs,A} = C_{J,A} \cdot (1 - t \cdot V_{BS}/V_{bi,A})^{-M_{J,A}} \quad (2)$$

where t switch denotes MOSFET type (+1 for NMOS, -1 for PMOS), $C_{J,A}$ is a plane junction capacitance per unit area at $V_{BS}=0V$, $V_{bi,A}$ is a built-in voltage, $M_{J,A}$ is a grading factor. An analogous formula is valid for $C_{bs,SW}$. In order to determine the parameter $C_{J,A}$, $V_{bi,A}$, $M_{J,A}$ we propose a new non-iterative method expressed by (3a), and by linear regression (3b).

$$C_{J,A} = C_{bs,A}(0) \quad (3a)$$

$$V_{BS} = t \cdot V_{bi,A} - M_{J,A} \cdot C_{bs,A} \cdot (dC_{bs,A}/dV_{BS})^{-1} \quad (3b)$$

The characteristics of the capacitance components and their parameters will be presented in the paper.

In the presented method the $C_{bs,G}$ term at accumulation is included in $C_{bs,A}$, and in effective values of $C_{J,A}$, $V_{bi,A}$, $M_{J,A}$. In our opinion it is a better solution than a standard approach, based on C-V characteristics of diode series and neglecting an effect of the gate. Next, more test MOSFETs are typically available, what improves a quality of the regression (1). Gated diode measurements may be also used in this method. However the method applicability is limited by the junction area, which cannot be too small.

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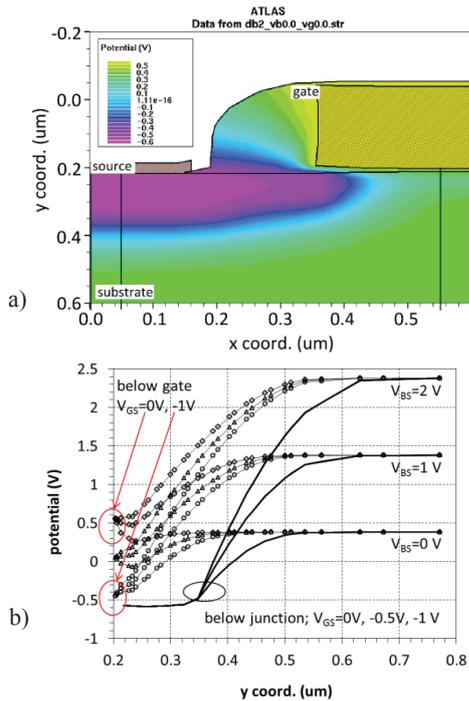


Fig.1: a) Potential distribution in p-channel MOSFET for $V_{BS}=V_{GS}=0V$; b) Potential distributions along lines as in a) for $V_{BS}=0, 1, 2V, V_{GS}=0, -0.5V, -1V$

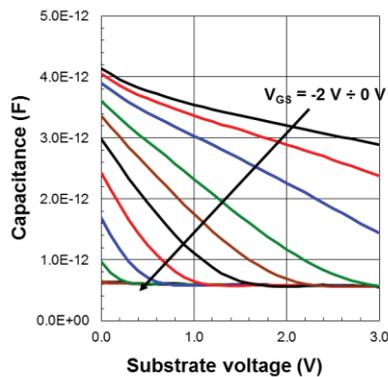


Fig.2: $C_{bs}(V_{BS})$ characteristics for p-channel MOSFET, $W=50\mu m, L=50\mu m; V_{GS}=-2..0V$

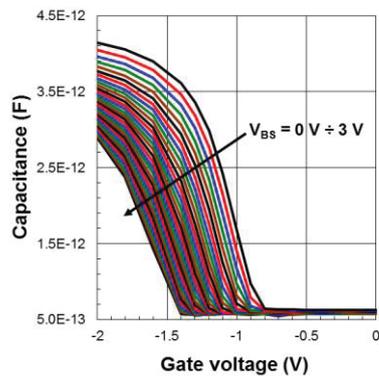


Fig.3: $C_{bs}(V_{GS})$ characteristics for p-channel MOSFET retrieved from data in Fig.2; a point of the strong inversion onset is clearly visible

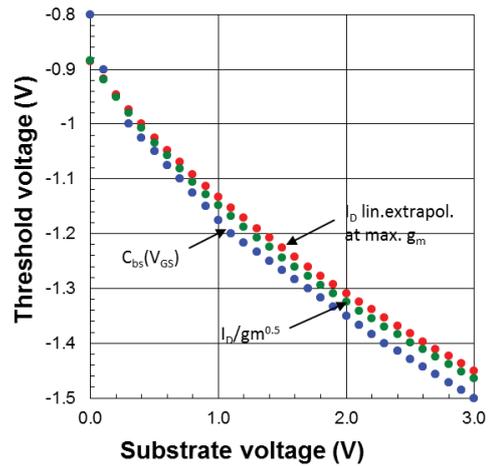


Fig.4: Threshold voltage extracted with three methods

Table 1. Threshold voltage extracted values

V_{BS}	$C_{bs}-V_G$	I_D-V_G	$I_D/g_m^{0.5}-V_G$
3.0	-1.50	-1.45	-1.46
2.0	-1.35	-1.31	-1.32
1.0	-1.18	-1.13	-1.15
0.0	-0.80	-0.88	-0.88

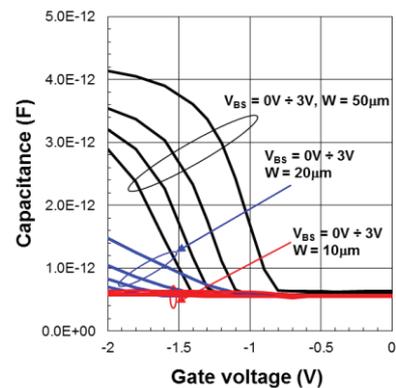


Fig.5: $C_{bs}(V_{GS})$ characteristics for p-channel MOSFETs of different channel widths

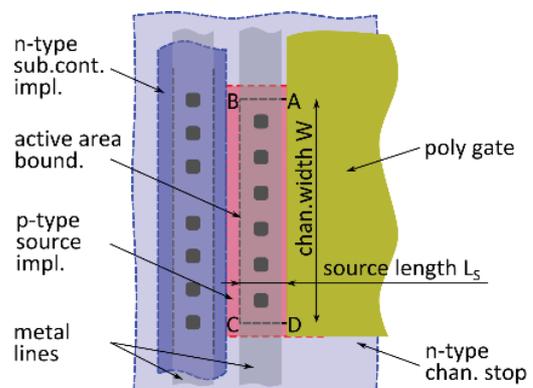


Fig.6: Part of the PMOSFET layout illustrating contribution of different parts of the source-substrate junction cap

Improvement of Silicide Resistivity for nMOSFET using In-situ Heavily Doped Si:P Epitaxial Growth

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1. Introduction

Recently, in order to overcome carrier mobility degradation of the scaled metal-oxide-semiconductor field-effect transistor (MOSFET), doped silicon epitaxial techniques such as Si_{1-x}Ge_x and Si_{1-x}C_x epitaxial growths are mainly used as stressors around the MOSFET channel. Since the atomic radius of carbon is smaller than silicon, the tensile stress caused by Si_{1-x}C_x can be applied to the channel and it enables to increase the mobility of electrons. However, Si_{1-x}C_x is not preferred for mass production due to the poor solubility of carbon in silicon body and the worst Si_{1-x}C_x epitaxial growth rate. Recently, heavily phosphorus doped silicon epitaxy has been suggested and applied to the semiconductor industry as an alternative to Si_{1-x}C_x [1-3]. Moreover, the heavily phosphorus doped Si is not only the higher tensile stressor but also the better source and drain with the lower contact resistivity. In addition, metal silicide formation of the source and drain can improve the electrical performance further.

We present here the electrical properties of nickel silicide formed on heavily phosphorus doped crystalline Si. We have found that the in-situ phosphorus-doped (ISPD) Si epitaxial growth can reduce the silicide contact resistivity significantly compared to the conventional phosphorus implantation method.

2. Experimental

Phosphorus implantation was carried out at 0 degree of tilt-angle, 10 keV of energy, and 1x10²¹ atoms/cm³. After the P implantation, annealing process was progressed by laser spike annealing (LSA) at 1150°C for curing implanted damages and activating dopants. ISPD Si with P concentration of 1x10²¹ atoms/cm³ was prepared by reduced-pressure chemical vapor deposition (RPCVD) [1]. Metal silicide layers were formed on the different heavily P doped Si (Si:P) samples using physical vapor deposited (PVD) nickel and rapid thermal process (RTP). In order to evaluate contact resistivity, circular transmission line model (CTLM) pattern was used [4]. Fig. 1 and 2 present the process flows. Fig. 3 shows the layout of CTLM pattern used in this study. The heavily doped Si:P films were analyzed by transmission electron microscopy (TEM), secondary ion mass spectroscopy (SIMS), and high-resolution X-ray diffraction (HR-XRD).

3. Results and Discussion

To compare the nickel silicide properties by the heavily doped Si:P formation methods, we prepared the Si:P films with same physical and chemical properties.

The TEM images of the both Si:P layers show that the defect-free crystalline Si:P were formed (Fig.4). Phosphorus concentration profiles by SIMS indicate that both implanted and ISPD samples have almost similar concentration level of 1x10²¹ atoms/cm³ (Fig. 5). The ISPD sample shows more uniform and abrupt dopant distribution than implantation sample. HR-XRD showed quantitative stress applied by phosphorus on substitutional sites in Si. The tensile stress amounts measured using HR-XRD were equivalent to 0.67 at% C_{sub} for the implanted Si:P and 0.69 at% C_{sub} for ISPD Si (Fig.6). Fig. 7 shows that the sheet resistivity (R_s) of the implanted Si:P is lower than the R_s of ISPD Si before metal process. However, surprisingly, the contact resistivity (R_c) results of CTLM measurement showed that silicide R_c of ISPD Si is lower than the R_c of implantation Si:P sample (Fig.8). R_c uniformity was also significantly improved in the case of ISPD Si epitaxial growth. To explain this phenomenon, we may suggest that different doping processes led different behaviors of dopant diffusion during the silicidation process. Further study will be carried out to know what the mechanism affects on the reduction of silicide R_c by the doping method.

4. Conclusion

We have found that the heavily doped Si:P samples can have comparable tensile stress when their phosphorus concentrations are similar regardless of doping methods. In contrast to the Si:P properties, silicide contact resistivity was reduced about an order of magnitude when the heavily doped Si:P was formed by ISPD Si epitaxial growth. Although implantation method has the merit of larger area doping, ISPD Si epitaxy can be suited for critical junction engineering with much improved silicide resistivity.

5. Acknowledgement

This work was supported by SK Hynix Inc. The authors thank Applied Materials, Inc. for assistance with in-situ phosphorus doped selective epitaxial growth wafer preparation.

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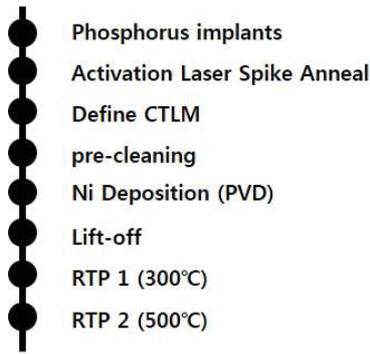


Fig.1: Process flow for P-implanted

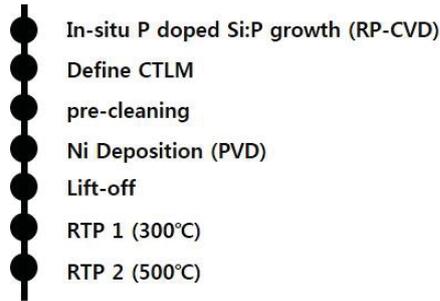


Fig.2: Process flow for ISPD

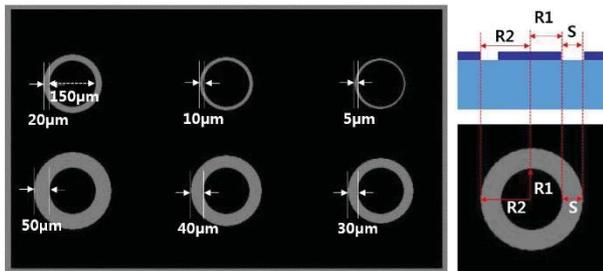


Fig.3: Layout of CTLM pattern

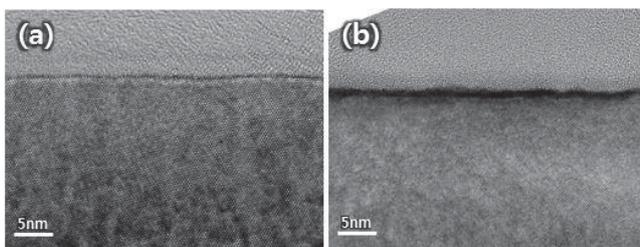


Fig.4: Cross-sectional HR-TEM image (a) P-implanted (b) ISPD

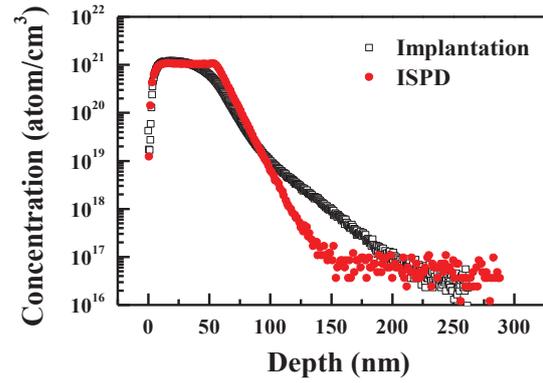


Fig.5: SIMS depth profiles of phosphorus concentration of P-implanted and ISPD Si samples.

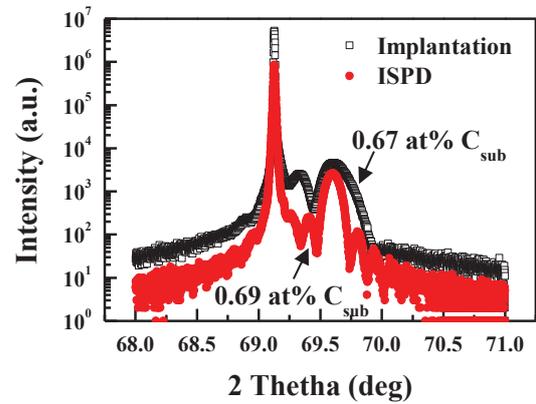


Fig.6: A comparison between P-implanted and ISPD HR-XRD plot

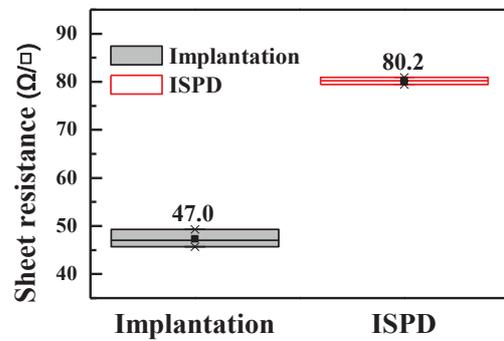


Fig.7: Sheet resistivity (Rs) before metal process

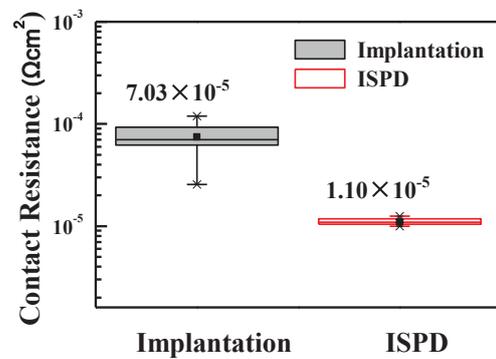


Fig.8: Distribution of contact resistance

Gated SiGe PIN Diodes Exposed to Visible Light Spectrum and Heavy-Ion Radiation

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1. Introduction

Several dimensional variations in the PIN diode structure or differences in SiGe alloy can occur as result of differences in fabrication process steps with direct impact on device response. However, environmental variables – such as exposition to visible light – and hazards – such as heavy-ion radiation – also interfere in the device response, causing circuit malfunctions if their behavior is not fully understood in order to be correctly predicted with success. This paper conducts a brief, but depth study of how these variables impact the PIN diode performance, important to space and sensor applications.

2. Experimental Gated PIN Diodes

The experimental cascades of gated PIN devices are fabricated by Global Foundries in the GF0.13 technology [1], using layout developed at FEL, experimentally characterized and also numerically simulated through Sentaurus Device TCAD Simulator [2]. Grown on top of the silicon standard bulk substrate is the active SiGe layer with doping level P- of 10^{15}cm^{-3} and peak acceptor doping concentration of $2.3549 \times 10^{17}\text{cm}^{-3}$ near interface. Anode P+ and cathode N+ doping regions are both $5 \times 10^{19}\text{cm}^{-3}$ and $0.1\mu\text{m}$ depth. The intrinsic region is $11\mu\text{m}$ long, with gate oxide dielectric EOT of 3.2nm and a thick silicon oxide layer covering the device. Four devices are measured, each containing different gate length and position. One PIN diode with full gate of $L_g=11\mu\text{m}$ and three PIN diodes with partial gate of $L_g=6\mu\text{m}$ placed in three positions on top of the intrinsic region: left, center and right. The simulation's initial mobility, recombination and electric field models for Si and Ge were adjusted based on experimental measurements.

3. Dark and Illuminated Experimental Devices

The electrical characterization was conducted using the Keithley 4200 in both dark and illuminated conditions, with the visible light spectrum (from 430nm to 770nm) used for the illuminated situation. Fig 1 to Fig 4 present the absolute cathode, anode, gate and bulk (substrate) currents in dark and illuminated conditions as a function of the anode ramp voltage V_{an} from -1V to $+1\text{V}$, for the full, left, center and right gate devices in three gate V_g biases: -0.5V , 0V and $+0.5\text{V}$, with cathode and bulk set to 0V . The light incidence increased the cathode I_{cat} and gate I_g current in several orders of magnitude with reverse bias applied due to photogeneration process and virtually no I_{an} or I_{bulk} variance, as anticipated. The bulk current falls in the expected level to the bias adopted in this work. Larger increase were noted for smaller gate lengths, which have wider windows available for light incidence, resulting in higher generated photocurrent [3]. For the full gate with $V_{an} < -0.5\text{V}$, an up to four-decade rise in the anode current I_{an} and I_{cat} occurs for $V_g = +0.5\text{V}$. Left and center gates presented similar results, with right

gate having excessively high I_g , rivaling to I_{an} and I_{cat} and almost no dependence with light incidence.

4. Process Variation Simulations

Numerical TCAD simulation models were compared and adjusted with experimental data, as presented in Fig. 5. After simulation validations, a batch of simulations were performed introducing process anomalies that replicate possible problems during fabrication process. Variation in the $\text{Si}_{1-x}\text{Ge}_x$ alloy concentrations during its epitaxial growth changes the height of barrier between semiconductor and oxide, resulting in displacement of direct bias voltage start in I_{an} , with possible compromising of correct operation mode of PIN diode, presented in Fig. 6 (a), changing the Ge proportion from 10% to 30%, causing the I_{an} shift to lower V_{an} value. The anode/cathode junction depth variation from $0.1\mu\text{m}$ to $0.01\mu\text{m}$ shifts the I_{an} direct bias to lower V_{an} and reduces the I_{an} peak value. The variation from $0.1\mu\text{m}$ to $0.5\mu\text{m}$ shifts the I_{an} in the opposite trend, as seen in Fig. 6 (b).

5. Heavy-Ion Radiation Simulations

The study of heavy-ion radiation through numerical simulations were made, applying a LET of $10\text{MeV}\cdot\text{cm}^2/\text{mg}$ [4] with radius of 50nm [5] and $V_{an} = \pm 0.5\text{V}$. The particle incidence takes place at 0.1ns and the I_{cat} peak occurs at $\sim 0.3\text{ns}$ and latter decays. The ionizing particle creates electron-hole pairs inside the active region and part of them recombines, while the remaining charge drifts, interfering on the electrical behavior of the device. Fig. 7 presents the total current density for the incidence angle of 0° at 0.1ns and at 0.3ns , showing that at first a thin layer of current is formed near gate interface. Next, most of the current generated is captured by the cathode and the peak in I_{cat} occurs (Fig 7b). In the incidence angle of 45° , the total current density is presented in Fig. 8 at 0.1ns and at 0.3ns , with rise in the total current density with the change in incidence angle and thicker current layer near gate interface. With the new incidence angle, the generated electron-hole pairs are now closer to the depletion region from cathode than for 0° angle and more susceptible to its electrostatic potential, rising almost two orders of magnitude in total current.

Conclusions

Multiple PIN diode structures with gate placed in different positions were measured and the structure with gate placed in the right side of the intrinsic region, next to the cathode region, returned as the less favorable situation, with gate leakage current levels that equals or surpasses the anode or cathode current. The center gate diode returned as a promising candidate for photodetection with gate bias of -0.5V or 0.0V , combining the larger cathode current sensitivity to visible light with the lowest gate leakage current. Calibrated numerical simulation models allowed to predict possible source of problems from fabrication

process that can result in the shift of direct bias voltage start and current overshoots following heavy-ion radiation in different angles. The gated PIN diode developed at FEI shows promising results as photodetector and with room to be implemented as a SEE radiation sensor in the near future.

This work is supported by FINEP, CNPq, CAPES and MOSIS.

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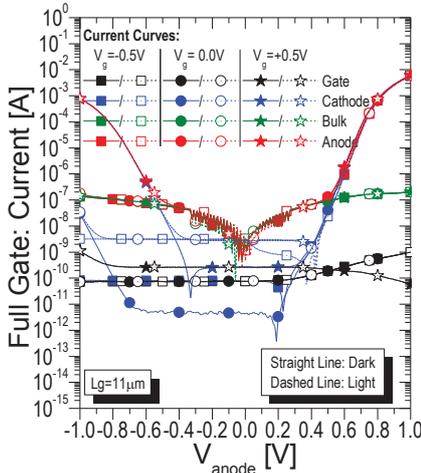


Fig. 1 – Electrical current as a function of anode ramp for full gated PIN diodes.

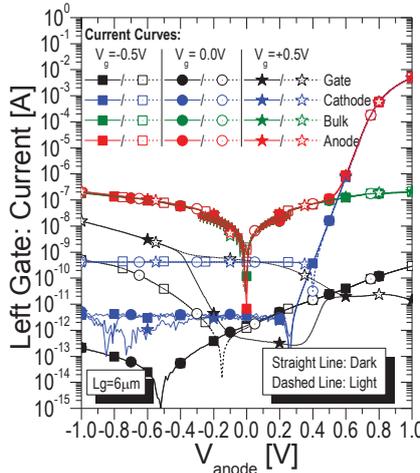


Fig. 2 – Electrical current as a function of anode ramp for left gated PIN diodes.

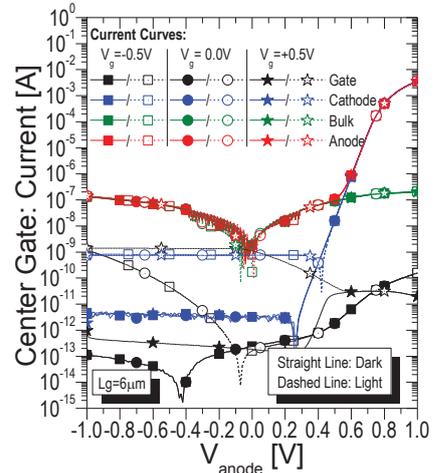


Fig. 3 – Electrical current as a function of anode ramp for center gated PIN diodes.

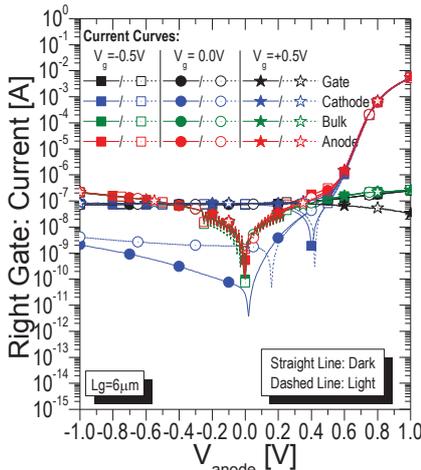


Fig. 4 – Electrical current as a function of anode ramp for right gated PIN diodes.

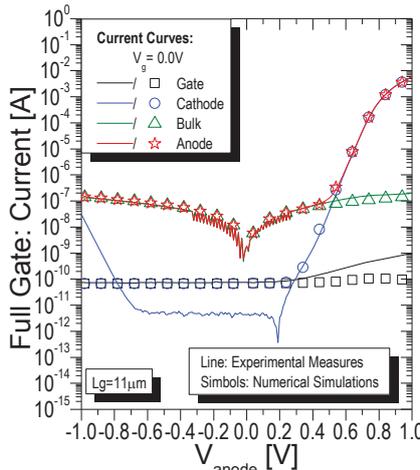


Fig. 5 – Measured and numerically simulated currents as a function of V_{anode} for full gated PIN.

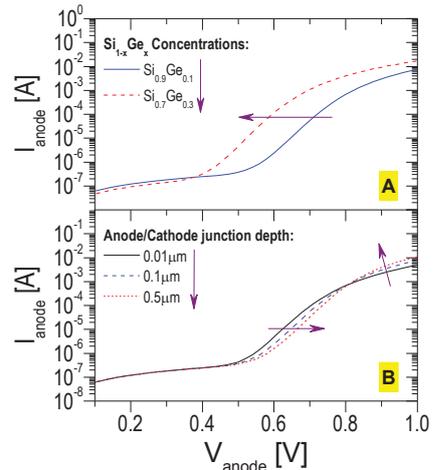


Fig. 6 – Variations in (a) $Si_{1-x}Ge_x$ concentration and (b) anode/cathode junction depth.

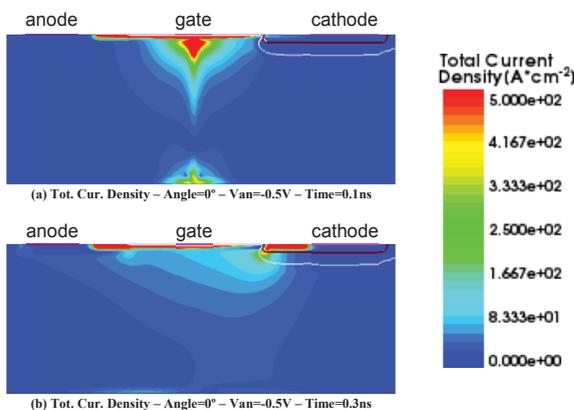


Fig. 7 – Total current density for the incidence angle of 0° at 0.1ns and at 0.3ns with $V_{an} = -0.5V$.

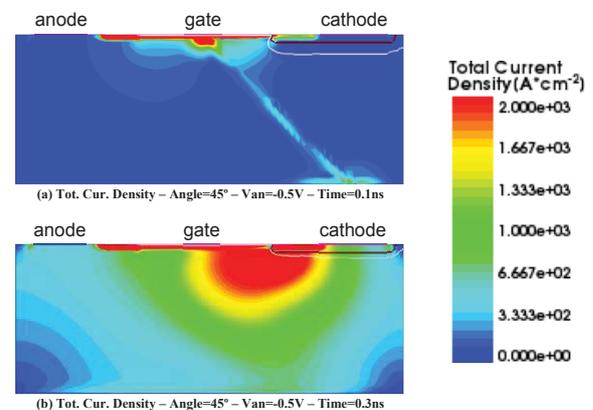


Fig. 8 – Total current density for the incidence angle of 45° at 0.1ns and at 0.3ns with $V_{an} = -0.5V$.

Recrystallization and Oxidation - Competing Processes during PECVD Ultrathin Silicon Layer High Temperature Annealing

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1. Introduction

Depending on application, different requirements on physical structure and properties of silicon ultrathin layer in double oxide barrier structure can be given. The most intriguing case is possibility of obtaining silicon nano-crystals (nanodots) in the dielectric (oxide) matrix, which can be achieved by very careful recrystallization and oxidation processes [e.g. 1-7]. As both of these processes require high temperature, they can take place at the same time, simultaneously, providing appropriate conditions are satisfied. The main difference between the conditions needed for them is presence of oxygen which obviously is required for oxidation process. It has to be realized that oxygen free conditions are very difficult to achieve. Hence, even in neutral gas annealing case this process can be expected. This work is supposed to provide grounds for practical use of annealing and/or oxidation of PECVD ultrathin silicon layers to fabricate different nanoelectronic and nanophotonic devices.

2. Experimental

In the experiment, Si (100) 5-9 Ωcm boron doped wafers were used as substrates. Atomic flat conditions of silicon wafer surface were ensured by sacrificial oxidation followed by selective oxide etch-off. Then, ultrathin layer silicon PECVD deposition was performed. Optimum conditions of this process were determined in previous works (e.g. [8, 9]). Basing on the previous results [2] we have narrowed the temperature range to between 700°C and 1000°C and limited significantly annealing time to maximum 5 minutes only. In this study the structures were annealed in 5,5N Ar.

The results of structures manufacturing was then examined by spectroscopic ellipsometry study. This method has proved already before [e.g. 2, 3, 9, 10] to be very sensitive and reliable, while fast and non-destructive, capable not only of evaluation of individual layer thickness in this multilayer structure, but, providing it is used carefully, allowing to obtain also information on the composition of the measured layers. In few individual cases, the results were also farther verified by HR-TEM observations. They did not, however, serve for collecting quantitative data on content of crystalline phase, keeping in mind that smaller than 3 nm nanocrystals cannot be successfully observed in TEM (as discussed also in [2]).

2. Results and analysis

In high temperatures as-deposited Si can undergo recrystallization. During the same process presence of

oxygen inevitably leads to silicon oxidation process. Obtained results prove that this effect cannot be ignored. This, in turn, complicates behavior of the studied system during annealing process. Consequently, amorphous silicon phase (a-Si) can either be subject of recrystallization or to oxidation (oxidation#1). It has to be realized that silicon nanocrystals (c-Si) are also prone to oxidation. Thus, this effect also has to be taken into consideration (oxidation#2). In order to understand the experimentally obtained results of annealing of structure of interest, we have to study kinetics of all three processes potentially involved shown schematically in Fig. 1.

The experiments were performed on structures with original thickness of as-deposited silicon layer thickness equal to 53 Å.

According to spectroscopic ellipsometry results (confirmed by HR-TEM), the as-deposited PECVD Si layer contains amorphous silicon phase (a-Si), as well as (limited fraction) nanocrystalline silicon phase (c-Si) and, interestingly – also - silicon oxide phase (SiO_2). In order to represent oxidation of top surface of ultrathin Si layer during annealing - (result of oxidation#1 or #2), additional SiO_2 layer was included in the optical model analysis (see Fig. 2).

The exemplary results shown in Figs.3-5 point out that in the studied annealing conditions we can observe competition of all of the expected effects. Number of significant conclusions can be drawn from the obtained results. The most significant of them are, e.g.:

- behavior of the studied system is very sensitive to any oxygen presence thus, oxidation cannot be ignored even for annealing in pure neutral gases;
- Si recrystallization kinetics is more sensitive to temperature than silicon oxidation;
- there exist conditions which allow for complete recrystallization of PECVD Si ultrathin layer;
- effective Si recrystallization is accompanied by oxidation process which consumes silicon (a-Si and c-Si), thus leading to loss of silicon phase thickness;
- careful controlling of oxygen presence in the system prior to high temperature annealing may allow for controlling the loss of silicon phase thickness.

Acknowledgements

This work was funded via National Grants by National Science Centre – DEC-2011/03/B/ST702595 (UMO-2011/03/B/ST7/02595)

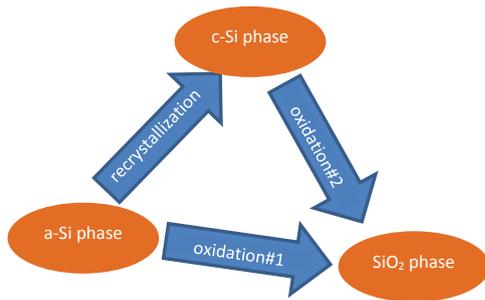


Fig. 1 Schema of effects competing during high temperature processes for PECVD silicon ultrathin layer containing structures.

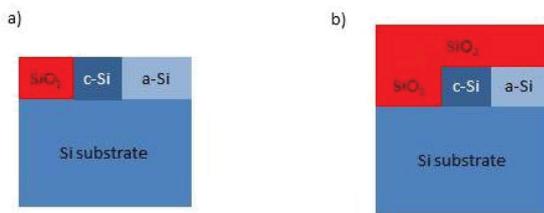


Fig. 2 Schemas of optical models used for analysis of spectroscopic ellipsometry data: a) for as deposited single PECVD Si layer parameters determination, b) for evaluation of structure properties after annealing process. In order to differentiate the two silicon oxides, the oxide phase in silicon layer will be referred to as “SiO₂ in PECVD Si”, while continuous oxide layer – “SiO₂ on top”.

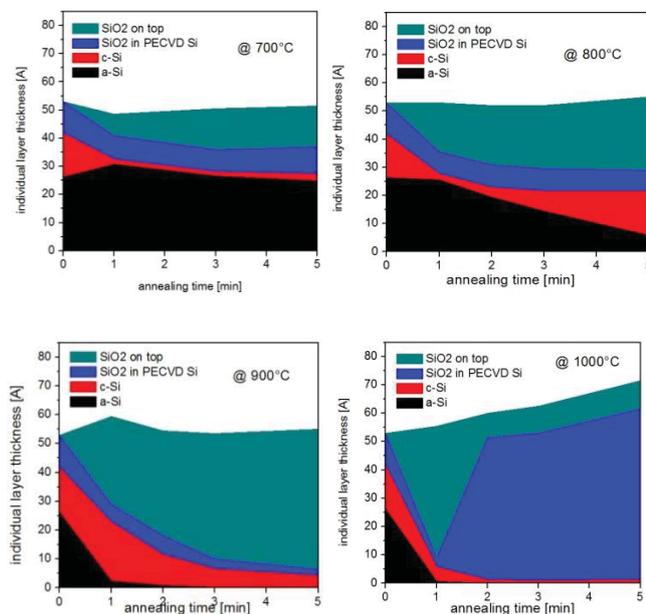


Fig. 3 Individual layers' and phases' reaction to annealing in pure argon in different temperature of PECVD Si layer. PECVD Si layer consists of a-Si, c-Si and SiO₂ in PECVD Si phases. SiO₂ on top is determined as separate layer.

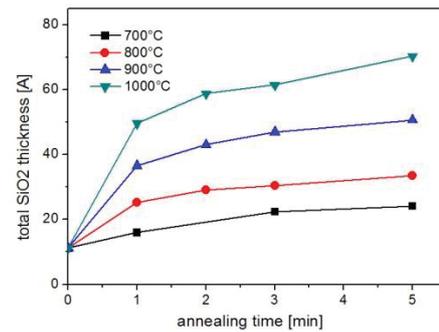


Fig. 4 Total oxide thickness (“SiO₂ on top” + “SiO₂ within PECVD Si”) changes during high temperature annealing.

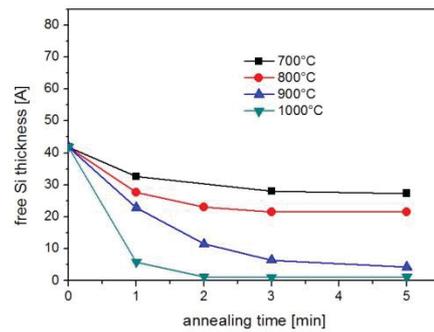


Fig. 5 Total free silicon (a-Si + c-Si) changes during high temperature annealing.

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Effect of Inner Interface Traps on High-K Gate Stack Devices Admittance Characteristics

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1. Introduction

Due to thermodynamic stability and electrical quality requirements for the substrate interface, a typical high-k gate stack comprises of an interfacial silicon dioxide layer beneath the high-k layer. In this paper, the effect of tunneling through traps located at the inner interface inside the high-k gate stack on the small-signal admittance parameters of the multilayer gate stack MIS tunnel diode is investigated by means of a theoretical model.

2. Theoretical Model

The band diagram of the considered structure is presented in Fig. 1. The applied theoretical model of the MIS tunnel diode, described in [1] and [2], is based on the steady-state analytical model [3] and a three-phase procedure utilized to determine the small-signal response. The model was expanded by including a small-signal response of the insulator traps located at the inner interface inside the gate stack, which are charged and discharged by processes of tunneling from/to the gate electrode (current J_{ST}) and processes of thermally activated elastic tunneling from/to the semiconductor conduction band (current J_{TC}) and the valence band (current J_{TV}) as depicted in Fig. 2. The calculation procedures for tunnel currents between the substrate and the gate electrode (J_{VT} , J_{CT}) utilize an analytical formula for tunnelling probability through a double-layer barrier presented in [4].

3. Discussion

The simulations were performed for gate stacks formed of metal gate, hafnium oxide and a silicon dioxide interfacial layer. The discrete (single-energy level) traps were located at the inner interface (i.e. between the high-k layer and the interfacial layer). The effect of relative location of the inner interface on small-signal admittance parameters of the considered structure are presented in Fig. 3 and Fig. 4. The parallel conductance (G_{pm}) and capacitance (C_{pm}) refer to the parallel equivalent circuit used in capacitance-voltage measurements. There is a significant peak of conductance at $x_{tr}/t_{stack} = 0.6$ (Fig. 3). It reflects the maximum efficiency of the tunnel current transport across the gate stack. In that case the current through the traps reaches its maximum (Fig. 5) and it is much more efficient than direct tunneling (J_{VT} , J_{CT}). Since the currents continuity is preserved at the trap node, for $x_{tr}/t_{stack} < 0.6$ the transport is limited by low J_{ST} value (due to the thick high-k layer). In the opposite case

($x_{tr}/t_{stack} > 0.6$), the thick interfacial layer (and thus low $J_{TC/V}$) limits the transport efficiency. If both insulator layers were made of the same material, the peak conductance would be obtained for $x_{tr}/t_{stack} = 0.5$ as was shown in [5].

If the interfacial layer is very thin (i.e. $x_{tr}/t_{stack} \rightarrow 1$) the inner interface traps act as they were substrate interface traps and their small-signal response can be observed in the inversion region ($-0.8 \text{ V} < U_g < -0.4 \text{ V}$) of the C-V (Fig. 4) and G-V (Fig. 3) characteristics.

For thick high-k layers ($x_{tr}/t_{stack} > 0.7$) there is no noticeable impact of the traps on C-V curves in the accumulation region (i.e. $U_g > 0.2 \text{ V}$). As in the aforementioned case of G_{pm} characteristics (Fig. 3), traps effect the C-V characteristic most significantly when $x_{tr}/t_{stack} = 0.6$ (Fig. 6). The discrepancies between C_{pm} and the maximum value of capacitance in the accumulation region can be clearly seen for the bias range above the flat band voltage (Fig. 6). In the case of a thin high-k layer ($x_{tr}/t_{stack} < 0.3$), there is a good agreement between C_{pm} and the maximum value of capacitance in the accumulation region, except a narrow bias range of $0.3 \text{ V} < U_g < 0.5 \text{ V}$. The sharp peak of C-V characteristic in the above mentioned bias range reflects enhanced small-signal communication between inner interface traps and the metal gate.

4. Conclusion

The presented discussion proved that the tunnel communication between the inner interface traps inside the high-k gate stack and both the gate electrode and the semiconductor substrate in many cases is significant and cannot be neglected in modelling small-signal admittance parameters of the multilayer gate stack devices.

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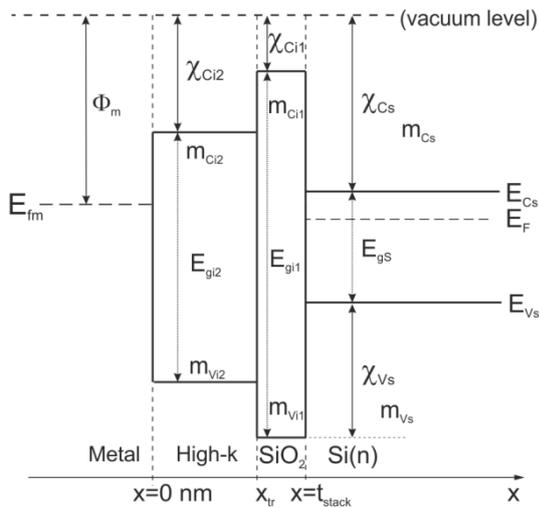


Fig.1: Band diagram of considered multilayer gate stack MIS tunnel diode.

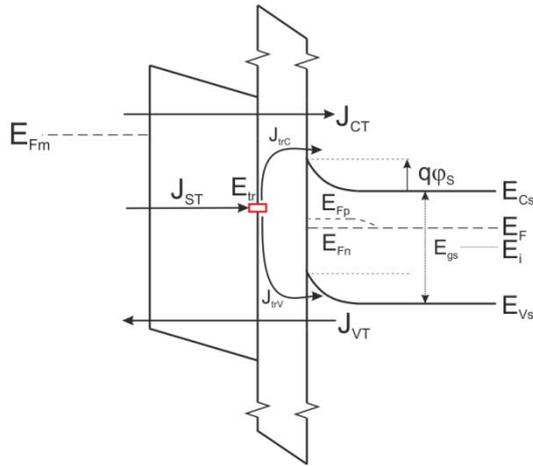


Fig.2: Currents flow implemented in the model.

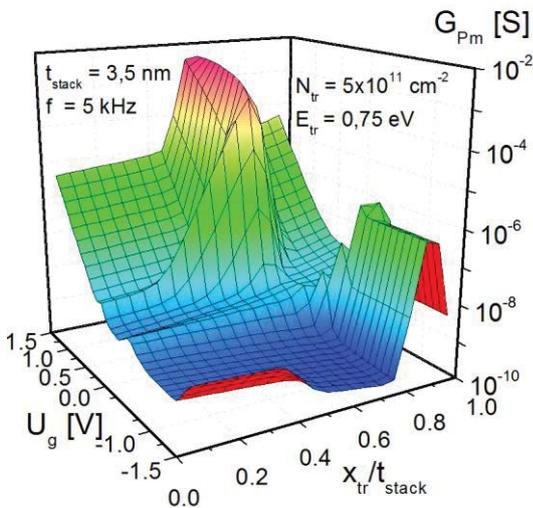


Fig.3: Simulated gate voltage dependencies of the parallel conductance G_{pm} .

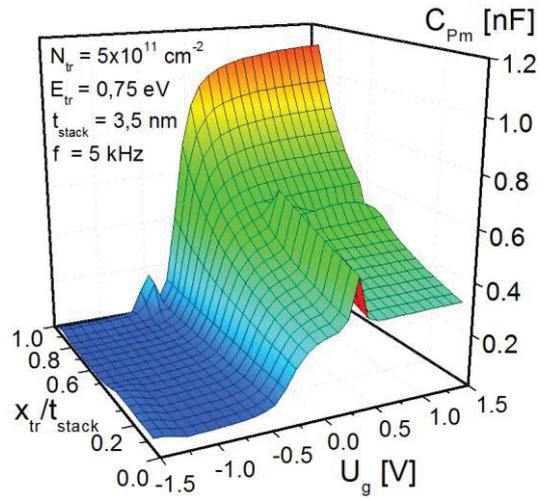


Fig.4: Simulated gate voltage dependencies of the parallel capacitance C_{pm} .

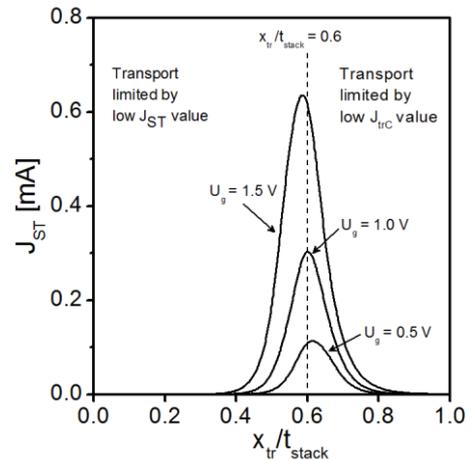


Fig.5: Simulated current via traps located at the gate stack inner interface.

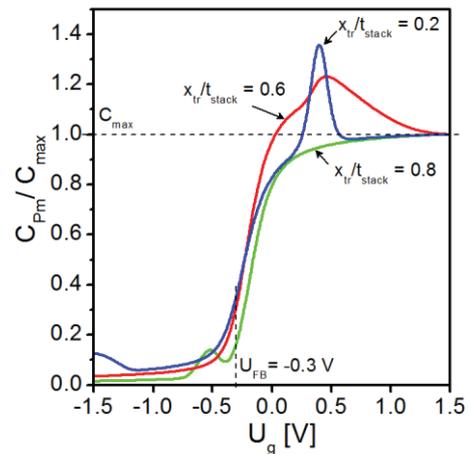


Fig.6: Normalized gate voltage dependencies of the parallel capacitance C_{pm} with x_{tr}/t_{stack} as a parameter.

Comparative Study of Vertical GAA TFETs and GAA MOSFETs in Function of the Inversion Coefficient

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Abstract

In this work, a comparative study between vertical silicon GAA TFETs and silicon GAA MOSFETs was realized, focusing on relevant analog parameters, as transistor efficiency, Early voltage, intrinsic voltage gain, unity gain frequency, and the product of the transistor efficiency multiplied by the unity gain frequency. The key parameter of comparison is the inversion coefficient (IC). The analysis was performed considering the different conduction regimes (weak, moderate and strong). MOSFETs have presented a higher transistor efficiency and a lower value of Early voltage in comparison with TFETs. In contrast, the latter technology presents a higher intrinsic voltage gain for the whole range of extracted ICs. Some other figures of merits, as the unity gain frequency and the product of the unity gain frequency and the transistor efficiency were obtained. A plateau was observed for the MOSFETs, but the TFETs transconductance and product only increase with the gate voltage.

Introduction

In order to overcome the technological limitations of conventional MOSFETs, devices with a new operation principle have been researched. The tunneling field effect transistors (TFETs) arise in this category as a promising candidate to substitute the conventional MOS devices and are based on band-to-band tunneling as the main conduction mechanism, in contrast to the drift/diffusion mechanisms of MOSFETs. This new technology presents as advantages a lower off-current and a subthreshold swing (SS) theoretically lower than 60 mV/dec, since they do not have the MOS limit due to the different operation principle [1–4].

Despite the mentioned advantages, the TFETs show a lower on-current level at high gate voltages, in comparison to the conventional devices. Therefore, new materials and new structures have been researched [5–6]. The structure studied in this work is the gate-all-around (GAA), which presents a stronger electrostatic coupling between the gate and the channel carriers in relation to the planar structure.

Although TFETs have been proposed mainly for digital applications, it has been observed that their analog behavior can be better if compared with the MOS transistors. [7–11]

In this work, the analog behavior of vertical gate all around TFETs is compared with vertical gate all around MOSFETs in terms of transistor efficiency, unity gain frequency, Early voltage and intrinsic voltage gain. The analysis was performed considering the different conduction regimes (inversion coefficient).

Device Characteristics

The studied devices were fabricated at imec, Belgium and are silicon gate-all-around (GAA) nTFETs and nMOSFETs, which use a top down vertical process flow. The gate stack consists of 3nm HfO₂ on 1nm SiO₂. The gate electrode is composed by TiN and α -silicon. Regarding their dimensions, the TFETs have a physical gate length (L_G) of 150 nm, a gate/source overlap (L_{GS}) of 30 nm, a gate/drain underlap (L_{GD}) of 50 nm and a channel length of 170 nm. The MOSFETs have a physical gate length (L_G) of 250 nm, a gate/source overlap (L_{GS}) of 140 nm, a gate/drain underlap (L_{GD}) of 50 nm and a channel length of 180 nm. The source and the drain region are doped with 1.10^{20} at.cm⁻³ boron (in the case of TFETs) and 2.10^{19} at.cm⁻³ As, respectively. The channel is doped with 1.10^{16} at.cm⁻³ As. The measured devices contain 100 nanowires in parallel and have 160 nm of diameter. The difference between the MOSFETs and the TFETs process resides in the source doping process. The source of the nMOS devices is doped with 2.10^{20} at.cm⁻³ As. The structure of the studied devices is shown in figure 1.

Experimental Results and Discussion

Figure 2 shows the transfer characteristic curves of both the tunneling and MOS transistors. As expected for silicon devices, the current level of the TFETs is approximately 4 orders of magnitude lower than the one of the MOSFETs due to the different conduction mechanisms (Band To Band Tunneling - BTBT). Since silicon has a high bandgap value, the BTBT onset voltage is high, i.e., a sufficiently high gate voltage needs to be applied to the gate in order to reach the BTBT dominated regime at the gate/source junction.

Aiming to compare the device behavior, the analog parameters analysis was performed as a function of the inversion coefficient (IC). The inversion coefficient is the normalized drain current in relation to the transition current [12]. This ratio depends on the difference between V_{GS} and the threshold voltage (V_T). Figure 3 shows the relation between the overdrive voltage ($V_{GS} - V_T$) and the inversion coefficient for the GAA MOSFET. In the case of MOSFETs, the extracted V_T is 0.48V. In the case of TFETs, the value used was the one corresponding to the BTBT onset voltage, which is equal to 1.9V. More details for the extraction method of this value can be found in [7, 13].

The first of the analyzed parameters is the transistor efficiency (gm/I_D). This parameter indicates the device capability of producing a high gain at the same power dissipation level. Figure 4 shows the experimental transistor efficiency as a function of the inversion coefficient for both technologies. One can notice that the maximum value of IC obtained for the TFET is approximately 1, due to the high value used for its threshold voltage. It is possible to observe that both technologies follow the same trend in terms of efficiency, i.e., its value decreases with the increase of IC, but the MOS devices present a higher gm/I_D than their tunneling counterparts. This occurs because the transconductance of MOSFETs is higher than the transconductance of TFETs.

The second analyzed parameter is the Early voltage (V_{EA}), which indicates the “quality” of the device output characteristic. As the tunneling mechanisms present a weaker dependence on drain voltage than the drift ones, TFETs present a better output characteristic at high V_D (higher V_{EA}). Figure 5 shows the Early voltage as a function of the gate voltage for TFET and MOSFET devices. The nMOS transistors presented V_{EA} values around -10V (almost constant over the V_{GS} range studied).

The intrinsic voltage gain (A_V) of both technologies was calculated using the following equation:

$$|A_V| \approx gm/g_{mD} \approx V_{EA} * gm / I_D$$

Based on this calculation, the curves of A_V as a function of IC, shown in figure 6, were obtained. It is possible to observe that in spite of the non-ideal behavior, the TFET in terms of I_{on} current and subthreshold slope, the intrinsic voltage gain is higher for all the conduction regimes in comparison with MOS technology. This effect happens because the Early voltage of TFETs is higher than the one of MOSFETs and compensates the lower values of transistor efficiency.

The unity gain frequency was also analyzed and was calculated using the following equation:

$$f_T = gm/2\pi C_{gg}$$

where C_{gg} is the total gate capacitance.

Figure 7 shows the curves of the unity gain frequency as a function of the inversion coefficient. The dashed curve corresponds to the simulated result. The simulation was performed in order to analyze the TFET behavior for $IC > 1$. It is noticeable that the f_T value of the MOSFET is higher than the one of the TFET. The

difference in the trend resides in the transconductance behavior variation (figure 8) for each technology. While gm suffers a degradation at high gate voltages for the MOS devices, it increases exponentially for TFETs.

One FoM (Figure of Merit) used in this work is the unity gain frequency multiplied by the transistor efficiency, presented in figure 9. The GAA MOSFET presents an optimum region (plateau) around IC = 1, while the GAA TFET presented no plateau region. It increases with IC, which is only observed for TFET devices.

Conclusions

In this work, a comparative study between GAA MOSFETs and GAA tunneling devices was presented. The analysis focused on analog parameters, such as the transistor efficiency, the Early voltage, the intrinsic voltage gain and the unity gain frequency. The parameters were compared considering the different conduction regimes. For this purpose, the inversion coefficient was utilized in the analysis.

Although the MOSFET efficiency is higher, its intrinsic voltage gain is lower in comparison with the TFET for all of the conduction regimes, due to the better output characteristic of the tunneling technology.

The MOS transistors presented a higher value of unity gain frequency for all of the analyzed inversion coefficients. Though, a

decrease of the product $f_T \times gm/I_D$ was observed for the MOS technology at higher current levels, while this product of TFETs only increased.

Acknowledgment

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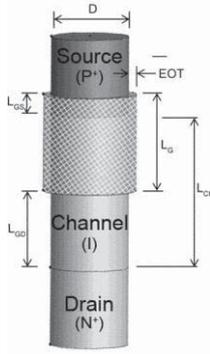


Fig.1—Structure of the devices.

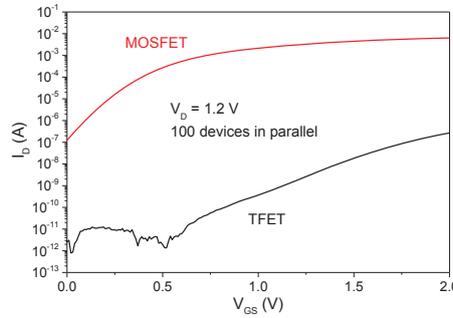


Fig.2—Experimental I_D and gm as a function of V_{GS} for GAA nTFETs and GAA nMOSFETs.

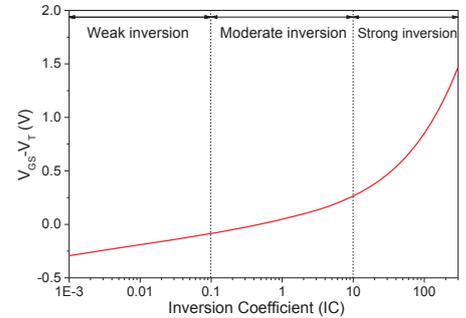


Fig.3 – Experimental $V_{GS}-V_T$ vs IC for a GAA MOSFET indicating the different conduction regimes.

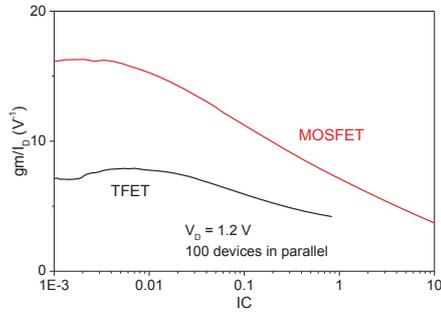


Fig.4 – Experimental gm/I_D as a function of IC for GAA TFET and GAA MOSFET.

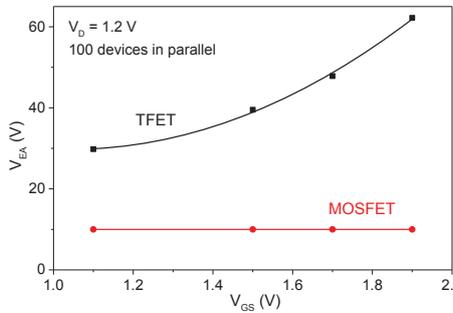


Fig.5 – Experimental V_{EA} as a function of V_{GS} for GAA TFET and GAA MOSFET.

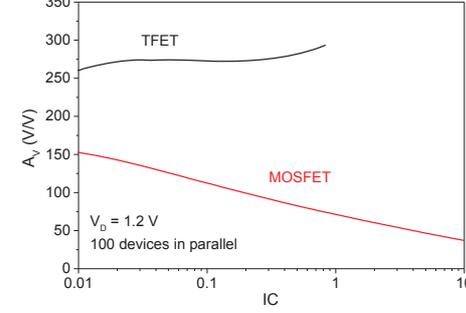


Fig.6 – Experimental A_V as a function of IC for GAA TFET and GAA MOSFET.

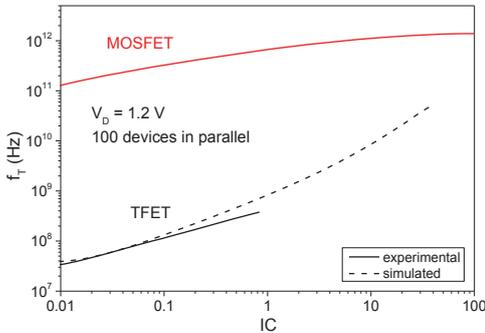


Fig.7 – Experimental and simulated f_T as a function of IC for GAA TFET and GAA MOSFET.

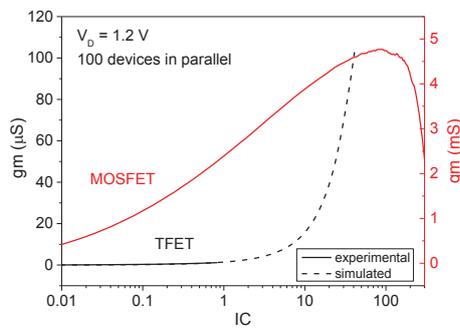


Fig.8 – Experimental and simulated gm as a function of IC for GAA TFET and GAA MOSFET.

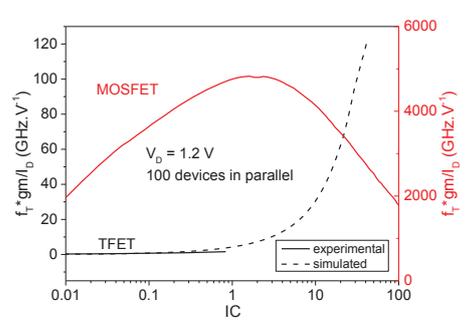


Fig.9 – Experimental and simulated $f_T \times gm/I_D$ as a function of IC for GAA TFET and GAA MOSFET.

Integration of Epitaxially Grown *in situ* Doped SiGe Layers in Monolithic 3D CMOS Fabrication

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1. Introduction

Scaling of Si based MOSFET devices has been the driving force behind the speed, power and cost requirements for CMOS applications. As devices are scaled below the 22 nm node, integration limitations rise most notably due to power consumption constraints and the negative impact of parasitic elements.

Source/drain (S/D) resistance (R_{SD}) degrades the performance of CMOS devices by reducing the ON current. Novel device architectures can boost device performance but R_{SD} is expected to dominate the total resistance along the current path. R_{SD} depends strongly on the dopant concentration at the S/D areas. Ion implantation is currently the doping method of choice but at the cost of difficulties in uniform doping profiles and risk of damaging the thin Si channel or even the buried oxide. The selective growth of *in situ* doped SiGe layers is an approach that can increase the active dopant concentration in the S/D regions while addressing the junction depth and profile issues. The aforementioned need for highly doped, shallow and abrupt S/D junctions can be fulfilled with the introduction of epitaxially grown SiGe layers [1–4]. These layers can be grown selectively on the device active areas and can be *in situ* doped. Selectivity is also an important aspect as it simplifies the fabrication process significantly and minimizes process related variability.

Low device power consumption requires supply voltage (V_{dd}) scaling and reduction of the actual interconnect length. Low V_{dd} operation can be achieved by introducing Ge as a channel layer. Compared to Si, germanium has lower band gap and higher hole and electron mobility. Threshold voltage control is more robust compared to Si since higher current flow at a lower lateral electric channel field can be achieved. Interconnect wire length related power losses are difficult to reduce without essentially shortening the physical interconnect length. This is challenging particularly for multi-level interconnect architectures. A promising solution that addresses the aforementioned issues is monolithic 3D integration by direct wafer bonding. In such a scheme the device layers are consecutively stacked on top of each other. A simple schematic for 2 device layers is shown in Fig. 1. Increased device density can be achieved for the same footprint, while at the same time reducing wire length. Such an integration, albeit without the use of Ge, has been demonstrated in [5] and indeed approximately 20%-30% reduction in power consumption can be projected.

2. Layer growth and device integration

In this work, epitaxial *in situ* doped SiGe layers grown selectively on patterned 100 mm Si wafers in a

ASM Epsilon 2000 RPCVD reactor at 650°C - 675°C. *In situ* doping includes both p- and n-type doping with boron and phosphorous respectively. Initial results show resistivity values of the order of 3 mΩcm, extracted by wafer scale Van der Pauw measurements (Table 1). AFM analysis for surface roughness and thickness was also performed and low surface roughness of < 3 nm is demonstrated (Table 1). Moreover, on MOSFET active areas ($2 \times 6 \mu\text{m}^2$), the thickness of the p+/n+ SiGe layers is 50 nm - 60 nm. Such a thickness provides a few sacrificial nm of SiGe to be consumed during NiSiGe formation. Dopant concentration was determined by SIMS and is found to be $8 \times 10^{19} \text{ cm}^{-3}$ for p-type doping and 10^{20} cm^{-3} for n-type doping. Surface preparation is a critical step in epitaxial growth. Si surfaces are cleaned *ex situ* in $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$ and HF solutions. Ge surfaces require a different cleaning approach. Standard surface clean procedures (SC-1, SC-2) contain H_2O_2 which is a known Ge etchant. Moreover Ge oxide is formed within seconds of air exposure. HF solutions are known to etch GeO_2 but complete removal of Ge sub oxides (GeO_x , $x < 2$) is challenging. HF and HCl solutions have been demonstrated to remove sub oxides [6,7]. Selective epitaxy is using Cl chemistry to achieve selective depositions and as such the potential of HCl as an *in situ* surface preparation agent will be investigated. The various cleaning methods will be evaluated also by their impact on the surface roughness via AFM measurements.

The epitaxially grown, *in situ* doped SiGe developed in this work can be integrated in fully depleted silicon on insulator (FDSOI) MOSFET fabrication process as S/D terminals (Fig. 3). Using Si, Ge, SiGe or other Ge alloys as channel materials, selective epitaxial layer growth can enable a low temperature process to fabricate low resistivity source and drain contacts.

Acknowledgments

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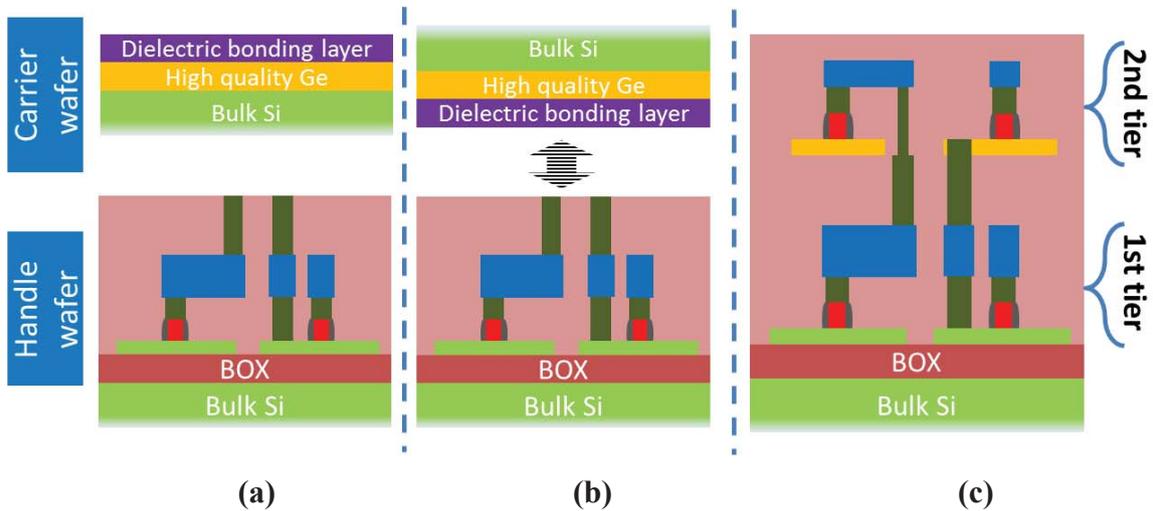


Figure 1. 3D monolithic integration using wafer bonding. The 1st device layer (tier) is fabricated on the handle wafer (a). Then the active layer for the 2nd tier is bonded on the top surface of the 1st tier (b). The resulting 2 tier device layer is shown in (c). Monolithic 3D integration can in principle facilitate the devices in $n > 2$ layers.

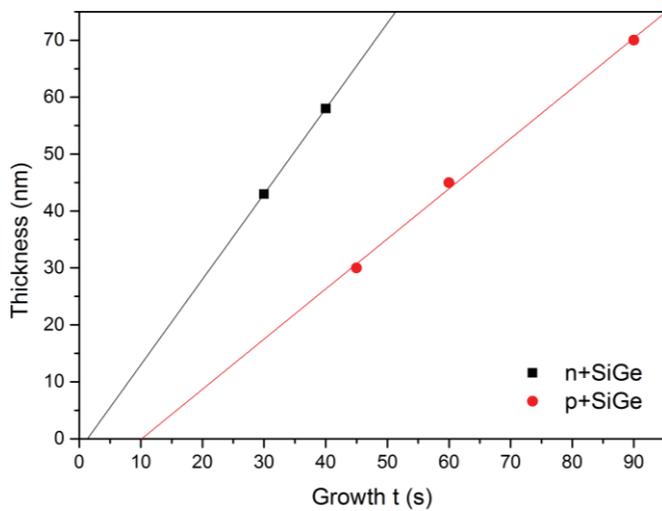


Figure 2. Growth rate of phosphorous (n+) and boron (p+) SiGe layers grown selectively on Si. The high growth are reproducible and the thickness is measured over several dies on a 100 mm Si wafer.

	P+SiGe	N+SiGe
Thickness (nm)	58	50
Roughness (nm)	2.4	2.7
Resistivity (mΩ cm)	3.5	2.5
Doping concentration (cm ⁻³)	$8 \cdot 10^{19}$	10^{20}

AFM images of SiGe selectively grown on MOSFET active area (2 x 6 μm)

Table 1. Layer properties of the epitaxially grown *in situ* doped SiGe. Doping concentration of $\sim 10^{20}$ ensures low contact resistivities.

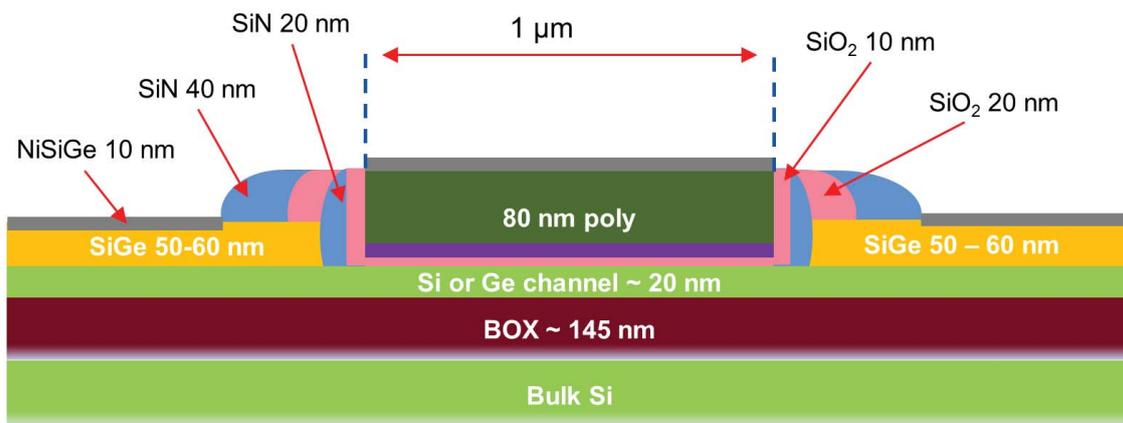


Figure 3. A simple schematic of a large gate length device with Si/Ge channel that employs *in situ* doped SiGe layers as source/drain pads.

Spin-dependent Resonant Tunneling in Ferromagnet-Oxide-Silicon Structures

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1. Introduction

Silicon, the main material of microelectronics, is perfectly suited for spin-driven applications due to its weak spin-orbit interaction and long spin lifetime [1,2]. Spin injection from a ferromagnetic electrode into *n*-silicon was claimed at room temperature [3] and also at elevated temperatures [4]. However, the amplitude of the signal extracted from a three-terminal injection method [3,4] is orders of magnitude larger than that predicted by a theory [1], provided the signal is caused by spin accumulation in silicon. Possible reasons for this discrepancy are currently heavily debated [1,5-8]. An alternative interpretation of the three-terminal signal magnitude based on spin-dependent magnetoresistance due to trap-assisted resonant tunneling was proposed [5]; however, the effects of spin dynamics and spin relaxation [6], which are important at room temperature, were not taken properly into consideration. Our goal has been to investigate the role of the spin dynamics on a trap including spin relaxation and decoherence in order to determine the trap-assisted tunneling magnetoresistance.

2. Method and Results

To highlight the role of spin relaxation and decoherence we introduce the corresponding relaxation terms into a Lindblad equation for the density matrix evolution of spin on a trap.

$$\rho = aI + a\sigma'_x + b\sigma'_y + c\sigma'_z \quad (1)$$

Here a, b, c are the spin projection expectation values on the axes x', y', z' , with the z' axis along the direction of the local magnetic field on the trap. The tunneling rate Γ_N from silicon to a trap does not depend on spin, while the tunneling rate $\Gamma_{\pm} = \Gamma_F(1 \pm p)$ from the trap to a ferromagnet depends on the spin projection $\sigma = \pm$ on the magnetization direction; here $p \leq 1$ is the interfacial current polarization in the ferromagnet. Assuming the local magnetic field on the trap is tilted by an angle Θ with respect to the magnetization (Fig.1), the following system of coupled stationary equations for the density matrix coefficients is obtained:

$$b\omega_L + c \left(\frac{1}{T_2} + \Gamma_F \right) = 0 \quad (2)$$

$$c\omega_L \cos(\Theta) - a \sin(\Theta) \left(\frac{1}{T_1} + \Gamma_F \right) - b \cos(\Theta) \left(\frac{1}{T_2} + \Gamma_F \right) = 0 \quad (3)$$

$$b \sin(\Theta) \left(\frac{1}{T_2} + \Gamma_F \right) - a \cos(\Theta) \left(\frac{1}{T_1} + \Gamma_F \right) - c\omega_L \sin(\Theta) = p\Gamma_F \alpha \quad (4)$$

$$(\Gamma_F + \Gamma_N)\alpha + p\Gamma_F(a \cos(\Theta) - b \sin(\Theta)) = \Gamma_N \quad (5)$$

Here ω_L is the spin precession Larmor frequency. The master equations include the spin lifetime T_1 and coherence time T_2 (typically $T_2 \leq T_1$). The current I due to tunneling via a trap is computed as

$$I = e\Gamma_F(1 - \alpha). \quad (6)$$

The current I differs from $I_0 = \Gamma_F \Gamma_N / (\Gamma_F + \Gamma_N)$ and depends on the angle Θ between the spin quantization axis and the magnetization orientation. Solving equations (2-6) results in the following expressions:

$$I = e \frac{\Gamma_F(\Theta) \Gamma_N}{\Gamma_F(\Theta) + \Gamma_N} \quad (6)$$

$$\Gamma_F(\Theta) = \Gamma_F \left(1 - p^2 \Gamma_F T_1 \left\{ \frac{\cos^2 \Theta}{\Gamma_F T_1 + 1} + \frac{T_2 \sin^2 \Theta (\Gamma_F T_2 + 1)}{T_1 \omega_L^2 T_2^2 + (\Gamma_F T_2 + 1)^2} \right\} \right)$$

In the case $T_1 = T_2 \rightarrow \infty$ one obtains

$$\Gamma_F(\Theta) = \Gamma_F \left(1 - p^2 \left\{ \cos^2 \Theta + \frac{\sin^2 \Theta}{\omega_L^2 / \Gamma_F^2 + 1} \right\} \right),$$

which is the corresponding expression for I from [5].

In extension to [5], (7) includes the effects of spin relaxation. When $\Gamma_F T_1 = \Gamma_F T_2 \ll 1$, the resistance dependence on the magnetic field is a Lorentzian function with the half-width determined by the inverse spin lifetime. A short spin relaxation time suppresses the “spin blockade” [5], which appeared at small Θ (Fig.2), in a similar fashion as the reduction of spin current polarization p (Fig.3). Due to the suppression of the last term in (6) at short T_2 with T_1 fixed, the amplitude of the $I(\Theta)$ modulation with Θ becomes more pronounced (Fig.4), in contrast to the intuitive expectation that strong decoherence should reduce the effect. In contrast to [5], at finite T_1 the modulation of $I(\Theta)$ is present at an arbitrary trap position relative to the contacts (Fig.5). Finally, an unusual non-monotonic dependence with T_2 of the magnetoresistance half-width as a function of the perpendicular magnetic field B , with the linewidth decreasing, at shorter T_2 is shown in Fig.6.

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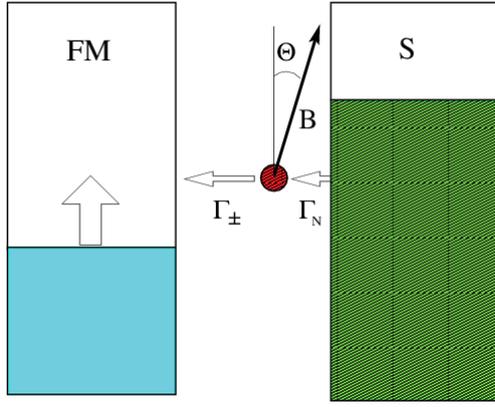


Fig.1: An electron tunnels with the rate Γ_N on the trap and Γ_{\pm} to the ferromagnet. A magnetic field \mathbf{B} defines the trap spin quantization axis OZ' , which is at an angle Θ to the magnetization orientation OZ in the ferromagnetic contact.

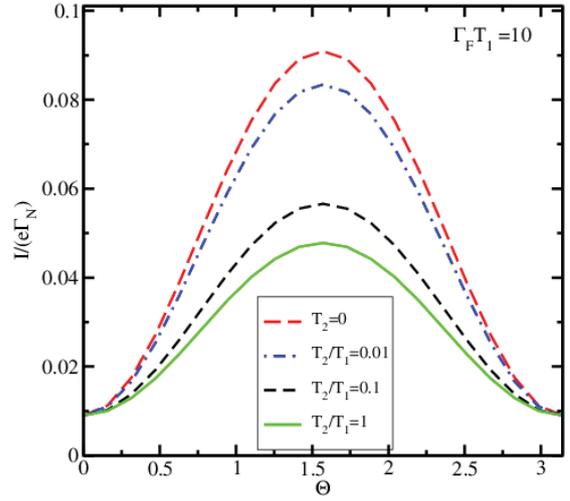


Fig.4: Current as a function of Θ , for $p=1$, $\Gamma_N/\Gamma_F = 10$, $\omega_L/\Gamma_F = 1$, $\Gamma_F T_1 = 10$, and several values of T_2/T_1 .

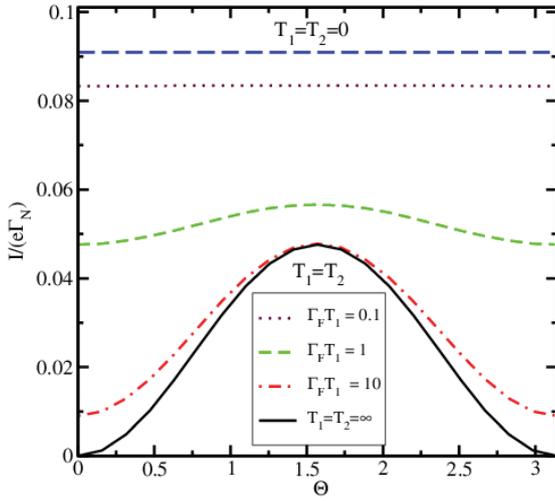


Fig.2: Current in units of $e\Gamma_N$ as a function of Θ for $p=1$, $\Gamma_N/\Gamma_F = 10$, $\omega_L/\Gamma_F = 1$, and several values of $T_2=T_1$.

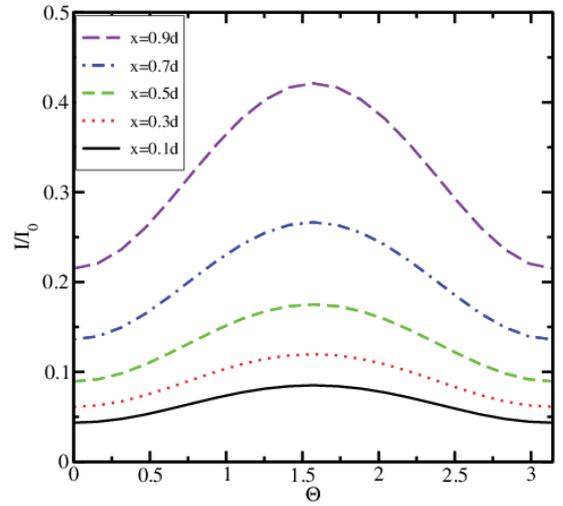


Fig.5: Normalized current as a function of the position x , for $p=1$, $\Gamma_N = \Gamma_0 \exp(-x/d)$, $\Gamma_F = \Gamma_0 \exp(-(d-x)/d)$, $T_2 = T_1$, $\omega_L T_2 = \Gamma_0 T_2 = 10$

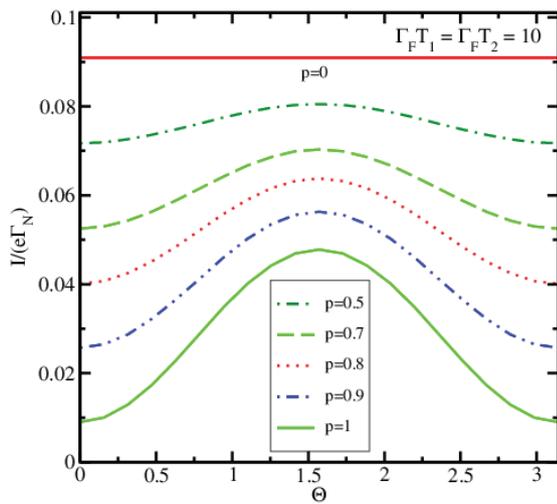


Fig.3: Current as a function of Θ , for $\Gamma_N/\Gamma_F = 10$, $\omega_L/\Gamma_F = 1$, $\Gamma_F T_1 = \Gamma_F T_2 = 10$, and several values of p .

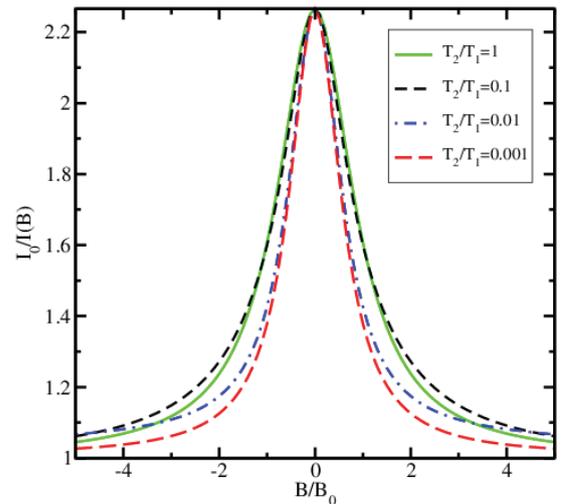


Fig.6: Magnetoresistance signal as a function of the perpendicular magnetic field \mathbf{B} for several T_2/T_1 , for $p=0.8$ and $\Gamma_F T_1 = 10$. The field \mathbf{B}_0 is parallel to the magnetization in the ferromagnet.

Finite Element Analysis at Semiconductor Die Level Modeling Heat Dissipation in an SOI Device

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1. Introduction

As semiconductor devices shrink, heat dissipation becomes ever more challenging. While that task is already difficult in bulk silicon devices, it takes on even greater difficulty in a silicon-on-insulator (SOI) device. In bulk silicon, the heat can travel through the silicon to the package lead frame. In SOI devices, however, the buried oxide and oxide trenches surrounding the device act as heat insulation, trapping the generated heat within the SOI tub. The thermal resistance of SOI devices has been seen to be as much as an order of magnitude higher than that for bulk silicon devices. [1]

Finite element analysis (FEA) is often used for package level simulations, but has gone largely unused at wafer and die level. FEA offers numerous opportunities to explore the effects of temperature, stress, and strain and to evaluate possible solutions. This paper examines use of FEA to evaluate heat dissipation in a buried N+ resistor in an SOI technology and the factors impacting temperature. “DC” and transient simulations provide information on how heat is dissipated in an SOI power structure without requiring costly and time consuming silicon fabrication.

2. The Model

The model “device” used in the simulations is a buried N+ doped resistor in an SOI structure. The N+ resistor resides in a P- doped epitaxial layer over buried oxide (BOX) and a P+ doped substrate with copper back metal. A thick oxide covers the epitaxial layer. N+ plugs contact the resistor, and metal contacts connect the resistor to mock pads with simulated bond wires. The structure is surrounded by an oxide-filled trench.

3. Experimentation

Using ANSYS Mechanical © 15.0, static (“DC”) and transient thermal-electrical simulations were run to examine the relationship between the temperature response in the resistor versus five model parameters:

- Current applied
- BOX thickness
- Contact material
- Contact opening area
- Substrate thickness

4. Results and Discussion

It is seen that finite element analysis (FEA) can be used to predict device behavior at wafer and die level, thereby alleviating the need to fabricate test silicon costing thousands of dollars and reducing cycle time of results from weeks to hours.

Increased BOX thickness resulted in greater retention of heat in the resistor and surrounding epitaxial layer. Thinner BOX permitted more of the heat to be dissipated through the P+ substrate and away from the resistor. The maximum temperature as a function of BOX thickness is seen to follow a second-order polynomial. This is consistent with previous research showing thermal resistance to be proportional to the square root of the BOX thickness (figure 4). [2][3][4]

Changes to the contact metal material were seen to have only minor impact on heating and cooling of the device. Thinning the underlying substrate offered a more significant temperature effect (figure 5).

Increases in the contact opening area resulted in improved temperature dissipation, but with diminishing returns with each increase (figure 6).

Addition of a third large contact to the center of the device, acting as a heat sink, resulted in greater heat dissipation than the equivalent addition of contact area on the ends of the device (figure 7).

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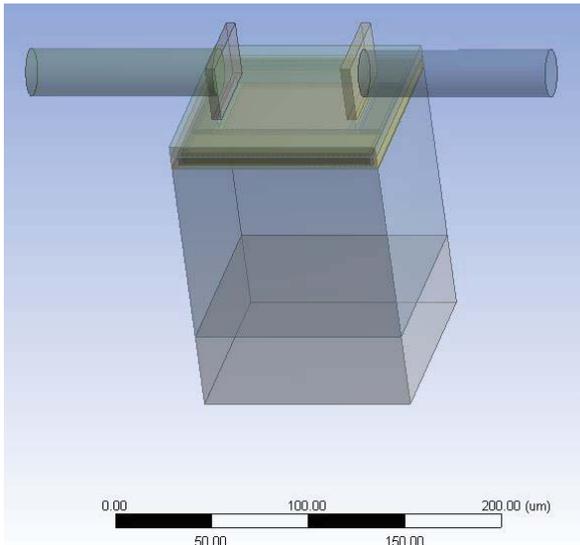


Fig.1: Model representation of the test structure

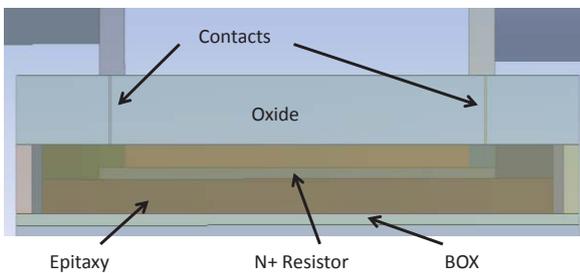


Fig.2: Test structure cross-section

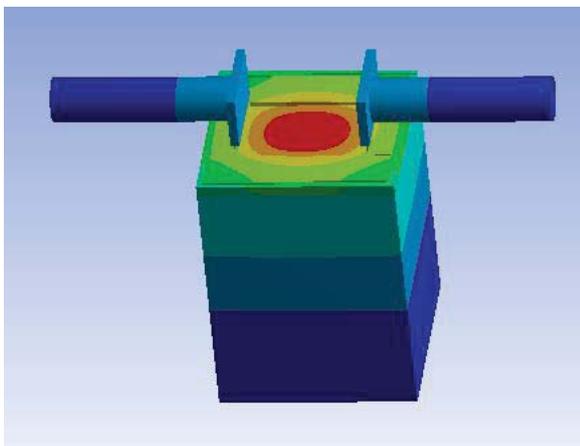


Fig.3: Example result showing "hot spot" at center of buried resistor.

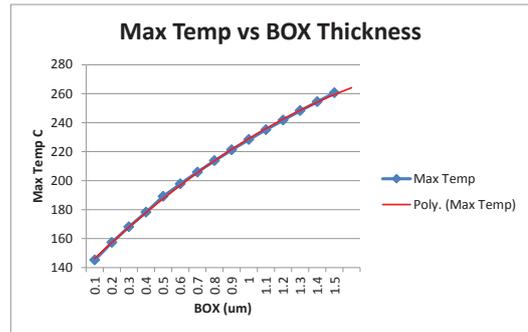


Fig.4: Model results for maximum device temperature as a function of BOX thickness

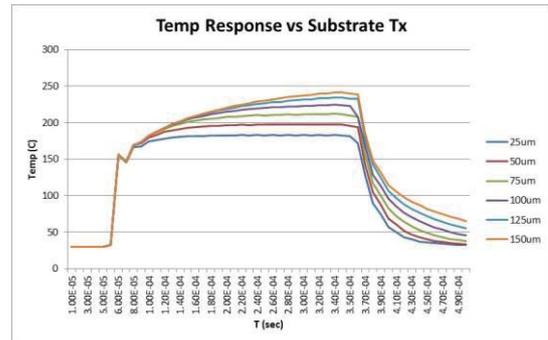


Fig.5: Transient model results for temperature over time as a function of P+ Substrate thickness

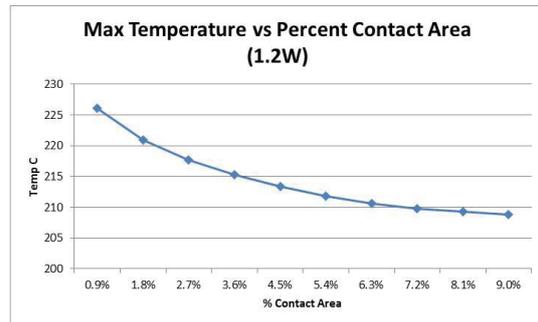


Fig.6: Maximum temperature as a function of increasing contact opening area (area expressed as a percentage of device area)

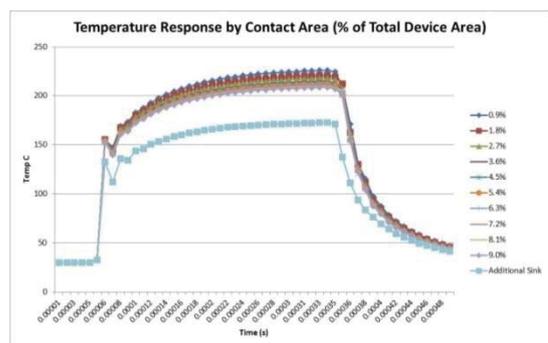


Fig.7: Transient temperature response as a function of increasing contact opening area (Also includes addition of third "heat sink" contact)

Conductivity Type Switching in Semiconductor Nanowires

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1. Introduction

Nanowires (NW) currently are one of the most implemented structures in CMOS and non CMOS applications: field-effect transistors, sensors, solar cells, photodetector switches, and thermoelectric systems. The NW structures have unique properties which are not present in bulk or thin film semiconductors. Due to large surface-to-volume ratio the surface traps play important role in whole properties of semiconductor nanowires [1-3]. Moreover, recently it was experimentally approved that due to the surface traps the conductivity can be controlled by the variation of NW diameter and at certain wire diameter the conduction type of NW changes from p to n [4]. Thus in general NW underlies surface morphology and size-dependent tunable electronic properties.

The formation of p- to n-type switching in a single NW controlled by surface roughness can be achieved by different ways. For instance, partially covering the surface of a III-V NW with wide bandgap passivation layer, to avoid the NW depletion [5], and leaving the rest of the NW surface length free of this layer thus influenced by surface traps and external factors, e.g. chemicals. This type of NW p-n-switching diodes can serve as sensitive sensors. Other way to modulate surface roughness causing p-n- switching in NW is the sharp modulation of the NW radius. However, for accurate design the dependence of NW characteristics on surface trapped charge should be well described. Recently several methods were proposed to model the influence of interface traps on device characteristics [2,3], but neither of them is accounted for minority carriers formation in NW channel.

In this paper we will theoretically study the phenomena of surface traps induced space charge penetration into the NW volume yielding fully depleted NWs for the small diameters to exhibit inverted type of conductivity.

2. Analytical analyzes of p-n-switching in NWs

We consider n-type nanowire and acceptor type surface traps. All donor impurities are assumed to be fully ionized and electrons from NW volume swept up to the surface over the existing near-surface band bending and then are captured there by unfilled surface traps. Therefore, the depletion charge layer forms near the surface which may spread deep inside the NW. When NW radius is much larger than the thickness of space charge layer the main contribution to NW conductivity is given by majority carriers from quasi-neutral n-channel near the NW core. The surface traps' effect becomes more pronounced for smaller diameters and large density of surface states when the NW becomes fully depleted and intrinsic conductivity is predicted. By further reducing the NW radius although

all the mobile electrons from NW volume were transferred to the surface states they fill only part of acceptor like surface traps, and the remaining part of surface traps start to capture electrons from valence band at given temperature. Consequently, the density of holes increases near the surface and the total number of holes in the whole volume of NW can be more than the total number of electrons (inversion and conductivity type switching).

Note that such switching as a function of diameter is possible only for the large density N_s of acceptor-like surface states: $N_s > RN_D/2$, where R is the NW radius, N_D is the density of donors.

We consider NWs with very high aspect ratio lengths, so that only radial distribution of potential is important. To describe the p-n-switching of NW we will ignore quantum effects that become important for extremely thin (<10 nm) NWs. Then partially or fully depleted and inverted NW represents an ideal situation for electrostatic analyses by solving the Poisson equation with consideration of both type of mobile charge, ionized donors and surface charge:

$$\frac{1}{r} \frac{\partial}{\partial r} \left(r \frac{\partial \varphi}{\partial r} \right) = -\frac{q}{\varepsilon_{sc}} (N_D^+ - n(r) + p(r)). \quad (1)$$

For the boundary conditions we take the electric field in the center: $\left. \frac{\partial \varphi}{\partial r} \right|_{r=0} = 0$, and on the surface: $\left. \frac{\partial \varphi}{\partial r} \right|_{r=R} = -q N_s f(E_t) / \varepsilon_{sc}$, where φ is the potential, $f(E_t)$ is the probability of occupation of interface traps at discrete energy level E_t , q -is an elementary charge.

In this stage of development we consider single discrete levels of surface traps.

The above form of Poisson equation does not admit to any closed form analytical solution. The exact solution of (1) can be done only numerically. Instead an approximate solution can be obtained using regional approach. The compact form solution for potential distribution in the form of Bessel functions has been derived. Then we numerically solve (1) with its boundary conditions in Wolfram Mathematica and compare our analytical calculations with these data. As it is illustrated in Fig.1 the agreement between the analytical model and numerical calculations is quite good.

The potential distributions for NWs with different diameters are depicted in Fig. 1. Calculations are done for GaAs NWs with different radii varying from 10nm to 120nm. Doping density is set to $N_D = 10^{17} \text{cm}^{-3}$. We consider discrete surface trap levels located close to mid-gap. The density of surface traps is set to $N_s = 10^{12} \text{cm}^{-2}$. Already at these densities the effect of surface traps becomes relevant. It is seen that developed analytical model well predicts the potential

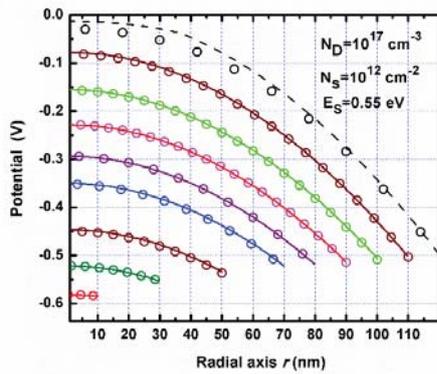


Fig.1: Potential distribution in radial direction for NWs with radiuses varying from 10nm to 120nm. Lines: approximated analytical model, circles: numerical calculations.

distribution over the large range of NW radii. The mismatch between the analytical and numerical calculations occurs at NWs with $R=120\text{nm}$ and more. This disagreement at large NW radii results from the assumptions we adopt at analytical derivation. However, NWs with such large radii are not in our interest since only a shallow space-charge depletion results from the surface states and therefore the p-n-switching effect cannot occur at these diameters. It is seen that when the NW radius is larger than 100nm at given parameters (N_D, N_S) the central part of NW is not influenced by surface traps and there is a quasi-neutral channel in the core, which provides the n-type conductivity. As smaller is the radius of NW the higher is central potential by its absolute value. For NWs with $R=30\text{nm}$ and less the central potential even is higher than the surface potential of NWs with radii more than 100nm (see Fig.1). This means that the depletion region is replaced by inverted channel which covers the total NW volume and NW switches to p-type conductivity. When it concerns to uniformly doped bulk semiconductor we described it by referring to mobile charge local concentration. But speaking about NW conduction type we cannot define it referring simply to mobile carriers' local concentration, as the carrier concen-

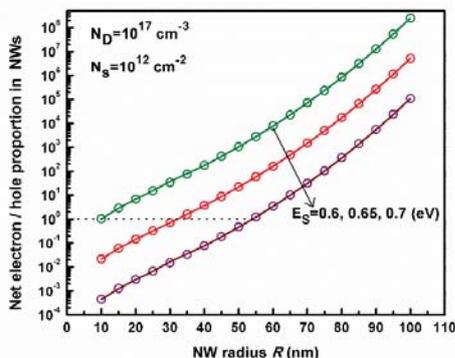


Fig.2: Net electron/hole ratio versus NWs radii calculated at different trap energies. Circles: numerical calculations, lines: derived analytical model.

tration, even at uniform doping density, can have a great variation from the surface to the NW center due to large band bending effects. Thus to define the conduction type of NW we should compare the integrated concentrations of electrons and holes over the NW radius.

The ratio of net mobile electrons over the net holes in NWs calculated for radii varying from 10nm to 100nm is illustrated in Fig.2. Calculations are done considering different positions of traps' levels within the upper half of band-gap. The curves depicted in Fig 2 introduce the calculations considering traps localized near to mid-gap energy level: with ionization energy $E_s=0.7\text{eV}$, and higher but still close to mid-gap: $E_s=0.6, 0.65\text{eV}$. It is seen that traps located at mid-gap are more effective, which is in accordance with existing literature [6]. For the given NW radius the ratio of electrons over the holes changes almost 10^3 times by varying the ionization energy with 0.1eV (see Fig.2).

It is seen that for NWs with radii varying from 40 to 70nm the amount of electrons and holes in NW is almost comparable, and thus the ambipolar conductivity is expected. The dotted line corresponds to condition when the net number of electrons and holes are equal. Following up with $E_s=0.7\text{eV}$ curve we see that at given parameters holes are majority in NWs with radii less than 35nm , and at 20nm we already have a p-type conductivity. This is in good agreement with experimental data [4], where p-type conductivity was measured for NWs with diameter less than 40nm . It is worth to note that in our calculations we choose the material and doping density in accordance with [4]. Consequently, by comparing the experimental data and our model we can estimate the surface traps density in NWs grown in [4].

In conclusion in this work we discuss the mechanism of n-p- switching in a NW due to the high density of surface traps. The developed semi-analytical model allows to perform hands-on calculations to estimate the dependence of p-n- switching on NW parameters.

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Fabrication and Characterization of InGaAs-on-insulator Lateral N+/n/N+ Structures

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Abstract – Lateral N+/n/N+ InGaAs-on-insulator structures are successfully fabricated by direct wafer bonding and selective regrowth. Electrical characterizations are performed for varying n-layer thickness from fully-depleted films up to the limit of partial depletion. Measurements under externally applied uniaxial tensile strain show an improved drive current.

1. Introduction

High-mobility channel materials such as Ge, SiGe and InGaAs are leading candidates to deliver the necessary power-performance benefits and added functionalities for future CMOS technologies and System-on-Chip applications (SoC). InGaAs-on-insulator layers are one possible approach [1] to integrate high-performance InGaAs FinFETs on Si [2] or realize hybrid InGaAs/SiGe CMOS circuits [3]. Nevertheless, those layers might suffer from additional carrier scattering compared to layers on bulk crystalline buffers such as InP [4] or InAlAs [5] owing to the presence of the back-side channel interface with the BOX. In this work, we fabricate and characterize lateral N+/n/N+ structures on InGaAs-on-insulator layers to mimic the channel transport of a MOSFET while minimizing the impact of process induced damages. The effect of InGaAs layer thickness and uniaxial tensile strain on transport characteristics are investigated.

2. Device fabrication

The lateral N+/n/N+ fabrication process mimics some of the key features of our InGaAs FinFETs process [3], such as obtained results are representative of what is expected in fully-processed devices. The n-layer is a non-intentionally doped InGaAs-on-insulator (InGaAs-OI) grown in a metalorganic vapor phase epitaxy reactor, with a background Hall carrier concentration of $2\text{-}3 \times 10^{16} \text{ cm}^{-3}$. InGaAs-OI layers on Si ($N_A = 2 \times 10^{17} \text{ cm}^{-3}$) are prepared by direct wafer bonding of nominally-undoped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ films of varying thickness (25 nm, 50 nm, 100 nm and 200 nm) grown on InP wafers as described in [6]. The BOX consists of 25 nm thermal SiO_2 , 10 nm Al_2O_3 and the high-k dielectric stack used in [2], for a resulting C_{ox} of $0.11 \mu\text{F}/\text{cm}^2$. The fabrication of lateral N+/n/N+ structures starts with the deposition of a SiO_2 hardmask to define the length of the n-region (Fig. 1(a)). Sn-doped $\text{In}_{0.53}\text{GaAs}$ N+ regions ($N_D = 5 \times 10^{19} \text{ cm}^{-3}$) are selectively grown (Fig. 1(b)) at low temperature as in [7]. The hardmask is removed (Fig. 1(c)) and a mesa isolation is performed by wet etching (Fig. 1(d)). The top interface of the n-region is formed with same high-k dielectric as used for the bottom interface. The process is completed by the deposition of a SiO_2 layer (Fig. 1(e)), contact holes and W contacts (Fig. 1(f)).

3. Electrical characterization and uniaxial strain

Back-channel measurements are carried out using the Si substrate as a back-gate. Transfer characteristics are reported in Fig. 2 for the three different InGaAs channel thickness. Although all structures present a modulation of the drain current with gate voltage, this modulation is reduced for thicker films. Indeed, the thinner channel thickness shows a clear behavior characteristic of a full-depletion of the channel with the steepest subthreshold swing, while the 200 nm thick InGaAs layers are at the limit of partial depletion since the drain current saturates for increasingly negative gate voltages. In addition, a dual V_T (at $V_g = -3\text{V}$ and $V_g = 1\text{V}$) behavior can be observed for samples with an InGaAs thickness of 50 nm and above. By comparison, the 25 nm thick sample shows a regular single V_T behavior. The peak electron mobility reaches 1100-1200 $\text{cm}^2/\text{V}\cdot\text{s}$ extracted from the transconductance in linear regime. Fig. 3(a) shows the ON-resistance which varies linearly with the channel length. Extrapolation of this curve indicates that all samples have a similar contact resistance (about $5 \text{ k}\Omega\cdot\mu\text{m}$), which is low for an InGaAs-OI sample due to the optimized process of the source/drain terminals. The sheet resistance strongly depends on thickness as illustrated in Fig. 3(b). This dependence can be explained by the presence of two parallel conduction channels [8]. Samples are diced in 2 cm x 3 mm pieces and mounted in a 3-point bending setup (Fig. 4) where uniaxial tensile strain can be applied up to 0.2 % (above, sample breaks). I_{ON} is found to increase with increasing uniaxial tensile strain applied along the $\langle 110 \rangle$ transport direction, at a rate of 10-15% per percent of strain (Fig. 5).

4. Conclusion

Lateral N+/n/N+ InGaAs-on-insulator structures are successfully fabricated and show promising transport properties, with electron mobility above $1100 \text{ cm}^2/\text{V}\cdot\text{s}$. Uniaxial tensile strain in the $\langle 110 \rangle$ transport direction increases on-current with a rate of 10-15% per percent of strain.

5. Acknowledgments

This work is supported by European projects COMPOSE³ and III-V-MOS.

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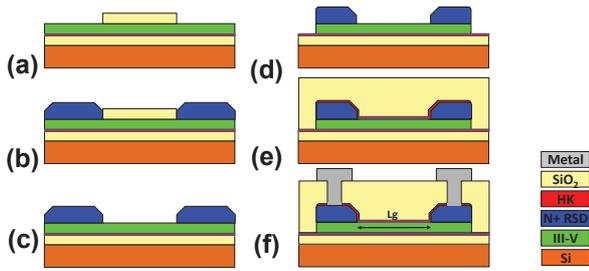


Fig. 1. Schematic of lateral N+/n/N+ test structure fabrication with (a) SiO₂ hardmask on InGaAs-OI layer with bottom passivation, (b) growth of N+ InGaAs, (c) hardmask removal, (d) mesa wet etching, (e) top passivation and interlayer dielectric deposition, (f) contact via and metallization.

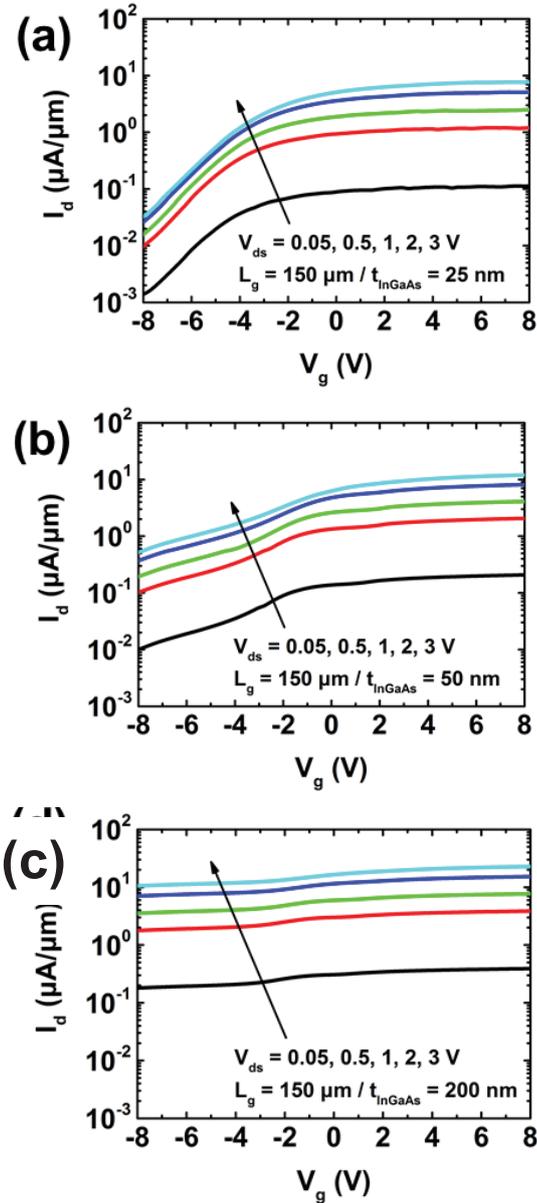


Fig. 2. I_d - V_g characteristics of lateral N+/n/N+ InGaAs-OI structures using the Si substrate as a back-gate, for (a) 25 nm, (b) 50 nm, (c) 200 nm thick InGaAs.

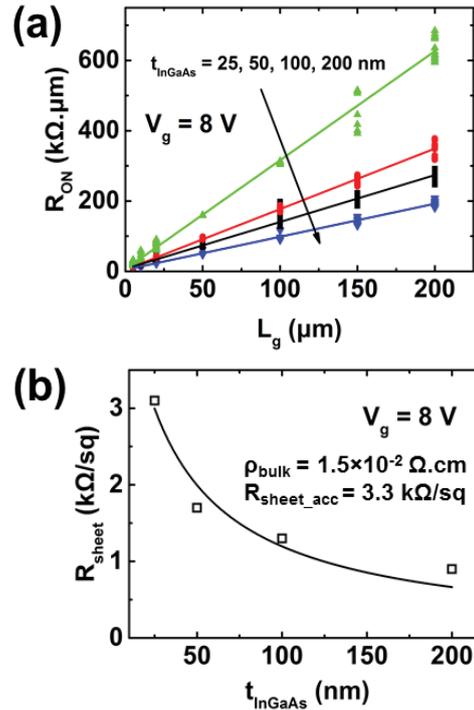


Fig. 3. (a) R_{ON} vs L_g extracted at $V_g = 8$ V and $V_{ds} = 50$ mV for 4 different InGaAs-OI thickness. (b) R_{sheet} from (a) vs InGaAs-OI thickness fitted by a two parallel conductance model.

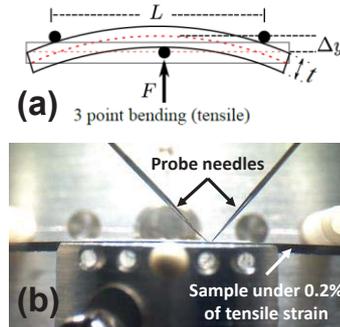


Fig. 4. (a) Schematic of 3-point bending configuration to apply uniaxial tensile strain on the sample. (b) Picture from the side of the 3-point bending setup (as in (a)) showing the vended beam of Si under tensile strain and the contact probe needles.

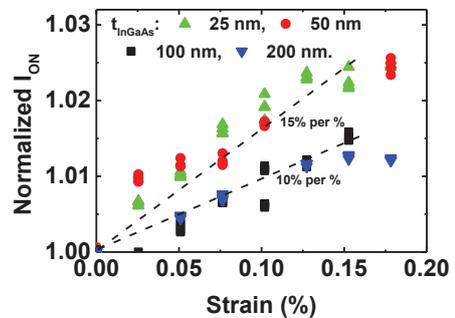


Fig. 5. Relative change of I_{ON} (at $V_g = 8$ V) vs uniaxial tensile strain for 4 different InGaAs-OI thickness.

Enhancing Electrical Performances of Metallic DG-SET Based Circuits by Tunnel Junction Engineering

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1. Introduction

This paper focuses on the Double Gate Single Electron Transistor (DG-SET) whose operation is based on the quantification of the electric charge, the quantum transport and Coulomb repulsion. These new components have exploited the phenomenon known as Coulomb blockade allowing the transit of electrons sequentially to precisely control the pumped flow. The granular nature of the electric charge in the transport of electrons by tunnel effect makes it possible to envisage the fabrication of low-power logic circuits in a high integration density. In addition to the miniaturization challenge, SETs has been known to have low driving current and low I_{on}/I_{off} ratio. In recent years, the emerging SET technology has been seen as a candidate to complement the ultimate CMOS. Moreover, the nano-damascene process is considered as a cool fabrication process that allows the co-integration of metallic SET in the BEOL with a low-power thermal budget (<450 °C) opening the way to the 3D integration [1]. In this paper, we propose to enhance the electrical performances of SET by means of its tunnel junction engineering. We demonstrate then the improved inverter's transfer function and the static noise margin (SNM) of DG-SET based SRAM cell.

2. Simulation

In this work, we consider integrating crested barrier into a metallic DG-SET to tackle these issues [2]. This unipolar approach uses the second gate in order to operate in two logical states; '0' and '1' by setting V_{G2} between $[0, V_{DD}=e/4C_G]$. In Figure 1, (a) P-type and (b) N-type DG-SET I_D-V_{G1} characteristics were simulated for $V_{G2}=GND$ (P-type) and $V_{G2}=V_{DD}=0.7V$ (N-type). SET and junction parameters are $C_{G1}=C_{G2}=0.057aF$ and $C_s=C_d=0.039aF$ for a 4-nm TiOx tunnel junction. It is conceivable to build CMOS-like standard digital or memory cells using P-SET and N-SET [3]. We will consider as the DG-SET to design elementary circuits such as DG-SET based inverter (Fig. 5) and SRAM bit-cell (Fig. 7). We thus compare the DG-SET based inverter and SRAM performances considering (i) single TiOx layer tunnel junction (ii) crested TiOx-TiO₂ barrier tunnel junction respectively (single and crested tunnel junctions are represented in Fig. 2). The DG-SET current-voltage characteristics (Fig. 3 & 4) are simulated in accordance with the orthodox theory [4, 5]. Starting from drain to source and gate voltages; the change in free energy, the tunneling event rate and the island electron occupancy probability are calculated to obtain the current characteristics [6]. Within this computation, the tunnel junction resistance was computed from the tunneling current using two approaches: (i) an analytical formulation [7] only allowing to consider single layer tunnel junction (ii) with the transfer matrix formalism for single layer or crested barriers [2, 8]. Then, the DG-SET-based inverter and SRAM simulations were obtained by using Verilog-

A model in Cadence environment. To reduce computation time, we used Look-Up-Tables (LUT) in order to retrieve current-voltage characteristics for each DG-SET.

3. Results and discussion

In order to optimize tunnel current in DG-SET, increasing driving current and I_{on}/I_{off} ratio, we will consider the use of a crested barrier tunnel junction. This junction is composed of 3nm plasma grown TiO_x which has a low dielectric constant of 3.5 and a low barrier height of 0.32eV in addition to a 1nm ALD deposited TiO₂ with dielectric constant of 35 and a barrier height of 1eV (Fig.2) [1, 9]. The dielectric constant difference between the first and the second layer is used to distribute the electric field mostly in the TiOx layer. In this way, the junction is more resistive at low applied potential because of the high potential barrier of TiO₂, but becomes very conductive at driving voltages since the TiO₂ layer becomes completely transparent with the high electric field in the TiOx layer. This junction is compared to a 4nm single layer TiO_x tunnel junction.

Thanks to tunnel junction engineering presented in this work, we are able to improve intrinsic characteristics of the nano-device as seen in Fig. 3 and Fig. 4. The I_{on}/I_{off} ratio increase is due to the reduction of the thermionic current contribution for an optimal tunneling current with different V_{DD} . The slope of the transfer function of the inverter is higher (Fig. 6) leading to a superior static noise margin of the SRAM cell (Fig. 8). Using crested barriers do not only allow better performances at circuit level (e.g. SNM in this work), but it could also contribute to consider SET technology, at least at the middle term, as a candidate to overcome power consumption and physical limitations facing CMOS technology. In term of perspectives, future works will focus on the device/circuit co-design. A thorough study with designers will be necessary to evaluate performance metrics (power consumption, delay, integration...) at large scale, and therefore bringing out the benefits of tunnel junction engineering and its impact at circuit level. The improvements shown on both device and circuits characteristics let us consider the hybrid integration of SET/CMOS logic and memory as an alternative for low-power applications such as IoT and embedded devices.

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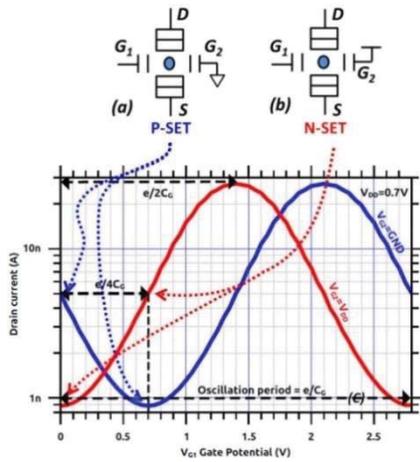


Fig.1: DG-SET configuration depending on the voltage applied to the second gate. (a) P-type. (b) N-type. (c) I_D-V_{G1} simulated data (our model) for $V_{G2} = \text{GND}$ (P-type) and $V_{G2} = V_{DD} = 0.7\text{V}$ (N-type). SET and junction parameters are $C_{G1}=C_{G2}=0.057\text{aF}$ and $C_s=C_d=0.039\text{aF}$ for a 4-nm TiOx Tunnel Junction [2].

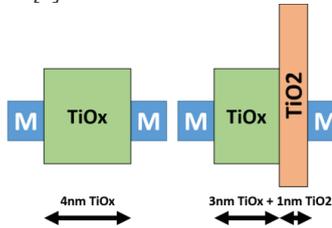


Fig.2: Cross section of the TiOx and TiOx +TiO₂ tunnel junction studied in this work

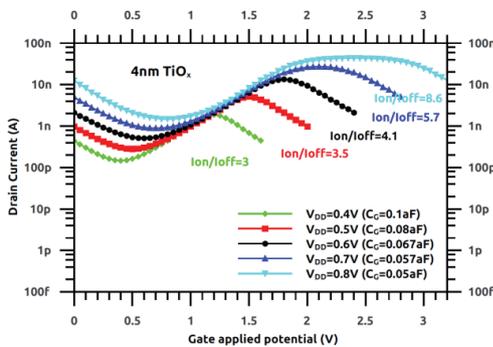


Fig.3: DG-SET I_D-V_{G1} curve and I_{on}/I_{off} ratio for TiOx tunnel junction varying the gate capacitance C_G

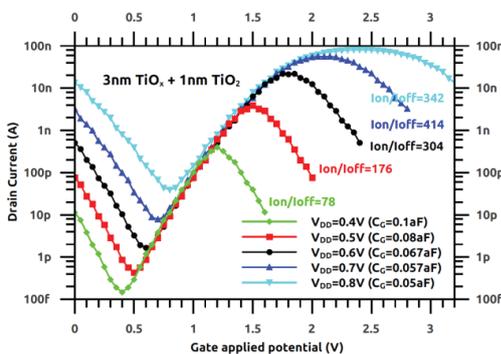


Fig.4: DG-SET I_D-V_{G1} curve and I_{on}/I_{off} ratio for TiOx+TiO₂ tunnel junction varying the gate capacitance C_G

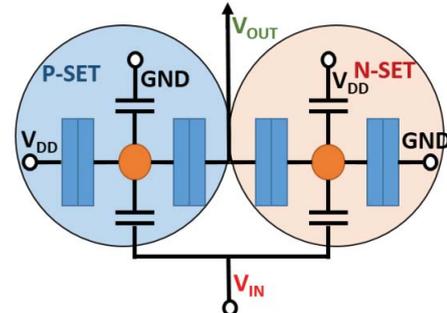


Fig.5: DG-SET based inverter schematic

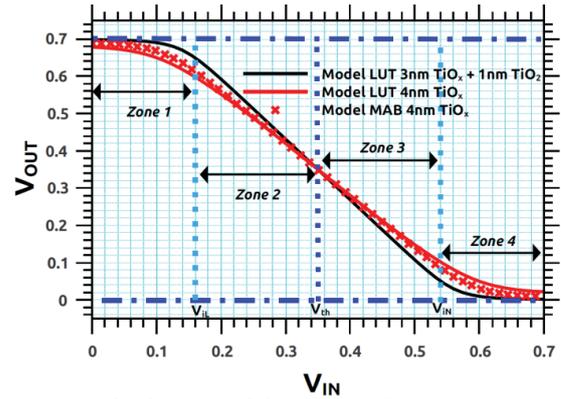


Fig.6: Transfer function of the DG-SET based inverter (MAB refers to the analytical formulation of the tunneling current [3]), LUT indicates that the model reads the data in a stored table previously calculated from Transfer Matrix method)

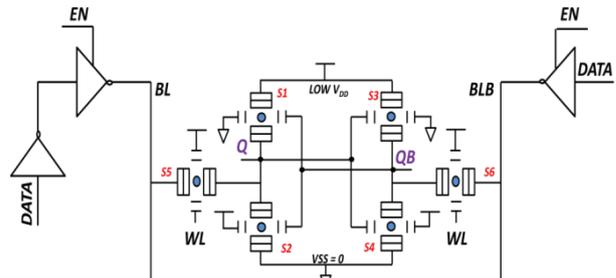


Fig.7: Schematic of the SRAM cell based on DG-SET. The circuit is composed by two N-SET access transistors, two inverters holding the stored data and tri-states buffers to manage the Read/Write cycles.

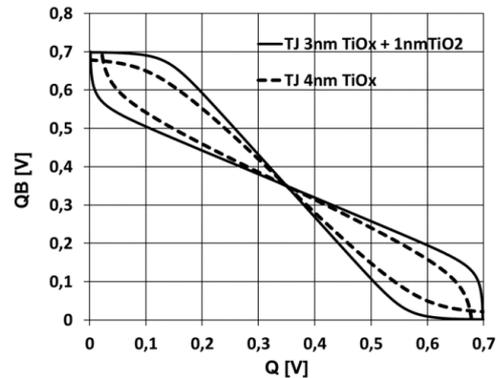


Fig.8: SRAM static noise margin butterfly curve during hold mode for TiOx single layer and TiOx/TiO₂ crested barrier. The TiOx/TiO₂ stack exhibits a better SNM window.

Transient Second Harmonic Generation and Correlation with Ψ -MOSFET in SOI Wafers

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Abstract: Silicon-on-Insulator (SOI) wafers are characterized using a non-destructive second harmonic generation (SHG) method. Correlation between the electrical parameters extracted from pseudo-MOSFET characteristics and the SHG signal is evidenced. A simple model allows reproducing the shape of the SHG curves.

1. Introduction

The characterization of interface/surface quality in SOI wafers needs to be performed non-destructively and before device fabrication. The well-established Ψ -MOSFET method can characterize efficiently the SOI electrical properties [1] but it is an invasive method. The Second Harmonic Generation (SHG) is a novel technique that could potentially lead to contactless, non-damaging characterization of SOI [2] and ultimately replace Ψ -MOSFET in the parameter extraction procedure. We have recently presented the SHG setup and preliminary data [3]. In this work, we study transient SHG signals on SOI samples with different geometries and we reproduce the measured curves using simple equations. A comparison between apparent D_{it} levels and SHG behavior is also reported.

2. Experiments & Modeling

Two sets of samples were studied: one with 18 nm Si film thickness and 25 nm BOX thickness and another with 12 nm ultrathin film and 145 nm thick BOX. Both passivated (with thermal oxide) and non-passivated (with native oxide) samples were measured. The Ψ -MOSFET technique was used to monitor the electrical characteristics and extract the D_{it} levels from the subthreshold slope [1, 4] in the $I_d - V_g$ graphs (Fig.1, Fig.2). The results are shown in Table 1.

The SHG measurements in time domain were performed using the Harmonic F1X probe provided by Femtomatrix [5]. The calculated transient SHG signals were obtained using [5]:

$$I^{2\omega}(t) = \left| |\chi^{(2)}| + |\chi^{(3)}| e^{i\theta} E(t) \right|^2 (I^\omega)^2 \quad (1),$$

where $\chi^{(2)}$ and $\chi^{(3)}$ are the non-linear interface second-order and bulk third-order susceptibilities respectively, θ is a relative phase between the 2 susceptibilities (complex numbers) and I^ω is the intensity of the incident light. The time-dependent field which gives rise to the Electric Field Induced SHG (EFISH) contribution [2] is described by [6]:

$$E(t) = Ae^{-t/t_1} - B(1 - e^{-t/t_2}) \quad (2),$$

where A and B are the initial electric fields related to traps; t_1 is the detrapping time constant and t_2 is the

trapping time constant (similar behavior with [6], but for lower doping concentration in our case).

At $t = 0$ there is a nonzero preexisting DC electric field $E_0 = A$, connected to the initial value of the SHG signal (Eq.1 with $E(t = 0) = E_0 = A$). This initial field is observed both in the model and the experiment.

The only parameters that were changed in the modeling were those in Eq.2, since the ones in Eq.1 are material dependent, thus were kept constant.

3. Results

Fig.3 shows the SHG signal of passivated and non-passivated 18 nm/25 nm SOI samples. The saturation signal (at 100s) is higher for the non-passivated sample, which can be attributed to the higher D_{it} value (lower surface quality [7]) than the passivated sample (Table 1). D_{it} is an effective value which includes the traps at the Si film/BOX interface and at the top surface via a coupling mechanism; the latter being affected by the passivation step [7]. A similar behavior was observed in [3]. Fig.4 shows the calculated curves and their associated parameters. The value of B which describes the saturation regime in the model (Fig.4) is higher for the non-passivated SOI, while the charging time is faster (smaller value of t_2).

The transient behavior of the SHG is similar in the case of the two 12 nm/145 nm SOI samples (Fig.5). The one with the worse interfacial quality (non-passivated) has a higher signal than the other (passivated). The corresponding D_{it} values are shown in Table 1. The inset of Fig.5 depicts the calculated curves along with the fit parameters. A difference is observed in the values of B (difference between the saturation values – higher B for the non-passivated sample); the SHG time evolution is qualitatively the same. It is noteworthy that in this case there is no initial discharging-like behavior as for the other sample set, which indicates the existence of other phenomena, relevant to the geometry and the processing steps of SOI wafers.

4. Conclusion

A qualitative comparison of effective D_{it} levels and SHG was established. A simple model was also shown to describe the transient behavior of the SHG signals. Our calculated curves reproduce well the transient SHG measurements obtained on different SOI geometries. This can lead potentially to a more quantitative connection of SHG with electrical parameters.

Acknowledgements.

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Table 1

SOI Sample	$\frac{D_{it}}{(\times 10^{12} eV^{-1}cm^{-2})}$
18 nm/25 nm, non-passivated	8.1
18 nm/25 nm, passivated	3.5
12 nm/145 nm, non-passivated	3.3
12 nm/145 nm, passivated	0.4

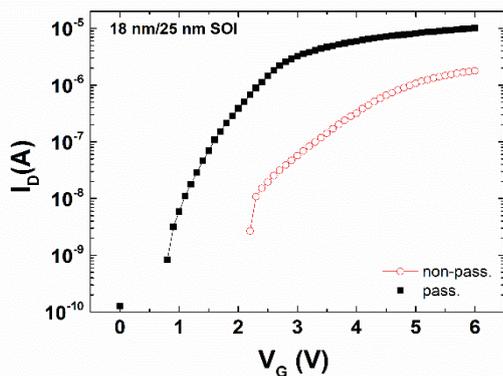


Fig.1: I_D - V_G curves obtained on 18 nm/25 nm SOI passivated (full symbols) and non-passivated (empty symbols) samples.

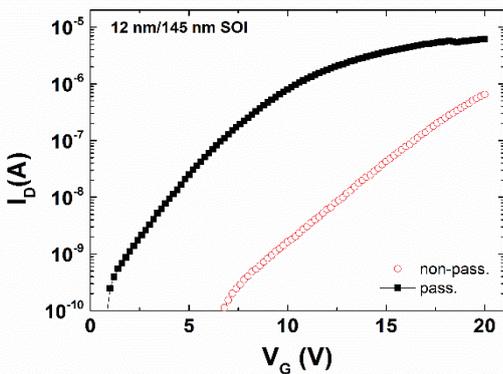


Fig.2: I_D - V_G curves obtained on 12 nm/145 nm SOI passivated (full symbols) and non-passivated (empty symbols) samples.

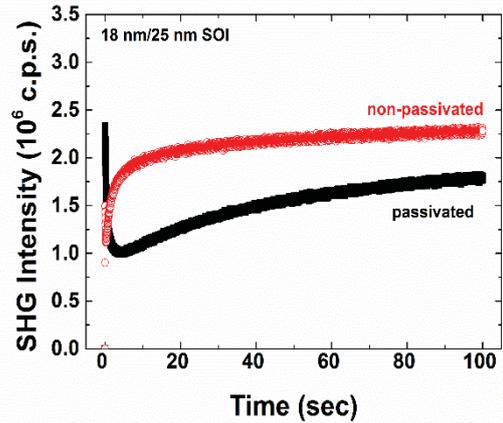


Fig.3: SHG signals from the 18 nm/25 nm SOI with native oxide on top of the Si film (non-passivated) and with a thermal oxide (passivated).

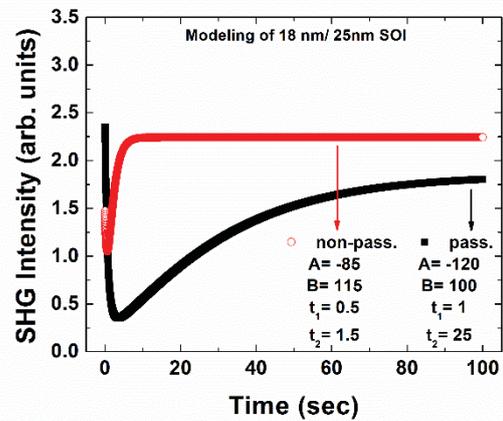


Fig.4: Calculated time dependent SHG curves showing similar behavior as in Fig.3. The parameters used in equation (2) are also shown.

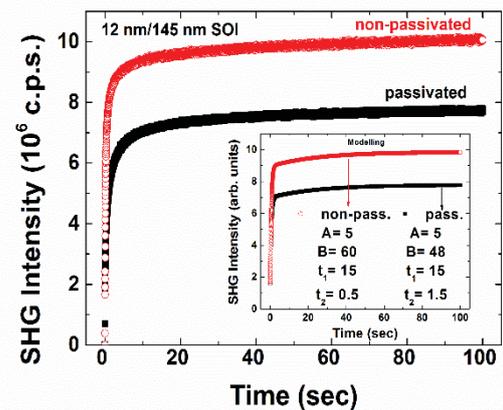


Fig.5: SHG signal from the 12 nm/145 nm SOI. The inset shows the similar calculated curves and the relevant parameters.

Geometrical Aspects of Three-Dimensional Silicon Carbide Oxidation Growth Rate Modeling

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1. Introduction

We investigate geometrical aspects of silicon carbide (SiC) and propose a direction dependent interpolation method for computing oxidation growth rates for three-dimensional simulations. Additionally, we analyze the temperature dependence of SiC oxidation for different crystal directions. Our approach is an essential step for highly accurate three-dimensional oxide growth simulations.

SiC is a wide bandgap semiconductor and has superior physical properties for power device applications, such as approximately three times wider bandgap, ten times larger electrical break-down field, and three times higher thermal conductivity, compared to silicon [1,2]. Therefore, SiC devices (e.g. MOSFETs) can better operate under high pressure, high frequency, and high temperature environments.

However, thermal oxidation of SiC is considerably more complicated compared to the oxidation of silicon [2]. There are one-dimensional oxidation models available [1,2,3,4], where the most popular one is the Deal-Grove model [3] and the more accurate Massoud empirical relation [1]. Due to their one-dimensional nature those models cannot correctly predict oxidation growth for three-dimensional SiC structures. Our approach extends these models by incorporating crystal direction dependence into the oxidation growth rate modeling.

2. Geometry of SiC

In this work we focus on the 4H-SiC polytype as it has been recognized as the most promising material for electronic high power, high frequency, and high temperature applications [3]. Geometrical aspects of SiC must be described mathematically in order to calculate growth rate variations for different crystal directions. We thus propose an interpolation method to convert an arbitrary crystal direction into a growth rate of oxidation according to known growth rates [1]. For fixed points of oxidation growth rate values we use the (0001), (10-10), (11-20), and (000-1) direction, which have been examined experimentally [1,3] and correspond to the Si-, m-, a-, and C-plane, respectively (Fig. 1). The parametric expression of the interpolation method is:

$$\begin{aligned}x &= (k_y + (k_x - k_y) \cos^2(3t)) \cos(t) \cos(u), \\y &= (k_y + (k_x - k_y) \cos^2(3t)) \sin(t) \cos(u), \\z &= k_z^+ \sin(u) \text{ for } u \geq 0, \\z &= k_z^- \sin(u) \text{ for } u < 0,\end{aligned}\quad (2)$$

where $t \in [0, 2\pi]$ and $u \in [-\pi/2, \pi/2]$ are arbitrary parametric variables and $k_{x,y,z}$ are known growth rates in x , y , and z direction, respectively. The positive and negative z coordinates are calculated separately, as the oxide growth on top k_z^+ and bottom k_z^- of the crystal are different. The proposed growth rate surface is then given by a non-linear interpolation between the known growth rate values and follows the geometry of SiC, i.e. the planes tangent to the growth rate surface at k_{Si} , k_m , k_a , and k_C are parallel to the corresponding atomic planes. It consists of a symmetric star shape in x - y plane and a tangent-continuous union of two half-ellipses in z direction (Fig. 2). The SiC oxidation growth rate surface is shown in Fig. 4 and Fig. 5, and its intersection curves with the x - y and x - z planes are shown in Fig. 3.

3. Growth Rates of Oxidation

We have obtained the growth rates of Si-, a-, and C-plane from experimentally measured data [1] and approximated the growth rate for the m-plane linearly based on published oxide thicknesses [5].

As the oxidation of SiC strongly depends on the temperature we use an Arrhenius plot to analyze the effect of temperature on the growth rates. Fig. 6 shows Arrhenius plots of the growth rates for all four SiC planes. These plots allow to directly obtain fixed growth rate values for different oxidation temperatures.

4. Summary

We have proposed an interpolation method for oxidation rates based on the SiC geometry, which converts an arbitrary crystal direction into a growth rate value. This allows to calculate SiC oxidation growth rates in three dimensions according to four known growth rate values. These vary with oxidation temperature and can be calculated with provided Arrhenius plots.

The authors wish to thank Y. Hijikata for providing experimental data. The financial support by the *Austrian Federal Ministry of Science, Research and Economy* and the *National Foundation for Research, Technology and Development* is gratefully acknowledged.

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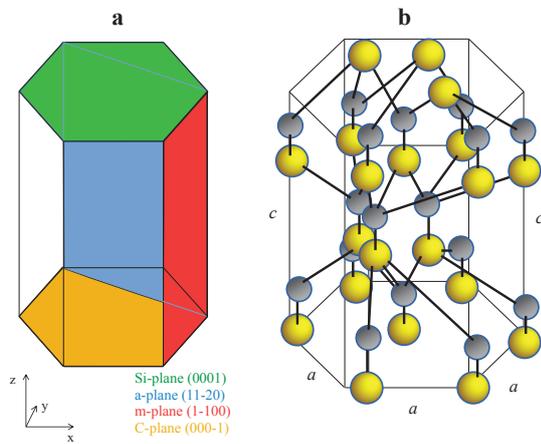


Fig.1: A schematic illustration of **a)** atomic planes of a hexagonal structure and **b)** atomistic view of a 4H-SiC polytype with sequence ABAC. Green, blue, red, and orange shapes show the Si-, a-, m-, and C- plane, respectively. Yellow spheres show the Si atoms, gray spheres C atoms, *a* is crystal dimension, and *c* is the crystal height.

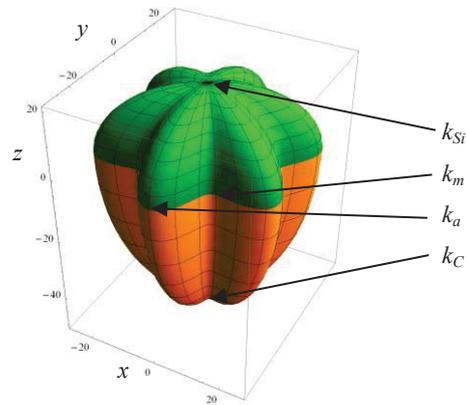


Fig.4: Three-dimensional parametric plot of 4H-SiC oxidation growth rates. An arbitrary direction growth rate is calculated according to the four known growth rates (k_{Si} , k_m , k_a , and k_C) shown with black arrows. The surface color shows calculations for positive (green) and negative (orange) *z* direction.

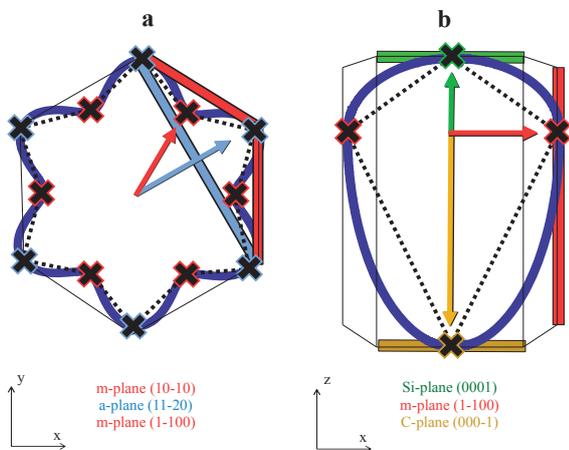


Fig.2: Schematic representation of the two-dimensional interpolation in the **a)** *x-y* and **b)** *x-z* plane. A linear (black dotted) and a non-linear (dark blue line) interpolation is used according to known growth rate values (black crosses) of Si- (green), m- (red), a- (blue), and C- plane (orange square). Colored arrows present directions towards the atomic planes.

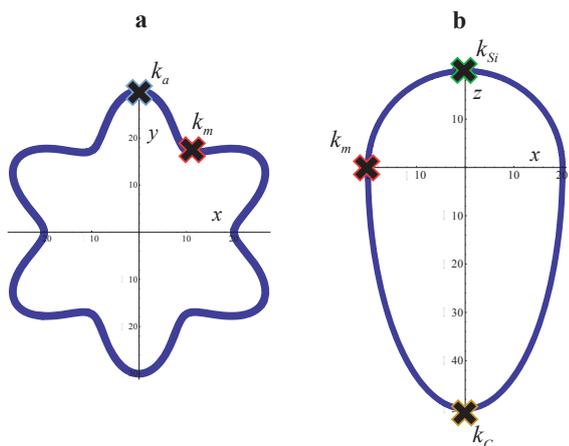


Fig.3: Two-dimensional **a)** *x-y* and **b)** *x-z* plots of 4H-SiC oxidation growth rates. Non-linear interpolation of growth rates is performed with the proposed method according to the known growth rate values (black crosses).

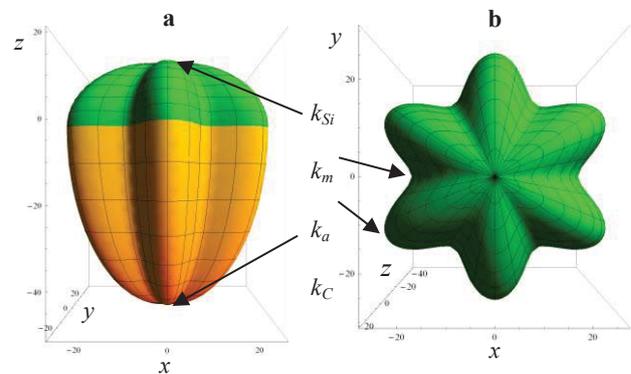


Fig.5: Three-dimensional parametric plot of 4H-SiC oxidation growth rates from **a)** side and **b)** top view. The four fixed points for the calculations are shown with black arrows. The surface color shows calculations for positive (green) and negative (orange) *z* direction.

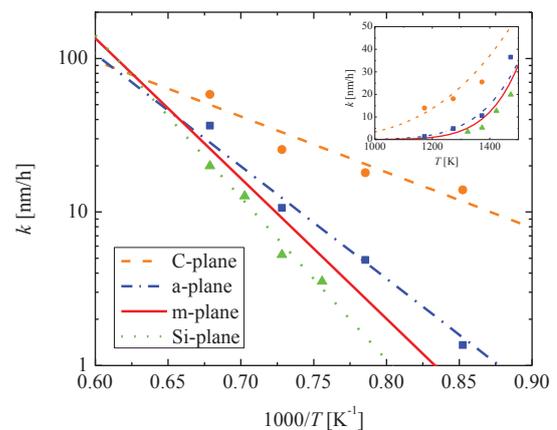


Fig.6: Arrhenius plots of 4H-SiC oxidation growth rates versus oxidation temperature for the Si- (green), m- (red), a- (blue, and C- plane (orange). Experimental data for the Si-, a- and C- plane (symbols) were obtained from [1].

On the Influence of the Back-Gate Bias on InGaAs Trigate MOSFETs

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1. Abstract

We analyze the behavior of InGaAs Trigate MOSFETs under the influence of a back-gate bias, V_{bg} . The charge distribution, the body-factor, the threshold voltage and the electron mobility dependences on V_{bg} are discussed. The InGaAs devices are benchmarked against Si ones demonstrating a higher impact of the back-gate bias for the formers.

2. Model and validation

A 2D self-consistent Schrödinger-Poisson (SP2D) solver based on the effective mass approach under non-parabolic corrections [1] has been used, including Γ , L and X valleys for $\text{In}_x\text{Ga}_{1-x}\text{As}$ ($x=0.53$) and the three pairs of anisotropic Δ valleys for Silicon. The electron mobility (μ) is calculated by solving the linearized Boltzmann Transport Equation using the implicit solution of the Momentum Relaxation Time approximation [2]. The main scattering mechanisms are considered: surface roughness (SR) [3,4], alloy disorder (AD) [5], interfacial coulomb dispersion (CO), bulk acoustic and optical phonons (PH) [6], and polar optical phonons (POP) [7] (only for the III-V material). The simulator has been validated against experimental data elsewhere [8,9]. The main parameters used in the simulations are listed in Table I, and will be applied to the trigate device geometry shown in Fig. 1. The device geometry is determined by the semiconductor width (W_S) and height (H_S), and the insulator and buried oxide thicknesses, t_{ins} and t_{box} , respectively.

3. Results

The behavior of InGaAs Trigates with $H_S=30\text{nm}$ and W_S values ranging from 5nm to 20nm is analyzed as a function of the back-gate bias. For benchmarking purposes, Si devices are also considered. For InGaAs, TaSiO_x was employed as front ($t_{ins}=2.5\text{nm}$) and buried insulator (with $t_{box}=20\text{nm}$ and 40nm). For Si, SiO_2 was used assuming the corresponding EOTs. Fig. 2 (right) represents the the threshold voltage (V_T) as a function of the back gate bias (V_{bg}). Fig. 2 (left) depicts the body factor value ($\gamma = \Delta V_T / \Delta V_{BG}$) as a function of the device width. A lower body factor (γ) is observed in thinner devices due to the poorer control of the back-gate voltage on the device channel. However, γ values close to 40mV/V can be achieved for a $t_{box}=20\text{nm}$, $W_S=20\text{nm}$ InGaAs trigate. These values are considerably higher than those achieved for Silicon structures of similar t_{ins}/t_{box} ratio and device heights [10]. The reason is mainly due to the electron charge distribution, which is plotted in Fig. 3 for the $W_S=20\text{nm}$ device, at two different back-gate biases ($\pm 2\text{V}$). As can be observed,

for the InGaAs device the charge is further from the front-gate interface and also from the lateral interfaces, because of the smaller confinement-effective mass, resulting in a stronger influence of the back-gate bias.

The influence of V_{bg} on the mobility (μ) has been analyzed in Fig. 4 for InGaAs and Si devices. It is demonstrated that positive V_{bg} can help to improve μ for large N_i values in the wider InGaAs device, but provokes a stronger degradation of the mobility at low N_i than in the Si case. As in Si, μ basically remains unchanged for $W_S=5\text{nm}$. In general, Si trigates show a more moderate dependence on V_{bg} (note the logarithmic scale and the different range of μ). Analyzing the mobility components (see Fig. 5), it can be concluded that SR scattering shows the strongest dependence on V_{bg} among all the considered mechanisms, in particular in the wider device case. Therefore, the changes on μ for the InGaAs devices can be explained according to the redistribution of the charge in the device and its proximity to the semiconductor-insulator interfaces as the back gate bias is modified.

4. Conclusions

Dynamic control of the threshold voltage as a function of the back gate bias has been analyzed as a function of the geometry and the channel material, demonstrating a higher influence as the width of the device is increased, and a stronger impact on InGaAs devices than in their Si counterparts. The role of the back gate bias on the mobility has also been analyzed: for wide devices, and in the whole range of N_i values, the influence of the back gate bias is higher in InGaAs than in Si trigates.

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Parameter	Value	Parameter	Value	Parameter	Value
m_{Γ} (InGaAs)	$0.046m_0$	E_g (InGaAs)	0.81eV	ΔE_c (Si-SiO ₂)	3.17eV
$m_{\Gamma-L}$ (InGaAs)	$1.661m_0$	ΔE_c (InGaAs-TaSiO _x)	1.97eV	Alloy Dis. V_0	0.528eV
m_{t-L} (InGaAs)	$0.115m_0$	$m_{t,\Delta}$ (Si)	0.91	Lat. SR Δ_{SR}	0.5nm
$\Delta E_{\Gamma-L}$ (InGaAs)	0.75eV	$m_{r,\Delta}$ (Si)	0.19	Top SR Δ_{SR}	0.4nm
α_{Γ} (InGaAs)	1eV^{-1}	α_{Δ} (Si)	0.5eV^{-1}	SR L_{SR}	1.5nm
α_L (InGaAs)	0.5eV^{-1}	E_g (Si)	1.11eV	N_{it} (cm ⁻²)	5×10^{11}

Table I. Relevant Si and InGaAs [10] parameters: effective mass (m), nonparabolicity factor (α), valleys gap ($\Delta E_{\Gamma-L}$), potential barrier with the insulator (ΔE_c) and energy gap (E_g). Non-polar phonons and Coulomb parameters taken from [6] (Si) and [11] (InGaAs). AD implemented after [5], with $V_0 = 0.528\text{eV}$.

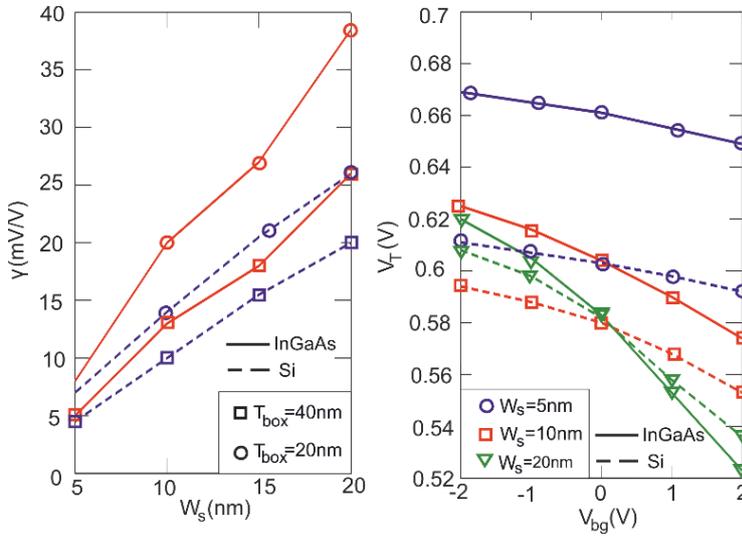


Fig. 2. Body factor as a function of W_s (left) and V_T vs. V_{bg} (right) for InGaAs and Si trigates with $H_s=30\text{nm}$. TaSiO_x (SiO₂) is used as gate and buried insulator for InGaAs (Si) devices.

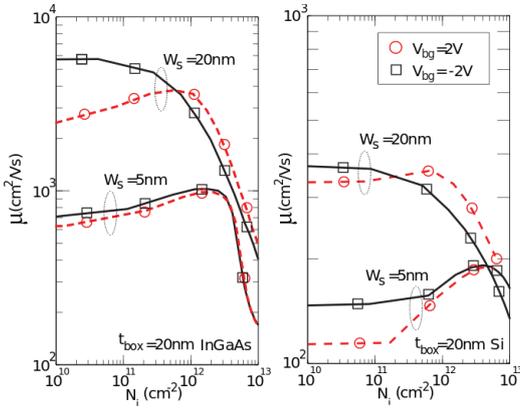


Fig. 4. Influence of the back-gate bias on μ for InGaAs (left) and Si (right) trigates, for $W_s=5\text{nm}$ and 20nm , and $V_{bg}=\pm 2\text{V}$ as function of the electron density.

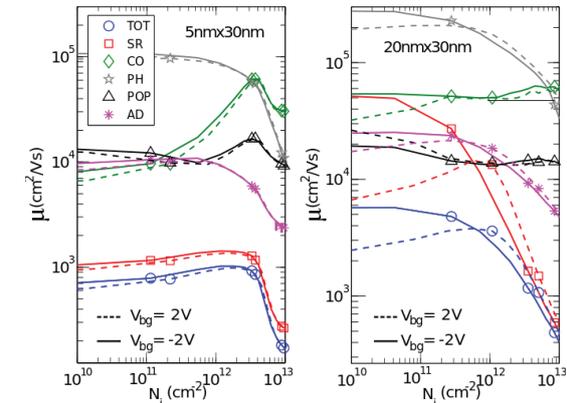


Fig. 5. Contribution of each scattering mechanism to the mobility of InGaAs trigates with $W_s=5\text{nm}$ (left) and $W_s=20\text{nm}$ (right).

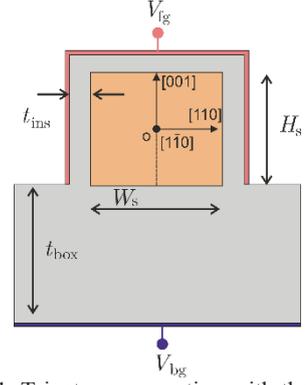


Fig. 1. Trigate cross-section with the main geometrical parameters. The device transport direction is $[1-10]$.

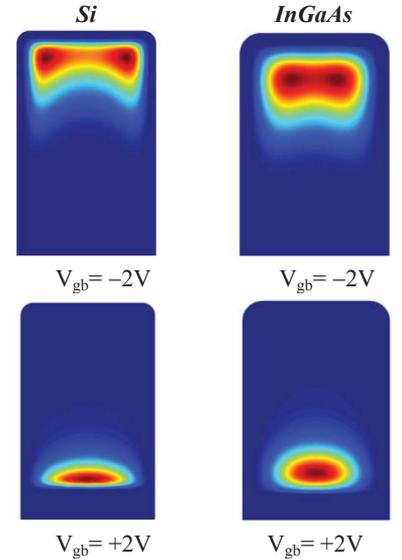


Fig. 3. Normalized charge distribution for $V_{gb}=\pm 2\text{V}$ for Si and InGaAs devices. $W_s=20\text{nm}$ and $N_i=1.25 \times 10^{11}\text{cm}^{-2}$.

Influence of Quantum Confinement Effects and Device Electrostatic Driven Performance in Ultra-scaled $\text{Si}_x\text{Ge}_{1-x}$ Nanowire Transistors

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INTRODUCTION

The gate-all-around (GAA) silicon nanowire FET structure has the potential of keeping Moore's law applicable beyond sub-5nm gate lengths. They are being investigated as an option near the end and beyond the current International Technology Roadmap for Semiconductors (ITRS). Moreover, various channel materials have been investigated in order to improve the performance [1]. One possibility is to replace the *Si* channel with Germanium- (*Ge*). *Ge* is of renewed interest as a semiconductor material to complement silicon due to its higher carrier mobility and the trend in gate dielectrics evolution [2]. *Ge* is also compatible to the existing CMOS technology which makes it easy to integrate. Moreover, using different ratio of *Si* and *Ge*, $\text{Si}_x\text{Ge}_{1-x}$, can lead to improvement of the material properties and the performance of nanowire transistors (NWT) [3]. Our main aim in this paper is to establish a link between different molar ratio of *Si* and *Ge* channel and electrostatic performance on ultra-scaled NWTs.

DEVICE STRUCTURE AND SIMULATION METHOD

The NWTs considered in this paper have similar geometrical dimensions to our recently published work [4]. All wires have a cylindrical cross-section with diameter of $D = 4$ nm. The channel has a low doping concentration in the gate region and warped with a high-*k* oxide material (Hafnium) while the source and drain region are relatively highly doped. The $\text{Si}_x\text{Ge}_{1-x}$ molar fraction which is the amount of a constituent (expressed in moles), divided by the total amount of all constituents in a mixture are varied from 10% to 90% for both *Si* and *Ge* in order to find the optimal electrostatic confinement and performance. The transport direction is along $\langle 110 \rangle$ crystallographic orientation. All NWTs have effective oxide thickness of $t_{\text{ox}} = 0.8$ nm, gate length 14 nm, spacer thickness of 5 nm, source/drain doping peak of $2 \times 10^{20} \text{ cm}^{-3}$ and channel doping of 10^{15} cm^{-3} . 3D view and the design parameters for all simulated devices are presented in Fig. 1 and Table 1 respectively.

Our simulations are based on a Poisson-Schrödinger (PS) quantum correction technology achieved in a drift-diffusion (DD) module of the GSS 'atomistic simulator' GARAND [5]. The PS model is coupled with the GARAND DD solution in stages to allow a computationally efficient manner of combining the impact of quantum confinement and carrier transport. To achieve this the DD simulation is carried out until convergence, then the quasi-Fermi level from

the converged DD solution is used as a fixed reference within the PS model to transfer the current transport behavior. The PS model is then solved until convergence to obtain a QM solution of the charge density. After this the QM charge density is used to obtain a fixed 'quantum correction' term. Using the fixed 'quantum correction' the DD simulation is carried out again until convergence is obtained.

RESULTS AND DISCUSSION

Fig. 2 shows the capacitance-voltage (C-V) characteristics for all simulated NWTs. Fig. 3 presents the gate voltage dependence of the mobile charge in the channel. As expected the mobile charge (Q_M) and the gate capacitance (C_G) increases with increasing gate voltage. Moreover, both the Q_M and C_G reveal their dependence on the *Si/Ge* molar fraction. In order to fairly evaluate the impact of the *Si/Ge* concentrations on the NWT's performance, Table 2 compares Q_M and C_G ($V_G = 0.60$ V) for identical Q_M ($V_G = 0.0$ V). To make this comparison fair, the $Q_M(V_G)$ curves are aligned by modifying the gate work function. From Table 2 the following important conclusions can be obtained. Firstly, $\text{Si}_{20}\text{Ge}_{80}$ has the highest C_G and Q_M/C_G ratio. Secondly, increasing *Ge* concentration leads to almost linear increase of Q_M/C_G ratio. Q_M/C_G ratio is an indicator for the 'intrinsic' NWT's speed. Higher value of the ratio means better 'intrinsic' speed.

The impact of the gate length on the drain-induced barrier lowering (DIBL), defined as $\Delta V_T/\Delta V_D$, and sub-threshold slope (SS) is illustrated in Fig. 4. There is a relatively little difference in the electrostatic behavior between the NWTs with different *Si/Ge* fraction. Fig. 5 presents the electron concentration and electrostatic potential for all devices along the transport direction. The charge in the channel and the potential increase with increasing *Si* concentration. Fig. 6 reveals the 2D charge distribution in the middle of the channel for all devices. The data show that the charge difference is not significant between various NWTs.

In summary, in this paper we have studied the impact of quantum mechanical effects on the electrostatic driven performance of $\text{Si}_x\text{Ge}_{1-x}$ NWTs at the sub 5-nm CMOS technology. By varying the *Si/Ge* molar fraction in NWTs, we established a link between the quantum confinement effects and the electrostatics in those devices. The NWT with $\text{Si}_{20}\text{Ge}_{80}$ combination has the highest Q_M/C_G ratio, the lowest DIBL and sub threshold slope (SS), which makes it the best choice from all other devices.

T _{oxide} (nm)	0.8
Gate Diameter (nm)	4
Gate length (nm)	14
Spacer thickness (nm)	5.0
S/D peak doping (cm ⁻³)	2×10 ²⁰
Channel doping (cm ⁻³)	10 ¹⁵
Substrate orientation	001
Nanowire orientation	110
Channel material	Si _x Ge _{1-x}
Drain voltages	0.05V, 0.7V

Table 1 Parameters of the simulated devices.

	$Q_M (\times 10^6 / \text{cm})$	$C_G (10^{-11} \text{F/cm})$	$Q_M / C_G (10^{17} / \text{F})$
Si	1.13008	3.864140	2.92453
Si ₉₀ Ge ₁₀	1.15170	3.897476	2.95499
Si ₈₀ Ge ₂₀	1.15990	3.927255	2.95346
Si ₇₀ Ge ₃₀	1.16580	3.953547	2.94874
Si ₆₀ Ge ₄₀	1.17150	3.976392	2.94614
Si ₅₀ Ge ₅₀	1.17870	3.999063	2.94744
Si ₄₀ Ge ₆₀	1.18690	4.014751	2.95635
Si ₃₀ Ge ₇₀	1.19790	4.026970	2.97469
Si ₂₀ Ge ₈₀	1.21280	4.03570	3.00517

Table 2 Q_M ($V_G=0.60\text{V}$), C_G ($V_G=0.60\text{V}$) and Q_M/C_G ratio at identical Q_M ($G_V=0\text{V}$) for NWTs at $L_G=14\text{nm}$.

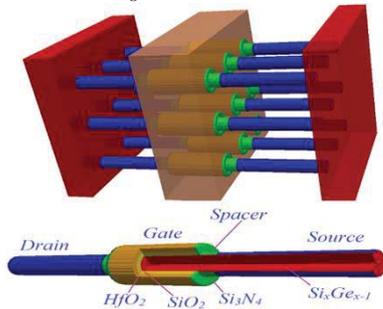


Fig. 1 3D schematic view of the circular NWT (down) and NWTs array (up).

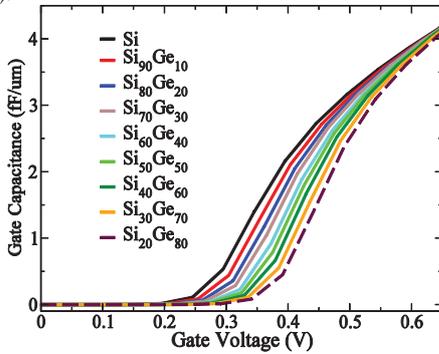


Fig. 2 Gate voltage dependence of the capacitance of all GAA NWTs at $L_G=14\text{nm}$ channel length.

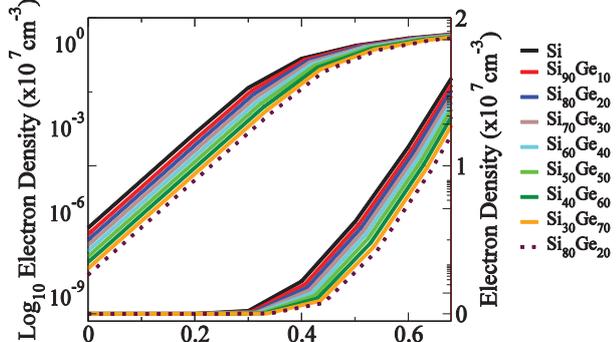


Fig. 3 Gate voltage dependence of the mobile charge of all GAA NWTs at $L_G=14\text{nm}$ channel length.

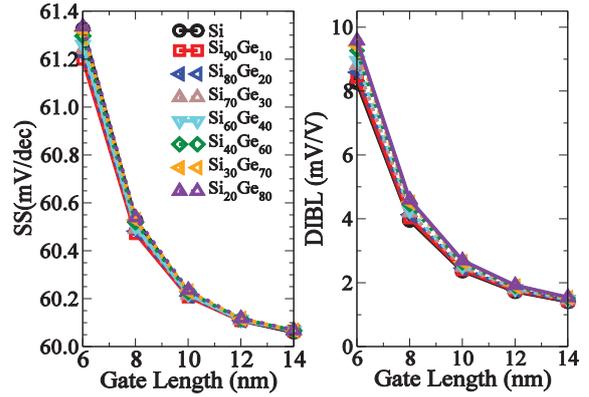


Fig. 4 Impact of Si/Ge concentration on the SS (left) and DIBL (right) for the circular nanowire.

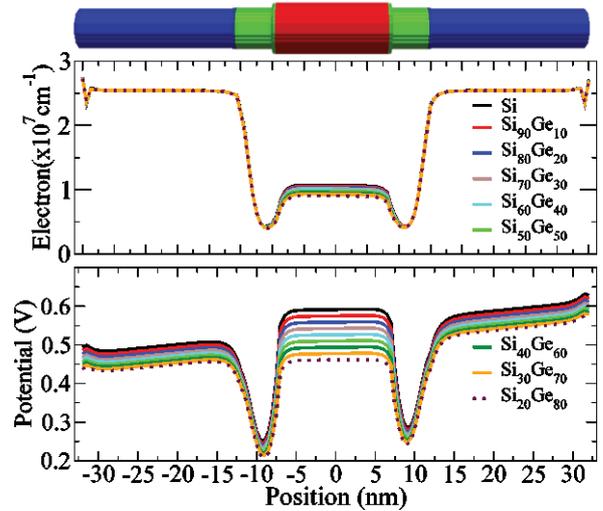


Fig. 5 Electron concentration (top) and electrostatic potential (down) along the transport direction of Si_xGe_{1-x} NWTs.

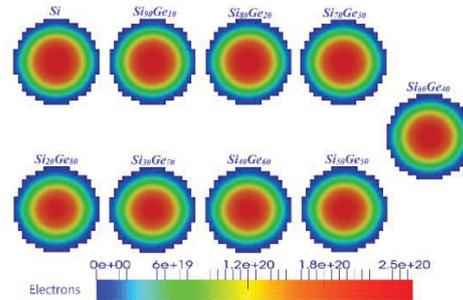


Fig. 6 2D charge distributions, in the middle of the channel, obtained for the Si_xGe_{1-x} NWTs with different Si/Ge concentration.

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Scanning Microwave Microscopy for Non-Destructive Characterization of SOI Wafers

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1. Introduction

State of the art ultra-thin Silicon-On-Insulator (SOI) substrates require novel experimental techniques able to provide high sensitivity, non-destructive characterization, for evaluation of interfaces quality but also of other parameters such as local thickness variation. This can be achieved by the implementation of non-contact optical methods, as recently demonstrated [1]. Beyond the optical wavelengths, microwaves can also offer a useful tool to that end.

Scanning Microwave Microscopy (SMM) is a technique that provides high sensitivity non-destructive, subsurface, point-wise characterization with nanometer scale lateral resolution [2]. For this a microwave signal is applied on a modified AFM tip that is placed in contact or in proximity to the device under test (DUT). The response of tip/DUT system is determined in this case by the local properties of the DUT but also by the properties beyond the top surface, as microwaves may penetrate inside the material under investigation. The technique is completely non-destructive for the DUT both for contact and near field operation.

The application of the proper de-embedding methodology on these measured signals allows the extraction of localized quantitative knowledge on the properties of the DUT [3,4]. This has been extensively demonstrated over the last years for doped layers in silicon [3-6] and on other materials as well as on applications beyond microelectronics, e.g. biological samples.

This paper presents the first experimental application of SMM for the characterization of SOI substrates and it mainly aims to highlight SMM potential as a characterization tool for state of art SOI technology.

2. Experimental Results and Discussion

The study is performed on two SOI structures with 88 nm thick Si film on top of 145 nm thick BOX, one with native oxide and one with passivation oxide on top. Thus the two samples have different density of states at the top Si/SiO₂ interface [7].

For SMM measurements the DUT is connected on the experimental setup as properly terminated shunt capacitor (Fig.1). Then a frequency in the range of 1 – 20 GHz is chosen (19.05 GHz in our case – Fig.2) for the microwave measurements to be performed and the DUT is scanned. For that frequency, microwaves may penetrate for tens of micrometers even in doped silicon layers and therefore

may provide characterization of the entire SOI structure.

The metallic AFM/SMM tip with the Si film and the oxide on top, form a MOS capacitor. This local capacitance determines the reflection of the microwave signal recorded. Among others this is affected by the band bending at the Si/SiO₂ interface; thus by the local density of states. Additionally, interface states have been reported to introduce losses to microwave propagation [8], thus their presence will also affect the measured signals.

In our case the two samples have been placed next to each other (Fig.3) and have been characterized during the same experiment (using the same tip and frequency), to obtain a reliable comparative study by minimizing the experimental variations. The typical signals recorded on the sample (Fig. 4), during an SMM experiment are the topography and the microwave reflection coefficient amplitude, S_{11} and phase, P_{11} (will be shown in the full paper) including also differential measurements, dS_{11}/dV (Fig.5) and dP_{11}/dV (Fig.6). The latter are particular useful to provide high sensitivity subsurface imaging.

The obtained results clearly demonstrate the subsurface differences between the two SOI samples. It is worth noting that the same level of signal is obtained on the BOX, in contrast to the levels of signals coming from the SOI part. The position of the Si film step is clearly identified. The microwave signals acquired on the SOI part of passivated samples (Fig.5,6(a)), are more uniform with respect to the non-passivated ones (Fig.5,6(b)). It should be also noticed that these measurements are local, with respect to other characterization techniques and allows detailed mapping of the DUT properties.

Although additional effort is required for a full calibration study in order to obtain for quantitative nanoscale characterization by SMM, this paper presents the first experimental evidence and should be considered as a promising starting point.

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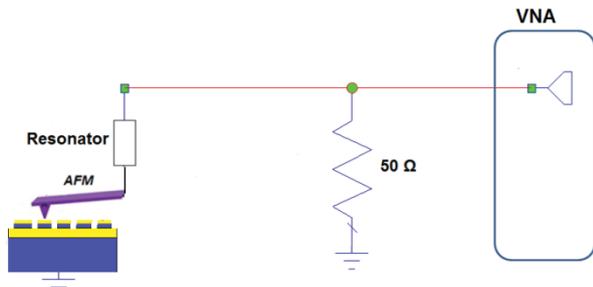


Fig.1: Simplified schematic of the experimental setup

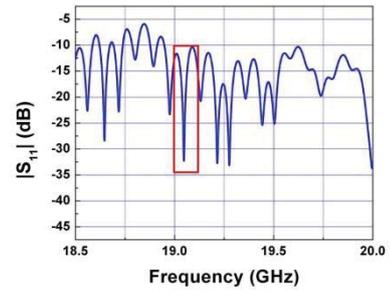


Fig.2: Frequency sweep – selected notch



Fig. 3: Photo of the devices placed on the SMM dark box

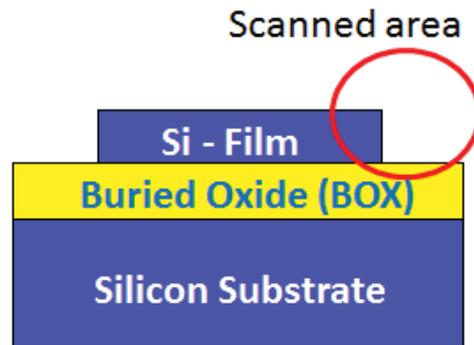
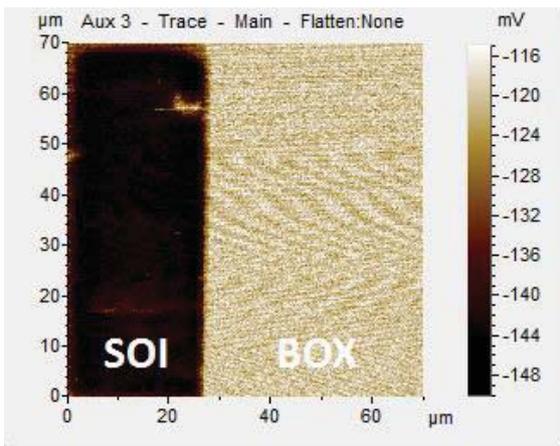
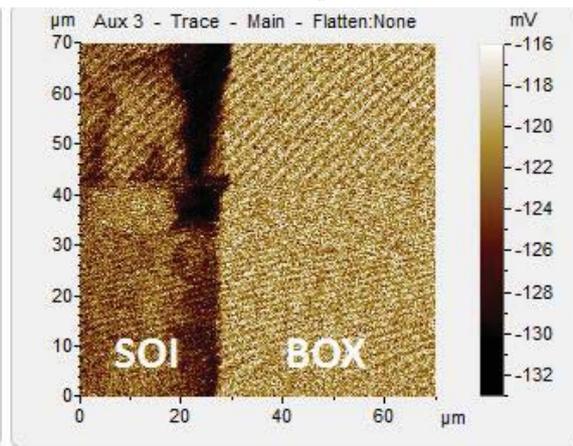


Fig. 4: Schematic of the DUT where the scanned area is depicted.

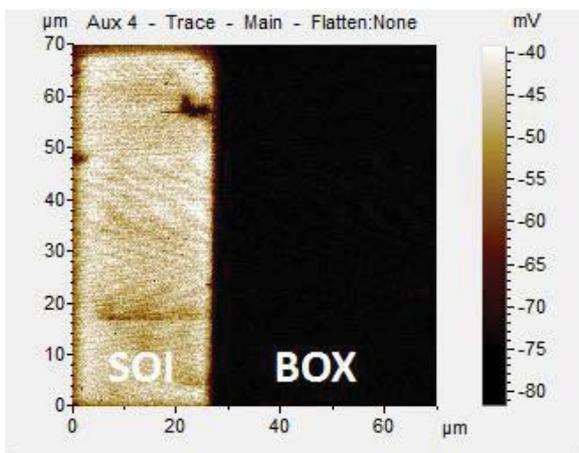


(a)

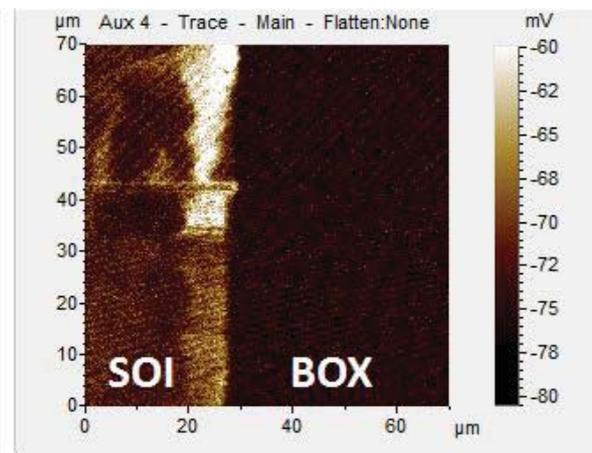


(b)

Fig. 5: dS_{11}/dV measurements on (a) passivated and (b) not passivated samples. A clear attenuation of the signal acquired on the SOI part is observed in (b).



(a)



(b)

Fig. 6: dP_{11}/dV measurements on (a) passivated and (b) not passivated samples. A clear attenuation of the signal acquired on the SOI part is observed in (b).

Influence of the Ge Amount at the Source on Transistor Efficiency of Vertical Gate All Around TFETs for Different Conduction Regimes

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In this work, the influence of the Ge amount at the source on transistor efficiency and intrinsic voltage gain of vertical gate all around TFETs is experimentally evaluated, comparing three different source compositions. The reference transistor has a source of 100% of Si, and the studied devices have 27% and 100% of Ge at the source. The increase of the Ge amount at the source enhances the tunneling current, without degrading the off state current, improves the subthreshold region characteristics and reduces the onset voltage. At the same current level, devices with a higher percentage of Ge present a higher Early voltage and improved efficiency, resulting in an increase of the intrinsic voltage gain. Comparing at the same gate bias, Ge source devices are also better due to their higher drain current value. At weak conduction regime, all devices show better analog characteristics due to their higher efficiency values. Considering the better performance of Ge source devices, two different HfO₂ thicknesses were also analyzed (3 nm and 2 nm). The device with thinner HfO₂ layer presents better transistor efficiency at both conduction regimes due to its better electrostatic coupling. However, when using high gate voltages, this device exhibit a strong degradation of the intrinsic voltage gain.

Introduction

Tunnel field effect transistors (TFETs) are new devices developed to overcome the conventional MOSFETs switching capability. The main conduction mechanism of TFETs is the band-to-band tunneling (BTBT) [1], which allows these devices to reach values of the subthreshold swing (SS) lower than the conventional MOSFET theoretical limit (60 mV/dec) [2–4].

However, using only silicon, TFET devices present low on-state current (I_{ON}) values. Focusing on the improvement of I_{ON} , alternative source compositions have been studied, aiming at the reduction of the material bandgap, decreasing the tunneling path and consequently improving BTBT [5–8].

Although TFETs were developed to improve the switching performance, the analog characteristics of TFETs have been recently studied and have shown promising results [9–13].

In this work, the impact of the conduction mechanism on the transistor efficiency and on the intrinsic voltage gain is evaluated for vertical gate all around TFET devices, with a Si, Si_{0.73}Ge_{0.27} and Ge source. The studied parameters were analyzed for two conditions: weak and strong conduction.

Device Characteristics

The analyzed devices are N-type vertical gate all around TFETs fabricated in imec/Belgium. These devices were measured using an Agilent B1500 Semiconductor Characterization System at the University of São Paulo.

These devices use a top down vertical process flow [14]. The devices have a physical gate length (L_G) of 150 nm, a total channel length (L_{CH}) of 220 nm, a gate/drain underlap (L_{GD}) of 100 nm, a gate/source overlap (L_{GS}) of 30 nm and a diameter of 140nm. Three different source compositions were studied, one of Si_{0.73}Ge_{0.27}, one of pure Ge and the other of pure Si. The gate stack is composed by a dielectric of 3nm HfO₂ on top of 1nm interfacial SiO₂ and covered by a TiN and amorphous silicon layer. For the Ge source device, also devices with 2nm of HfO₂ were analyzed. The drain region is doped with 2×10^{19} As/cm³, the source is doped with 1×10^{20} B/cm³ and the channel is doped with 1×10^{16} As/cm³. More details regarding these structures can be found in [7].

Experimental Results and Discussion

The experimental drain current (I_{DS}) as a function of the gate voltage (V_{GS}) for Si, Si_{0.73}Ge_{0.27} and Ge source TFETs is presented in figure 1.

From this figure it is possible to observe that the Ge device has the highest I_{ON} , due to its smaller bandgap (0.66 eV). The reduction of the bandgap decreases the tunneling path and increases the overlap between bands at the source/channel junction, resulting in a higher BTBT current. This reduction of the bandgap also causes a decrease of the BTBT onset voltage, as can be observed for the Ge devices.

Since the Ge source devices present a higher I_{ON} current, while their I_{OFF} is only slightly higher than compared to the Si device, this results in an improved I_{ON}/I_{OFF} ratio for the Ge source devices.

The transistor efficiency (gm/I_{DS}) is a very important figure of merit for analog application. From gm/I_{DS} as a function of normalized I_{DS} (figure 2), it is possible to study the efficiency behavior from weak to strong conduction regime. From figure 2, it is noticeable that when the amount of Ge in the source increases, the device efficiency also increases for all I_{DS} ranges due to the higher BTBT dominance that results in a better subthreshold swing (weak regime) and higher gm (strong regime).

Figure 3 shows the extracted values of gm/I_{DS} for a fixed current at weak conduction, at strong conduction and also with the same gate bias of 1.9V, for all the different sources devices. In weak conduction, as the reduction of the bandgap increases the I_{ON}/I_{OFF} ratio, it improves the subthreshold region behavior, resulting in an improvement of the gm/I_{DS} due to its dependence on the subthreshold swing. In strong conduction, as the comparison is made using the same I_{DS} , and the transconductance is higher for a higher percentage of Ge, the gm/I_{DS} is also higher for the Ge source devices.

When comparing at a fixed bias of $V_{GS}=1.9$ V, an opposite behavior can be noticed: the increase of the Ge percentage at the source degrades the gm/I_{DS} . This behavior can be explained by the high I_{DS} values for Ge source devices, which becomes more pronounced than the gm improvement.

Figure 4 presents the Early voltage (V_{EA}) for the different sources compositions. Focusing on the comparison that considers the same drain current level, in weak and strong conduction, the Ge source devices are less dominated by the BTBT mechanism [15], being less influenced by the drain voltage (V_{DS}), improving V_{EA} .

When the gate is biased at 1.9V, there is a competition between two factors: the conduction mechanism and the current level. As the BTBT onset voltage is lower for higher percentages of Ge at the source [10, 16], the Ge source devices have more BTBT influence, increasing the influence of V_{DS} , which tends to degrade V_{EA} . However, the increase of the current level in Ge source devices, caused by the bandgap reduction, tends to increase V_{EA} . Since the latter is more pronounced than the former, it results in a considerable improvement of the V_{EA} .

The intrinsic voltage gain analysis (Fig. 5) was also performed comparing the same V_{GS} (1.9 V), and the same current level in weak and strong conduction. Among all the comparisons, the best results were obtained for the weak conduction. Although the trap assisted tunneling (TAT) has a strong influence in this regime and the obtained Early voltage is smaller than the one obtained for strong conduction, in weak conduction the gm/I_{DS} values become the predominant factor on the intrinsic voltage gain.

However, independent of the proposed comparison, the Ge source TFET always presents a better A_V behavior. In weak conduction due to a better subthreshold swing (better gm/I_{DS}), in strong inversion due to the better gm (better gm/I_{DS}) and for $V_{GS}=1.9$ V due to the higher V_{EA} .

As the Ge source device showed to be the best among the analyzed

devices, the comparison between the Ge source devices with 3 nm of HfO₂ and 2 nm of HfO₂ in the gate stack was also performed. Figure 6 presents the I_{DS} as a function of the V_{GS} for these devices. In this figure it is possible to observe that the 2 nm HfO₂ device in spite of more I_{OFF} due to the increase of the gate current, has a better electrostatic coupling, resulting in an improved subthreshold swing and I_{ON}. This improvement can also be observed in the gm/I_{DS} as a function of the normalized I_{DS} (Figure 7), where the 2 nm HfO₂ device curve has higher values of gm/I_{DS} for all I_{DS} values, even when comparing at the same external bias (V_{GS}=1.9V).

Table 1 presents the values of V_{EA} and A_V for both devices. The 2 nm HfO₂ devices have higher V_{EA} values for both weak and strong conduction regimes, due to its higher electric coupling. However, for V_{GS}=1.9 V, the 2 nm HfO₂ devices exhibit a degradation of V_{EA}, caused by the strong influence of the BTBT mechanism.

Table 1 – Values of V_{EA} and A_V for the Ge source devices.

T _{HfO2}	V _{EA} (V)			A _V (dB)		
	Weak	Strong	V _{GS} =1.9V	Weak	Strong	V _{GS} =1.9V
3 nm	161	209	375	67.1	66.3	60.8
2 nm	388	504	116	76.4	75.6	52.7

Considering the A_V, in the weak and strong conduction regimes 2 nm HfO₂ corresponds with a higher A_V because it has an improvement in the gm/I_{DS} and in the V_{EA}, however, at V_{GS}=1.9 V it is degraded due to its V_{EA} and gm/I_{DS} degradation.

Conclusions

In this work a comparative study of the Ge amount at the source of gate all around TFET devices was performed, for three different conditions: fixed current at weak and strong conduction regimes and also for the same gate voltage (1.9 V). The increase of the Ge amount at the source reduces the bandgap, and consequently the tunneling path, that in turns increases the overlap between bands at the source/channel junction and the BTBT current of TFETs.

For all comparisons, the devices with a higher amount of Ge presented better analog characteristics than the others. Considering the conduction regime, although the Early voltage is smaller in weak conduction, the improvement of gm/I_{DS} led to the best A_V characteristics for all analyzed devices. Therefore it can be concluded that the Ge device in weak conduction regime is the most recommended device for analog applications, among all the studied devices.

The Ge device with the gate stack formed with 2 nm of HfO₂ proved itself to have even better analog characteristics than the 3 nm

HfO₂ one, due to its better electrostatic coupling, being even better when it is working in the weak conduction regime.

Acknowledgment

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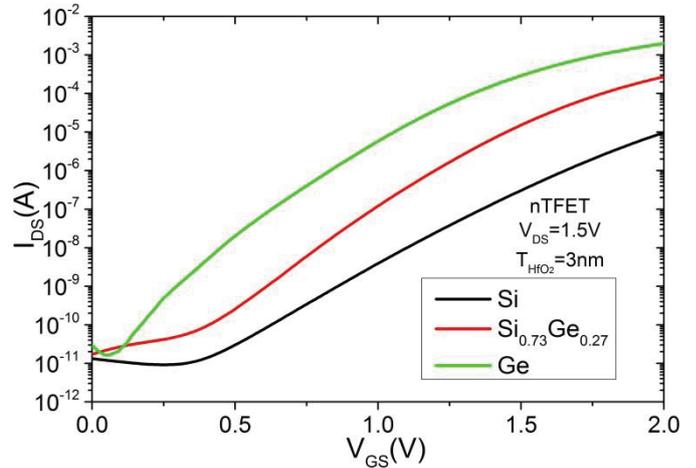


Fig. 1 – Experimental I_{DS} vs V_{GS} for TFETs with different source composition.

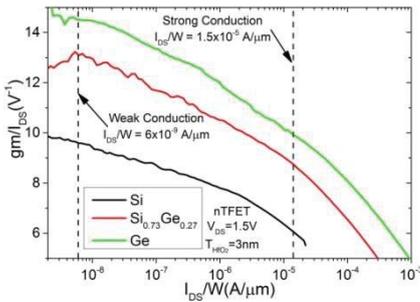


Fig. 2 – Experimental gm/I_{DS} vs I_{DS}/W for TFETs with different source compositions.

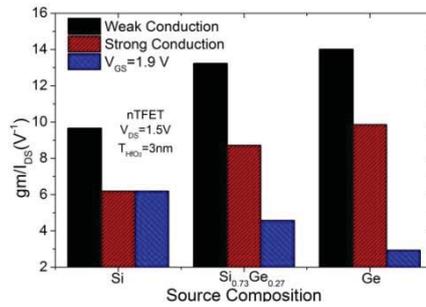


Fig. 3 – Values of gm/I_{DS} for different conduction regimes and source compositions.

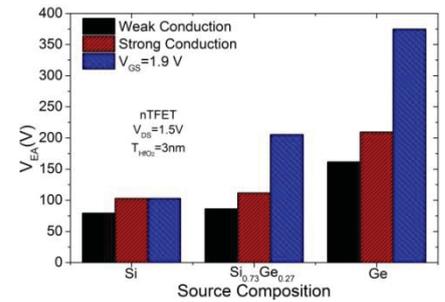


Fig. 4 – Values of V_{EA} for different conduction regimes and source compositions.

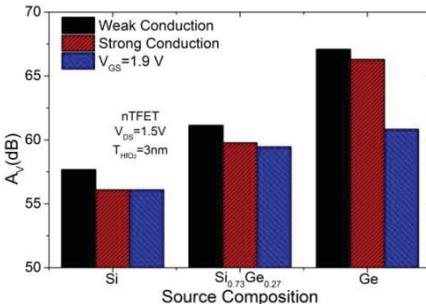


Fig. 5 – Values of A_V for different conduction regimes and source compositions.

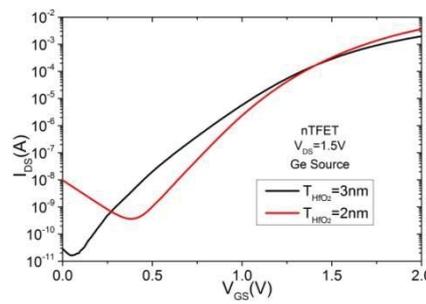


Fig. 6 – Experimental I_{DS} vs V_{GS} for Ge source TFETs with different HfO₂ thickness.

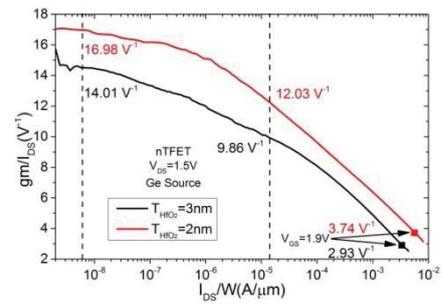


Fig. 7 – Experimental gm/I_{DS} vs I_{DS}/W for Ge source TFETs with different HfO₂ thickness.

Analysis of TFET and FinFET Differential Pairs with Active Load from 300K to 450K

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Abstract – The aim of this work is to compare differential pairs designed with TFETs or FinFETs and evaluate the impact of the working principle of each technology on differential (A_d) and common-mode (A_{cm}) voltage gains and on the susceptibility to the temperature. Circuits with TFETs present higher peak values of A_d and common mode rejection rate (CMRR), but this performance is observed for a narrow input voltage range. When the temperatures raises, differential pair with TFET keeps its parameters almost unchanged, while FinFETs are clearly degraded, revealing a promising application of Tunnel-FET devices.

1. Introduction

The continuous scale-down faced by MOSFET devices in the past few decades turned leakage currents and short-channel effects into major concerns. Considering that the supply voltage has not been reduced at the same proportion, it is clear that power dissipation becomes also a major roadblock [1, 2].

In order to overcome the subthreshold swing limit of 60 mV/decade at room temperature, Tunnel Field Effect Transistors (TFETs) have been considered a promising alternative [3]. These devices are based on a gated p-i-n diode structure, in a way that band-to-band tunneling (BTBT) replaces drift-diffusion, reducing short-channel effects and subthreshold swing [4, 5].

This work studies the suitability of TFET technology in a basic circuit, namely a differential pair with active load. The results have been compared to FinFETs at room and high temperatures using numerical simulations.

2. Device Characteristics

The devices used in this work represent the cross-section of a FinFET structure. The channel length and the distance between their 2 gate oxide interfaces are kept constant along the study, with values of 60 and 40nm respectively. The gate is self-aligned to both channel/drain and channel/source junctions.

Numerical simulations have been performed with low doped channel ($5 \times 10^{15} \text{ cm}^{-3}$) and 10^{20} cm^{-3} doped drain and source. TFET and FinFET devices are simulated with the same structure, but changing the source type. Figure 1 illustrates the case of pTFET and pFinFET.

The gate stack is composed of a midgap material with workfunction of 4.7eV and a gate oxide with thickness of 2nm.

3. Methodology

The circuit of the differential pair with active load is schematically represented in Figure 2. The power supply (V_{DD}) is 1.7V and V_{SS} is -1.7V. Input voltages v_{in1} and v_{in2} refer to the gate of Q_1 and Q_2 transistors respectively and the output voltages v_{out1} and v_{out2} are their drains in the same order. The transistors currents I_{d1} and I_{d2} and the total I current are represented in Figure 2 as well. The circuit has been simulated with Atlas Mixed Mode.

The comparison has been performed based on parameters such as the differential voltage gain (A_d), the common-mode voltage gain (A_{cm}) and the common-mode rejection ratio (CMRR). The differential voltage gain is obtained when the differential input voltage (v_{id}) is defined as the difference $v_{in1} - v_{in2}$. The common-mode voltage gain is extracted when $v_{in1} = v_{in2} = v_{icm}$. Therefore, A_d , A_{cm} and CMRR are calculated according to equations below.

$$A_d = \frac{|v_{out2}|}{|v_{id}|} \quad A_{cm} = \frac{|v_{out2}|}{|v_{icm}|} \quad CMRR = \frac{|A_d|}{|A_{cm}|}$$

After the comparison of circuits with TFETs and FinFETs at room temperature, the same parameters are obtained for temperatures ranging from 300 to 450K.

4. Results and Analysis

The first part of this work focused on the comparison of TFET and FinFET differential pair at room temperature. Figures 3, 4 and 5 refer to the condition as a function of differential input (v_{id}). Figure 3 reveals two main differences between these circuits, namely the output voltage for zero input and the non-linear curve of v_{out2} . For FinFETs, the mobility difference between carriers should be compensated by the bias condition for pFinFETs in the active load and nFinFETs in the differential pair. Therefore, the output voltage for $v_{id} = 0V$ is -0.55V for FinFETs and nearly zero for TFETs, since its current is basically due to BTBT, which occurs quite close to the channel/source junction and depends mainly on its bandgap. Regarding the shape of v_{out2} for TFET, it is important to notice the very high slope for low input voltages and the clear saturation for $|v_{id}| > 0.2$. The susceptibility to the input voltage leads to a higher values of differential gain, which may be justified by considering that this parameter is directly proportional to the transistor transconductance (g_m) and output resistance (r_o). As previously observed in [6], even with higher g_m values for FinFETs, TFETs advantage in terms of r_o prevails.

Figure 4 illustrates this behavior in terms of drain current variation. At the same time, it shows the influence of the circuit asymmetry, due to the short circuit between Q_3 gate and drain, which keeps Q_3 in the saturation region for a wider range of input voltage than Q_4 . Figure 5 reveals the consequent differential gains for the circuits with TFETs and FinFETs. The results are normalized for a unitary gain for FinFETs at $v_{id} = 0V$, so that it is clear that the peak value obtained for TFETs is more than 50 times higher. A similar behavior had been observed for differential pairs with passive load in [7], including highest A_d and stricter linear regions for TFETs. On the other hand, without the mentioned Q_3 short circuit, I_d/I curves used to be symmetric to v_{id} .

Figure 6 exhibits the common-mode gain as a function of $v_{icm} = v_{in1} = v_{in2}$, following the same previously explained normalization criteria. In this case, the output voltages was closely linear for both circuits and the slope was relatively similar to each other. This way, there is no clear peak in any curve and the relative difference is much smaller than the one observed in Figure 5. A direct consequence may be noticed in the CMRR, which is related to the differential and common-mode gains ratio. Based on this parameter, the performance of differential pair with TFETs is more suitable than with FinFETs, since the former presented up to 22 times bigger CMRR than the latter.

In the second part of this work, these circuits have been analyzed in terms of susceptibility to the temperature. Once more, A_d , A_{cm} and CMRR have been selected as relevant parameters and their relative variation for temperatures up to 450K have been plotted in Figure 7, 8 and 9 respectively.

Regarding the differential gain, values for FinFET clearly decreased by more than 50%, which may be explained by the mobility degradation for higher temperatures. Meanwhile, TFET was nearly constant, since the bandgap narrowing is closely compensated by the output conductance (g_D) increase. In terms of common-mode gain, TFET presents a slight increase, while FinFET reduction is relevant, but not as much as the one observed for A_d . As a consequence, CMRR for FinFETs reduces more than 20% and for TFETs decreases around 3%. Remembering that at room temperature the circuit with TFETs had already presented better CMRR values for low input voltages, it should be highlighted that this difference gets even more relevant as the temperatures goes up to 450K.

5. Conclusions

This paper analyzed the suitability of differential pairs with active load designed with TFET or FinFET devices. A quantitative comparison has been performed based on the differential gain, the common-mode gain and the common-mode rejection ratio.

In the differential condition, TFETs presented a high susceptibility to the input voltage, leading to a more than 50 times higher value of A_d . On the other hand, there was a

saturation for $|v_{id}| > 0.2V$, while FinFETs presented a linear behavior for the whole input range. The common-mode gain difference was much less significant, in a way that the CMRR was more than 20 times bigger for the circuit with TFETs.

For higher temperatures, differential pairs with FinFETs have been clearly affected by the mobility degradation, leading to a decrease in the 3 studied parameters. TFETs presented a less susceptible behavior, due to the compensation of bandgap narrowing and g_D increment. CMRR decreased 21% for FinFETs, while there was a slight increase for TFETs.

To conclude, it was observed that the differential pair with TFETs presented better global results for low input voltages, but had a stricter range to work in the linear region.

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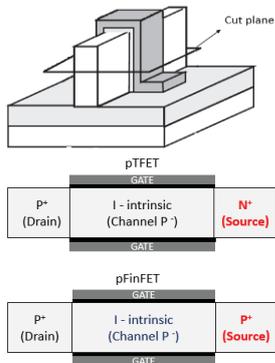


Fig. 1 – P-type TFET and FinFET structure and the respective cut plane.

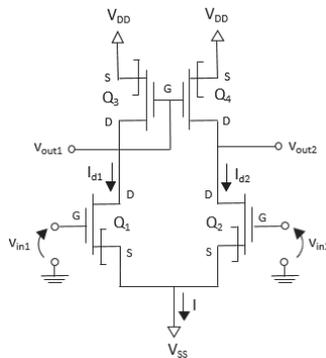


Fig. 2 – Basic TFET circuit of a differential pair with active load.

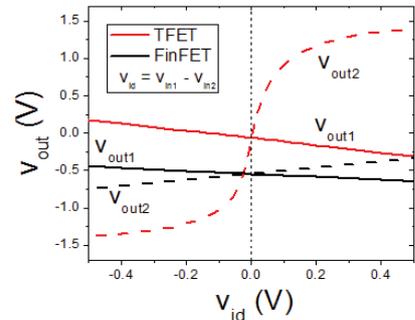


Fig. 3 – Output voltages as a function of the differential input voltage.

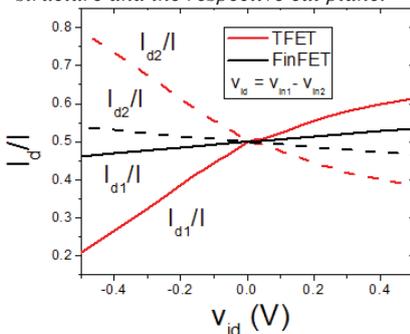


Fig. 4 – I_{d1}/I and I_{d2}/I ratios as a function of the differential input voltage.

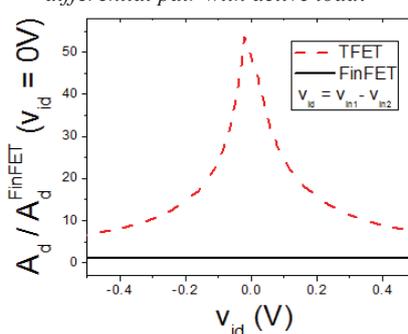


Fig. 5 – Differential gain as a function of the differential input voltage

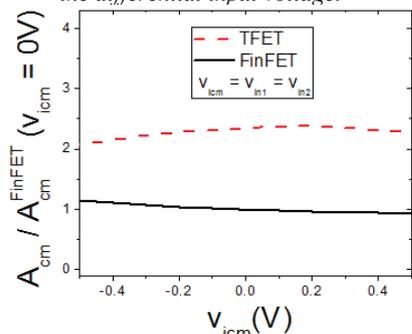


Fig. 6 – Common-mode gain as a function of the input voltage

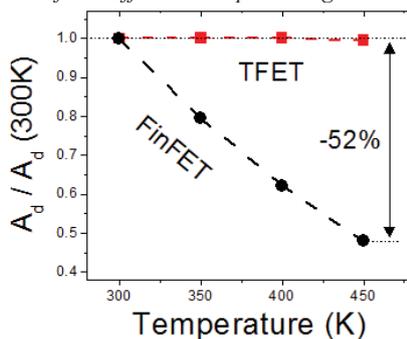


Fig. 7 – Differential gain for temperatures from 300 to 450K

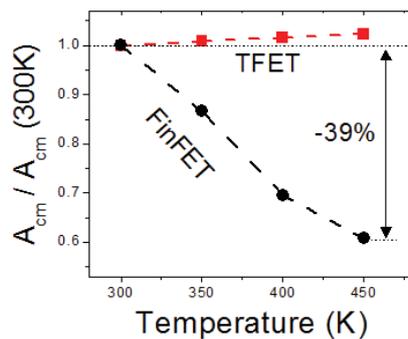


Fig. 8 – Common-mode gain for temperatures from 300 to 450K

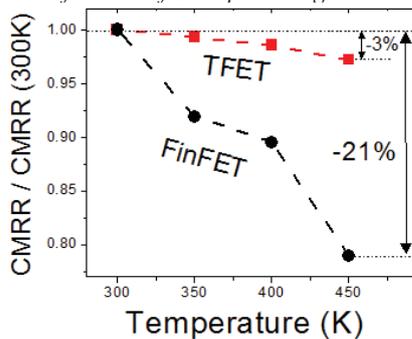


Fig. 9 – Common-mode rejection ratio for temperatures from 300 to 450K

Numerical Simulation of Gunn Oscillation in AlGaAs/InGaAs High-Electron Mobility Transistor

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1. Introduction

Since the electromagnetic wave in the terahertz (THz) frequency range has potential applications in various areas, the THz emitting devices have gained great interest. Among various possible THz emitting devices, a transistor-type THz emitting device can reduce the form factor significantly, since it does not require the external laser source.

Recently, the plasma instability in the high-electron mobility transistor (HEMT) [1] has been simulated by the current authors. [2] With a set of device parameters, it is predicted that the plasma instability in the HEMT results in an oscillation well above 1 THz. Another possible mechanism to generate a high-frequency oscillation is the Gunn oscillation. It is expected that the oscillation frequency is in the sub-THz range, which is considerably lower than that due to the plasma instability.

In this work, the simulation results for the Gunn oscillation in an AlGaAs/InGaAs HEMT are presented. The simulated device structure and the simulation methodology are introduced in Section 2. The simulation results are shown in Section 3. Finally, the conclusion is made in Section 4.

2. Device structure and simulation methodology

The $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}/\text{In}_{0.25}\text{Ga}_{0.75}\text{As}$ HEMT structure is shown in Fig. 1. The thickness of the InGaAs channel layer is 10 nm. A delta-doping layer whose sheet density is 10^{11} cm^{-2} is introduced to the AlGaAs barrier. The channel length is 150 nm and the length of each recessed region is 500 nm. The total channel width is 120 μm . A 0.8 μm -thick buffer layer is modeled as a perfect insulator for simplicity.

A commercial device simulator [3] has been employed to solve the drift-diffusion equations. The mobility model with the negative differential mobility (NDM) effect [4] is considered for the electron mobility in the channel layer. The electric field parallel to the electron current is used as the driving force of the mobility model. The electron-hole pair generation due to the impact ionization and quantum confinement effect are neglected in this work.

In order to simulate the autonomous on-set of the oscillation, a transient simulation has been performed. The supply voltage, which is connected to the drain terminal through a resistor of 1 Ω , is rapidly ramped up to the given target value. Once after the target value is achieved, the supply voltage is kept for a sufficiently long time to yield a stabilized oscillatory waveform. Such a numerical experiment is repeated for various bias points. The oscillation frequency and amplitude are

measured. In order to prevent unwanted damping by the numerical dissipation, the maximum allowed time step is limited to 0.1 psec.

3. Simulation results

Fig. 2 shows the dc drain current and trans-conductance as a function of the gate voltage. The drain-to-source bias voltage is 1.0 V. The NDR effect in the velocity saturation model yields large difference in the trans-conductance. It is noted that convergence problems have been observed with the NDM model for higher gate voltages.

A typical transient behavior of the drain terminal current is shown in Fig. 3. The ramping speed of the supply voltage is 10 V nsec^{-1} . During the ramping period, the oscillation of the drain current starts. Even after the ramping period is finished at 60 psec in this example, a stabilized oscillation can be clearly observed.

The electron density shown in Fig. 4 clearly shows that the oscillation takes place in the recessed region between the gate and drain terminals.

In Fig. 5, the oscillation frequency is shown as a function of the supply voltage. The oscillation is observed only for a narrow range of the gate voltage. In this example, it is observed in the gate voltages between 0.04 V and 0.08 V. In Fig 2, unusual behavior of the trans-conductance due to the NDR effect is observed in this voltage range. The oscillation frequency shows a considerable dependence on the drain voltage. Note that the oscillation frequency is determined by the HEMT itself, because no external resonator is connected to the HEMT.

The peak-to-peak amplitude of the drain current fluctuation is shown in Fig. 6. With the resistor of 1 Ω , the peak-to-peak amplitude exhibits its maximum value of 1.44 mA at the gate voltage of 0.08 V. In this case, the amplitude is insensitive to the supply voltage, at least up to 1.0 V.

4. Conclusion

The Gunn oscillation in the AlGaAs/InGaAs HEMT has been simulated. It has been shown that the Gunn oscillation can be observed for a certain range of bias points. The electron density clearly shows that the recessed region between the gate and drain terminals plays an important role in the Gunn oscillation. The oscillation frequency and amplitude are shown as functions of the bias voltages.

This work is supported by the Samsung Research Funding Center of Samsung Electronics under Grant SRFC-IT1401-08.

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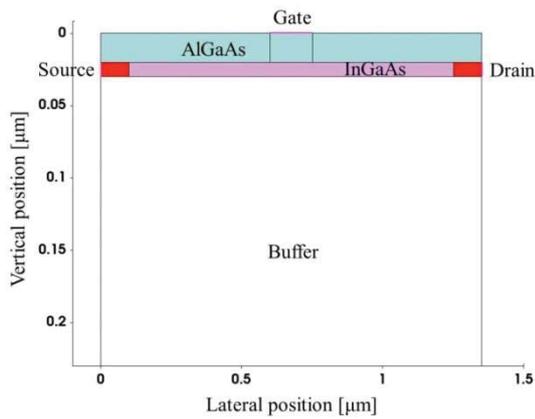


Fig.1: Schematic of the simulated AlGaAs/InGaAs HEMT structure. The channel length is 150 nm and the length of each recessed region is 500 nm. The thickness of the buffer layer is 0.8 μm .

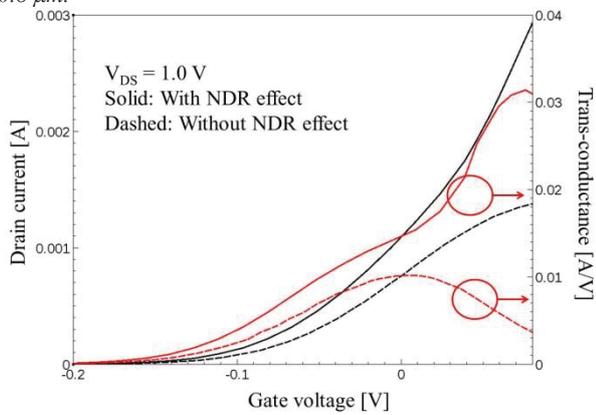


Fig.2: Simulated dc I_d - V_g relation at the drain-to-source bias voltage of 1.0 V. The trans-conductance is also shown. Solid lines are obtained with a mobility model considering the NDR effect. For dashed lines, the NDR effect is neglected in the velocity saturation model.

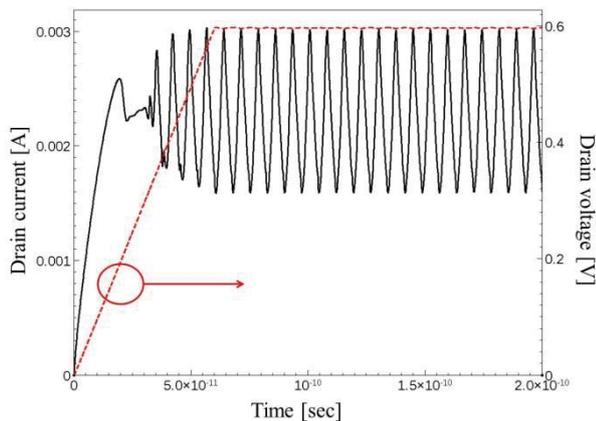


Fig.3: Transient behavior of the drain terminal current. The gate voltage is 0.06 V and the supply voltage connected to the drain terminal is ramped up to 0.6 V with a ramping rate of 10 V nsec^{-1} .

- [3] Sentaurus Device User Guide, Synopsys Inc. (2014).
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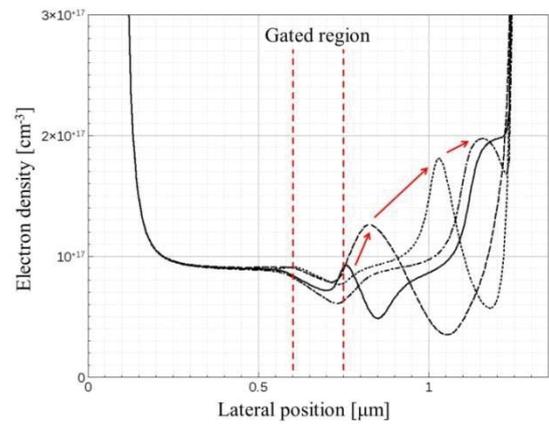


Fig.4: Snap shot of the electron density at the AlGaAs/InGaAs interface at various time points with a 2 psec step. The values at the middle of the channel layer are taken. The gate voltage is 0.06 V and the supply voltage in the drain side is 0.6 V.

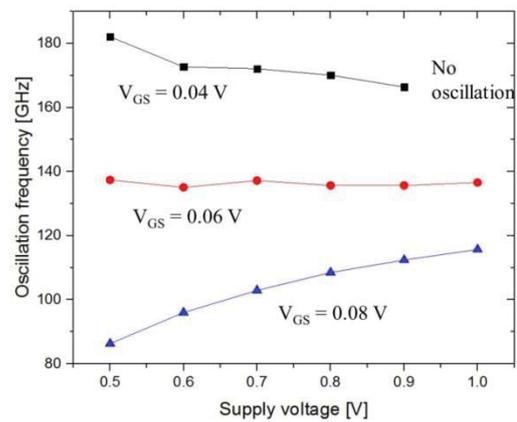


Fig.5: Oscillation frequency as a function of the supply voltage. Three cases of the gate voltage (0.04 V, 0.06 V, and 0.08 V) are considered. For other gate voltages outside this range (such as 0.0 V or 0.1 V), no oscillation is observed.

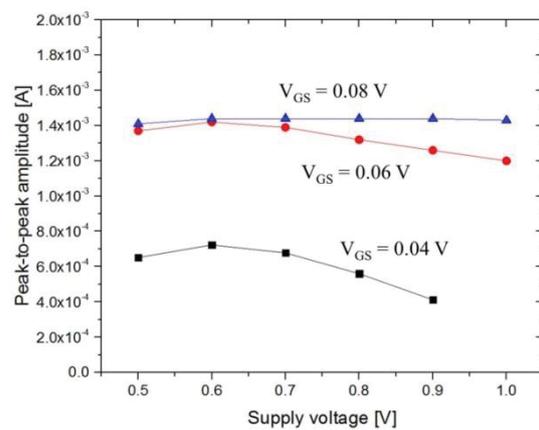


Fig.6: Peak-to-peak amplitude as a function of the supply voltage.

Metal-Graphene Contact Capacitance

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1. Introduction

Properties of the metal-graphene contact are crucial for efficient electrical operation of graphene devices. In spite of extensive research in this field the metal-graphene capacitance and its dependence on the measurement frequency have not been studied up to now. Thus, in this work a theoretical analysis of the Metal-graphene capacitance is carried out, and the experimental study of the frequency dependence of the capacity of Ni-graphene contact fabricated on SiO₂/Si structure is performed.

2. Theory

Schematic view of the contact is shown in Fig.1. The contact capacitance can be determined from the following expression [1]:

$$C = -\frac{e}{V_1} \int_0^\infty n_1(x) dx,$$

where $n_1(x)$ is the nonequilibrium charge concentration induced in graphene by the alternative voltage $V_1 \sim \exp(i\omega t)$, which was applied between metal contact and graphene layer. The $n_1(x)$ is found from the continuity equation

$$i\omega n_1 = \frac{\sigma}{e} \left(\frac{\pi \hbar^2}{2em_c} \frac{\partial^2 n_1}{\partial x^2} - \frac{\partial^2 \varphi(x, 0)}{\partial x^2} \right),$$

where σ is the graphene conductivity. The graphene conductivity can be presented as of $\sigma = e^2 D_n D$, where D_n is the diffusion coefficient, and $D = 2m_e/\pi \hbar^2$ is the density of states, where $m_e = E_s/v_F^2$ is the cyclotron mass, E_s is the carries energy. The expression for the density of states takes into account that spin (g_s) and valley (g_v) degeneracy in graphene are 2.

The electrostatic potential $\varphi(x, z)$ can be obtained from Laplace equation with the following boundary conditions:

$$\varphi(0, z) = 0; \frac{\partial \varphi(x, 0)}{\partial z} = \frac{2\pi e n_1(x)}{\varepsilon}; \varphi(x \rightarrow \infty, 0) = V_1,$$

where ε is the dielectric constant of the dielectric substrate. The solution of the Laplace equation is

$$\varphi(x, z) = -\frac{4e}{\varepsilon} \int_0^\infty v(\lambda) e^{-\lambda z} \sin(\lambda x) \frac{d\lambda}{\lambda},$$

where $v(\lambda) = \int_0^\infty n_1(x) \sin(\lambda x) dx$ is the Fourier component of $n_1(x)$. Thus, an equation for $n_1(x)$ can be obtained, which can be solved by using of Fourier sine transformation in the following form

$$n_1(x) = -\frac{4eV_1}{\pi^2 \hbar^2 v_F^2} \left(E_s + \frac{eV_1}{2} \right) \int_0^\infty \frac{\lambda \sin(\lambda x) d\lambda}{\lambda^2 + \frac{2}{a} \lambda + \frac{i}{al}}.$$

The metal-graphene contact capacitance per unit length of the contact is

$$C = -\frac{e}{V_1} \int_0^\infty n_1(x) dx = \frac{\varepsilon}{\pi^2} \frac{1 + \frac{eV_1}{2E_s}}{\sqrt{(1 - \frac{ia}{T})}} \ln \left(\frac{1 + \sqrt{(1 - \frac{ia}{T})}}{1 - \sqrt{(1 - \frac{ia}{T})}} \right),$$

where $a = \varepsilon \hbar^2 / 2e^2 m_e$ is the screening length, and $l = \pi \sigma / \omega \varepsilon$ is the relaxation length in graphene. For relatively low frequency, when $a \ll l$, the contact capacitance has the following form

$$C \cong \frac{\varepsilon}{\pi^2} \left(1 + \frac{eV_1}{2E_s} \right) \left[\ln \left(\frac{8\pi e^2 m_e \sigma}{\varepsilon^2 \hbar^2 \omega} \right) - i \frac{\pi}{2} \right]. \quad (1)$$

It should be noted that when the inverse boundary conditions for Laplace equation are applied the coefficient before square bracket reads as $(1 - eV_1/2E_s)$. Therefore a coefficient in the expression (1) for the equivalent measured capacitance is $[1 - (eV_1/2E_s)^2]$. Moreover, the this coefficient depends on the alternative voltage amplitude, that is absent in the case of the contact capacitance between 3D metal and 2D electron gas [1].

3. Experiment and Results

Verification of the theory was performed by using of the Ni-graphene contact. The graphene layer was synthesized by CVD technique on Cu and transferred onto SiO₂/p-Si structure with the thickness of the SiO₂ layer about 300 nm. The quality of the graphene layer was checked by micro-Raman spectroscopy and scanning Kelvin probe technique [2]. The result shows that the graphene contains a single layer and consists of single crystalline blocks with the sizes about 5-10 μm (Fig.2).

The Ni contacts were deposited on the graphene surface by dc magnetron sputtering to fabricate the transmission line (TL) with a same size of the contacts with different distances between them. The transmission lines were surrounded with defect arias formed by electron beam (the dose is more than $4 \times 10^3 \mu\text{C}/\text{cm}^2$, and energy is 3 keV) (see the inset in Fig.3). Resistance of the contacts, that was determined by TL, equals to about 65 Ohm and the graphene resistivity is about 200 Ohm \times sq (Fig.3).

Measurements of graphene impedance vs. measurement frequency were carried out using parallel equivalent circuits at zero bias between the two contacts. The used frequency range was $10^2 - 10^6$ Hz, the amplitude of the input a.c. signal was in the range from 30 mV to 1 V. Agilent 4284A Precision LRC Meter was used for the measurements. Dependence of the capacitance vs. measurement frequency at 30 mV input a.c. signal can be described by the expression $C(\omega) = C_0 - C_S(V_1) \ln(\omega + \omega_0)$ (Fig.4 (a)), and dependence of the capacitance vs. amplitude of a.c. input signal can be written as $C_S(V_1) = A[1 - (eV_1/2E_s)^2]$ (Fig. 4 (b)). Treatment of the area between the contacts by electron beam with the dose of $1 \times 10^2 \mu\text{C}/\text{cm}^2$ (see insert Fig. 5(a)) results in the decrease of the slope of $C = C(\ln(\omega))$ and emergence of “jumps” on the curve of $C = C(V_1)$ (see Fig. 5).

4. Conclusions

Dependence of the Me-graphene contact capacitance on the measurements frequency has been observed. It is suggested that the observed logarithmic dependence of the capacitance on the frequency is associated with 2D properties of the single layer graphene.

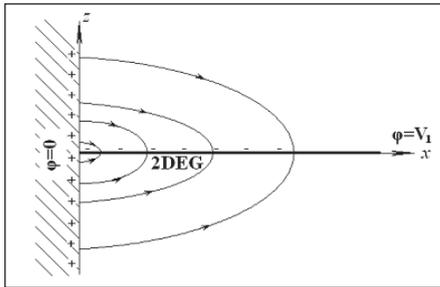


Fig.1: Schematic view of the contact with a 2D graphene layer.

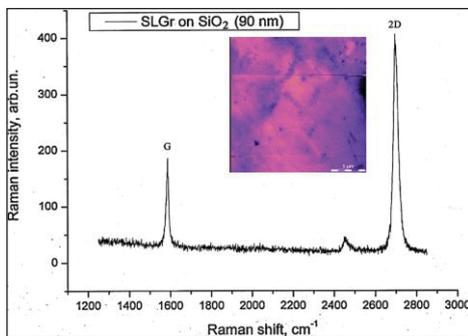


Fig.2: Raman spectra of the graphene film on the SiO₂/Si structure. Inset: Map of the graphene surface potential measured by scanning Kelvin probe force microscopy (SKPFM) technique.

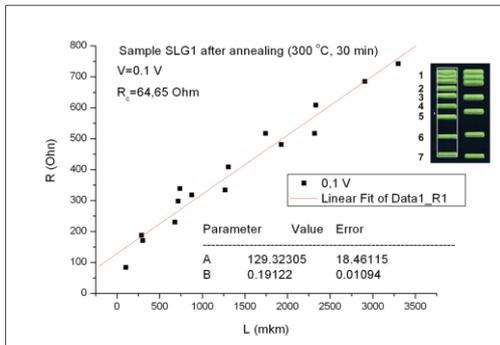
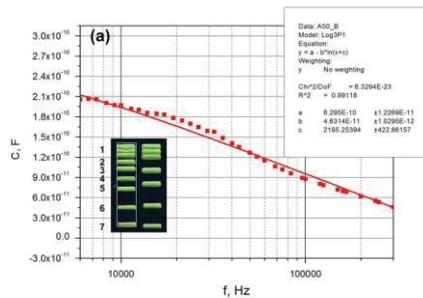


Fig.3: Contact resistances of the Me contact-graphene and surface graphene resistivity obtained from the TL technique measurement.



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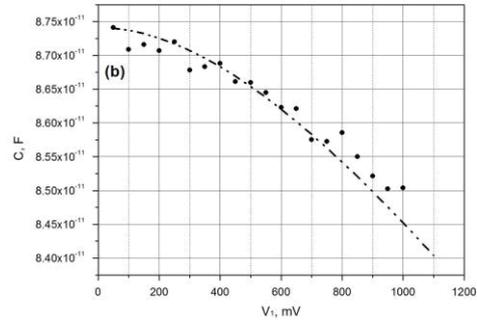


Fig.4: Dependence of the capacitance between the contacts number 3 and 4 vs. measurement frequency (distance between of the contacts is 288 μm , input a.c. signal is 30 mV) (a), and dependence of the capacitance vs. the amplitude of a.c. input signal ($f=100$ kHz) (b).

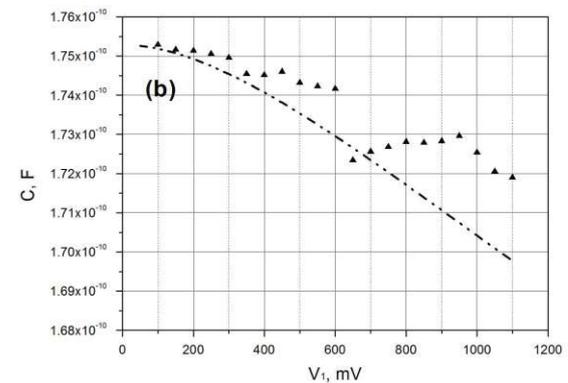
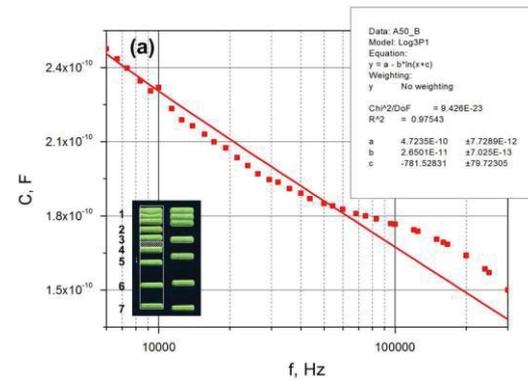


Fig.5: Dependence of the capacitance between the contacts number 3 and 4 vs. measurement frequency after the treatment by electron beam with the dose of $1 \times 10^2 \mu\text{C}/\text{cm}^2$ (a), and dependence of the capacitance vs. amplitude of a.c. input signal ($f=100$ kHz) (b).

Author Index

Adachi, K.	54	Bordallo, C.C.M.	136
Adamu-Lema, F.	132	Boudier, D.	24
Agopian, P.G.D.	10, 60, 112, 136, 138	Bounouar, M.A.	124
Al-Ameri, T.	132	Bourdet, L.	64
Alarcon, E.	82	Brachtendorf, G.	30
Aldegunde, M.	32	Brinciotti, E.	134
Alexander, C.	34	Brown, A.R.	34
Ali, S.Z.	88	Buca, D.	16
Alper, C.	14	Bühler, R.T.	106
Amit, I.	6	Caimi, D.	72, 122
André, N.	88	Calmon, F.	92, 124
Andrieu, F.	50, 98	Campabadal, F.	48
Asenov, A.	34, 132	Carin, E.	24
Athanasiou, S.	86	Cassé, M.	64, 94
Aymerich, X.	48	Chalker, P.R.	18
Baccarani, G.	12	Changala, J.	126
Bae, Y.	28	Cheng, B.	34
Balakrishnan, K.	72	Cho, I.-T.	28
Baldauf, T.	2	Choi, J.	104
Barraud, S.	4, 64, 94	Chowdhury, M.F.	100
Baumgartner, O.	84	Claeys, C.	10, 60, 112, 136
Bawedin, M.	98	Claverie, A.	50
Baylac, E.	50	Collaert, N.	24
Beck, R.B.	108	Crespo-Yepes, A.	48
Ber, K.	108	Cretu, B.	24
Berthelon, R.	50	Cristoloveanu, S. ...	28, 58, 74, 86, 98, 122, 126, 134
Bittner, K.	30		

Crupi, F.....	80	Garidis, K.	114
Czornomaz, L.	58, 72, 122	Georgiev, V.P.	132
Damianos, D.....	126	Gérard, P.....	88
De Franceschi, S.....	71	Ghibaud, G.	52, 78
de Streel, G.....	66	Giacomini, R.	66, 106
Demel, H.	84	Glass, S.....	16
Deshpande, V.....	72, 122	Głuszko, G.....	102
Dimitriadis, C.A.	52	Gnani, E.....	12
Djara, V.....	72, 122	Gnudi, A.	12
Donetti, L.	56	Godkin, A.	6
Drouin, D.....	124	Godoy, A.	56, 130
Dubois, F.	92	Golanski, D.....	74
Dutartre, D.....	50	Gomeniuk, Yu.V.	142
El Dirani, H.	74	Gonzalez, M.B.....	48
El Hajjam, K.G.....	124	Gonzalez-Medina, J.M.	130
Elmessary, M.A.....	32	Graef, M.	38
Esseni, D.....	80	Graziosi, T.....	92
Farokhnejad, A.	38	Grillet, C.....	62
Faynot, O.....	94	Grossi, A.....	46
Feng, X.	22	Haendler, S.....	52
Ferrari, P.....	74	Hain, F.....	38
Filipovic, L.....	68	Hall, S.....	18
Flandre, D.....	66, 88, 90	Haond, M.....	50, 66, 78
Fompeyrine, J.....	72, 122	Hartmann, J.M.....	16
Fonteneau, P.	74	Hashemi, P.....	72
Francis, L.A.....	88	Heinzig, A.	2
Funakubo, H.....	42	Hellström, P.-E.....	114
Galy, Ph.....	86	Henning, A.	6
Gámiz, F.....	14, 26, 41, 56, 130	Hokazono, A.....	54

Hong, S.-M.....	140	Kloes, A.....	38
Horst, F.....	38	Ko, D.-H.....	104
Hosenfeld, F.....	38	Ko, E.....	104
Hosey, G.P.....	118	Kosina, H.....	96
Hössinger, A.....	68, 128	Kurosawa, M.K.....	42
Iannazzo, M.....	82	Lacord, J.....	4
Ikonic, Z.....	16	Langer, R.....	60
Im, K.-S.....	28	Lanuzza, M.....	80
Indalecio, G.....	32	Lee, J.-H.....	28
Iñíguez, I.....	38	Lee, M.....	104
Ionescu, A.M.....	14	Legrand, C.A.....	74, 86
Ionica, I.....	58, 126, 134	Lemme, M.C.....	82
Iwai, H.....	76	Leroux, C.....	78
Jang, J.-H.....	140	Lesieur, P.....	92
Jasiński, J.....	110	Li, G.....	88
Jaud, M.-A.....	4	Li, J.....	64
Jin, J.D.....	18	Lindberg, J.....	32
Josse, E.....	50	Luong, G.V.....	100
Jungemann, C.....	30	Maestro, M.....	48
Kaminski, A.....	126	Majkusiak, B.....	110
Karatsori, T.A.....	52	Malesińska, J.....	102
Karbasian, G.....	20	Manstetten, P.....	68
Karner, M.....	84	Mantl, S.....	16, 100
Kataria, S.....	82	Marcelli, R.....	134
Kazemi Esfeh, B.....	90	Marin, E.G.....	130
Kernstock, C.....	84	Marin-Cudraz, D.....	74
Kienberger, F.....	134	Marquez, C.....	26
Kilchytska, V.....	66, 90	Martinie, S.....	4, 64
Kim, S.-W.....	104	Martin-Martinez, J.....	48

Martino, J.A.....	10, 60, 98, 112, 136, 138	Ohata, A.	26
Martino, M.D.V.....	138	Oliveira, A.V.....	60
Matsuzawa, K.....	54	Olivo, P.....	46
Mazurak, A.....	110	Orlov, A.O.....	20
Medina-Bailon, C.....	56	Ortolland, S.	50
Michalas, L.....	134	Östling, M.....	114
Mikolajick, T.....	2	Padilla, J.L.....	14
Millar, C.....	34	Pala, M.	62
Mitard, J.	60	Palestri, P.....	80
Mitrovic, I.Z.....	18	Pandey, H.	82
Mitterbauer, F.....	84	Pavan, P.....	44
Miyata, T.....	54	Pavanello, M.A.....	94
Mohamad, B.....	78	Paz, B.C.....	94
Moselund, K.....	8	Pelissier, D.	126
Nafria, M.....	48	Pelloux-Prayer, J.....	64
Nagy, D.	32	Pereira, A.S.N.....	66
Nakagawa, S.....	42	Perez, E.....	46
Narimani, K.....	100	Petrosyan, S.....	120
Navarro, C.....	4, 98	Pirro, L.	58, 122, 134
Nawratil, G.....	128	Planes, N.	66
Nazarov, A.N.....	142	Poiroux, T.....	50
Nedjalkov, M.....	34	Poncelet, O.	88
Neophytou, N.....	96	Pourfath, M.....	96
Nersesyan, S.....	120	Prégaldiny, F.	120
Nicolas, R.....	50	Puglisi, F.M.....	44
Niquet, Y.-M.....	64	Radamson, H.....	114
Novo, C.D.	106	Rama, I.	48
O'Connor, E.	72	Raskin, J.-P.....	90
Oh, H.....	104	Reggiani, S.....	12

Reibold, G.	78, 94	Solaro, Y.....	74
Rideau, D.....	64, 78	Sousa, M.....	72
Riel, H.	8	Stanojevic, Z.....	84
Rodriguez, N.	26	Stork, H.	1
Rodriguez, R.....	48	Strangio, S.	80
Rooyackers, R.	10, 112, 136	Sugahara, S.....	42
Rosenwaks, Y.....	6	Sverdlov, V.....	116
Ruiz, F.G.	130	Swaminathan, N.	6
Sadi, T.	34	Takamura, Y.....	42
Sampedro, C.....	56	Tanaka, Ch.	54
Sano, N.....	36	Thean, A.	10, 24, 112, 136
Sant, S.....	8	Theodorou, C.G.....	52
Sasaki, K.R.A.	98	Thesberg, M.....	96
Savoy-Navarro, A.....	92	Tiagulskiy, S.I.	142
Schenk, A.	8	Tienda-Luna, I.M.	130
Schulte-Braucks, C.....	16, 100	Tomaszewski, D.	102
Segev, G.	6	Trellenkamp, S.	100
Selberherr, S.	68, 116, 128	Triozon, F.....	64
Selmi, L.	80	Trommer, J.	2
Seoane, N.	32	Udrea, F.....	88
Shalev, G.	6	Vandooren, A.	10, 112, 136
Shaw, A.	18	Veloso, A.....	24
Shuto, Y.....	42	Vignetti, M.M.....	92
Silveira, M.A.G.	106	Vinet, M.	4, 94
Simoen, E.	10, 24, 60, 112, 136	Visciarelli, M.....	12
Šimonka, V.....	128	Vitrant, G.....	126
Sivieri, V.B.....	112, 136	Vodapally, S.....	28
Slobodyan, A.M.	142	von den Driesch, N.....	16
Snider, G.L.	20	Wang, L.	34

Weber, W.M.....	2	Yamamoto, S.....	42
Weinbub, J.....	68, 128	Yesayan, A.	120
Wenger, Ch.....	46	Yu, D.	22
Witters, L.....	60	Zambelli, C.....	46
Won, Ch.-H.	28	Zeng, Y.....	88
Wong, H.	22	Zhang, J.	22
Wrench, J.S.	18	Zhao, Q.T.	16, 100

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