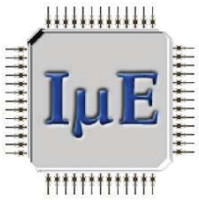
2016 Joint International EUROSOI Workshop
and International Conference
on Ultimate Integration on Silicon

# EURSOI-ULIS 2016


Institute for Microelectronics
TU Wien, Vienna, Austria

January 25- 27, 2016







IEEE catalog number: CFP1649D-USB

ISBN: 978-1-4673-8608-1

ISBN 978-1-4673-8608-1 IEEE Catalog number CFP1649D-USB

**The Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)** is a three days meeting bringing together the experts from Industry and Academia in technology, physics, modeling, simulation, and characterization of advanced nano-scale semiconductor-on-insulator and silicon-compatible devices from Europe and all over the world. For more than ten years the EUROSOI Workshop and the ULIS Conference provided a platform for the European micro- and nanoelectronic community to share the most recent advances, discuss the hottest topics in the field and outline current trends defining the future progress. As the future of microelectronics is believed to be determined by fully depleted SOI and FinFET devices enabling new functionalities, the two sister conferences were merged in 2015 in order to further boost their importance and scientific impact. Encouraged by the great success of the first joint EUROSOI-ULIS event, the second joint EUROSOI-ULIS 2016 Conference is hosted by the Institute for Microelectronics, TU Wien, Austria. The aim of the EUROSOI-ULIS Conference is to provide an open forum for the presentation and discussion of recent advances in the fields of More Moore, More than Moore, and Beyond CMOS applications. The hot topics introduced by outstanding international invited speakers will further be discussed at the sessions with a particular focus on modern SOI technology and advanced nanoscale devices. The Conference Committees and organizers hope you will enjoy the conference and the social program.

Conference Chairs
Viktor Sverdlov, Siegfried Selberherr, Technische Universität Wien, Austria
{sverdlov | selberherr}@tuwien.ac.at

Program Chair
Franciso Gámiz, University of Granada, Spain
fgamiz@ugr.es

Honorary Chair
Sorin Cristoloveanu, IMEP-INP Grenoble MINATEC, France
sorin@minatec.grenoble-inp.fr

ISBN 978-1-4673-8608-1 IEEE Catalog number CFP1649D-USB

# 2016 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon

## Organizing Committee

Viktor Sverdlov (Institute for Microelectronics, TU Wien), Conference co-Chair

Siegfried Selberherr (Institute for Microelectronics, TU Wien), Conference co-Chair

Francisco Gámiz (University of Granada), Technical Program Chair

Sorin Cristoloveanu (IMEP Minatec, Grenoble), Honorary Chair

## Steering Committee

Francis Balestra (IMEP Minatec, France)

Marylin Bawedin (IMEP Minatec, France)

Cor Claeys (IMEC, Belgium)

Sorin Cristoloveanu (IMEP Minatec, France)

Olivier Faynot (CEA-LETI, France)

Francisco Gámiz (Universidad de Granada, Spain)

Elena Gnani (University of Bologna, Italy)

Benjamin Iñiguez (Universitat Rovira i Virgili, Spain)

Enrico Sangiorgi (University of Bologna, Italy)

Luca Selmi (University of Udine, Italy)

Viktor Sverdlov (TU Wien, Austria)

Andrei Vladimirescu (ISEP, France)

ISBN 978-1-4673-8608-1 IEEE Catalog number CFP1649D-USB

# Technical Program Committee

M.Ashraf Alam (Purdue University, USA)
Francis Balestra (IMEP Minatec, France)
Marylin Bawedin (IMEP Minatec, France)
Cor Claeys (IMEC, Belgium)
Jean Pierre Colinge (TSMC, Taiwan)
Nadine Collaert (IMEC, Belgium)
Sorin Cristoloveanu (IMEP Minatec, France)
Kristin De Meyer (IMEC, Belgium)
Gerben Doornbos (TSMC, Belgium)
Olivier Faynot (CEA-LETI, France)
Claudio Fiegna (University of Bologna, Italy)
Denis Flandre (UC Louvain, Belgium)
Francisco Gámiz (Universidad de Granada, Spain)
Gerard Ghibaudo (IMEP Minatec, France)
Michel Haond (ST Microelectronics, France)
Jan Hoentschel (Global Foundries, Germany)
Benjamin Iñiguez (Universitat Rovira i Virgili, Spain)
David Leadley (University of Warwick, UK)
Max Lemme (University of Siegen, Germany)
Siegfried Mantl (FZ Juelich, Germany)
Stephane Monfray (ST Microelectronics, France)
Mikael Östling (KTH Royal Institute of Technology, Sweden)
Pierpaolo Palestri (University of Udine, Italy)
Thierry Poiroux (CEA-LETI, France)
Quentin Rafhay (IMEP Minatec, France)
Heike Riel (IBM Research Zurich, Switzerland)
Scott Roy (University of Glasgow, UK)
Enrico Sangiorgi (University of Bologna, Italy)
Viktor Sverdlov (TU Wien, Austria)
Jordi Sune (UA Barcelona, Spain)
Andrei Vladimirescu (ISEP, France)
Alexander Zaslavsky (Brown University, USA)

ISBN 978-1-4673-8608-1 IEEE Catalog number CFP1649D-USB

# 2016 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon

## Session I: SOI for Low Power and Sensors

**Strain-Engineering for Improved Tunneling in Reconfigurable Silicon Nanowire Transistors**
*T. Baldauf, A. Heinzig, T. Mikolajick, J. Trommer, and W.M. Weber* ..... 1

**Reconfigurable Field Effect Transistor for Advanced CMOS: A Comparison with FDSOI Devices**
*C. Navarro, S. Barraud, S. Martinie, J. Lacord, M.-A. Jaud, and M. Vinet* ..... 5

## Session II: Tunnel FETs

**III-V-based Hetero Tunnel FETs: A Simulation Study with Focus on Non-ideality Effects (invited)**
*A. Schenk, S. Sant, K. Moselund, and H. Riel* ..... 9

**Intrinsic Voltage Gain of Line-TFETs and Comparison with Other TFET and MOSFET Architectures**
*P. G. D. Agopian, J. A. Martino, R. Rooyackers, A. Vandooren, E. Simoen, A. Thean, and C. Claeys* ..... 13

**Optimization of GaSb/InAs TFET Exploiting Different Strain Configurations**
*M. Visciarelli, E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani* ..... 16

**Assessment of Confinement–Induced Band–to–Band Tunneling Leakage in the FinEHBTFET**
*J. L. Padilla, C. Alper, F. Gámiz, and A.M. Ionescu* ..... 20

## Session III: Semiconductor Processing

**Process Modules for GeSn Nanoelectronics with High Sn-contents**
*C. Schulte-Braucks, S. Glass, E. Hofmann, D. Stange, N. von den Driesch, Q.T. Zhao, D. Buca, S. Mantl, J.M. Hartmann, and Z. Ikonic* ..... 24

**Controlling the Physical and Electrical Properties of ALD Grown ZnO using Nb as a Dopant**
*A. Shaw, J. D. Jin, I. Z. Mitrovic, S. Hall, J. S. Wrench, and P. R. Chalker* ..... 28

**Single-electron Transistors featuring Silicon Nitride Tunnel Barriers prepared by Atomic Layer Deposition**
*G. Karbasian, A.O. Orlov, A.S. Mukasyan, and G.L. Snider* ..... 32

**On the Scaling of Lanthanum Oxide Gate Dielectric Film into the Subnanometer EOT Range**
*H. Wong, J. Zhang, X. Feng, D. Yu, H. Iwai, and K. Kakushima* ..... 36

ISBN 978-1-4673-8608-1 IEEE Catalog number CFP1649D-USB

# Session IV: Frequency Phenomena and Noise

**Electrical Characterization of Random Telegraph Noise in Back-Biased Ultrathin Silicon-On-Insulator MOSFETs**
*C. Marquez, N. Rodriguez, F. Gámiz, and A. Ohata* ..... 40

**1/f -Noise Characteristics of AlGaN/GaN Omega Shaped Nanowire FETs**
*S. Vodapally, C.-H.Won, I.-T. Cho, J.-H. Lee, Y. Bae, S. Cristoloveanu, K.-S. Im, and Ju.-H. Lee* ... 44

**Simulation of Plasma Resonances in MOSFETs for THz-Signal Detection**
*C. Jungemann, K. Bittner, and H. G. Brachtendorf* ..... 48

# Session V: Modeling 1

**Scaling/LER Study of Si GAA Nanowire FET using 3D Finite Element Monte Carlo Simulations**
*M.A. Elmessary, D. Nagy, M. Aldegunde, N. Seoane, G. Indalecio, J. Lindberg, W. Dettmer, D. Perić, A. J. García-Loureiro, and K. Kalna* ..... 52

**Simulation Analysis of the Electro-Thermal Performance of SOI FinFETs**
*L. Wang, T. Sadi, A. R. Brown, M. Nedjalkov, C. Alexander, B. Cheng, C. Millar, and A. Asenov* .... 56

**Space-Average Impurity-Limited Resistance and Self-Averaging in Quasi-1D Nanowires**
*N. Sano* ..... 60

**Numerical Analysis and Analytical Modeling of RDF in DG Tunnel-FETs**
*M. Graef, F. Hain, F. Hosenfeld, F. Horst, A. Farokhnejad, B. Iñíguez, and A. Kloes* ..... 64

# Session VI: Advanced Memory

**Capacitor-less Memory: Advances and Challenges (invited)**
*F. Gámiz* ..... 68

**Inverse-magnetostriction-induced Switching Current Reduction of STT-MTJs and its Application for Low-voltage MRAMs**
*Y. Takamura, Y. Shuto, S. Yamamoto, H. Funakubo, M.K. Kurosawa, S. Nakagawa, and S. Sugahara* ..... 72

**A Consistent Picture of Cycling Dispersion of Resistive States in $HfO_X$ Resistive Random Access Memory**
*F.M. Puglisi and P. Pavan* ..... 76

**Performance and Reliability Comparison of 1T-1R RRAM Arrays with Amorphous and Polycrystalline $HfO_2$**
*A. Grossi, E. Perez, C. Zambelli, P. Olivo, and C. Wenger* ..... 80

**Intra-device Statistical Parameters in Variability-aware Modelling of Resistive Switching Devices**
*A. Crespo-Yepes, J. Martin-Martinez, I. Rama, M. Maestro, R. Rodriguez, M. Nafria, X. Aymerich, M. B. Gonzalez, and F. Campabadal* ..... 84

ISBN 978-1-4673-8608-1 IEEE Catalog number CFP1649D-USB

# Session VII: Design, Characterization, and Performance

**Impact of the Design Layout on Threshold Voltage in SiGe Channel UTBB-FDSOI pMOSFET**
*R. Berthelon, F. Andrieu, S. Ortolland, R. Nicolas, T. Poiroux, E. Baylac, D. Dutartre, E. Josse, A. Claverie, and M. Haond* ..... 88

**Drain Current Local Variability from Linear to Saturation Region in 28nm Bulk NMOSFETs**
*T. A. Karatsori, C. G. Theodorou, S. Haendler, C. A. Dimitriadis, and G. Ghibaudo* ..... 92

**Investigation of BSIM4 Parameter Extraction and Characterization for Multi Gate Oxide-Dual Work Function (MGO-DWF)-MOSFET**
*C. Tanaka, K. Matsuzawa, T. Miyata, K. Adachi, and A. Hokazono* ..... 96

**Confinement Orientation Effects in S/D Tunneling**
*C. Medina-Bailon, C. Sampedro, F. Gámiz, A. Godoy, and L. Donetti* ..... 100

**Volume and Interface Conduction in InGaAs Junctionless Transistors**
*L. Pirro, H. J. Park, I. Ionica, M. Bawedin, S. Cristoloveanu, L. Czornomaz, V. Djara, and V. Deshpande* ..... 104

# Session VIII: Modeling 2

**VDD Scaling of Ultra-thin InAs MOSFETs: A full-quantum Study**
*C. Grillet and M. Pala* ..... 108

**Contact Resistances in Trigate Devices in a Non-Equilibrium Green's Functions Framework**
*L. Bourdet, J. Li, J. Pelloux-Prayer, F. Triozon, M. Cassé, S. Barraud, S. Martinie, D. Rideau, and Y.-M. Niquet* ..... 112

**Analysis and Modelling of Temperature Effect on DIBL in UTBB FD SOI MOSFETs**
*A. S. N. Pereira, G. de Streel, N. Planes, M. Haond, R. Giacomini, D. Flandre, and V. Kilchytska* . 116

**Using One-dimensional Radiosity to Model Neutral Particle Flux in High Aspect Ratio Holes**
*P. Manstetten, L. Filipovic, A. Hössinger, J. Weinbub, and S. Selberherr* ..... 120

# Session IX: Advanced Devices and Three-Dimenisonal Integration

**SOI Platform for Spin Qubits (invited)**
*S. De Franceschi, R. Maurand, A. Corna, D. Kotekar-Patil, X. Jehl, M. Sanquer, R. Lavieville, L. Hutin, S. Barraud, M. Vinet, and Y.-M. Niquet* ..... 124

**First RF Characterization of InGaAs Replacement Metal Gate (RMG) nFETs on SiGe-OI FinFETs Fabricated by 3D Monolithic Integration**
*V. Deshpande, V. Djara, E. O'Connor, D. Caimi, M. Sousa, L. Czornomaz, J. Fompeyrine, P. Hashemi, and K. Balakrishnan* ..... 127

**A Sharp-Switching Gateless Device (Z3-FET) in Advanced FDSOI Technology**
*H. El Dirani, Y. Solaro, P. Fonteneau, C. A Legrand, D. Marin-Cudraz, D. Golanski, P. Ferrari, and S. Cristoloveanu* ..... 131

ISBN 978-1-4673-8608-1 IEEE Catalog number CFP1649D-USB

# Session X: End of Scaling and Beyond CMOS

**Robust EOT and Effective Work Function Extraction for 14 nm Node FDSOI Technology**
*B. Mohamad, C. Leroux, D. Rideau, M. Haond ,G. Reimbold, and G. Ghibaudo* ..... 135

**Benchmarks of a III-V TFET Technology Platform against the 10-nm CMOS Technology node Considering 28T Full-Adders**
*S. Strangio, P. Palestri, M. Lanuzza, D. Esseni, F. Crupi, and L. Selmi* ..... 139

**Improved Voltage Gain in Mechanically Stacked Bilayer Graphene Field Effect Transistors**
*H. Pandey, S. Kataria, V. Passi, M. Iannazzo, E. Alarcon, and M.C. Lemme*..... 143

**Simulation Study on the Feasibility of Si as Material for Ultra-Scaled Nanowire Field-Effect Transistors**
*Z. Stanojevic, O. Baumgartner, M. Karner, F. Mitterbauer, H. Demel, and C. Kernstock* ..... 147

# Session XI: Advanced Devices

**GDNMOS: A New High Voltage Device for ESD Protection in 28nm UTBB FD-SOI Technology**
*S. Athanasiou, C.-A. Legrand, S. Cristoloveanu, and Ph.Galy* ..... 151

**Operation of Suspended Lateral SOI PIN Photodiode with Aluminum Back Gate**
*G. Li, N. André, O. Poncelet, P. Gérard, S. Zeeshan Ali, F. Udrea, L.A. Francis, Y. Zeng, and D. Flandre* ..... 155

**RF SOI CMOS Technology on 1st and 2nd Generation Trap-Rich High Resistivity SOI Wafers**
*B. Kazemi Esfeh, V. Kilchytska, D. Flandre, and J.-P. Raskin*..... 159

**Effective Hole Mobility and Low-Frequency Noise Characterization of Ge pFinFETs**
*A.V. Oliveira, P. G. D. Agopian, J. A. Martino, E. Simoen, J. Mitard, L. Witters, R. Langer, N. Collaert, C. Claeys, and A. Thean*..... 162

# Session XII: Posters

**A Novel 3D Pixel Concept for Geiger-mode Detection in SOI Technology**
*M. M. Vignetti, F. Calmon, P. Lesieur, F. Dubois, T. Graziosi, and A. Savoy-Navarro* ..... 166

**Analog Performance of n- and p-FET SOI Nanowires Including Channel Length and Temperature Influence**
*B.C. Paz, M.A. Pavanello, M. Cassé, S. Barraud, G. Reimbold, M. Vinet, and O. Faynot* ..... 170

**Body Factor Scaling in UTBB SOI with Supercoupling Effect**
*K.R.A.Sasaki, J.A.Martino, C.Navarro, M.Bawedin, F. Andrieu, and S.Cristoloveanu*..... 174

**Current Mirrors with Strained Si Single Nanowire Gate All Around Schottky Barrier MOSFETs**
*K. Narimani, G. V. Luong, C. Schulte-Braucks, S. Trellenkamp, Q.T. Zhao, S. Mantl, and M. F. Chowdhury*..... 178

ISBN 978-1-4673-8608-1 IEEE Catalog number CFP1649D-USB

**A Method for Combined Characterization of MOSFET Threshold Voltage and Junction Capacitance Eliminating Channel Current Effect**
*D. Tomaszewski, G. Głuszko, and J. Malesińska* ..... 182

**Gated SiGe PIN Diodes Exposed to Visible Light Spectrum and Heavy-Ion Radiation**
*R. T. Bühler, C. D. Novo, M. A. G. Silveira, and R. Giacomini* ..... 186

**Recrystallization and Oxidation - Competing Processes during PECVD Ultrathin Silicon Layer High Temperature Annealing**
*R.B. Beck and K. Ber* ..... 190

**Effect of Inner Interface Traps on High-K Gate Stack Admittance Characteristics**
*A. Mazurak, J. Jasiński, and B. Majkusiak* ..... 194

**Comparative Study of Vertical GAA TFETs and GAA MOSFETs in Function of the Inversion Coefficient**
*V. B. Sivieri, P. G. D. Agopian, J. A. Martino, R. Rooyackers, A. Vandooren, E. Simoen, A. Thean, and C. Claeys* ..... 198

**Influence of Spin Relaxation on Trap-assisted Resonant Tunneling in Ferromagnet-Oxide-Semiconductor Structures**
*V. Sverdlov and S. Selberherr* ..... 202

**Modeling Heat Dissipation in an SOI Device - Finite Element Analysis at Semiconductor Die Level**
*George P. Hosey* ..... 206

**Conductivity Type Switching in Semiconductor Nanowires**
*A. Yesayan, S. Petrosyan, and F. Prégaldiny* ..... 210

**Fabrication and Characterization of InGaAs-on-insulator Lateral N+/n/N+ Structures**
*L. Czornomaz, V. Djara, V. Deshpande, D. Caimi, L. Pirro, S. Cristoloveanu, and J. Fompeyrine* ..... 214

**Enhancing Electrical Performances of Metallic DG-SET based Circuits by Tunnel Junction Engineering**
*K.G. El Hajjam, M.A. Bounouar, D. Drouin, and F. Calmon* ..... 218

**Transient Second Harmonic Generation and Correlation with Ψ-MOSFET in SOI Wafers**
*D. Damianos, I. Ionica, A. Kaminski-Cachopo, G. Vitrant, S. Cristoloveanu D. Blanc Pelissie, M. Kryger, and J. Changala* ..... 222

**Direction Dependent Three-Dimensional Silicon Carbide Oxidation Growth Rate Calculations**
*V. Šimonka, G. Nawratil, A. Hössinger, J. Weinbub, and S. Selberherr* ..... 226

**On the Influence of the Back-gate Bias on InGaAs Trigate MOSFETs**
*E.G. Marin, F.G. Ruiz, A. Godoy, J.M. Gonzalez-Medina, I. M. Tienda-Luna, A. Toral, and F. Gámiz* ..... 230

**Influence of Quantum Confinement Effects and Device Electrostatic Driven Performance in Ultra-scaled $Si_xGe_{1-x}$ Nanowire Transistors**
*Talib Al-Ameri, V. P. Georgiev, F. Adamu-Lema, X. Wang, and A. Asenov* ..... 234

**Scanning Microwave Microscopy for Non-Destructive Characterization of SOI Wafers**
*L. Michalas, I. Ionica, E. Brinciotti, L. Pirro, F. Kienberger, S. Cristoloveanu, and R. Marcelli* ..... 238

ISBN 978-1-4673-8608-1 IEEE Catalog number CFP1649D-USB

**Influence of the Ge Amount at Source on Transistor Efficiency of Vertical Gate All Around TFET for Different Conduction Regimes**
*C. C. M. Bordallo, V. B. Sivieri, J. A. Martino, P. G. D. Agopian, R. Rooyackers, A. Vandooren, E. Simoen, A. Thean, and C. Claeys* ..... 242

**Analysis of TFET and FinFET Differential Pairs with Active Load from 300K to 450K**
*M.D.V. Martino, J.A. Martino, and P.G D. Agopian* ..... 246

**Numerical Simulation of Gunn Oscillation in AlGaAs/InGaAs High-Electron Mobility Transistor**
*S.-M. Hong and J.-H. Jang* ..... 250

**Metal-Graphene Contact Capacitance**
*A.M. Slobodyan, S.I. Tiagulskiy, Yu.V. Gomeniuk, and A.N. Nazarov* ..... 254

ISBN 978-1-4673-8608-1 IEEE Catalog number CFP1649D-USB

# Strain-Engineering for Improved Tunneling in Reconfigurable Silicon Nanowire Transistors

Tim Baldauf, André Heinzig, Thomas Mikolajick, Walter Michael Weber
Center for Advancing Electronics Dresden (CfAED)
and Chair of Nanoelectronic Materials,
TU Dresden, Germany
Tim.Baldauf@namlab.com

Jens Trommer, Thomas Mikolajick, Walter Michael Weber
NaMLab gGmbH, Dresden, Germany

***Abstract*— Mechanical stress has the potential to be an efficient performance booster for diverse emerging research devices based on tunneling phenomena, such as tunnel FETs, resonant tunnel FETs and reconfigurable FETs. The effect is highly dependent on the constellation between the stress source and the crystal orientation. Although stress engineering is well established for enhancement carrier mobility, it is rather unexplored for the control of tunneling. In this work stress profiles formed by four different sources are studied by device simulations of reconfigurable silicon nanowire transistor using two independently gated Schottky junctions. Self-limited oxidation of the intrinsic silicon nanowire is used as an example to describe the effects of mechanical stress on the multi-valley band structure applying the deformation potential theory and on the average effective tunneling mass. The transfer characteristics of strained n- and p-type transistors are analyzed with respect to the current ratio between electron and hole conduction which is important to implement reconfigurable CMOS circuits. It has been verified that mechanical stress formed by oxidation as well as stressed top layers are effective options to control the current injection through the Schottky junctions and thus to achieve symmetric operation of reconfigurable nanowire devices.**

***Keywords*— *Silicon nanowire, reconfigurable logic, CMOS, RFET, SBFET, tunneling, Schottky junction, stress, strain, deformation potential, self-limited oxidation, simulation, TCAD***

## I. Introduction

As an alternative to multigate metal oxide semiconductor field effect transistors (MOSFETs) which will be ultimately limited in scaling, reconfigurable nanowire (NW) transistors (RFETs) provide an increased functionality of high integrated circuits beyond device scaling [1]-[3]. With its two independently gated Si-$NiSi_2$ Schottky junctions (SJ) at source and drain side the RFET is able to work as either a unipolar n- or p-FET device using the same physical structure [4] (Fig.1). This feature enables multifunctional and reprogrammable logic circuits. As an example, 6 RFETs realizing a logic gate that can be switched between NAND and NOR functionality as well as 1-bit adders with half of the number of transistors compared to CMOS could be shown recently [5],[6]. Nevertheless, the drain currents of unstrained n- and p-RFETs with Si-$NiSi_2$ junctions (barrier for electrons ~0.66 eV, for holes ~0.46 eV) are not symmetric and thus do not satisfy the requirements for complementary circuit operation using a device with the same geometry as n or p transistor. In this work we employ mechanical stress to modify the band structure of the semiconductor nanowire channel yielding an effective mechanism to precisely adjust the symmetry between n- and p-RFET without the need of doping or altering the electrode material composition [7]. TCAD process and device simulations are used to analyze the NW induced stress profile and the resulting transfer characteristics of n- and p-RFET, verifying the experimental evidence [4] and showing further that strain incorporation can fine-tune electron and hole tunneling currents.

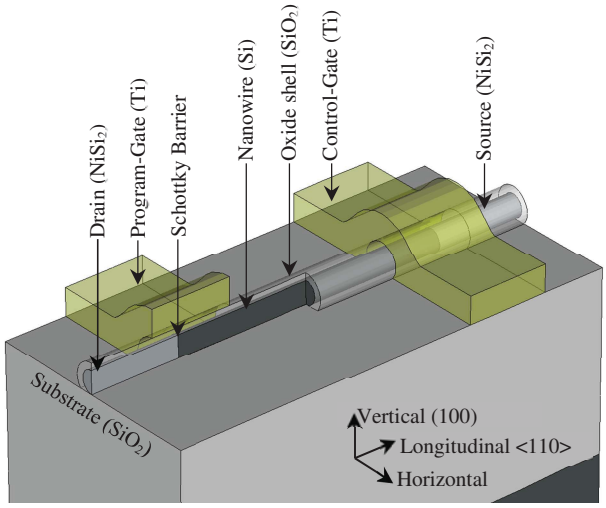



**Fig.1:** *Schematic view of a reconfigurable silicon NW-FET with two independently gated schottky junctions at source and drain side.*

For a device simulation considering stress the tunneling probability calculated by the Wentzel-Kramers-Brillouin (WKB) approximation was combined with the deformation potential theory of a multi-valley band structure and a stress depended effective tunneling mass [8]. Note that transport is not individually calculated for each subband and for tunneling the weighed contribution of each subband is lumped into a single effective band.

In this work the induced mechanical stress introduced through four different methods (Fig.2): a compressive radial stress from the oxidation of the silicon NW, epitaxial stress from the silicidation of source/drain contacts, metal gate contacts with an intrinsic compressive stress and a tensile stressed top layer deposited on top of the device.

The achieved results are also relevant and applicable for other type of devices encompassing tunneling through a barrier in the on-state.

## II. Mechanical Stress of Oxidized Silicon NW

The radial compressive stress of the silicon NW formed by oxidation is a relatively uncomplicated method to induce mechanical stress and will be described in more detail.

A 220 nm long and nearly 20 nm thick undoped silicon NW with a <110> channel direction and six facets (two times (100),

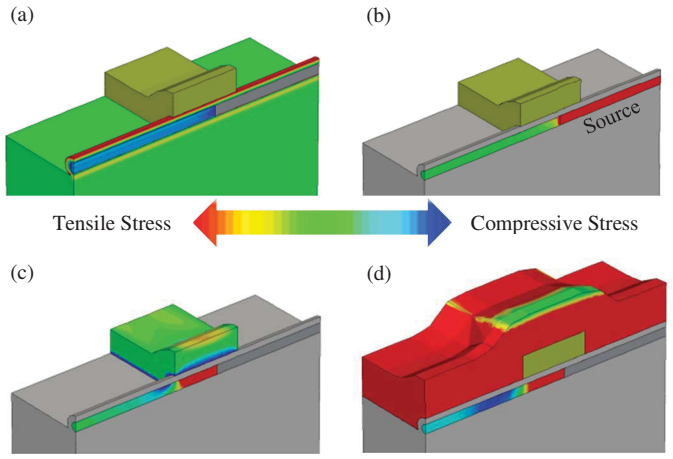



**Fig.2:** *Simulated stress profiles of silicon nanowire induced by several stress sources: (a) compressive stress from oxide shell, (b) stress from the silicidation of source/drain contacts (tensile), (c) compressive stressed metal gates and (d) tensile stressed layer on top of the device. (Scale is individual normalized to maximum value)*

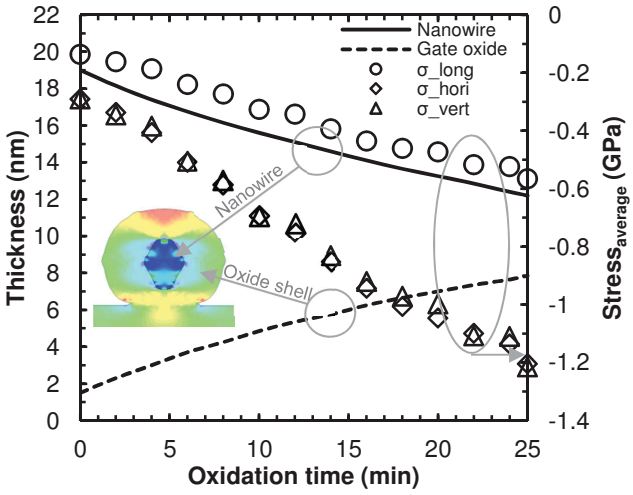



**Fig.3:** *Simulated average thickness of silicon NW $t_{si}$, gate oxide thickness $t_{ox}$ (left) and average stress values near the schottky junction (right) versus oxidation time (875 °C, $O_2$ = 10 slm). Initial values were $t_{si}$ = 19 nm and $t_{ox}$ = 1.5 nm (native oxide).*

four times (111)) was oxidized at 875°C with 10 slm $O_2$ reproducing the experimental structure [4]. Note that the reaction rate for (111) surfaces are 30 % to 100 % higher than for (100) resulting in an oval NW cross section. The appearing oxide has approximately twice the thickness versus the consumed silicon leading to a strong volume expansion of the silicon oxide shell and consequently giving a radial compressive stress in the NW (Fig.3). In addition, the stress modulated reaction rate at the Si-$SiO_2$ interfaces and the stress dependent oxygen diffusion in the tensile oxide shell cause a self-limitation of oxidation shown by the slightly saturating gate oxide thickness with increasing time. The average stress values of the three basic directions (longitudinal – channel direction, vertical – wafer orientation, horizontal – wafer flat) increase roughly linearly with the simulated oxidation time and are in a ratio of 2:1 between the radial and the longitudinal direction.

## III. Stressed Schottky Barrier Devices

The asymmetric transfer characteristics of n- and p-type NW-RFETs based on unstrained Si-$NiSi_2$ Schottky junctions arise mainly from dissimilar tunneling probabilities of electrons and holes. The simulations of an unstrained structure with 12 nm NW thickness and 8 nm gate oxide shell (after 25 min oxidation) show a ratio of 0.13 between the currents for electron n-type and the p-type device (referred to as n/p ratio in the following). Considering the mechanical stress the ratio could be enhanced to 1.20 nearly matching the experimental results with a ratio of 1.05 [4] (Fig.4). There are two sets of important parameters influencing the tunneling probability which are depending on the mechanical stress. One set is the band offset from the Fermi level of the injecting contact to the corresponding effective band edges $E_C$ and $E_V$. The other set is given by the average effective tunneling masses of electrons $\overline{m^*_{t,e}}$ and holes $\overline{m^*_{t,h}}$.

For determining the barrier heights $\Phi_{B,e}$ and $\Phi_{B,h}$ the $NiSi_2$ workfunction was fixed at ~ 4.73 eV related to the vacuum level and the affinity of the corresponding band edges was calculated. This corresponds to an ideal Schottky barrier height, neglecting for simplicity Fermi level pinning due to interface states such as metal induced gap states (MIGS). For the tunneling case at the Schottky barriers the conduction or valance band edge is so strongly bent that the width of the barrier becomes smaller than the tunneling distance of the carriers. The compressive radial stress lowers the electron barrier and thus also the barrier width increasing the tunneling probability. Conversely, the hole barrier increases and the hole tunneling probability decreases (inset Fig.3). In our simulations this stress dependent energy shift of conduction and valence band edge is taken into account by the deformation potential theory which is applied to all relevant subbands. Non-hydrostatic mechanical stress distorts the strong symmetry of the silicon lattice and results in an energetic split between the subbands. Consequently, electrons and holes are redistributed between lower or higher energy levels. The effective band edges are calculated through averaging of weighted subbands. The same methodology is employed for the average effective tunneling masses. Due to the stress that is linearly increasing with oxidation time and a direct dependency of the deformation potential the change of barrier height shows a nearly linear behavior as well (Fig.5 (a)).

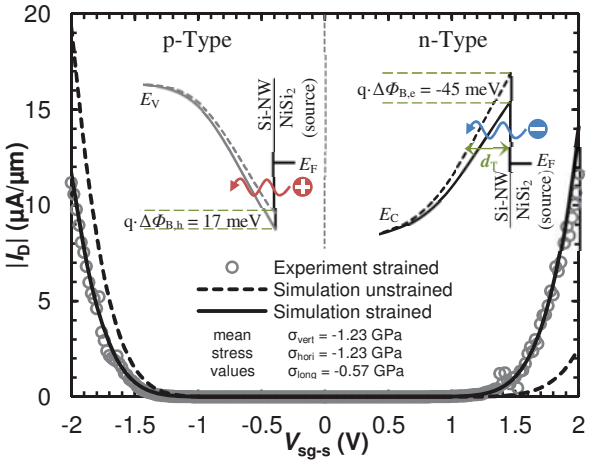



**Fig.4:** *Simulated and measured drain current of a nanowire device as a function of the control gate voltage $V_{sg-s}$ normalized to the NW diameter. The control gate voltage $V_{dg-s}$ was 2 V to achieve n- type characteristics and -2 V to achieve p-type characteristics. The drain voltage $V_{d-s}$ was to 2 V for n-Type and -2 V for p-type respectively. Simulations were performed for the unstrained case (dashed) and the included stress after 25 minutes oxidation (solid). The inset shows a schematic view of strained and unstrained electron barrier (left) and hole barrier (right) at the source junction. The vertical axis is the energy, the horizontal is the longitudinal distance to the metallurgic interface.*

The effective tunneling masses of electrons and holes are derived from band bending at the conduction band minimum and valence band maximum simulated with the empirical pseudopotential method. Each subband has its own effective tunneling mass which is oriented perpendicular to the SJ and has an indirect but exponential influence on the tunneling into or out of the subband. Mechanical stress modulates the band bending and therefore the effective mass near the subband edge where the most carriers are located. This effect is much stronger for the valence band than for the conduction band. The significant stress dependent change of the average effective tunneling mass (Fig.5 (b)) comes also from the redistribution of charge carriers as the subbands are being modulated energetically similar to the case of the effective barrier height. As an example, in the case of the radial compressive stress from oxidation combined with the <110> channel direction the electron subbands in <001> direction having an effective mass of $0.2 \cdot m_0$ are lowered while the subbands in the (110) plane with an effective mass of $0.32 \cdot m_0$ are lifted. This increases the tunneling probability into or out of the <001> - subbands compared to the <100> - or <010> - subbands and hence decreases the average effective electron tunneling mass. Conversely, the heavy hole band is lifted while the light hole band is lowered resulting in an increased average effective tunneling mass for holes.

Both effects, barrier modulation and effective mass tuning, applied individually show comparable influences on the corresponding drain current modulation $\Delta I_{D,strain}$ which is defined as the percentage difference between the strained and the unstrained simulation normalized to the unstrained value (Fig.6, 20 minutes oxidized NW). The impact of the barrier height is slightly higher than the one of effective tunneling mass most likely due to the combination of the Schottky barrier height determined by the $NiSi_2$ workfunction and the choice of silicon crystal orientation. Thus with a different crystal orientation the stress depended modulation of the average effective tunneling mass could be weaker whereby the influence of the barrier height will become dominant. It is also visible that the combination of both effects has a higher/lower impact for the electrons/holes of the n-type/p-type than expected from the linear superposition of the effects. This means that barrier height and effective tunneling mass need to be considered at the same time as the effects on the tunneling probability amplify or diminish each other under the influence of mechanical stress.

Using the stress-modulation from oxidation for NW RFETs the transport characteristics of the gated SB should always be considered in connection with the geometry of the device. Consequently, $t_{si}$ and $t_{ox}$ are determined by the oxidation time and have a direct influence on the gate control.

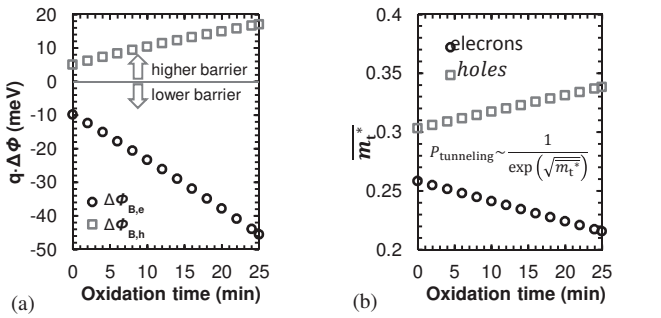



**Fig.5:** *Stress dependent parameters as function of oxidation time (a native oxide of 1.5 nm was assumed): (a) change of barrier height and (b) effective electron and hole mass averaged over the corresponding subbands.*

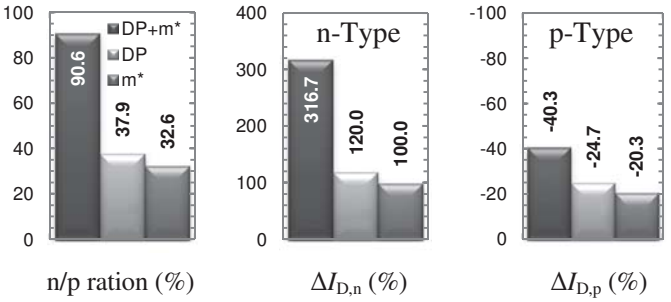



**Fig.6:** *n/p ratio and drain current modulations ($\Delta I_{D,strain}$) caused by a 20 min oxidization in a RFET structures. The three bars show the dependency of the stress modulated effective tunneling mass only (m*), the deformation potential theory only (DP) and the combination of both methods (DP+m*).*

The effect is shown in Fig.7 by the n/p ratio of an unstrained device. A thinner gate oxide achieved after short oxidation times allows a stronger band modulation in the NW and increases the tunneling through the higher electron barrier. Therefore the n/p ratio is increased. With the progressive oxidation the ration as determined by pure geometric and electrostatic considerations decreases to 13 %. This can be compensated with mechanical stress shown by the n/p ratio of the strained device. For this combination of a NW with 19 nm initial diameter and 1.5 nm initial native oxide we simulated a nearly ideal n/p ratio of 100 % after 22 minutes oxidation time comparable to the experimental result of 105 %. It can also be assumed that NWs with thinner initial $t_{si}$ have less volume compared to the grown gate oxide then thicker ones and will be more stressed after the same oxidation time.

To decouple the stress effects from the geometry in device simulations every oxidation time was simulated with and without stress dependent models to calculate a relative drain current change $\Delta I_{D,strain}$ for n- and p-RFET. The stress induced current amplification of the n-type transistors increase slightly exponential in this case and rises up to approximately 400 %. In contrast p-type transistors show degradation up to -50 %.

As mentioned above, a thick gate oxide with high radial stress is a disadvantage for the gate control hence other possible stress sources have been investigated. As first alternative the epitaxial stress from the silicidation of the source and drain contacts should be considered.

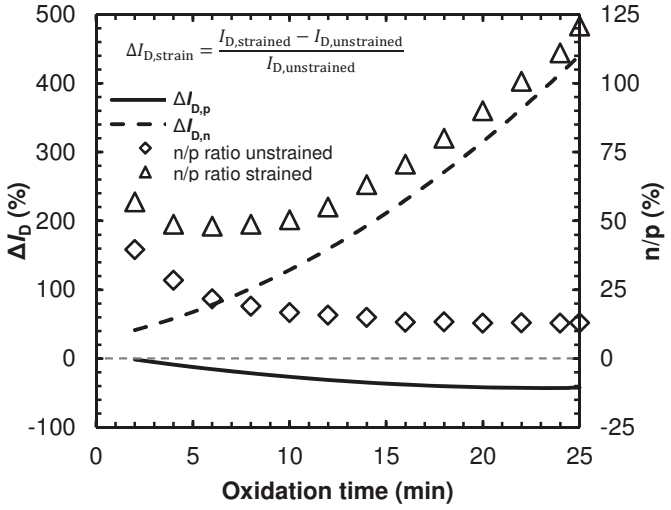



**Fig.7:** *Stress induced modulation of the drain current $\Delta I_{D,strain}$ (lines) and n/p ratio of strained and unstrained RFET structures (symbols) as a function of oxidation time. For the thicknesses of Si-NW or gate oxide as well as average mechanical stress of the corresponding oxidation time see Fig.3.*

It could be observed that such a thin NW structure promote the formation of a very sharp silicon rich $NiSi_2$ phase with a lattice constant slightly smaller than silicon and hence an intrinsic tensile stress for the silicide region should be formed [9]. Results on the exact stress values are currently not available. Therefore, an estimated intrinsic tensile stress of 500 MPa was assumed. In the process simulation it could be seen that this stress expands only on the first 5 nm distance within the silicon NW beyond the metallurgic junction and relaxes strongly which results in relatively low average stress values above the tunneling region (Tab.1). Thus, no large changes in effective tunneling mass and band deformation occur leading to a slightly increased n/p ratio of 19 % for a comparable structure with 12 nm NW thickness and 8 nm gate oxide shell (after 25 min oxidation). A further source of mechanical stress could be the top lying gate contact. Depending on the process conditions a tensile or compressive stress can be imprinted [10]. Both variants, with +1.0 GPa and -1.0 GPa intrinsic gate stress, have been examined. With the compressive gate we achieved a n/p ratio of 31 % although a raised electron and a lowered hole barrier degrading the ration actually. The resulting improvement of the ratio comes from the increased effective tunneling mass of holes.

The most promising alternative is a stressed top layer above the complete structure. Silicon-nitride ($Si_3N_4$) is normally used for stress enhanced planar MOSFETs in industrial production and can be produced either with a compressive intrinsic stress up to 3.5 GPa or a tensile intrinsic stress up to -1.7 GPa [11][12]. That makes this stress source very generally applicable for use in other nano-scale transistor types having an energy barrier for tunneling in the on-state and also for application to different crystal orientations. In the case of the NW RFET a tensile stressed top layer could improve the n/p ratio to 25 % for the comparable structure to a 25 minutes oxidized NW. To improve the stress application by the silicon-nitride top layer we simulated also a structure with a gate oxide thickness of only 2 nm having an unstrained n/p ratio of nearly 60 %. However, it was also necessary to adjust the thickness of the gate contact lying between the stressed top layer and the SB because the gate material directly at the interface to the tensile silicon-nitride becomes compressively stressed eliminating the tensile stress originating from the sides of the gate region. Thus, for certain gate thicknesses the stress above the SB can vanish. This calls for a thicker gate layer to relax the compressive component of the top side interface and to develop the tensile portion over the SB. For the improved RFET structure with the tensile stressed top layer we observed a n/p ratio of 1.09 %.

**Tab.1:** *Overview of the simulated imprinted stress values, stress dependent effective masses and change of barrier height as well as n/p ratio (unstrained **0.13**) for the four investigated stress sources.*

| | Oxide (compressive) | $NiSi_2$ (tensile) | Metal-Gate (compressive) | Overlayer (tensile) |
|---|---|---|---|---|
| $\sigma_{long}$ (GPa) | -0.57 | 0.12 | 0.59 | 0.37 |
| $\sigma_{hori}$ (GPa) | -1.23 | -0.09 | -0.24 | 0.08 |
| $\sigma_{vert}$ (GPa) | -1.23 | -0.08 | 0.41 | -0.30 |
| $m_{t,e}^* / m_{t,h}^*$ | 0.22/0.34 | 0.25/0.31 | 0.28/0.52 | 0.21/0.27 |
| $q{\cdot}\Delta\Phi_{B,e}$ / $q{\cdot}\Delta\Phi_{B,h}$ (meV) | -45/17 | 0/-1 | 8/-13 | -8/-8 |
| **n/p** | **1.20** | **0.19** | **0.31** | **0.25** |

## IV. Conclusion

Mechanical stress provides a flexible dopant-free method to adjust drain currents in energy barrier based transistors and to precisely tune the ratio between the current of the n- and the p-RFET. A stress profile generated by thermal oxidation of the silicon NW was used to describe the stress dependent multi-valley band structure and the average effective tunneling mass as primary modifiable parameter of the current injection through the Schottky junctions. Furthermore, we could show the influence of both parameters separately as well as the amplifying impact of their combination. With the oxidized NW RFET we achieved a symmetric transfer characteristic between n- and p-RFET, highly matching previous reported experimental results of [4]. As alternative to a thick gate oxide with disadvantages for the electrostatics of the device we investigated the mechanical stress formed by the silicidation of the source and drain contacts, the metal-gate and a stressed silicon-nitride overlayer. A tensile overlay in combination with an improved structure seems to be a promising approach for current VLSI technologies providing the applicability of this method in conventional top-down process flows. In summary mechanical stress is a versatile tool to tune electron and hole conduction in devices based on barrier tunneling (RFETs) as well as band-to-band tunneling devices (TFETs) [13].

## Acknowledgment

Parts of this work is supported by “Deutsche Forschungs-Gemeinschaft (DFG)” in the project ReproNano (MI 1247/6-2 and WE 4853/1-2) and the Cluster of Excellence `CfAED`

## References

[1] C. W. Lee, C. G. Yu, J. T. Park, J. P. Colinge, “Device design guidelines for nano-scale MuGFETs”, *Solid-State Electronics*, vol. 51(3), pp. 505-510, 2007

[2] W. M. Weber, A. Heinzig, J. Trommer, D. Martin, M. Grube, T. Mikolajick, “Reconfigurable nanowire electronics – A review”, *Solid-State Electronics*, vol. 102, pp. 12-24, 2014

[3] J. Zhang, X. Tang, P.-E Gaillardon, G. De Micheli, “Configurable Circuits Featuring Dual-Threshold-Voltage Design With Three-Independent-Gate Silicon Nanowire FETs”, *IEEE Transactions on Circuits and Systems I*, vol.61(10), pp 2851-2861, 2014

[4] A. Heinzig, J. Trommer, D. Grimm, T. Mikolajick, W. M. Weber, “Dually active silicon nanowire transistors and circuits with equal electron and hole transport”, *Nano Lett.*, vol. 13, pp. 4176–4181, Aug. 2013

[5] J. Trommer, A. Heinzig, S. Slesazeck, T. Mikolajick, W. M. Weber, “Elementary aspects for circuit implementation of reconfigurable nanowire transistors”, *IEEE electron device letters*, vol. 35(1), pp. 141-143, 2014

[6] J. Trommer, A. Heinzig, T. Baldauf, S. Slesazeck, T. Mikolajick, W. M. Weber, “Functionality-Enhanced Logic Gate Design Enabled by Symmetrical Reconfigurable Silicon Nanowire Transistors”, *IEEE Transactions on Nanotechnology*, no. 99, 2015

[7] T. Baldauf, A. Heinzig, J. Trommer, T. Mikolajick, W.M. Weber, “Stress-Dependent Performance Optimization of Reconfigurable Silicon Nanowire Transistors”, *IEEE Electron Device Letters*, vol.36(10), pp. 991-993, 2015

[8] M. V. Fischetti, S. E. Laux, “Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys”, *J. Appl. Phys*. 1996, 80: 2234

[9] A. Steegen and K. Maex, “Silicide-induced stress in Si: origin and consequences for MOS technologies”, *Materials Science and Engineering: R: Reports*, vol. 38.1, pp. 1-53, 2002.

[10] C. Y. Kang, et al., “A Novel Electrode-Induced Strain Engineering for High Performance SOI FinFET utilizing Si (1hannel for Both N and PMOSFETs”, *IEEE International Electron Devices Meeting*, Proceedings IEDM'06, 2006.

[11] S. Flachowsky, A. Wei, T. Herrmann, et al., “Gate length scaling trends of drive current enhancement in CMOSFETs with dual stress overlayers and embedded-SiGe”, *Materials Science and Engineering*, vol. 154, pp. 98-101, 2008

[12] S. E. Thompson, et al., “Uniaxial-process-induced strained-Si: extending the CMOS roadmap”, *IEEE Transactions on Electron Devices*, vol. 53.5 pp. 1010-1020, 2006

[13] Q. T. Zhao, J. M. Hartmann, S. Mantl, “An improved Si tunnel field effect transistor with a buried strained source”, *IEEE Electron Device Letters*,vol. 32(11), pp. 1480-1482, 2011

# *Reconfigurable field effect transistor for advanced CMOS: a comparison with FDSOI devices*

C. Navarro, S. Barraud, S. Martinie, J. Lacord, M.-A. Jaud and M. Vinet
CEA-LETI, MINATEC Campus, F-38054 Grenoble, France
E-mail: Carlos.NAVARRO@cea.fr

***Abstract*— The optimization of Reconfigurable FET (RFET) devices is carried out in planar SOI technology. The electrostatic behavior, drive current and logic inverter operation are then discussed and compared with planar 28nm FDSOI devices.**

***Keywords—CMOS; FDSOI; Reversible FET; Reconfigurable FET; RFET; Schottky barrier;***

## I. INTRODUCTION

Much attention is being paid nowadays to alternative devices for future electronics. Among all the possible candidates (Trigate FETs [1], Tunneling FETs [2], stacked nanowires [3]…), Reconfigurable FETs, RFETs [4], stand as an interesting path to achieve reprogrammable logic in future circuits.

RFETs feature metallic source and drain (S/D) regions. Additional polarity gates (PGs) control the S/D schottky barriers (SB). This allows to in-situ switch from N to P-like FETs by selecting which carrier is injected by tunneling. The RFET advantages are: i) no doping required for S/D regions (no random dopant fluctuations), ii) fewer fabrications steps and lower thermal budget (no S/D implantation, dopant activation or epitaxy), iii) possible reduction of device number for similar logic functions and iv) reversible operation.

In this work we optimized the RFET structure (Fig. 1a-c) and we realize a native benchmark with FDSOI (Fig. 1d) using identical 28 nm planar technology at device and single stage circuit level.

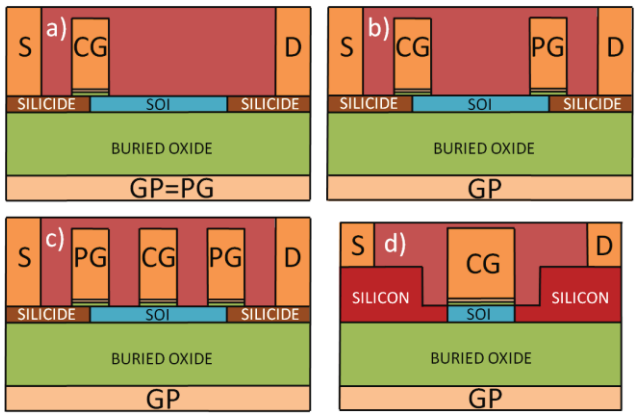



*Fig. 1. a) 1-Gate, b) 2-Gates and c) 3-Gates RFET structures compared to d) 28 nm FDSOI featuring same gate-stack and films thicknesses. S/D regions are metallic (silicides) in RFETs while highly doped Silicon is used in FDSOI. CG = control gate, PG = polarity gate and GP = ground plane.*

## II. RFET: PRINCIPLES OF OPERATION

The RFET theory follows the basis of SB-MOSFETs [5, 6]. The metallic S/D regions guarantee the conduction of either electrons or holes. Since the S/D metal workfunction is not aligned with the Silicon energy of conduction or valence bands, the injection of carriers in the channel is poor and requires the modulation of the schottky barrier thickness close to the source. The current is then determined by the thermionic (carriers with enough energy to surmount the energy barrier) and the field emission (carrier tunneling the barrier) transport mechanisms. In order to achieve symmetrical N/P transfer characteristics, metal work-functions close to the Silicon mid-gap are preferred. This makes the thermionic emission to be very low due to the relatively high electron/hole schottky barrier (close to half the Silicon energy band-gap, $\phi_b \approx 0.56$ eV). The modulation of the front-channel energy bands by the PGs is represented in Fig. 2 for the 3-Gates RFET structure (Fig. 1c) at low drain voltage ($V_{DS} \approx 0V$). As observed, the energy barrier thickness, related to the carrier tunneling, can be controlled thanks to the PG voltage applied with respect to S/D. Positives PG biases enable electrons to tunnel from the metallic source to the conduction band (Fig. 2a) while negative voltages do the same for holes toward the valence band (Fig. 2b). This carrier injection is more efficient closer to the front-channel where the electrostatic control induced by the polarity gates permits a sharper energy band bending. On the other hand, the control gate (CG) is responsible of controlling the current flow by inducing (OFF-state) or not (ON-state) an energy barrier in the middle of the channel.

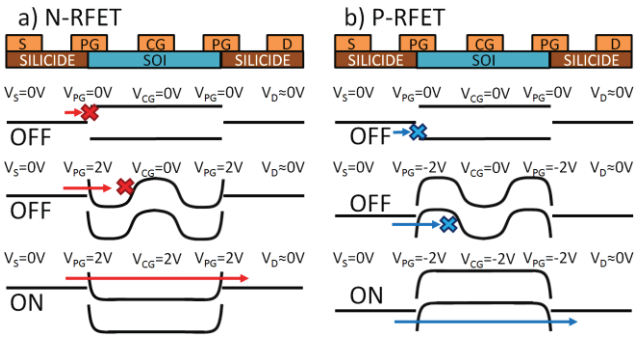



*Fig. 2. Simplified front-channel energy bands diagram for the 3-Gates RFET at $V_{DS} \approx 0V$. a) N-type ($V_{PG}$=+2V) and b) P-type operation ($V_{PG}$=-2V) in OFF-state and ON-state. The PGs select the carrier that is allowed to tunnel while the CG controls the current flow (ON/OFF) from source to drain as in typical MOSFETs.*

## III. Simulation Setup

Three different RFET configurations were initially considered based on the number of top gates. In case of the 1-Gate (1G) RFET (Fig. 1a); in order to achieve the reversible behavior, the device takes advantage of the planar FDSOI structure and uses the ground plane (GP) as PG to select between the N and P operation while the top gate acts as typical current control gate [7]. The opposite configuration with the top gate working as PG and the GP as CG was also considered. On the other hand, both the 2-Gates (2G) (Fig. 1b) [4] and 3-Gates (3G) RFETs (Fig. 1c) [8] architectures rely on one or two functional top PGs to privilege the tunneling of a given carrier (the GP remains grounded). Preliminary simulations, using Synopsys TCAD [9], were carried out to optimize these planar RFET structures in terms of electrostatics (DIBL, subthreshold Swing (SS) and driven current, $I_{ON}/I_{OFF}$) and discern the most promising. The computation of the tunneling probabilities is based on the WKB approximation by using non-local tunneling between silicides and silicon [9]. The S/D silicide workfunction is set to 4.66 eV ($\phi_b \approx 0.61/0.51$ for electrons/holes) while the relative electron effective masses are $m_e^* = 0.3$ and $m_h^* = 0.2$ as in [10]. The resultant performance is strongly affected by the selected RFET design, Fig. 3. The main electrostatic parameters are summarized in Table 1 for the different RFETs configurations at constant Si-film length, $L_{SOI}$ = 120nm. Among all the architectures considered, the 3G-RFET is the unique demonstrating competitive electrostatic characteristics: SS below 100 mV/dec, sub-100 mV/V DIBL and $I_{ON}/I_{OFF}$ around $10^6$ A/A.

The final optimized 3G-RFET structure features $t_{SOI}$ = 6.5 nm, $t_{BOX}$ = 25 nm and EOT = 1.55 nm. The gates length is fixed to 20 nm while their spacing is 15 nm. The overlapping of PGs with the body is 10 nm leading to a final silicon film length of $L_{SOI}$ = 70 nm. The carrier mobility fits experimental 28 nm FDSOI results at similar gate length [11] (constant mobility fixed at 227/60 $cm^2 \cdot V^{-1} \cdot s^{-1}$ for electrons/holes). The FDSOI structure used to benchmark the RFETs presents a 27 nm control gate with the same film architecture than RFETs. A 15 nm epitaxy is performed to raise the S/D regions and reduce the series resistance. Unless otherwise specified, all devices feature a constant width of 1µm.

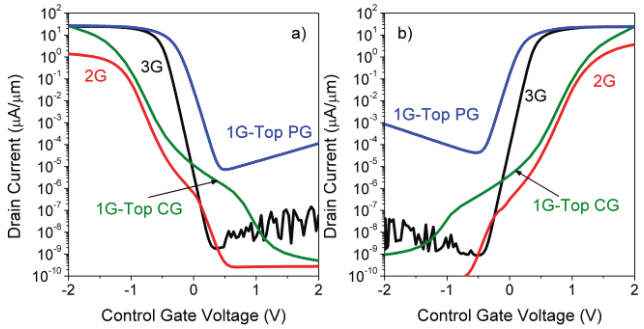



*Fig. 3. a) P-RFET and b) N-RFET comparison between different architectures featuring distinct number of top-gates (Fig. 1a-c). $V_{BG}$=0V (2G & 3G) and $V_{DS}$=±1V. $V_{PG}$=2V (N-RFET) and $V_{PG}$=-2V (P-RFET). $L_{CG/PG}$ = 30nm, $L_{SOI}$ = 120nm, EOT ≈ 1.5nm, $t_{SOI}$ = 10nm and $t_{BOX}$ = 25nm.*

TABLE I. RFET Comparison

| - | | SS mV/dec | DIBL mV/V | $I_{ON}$ µA/µm | $I_{OFF}$ nA/µm | $I_{ON}/I_{OFF}$ $\cdot 10^5$A/A |
|---|---|---|---|---|---|---|
| 1G-RFET Top = CG | P | 169.3 | - | 16.5 | 15.86 | 0.01 |
| | N | 174.9 | - | 16.9 | 21.11 | 0.008 |
| 1G-RFET Top = PG | P | 110.0 | - | 19.8 | 0.90 | 0.22 |
| | N | 108.1 | - | 18.5 | 0.73 | 0.25 |
| 2G-RFET | P | 149.9 | - | 1.5 | 192.4 | 0.00007 |
| | N | 161.3 | - | 3.9 | 62.1 | 0.0006 |
| 3G-RFET | P | 80.2 | 46.3 | 21.5 | 0.05 | 4.32 |
| | N | 78.7 | 45.3 | 19.6 | 0.04 | 4.30 |

**Table 1:** *Planar RFET comparison for different number of top gates. $V_{BG}$ =0V (2G & 3G) and $V_{DS}$=±1V. $V_{PG}$=2V (N-RFET) and $V_{PG}$=-2V (P-RFET). $V_T$ = $V_{CG}$ ($I_{DS}$=0.1µA/µm), $I_{ON}$ = $I_{DS}$ ($V_{CG}$=$V_T$±0.65V) and $I_{OFF}$ = $I_{DS}$ ($V_{CG}$=$V_T$∓0.35V). $L_{CG/PG}$ = 30nm, $L_{SOI}$ = 120nm, EOT ≈ 1.5nm, $t_{SOI}$ = 10nm and $t_{BOX}$ = 25nm.*

## IV. Optimized 3G-RFET vs. FDSOI

Fig. 4 presents the drain current comparison between the 3G-RFET and FDSOI. Table 2 outlines the $I_{ON}/I_{OFF}$ ratio currents and the main electrostatic results at minimum and equivalent effective gate length for FDSOI. The RFETs ON current is about 15-50 times lower. This reduction of drain current is related to: i) the low efficiency of the carrier injection mechanism by tunneling (at silicide/silicon interface), ii) to the additional resistance between PG and CG contacts and iii) to the reduced lateral electric field. Fig. 5 illustrates the top-interface energy bands for similar biasing conditions and effective gate length. The lateral electric field (slope of the energy) is weaker in RFETs than in FDSOI. The equipotential lateral PGs prevent the development of an intense lateral field to accelerate carriers leading to a lower drain current. The control gate capacitance is compared in Fig. 6a for $V_{DS}$ = 0V in isolated devices. Fig. 6b presents the RFET polarity gate capacitance.

TABLE II. Electrostatic Results

| - | | SS mV/dec | DIBL mV/V | $I_{ON}$ µA/µm | $I_{OFF}$ nA/µm | $I_{ON}/I_{OFF}$ $\cdot 10^5$A/A |
|---|---|---|---|---|---|---|
| 3G-RFET | P | 84 | 98 | 24.5 | 0.19 | 1.27 |
| | N | 84 | 94 | 22.2 | 0.20 | 1.11 |
| 27 nm FDSOI | P | 95 | 148 | 447 | 1.19 | 3.77 |
| | N | 94 | 136 | 1160 | 0.88 | 13.1 |
| 60 nm FDSOI | P | 71 | 37 | 309 | 0.03 | 117 |
| | N | 70 | 30 | 1020 | 0.02 | 518 |

**Table 2:** *Optimized 3G RFET vs. FDSOI benchmark in planar 28-FDSOI. $V_{BG}$=0V and $V_{DS}$=±1V. $V_{PG}$=2V (N-RFET) and $V_{PG}$=-2V (P-RFET). $V_T$ = $V_{CG}$ ($I_{DS}$=0.1µA/µm), $I_{ON}$=$I_{DS}$ ($V_{CG}$=$V_T$±0.65V) and $I_{OFF}$ =$I_{DS}$ ($V_{CG}$=$V_T$∓ 0.35V).*

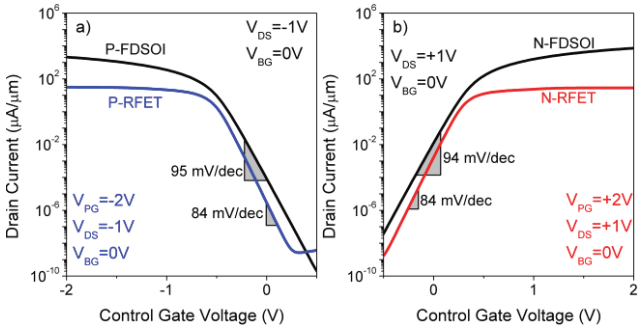



*Fig. 4. a) P- and b) N-type current comparison between optimized 3G RFET and FDSOI devices. RFET $L_{SOI}$=70nm. FDSOI $L_{SOI}$=27nm.*

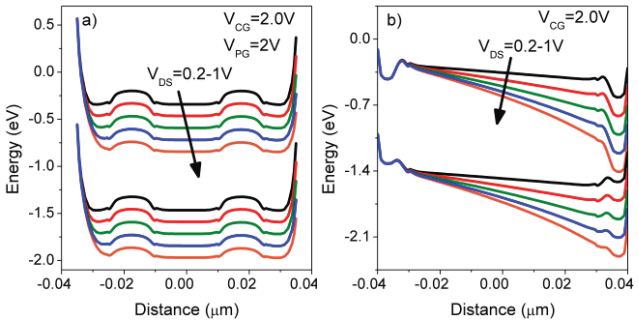



*Fig. 5. Horizontal (≈ 0.5 nm from top-interface) N-MOS conduction and valence energy bands for (a) RFET and (b) FDSOI at similar length. $V_{BG}$=0V.*

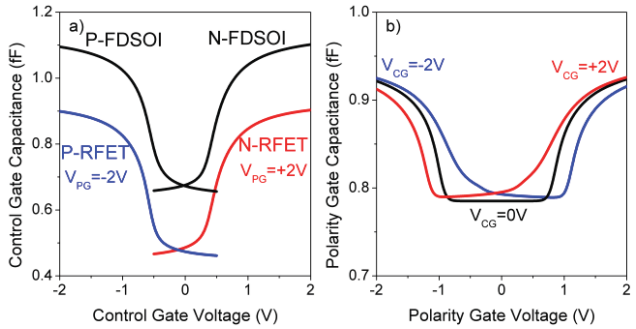



*Fig. 6. Capacitance benchmark for a) control gate in isolated RFET and FDSOI. b) Single 3G RFET polarity-gate capacitance at different control gate biases. $V_{DS}$=0V and $V_{BG}$=0V. FDSOI/RFET $W_P$=$W_N$=1μm.*

Despite the smaller RFET control gate capacitance due to the thicker spacers, the additional PGs yield a larger load capacitance when driving all top gates simultaneously to reprogram the device.

Fig. 7a depicts the mixed-mode voltage-transfer characteristics (VTC) of logic inverters made with FDSOI and RFET devices. The RFET VTC is degraded since the drain current at high/low (N/P-RFET) $V_{CG}$ is determined by the tunneling barrier thickness rather than by the control gate-induced energy barrier. Fig. 7b illustrates how the FDSOI inverter response outraces the RFET. A 0.3 fF capacitance was included at the output to account for parasitic as in [12]. No other capacitances or resistances due to interconnections have been accounted. The rise, $t_{LH}$, and fall, $t_{HL}$, times are calculated as the crossing points at 50% of the power supply, $V_{DD}$, and averaged to extract the inverter propagation delay [13], $\tau_P$, in Fig. 8a. RFETs feature, at least, 70 times larger delay than FDSOI ($V_{DD}$ = 2V). These delay differences contrast with the inverter logical effort, *g*, stated in [14]. The modest RFET currents, Fig. 8b, yield high equivalent resistances ($R=V_{DS}/I_{DS}$), thus longer $\tau_P$ [13]:

$$\tau_P = \ln(2)\cdot C_L \cdot R \qquad (1)$$

with $C_L$ being the total inverter load capacitance. Fig. 8b also demonstrates the symmetric current curves for N- and P-RFETs and how RFETs are not suitable for low-power applications (< 1V). As $V_{DD}$ is reduced, the current

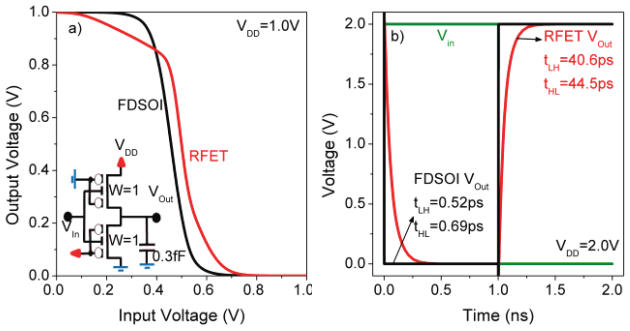



*Fig. 7. Mixed-mode a) Voltage-Transfer Characteristics and b) transient response to square signal. Inset: RFET inverter with 0.3 fF output capacitance. FDSOI $W_P$=2·$W_N$. RFET $W_P$=$W_N$.*

dramatically drops. The energy-bands bending is small resulting in thick energy barriers and low tunneling efficiency.

To compute the energy per transition, E, we used [13]:

$$E = C_L \cdot V_{DD}^2 \qquad (2)$$

where $C_L$ was approximated using Eq. (1) through the propagation delay ($\tau_P$) and the equivalent resistance obtained with the maximum current (Fig. 8b). $C_L$ = 2.2 and 2.0 fF were obtained for FDSOI and RFET inverters, respectively. These capacitance values agree with results in Fig. 6a. The averaged energy per transition is represented in Fig. 9a. Very similar values are found for both FDSOI and RFETs as a result of having comparable output capacitances, $C_L$. As observed, the energy can be made arbitrarily low by reducing the power supply. From this perspective, the optimum voltage to run the circuit would be the lowest possible that still ensures functionality. This comes at expense of the delay, Fig. 8a. A more relevant metric combining the measure of consumption and performance is the energy delay product (EDP) [13], represented in Fig. 9b:

$$EDP = E\cdot \tau_P \qquad (3)$$

The optimum $V_{DD}$ is therefore 1 V for FDSOI while for RFETs is larger than the maximum $V_{DD}$ considered, 2 V. In any case, we find a much lower EDP for 28 nm FDSOI technology than for RFETs.

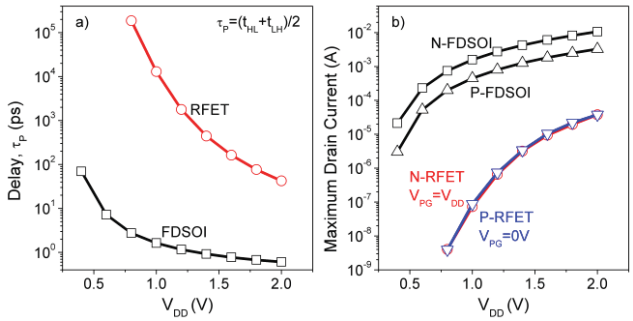



*Fig. 8. a) Mixed-mode delay and b) isolated device maximum drain current benchmark. The RFET delay is much larger than in FDSOI due to the low tunneling current.*

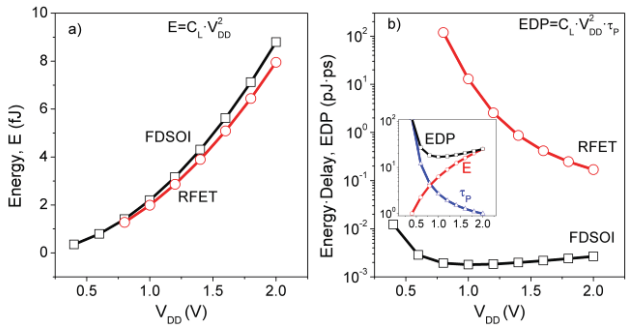



*Fig. 9. a) Energy per operation and b) energy delay product comparison. The inset shows the normalized energy, delay and EDP for FDSOI.*

## V. Conclusions and Perspectives

We have shown that RFETs turn to be not competitive at device or single logic gate level as compared to 28 nm FDSOI technology. Their limited current leads to much larger delays and EDP. Nevertheless, the advantages are expected to arise from a wise, but challenging, circuit conception where the reprogrammable logic can be useful to reduce the number of devices required.

## *Acknowledgment*

Project supported by the French ANR via Carnot funding.

## *References*

[1] S. Barraud *et al.*, "Performance of omega-shaped-gate silicon nanowire MOSFET with diameter down to 8nm," *IEEE Electron Dev. Lett.*, vol. 33, p. 1526, 2012.

[2] A. Villalon *et al.*, "Experimental investigation of the tunneling injection boosters for enhanced ION ETSOI Tunnel FET," *IEEE Trans. Electron Dev.*, vol. 60, pp. 4079, 2013.

[3] L. Gaben *et al.* "Stacked-Nanowire and FinFET transistors: guidelines for the 7nm node", In proceedings of the 2015 International Conference on Solid State Devices and Materials.

[4] A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick, and W.M. Weber, "Reconfigurable Silicon Nanowire Transistors," *Nano Letters*, vol. 12 (1), 119, 2012.

[5] M.p. Lepselter and S.M. Sze, "S-IGFET: An insulated-gate field-effect transistor using Schohttky barrier contacts for source and drain," *Proc. IEEE*, vol. 56 (8), pp. 1400, 1968.

[6] J.M. Larson and J.P. Snyder, "Overview and status of metal S/D Schottky-barrier MOSFET technology," in *Electron Devices, IEEE Transactions on* , vol. 53 (5), pp. 1048, 2006.

[7] U. Schwalke, T. Krauss and F. Wessely, "CMOS without Doping on SOI: Multi-Gate Si-Nanowire Transistors for Logic and Memory Applications," in ECS J. Solid State Sci. Technol., vol. 2 (6), Q88, 2013.

[8] J. Zhang, X. Tang, P-E. Gaillardon, G. De Micheli, "Reconfigurable Silicon Nanowire Transistors," in *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61 (10), pp. 2851, 2014.

[9] Synopsys TCAD, Version J-2014.09-SP2, Synopsys, Inc, 2014.

[10] J. Trommer, A. Heinzig, S. Slesazeck, T. Mikolajick and W.M. Weber, "Elementary Aspects for Circuit Implementation of Reconfigurable Nanowire Transistors," in *IEEE Electron Device Lett.*, vol. 35 (1), pp.141, 2014.

[11] B. DeSalvo *et al.*, "A mobility enhancement strategy for sub-14nm power-efficient FDSOI technologies," in *Electron Devices Meeting (IEDM), 2014 IEEE International*, pp.7.2.1, 2014.

[12] M. De Marchi *et al.*, "Top-Down Fabrication of Gate-All-Around Vertically-Stacked Silicon Nanowire FETs With Controllable Polarity," in *IEEE Trans. Nanotechnol*, vol. 13 (6), pp. 1029, 2014.

[13] J.M. Rabaey, A. Chandrakasan and B. Nikolic, in "The CMOS inverter" in *Digital Integrated Circuits. A Design Perspective*, Prentice Hall, 2003.

[14] J. Trommer *et al*., "Functionality-Enhanced Logic Gate Design Enable by Symmetrical Reconfigurable Silicon Nanowire Transistors" *IEEE Tans. Nanotechnol*., vol. 14 (4), pp. 689, 2015.

# III-V-based Hetero Tunnel FETs: A Simulation Study with Focus on Non-ideality Effects

(Invited Paper)

Andreas Schenk*, Saurabh Sant*, Kirsten Moselund†, and Heike Riel†
*Integrated Systems Laboratory, ETH Zurich, CH-8092 Zürich, Switzerland
†IBM Research-Zurich, Säumerstrasse 4, 8803 Rüschlikon, Switzerland

Email: schenk@iis.ee.ethz.ch

## I. Abstract

We present semi-classical simulations of Gate-overlapped-Source Tunnel Field Effect Transistors (GoS-TFETs) taking into account the effects of trap-assisted tunneling, channel quantization, surface roughness, and density-of-state tails.

## II. Introduction

In quest of new (”post-CMOS”) switches, in particular for ultra-low power application, the Tunnel Field Effect Transistor (TFET) [1] raised a lot of attention. The working principle of this device is the generation of electron-hole pairs by band-to-band tunneling (BTBT) between the valence band (VB) and the conduction band (CB). Thus, contrary to the common MOSFET, the source of current in a TFET is not thermionic injection, but inter-band generation.The inter-band tunnel transitions can be either direct (at the $\Gamma$-point) or indirect (e.g. from the $\Gamma$-point to the k-point of the minimum of the CB valleys as in silicon). In the latter case a phonon is needed for momentum conservation. A TFET is essentially a gated, reversed-biased *pin* diode, and the width of the tunnel barrier is modulated by the gate voltage. It is even possible to turn on the BTBT generation quickly as a consequence of the gate-induced energetic alignment between CB and VB, which eventually results in an average slope (averaged over 3 - 4 decades in the current after the onset of BTBT) steeper than 60 mV/dec. That’s why TFETs belong to the so-called ”steep-slope devices”.

III-V/Si hetero junctions have been proposed for an improved on-current as compared to Si TFETs [2]. The BTBT rate can be increased by using small-gap semiconductors like InAs or $In_{0.53}Ga_{0.47}As$ as source material, while ambipolar leakage is reduced by the wide band gap of the channel/drain materials Si or InP. Nanowires (NWs) are advantageous in terms of gate control and strain relaxation when their diameter is scaled down [3]. Borg et al. integrated individual InAs/Si hetero-structure NW tunnel diodes onto Si using selective epitaxy in nanotube templates [4], an approach which allows to start with Si substrates of any crystalline orientation and to scale the diameter of the NWs down to reasonable limits, thereby improving previous techniques of nanometer-scale hetero epitaxy [5]–[8]. Temperature-dependent *IV*-measurements of p-type TFETs fabricated by this technology indicated that the sub-threshold swing (SS) is limited by traps [9]. The present TCAD simulation study partly takes advantage of the geometry (see Fig. 1), the measured *IV*-characteristics, and the limited electrical characterization of these devices. In this paper, all simulations are performed with the semi-classical device simulator Sentaurus-Device (S-Device) [10] using the nonlocal BTBT model with calibrated parameters [11]. Non-ideality effects as trap-assisted tunneling (TAT) via interface and bulk traps, channel quantization, roughness at material interfaces, and density-of-state (DOS) tails induced by random doping fluctuations (RDF), are modeled in the frame of the so-called Physical Model Interface (PMI) of S-Device. The developed models for the non-idealities and their impact on the transfer characteristics are presented in Section IV.

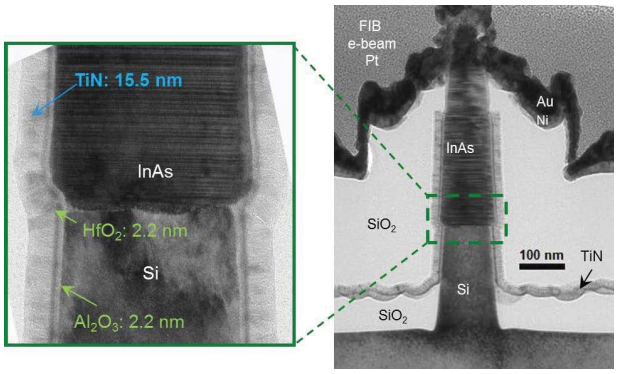



Fig. 1: TEM image of an InAs/Si NW p-TFET showing the geometrical dimensions and a close-up of the InAs/Si interface which is not smooth across the entire junction area and has a high density of defects. Also visible are stacking faults caused by the change in crystal structure of InAs between wurtzite and zincblende. Figure taken from [9].

## III. Experimental data of p-type InAs/Si NW TFETs

InAs nanowires with diameters of few tens of nanometers have been grown on Si substrates by IBM Research Zurich [12]. This material configuration provides a small effective tunnel gap (low tunnel barrier) while allowing for integration on a Si platform which maintains the advantages of Si for the channel and drain regions. Although the TFETs based on this technology (shown in Fig. 1) exhibit a good electrostatic control due to their gate-all-around configuration, they can still be considered as bulk-like, i.e. geometrical confinement is negligible. The measured transfer characteristics are shown in Fig. 2 for two different temperatures. The measured on-current at room temperature is 1.62 $\mu$A ($\sim$ 5.2 $\mu$A/$\mu$m) at $|V_{GS}|$ = 1.0 V, $|V_{DS}|$ = 0.5 V and the $I_{on}/I_{off}$ ratio is $\sim$ $10^6$. The

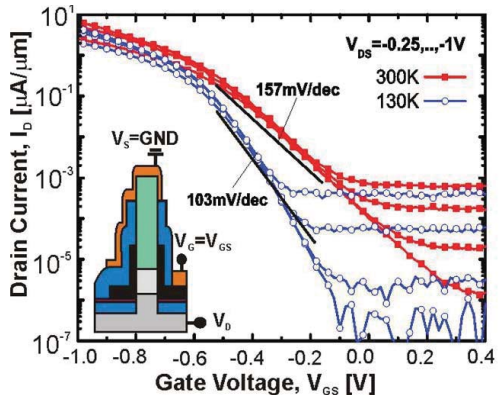



Fig. 2: Measured $I_{\mathrm{D}}V_{\mathrm{GS}}$-characteristics of the InAs/Si NW p-TFET of Fig. 1 for two temperatures and different values of $V_{\mathrm{DS}}$. Figure taken from [9].

steeper SS obtained at 130 K clearly proves the presence of traps, which limit sub-60 mV/dec operation.

## IV. Impact of Non-ideality Effects on TFET Performance

The ideal slope of the TFET characteristics (neglecting all non-idealities) is determined by the details of the onset of BTBT. In GoS-TFETs, BTBT takes place along two kinds of tunnel paths - almost parallel to the gate and across the pn-junction ("point tunneling" paths) and almost perpendicular to the gate and within the source ("line tunneling" paths). Often point tunneling sets in first, since line tunneling only starts after the energetic alignment of VB and CB (inversion conditions in the source channel). A sub-thermal SS of point tunneling is hard to achieve because a sudden and strong 3D-3D DOS matching is only possible when the band edge profile is "step-like" which requires (i) a perfect gate control, (ii) a very steep doping gradient, and (iii) preferably the gate edge exactly at the pn-junction (which, however would kill line tunneling completely). A sub-thermal SS of line tunneling is easier to achieve thanks to the cut of the semiconductor band gap at the oxide interface and the 2D-3D DOS matching. One of the design goals is, therefore, to delay the onset of point tunneling. Two means can be used for this: the band offsets of the hetero-structure and pocket implants [19]. All non-idealities discussed in the following act contrary to a sub-thermal slope.

### A. Trap-assisted Tunneling

TAT is an additional electron-hole pair generation mechanism in TFETs which sets in prior to BTBT due to the lower tunnel barrier. Being a multi-phonon, field-assisted process, it requires efficient generation-recombination (G-R) centers (as usual called "traps" in the following). Three kinds of traps may contribute to the TAT current: bulk traps, traps at the material interface of the hetero-structure, and traps at the oxide interface. Note, that CV experiments to extract $D_{\mathrm{it}}$ at interfaces do not measure the density-of-states of G-R centers active in the multi-phonon process. The latter is only a subset of the measured $D_{\mathrm{it}}$ levels. The S-Device model for interface TAT needs an additional parameter "interaction volume of the trap" which is not only a scaling factor but serves to distinguish

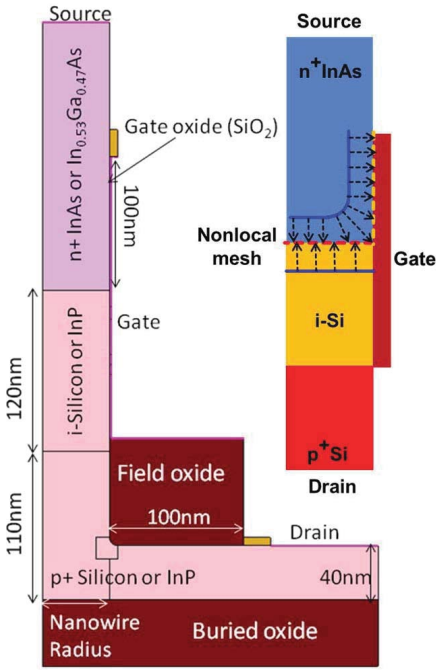



Fig. 3: Simulation domain of the GoS InAs/Si NW TFET (left) and nonlocal mesh for TAT tunnel paths from traps at hetero-interface (dashed red) and traps from gate oxide interface (dashed yellow).

between the charging of the trap levels and the electron-phonon coupling of the trap states. The physics at interfaces is highly self-consistent: already the occupation of the $D_{\mathrm{it}}$ changes the electrostatics and, thus, the onset voltage and the tunnel rates (including the BTBT rate). Surface SRH generation without tunneling causes a leakage current which appears to be gate-bias-dependent due to the downward move of the quasi-Fermi levels in the CB which gradually empties the final states for the generation process. We found that in InAs/Si NW TFETs, bulk traps cannot explain the measured weak slope [20]. In GoS InAs/Si NW TFETs, both gate-oxide and material interface traps are expected to contribute to TAT. Fig. 3 illustrates the simulation domain which adapts the geometry of the fabricated device shown in Fig. 1. Appropriate internal region interfaces must be defined to connect the traps with source and drain on a nonlocal mesh which supports the actual tunnel paths. As an example we show in Fig. 4 the different generation contributions that yield the total $I_{\mathrm{D}}V_{\mathrm{GS}}$-curve for the case of gate-oxide interface traps. Note, that the initial branch is solely determined by surface SRH generation! When the electron quasi Fermi level crosses the CB edge, the contribution of surface SRH generation remains constant and the out-tunneling from trap levels into the CB starts to become effective. This provides a" short-cut" to the thermal electron emission step. With increasing gate bias the tunnel probability increases and the most probable transition energy shifts towards the VB edge which finally yields a current comparable to the pure BTBT current.

### B. Channel Quantization

Line tunneling starts when the transistor channel becomes strongly inverted. Under such conditions, the triangular-like

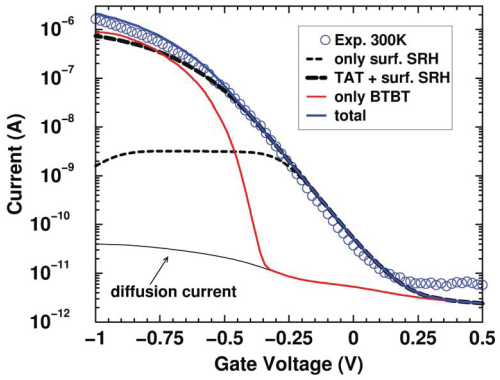



Fig. 4: The different generation contributions to the drain current of the InAs/Si NW p-TFET at 300 K shown in the left part of Fig. 3: only surface SRH generation (short-dashed), TAT included (long-dashed), only BTBT (solid red), total (solid blue). Parameters: $V_{\mathrm{DS}} = 0.5\mathrm{V}$, $DOS_{\mathrm{InAs}} = 3.4 \cdot 10^{17}\,\mathrm{cm}^{-3}$, $WF = 4.8\,\mathrm{eV}$, $\sigma_{\mathrm{n,p}} = 10^{-14}\,\mathrm{cm}^2$, $D_{\mathrm{it}} = 10^{13}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ [14], $V_{\mathrm{trap}} = 10\,\mathrm{Å}^3$, $S\hbar\omega = 120\,\mathrm{meV}$.

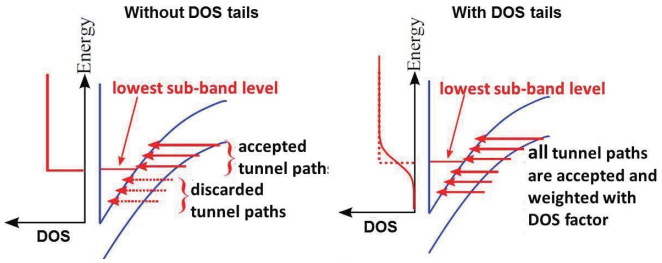



Fig. 5: Modeling the effect of channel quantization without (left) and with 2D DOS tails (right).

potential well of the channel quantizes the electronic states and a 2DEG forms. This shifts the onset voltage of line tunneling to a higher value when compared with the 3DEG case [13]. Besides, the nature of the wave functions changes from Airy functions to "quantized" Airy functions, which modifies the tunnel generation rate. These effects are not covered by the default "dynamic nonlocal path BTBT model" based on Kane's treatment of BTBT [15], available in S-Device [10]. A method to model the quantization effect within a semi-classical framework has been proposed by Vandenberghe et al. [16]: Tunneling paths with energies above the lowest sub-band level are accepted while those with a lower energy are rejected, as illustrated in the left part of Fig. 5. We incorporated such a model in S-Device by developing our own code for the "dynamic non-local path BTBT model" using the PMI for "nonlocal recombination". The implemented algorithm detects a line tunneling path at a proper energy by checking whether the extension of this path intersects the oxide interface. If not, it is not considered to be affected by channel quantization. As an alternative to this rather involved approach, a much simpler method was developed making use of the Quantum Potential Correction (QPC) available in S-Device. In the electrical quantum limit [21] (constant field) the QPC for the splitting of the lowest sub-band is given by

$$E_{\mathrm{QM}} = \begin{cases} \hbar\Theta_c \cdot a_1 - d_{\mathrm{ox}}F & \text{if } E_{\mathrm{QM}} > 0 \\ 0 & \text{otherwise,} \end{cases}$$

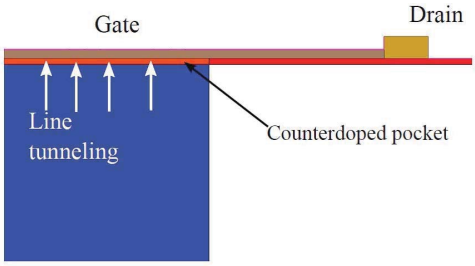



Fig. 6: InGaAs TFET with counter-doped pocket. The special geometry favors line tunneling and is used to analyze the impact of surface roughness on line tunneling.

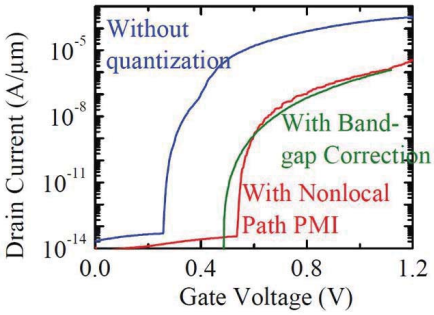



Fig. 7: Comparison between the nonlocal PMI model which employs the path rejection method (red), the PMI model that modifies the band gap (green), and the case without channel quantization (blue).

where $\hbar\Theta_c = (e^2\hbar^2F^2/2m_c)^{1/3}$ and $a_1$ denotes the first zero of the Aity function. The resulting effective CB edge is then computed by $E_{\mathrm{CB}}^{\mathrm{eff}} = E_{\mathrm{CB}} + E_{\mathrm{QM}}$. A special TFET geometry which favors vertical tunneling (see Fig. 6) was simulated to compare both quantization correction methods. The results are plotted in Fig. 7. The good agreement between the two models suggests that the simpler model for quantum correction is as effective as the elaborate model.

### C. Roughness of Gate Oxide Interface

In the absence of surface roughness, the sub-band levels are well defined and the 2D DOS has the well-known staircase form. A rough oxide-semiconductor interface causes random fluctuations of the boundary wall of the triangular-like potential well. As a consequence, the step-like DOS smears out to form tail states as shown in the right part of Fig. 5. A simplified model for 2D DOS tails originating from an arbitrary random field has been derived by Quang et al. [17]. Here, we apply their model to the case of a random potential due to surface roughness. Instead of rejecting the tunnel paths below the lowest sub-band energy, the energy of the tunnel path relative to the ideal sub-band level is determined and the DOS factor is calculated for this relative energy. The spectral tunnel rate from the "dynamic nonlocal path BTBT model" is then multiplied with the 2D DOS to obtain the integrated tunnel rate. This approach has been made available in S-Device by modifying the code for the PMI model of channel quantization. The same "vertical" TFET as shown in Fig. 6 was simulated using the above model. Its transfer characteristics without and with

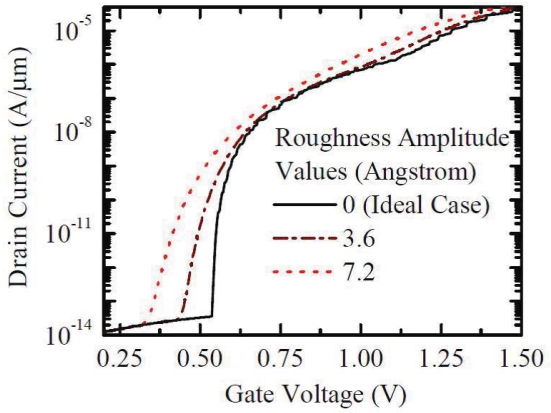



Fig. 8: Effect of the surface roughness amplitude on the transfer characteristics of the TFET in Fig. 6.

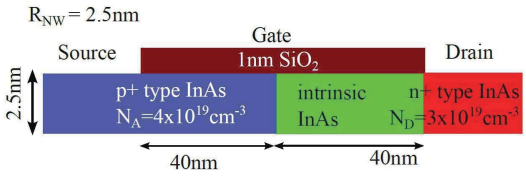



Fig. 9: Device structure to model the effect of DOS tails caused by random dopant fluctuations.

the inclusion of 2D DOS tails due to surface roughness are presented in Fig. 8.

### *D. DOS Tails from Random Dopant Fluctuations*

Kanes model of DOS tails [18] includes the effect of random dopant fluctuations (RDF). Using his tail-state description, we derived a semi-analytical expression of the generation rate to model the effect of RDF-induced DOS tails in the frame of zero-phonon TAT [22]. Tail states are considered as trap states with sufficient localization. Transitions from VB tail states to CB Bloch states and from VB Bloch states to CB tail states are taken into account, whereas transitions between tail states are neglected due to their much smaller tunnel probability. The proximity of the tail states to the band edges allows easy thermal excitation into conducting states which completes the inter-band process. There are two differences to a BTBT transition: (i) the tunnel gap is effectively reduced, (ii) instead of the reduced effective mass the imaginary dispersion is dominated by the respective single-band mass, the mass of the localized state being a fit parameter. The second fit parameter is the characteristic energy of the DOS tail. The model was implemented in S-Device using the PMI for "non-local recombination". To analyze the impact of RDF-induced tail states on TFETs, we simulated a gate-all-around InAs nanowire TFET (see Fig. 9). The transfer characteristics of this device with and without RDF-induced DOS tails are presented in Fig. 10. One observes an earlier onset of tunneling and a degradation of the SS as consequence of the tail states.

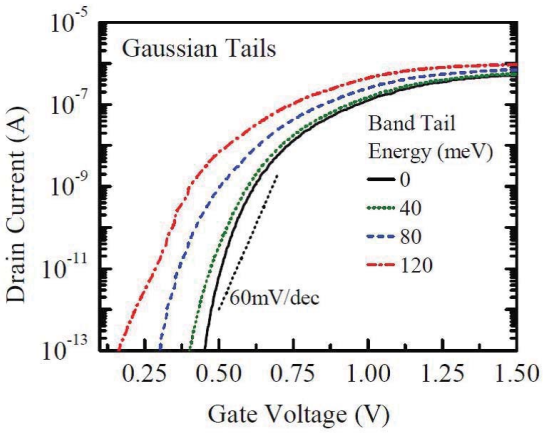



Fig. 10: Effect of RDF-induced DOS tails on the transfer characteristics of the TFET shown in Fig. 9.

## V. Conclusion

Various mechanisms contribute to the degradation of the SS in GoS-TFETs. As main effects we identified (i) the surface SRH generation at the oxide interface in combination with zero-phonon tunneling from trap levels into the CB and (ii) TAT at the material interface with weak phonon assistance. Channel quantization delays the onset of line tunneling which may be hidden if point tunneling dominates, but it also reduces the on-current. Two TCAD solutions to include channel quantization were presented. Furthermore, we developed models for the impact of surface roughness and RDF-induced DOS tails on the SS. Although values of the characteristic energies by which the DOS is smeared out are not known, it seems that both effects could become visible if TAT is suppressed.

## VI. Acknowledgment

Funding from the European Communitys Seventh Framework Programme under Grant Agreement No. 619509 (Project E$^2$SWITCH) is acknowledged.

## References

[1] S. Banerjee et al., IEEE Electron Dev. Lett. **8**, 347 (1987).
[2] A. S. Verhulst et al., IEEE Electron Dev. Lett. **29**, 1398 (2008).
[3] M. T. Björk et al., Appl. Phys. Lett. **80**, 1058 (2002).
[4] M. Borg et al., Nano Letters **14** (4), 1914 (2014).
[5] M. T. Björk et al., Appl. Phys. Lett. **97**, 163501 (2010).
[6] K. Tomioka et al., Appl. Phys. Lett. **98**, 083114 (2011).
[7] K. E. Moselund et al., IEEE Electron Dev. Lett. **33**, 1453 (2012).
[8] H. Riel et al., IEDM Tech. Digest, pp. 391-394, 2012.
[9] D. Cutaia et al., IEEE Journal of the Electron Dev. Soc. **3** (3), 176 (2015).
[10] Sentaurus-Device User Guide, version 2015.06, Synopsys Inc., Mountain View, California (2015).
[11] H. Carrillo-Nuñez et al., Solid-State Electronics **113**, 61 (2015).
[12] K. E. Moselund et al., J. Appl. Phys. **113**, 184507 (2013).
[13] W. G. Vandenberghe et al., Appl. Phy. Lett. **98**, 143503 (2011).
[14] P. Mensch et al., IEEE Trans. Nanotechnol. **12** 3, 279 (2013).
[15] E. O. Kane, J. Phys. Chem. Solids **12**, 181 (1959).
[16] W. G. Vandenberghe et al., Proc. SISPAD, 271 (2011).
[17] D. N. Quang et al., phys. stat. sol. (b) **207**, 111 (1998).
[18] E. O. Kane, Phys. Rev. **131**, 79 (1963).
[19] S. Sant et al., Trans. Electr. Dev., DOI: 10.1109/TED.2015.2489844.
[20] A. Schenk et al., Proc. DRC, 201 (2012).
[21] T. Ando, A. B. Fowler, and F. Stern, Rev. Mod. Phys. **54**, 437 (1982).
[22] A. Schenk, J. Appl. Phys. **71** (7), 3339 (1992).

# Intrinsic voltage gain of Line-TFETs and comparison with other TFET and MOSFET architectures

P. G. D. Agopian, J. A. Martino
LSI/PSI/USP
University of Sao Paulo
Sao Paulo, Brazil
agopian@lsi.usp.br

R. Rooyackers, A. Vandooren, E. Simoen, A. Thean and C. Claeys
Imec
E.E. Dept., KU Leuven
Leuven, Belgium

***Abstract*— In this work the intrinsic voltage gain (AV) is for the first time experimentally analyzed for a planar Line-TFETs and its performance is compared with different MOSFET and point TFET architectures (FinFET and GAA:Gate-All-Around) at both room and high temperatures. The Line-TFET shows a much better intrinsic voltage gain than all studied MOSFET devices (FinFET and GAA). However, when it is compared to other TFET structures, Line-TFETs show a worse AV. Besides the AV, a higher on-state current was obtained for Line-TFETs, which leads to a good compromise for analog application.**

***Keywords: Line-TFET; Intrinsic Voltage Gain; different device architectures***

## I. INTRODUCTION

Tunnel-FETs have drawn the attention of the international community, as an alternative for MOSFETs, when focusing on extremely small technology nodes, due to their high speed switching capability [1]. Several works report the research on different materials and different geometries aiming to reach the smaller subthreshold swing. However, some recent work has also pointed out the great potential of these devices for analog applications [2-4].

In this work the planar heterojunction Line-nTFET is analyzed experimentally through the basic analog parameters, focusing mainly on intrinsic voltage gain. The intrinsic voltage gain of this Line-TFET is also compared with devices with different architectures like FinFET (MOSFET and TFET transistors) [2] and Gate-all-around (MOSFET and TFET) [5], for temperatures ranging from room temperature up to 150ºC. For the latest case, the intrinsic voltage gain of a GAA-TFETs with different source compositions were also compared with line-TFET one.

## II. DEVICE CHARACTERISTICS

The Si/SiGe heterojunction Line-nTFET devices were fabricated on (100) 300-mm silicon-on-insulator wafers in imec/Belgium. The highly boron doped ($1x10^{20}$ $cm^{-3}$) $Si_{0.55}Ge_{0.45}$ source extends under the gate and is capped with a thin intrinsic silicon pocket layer (~5nm). The source and the drain regions are separated by a nominally undoped Si channel.

The gate stack is composed by a 1nm interfacial $SiO_2$ layer followed by 1.8nm of $HfO_2$, 2nm of TiN and p-doped amorphous silicon. The channel width (W) ranges from 110nm to 200nm and two different gate lengths were evaluated (1µm and 130nm).

Figure 1 presents a schematic structure of a Line-TFET and more details on this structure/fabrication can be found in [6].

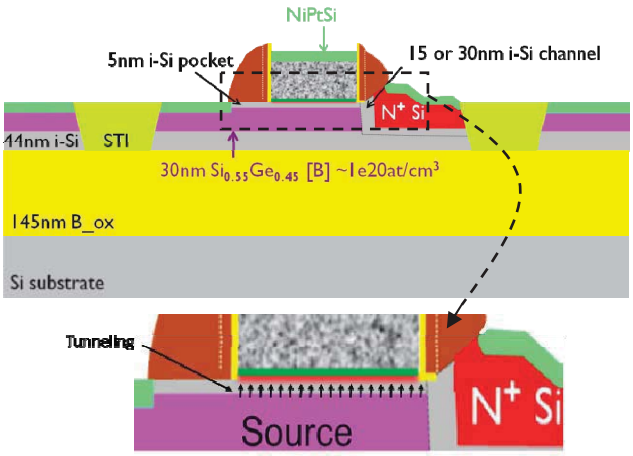



**Fig. 1** – Line-TFET structure.

## III. EXPERIMENTAL RESULTS AND DISCUSSION

In Line-TFETs the source extends under the gate region increasing the tunneling junction area where tunneling occurs in the same gate electric field direction because the gate does not overlap the channel region (intrinsic region between source and drain) avoiding point tunneling. This architecture results in a high on-state current (Figure 2). It is also possible to observe from the transfer characteristics that the smaller the drain bias ($V_{DS}$) the steeper is the drain current ($I_{DS}$) in the subthreshold region. The SS improvement becomes even more pronounced with increasing gate length and consequently the tunneling area as reported in [6]. However, evaluating the $I_{DS}$ as a function of $V_{DS}$ (figure 3), it is clear that at low gate bias the output characteristic is degraded and becomes inappropriate for analog applications.

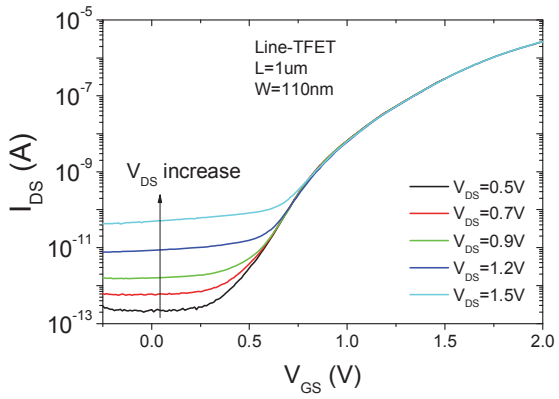



**Fig. 2** – Experimental transfer curves of a Line-TFET for different drain bias.

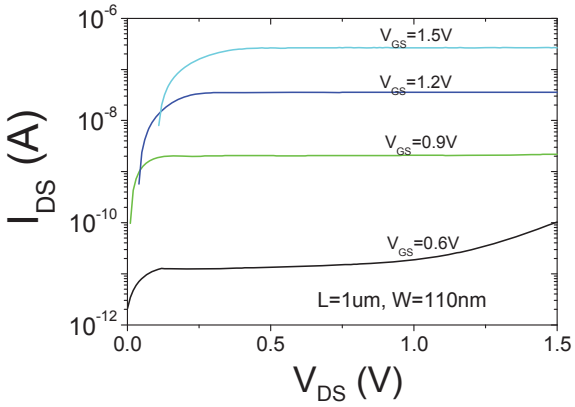



**Fig. 3** – Experimental output characteristic of a Line-TFET for different gate bias.

Considering that the intrinsic voltage gain ($A_V$) is an important figure of merit for analog analysis of the transistors, the transconductance (gm) and output conductance ($g_D$) were evaluated for different bias, channel lengths and channel widths, aiming to optimize the Line-TFET $A_V$ performance.

Besides that the gm increases with $V_{GS}$ (due to the higher overlap between bands), the Line-TFETs present a larger tunneling current and also a higher gm for longer channel length due to the larger tunneling junction area underneath the gate as shown in figure 4 (source / Si pocket). Evaluating the $g_D$ parameters (figure 5), a smaller gate length dependence is observed but a high dependency on drain bias and for high $V_{DS}$ the TFET devices operate more in the "saturation like" region, resulting in a better $g_D$.

The $g_D$ and gm parameters were also evaluated for different channel widths (W) at high $V_{GS}$ (1.5V) as a function of drain bias (figure 6). Although the drain bias does almost not affect the transconductance, gm increases with the channel width as expected. On the other hand, the output conductance ($g_D$) depends on both the drain bias and the channel width. While the channel width increases, the drain current also increases which degrades the output conductance. The higher drain bias contributes to the $g_D$ improvement as previously observed (the TFET operates more in "saturation like" region).

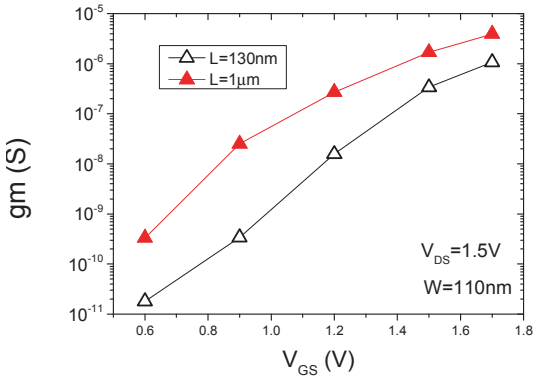



**Fig. 4** – Transconductance as a function of gate bias for different channel lengths

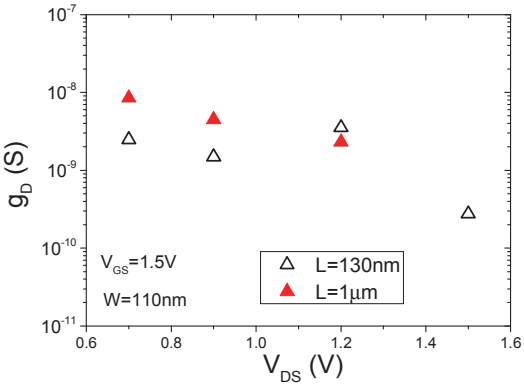



**Fig. 5** – $g_D$ as a function of drain bias for different channel lengths.

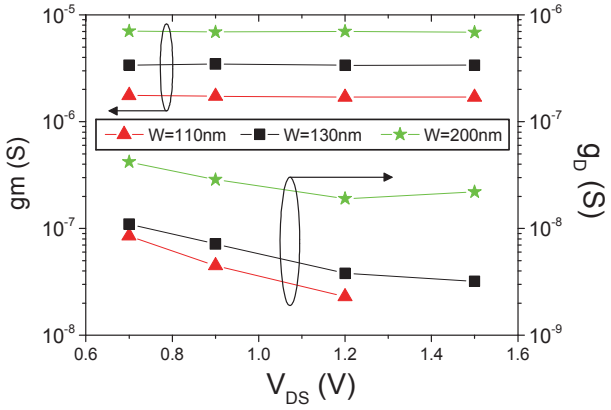



**Fig. 6** – gm and gD as a function of drain bias for different channel widths.

Since the $A_V$ corresponds to the gm over $g_D$ ratio, the output characteristic improvement associated with a $V_{DS}$ increase leads to an optimization of the bias operation point for the analog performance of Line-TFETs. Although the dispersion of the $A_V$ values among different channel widths and lengths is not that high, the best $A_V$ values were obtained for the device with W=130nm and L=1µm in the studied temperature range (figure 7). Taking this device as a reference,

a comparison of this planar Line-TFET among different devices (MOS and TFET) architectures (FinFET and GAA) was performed.

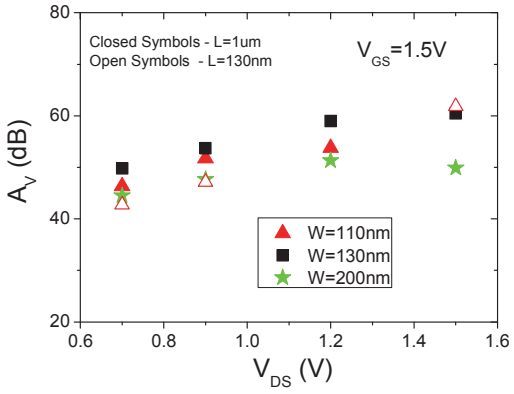



**Fig. 7** – $A_V$ behavior as a function of VDS for Line-TFETs with different channel widths and lengths.

The first comparison, shown in figure 8, is focused on the $A_V$ performance among the planar Line-TFET and transistors fabricated with the FinFET structure (tunnel-FET and MOSFET) for temperatures ranging from 25ºC to 150ºC. From this comparison it is possible to see that although the Line-TFETs $A_V$ is smaller than the one obtained for the TFET with the FinFET structure, a Line-TFET presents an improvement of at least 30 dB when compared with the conventional FinFET (MOSFET technology), for the temperature range considered.

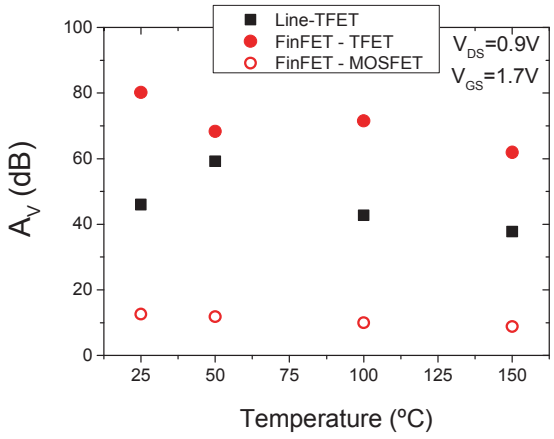



**Fig. 8** – Experimental comparison of AV as a function of temperature among Line-TFET, FinFET-TFET and FinFET MOSFET.

The same comparison was performed considering Line-TFETs and vertical GAA structures (TFETs with different source compositions and Si-MOSFETs) as can be seen in figure 9. Independent of the source composition, the GAA-TFETs present higher $A_V$ values than the Line TFETs. However when the Line-TFET is compared with a GAA MOSFET, the Line TFET seems to be better again.

Although Line-TFETs do not reach $A_V$ values as high as for GAA-TFETs and Fin-TFETs, when a high on-state current is required, planar Line-TFETs can be considered as an alternative, since it reaches on-state currents much higher than the other TFET structures studied in this paper.

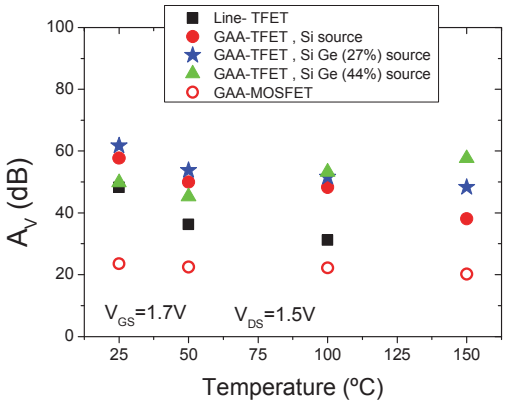



**Fig. 9** – Experimental comparison of $A_V$ as a function of temperature among Line-TFET, GAA-TFET (with different source compositions) and GAA-MOSFET.

## IV. Conclusions

This paper presents for the first time the intrinsic voltage gain of Line-TFETs and shows that although this planar TFET architecture does not present the highest $A_V$ values when compared with the two other vertical TFET architectures (FinFET-TFET and GAA-TFET), the Line-TFET can be a good alternative to replace MOSFETs since it reaches high on-state currents and a better intrinsic voltage gain than the advanced MOSFET architectures (at least 30dB higher than FinFETs and 10dB higher when compared with GAA-MOSFETs).

## Acknowledgment

The authors would like to thank CNPq, FWO and FAPESP for the financial support during the execution of this work and the support from the imec's Logic Device Program and its Core Partners.

## References

[1] A. M. Ionescu and H. Riel, Nature, vol.479, pp.329 – 337, 2011.
[2] P. G. D. Agopian, et al., IEEE Trans. Electron Devices, vol.60, pp.2493-2497, 2013
[3] P. G. D. Agopian, et al., IEEE Trans. Electron Devices, vol.62, pp.16-22, 2015
[4] Q.-T. Zhao, et al., J. Electron Device Society, vol.3, no.3, pp. 103-114, 2015.
[5] P. G. D. Agopian, et al., EuroSOI-ULIS, pp.233-236, 2015
[6] A. M. Walke, et al., IEEE Trans. Electron Devices, vol.61, no. 3, pp. 707- 715, 2014.

# Optimization of GaSb/InAs TFET exploiting different strain configurations

M. Visciarelli, E. Gnani, A. Gnudi, S. Reggiani, G. Baccarani
ARCES and DEI - University of Bologna, Viale Risorgimento 2, 40136 Bologna, Italy
Email: michele.visciarelli2@unibo.it

***Abstract*—A simulation study exploring the possibility of performance improvements related with the application of stress to nanowire TFETs is carried out. It is demonstrated that appropriate strain conditions, i.e., biaxial tensile strain, induce a remarkable enhancement of the on-state current thanks to bandgap reduction. However, a careful optimization of the device cross-section and strain level must be carried out in order to preserve the device subthreshold swing.**

***Index Terms*—Full-quantum simulation, Tunnel Field-Fffect Transistor (TFET), Strain configurations**

## I. Introduction

Tunnel FETs are one of the most promising device architectures which could possibly overcome the fundamental MOSFETs limit of the inverse subthreshold slope SS $\geq$ 60 mV/dec. A steeper SS is in fact an essential prerequisite for an aggressive supply-voltage scaling below 0.5 V in CMOS technology [1], [2], [3]. This device architecture, however, is still affected by a number of drawbacks as yet unsolved: 1) achieving a higher on-state current $I_{\mathrm{ON}}$; 2) suppressing ambipolar effects, and, 3) dealing with the superlinear onset and high saturation voltage of the output characteristics [4].
There is wide consensus on the use of heterostructures with staggered or broken-gap lineups to boost the TFET on-state current. [5], whereas a careful optimization of the device geometry, doping levels, and gate-stack is required to improve the device performance. Process-induced strain is normally used in Si-based CMOS devices to boost circuit-speed, and to maintain the historical CMOS performance trend over different technology generations. This is due to the stress capability to increase the average carrier mobility and the injection velocity into the channel [6]. Recently, it has been asserted that a substantial performance improvement of homojunction InAs nanowire (NW) TFETs can be achieved by using appropriate stress conditions [7], [8], [9]. However, identifying stress conditions able to reduce the bandgap and the imaginary wave vector in the energy gap without appreciably degrading the off-state current, is a challenging task due to the ambipolarity effect related with channel-drain band lineup.

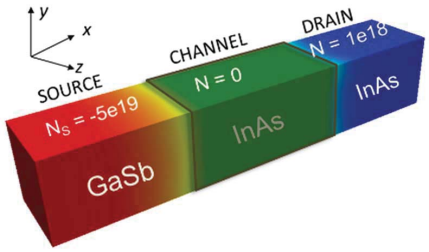



Fig. 1. Schematic view of the device under investigation.

## II. Effect of strain

Simulations have been performed for a GaSb/InAs heterojunction TFET, that has been the subject of a wide investigation in the last few years [5]. A schematic view of the device is shown in Fig. 1. The first investigated TFET has a square cross section with $T_{side} = 5$ nm, $L_{source} = 20$ nm, $L_{gate} = 17$ nm and $L_{drain} = 40$ nm, p-type source doping $N_S = 5 \times 10^{19}$ cm$^{-3}$, n-type drain doping $N_D = 10^{18}$ cm$^{-3}$, EOT = 1nm, and is similar to the TFET presented in [5]. The drain doping has been reduced to limit ambipolar effects related with channel-drain band lineup. Therefore, a longer drain region is necessary to ensure charge neutrality at the drain contact. The nanowire transport orientation is [100]; however, it has been shown that the real, as well as the main imaginary branches of the energy dispersion relation, are very similar for the [100], [110], and [111] orientations [7].
The in-house simulator employed for the present investigation is based on an 8-band $\mathbf{k} \cdot \mathbf{p}$ Hamiltonian [5], to accurately model multiband effects and the complex band structure of our devices. All calculations are carried out in a full 3-D framework, which properly accounts for anisotropic effects and different strain conditions. The Hamiltonian has been properly extended to take into account strain effects via the Pikus-Bir formalism. Under arbitrary stress conditions, the periodicity of the crystal is destroyed, and Bloch's theorem is no longer valid. However, the crystal periodicity can be restored by a transformation from an unstrained coordinate system $x$ to

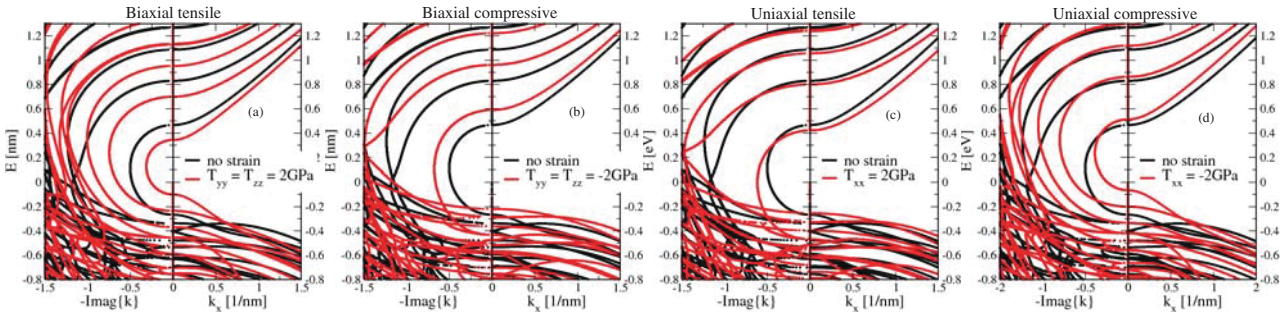



Fig. 2. Energy dispersion for the $5 \times 5\,\text{nm}^2$ InAs nanowire: (a) biaxial tensile $T_{yy} = T_{zz} = 2\,\text{GPa}$; (b) biaxial compressive $T_{yy} = T_{zz} = -2\,\text{GPa}$; (c) uniaxial tensile $T_{xx} = 2\,\text{GPa}$; (d) uniaxial compressive $T_{xx} = -2\,\text{GPa}$. Biaxial tensile strain shifts up the valence band and lowers the conduction band, giving the largest gap reduction among all cases. For the uniaxial tensile and biaxial compressive strain, the imaginary wave vector does not connect the lowest conduction subband with the highest valence subband, but with a valence subband at $\approx 0.2\,\text{eV}$ below the highest one.

TABLE I

ENERGY BANDGAPS AND ELECTRON (HOLE) EFFECTIVE MASS OF THE FIRST CONDUCTION (VALENCE) SUBBAND BOTH FOR A $5\times5$ NM$^2$ INAS AND GASB NW FOR THE UNSTRAINED, BIAXIAL COMPRESSIVE AND TENSILE STRESS CONDITIONS IN THE CROSS SECTION, AND UNIAXIAL COMPRESSIVE AND TENSILE STRESS CONDITIONS ALONG THE TRANSPORT DIRECTION. THE EFFECTIVE MASS VALUES ARE EVALUATED FROM THE REAL BRANCH OF $E(k)$.

| $5\times5$ nm$^2$ InAs NW - stress = 2 GPa | | | | | |
|---|---|---|---|---|---|
| | Unstrained | Biaxial tens. | Biaxial comp. | Uniaxial tens. | Uniaxial comp. |
| $E_G$ [eV] | 0.733 | 0.437 ($-40\%$) | 0.806 (+10%) | 0.676 ($-8\%$) | 0.564 ($-23\%$) |
| $m_e$ [$m_0$] | 0.057 | 0.036 ($-37\%$) | 0.077 (+35%) | 0.072 (+26%) | 0.043 ($-24.5\%$) |
| $m_h$ [$m_0$] | 0.057 | 0.033 ($-42\%$) | 0.33 (+48%) | 0.33 (+48%) | 0.039 ($-31\%$) |
| $5\times5$ nm$^2$ GaSb NW - stress = 2 GPa | | | | | |
| | Unstrained | Biaxial tens. | Biaxial comp. | Uniaxial tens. | Uniaxial comp. |
| $E_G$ [eV] | 1.273 | 0.94 ($-26\%$) | 1.69 (+32%) | 1.17 ($-8\%$) | 1.084 ($-15\%$) |
| $m_e$ [$m_0$] | 0.068 | 0.05 ($-26\%$) | 0.084 (+23.5%) | 0.079 (+16%) | 0.058 ($-14.7\%$) |
| $m_h$ [$m_0$] | 0.13 | 0.07 ($-46\%$) | 0.256 (+97%) | 0.256 (+97%) | 0.08 ($-38\%$) |

a deformed coordinate system $x'$. The effect of this transformation is a Hamiltonian $H$ where a strain-dependent matrix $H_{strain}$ is directly added to the usual $\mathbf{k} \cdot \mathbf{p}$ matrix [10]. Spurious solutions are eliminated using the procedure proposed in [11]. Material parameters are taken from [12] and bowing effects are included. All simulations are carried out at $V_{\text{DD}} = 0.3\,\text{V}$.

The energy dispersion relationship of the InAs square well with $T_{side} = 5$ nm is shown in Fig. 2 for the unstrained and strained conditions: biaxial tensile ($T_{yy} = T_{zz} = 2\,\text{GPa}$), biaxial compressive ($T_{yy} = T_{zz} = -2\,\text{GPa}$), uniaxial compressive ($T_{xx} = -2\,\text{GPa}$), uniaxial tensile ($T_{xx} = 2\,\text{GPa}$). Both biaxial tensile and uniaxial compressive stress shift up the valence band, but biaxial stress also lowers the conduction band and, thus, obtains the largest reduction of the energy gap and of the imaginary wave-vector in the gap. A similar trend is obtained for GaSb (not shown). Table I reports the energy bandgap and electron (hole) effective masses of the first conduction (valence) subband, for both InAs and GaSb, and for the unstrained, biaxial compressive and tensile stress conditions in the cross section, and uniaxial compressive and tensile stress conditions along the transport direction. Note that the InAs band structure seems to be more sensitive to stress than GaSb.

Another important aspect is that the alignment between the source valence and channel conduction bands at the heterojunction ($\Delta E_C$) is affected by strain. This parameter is strictly related with the tunnelling probability at the source/channel junction and, thus, to the device on-state current. For $T_{side} = 5$ nm, $\Delta E_C$ decreases from 0.24 eV for the unstrained case to 0.02 eV (90%) and 0.163 eV (32%) for the biaxial tensile and uniaxial compressive stresses, respectively.

Fig. 3 compares the I-V curves of a $5 \times 5\,\text{nm}^2$ GaSb/InAs heterojunction NW TFET for different stress conditions. The biaxial tensile stress reduces the threshold voltage $V_T$ and increases the on-state current, while the uniaxial compressive stress has a smaller impact on the I-V curve. Biaxial tensile stress provides a better on-state current, but also a degradation of subthreshold slope. This is due to an increased source degeneracy caused by the reduced hole

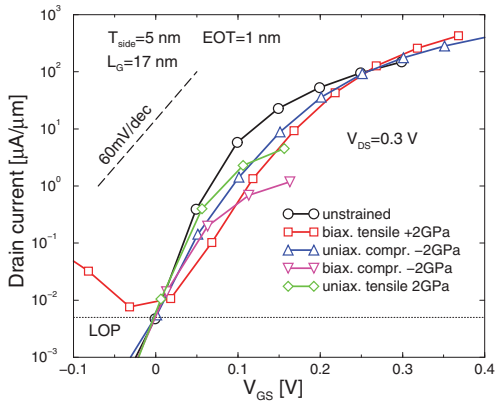



Fig. 3. Turn-on characteristics of a 5×5 nm$^2$ GaSb/InAs NW TFET for different stress conditions. The current is normalized by device side and the curves are shifted to match the $I_{OFF}$ target of the LOP application (5 nA/$\mu$m). $V_{DS}$ = 0.3 V. The biaxial tensile stress increases the on-state current, whereas the uniaxial compressive stress has a smaller impact on the I-V curve.

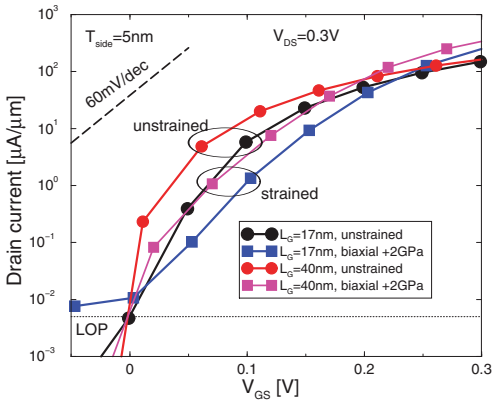



Fig. 4. Turn-on characteristics of a 5×5 nm$^2$ GaSb/InAs NW TFET for $L_G$ = 17 and 40 nm, under unstrained and biaxial strained conditions. The current is normalized to the cross-section side and the curves are shifted to match the $I_{OFF}$ target of the LOP application (5 nA/$\mu$m). $V_{DS}$ = 0.3 V. The $L_G$ increase from 17 to 40 nm provides a decrease of the leakage current, a slope improvement and a higher on-state current. For the biaxial tensile stress condition, a 37% increase of $I_{ON}$ at $V_{GS}$ = $V_{DD}$, $V_{DS}$ = $V_{DD}$ can be achieved.

effective mass (see Table I), as also demonstrated in [13]. Furthermore, band-to-band tunneling (BTBT) increases at the drain side, because of the smaller bandgap. Anyway, among all possible strain configurations, the biaxial tensile and the uniaxial compressive ones provide the best tradeoff between $I_{ON}$ and SS. Hence, the investigation has been focused on these two types of stress.

## III. Device Optimization

A careful optimization of the applied strain level and of the device geometry (i.e., cross-section size and channel length) must be carried out to optimize the device performance. For example, the effect of the channel length is shown in Fig. 4. The increase of $L_G$ from 17 nm to 40 nm provides a decrease of the leakage current, a slope improvement and a higher on-state current, mainly due to the biaxial tensile stress condition, where a $+37\%$ in $I_{ON}$ can be achieved at $V_{GS} = V_{DD}$ and $V_{DS} = V_{DD}$. However, the on-state current is still relatively low, at 0.34 mA/$\mu$m. One of the most straightforward approaches to improve $I_{ON}$ is the increase of the cross-section size. This size affects the device bandgap and the electron and hole effective masses. Increasing the device cross section from a $5 \times 5\,\text{nm}^2$ to a $10 \times 10\,\text{nm}^2$ affects the band offset $\Delta E_C$, which becomes 0.048 eV (80% of the $5 \times 5\,\text{nm}^2$ device) for the unstrained case and 0.093 eV and 0.025 eV for a biaxial tensile and uniaxial compressive stresses of 1 GPa, respectively. Note that a negative $\Delta E_C$ means a broken-gap heterojunction instead of a staggered one. The turn-on curves of the $10 \times 10\,\text{nm}^2$ GaSb/InAs heterojunction TFET are shown in Fig. 5 for different stress conditions, together with the unstressed $5 \times 5\,\text{nm}^2$ I-V curve with $L_G = 40$ nm for comparison. For the unstressed case an

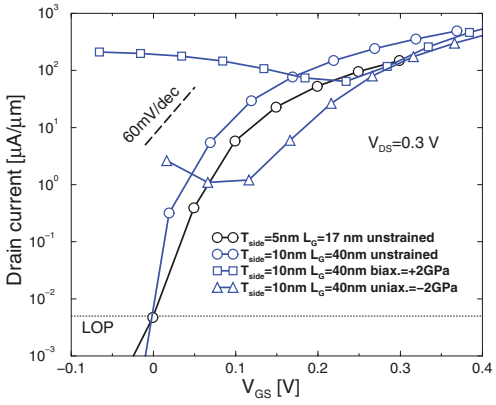



Fig. 5. Comparison of the turn-on curves of a $10 \times 10\,\text{nm}^2$ GaSb/InAs NW TFET for different stress conditions (2GPa). The current is normalized to the cross section side and the curves are shifted to match the $I_{OFF}$ target of the LOP application (5 nA/$\mu$m). $V_{DS}$ = 0.3 V. The I-V curve of the unstrained $5 \times 5\,\text{nm}^2$ TFET is shown for comparison.

$I_{ON}$ improvement of 160% is achieved at $V_{DD}$ = 0.3 V with respect to the smaller device. However, ambipolarity causes an unacceptable performance degradation when both stress conditions are applied. The $10 \times 10\,\text{nm}^2$ nanowire bandgap is about half that of the $5 \times 5\,\text{nm}^2$ nanowire, and 1/3 for a 2 GPa strain (0.2-0.3 eV). As demonstrated in [13], the occurrence of the ambipolar effect is prevented if the following condition is fulfilled: $qV_{DD} < E_G - (E_{vs} - E_{FS}) - (E_{FD} - E_{cd})$ with $E_{vs}$ the valence band in the source, $E_{cd}$ the conduction band in the drain, and $E_{FS}$ and $E_{FD}$ the source and drain Fermi levels, respectively. Hence, for zero source and drain degeneracy, a supply voltage lower than the bandgap should in principle

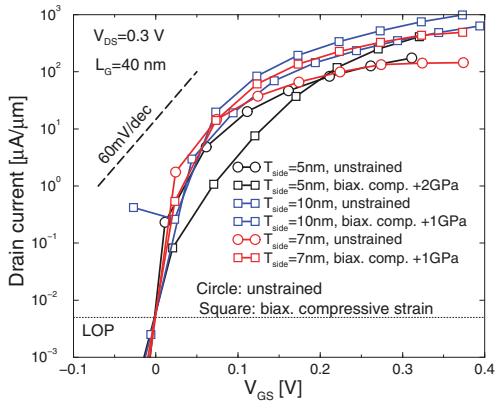



Fig. 6. Turn-on curves of a $5 \times 5, 7 \times 7$ and $10 \times 10\,\mathrm{nm}^2$ GaSb/InAs NW TFET for different stress conditions. $L_G = 40\,\mathrm{nm}$, $V_{\mathrm{DD}} = 0.3\,\mathrm{V}$. $I_{\mathrm{OFF}} = 5 \times 10^{-9}\,\mathrm{A}/\mu\mathrm{m}$ (LOP).

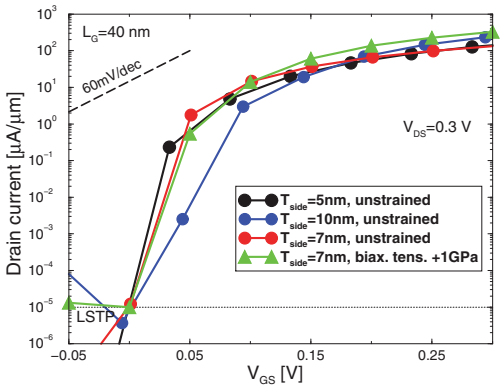



Fig. 7. Turn-on curves of a $5 \times 5, 7 \times 7$ and $10 \times 10\,\mathrm{nm}^2$ GaSb/InAs NW TFET for different stress conditions. The currents are normalized to the cross section side and are shifted to match the $I_{\mathrm{OFF}}$ target of the LSTP application (10pA/$\mu$m). For $\mathrm{V_{DS}}$ = 0.3V the largest ON-curret is achieved with $\mathrm{T}_{side}$ = 7 nm, $\mathrm{L}_G$ = 40 nm and applying a biaxial tensile stress of 1 GPa.

be applied to prevent ambipolarity. The above condition becomes more restrictive if source and drain are degenerate. Therefore, a moderate strain must be applied (1 GPa instead of 2 GPa) and an optimization of the drain region is required. In order to take advantage from the on-state current increase provided by the biaxial stress condition, with a moderate degradation of the subthreshold swing, a $7 \times 7\,\mathrm{nm}^2$ device has been simulated as well. Fig. 6 shows the turn-on curves of the investigated devices, namely the $5 \times 5, 7 \times 7$ and $10 \times 10\,\mathrm{nm}^2$ NW TFETs. The device able to fulfill the $I_{\mathrm{OFF}}$ requirement and to provide the best on-state current is the $7 \times 7\,\mathrm{nm}^2$ with a biaxial tensile strain of 1 GPa, that features $I_{\mathrm{ON}} = 0.4$ mA/$\mu$m. The subthreshold slope is also slightly better that that of the unstrained $10 \times 10\,\mathrm{nm}^2$ device. Furthermore, the $7 \times 7\,\mathrm{nm}^2$ TFET with a biaxial tensile strain of 1 GPa provides the best performance even if we target the $I_{\mathrm{OFF}}$ value for the LSTP application (see Fig. 7).

## IV. Conclusions

A simulation study exploring the possibility of TFET performance improvements under the application of appropriate stress conditions has been carried out. For this purpose, the in-house developed simulator based on an 8-band $\mathbf{k} \cdot \mathbf{p}$ Hamiltonian has been properly extended to take into account the effects of strain via the use of Pikus-Bir formalism. It is demonstrated that biaxial tensile strain induces a remarkable $I_{\mathrm{ON}}$ enhancement thanks to the bandgap reduction. However, taking advantage of stress requires a very tight control of the fabrication processes, i.e. device cross section and length, as well as strain condition and intensity.

## Acknowledgment

This work has been supported by the EU Grant No. 619509 (E2Switch).

## References

[1] A. Seabaugh and Q. Zhang, "Low-voltage tunnel transistor for beyond CMOS logic". *Proc. IEEE*, vol. 98, no. 12, pp. 2095-2110, Dec. 2010

[2] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches". *Nature*, vol. 479, no. 7373, pp. 329-337, Nov. 2011

[3] H. Lu and A. Seabaugh, "Tunnel field-effect transistors: state-of-the-art". *J. Electron Device Soc.*, vol. 2, no. 4, Jul. 2014

[4] E. Gnani, A. Gnudi, S. Reggiani and G. Baccarani, "Drain-conductance optimization in nanowire TFETs by means of a physics-based analytical model". *Solid State Electronics*, vol. 84, pp. 96-102, Mar. 2013

[5] E. Baravelli, E. Gnani, R. Grassi, A. Gnudi, S. Reggiani and G. Baccarani, "Optimization of n- and p-type TFETs integrated on the same InAs/AlxGa1-xSb technology platform". *IEEE Trans. Electron Devices*, vol. 61, no. 1, pp. 178-184, Jan. 2014

[6] O. Penzin, L. Smith, A. Erlebach, and K. -H. Lee, "Layer thickness and stress-dependent correction for InGaAs low-field mobility in TCAD applications". *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 493-500, Feb. 2015

[7] F. Conzatti, M. G. Pala, D. Esseni, E. Bano and L. Selmi, "Strain-induced performance improvements in InAs nanowire tunnel FETs". *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2085-2092, Aug. 2012

[8] F. Conzatti, M. G. Pala, D. Esseni, and E. Bano, "Investigation of localized versus uniform strain as a performance booster in InAs tunnel-FETs". *Solid State Electronics*, vol. 88, pp. 49-53, Aug. 2013

[9] F. Conzatti, M. G. Pala, D. Esseni, E. Bano, and L. Selmi, "A simulation study of strain induced performance enhancements in InAs nanowire Tunnel-FETs", *IEEE International Electron Devices Meeting*, p. 5.2.1, 2011.

[10] T. Bahder, "Eight-band k*p model of strained zinc-blende crystals". *Phys. Rev. B*, vol. 41, no. 17, pp. 11992-12001, Feb. 1990

[11] B. A. Foreman, "Elimination of spurious solutions from eight-band kp theory". *Phys. Rev. B*, vol. 56, pp. R12748-R12751, Jul. 2001

[12] I. Vurgaftman and J. R. Meyer, *Band parameters for IIIV compound semiconductors and their alloys*, J. Appl. Phys., vol. 89, no. 11, pp. 58155875, 2001.

[13] E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, "Drain-conductance optimization in nanowire TFETs by means of a physics-based analytical model", *Solid-State Electronics*, v. 84, p. 96-102, 2013.

# Assessment of Confinement–Induced Band–to–Band Tunneling Leakage in the FinEHBTFET

J.L. Padilla*†, C. Alper*, F. Gámiz† and A.M. Ionescu*
*Nanoelectronic Devices Laboratory
École Polytechnique Fédérale de Lausanne, Lausanne CH-1015, Switzerland
Email: jose.padilladelatorre@epfl.ch
†Departamento de Electrónica y Tecnología de los Computadores
Universidad de Granada. Avda. Fuentenueva s/n, 18071 Granada, Spain

***Abstract*—In conventional planar EHBTFETs, the interband tunneling phenomena responsible for the drive current takes place vertically in the section of the channel where top and bottom gates overlap. As a result, the horizontal extent of this overlapping between gates is the limiting factor for both the available band–to–band tunneling area and the occupied wafer space. Hence, any design seeking to increase the horizontal size of the device for boosting the ON current levels would not allow for a restrained surface occupation. In contrast with this, the FinEHBTFET is a very promising structure in terms of scalability due to the decoupling between the tunneling area and the required space in the wafer. However, harmful quantum mechanical confinement effects, such as the appearance of parasitic tunneling leakage contributions, need to be assessed in this type of devices in order to quantify their importance and minimize their impact on the device performance.**

## I. Introduction

Due to the band–to–band tunneling (BTBT) mechanisms responsible for the operation of tunnel field–effect transistors (TFETs), these devices are immune to the subthreshold swing limitation of 60mV/dec entailed by thermionic emission processes [1]. This situation has led to regard TFETs as excellent candidates [2] to become steep slope switches with enormous scalability potential. As a result, great amount of research has been devoted to them in terms of simulation, modeling and, more recently, fabrication [3]–[6]

The demonstration of higher performance for those TFETs featuring BTBT paths aligned with the gate induced electric field [4], [7], [8], and for those configurations exploiting dimensionality through tunneling between 2-D electron and hole gases [9], [10], led to propose the planar Electron–Hole Bilayer TFET (EHBTFET) as a very appealing solution for very low power operation [11]. Nevertheless, field–induced quantum confinement effects caused the appearance of parasitic tunneling leakage currents [10], [12]. For suppressing these deleterious tunneling contributions, a heterogate structure (HG–EHBTFET) with different gate materials was introduced [12] with potential fabrication feasibility through the use of electron beam, selective/angle ion implantation, or precise lithographic alignment.

The discretization of conduction and valence bands into differentiated energy levels resulting from confinement [13] demonstrated to entail an important degradation of ON-current levels not only in conventional TFETs [13], [14], but also in bilayer TFETs [15]. The use of asymmetric configurations in both top and bottom gates was proposed [16] to bypass this limitation by the arrangement of pseudobilayer structures inside the channel [17] that could, as an extra advantage, mitigate the so-far expected technological difficulties derived from confining very high concentrations of opposite carriers in ultrathin layers [3], [18].

As the drive current in the HG–EHBTFET is due to vertical BTBT in the central part of the channel where top and bottom gates overlap [12], the device performance would be degraded when scaled down. This setback can be avoided by modifying the conception of the device and inserting a narrow gated fin on top of a $\mathrm{n}^+ - \mathrm{i} - \mathrm{p}^+$ diode. This solution [19] allowed, in principle, to increase the tunneling surface without impacting the required wafer area and preserving the device density. However, semiclassical simulations [19] did not capture neither the deleterious impact from subband discretization, nor the appearance of parasitic lateral tunneling paths similar to those reported in planar EHBTFETs. In this paper, we assess the nature of the tunneling leakage contributions arising in the germanium FinEHBTFET and suggest possible solutions to get rid of them.

## II. Device Structure

The FinEHBTFET under study is depicted in Fig. 1 with a germanium source $\mathrm{p}^+$ region ($10^{20}$ atoms/cm$^3$); an intrinsic channel region ($10^{15}$ atoms/cm$^3$) with a central gate-sandwiched fin, plus two lateral side underlaps; and a drain $\mathrm{n}^+$ region ($10^{20}$ atoms/cm$^3$). The body thickness, $t_{\mathrm{body}}$, and the fin thickness, $t_{\mathrm{fin}}$, are chosen to be 10nm. Front and back gate dielectrics are 3nm-thick $HfO_2$ layers. Workfunctions will be engineered for every polarization considered in this work so that alignment between first conduction and valence subbands inside the fin takes place at very low front gate voltage, $V_{\mathrm{FG}}$. Namely, we select $V_{\mathrm{FG,align}} = 0.04$V. Back gate voltage, $V_{\mathrm{BG}}$, will be initially set to 0V without generality loss and $V_{\mathrm{DS}}$ will be fixed to $V_{\mathrm{DD}} = 0.3$V throughout this paper. A heterogate solution has been included at the front gate in order to avoid parasitic lateral tunneling from the overlap region to the front gate underlap. The nature of this lateral tunneling would be analogous to that reported for the EHBTFET [12],

ISBN 978-1-4673-8608-1  IEEE Catalog number CFP1649D-USB

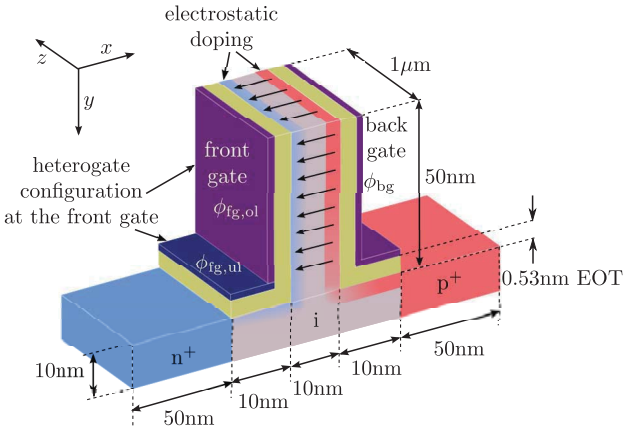



Fig. 1. Schematic representation (not to scale) of the FinEHBTFET considered in this work. The gated fin is inserted over the intrinsic region of a $n^+ - i - p^+$ diode. This setup decouples the occupied wafer area from the BTBT area responsible for the drive current. Parasitic lateral tunneling to the front gate underlap is suppressed by means of a heterogate layout.

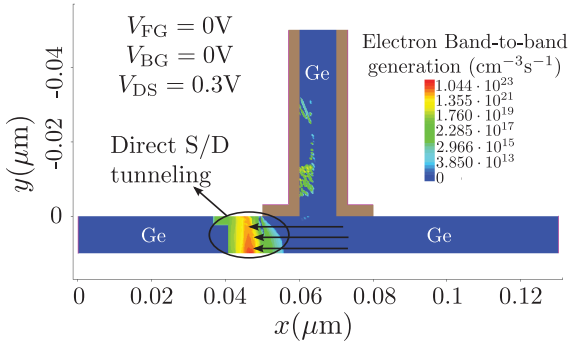



Fig. 2. Electron band–to–band generation rate due to direct source–drain tunneling. This contribution turns out to be noticeable for a Ge body due to the shrinkage of the horizontal length compared to planar EHBTFET structures.

[20] and arises from the different strength of quantization in both overlap and underlap zones. Should this heterogate layout be removed, notable degradation would appear in the switching behavior of the device as we will demonstrate in the following.

## III. Simulation Scheme

The simulation approach that we follow has been deeply analyzed in great part of our recent research [12], [16], [17], [21]. It incorporates quantum mechanical confinement through a customized hybrid usage of the most recent versions of the TCAD simulators Silvaco ATLAS (v.5.20.2.R) [22] and Synopsys Sentaurus (v.2014.09) [23]. Essentially, we divide the calculation process into two consecutive steps. First, we solve in a self-consistent way the Schrödinger and Posisson equations in order to obtain the quantized electrostatics and the subband discretization of the conduction and valence bands [15], [24]. And, second, we inject carriers by means of the dynamic nonlocal BTBT model of Sentaurus as a postprocessing calculation. Given that BTBT injection has been proven [14], [15], [25] to not affect in a meaningful way the potential and charge distributions that would result in absence of tunneling, this postprocessing approach allows very accurate predictions combined with reduced simulation times. Two important remarks need to be done at this point. First, in order to reproduce the potential shape and free charge distribution arising from the Schrödinger-Poisson equations, a calibrated density gradient model needs to be used. Second, as discretization into subbands leads to an effective bandgap widening, we have to include a bandgap increase so that the resulting modified band edges play the role of their respective first bound states, $E_{hh1}$ and $E_{e1}$. Analogous techniques based on TCAD customization procedures have been also recently developed by other authors [25], [26].

## IV. Results and Discussion

### A. Direct source–to–drain tunneling.

In Fig. 2, we observe that the shrunk horizontal length of the FinEHBTFET (compared to other EHBTFET structures [12], [15]) makes direct S/D tunneling to appear in the device. In order to avoid this issue, we replace the source, the drain and the bottom body by $Si_{0.6}Ge_{0.4}$ which increases the effective bandgap and suppresses the S/D tunneling.

### B. Diagonal fin–to–underlap tunneling.

Optimized workfunctions for fixing subband alignment inside the fin at $V_{FG,align} = 0.04V$ and for avoiding parasitic tunneling from the bottom part of the fin to the front gate underlap (see heterogate setup in Fig. 1) are found to be $\phi_{fg,ol} = 3.06eV$, $\phi_{fg,ul} = 4.50eV$ and $\phi_{bg} = 5.05eV$ at $V_{BG} = 0V$. Note how, if we arranged $\phi_{fg,ul} = \phi_{fg,ol} = 3.06eV$, Fig. 3 (top) demonstrates that an unwanted lateral tunneling ending in the front gate underlap would be triggered before the alignment of first electron and hole subbands in the fin. Fig. 3 (bottom) illustrates this fact by showing the subband profile along the $\overline{AB}$ path sketched in Fig. 3 (top). The existence of a certain energy window allowing BTBT gives rise to this leakage current.

### C. Diagonal fin–to–fin tunneling.

Once the parasitic tunneling phenomena outlined above have been removed, the last leakage contribution arises. This leakage current comes from the push-up effect that subbands undergo as we descend along the fin approaching its bottom side. In order to visualize it, let us inspect Fig. 4 (top) which displays the behavior of first subbands for electrons (resp. heavy holes) along vertical cuts inside the fin taken at 1nm distance from the front gate insulator interface (resp. back gate insulator interface). As a result of this observed push-up effect, diagonal alignment between $E_{hh1}$ and $E_{e1}$ is favored at $V_{FG} < 0.04V$ (i.e. before the triggering of the horizontal BTBT responsible for the drive current of the FinEHBTFET). Fig. 4 (bottom) confirms the appearance of a certain BTBT generation rate following these diagonal paths inside the fin at $V_{FG} = 0.02V$.

In order to remove these harmful tunneling processes, we propose to insert a n-doped buffer ($3 \times 10^{18} cm^{-3}$) of 10nm at the bottom of the fin so that $E_{hh1}$ would be lowered in that region and, thus, diagonal BTBT prevented for $V_{FG} < 0.04V$.

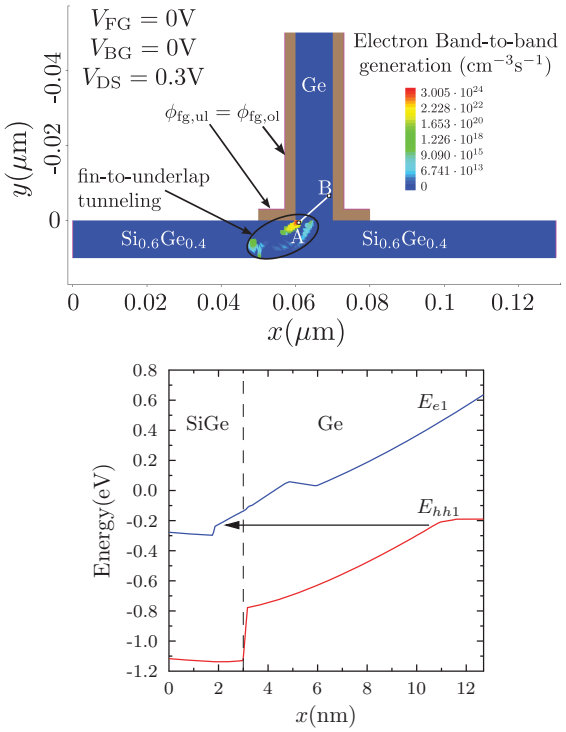



Fig. 3. (Top) Parasitic lateral BTBT from the bottom of the fin to the front gate underlap at $V_{FG} = 0V$ when $\phi_{fg,ul} = \phi_{fg,ol}$. (Bottom) Band profile along the diagonal $\overline{AB}$ segment showing the energy aligment between subbands that allows the appearance of BTBT.

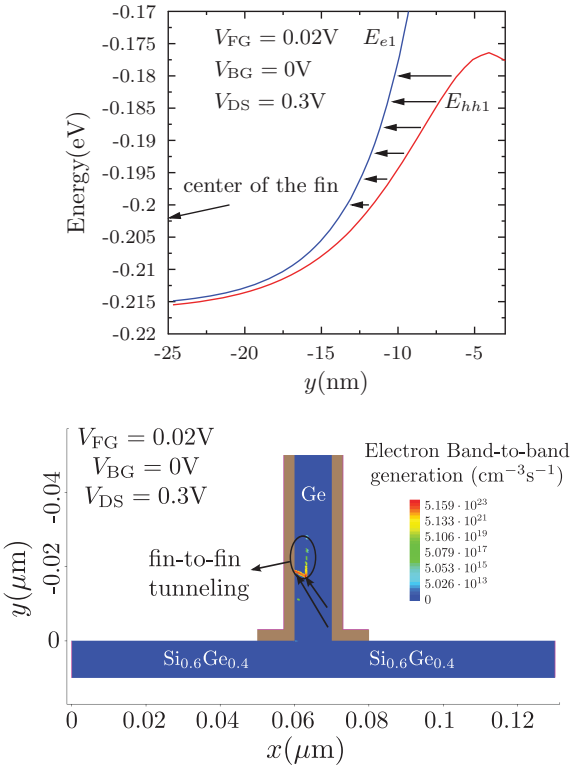



Fig. 4. (Top) Subband profiles along vertical cuts demonstrating parasitic lateral BTBT paths from the bottom to the center of the fin at $V_{FG} = 0.02V$ due to the push-up effect on the subbands. $E_{hh1}$ cut (resp. $E_{e1}$ cut) is taken at 1nm from the back gate interface (resp. front gate interface). (Bottom) 2D map of the electron generation rates illustrating the appearance of the lateral tunneling contributions.

The resulting structure is depicted in Fig. 5 (top) along with the modified subband profiles (bottom) across the aforementioned vertical cuts showing that no diagonal alignment is now attained at $V_{FG} = 0.02V$.

### *D. Resulting transfer characteristics.*

The $I_{DS} - V_{FG}$ curves corresponding to the different configurations hereinabove discussed for the FinEHBTFET are displayed in Fig. 6. Observe how a notable switching abruptness is attained in total absence of parasitic lateral tunneling. For the fully optimized device, we report an outstanding point swing, $SS_{pt}$, of 1.6mV/dec and an average swing, $SS_{av}$, of 40.5mV/dec. Point swing is taken at $V_{FG} = V_{FG,align}$; whereas average swing is estimated between $V_{FG} = V_{FG,align}$ and $V_{FG} = V_{DD} = 0.3V$. Direct BTBT materials and/or reduced bandgap materials like InAs or $In_{0.53}Ga_{0.47}As$ are expected to provide enhanced $I_{ON}$ levels.

## V. Conclusion

We have assessed the effects of quantum mechanical confinement in the Fin Electron–Hole Bilayer TFET showing that parasitic tunneling processes severely degrade the otherwise abrupt switching behavior expected from this type of devices. We have proposed an optimized structure that suppresses the different kind of harmful tunneling phenomena and reports outstanding steep slope transfer characteristics for germanium.

## Acknowledgments

This work was supported by the European Community's Seventh Framework Programme under Grant Agreement No. 619509 (Project E2-Switch) and Marie Curie Action under Grant Agreement No. 291780 (Andalucía Talent Hub).

## References

[1] J. Appenzeller, M. Radosavljevic, J. Knoch, and P. Avouris, "Tunneling Versus Thermionic Emission in One-Dimensional Semiconductors," *Physical Review Letters*, vol. 92, no. 4, 2004.

[2] U. E. Avci, D. H. Morris, and Y. A. Young, "Tunnel Field–Effect Transistors: Prospects and Challenges," *IEEE Journal of the Electron Devices Society*, vol. 3, no. 3, pp. 88–95, 2015.

[3] S. Agarwal, J. T. Teherani, J. L. Hoyt, D. A. Antoniadis, and E. Yablonovitch, "Engineering the Electron–Hole Bilayer Tunneling Field–Effect Transistor," *IEEE Transactions on Electron Devices*, vol. 61, no. 5, pp. 1599–1604, 2014.

[4] M. Schmidt, A. Schfer, R. A. Minamisawa, D. Buca, S. Trellenkamp, J. M. Hartmann, Q. T. Zhao, and S. Mantl, "Line and Point Tunneling in Scaled Si/SiGe Heterostructure TFETs," *IEEE Electron Device Letters*, vol. 35, no. 7, pp. 699–701, 2014.

[5] G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, H. W. Then, and R. Chau, "Fabrication, Characterization and Physics of III-V Heterojunction Tunneling Field–Effect Transistors H-TFET for Steep Sub-threshold Swing," in *Proc. IEEE International Electron Devices Meeting (IEDM)*, 2011, pp. 33.6.1–33.6.4.

[6] D. Sarkar, X. Xie, W. Liu, W. Cao, J. Kang, Y. Gong, S. Kraemer, P. M. Ajayan, and K. Banerjee, "A subthermionic tunnel field–effect transistor with an atomically thin channel," *Nature*, vol. 526, pp. 91–95, 2015.

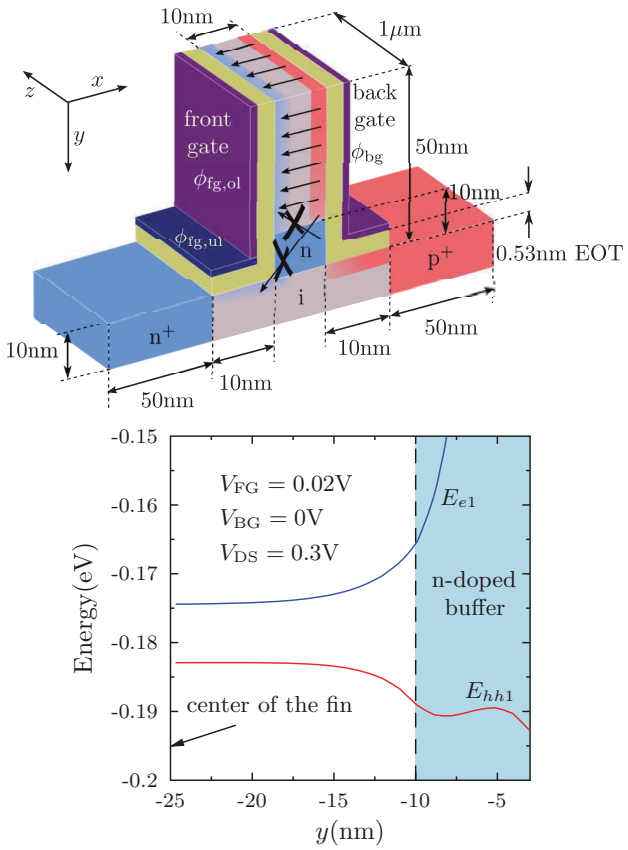



Fig. 5. (Top) Revised FinEHBTFET including a n-doped buffer at the bottom of the fin. (Bottom) Vertical $E_{hh1}$ cut (resp. $E_{e1}$ cut) at $V_{FG} = 0.02V$ and 1nm apart from the back gate interface (resp. front gate interface) resulting from the inclusion of the buffer.

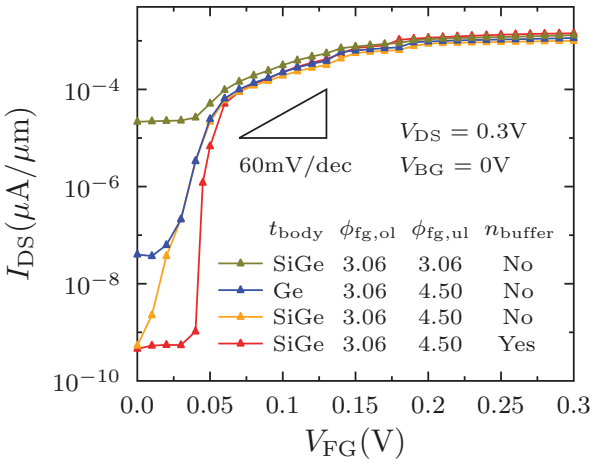



Fig. 6. Comparison between the germanium $I_{DS} - V_{FG}$ curves resulting from the optimization solutions leading to the removal of harmful diagonal tunneling contributions.


[7] Y. Lu, G. Zhou, R. Li, Q. Liu, Q. Zhang, T. Vasen, S. D. Chae, T. Kosel, M. Wistey, H. Xing, A. Seabaugh, and P. Fay, "Performance of AlGaSb/InAs TFETs With Gate Electric Field and Tunneling Direction Aligned," *IEEE Electron Device Letters*, vol. 33, no. 5, pp. 655–657, 2012.

[8] I. A. Fischer, A. S. M. Bakibillah, M. Golve, D. Hahnel, H. Isemann, A. Kottantharayil, M. Oehme, and J. Schulze, "Silicon Tunneling Field-Effect Transistors With Tunneling in Line With the Gate Field," *IEEE Electron Device Letters*, vol. 34, no. 2, pp. 154–156, 2013.

[9] S. Agarwal and E. Yablonovitch, "Using dimensionality to achieve a sharp tunneling FET (TFET) turn-on," in *DRC 69th Annual*, 2011, pp. 199–200.

[10] C. Alper, P. Palestri, L. Lattanzio, J. L. Padilla, and A. M. Ionescu, "Two Dimensional Quantum Mechanical Simulation of Low Dimensional Tunneling Devices," in *in Proc. ESSDERC*, 2014, pp. 186–189.

[11] L. Lattanzio, L. De Michielis, and A. M. Ionescu, "Complementary Germanium Electron-Hole Bilayer Tunnel FET for sub-0.5-V Operation," *IEEE Electron Device Letters*, vol. 33, no. 2, pp. 167–169, 2012.

[12] J. L. Padilla, C. Alper, F. Gamiz, and A. M. Ionescu, "Assessment of field–induced quantum confinement in heterogate germanium electron–hole bilayer tunnel field–effect transistor," *Applied Physics Letters*, vol. 105, no. 8, pp. 082 108–1–082 108–4, 2014.

[13] W. Vandenberghe, B. Soree, W. Magnus, G. Groeseneken, and M. Fischetti, "Impact of field-induced quantum confinement in tunneling field-effect devices," *App. Phys. Lett.*, vol. 98, p. 143503, 2011.

[14] J. L. Padilla, F. Gamiz, and A. Godoy, "The effect of quantum confinement on tunneling field-effect transistors with high-$\kappa$ gate dielectric," *Applied Physics Letters*, vol. 103, no. 11, pp. 112 105–1–112 105–4, 2013.

[15] C. Alper, L. Lattanzio, L. De Michielis, P. Palestri, L. Selmi, and A. M. Ionescu, "Quantum Mechanical Study of the Germanium Electron–Hole Bilayer Tunnel FET," *IEEE Transactions on Electron Devices*, vol. 60, no. 9, pp. 2754–2760, 2013.

[16] J. L. Padilla, C. Alper, A. Godoy, F. Gamiz, and A. M. Ionescu, "Impact of Asymmetric Configurations on the Heterogate Germanium Electron–Hole Bilayer Tunnel Field–Effect Transistor Including Quantum Confinement," *IEEE Transactions on Electron Devices*, vol. 62, no. 11, pp. 3560–3566, 2015.

[17] J. L. Padilla, C. Alper, C. Medina-Bailon, F. Gamiz, and A. M. Ionescu, "Assessment of pseudo–bilayer structures in the heterogate germanium electron–hole bilayer tunnel field–effect transistor," *Applied Physics Letters*, vol. 106, no. 26, pp. 262 102–1–262 102–4, 2015.

[18] A. Revelant, A. Villalon, Y. Wu, A. Zaslavsky, C. Le Royer, H. Iwai, and S. Cristoloveanu, "Electron–Hole Bilayer TFET: Experiments and Comments," *IEEE Transactions on Electron Devices*, vol. 61, no. 8, pp. 2674–2681, 2014.

[19] Z. Zhu, H. Zhu, M. Xu, J. Zhong, C. Zhao, D. Chen, and T. Ye, "A Novel Fin Electron–Hole Bilayer Tunnel Field–Effect Transistor," *IEEE Transactions on Nanotechnology*, vol. 13, no. 6, pp. 1133–1137, 2014.

[20] C. Alper, P. Palestri, L. Lattanzio, J. L. Padilla, and A. M. Ionescu, "Two Dimensional Quantum Mechanical Simulation of Low Dimensional Tunneling Devices," *Solid-State Electronics*, vol. 113, pp. 167–172, 2015.

[21] J. L. Padilla, C. Alper, F. Gamiz, and A. M. Ionescu, "Comment on Germanium electron–hole bilayer tunnel field–effect transistors with a symmetrically arranged double gate," *Semiconductor Science and Technology*, vol. 30, no. 12, pp. 128 001–1–128 001–3, 2015.

[22] Silvaco, *ATLAS users manual*, November 2014.

[23] Synopsys, *Sentaurus Device Tool Manual*, 2014.09.

[24] D. Verreck, A. S. Verhulst, K.-H. Kao, W. G. Vandenberghe, K. De Meyer, and G. Groeseneken, "Quantum Mechanical Performance Predictions of p-n-i-n Versus Pocketed Line Tunnel Field-Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 60, no. 7, pp. 2128–2134, 2013.

[25] A. M. Walke, A. S. Verhulst, A. Vandooren, D. Verreck, E. Simoen, V. R. Rao, G. Groeseneken, N. Collaert, and A. V. Y. Thean, "Part I: Impact of Field-Induced Quantum Confinement on the Subthreshold Swing Behavior of Line TFETs," *IEEE Transactions on Electron Devices*, vol. 60, no. 12, pp. 4057–4064, 2013.

[26] G. B. Beneventi, E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, "Optimization of a Pocketed Dual–Metal–Gate TFET by Means of TCAD Simulations Accounting for Quantization-Induced Bandgap Widening," *IEEE Transactions on Electron Devices*, vol. 62, no. 1, pp. 44–51, 2015.

# Process Modules for GeSn Nanoelectronics with high Sn-contents

C.Schulte-Braucks, S. Glass, E. Hofmann, D. Stange, N. von den Driesch, Q.T. Zhao, D. Buca, S. Mantl
Peter-Grünberg-Institute 9 (PGI-9) and JARA-FIT
Forschungszentrum Jülich GmbH
52428 Jülich, Germany

J.M. Hartmann
University of Grenobles Alpes, F38000 and
CEA, LETI, MINATEC Campus, F-38054,
Grenoble, France

Z. Ikonic
Institute of Microwaves and Photonics, School of Electronic and Electrical Engineering
University of Leeds
LS2 9JT, Leeds, United Kingdom

***Abstract*—In this paper we present a systematic study of GeSn n-FETs. First, process modules such as high-k metal gate stacks and NiGeSn - metallic contacts for use as source/drain contacts are characterized and discussed. GeSn alloys of different Sn content allow the study of the capacitance-voltage (CV) and contact characteristics of both direct and indirect bandgap semiconductors. We then present GeSn n-FET devices we have fabricated. The device characterization includes temperature dependent IV characteristics. As important step towards GeSn for tunnel-FET $Ge_{0.87}Sn_{0.13}$ tunnel-diodes with negative differential resistance at reduced temperature are shown. The present work provides a base for further optimization of GeSn FET and novel tunnel FET devices.**

***Keywords—GeSn, MOSFET, high-k/metal gate, NiGeSn***

## I. INTRODUCTION

GeSn alloys are group IV semiconductors that rapidly evolved within the last years. Thanks to the availability of high-Sn content and strain relaxed layers, we were recently able to prove the existence of a fundamental direct bandgap in a group IV alloy grown on Si [1]. Having direct bandgap (DBG) GeSn alloys is a definite boon for Si based photonics. However such alloys may also serve as performance booster for nanoelectronic devices. The small effective mass and reduced scattering at the center of Brillouin zone allows increased mobility of Γ- electrons and performance improvement of GeSn MOSFETs. In addition the possibility of combining direct band-to-band tunneling and the low bandgap should yield efficient band to band tunneling in tunnel field effect transistors (TFETs).

Theoretical k.p - calculations predict a significant mobility enhancement as soon as the population of Γ-valley increases. For indirect GeSn alloys the mobility is dominated by electrons occupying the L-valley until Sn contents around 9 at.% are reached. For larger Sn contents above the indirect to direct bandgap transition, the Γ-valley becomes populated and the boost in electron mobility becomes significant. The calculated Sn-dependent Γ-valley population and mobility is presented in Fig.1. The mobility of Γ–electrons itself is much larger than mobility of L-electrons, due to a much smaller effective mass and density of states of the former. In direct GeSn, with the L valley not considerable above Γ, strong intervalley Γ–L scattering limits the mobility of Γ–electrons. However when Sn-content and thus the Γ-L spacing further increase this scattering process is suppressed. As a consequence the Γ mobility, as well as the average mobility, strongly increase.

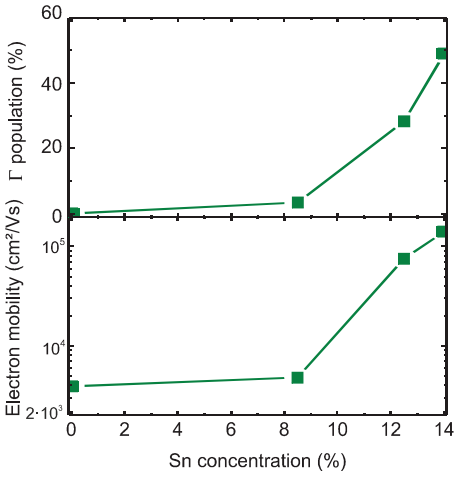



Fig. 1. Calculated Γ-valley population (top) and electron mobility vs Sn-content (bottom) as obtained by k.p-theory.

This research received funding from the EU FP7 project E2SWITCH (619509) and the BMBF project UltraLowPow (16ES0060 K).

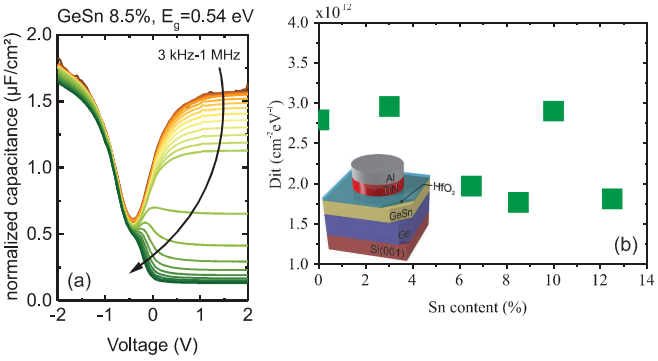



Fig. 2(a) CV-characteristics of TiN/6 nm $HfO_2$/$Ge_{0.915}Sn_{0.085}$ MOScap for a set of frequencies. (b) Dit at midgap for several Sn-contents extracted at low-T.

Preliminary works on p- and n- MOSFETs [2], [3] and even TFETs [4] based on GeSn alloys have been reported, however, with Sn-contents and strain values far below the indirect to direct transition. The low solid solubility of Sn in Ge < 1at.% and the far non-equilibrium growth results in a very limited thermal budged < 350°C for Sn-contents above 10 at.% making process integration challenging as elevated processing temperatures would result in Sn-segregation and precipitation.

In this work we discuss advances on low temperature (T) process modules for GeSn-FET devices with Sn-contents up to 13 at.% including high-k/metal gate stacks with interface trap densities in the $10^{12}$ $eV^{-1}cm^{-2}$-range and low resistivity NiGeSn contacts with ultra-low Schottky barrier heights. Emphases is placed on the fabrication and characterization of tunneling diodes with 13 at.% Sn as well as on first steps toward direct bandgap GeSn n-FETs.

## II. Experimental

Due to the low solid solubility of Sn in Ge < 1 at.% GeSn layers with Sn-contents up to 13 at.% are grown far from equilibrium growth conditions in an industry compatible AIXTRON TRICENT RPCVD reactor [5]. All process modules were kept below 350°C in order to avoid Sn -diffusion and segregation. As a first key module MOS-capacitors (MOScaps) with high-k/ metal gate stacks on GeSn

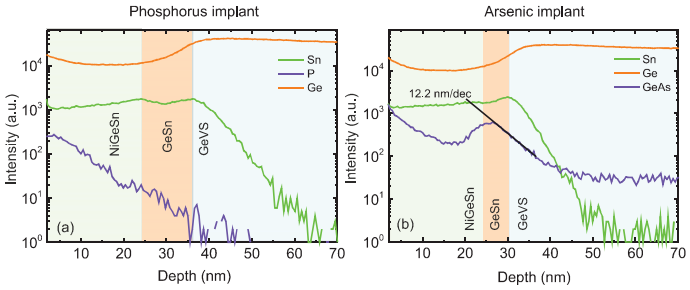



Fig. 4. SIMS-profiles of NiGeSn/GeSn contacts: For Phosphorous impantation no segregation was observed (a), whereas there is a clear peak in the Arsenic profile (b).

have been investigated. After surface preparation in HF-HCl wet cleaning 6 nm $HfO_2$ dielectric followed by 40 nm TiN metal were deposited at low temperature by atomic layer deposition (ALD) and sputter deposition, respectively. MOScaps with Sn-contents between 0 at.% (Ge-substrate) and 12.5 at.% were fabricated. In doing so standard CMOS technology such as photo lithography and reactive ion etching were used to define structures. The fabrication ended up with a lift off process including the deposition of 150 nm Al for contacts followed by forming gas annealing at 300°C. A set of Capacitance-Voltage (CV)-curves for different frequencies measured on TiN/$HfO_2$/$Ge_{0.915}Sn_{0.085}$ is shown in Fig.2(a). The good GeSn/$HfO_2$ interface quality is evidenced by the small frequency dependent flat-band voltage shift and the small frequency dispersion in accumulation. As a characteristic of low bandgap semiconductors, the CV-curves feature a strong minority carrier inversion response even at high frequencies > 100 kHz. As a consequence the so called weak-inversion hump hinders a reliable extraction of interface trap density (Dit) at room temperature [6]. However, at lower temperatures the minority carrier inversion response is reduced and by applying the low-T conductance method Dit values of $2x10^{12}$ $cm^{-2}eV^{-1}$ at midgap were extracted for GeSn capacitors with different Sn contents (Fig. 2(b)).

Metal-semiconductor-metal diodes based on NiGeSn/GeSn Schottky contacts were fabricated using an oxide mask. After native oxide removal, 10 nm of Ni were deposited by sputter deposition and ~ 23 nm NiGeSn was formed by rapid thermal annealing for 10 s in $N_2/H_2$ forming gas atmosphere. Unreacted

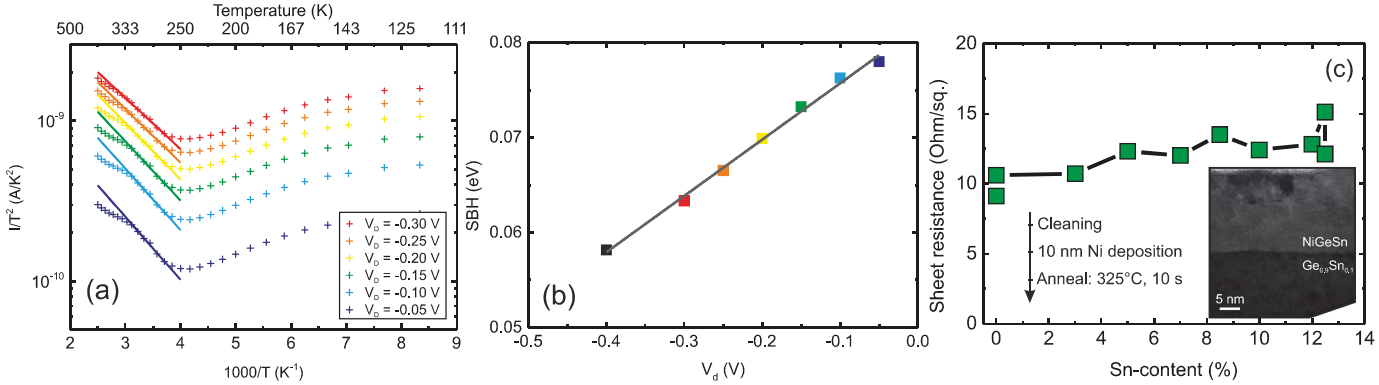



Fig. 3. Investigation of NiGeSn Schottky-contacts (a) Arrhenius plot of current characteristics. The linear region is fitted and SBH is exctracted from the slope. (b) SBH vs. applied bias from (a). The SBH for 0 V is extracted by extrapolation to 0 V. (c) Sheet resistance for NiGeSn fabricated on several GeSn substrates. The inset depicts a TEM micrograph of a NiGeSn/GeSn contact.

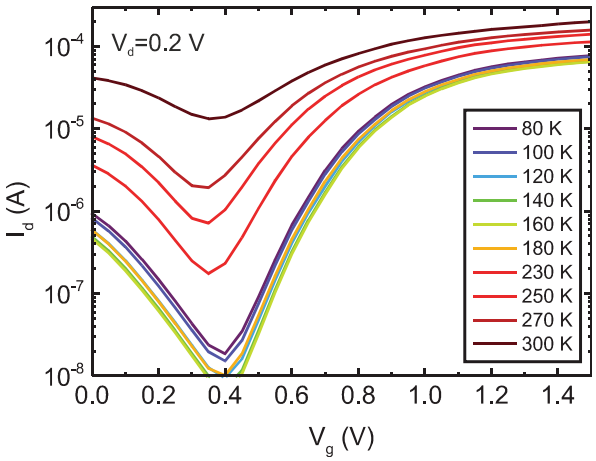



Fig. 5. Tranfer characteristics of $Ge_{0.93}Sn_{0.07}$ n-FETs at different temperatures.

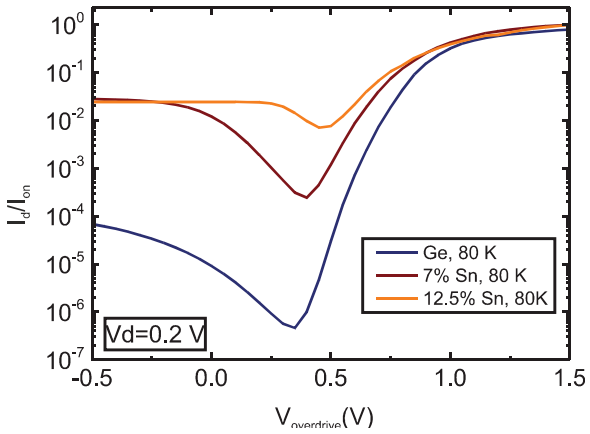



Fig. 6. $I_d/I_{on}$ ratio of GeSn n-FETs at 80 K for several Sn-contents.

Ni was removed by sulfuric acid (96 % aq.). The lowest sheet resistance was obtained by stano-germanidation at 325°C [7]. The low-resistive NiGeSn-phase could be maintained over the complete available Sn-content range from 0 to 12.5 at. %. The sheet resistance of NiGeSn for several Sn-contents is shown in Fig.3(c). Furthermore a smooth NiGeSn/GeSn interface was obtained as shown by the cross-sectional Transmission-Electron-Microscopy (TEM) image in the inset of Fig.3(c). I-V characteristics of two back-to back connected NiGeSn/GeSn Schottky diodes were measured in a temperature range from 350 K down to 100 K. From Arrhenius plots of the current characteristics for different voltages (Fig.3(a)) the Schottky-barrier height (SBH) was extracted by fitting the linear region. In order to exclude the image force lowering by the applied voltage the SBH at 0 V was obtained by plotting the extracted SBH from Fig.3(a) against the applied bias and extrapolating to 0 V, as shown in Fig.3(b). Similar to NiGe/Ge contacts the Schottky barrier of NiGeSn on GeSn for holes is very small. A SBH of 0.08 eV has been extracted for NiGeSn/$Ge_{0.875}Sn_{0.125}$ (p-type) which makes NiGeSn an ideal contact for p-type devices. However, this implies very high Schottky barriers for electrons leading to high S/D resistances for n-type GeSn and demanding further investigation on n-type GeSn-contacts.

Dopant segregation (DS) is a well know method for SBH-tuning [8]. The dopant segregation effect on GeSn with n-type dopants is presented below. Both P and As were first implanted into GeSn test-structures at a dose of $1x10^{15}$ $cm^{-2}$ at energies of 7 and 13 keV, respectively. Then a NiGeSn layer was formed with the above mentioned annealing parameters. Subsequently doping profiles were analyzed by means of Time of Flight Secondary-Ion-Mass-Spectrometry (ToF-SIMS). Whereas there is no peak visible in the doping profile for P, a snowplough effect has been observed for As leading to a peak in the As-concentration at the NiGeSn/GeSn interface (Fig.4). The differences in DS for As and P might be attributed to differences in solubility and diffusion.

Combining the above described process modules GeSn n-MOSFETs were fabricated with Sn contents of 0 at.%, 7 at.% and 12.5 at.% using ion implanted source/drain (S/D) contacts after forming a gate stack with TiN/$HfO_2$. The transfer curves of the GeSn-nFETs for a series of temperatures are shown in Fig.5. At room temperature the device shows a low $I_{on}/I_{off}$ ratio and a reduced on current at lower temperature due to the poor n+/p junctions in the S/D regions. The limited thermal budget used in order to avoid Sn diffusion, here 350°C, was not sufficient to recrystallize the amorphized regions created by ion implantation, leading to very poor junctions with low activation and high access resistances. This is even more critical for high Sn content devices as shown in Fig.6 at 80K. Apart from the un-healed implantation damage the unintentional background doping of GeSn increases with increasing Sn-content. Furthermore the bandgap is decreased. Both factors lead to increased S/D-leakage and gate induced drain-leakage (GIDL) which is caused by band to band tunneling and increases exponentially with the reduced bandgap. This is also visible in the temperature dependence of the transfer characteristics in Fig. 5. The S/D leakage strongly decreases for temperatures below 200 K. The solution for maintaining crystalline GeSn is the use of in-situ doping and selective growth in the S/D region. The in-situ doping is discussed below in terms of tunneling diodes.

As demonstration of the potential of direct bandgap GeSn for band to band tunneling, and the advantage of in-situ doping over ion implantation, we have fabricated GeSn tunneling diodes as an important step towards advanced GeSn based

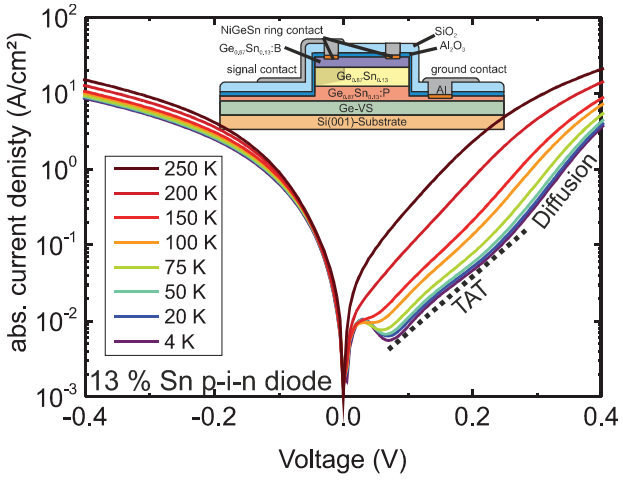



Fig. 7. Temperature dependent I-V measurements of a $Ge_{0.87}Sn_{0.13}$ p-i-n diode showing clear NDR for low-T.

TFETs. We could push the Sn-content up to 13 at.% as a follow up to previous results with a stack of 9 at.% and 11 at.% [9] enabling an even lower bandgap and higher directness of the GeSn. As a proof of band-to-band tunneling negative differential resistance (NDR) is observed at low-T (Fig.7), demonstrating a high doping level of both p and n-type dopants, which is essential for MOSFETs and TFETs. However, due to enhanced diffusion and trap assisted tunneling (TAT) in this low-bandgap semiconductor the NDR vanishes for temperatures above 100 K. In forward bias > 0.1 V two distinct regions separated by a kink in the slope of the I-V curve are visible. Whereas the medium part of the curve 0.1 V < $V_d$ < 0.3 V can be attributed to TAT, diffusion current is dominating for strong forward bias > 0.3 V. We expect further improvements in the peak to valley current ratio and a move towards room temperature NDR with optimized doping profiles.

## III. Conclusion

We presented process module developments for GeSn-FETdevices including high-k metal gate stacks, NiGeSn contacts as well as GeSn-nFETs with Sn-contents >10 at.%. MOScaps with $HfO_2$ on GeSn showed good C-V characteristics with Dit levels of $10^{12}$ $eV^{-1}cm^{-2}$. Uniform NiGeSn contacts on p-GeSn indicated very small Schottky barrier heights, while the Schottky contacts on n-GeSn can be optimized by As dopant segregation. Junctions made by ion implantation face challenges due to the metastability of GeSn, which can be solved by in-situ doping as illustrated by GeSn-tunnel diodes with 13 at.% Sn which show characteristic negative differential resistance at low-T.

## References


[1] S. Wirths, R. Geiger, N. von den Driesch, G. Mussler, T. Stoica, S. Mantl, Z. Ikonic, M. Luysberg, S. Chuissi, J. M. Hartmann, H. Sigg, J. Faist, D. Buca and G. Grützmacher, Lasing in direct-bandgap GeSn alloy grown on Si, Nature Photonics, 9(2), pp. 88–92, 2015.

[2] S. Gupta, B. Vincent, B. Yang, D. Lin, F. Gencarelli, J.-Y.J. Lin, R. Chen, O. Richard, H. Bender, B. Magyari-Köpe, M. Caymax, J. Dekoster, Y. Nishi, and K.C. Saraswat, Towards high-mobility GeSn channel nMOSFETs: Improved surface passivation using novel ozone oxidation method, Electron Devices Meeting (IEDM), 2012 IEEE International, pp. 16.2.1–16.2.4, 2012.

[3] G. Han, S. Su, C. Zhan, Q. Zhou, Y. Yang, L. Wang, P. Guo, W. Wei, C.P. Wong, Z. X. Shen, B. Cheng, and Y.-C. Yeo, High-mobility Germanium-Tin (GeSn) p-channel MOSFET featureing metallic source/drain and sub-370°C process modules, Electron Devices Meeting (IEDM), 2011 IEEE International, pp. 402–404, 2011.

[4] Y. Yang, S. Su, P. Guo, W. Wang, Y. Gong, L. Wang, K. L. Low, G. Zhang, C. Xue, B. Cheng, G. Han, and Y.-C. Yeo, Towards direct band-to-band tunneling in p-channel tunneling field effect transistor (TFET): Technology enablement by Gemanium-Tin (GeSn), Electron Devices Meeting (IEDM), 2012 IEEE International, pp. 16.3.1–16.3.4, 2012.

[5] N. von den Driesch, D. Stange, S. Wirths, G. Mussler, B. Holländer, Z. Ikonic, J. M. Hartmann, T. Stoica, S. Mantl, D. Grützmacher, and D. Buca, Direct bandgap group IV epitacy on Si for laser application, Chem. Mater., 27(13), pp. 4693–4702, 2015

[6] K. Martens, C. O. Chui, G. Brammertz, B. de Jaeger, D. Kuzum, M. Meuris, M. M. Heyns, T. Krishnamohan, K. Saraswat, M. E. Maes, and G. Groeseneken, On the correct extration of interface trap density of MOS devices with high-mobility semiconductor substsrates, IEEE Transactions on Electron Devices, vol 55, 547, 2008.

[7] S. Wirths, R. Troitsch, G. Mussler, J.-M Hartmann, P. Zaumseil, T. Schroeder, S. Mantl, and D. Buca, Ternary and quaternary Ni(Si)Ge(Sn) contact formation for highly strained Ge p- and n-MOSFETs, Semicond. Sci. Technol., 30(5), p. 055003, 2015.

[8] M. Mueller, Q. T. Zhao, C. Urban, C. Sandow, D. Buca, S. Lenk, S. Estévez, and S. Mantl, Schottky-barrier height tuning of NiGe/n-Ge contacts using As and P segregation, Mater. Sci. Eng. B, vol. 154–155, pp. 168–171, 2008

[9] C. Schulte-Braucks, D. Stange, N. von den Driesch, S. Blaeser, Z. Ikonic, J. M. Hartmann, S. Mantl, and D. Buca., Negative differential resistance in direct bandgap GeSn p-i-n structures, Appl. Phys. Lett.,107(4), p. 042101, 2015

# Controlling the physical and electrical properties of ALD grown ZnO using Nb as a dopant

A. Shaw[1], J. D. Jin[1], I. Z. Mitrovic[1], S. Hall[1], J. S. Wrench[2] and P. R. Chalker[2]
[1]Department of Electrical Engineering and Electronics, University of Liverpool, Liverpool, UK.
[2]Centre for Materials and Structures, School of Engineering, University of Liverpool, Liverpool, UK.

*Abstract*— **Thin-film transistors (TFTs) have been fabricated using atomic layer deposition (ALD) Nb-doped ZnO (Nb:ZnO) for the active layer. The optical and electrical properties of the Nb:ZnO TFTs for Nb cycle percentage between 0 and 12.5 % were studied. The optical band gap is seen to increase with Nb content, where a cycle percentage of 12.5% gives an increase of 0.27 eV to 3.54 eV. The device with 3.8% Nb:ZnO exhibited the best TFT characteristics, with an On/Off ratio of $10^8$, saturation mobility of 5.1 $cm^2/Vs$, threshold voltage of 5.1 V and sub-threshold swing of 0.51 V/dec. The characteristic temperature of the material, derived from a model based on an exponential density of states, indicates that the disorder within the material is reduced compared to the use of Mg doping.**

***Keywords— Zinc Oxide (ZnO), Niobium-doped ZnO (Nb:ZnO), thin film transistors (TFTs), atomic layered deposition (ALD), TFT modelling***

## I. Introduction

Over recent years transparent conducting oxides (TCOs) have gathered considerable interest due to their ease of fabrication, low cost, relatively high mobility, conductivity and optical transparency compared to amorphous and poly-crystalline Si TFTs. This has allowed for the possibility of fully transparent electronics being integrated into such applications as heads-up display on windscreens, active matrix displays and local environmental control. For active matrix displays, zinc oxide (ZnO) based materials have been the favourable choice in thin film transistors (TFTs). As-grown ZnO contains a large number of defects giving rise to unacceptably high conductivity, hence the requirement of materials such as indium and gallium (IGZO). The gallium serves to stabilise the structure and hence the threshold voltage and the indium to increase the mobility [1]. However, indium suffers from large fluctuations in high cost and has a low level of abundance which makes it not viable for long-term mass production.

Currently extensive research into non-indium based materials is being conducted for ZnO based TFTs including; gallium [2], silicon [3] and our own work on magnesium [4]. Niobium is an attractive dopant candidate for ZnO, as its high valency ($Nb^{5+}$) offers the prospect of requiring lower concentrations as a substitutional dopant for $Zn^{2+}$ and consequently reduced disorder and carrier scattering. Nb-doping has been explored previously in pulse laser deposited [5,6] and RF sputtered [7] Nb:ZnO TCOs, but not via atomic layer deposition (ALD) using the approach reported here for an active layer for TFTs.

It is common practice within the literature to adopt the standard MOSFET equations to describe the electrical behaviour. However, it is evident in many cases that there is no distinct subthreshold and above threshold regions. In this work, the multiple trapping and release (MTR) model [8] proposed by Torricelli et al. [9] is applied to fit the TFT experimental electrical characteristics. The model describes the current transport in terms of carriers hopping between defect band tail energy states which follow an exponential relationship with energy; the defect states being related to the disordered nature of the Nb:ZnO material. This model constitutes a similar approach to those reported for amorphous Si [10], organic materials [11] and small grain polycrystalline materials [12].

Here we report enhanced optical properties of ALD grown Nb:ZnO material obtained using variable angle spectroscopic-ellipsometry (VASE) and correlate these results with TFT electrical performance.

## II. Experimental

The films were grown using ALD at 200 $^oC$ with precursors diethyl zinc and niobium pentaethoxide for ZnO and Nb respectively on a thermally oxidised n-type Si wafer (50 nm $SiO_2$) with 10 nm of 200 $^0C$ ALD $Al_2O_3$ to act as a capping layer. The Nb content was controlled by varying the percentage between the Zn and Nb precursors for cycle percentages between 0 and 12.5%. Simple bottom-gated TFTs with 50 nm Nb:ZnO as the active layer were fabricated by evaporating Al electrodes, with patterning achieved by lift-off photolithography and wet-etching to isolate each device. Prior to electrical characterisation the films were subsequently annealed at 300 $^oC$ in air for 1 hour to further reduce the film conductivity.

## III. Results and Discussion

Fig.1(a) shows Tauc plots derived from VASE where Nb:ZnO and ZnO films are compared. There is an evident shift of the absorption edge for Nb:ZnO towards higher energy, being indicative of a band gap ($E_g$) energy increase of 0.27 eV in comparison to the ZnO sample, for the maximum cycle percentage of 12.5%. Fig.1(b) shows the effect on the band gap of increasing cycle percentages of Nb. The dependence of % Nb on $E_g$ is seen to be linear initially

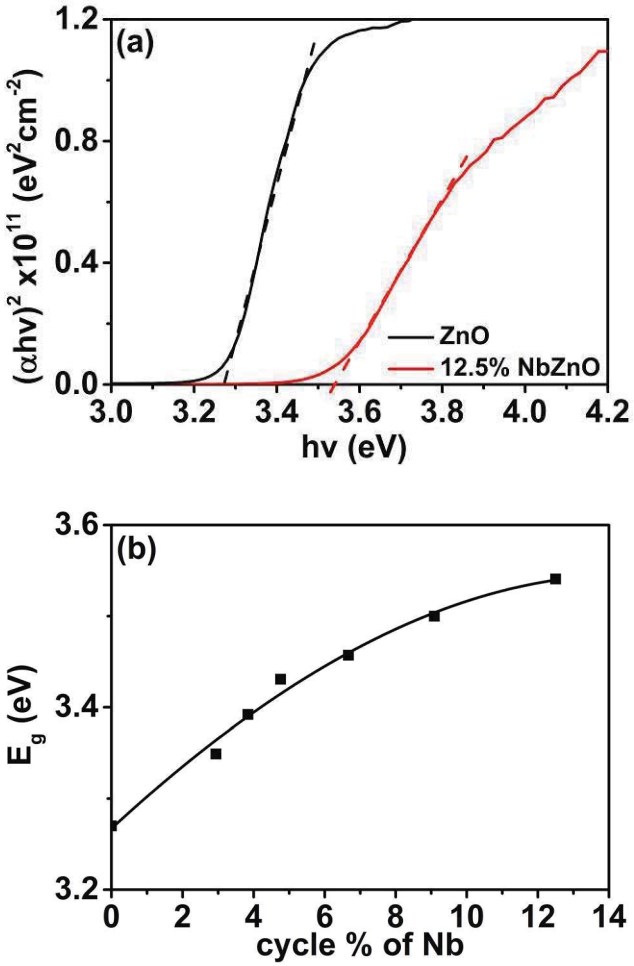



Fig. 1. (a) Tauc plot for ZnO and NbZnO where $\alpha$ is the absorption coefficient and $h\upsilon$ is the photon energy (b) Summary of band gap ($E_g$) increase with increase cycle percentage of Nb from 0% to 12.5%

indicative of the crystal structure remaining constant. At higher concentrations the dependence goes sub-linear possibly due to the films becoming less crystalline as demonstrated by XRD in [13,14] and our own measurements (not shown). This increase in $E_g$ can be explained by the Burstein-Moss effect where the carriers arising from the niobium fill the states above the conduction band which in turn, itself shifts to higher energies. This effect has been confirmed with other Nb:ZnO films [5] and Mg [4] and Ga [15] doped ZnO films.

The standard MOSFET equations were implemented in order to benchmark the TFT performance with the literature. The threshold voltage ($V_T$) and saturation mobility ($\mu_{sat}$) were extracted using the MOSFET equation The extracted TFT parameters for Nb cycle percentages between 0% and 12.5% are presented in Table I, where the channel length ($L$) and width ($W$) are 40 µm and 400 µm respectively.

$$I_D = \frac{W}{2L}\mu_{sat}C_o(V_{GS} - V_T)^2 \qquad (1)$$

TABLE I. COMPARISON OF TFT PARAMETERS FOR NB:ZNO WITH VARYING CYCLE FRACTION FROM 0 TO 12.5%

| Nb cycle fraction (%) | On/Off ratio | $V_T$ (V) | $\mu_{sat}$ ($cm^2$/Vs) | *SS* (V/dec) |
|---|---|---|---|---|
| 0 | $1.0 \times 10^4$ | 9.32 | 1.41 | 2.97 |
| 2.9 | $6.07\times 10^7$ | 7.63 | 5.1 | 1.07 |
| 3.8 | $1.4 \times 10^8$ | 7.06 | 5.13 | 0.51 |
| 4.8 | $1.5 \times 10^7$ | 4.1 | 0.88 | 0.39 |
| 6.67 | $1.24\times 10^6$ | 2.47 | 0.78 | 0.32 |
| 9.1 | $3.2 \times 10^7$ | 3.59 | 0.32 | 0.36 |
| 12.5 | $1.17\times 10^6$ | 1.05 | 0.07 | 1.25 |

where $C_o$ is the gate oxide capacitance per unit area and $V_{GS}$ the gate source voltage. The effective subthreshold swing (*SS*) was also extracted at the steepest part of the transfer slope and is interpreted here as an indication of the trap concentration, $N_t$ in the film and at the interface:

$$SS = \left(\frac{d\log(I_D)}{dV_{GS}}\right)^{-1} = \frac{N_t}{C_o}kT\ell n(10) \qquad (2)$$

Equations (1,2) are commonly adopted in the literature, presumably for ease of comparison between reported device metrics. It is evident in Table I that for all of the doped samples that the *On/Off* ratio has been dramatically improved because the *Off*-current has been reduced. Cycle percentages 3.8 to 9.09% have a relatively low sub-threshold swing which indicates a reduction of the interface states, density and disorder of the film. This reduced *SS* can be attributed to the influence of Nb. Moreover, it is apparent that with increasing Nb cycle percentage, the $V_T$ shifts to lower voltages and $\mu_{sat}$ is initially enhanced by the Nb as saturation is achieved. However, as Nb is further increased, $\mu_{sat}$ is reduced. From Table I, 3.8% Nb:ZnO has the best TFT characteristics with the highest *On/Off* ratio of $1.4 \times 10^8$ and $\mu_{sat}$ = 5.1 $cm^2$/Vs, with a low $V_T$ =5.1 V and *SS* = 0.51 V/dec. Fig. 2 shows a comparison of the TFT characteristics for the ZnO and 3.8% Nb:ZnO TFTs. Fig.2 (a) and (b) both demonstrate good saturation of current for the ZnO and Nb:ZnO respectively. However, the transfer characteristics in Fig.2(c) illustrate that the addition of 3.8% of the cycle ratios of Nb effectively reduces the conductivity of the film and in turn drastically reduces the *Off*-current by from $10^{-8}$ to $10^{-12}$ A: 4 orders of magnitude.

The aforementioned extracted parameters assume the validity of standard Si MOSFET theory in these accumulation mode devices; a commonly used assumption in the literature which allows for easy comparison of technologies. However, it is evident from the transfer characteristics in Fig.2(c), that the TFT does not follow distinct sub-threshold and quadratic regions. Therefore, the transport mechanism MTR model is employed to explain the characteristics [9,11]. The MTR model involves charge carriers trapped in localized states within the bandgap are thermally excited towards the delocalized states (conduction band) by hopping between

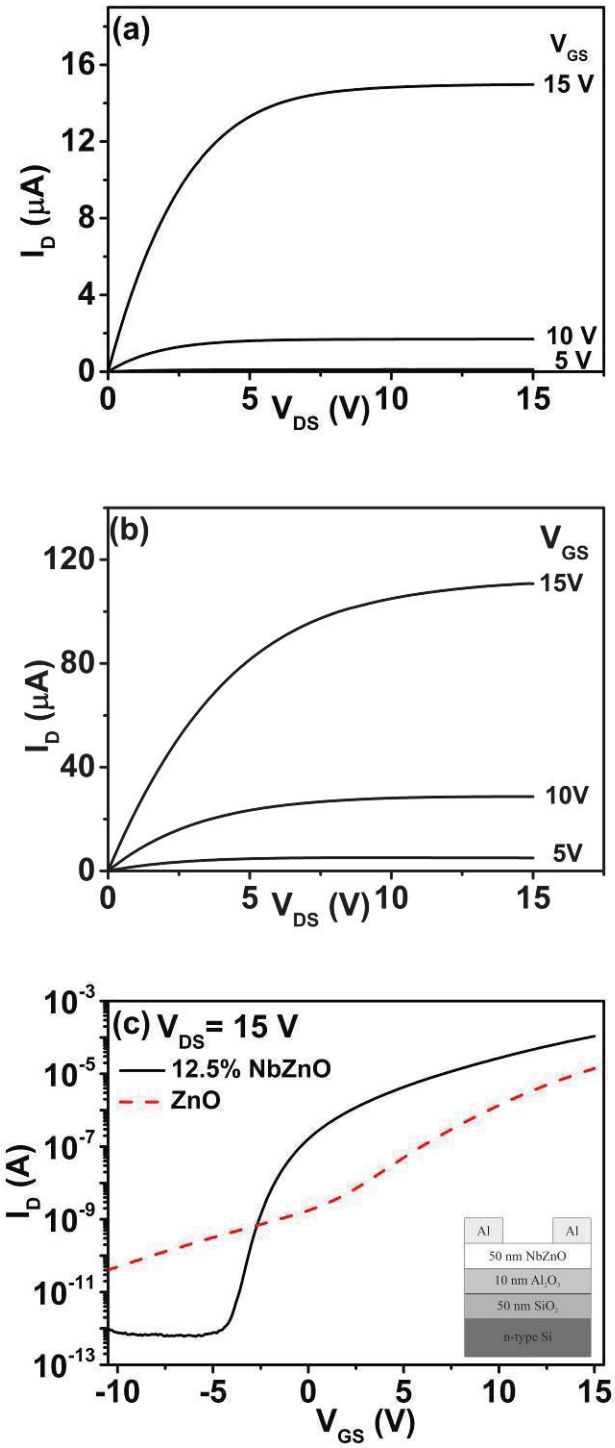



Fig. 3. Output characteristics for the (a) ZnO and (b) 3.8% NbZnO and (c) transfer characteristics of 3.8 % NbZnO and ZnO. The inset shows a schematic of the NbZnO TFTs

localized states [9]. Once these charge carriers reach the conduction band, they can contribute to the charge transport.

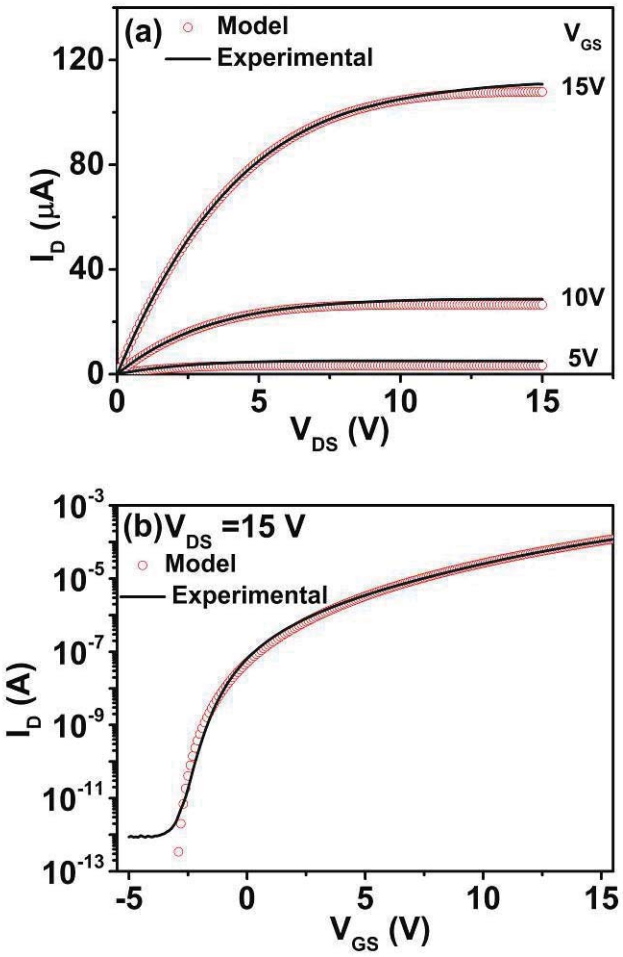



Fig. 2. (a) output and (b) transfer fittings of the 3.8% NbZnO TFT using the MTR model. The fitting parameters are; $V_{FB}$= −3.12 V, (model parameters are defined in [6])

A two term exponential density of defect states is assumed in the model

$$g(E) = N_{deep} \exp\left[\frac{E - E_c}{kT_{deep}}\right] + N_{tail} \exp\left[\frac{E - E_c}{kT_{tail}}\right] \quad (3)$$

where $N_{deep}$ and $N_{tail}$ are the number of deep and tail states respectively, at the conduction band ($E_C$) and $T_{deep}$ and $T_{tail}$ are the characteristic temperatures for the deep and tail states respectively. It can be noted that for ZnO the deep states are dependent on the oxygen vacancies and tail states on the zinc interstitials [16]. It can be shown that, (3) can be simplified to a single exponential $g(E) \sim \exp\left[{(E-Ec)}/{kT_o}\right]$, where $T_o$ is a characteristic temperature which is closely related to the tail states [9]. The parameter $T_o$ provides an indication of the degree of disorder in the film. This treatment leads to a power-law dependence of the transfer characteristics, where the drain current equation is defined as

$$I_D = \frac{W}{L}\beta\left[(V_{GS} - V_{FB})^{\gamma} - (V_{GS} - V_{FB} - V_{DS})^{\gamma}\right] \quad (4)$$

where $V_{FB}$ is the flat band voltage, $\gamma=2T_o/T$, T is the absolute temperature and $\beta$ is defined as

$$\beta = \sigma_o \frac{\varepsilon_s}{C_{ox}} V_t \left( \frac{1}{\gamma - 1} \right) \left( \frac{C_{ox}^2 \sin\left(2\pi/\gamma\right)}{2\pi N_t q \varepsilon_s V_t} \right)^{\frac{\gamma}{2}} \quad (5)$$

where $\sigma_o$ is a conductivity pre-factor, $\varepsilon_s$ is the permittivity of Nb:ZnO (assumed the same as bulk ZnO), $N_t$ is the number of traps, $q$ is the charge of an electron, and $V_t$ is the thermal voltage ($kT/q$). The drain voltage $V_{DS}$ is defined in the triode region ($V_{DS} > V_{GS}$-$V_{FB}$) and $V_{GS}$-$V_{FB}$ in the saturation region ($V_{DS} \leq V_{GS}$-$V_{FB}$).

Using this model, a good fit is observed in Fig.3 for both transfer and output characteristics. The fitting parameters used are $V_{FB}$= −3.12 V, $T_o$=657 K and $\beta$= $3.32\times10^{-11}$. All these fitting parameters are all related to the physical properties of materials, where $N_t$ and $T_o$ are dependent on the DOS of the Nb:ZnO, $V_{FB}$ is determined by the insulator-semiconductor interface and deep traps and $\sigma_o$ is the Nb:ZnO bulk conductivity. Furthermore, if we compare the $T_o$ parameter with previously reported values for IGZO, ZnO and MgZnO (400 K [17], 710 K [9] and 791 K [18] respectively), it can be seen that Nb doping has successfully reduced the disorder of the films nearer to that of IGZO. This is also confirmed with the lower *SS* obtained when using the standard MOSFET analysis.

## IV. Conclusion

The effectiveness of Nb doping of ALD grown ZnO, with regards to enhanced optical properties and electrical characteristics for effective TFT performance has been demonstrated. The band gap has been increased with added Nb content due to the Burstein-Moss effect. The 3.8% cycle percentage sample demonstrates the best TFT characteristics where a relatively low *SS* confirms that the disorder of the film has been reduced compared to the Mg-doped films [18]. This is further confirmed by the lower value of characteristic temperature, $T_o$ than for other doping types.

## Acknowledgment

This work is supported by Engineering and Physical Science Research Council, UK, under project EP/K018884/1.

## References

[1] H. Hosono et al.,J. "Ionic amorphous oxide semiconductors: Material design, carrier transport, and device application", Non-Cryst. Solids, vol. 352, pp. 851– 858, 2006.

[2] T. Nam et al., "Growth characteristics and properties of Ga-doped ZnO (GZO) thin films grown by thermal and plasma-enhanced atomic layer deposition", Appl. Surf. Sci., vol. 295, pp.260-265, 2014.

[3] S. H. Lee et al., "Effects of co-sputtering powers on the properties of silicon-incorporated zinc oxide used as a channel layer of thin film transistors", Thin Solid Films, vol. 549, pp.46-49, 2013.

[4] J. S. Wrench et al., "Compositional tuning of atomic layer deposited MgZnO for thin film transistors", Appl. Phys. Lett. vol. 105(20), pp. 202109, 2014.

[5] J. Shao et al., "Metal-semiconductor transition in Nb-doped ZnO thin films prepared by pulsed laser deposition", Thin Solid Films, vol. 518, pp. 5288-5291, 2010.

[6] J. M. Lin et al., "Nb-doped ZnO transparent conducting films fabricated by pulsed laser deposition", Appl. Surf. Sci., vol. 255, pp. 6460-6463, 2009.

[7] C. Feng et al., "Preparation and Characterization of Transparent Conductive Nb-Doped ZnO Films by Radio-Frequency Sputtering", Chin. Phys. Lett., vol 26 (3), pp. 034210, 2008.

[8] P. Servati et al., "Generalized transport-band field-effect mobility in disorderd organic and incorganic semiconductors", Phys. Rev. B., vol 84. pp.245210, 2006.

[9] F. Torricelli et al., "Transport physics and device modeling of zinc oxide thin-film transistors part I: Long-channel devices", IEEE Trans. Electron Devices, vol. 58, pp. 2610-2619, 2011.

[10] M. Shur et al., "Physics of amprphous silicon based alloy field-effect transistors", Solid State Electron., vol. 45 (9), pp. 1525-1520, 2001

[11] M. Raja et al., "Analytical device models for disordered organic Schottky diodes and thin-film transistors for circuit simulations", IET Circuits Devices Syst., vol. 6(2), pp.122, 2012.

[12] M. Hack et al., "Physical models for degradation effects in polysilicon thin-film transistors", IEEE Trans. Electron Devices, vol. 40 (5), pp. 890-897, 1993.

[13] V. Gokulakrishnanb et al., "Structural, Optical, and Electrical Properties of Nb-Doped ZnO Thin Films Prepared by Spray Pyrolysis Method", J. Electron. Mater., vol. 40 (12), pp. 2382-2387, 2011

[14] H. Yoon et al., "Photodegradation ofmethyleneblueofniobium-doped zinc oxide thin films produced by electrostatic spray deposition", Ceram. Int., vol. 40, pp. 7567-7571, 2014.

[15] A. Segura et al., "High conductivity of Ga-doped rock-salt ZnO under pressure: Hint on deep-ultraviolet-transparent conducting oxides", Appl. Phys. Lett., vol. 88(1), pp. 011910, 2006.

[16] J. Robertson, "Disorder and instability processes in amorphous conducting oxides", Phys. Status Solidi (B), vol. 245 (6), pp.1026-1032, 2008.

[17] S. Lee et al., "Trap-limited and percolation conduction mechanisms in amorphous oxide semiconductor tin film transistors (TFTs)", Appl. Phys. Lett., vol. 98 (20), pp.203508, 2011.

[18] A. Shaw et al., "Physical and electrical characterization of Mg-doped ZnO thin-film transistors ", Proc. Of ESSDERC, pp. 206-209, 2015.

# Single-electron transistors featuring silicon nitride tunnel barriers prepared by atomic layer deposition

Golnaz Karbasian, Alexei O. Orlov, Alexander S. Mukasyan, and Gregory L. Snider
University of Notre Dame, Notre Dame IN, 46556, USA. Email:aorlov@gmail.com

***Abstract*—Single electron transistors (SET) featuring metal (Ni) electrodes and silicon nitride dielectric barriers prepared by atomic layer deposition are fabricated and tested. Electrical characterization of the devices reveals electrostatic energy parameters consistent with the parameters of the designed tunnel junctions. In addition, an analysis of temperature dependence of conductance confirms the formation of metal-insulator-metal (MIM) junctions with negligible in-series contribution of any surface native metal oxide. However, the fabricated devices exhibit a very high level of electrical noise, far exceeding the commonly observed shot noise. Experimental investigation reveals the random telegraph signal (RTS) nature of the observed excess noise. The RTS noise in electronic devices is commonly associated with charging of external traps that are electrostatically coupled to the SET island. In the devices under study, however, the defects that result in the observed RTS noise are demonstrated to reside *within* the tunnel junctions. Our results also indicate the critical importance of interface states and surface preparation for achieving good performance of the SETs fabricated using ALD to form the tunnel barrier.**

***Keywords—single electron transistor, atomic layer deposition, silicon nitride, random telegraph signal, single charged defects.***

## I. Introduction

The downscaling of electronic device dimensions enables the use of ultrathin layers down to a few atomic layers which requires a good understanding of underlying physical and chemical processes that govern each nanofabrication step. In single electron transistors (SETs) [1] charge transfer through the device is guided by the Coulomb charging energy $E_C=e^2/2C$ where $e$ is an elementary charge and C is the total capacitance of the island. The performance of an SET critically depends on the quality of a few-atomic-layer thick barrier in the source and drain tunnel junctions. For instance, the presence of defects in the dielectric will affect the noise exhibited by the SETs, and non-uniformities in the dielectric lead to strong variations in the SET characteristics. The unique sensitivity of SETs to single charge defects in the tunnel dielectric makes them ideal sensors for evaluating the quality of ultrathin dielectrics with "princess and the pea" sensitivity. Here, we use the electrical characterization of SETs to identify the origin of charged defects in the devices and to evaluate the strength of the observed noise. Additionally, several techniques are explored to passivate the defects in the fabricated devices.

## II. Fabrication and Experiment

### A. Device fabrication

The metal-insulator-metal (MIM) SETs are fabricated using a combination of high-resolution electron beam lithography (EBL), nanodamascene planarization, and $Si_3N_4$ tunnel barrier dielectric formation using plasma-enhanced atomic layer deposition (PEALD) [2, 3]. Figure 1 shows a micrograph of a fabricated device. First, using a Vistec EBPG 5200 100-keV EBL system, the pattern of the island is defined in polymethylglutarimide (PMGI) spun on the thermal $SiO_2$ substrate [4]. PMGI is used as a mask for $SiO_2$ etch due to its higher etch resistance than polymethylmethacrylate (PMMA). The pattern of the island is then transferred into the oxide using Ar, $C_4F_8$, $CHF_3$, and $CF_4$ chemistry in an inductively coupled plasma (ICP) etcher. Next, Ni is deposited by e-beam evaporation at the base pressure of $<8\times10^{-7}$ Torr to fill the trench in $SiO_2$, while the field is still covered by the remaining PMGI mask. The evaporated metal on the field along with the underlying PMGI is then lifted off by MR-Rem 400 stripper from Micro Resist Technology, heated to 70°C. Chemical mechanical polishing (CMP) is then used to remove any residual Ni on the oxide field, while leaving the island trench filled with Ni. Next, 21 cycles of PEALD of $Si_3N_4$ is performed in an Oxford FlexAL system, with Bisdiethylaminosilane ($C_8H_{22}N_2Si$) and $H_2+N_2$ plasma to form the $Si_3N_4$ dielectric barrier covering the island. Finally, Ni source and drain are defined by a second EBL and liftoff. Two post-fabrication treatments were also investigated: $H_2$ plasma treatment to ensure reduction of NiO potentially formed during exposure of the junctions to the ambient, and $N_2$ plasma treatment with the goal of passivating the nitrogen vacancies that are possibly formed in the barrier.

### B. Experiment

Next, devices are bonded to a chip carrier and electrically tested in the range of temperatures from 300K down to 0.4K in a closed-cycle $^3$He refrigerator. For electrical characterization we use standard lock-in technique with AC and DC voltage sources connected to the drain, and source connected to the input of transimpedance amplifier. Differential conductance $G=dI_{ds}/dV_{ds}$ is measured at 8-30 Hz with excitation level of 1 mV in the temperature range of 300 K-10 K and 100 μV for lower temperatures down to 0.4 K. The conductance of fabricated devices measured at room temperature exhibits wide spread of values, from 10 nS up to 1 μS for nominally identical devices. This is likely to originate from non-uniformities in the $Si_3N_4$ that is formed during the PEALD.

This work was supported by National Science Foundation grants DMR-1207394 and CHE-1124762.

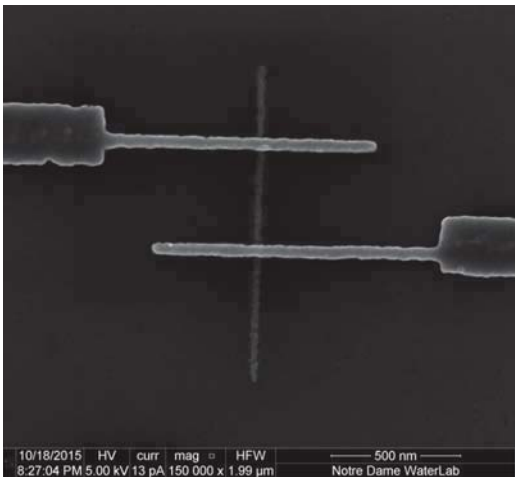



Fig. 1. Scanning electron micrograph (SEM) of the fabricated device

Two dimensional maps $G(V_g, V_{ds})$, a standard test for SET characterization, are acquired for more than 10 devices, and all of them show "Coulomb diamonds" with the shape typical for SETs with MIM junctions and characteristic energy gap, $4\times E_C$ in the range 1.5 to 2 meV. An experimentally obtained diamond plot for a typical device is shown in Fig. 2a. To evaluate parameters of the junctions, we perform simulations based on orthodox model [5], where the capacitance matrix is defined using parameters obtained from the shape of Coulomb diamonds [1], and the values of the junction conductances are obtained by fitting the shapes of experimental $G(V_{ds})$ measurements to the model. Fig. 2b shows the results of simulations with the following parameters: $C_s$=45 aF, $C_d$=52 aF, $C_g$=27.6 aF, $G_s$=0.55 µS, and $G_d$=0.2 µS. Neglecting fringing field, a parallel plate estimate for junction capacitance of 30 × 20 nm$^2$ overlap and using SiN with dielectric constant of ε=7 and thickness of 1 nm, gives the value of the expected junction capacitance ~35 aF, in reasonable agreement with the experiment.

Dissimilar (by a factor of >2) conductance of the junctions can be attributed to non-uniformities in the ALD dielectric layer where a thinner "weak spot" in the dielectric may drastically change device conductance while not significantly affect its capacitance. An important known issue for MIM SET devices with ALD dielectric is the formation of interfacial metal oxide during the ALD process [2, 3, 6], resulting in a strong temperature dependence of conductance in the peaks of Coulomb blockade oscillations (CBOs). To investigate the potential presence of NiO in Ni-$Si_3N_4$-Ni junctions, we measure temperature dependence of the SET zero-bias conductance for a slowly increasing temperature. During the experiment, the $V_g$ bias is continuously swept over five periods of CBOs while temperature slowly increases, so the temperature dependence of conductance can be accurately evaluated at both peaks and valleys of CBOs. The result of the experiment is presented in Fig. 3, where ln $G(V_{ds}=0)$ is plotted as a function of inverse temperature 1/T. According to the orthodox theory of Coulomb blockade for MIM SETs [7], as the temperature is reduced to T≈ $4Ec/k_B$, the conductance

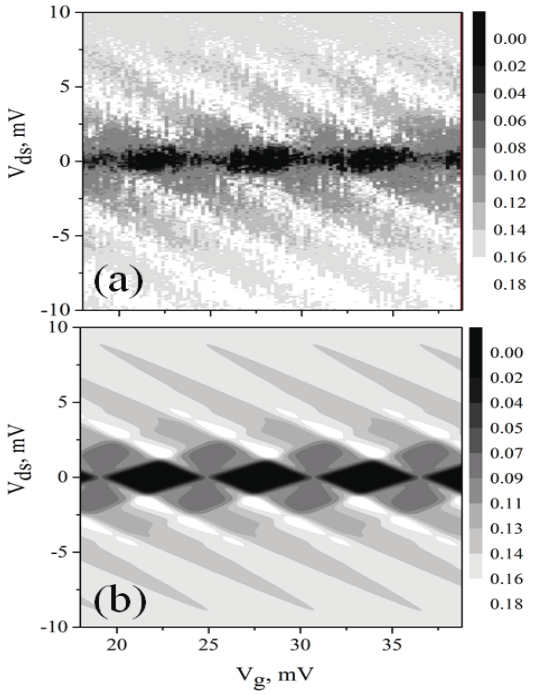



Fig. 2. Typical Coulomb diamond plot for SET with 21 layer of SiN (sample NT-G1): (a) experiment (b) simulations using orthodox model. Gray scale in µS.

through the device decreases due to Coulomb blockade in the island. As the temperature is lowered, the differential conductance in the peaks of the CBO stays at a level $G_{max}=G_0/2$ (blue dashed line in Fig.3) where $G_0$ is conductance at high temperature ($T>>E_C/k_B$), while with lowering T the conductance in the valleys is exponentially suppressed with an activation energy of $E_C$: $G(T)=G_0 \exp(-E_C/k_BT)$. The experiment shows exactly this: for $1/T<0.2$ the data are merged into a line, while for $1/T>0.2$ the line diverges into an

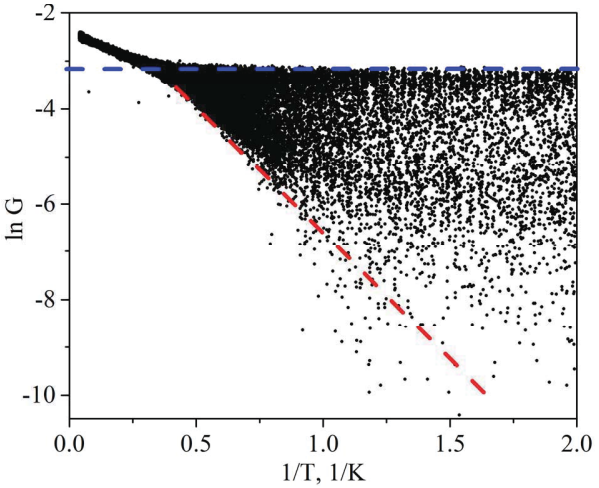



Fig. 3. Temperature dependence of conductance at $V_{ds}$=0. Data are acquired for $V_g$ bias swinging in the range over five periods of Coulomb blockade oscillations for slowly changing temperature. Variation in the density of points is the result of non-linear axis transformation.

area with minimal values approaching the red dashed line corresponding to the thermal activation over the barrier. A very close proximity of the expected CBO maxima to the blue dashed line ($G_0/2$) indicate an insignificant contribution of in-series thermally activated NiO surface oxide in the junctions to the total conductance [2, 3] and the activation energy $E_A \approx 0.5$ meV extracted from this measurement closely matches the charging energy value obtained from Coulomb diamond plot.

The observed Coulomb diamond plot also reveals a very large level of excess "switching noise." An example of such noise is shown in Fig. 4, where two traces of $G(V_{ds})$ were measured for the same $V_g$, showing multiple jumps between several states. This is a signature of RTS, a random phenomenon stemming from capture and release of charge carriers in single traps near the conducting channel of an electronic device [8]. In the case of SETs, the RTS can be treated as an additional offset charge that modulates conductance through the SET, a process that was investigated in detail in [9]. If several of such modulators are active simultaneously the resulting pattern is identified as "multi-level RTS" [10]. To understand the origin of this noise we experimentally acquire a large number of $G(V_{ds})$ traces, in addition to those shown in Fig 4, for a fixed value of $V_g$ and then calculated the "time averaged" curve (red line in Fig 5a). We also averaged $G(V_{ds})$ traces over the full span of 3 experimentally obtained Coulomb diamonds (magenta line in Fig. 5a). As expected, "diamond average", i.e. conductance averaged over full Coulomb diamond has no oscillatory features. In contrast, noticeable oscillatory features are observed for time averaged trace at fixed $V_g$ in Fig 5a. To replicate the experimentally observed features with simulations we performed iterative averaging over a variable span of $V_g$, centered on the gate bias used in experiment (red line in Fig. 5b). For simplicity, a uniform distribution was assumed for curves weights in the averaging $V_g$ interval. Additionally, a diamond average over three full diamonds was calculated (magenta line in Fig 5b). Finally, we subtracted respective diamond averages from time average (experiment) or narrow $V_g$ span average (calculations). The results shown in Fig. 5c are in reasonable agreement with each other, indicating the validity of the proposed charge offset evaluation technique.

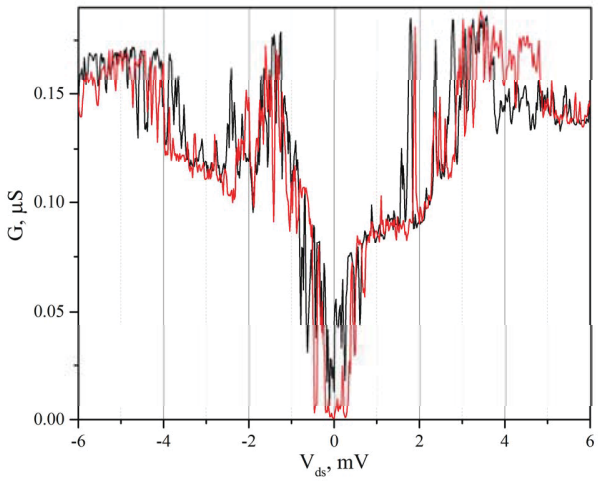



Fig. 4. Two consecutive sweeps of $V_{ds}$ taken at $V_g$=27 mV (sample NT-G1). Very strong "switching noise" is clearly visible.

### C. Discussion

We believe that the observed results shed light on the equivalent magnitude of charge offset noise. Experiment reveals that the observed time averaged $G(V_{ds})$ trace can be replicated by averaging of multiple traces uniformly distributed in the offset charge span of $\delta Q_g = e\,(\delta V_g/\Delta V_{CBO}) \approx 0.3\ e$. This is a "full swing" of charge fluctuation, meaning that deviation from average is up to 0.15 e in a bandwidth of 0.78 Hz, or 0.17 e/√Hz. This is a very large noise level, exceeding by many orders of magnitude both the shot noise caused by charge discreteness and 1/f noise that limits the sensitivity of SETs at levels $\approx 0^{-4}/\sqrt{\text{Hz}}$ at low frequencies. Can a single trap in a junction lead to this level of charge fluctuations? The impact of charging of a single electron trap depends on coupling of that trap to the island. The case of charged traps coupled to gate, island and source (or drain) of the SET was studied in [11], where it was observed that a single trap can cause an abrupt shift in CBO pattern (e.g. from peak to a valley). Note that in such a case the appearance of a specific trap is gate voltage dependent (i.e. it changes the conductance over specific range of gate bias and stays "mute" elsewhere [9, 11]). Here the situation is qualitatively different: the switching events are "gate independent" i.e. occurring with equal probability at any gate voltage. That implies that the source of switching is not electrostatically coupled to the gate. Therefore it is reasonable to assume that the source of this noise is located *within* the tunnel junctions - either in the ALD dielectric or in the interfacial layers adjacent to the dielectric where it is shielded from electric field emanating from the gate. The trap charging/discharging process in the junction decoupled from the gate nonetheless leads to offsets of Coulomb diamond patterns along $V_g$ axis because the action of that trap is equivalent to an extra gate potential acting on the island. The strength of coupling from such trap to the island determines the strength of the observed shift. If a trap located in the source

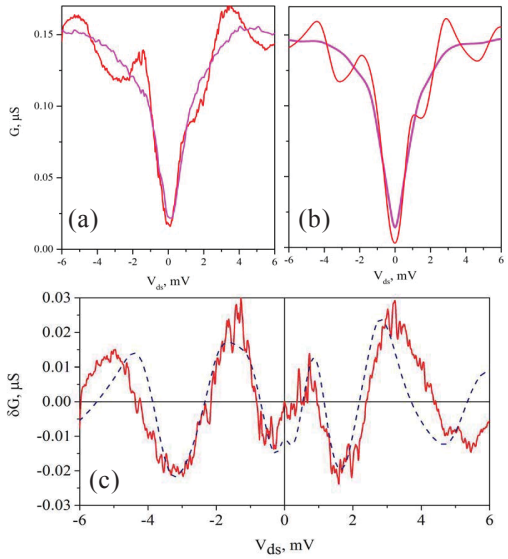



Fig. 5. Results of $G(V_{ds})$ "span average" vs time average at $V_g$=const: (a) – experiment. Red: average of 57 traces at $V_g$=27 mV. Magenta: "diamond average," i.e. traces averaged over $V_g$ span of three full Coulomb diamonds in Fig. 2 a. (b) – simulations. Red: ensemble average over 25.5 mV< $V_g$<27.2 mV span. Magenta: diamond average over $V_g$ span of three full Coulomb diamonds in Fig 2 b.(c) Comparison of the experiment and the simulations after "diamond average" subtraction. Red–experiment; dashed blue line- simulations

(drain) junction is equally coupled to the source (drain) and the island, the change in its population by one electron will exert a 0.5 *e* charge and shift the diamonds by a half of a CBO period. The experimentally observed averaged diamond shift of 0.2-0.3 *e* can be explained by action of the traps located closer to the junction's interfaces (i.e. asymmetrically coupled, leading to smaller charge offsets) or may results from oversimplified model used in simulations. Nonetheless, this value is consistent with the model of traps acting inside the junctions. Since the observed switching noise has no identifiable voltage threshold in $V_{ds}$ it is reasonable to assume that several different traps located inside the tunnel junction are participating in the process: as $V_{ds}$ changes, certain traps become active within certain range of $V_{ds}$ resulting in a "multiple RTS" signature. The exact number of traps participating in the process is not precisely known and remains to be investigated.

We have previously demonstrated that by using a combination of anneal and reducing plasma treatments it is possible to nearly completely suppress this type of noise in Ni-$SiO_2$-Ni junctions [12]. In other words, those charge defects could be potentially healed with proper treatments.

So far, $N_2$ plasma on the finished devices to fill the nitrogen vacancies in the nitride or $H_2$ plasma to chemically reduce the parasitically formed NiO does not seem to be effective in decreasing the observed noise. One potential drawback of such treatments after device fabrication is the top Ni source-drain electrodes that impede delivery of the chemical elements ($H_2$ and $N_2$) to the underlying barrier and island. The abundant traps in SiN film are generally obtained by N atoms substituted by Si atoms, producing silicon dangling bonds, referred to as *K*-center defects [13]. Other defects can be associated with the presence of hydrogen typically present in the Si-N structure [14]. It was shown that the number of defects can be reduced by high temperature (~1000°C) heat treatment of the layer or producing Si-rich compositions [13]. Another source of defects which need to be addressed is inadequate surface preparation.

## III. Conclusions

In conclusion, the MIM SETs featuring ALD $Si_3N_4$ as barrier dielectric are fabricated for the first time, to the best of our knowledge. Analysis of temperature dependence of conductance confirm the formation of MIM junctions with negligible in-series contribution of native surface oxide, in contrast with the NiO that is observed to parasitically form in MIM Ni-$SiO_2$-Ni junctions, [2, 3]. However, very large magnitude of observed RTS noise indicates a large density of traps inside the tunnel junctions. We are currently investigating high temperature and plasma treatments of the $Si_3N_4$ ALD layers and improved surface preparation to reduce the number of defects inside the junctions. Noise analysis technique proposed here can be also extended for characterization of various single-electron devices and identification of charged defects in these structures.

## Acknowledgment

Authors are grateful to Dr. Benoit Roche for useful discussions on the trap impact on the SET operation and general comments.

## References

[1] K. K. Likharev, "Single-electron devices and their applications," *Proceedings of the IEEE,* vol. 87, pp. 606-632, 1999. M. Fujii, T. Kita, S. Hayashi and K. Yamamoto, Journal of Physics: Condensed Matter 9 (41), 8669 (1997).

[2] G. Karbasian, M. S. McConnell, A. O. Orlov, S. Rouvimov, and G. L. Snider, "Experimental demonstration of single electron transistors featuring SiO2 plasma-enhanced atomic layer deposition in Ni-$SiO_2$-Ni tunnel junctions," *Journal of Vacuum Science & Technology A,* vol. 34, p. 01A122, 2016.

[3] G. Karbasian, A. O. Orlov, and G. L. Snider, "Fabrication of nanodamascene metallic single electron transistors with atomic layer deposition of tunnel barrier," *Journal of Vacuum Science & Technology B,* vol. 33, p. 06FG02, 2015.

[4] G. Karbasian, P. J. Fay, H. Xing, D. Jena, A. O. Orlov, and G. L. Snider, "High aspect ratio features in poly(methylglutarimide) using electron beam lithography and solvent developers," *Journal of Vacuum Science & Technology B,* vol. 30, p. 06FI01, 2012.

[5] M. Pierre, M. Hofheinz, X. Jehl, M. Sanquer, G. Molas, M. Vinet*, et al.*, "Background charges and quantum effects in quantum dots transport spectroscopy," *The European Physical Journal B,* vol. 70, pp. 475-481, 2009/08/01 2009.

[6] M. S. McConnell, L. C. Schneider, G. Karbasian, S. Rouvimov, A. O. Orlov, and G. L. Snider, "Atomic layer deposition of Al2O3 for single electron transistors utilizing Pt oxidation and reduction," *Journal of Vacuum Science & Technology A,* vol. 34, p. 01A139, 2016.

[7] C. W. J. Beenakker, "Theory of Coulomb-blockade oscillations in the conductance of a quantum dot," *Physical Review B,* vol. 44, pp. 1646-1656, 07/15/ 1991.

[8] M. J. Kirton and M. J. Uren, "Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (1/*f*) noise," *Advances in Physics,* vol. 38, pp. 367-468, 1989.

[9] M. Hofheinz, X. Jehl, M. Sanquer, G. Molas, M. Vinet, and S. Deleonibus, "Individual charge traps in silicon nanowires," *Eur. Phys. J. B,* vol. 54, pp. 299-307, 2006.

[10] K. Kandiah, M. O. Deighton, and F. B. Whiting, "A physical model for random telegraph signal currents in semiconductor devices," *Journal of Applied Physics,* vol. 66, pp. 937-948, 1989.

[11] H. C. George, M. Pierre, X. Jehl, A. O. Orlov, M. Sanquer, and G. L. Snider, "Application of negative differential conductance in Al/AlOx single-electron transistors for background charge characterization," *Applied Physics Letters,* vol. 96, p. 042114, 2010.

[12] G. Karbasian, "Fabrication of Metallic Single Electron Transistors Featuring Plasma Enhanced Atomic Layer Deposition of Tunnel Barriers," Doctor of Philosophy, Electrical Engineering, University of Notre Dame, 2015.

[13] E. Vianello, F. Driussi, P. Blaise, et al. , "Explanation of the charge trapping properties of silicon nitirde storage layers for NVMs," IEEE Trans. Electron Devices vol. 58, no. 8, pp. 2483–2499, Aug. 2011

[14] Ken'ichiro Sonoda, Eiji Tsukuda, Motoaki Tanizawa, and Yasuo Yamaguchi, " Electron trap level of hydrogen incorporated nitrogen vacancies in silicon nitride" J. Appl. Phys. 117, 104501 (2015).

# On the Scaling of Lanthanum Oxide Gate Dielectric Film into the Subnanometer EOT Range

Hei Wong and Jieqiong Zhang
Department of Electronic Engineering
City University of Hong Kong, Tat Chee Avenue
Kowloon, Hong Kong SAR
Email: heiwong@ieee.org

Xuan Feng and Danqun Yu
School of Information Science and Electronic Engineering
Zhejiang University, Zheda Road
Hangzhou, China

Hiroshi Iwai and Kuniyuki Kakushima
Interdisciplinary Graduate School of Science and Engineering
Tokyo Institute of Technology
Yokohama, Japan

***Abstract*—High-k gate dielectric integration had been one of the key technological boosters for 45 nm CMOS technology and beyond. Just a couple technology nodes after adopting the hafnium-based high-k materials, the high-k scaling have already lost its momentum. It is anticipated that the EOT scaling will be in the rate less than 0.03 nm reduction/generation in coming technology nodes. Putting aside the fabrication and reliability issues for high-k integration, high-k films in a couple nanometers are facing scalability issues. For half nanometer EOT gate dielectric, the physical thickness of high-k film will be less than 4 nm, large gate leakage will be encountered again. Meanwhile, the high-k/metal gate and high-k/silicon interfaces will be the primary constraint for achieving gate dielectric film in this EOT range. This work, taking $La_2O_3$ as example, demonstrates some of these issues related to the further subnanometer EOT scaling.**

***Keywords—high-k gate dielectric; subnanometer EOT; $La_2O_3$; interface reaction***

## I. INTRODUCTION

In downsizing the CMOS gate dielectric film, the reduction rate is far slower than that suggested by the constant field scaling rule and the technology roadmap prediction even in the sense of equivalent (silicon) oxide thickness (EOT) in the last decades [1]. The slow downsizing rate was first due to the physical thickness limit of bulk silicon dioxide and the less controllable atomic layer uniformity of ultrathin film in mass production [2]. These issues were overcome by introducing much thicker high-k metal oxide films [3-4]. However, the EOT reduction could only proceed by a couple tenths of a nanometer. The much poorer properties and less thermal stability of the metal oxides hindered the further EOT downsizing [1]. The ideal gate oxide EOT for 14 nm gate length technology should be less than half nanometer but the actual EOT used was still around 0.8 nm [5]. We need to produce thinner EOT for maintaining further device downsizing, boosting the device characteristics, and suppressing the "off current" of CMOS devices [6].

When scaling towards the subnanometer range, especially around half nanometer, it is an issue of whether technologically feasible rather than the issues related to characteristic, reliability, or variability degradation. The less scalable silicon/high-k and the metal gate/high-k interfaces pose the ultimate technology constraint on further EOT scaling [7-8]. In this paper, we shall discuss, taking lanthanum oxide ($La_2O_3$) as an example, the issues and challenges of fabricating subnanometer EOT gate dielectric. In Section II will be discussed some characteristics of high-k films in a couple nanometers thick. The interface material interaction at the Si/$La_2O_3$ and W/$La_2O_3$ interfaces that leading to the EOT degradation will be discussed in Section III.

## II. HIGH-K DIELECTRICS IN NANOMETER SCALE

When the high-k dielectric is scaled down to a couple nanometers, its challenge will be much server than the silicon oxide and silicon nitride of the same physical thickness. High-k oxides are often found to have much higher bulk trap (mainly the oxygen vacancies, and some cases the grain boundary states of high-k nanocrystallites)[9-10] than the silicon oxide ones, as a result the high-k film has much larger leakage current for same physical thickness. The advantage of "physically thicker" will be dismissed when the physical thickness of the high-k film is reduced to a couple nanometers. In addition, direct tunneling will take place in high-k films with thicknesses in this range as high-k materials have much smaller band offsets [1] with silicon and sometimes have lighter carrier effective masses [9-11] which made the direct tunneling to occur at thicker film. Figure 1 lists the estimated thicknesses for direct tunneling to occur for $HfO_2$ and $La_2O_3$ films. In principle, half nanometer EOT could be achieved with 3.5 nm thick $La_2O_3$, this thickness is far thinner than the direct tunneling limit of $La_2O_3$ as estimated. Note that the effective masses, taken from various sources [11-13], need some further confirmation. Data extracted from current-voltage characteristics usually are inaccurate. Theoretical data from first principle calculation may need to be calibrated in

some ways [11]. However, it is quite sure that the effective masses of different modifications can vary greatly [11]. Significant enhancement in gate leakage is expected as result of direct tunneling and trap-assisted conduction in the film.

| *EOT* (nm) ($SiO_2$ Thickness) | 1.0 | 0.7 | 0.5 |
|---|---|---|---|
| $La_2O_3$ Physical Thickness (nm) | 6.9 | 4.8 | 3.5 |

| Parameter | $SiO_2$ | $La_2O_3$ | $HfO_2$ |
|---|---|---|---|
| $\kappa$ | 3.9 | 27 | 24 |
| $\Delta E_C$ (eV) | 3.5 | 2.30 | 1.5 |
| $\Delta E_V$ (eV) | 4.4 | 2.6 | 3.4 |
| $m_e^*$ | 0.4 | 0.26 | 0.68 |
| $m_h^*$ | 0.33 | 0.5 | 0.29 |
| $t_{DT}$ (nm) | 3.0 | 4.6 | 3.5 |

$$EOT = \frac{\kappa_{ox}}{\kappa_{high-\kappa}} t_{high-\kappa}$$

$$t_{DT,high-k} = t_{DT,ox} \sqrt{\frac{m^*_{e,ox}\Phi_{B,ox}}{m^*_{e,high-k}\Phi_{B,high-k}}}$$

Fig. 1. Scaling high-k to subnanometer EOT will push the gate dielectric film to direct tunneling limit again as high-k metal oxides have much smaller band offsets with silicon.

## III. Interfacing with High-k

### A. Lanthanum oxide/silicon interface

Most high-k oxides can readily react with the interfacial silicon oxide or the silicon substrate [14-16]. Depending on the process temperature, partial pressure of oxygen, several different chemical reactions may take place (see Fig.2) [9, 14-16]. The reactions can lead to the formation of a silicate layer with much smaller k values. It becomes the critical constraint for half-nanometer EOT. For $HfO_2$ film, the proposed technique for suppressing the interface layer is the scavenging process [17-18]. By introducing some metals with positive Gibbs free energies and treated at sufficient high temperature, the interfacial $SiO_2$ or silicate layer can be scavenged and thus improves the EOT [17-18]. The scavenging process requires a high temperature (*e.g.* > 800 °C) which may cause some instability issues [1]. In addition, the required processing temperature is well above the available thermal budget in general. For $La_2O_3$/Si stack, no scavenging phenomenon has been reported so far. Instead, it is often reported that a high-temperature treatment on the $La_2O_3$/Si stack could result in silicates formation via the calcinations process [1]. Figure 3 compares the cross section view of as-deposited W/$La_2O_3$/Si and with 600 °C annealing. A thick interface silicate layer was found in annealed sample. The existence of interface silicate bonding was confirmed with angle-resolved x-ray photoelectron spectroscopy (XPS) measurements. As depicted in Fig.4 taken from 600 °C thermal annealed sample, highly-distorted Si 1s XPS peak with notable energy shifts were observed near the $La_2O_3$/Si interface. Gaussian decomposition of the peak reveals that this XPS spectrum is constituted by Si-O bonding (with peak energy of 153.9 eV) and La-O-Si bonding (with peak energy of 150.8 eV). This silicate layer causes significant EOT degradation [15]. Unlike the $HfO_2$/Si stack where the interface silicate layer can be suppressed with the scavenging process, the interface silicate layer in the $La_2O_3$/Si stack is hard to be suppressed. The substrate Si can even be incorporated into the bulk $La_2O_3$. It was suggested the interfacial layer growth is a consequence of $La_2O_3$ and $SiO_2$ calcinations. Thus suppressing the interface oxidation such as reduce the amount of oxygen in ambient and in the metal gate should be an effective way to suppress the growth of interface silicate layer and the increase of gate dielectric EOT.

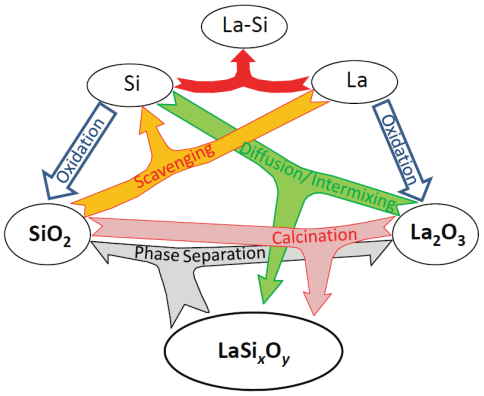
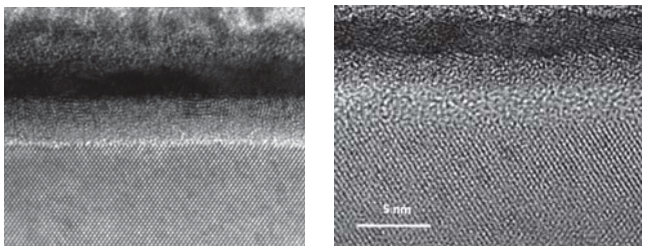



Fig. 2. Possible chemical reactions amongst Si, La, $SiO_2$, $La_2O_3$, and $LaSi_xO_y$. Direct reaction between $La_2O_3$ and Si, interface oxidation, and $SiO_2$/$La_2O_3$ calcination can lead to the formation of a complex oxide layer with a smaller k value. It becomes the lower bound for minimum EOT to be achieved. Adopted from [7].




**(a) As-deposited** **(b) 600 °C Annealed**

Fig. 3. A thick silicate layer at the $La_2O_3$/Si interface make the resulting film to have a much large EOT. TEM picture showing the layered structure of cross-section view of the W/$La_2O_3$/Si stack: (a) as-deposited sample with sharp interfaces; (b) annealed sample with a thick silicate layer at the $La_2O_3$/Si interface.

### B. Lanthanum oxide/metal gate interface

The interfacial layer at the high-k/metal gate interface may also cause the EOT degradation. The metal/high-k interface layer can be either an insulating or conducting layer [1]. Yet W/$La_2O_3$ stack is a good option in the sense of smaller EOT and other characteristics [19]. The TEM picture shown in Fig. 3(b) also reveals the existence of transition layer at W/$La_2O_3$ interface. XPS study on the W bonding states in this region indicates that the major bonding states are oxidized tungsten phases ($WO_x$) [19]. To perform more precise probing on the interface bonding states, the W layer was first thinning with Ar sputtering for 4.5 min. Then angle-resolved XPS measurement was conducted at take-off angle ranging from 0

to 90°. As shown in Fig. 5, in addition to the W 4f twin peaks at 31.5 and 33.5 eV for elemental W, additional board peaks were found in the energy ranging from 35 to 39 eV. These peaks were due to some oxidized W phases [19]. The signals of oxidized W peak become stronger at larger take-off angles indicating the presence of larger amount of oxidized states at the W/$La_2O_3$ interface. As $WO_x$ are conductive, it can be considered as part of W electrode and should not cause EOT degradation [1, 19]. However, if further thermal treatment is to be proceeded, the tungsten oxide may be reduced to some forms with lower oxidation states and the released oxygen will cause the $La_2O_3$/Si interface oxidation and results in an increase of EOT as mentioned in Sec. IIIA. In addition, when the sample was subjected to thermal annealing at 600 °C, W-O-La bonding was found. As shown in Fig.6, the La 3d XPS taken near the W/$La_2O_3$ interface is highly skewed. Gaussian decomposition of the spectrum indicates that there is a peak at energy of 855 eV. This peak was assigned to the La-O-W bonding []19] which may cause the EOT degradation and needs to be taken care in half nanometer EOT film.

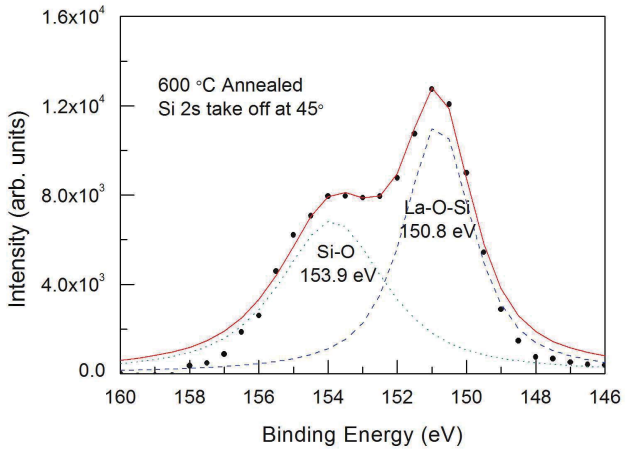



Fig. 4. Angle-resolved Si 2s XPS taken at $La_2O_3$/Si interface showing significant amount of silicate bonding.

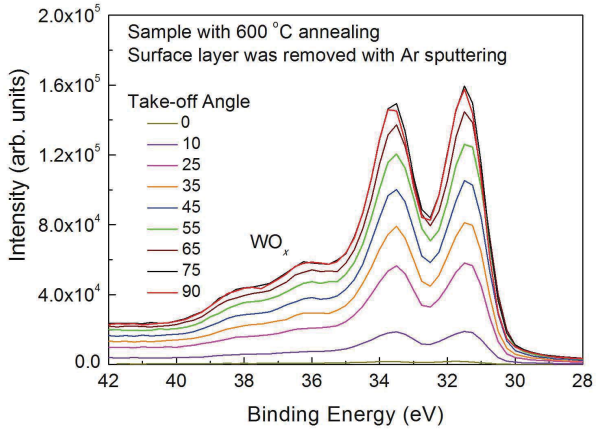



Fig. 5. Typical W 4f XPS spectra at different depths showing strong $WO_x$ peaks at the W/$La_2O_3$ interface. The sample was thermally annealed at 600 °C for 30 min.

## IV. Conclusion

The introduction of high-k material has enabled the production of subnanometer EOT gate dielectric film for recent technology nodes. However, the gate dielectric EOT scaling been slowed down again. From device performance point of view, scaling of high-k film into half-nanometer EOT, which will be used in 6 nm gate length devices, will push the physical thickness of the high-k film into direct tunneling range and that gives rise a significant increase in the gate leakage current. From process point of view, the high-k/Si and high-k/metal gate interfaces have become the predominant limiting factor in achieving half-nanometer EOT. For $La_2O_3$ data presented in this work, interface reactions which lead to the significant increase of EOT were found for sample with 600 °C thermal annealing. In that sense, better interface control will be more important than the introduction of even higher k value materials. It is a great challenge for achieving gate dielectric with EOT in the half nanometer range.

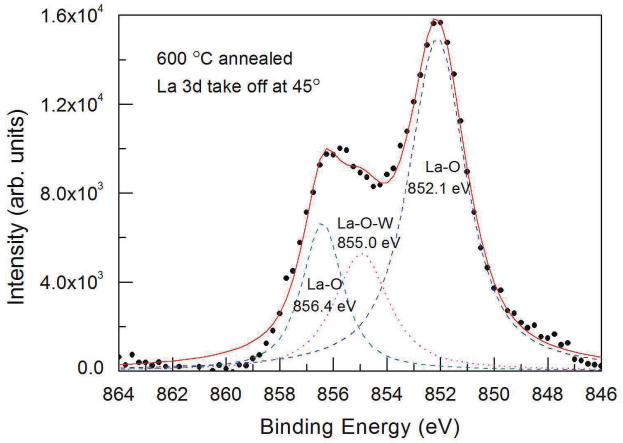



Fig. 6. Gaussian decomposition of the La 3d XPS near the W/$La_2O_3$ interface reveals the La-O-W bonding. The sample was annealed at 600 °C for 30 min.

## Acknowledgment

This work is supported by the National Natural Science Foundation of China under the grant No. 61376111.

## References

[1] H. Wong, and H. Iwai, "On the scaling of subnanometer EOT gate dielectrics for ultimate nano CMOS technology," Microelectron. Engineer., vol. 138, pp. 57-76, 2015.

[2] H. Wong, and H. Iwai, "On the scaling issues and high-k replacement of ultrathin gate dielectrics for nanoscale MOS transistors," Microelectron. Engineer., vol. 83, pp. 1867-1904, 2006.

[3] C. Fiegna, H. Iwai, T. Wada, T. Saito, E. Sangiorgi, B. Riccò, "A new scaling methodology for the 0.1-0.25µm MOSFET", Tech. Dig. Sympo. VLSI Technology, pp.33-34, May, 1993, Kyoto, Japan.

[4] H. Iwai, S. Ohmi, S. Akama, C. Ohshima, I. Kashiwagi, A. Kikuchi, J. Taguchi, H. Yamamoto, I. Ueda, A. Kuriyama, J. Tonotani, Y. Kim, Y. Yoshihara, H. Ishiwa, "High dielectric constant gate insulator technology using rare earth oxides", in S. Kar, D. Misra, R. Singh, F.

Gonzalez, Ed. Proc. Int. Symp., Physics and Technology of High-k Dielectrics I, 202th ECS Meeting, pp.27-40, October 2002.

[5] Intel 14 nm technology. http://www.intel.com/content/www/us/en/siliconinnovations/intel-14nm-technology.html.

[6] K. Kakushima, K. Tachi, P. Ahmet, K. Tsutsui, N. Sygii, and T. Hattori, "Advantage of further scaling in gate dielectric below 0.5 nm of equivalent oxide thickness with $La_2O_3$ gate dielectrics," Microelectron. Reliab., vol.50, pp.790-793, 2010.

[7] H. Wong, J. Zhang, S. Dong, K. Kakushima, and H. Iwai, "Thermal annealing, interface reaction, and lanthanum-based sub-nanometer EOT gate dielectrics," Vacuum, vol. 118, pp. 2-7, 2015.

[8] D. J. Lichtenwalner, J. S. Jur, A. I. Kingon, M. P. Agustin, Y. Yang, S. Stemmer, L. V. Goncharova, T. Gustafsson, and E. Garfunkel, "Lanthanum silicate gate dielectric stacks with subnanometer equivalent oxide thickness utilizing an interfacial silica consumption reaction," J. Appl. Phys., vol.98, art. No. 024314, 2005 .

[9] H. Wong, H. Iwai, K. Kakushima, B. L. Yang, and P. K. Chu, "XPS study of the bonding properties of lanthanum oxide/silicon interface with a trace amount of nitrogen incorporation," J. Electrochem. Soc., vol. 157, pp. G49-G52, 2010.

[10] H. Wong, Nano-CMOS Gate Dielectric Engineering, CRC Press, Boca Raton, 2012

[11] T.V. Perevalov, V.A. Gritsenko, S.B. Erenburg, A.M. Badalyan, H. Wong, C.W. Kim, "Atomic and electronic structure of amorphous and crystalline hafnium oxide: x-ray photoelectron spectroscopy and density functional calculations," J. Appl. Phys., vol.101, art. No. 053704, 2007.

[12] S. Monaghan, P.K. Hurley, K. Cherkaoui, M.A. Negara, A. Schenk, "Determination of electron effective mass and electron affinity in $HfO_2$ using MOS and MOSFET structures," Solid-State Electron., vol.53, pp.438–444, 2009.

[13] C.L. Hinkle, C. Fulton, R.J. Nemanich, G. Lucovsky, "A novel approach for determining the effective tunneling mass of electrons in $HfO_2$ and other high-K alternative gate dielectrics for advanced CMOS devices," Microelectron. Engineer. vol.72, pp. 257-262, 2004.

[14] H. Yamada, T. Shimizu and E. Suzuki, "Interface reaction of a silicon substrate and lanthanum oxide films deposited by metalorganic chemical vapor deposition," Jpn. J. App. Phys., vol.41, pp.L368-370, 2002.

[15] T. Kawanago, Y. Lee, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, and H. Iwai, "EOT of 0.62 nm and high electron mobility in La-silicate/Si structure based nMOSFETs achieved by utilizing metal-inserted poly-Si stacks and annealing at high temperature," IEEE Trans. Electron Devices, vol. 59, pp. 269-276, 2012.

[16] J. Zhang, H. Wong, D. Yu, K. Kakushima, and H. Iwai, "X-ray photoelectron spectroscopy study of high-k $CeO_2/La_2O_3$ stacked dielectrics," AIP Advances, vol. 4, art. No. 117117, 2014.

[17] T. Ando, M.M. Frank, K. Choi, C. Choi, J. Bruley, M. Hopstaken, M. Copel, E. Cartier, A. Kerber, A. Callegari, D. Lacey, S. Brown, Q. Yang, V. Narayanan, "Understanding mobility mechanisms in extremely scaled $HfO_2$ (EOT 0.42 nm) using remote interfacial layer scavenging technique and Vt-tuning dipoles with gate-first process," in: Tech. Dig. International Electron Device Meeting, Washington, DC, USA, 7–9 December 2009, pp. 423–426.

[18] M. Copel, S. Guha, N. Bojarczuk, E. Cartier, V. Narayanan, V. Paruchuri, "Interaction of $La_2O_3$ capping layers with $HfO_2$ gate dielectrics," Appl. Phys. Lett., vol.95, art. No. 212903, 2009.

[19] H. Wong, J. Zhou, J. Zhang, H. Jin, K. Kakushima, H. Iwai "The interfaces of lanthanum oxide-based subnanometer EOT gate dielectrics," Nano Research Lett., vol.9, art. No.472, 2014.

# Electrical Characterization of Random Telegraph Noise in Back-Biased Ultrathin Silicon-On-Insulator MOSFETs

Carlos Marquez, Noel Rodriguez, Francisco Gamiz
Department of Electronics, CITIC-UGR
University of Granada
18071, Granada, Spain
Email: carlosmg@ugr.es

Akiko Ohata
Collaboration Center for Research and Development
Utsunomiya University, Japan

***Abstract*—Random Telegraph Noise (RTN) has been studied in ultrathin SOI MOSFET by introducing a new protocol which aims to identify unequivocally the single-trap RTN signals in optimum bias conditions for its electrical characterization. The methodology combines a modified Weighted Time Lag Plot algorithm assisted with $1/f$ spectral scanning by gate bias. The procedure has been applied to study the influence of the back-gate bias on the RTN characteristics of the SOI devices with coupled front and back interfaces, revealing unusual characteristics compatible with the trap escaping to the gate metal contact.**

## I. Introduction

Random Telegraph Noise (RTN) remains as a critical constrain when the characteristic dimensions of the semiconductor devices are shrunk to the deca-nanometer range [1], [2]. Paired with the decrease of the signal levels, the introduction of Ultrathin Silicon-On-Insulator substrates also entails the appearance of additional effects related with the electrostatic coupling between the top-channel and the Si-film/BOX interfaces [3], [4]. Substrate bias is one of the more relevant applications of interface coupling (great importance for mobility boosting, $V_T$ tuning... [5]), but its role on the RTN characteristics has not been fully studied yet [6], [7]. A systematic measuring protocol, to cope with the new challenges of RTN characterization, has been introduced based on a modified Weighted Time Lag Plot (WTLP) approach combined with the Spectral Scanning by Gate Bias (SSGB). This method allows the selection of single traps, identifying the best operation region to characterize the RTN signature under substrate bias conditions.

## II. Characterization Method

The characterization setup is based on an Agilent B1517A high resolution Source-Measurement-Unit (SMU) monitoring repeatedly the drain current during periods of $400s$ at a $2ms$ sampling-rate (the schematic is shown in Figure 1.a). The acquisition periods were repeated until a minimum number of 100 transitions in the current signal were captured to guarantee the significance of the statistics. The 1/f noise is characterized by using a low noise current amplifier connected to a software-based spectrum analyzer through a high resolution A/D converter (Figure 1.b). High-$k$ metal-gate SOI nMOSFETs, fabricated at CEA-LETI in a 22nm process, were selected for the experiments [8]. The transistors feature an ultrathin body of $t_{Si} = 7nm$, Buried-OXide (BOX) thickness of $t_{BOX} = 145nm$, gate length of $L = 100nm$ and gate width of $W = 80nm$. The hafnium-based gate oxide has an equivalent oxide thickness (EOT) of $t_{EOT} = 1.3nm$.

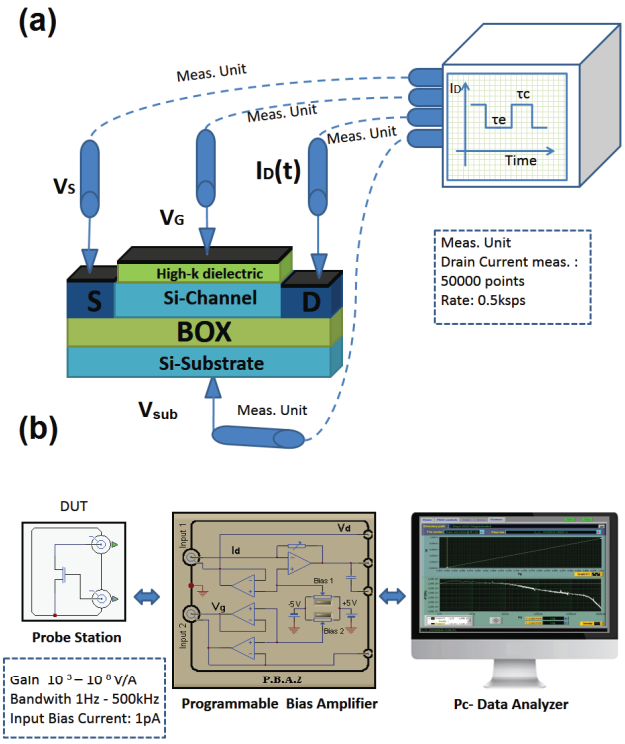



Fig. 1. (a) Schematic of the experimental setup developed for the RTN measurements. Each transistor terminal is monitored by an Agilent B1517A SMU at a rate of 500 samples per second. (b) Schematic of the $1/f$ measurement setup based on a programmable low-noise amplifier.

ISBN 978-1-4673-8608-1

IEEE Catalog number CFP1649D-USB

## III. Experiments and Discussion

Identifying the RTN signals corresponding to single traps is one of the most challenging task during its electrical characterization. Examples of drain current, affected by RTN, measured as a function of time are shown in Figure 2 for different devices. When two current levels are clearly detected (revealing the existence of a single active trap, Figure 2.a), the time at the high- and low-current states, in average, corresponds to the capture ($\tau_c$) and emission ($\tau_e$) time respectively [9]. However, the selection of single traps is not straight forward in cases as the one shown in Figure 2.b, where the drain current of several devices is monitored revealing different multi-trapping events.

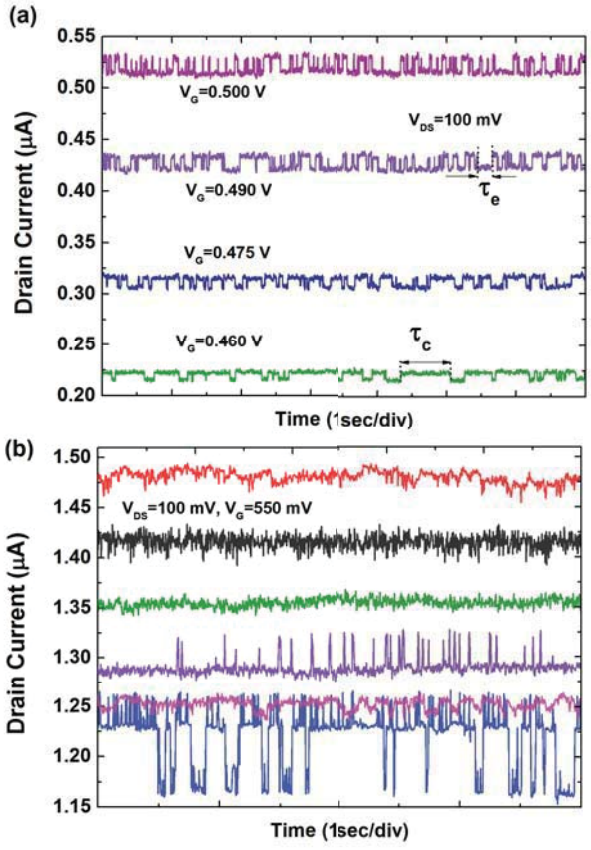



Fig. 2. Drain current signal presenting RTN as a function of time for different gate voltages. (a) Device with clear single active trap. (b) Devices with possible multi-trap situation.

The determination of the traps of interest can be carried out unambiguously by a modified version of the Time Lag Plot method (TLP) partially based on the approach described in [10] and [11]. Each point of the TLP space (events) $(I_D(i), I_D(i+1))$ is weighted by the *appearance* function, $\mathcal{A}(I_D(i), I_D(i+1))$, which accounts for the number of events inside a certain circle of the TLP space:

$$\mathcal{A}(I_D(i), I_D(i+1)) = \sum_{j=1}^{N-1} \xi(I_D(j), I_D(j+1)) \quad (1)$$

where,

$$\xi(I_D(j), I_D(j+1)) = \\ = \begin{cases} 1 \text{ if } d\{[I_D(j), I_D(j+1)], [I_D(i), I_D(i+1)]\} \leq r \\ 0 \text{ if } d\{[I_D(j), I_D(j+1)], [I_D(i), I_D(i+1)]\} > r \end{cases} \quad (2)$$

$N$ is the total number of samples inside the time frame analyzed; $d\{.,.\}$, is the Euclidean distance function; and $r$ is appearance radius, $r = 10^{-6}\sigma\ (A)$ (with $\sigma$ the standard deviation of the samples within the time frame).

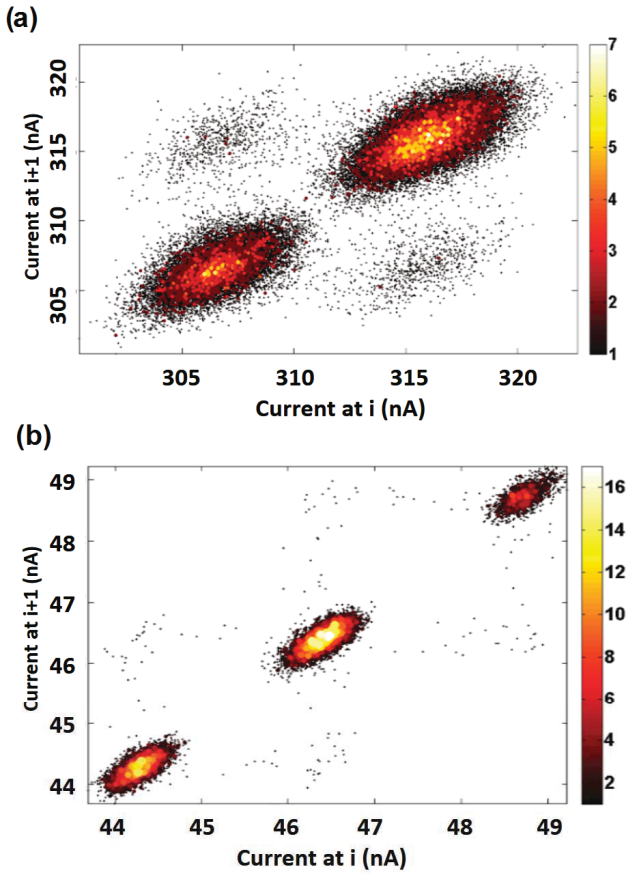



Fig. 3. Weighted TLP of the drain current signal: (a) transistor of Figure 2.a with $V_G = 0.475V$ where two lobes (states) result of the single active trap are clearly shown. (b) Three lobes identifying the characteristic signature of two traps.

This sample-weighted approach of the conventional Time Lag Plot method allows to identify the RTN levels clearly as populated regions in the diagonal of the TLP space, while populated regions outside the diagonal are related to the transitions between states. In Figure 3, we show results of the application of the method. Two lobes indicate the presence of

a single trap (Figure 3.a) whereas the results in Figure 3.b reveal the existence of three predominant current levels (two traps).

Identifying single trap RTN also requires the proper selection of the gate bias range where the characteristic times of the trap ($\tau_c$, $\tau_e$) are similar enough to each other so the transition events between states can be observed in a reasonable time frame. This can be facilitated by obtaining the $1/f$ curve for a given bias (preferentially close to the threshold voltage, Figure 4. Inset). The corner frequency is determined by the sum of the inverse of the characteristic times ($f_c = 1/\tau_e + 1/\tau_c$) [12]. Once the corner frequency is located, the spectral density of the current noise, $S_I$, is measured while $V_G$ is swept leading to a $S_I - V_G$ curve as shown in Figure 4 (Spectral Scanning by Gate Bias, SSGB). The bell shaped characteristic identifies the bias range where the RTN will be easily observable ($V_G \in$[0.42V, 0.56V] for this particular case).

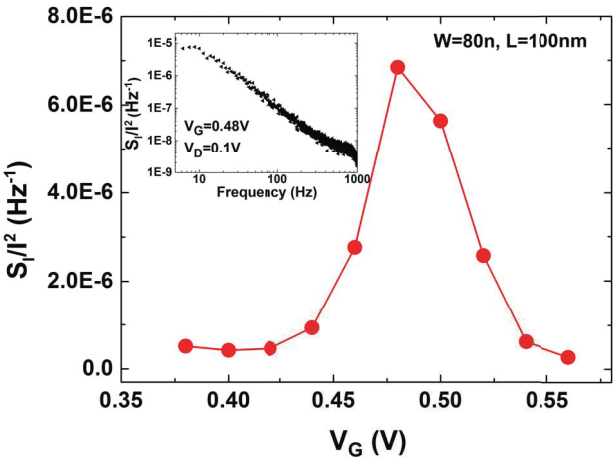



Fig. 4. Normalized current noise power $S_I$ dependence with the $V_G$ (SSGB) for the transistor shown in Figure 2.a). Inset: $S_I$ vs. Frequency for the same device at a given bias point.

Figure 5 shows typical $\tau_c/\tau_e$ ratios used to extract the physical parameters of the traps ( [13]) for two different samples when a substrate bias is applied; the front gate overdrive voltage range is selected with the SSGB procedure previously described. As observed, although the curves are presented as a function of the overdrive voltage (note that $V_T$ will be modified by $V_{SUB}$ when the back interface is in depletion), the $\tau_c/\tau_e$ ratio depends on the particular value of $V_{SUB}$ (despite that the inversion charge is the same in all cases). Note also that this dependence on $V_{SUB}$, for a given inversion charge, is different for the particular trap considered (Figure 5.a vs. 5.b).

Figure 6 shows the values of $\tau_c$ and $\tau_e$ as a function of the overdrive voltage for the previous devices. From the analysis of this plot we can appreciate that for a given overdrive voltage, the capture time ($\tau_c$) decreases whereas the emission time ($\tau_e$) increases as $V_{SUB}$ increases.

From Figure 6 one may also notice that this behavior is

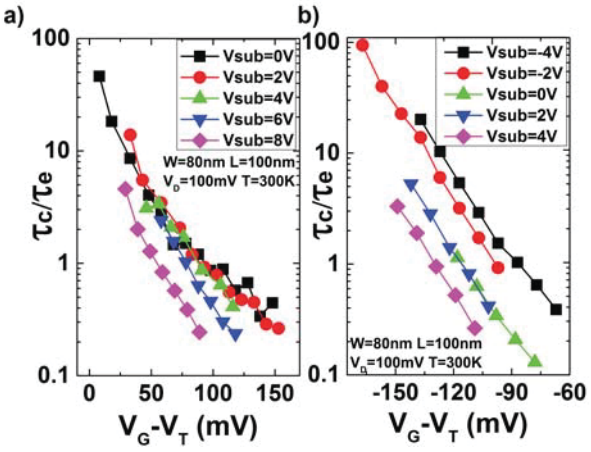



Fig. 5. $\tau_c/\tau_e$ ratios respect to the gate overdrive bias for different negative and positive substrate biases. Results from two different devices (a) and (b) and the same physical dimensions.

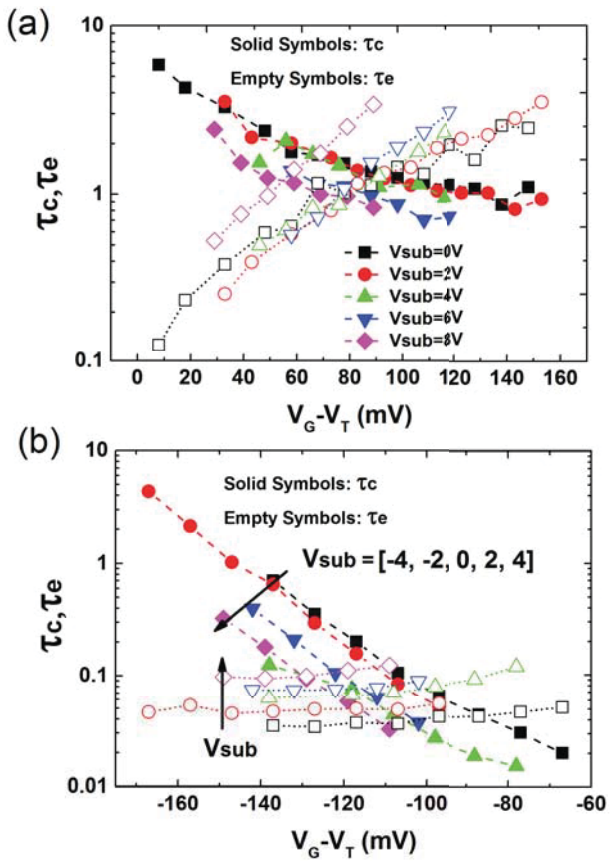



Fig. 6. $\tau_c$ and $\tau_e$ ratios respect to the gate overdrive for different substrates biases in the same devices than in Fig. 5.

observed both for attractive (linear dependence of $\tau_c$ and $\tau_e$ with the gate bias, Figure 6.a) or neutral traps (linear dependence of $\tau_c$ and constant value $\tau_e$ with the gate bias, Figure 6.b) [14]. This effect is contrary from the one we may expect considering classical RTN models relying on the

inversion charge and the possible intensification of the role of the electric field in the Si-film while increasing the substrate bias [15]. In contrast, these results are compatible with the fact that the trap is escaping to the metal gate contact since, for this mechanism, the lower the electric field intensity in the gate oxide, the larger the probability of the trap to be filled [16].

## IV. Conclusion

We have introduced an exhaustive method to identify experimentally, single-trap Random Telegraph Noise by combining the modified Weighted Time Lag Plot method (w-TLP) with the $1/f$ Spectral Scanning by Gate Bias technique (SSGB). The characterization procedure has been implemented in ultrathin SOI MOSFETs when a substrate bias is applied. The results show a non-intuitive tendency leading to an increase of the emission time (decrease of capture time) when the electric field in the film is relaxed by increasing the substrate bias, for a given inversion charge. However this behavior could be explained by the trap escaping to the gate metal contact.

## Acknowledgment

The authors would like to thank Dr. O. Faynot and Dr. F. Andrieu from CEA-LETI for sample supplying. This work has been partially funded by Spanish Government through project TEC-2014-59730, the BBVA-Spain Foundation for the "Ayudas para Investigadores y Creadores Culturales" program and the European Union under project WAYTOGO FAST.

## References

[1] M.-H. Tsai and T.-P. Ma, "The impact of device scaling on the current fluctuations in MOSFET's," *IEEE Transactions on Electron Devices*, vol. 41, no. 11, pp. 2061–2068, 1994.

[2] P. Fantini, A. Ghetti, A. Marinoni, G. Ghidini, A. Visconti, and A. Marmiroli, "Giant Random Telegraph Signals in Nanoscale Floating-Gate Devices," *IEEE Electron Device Letters*, vol. 28, no. 12, pp. 1114–1116, 2007.

[3] A. Ohata, J. Pretet, S. Cristoloveanu, and A. Zaslavsky, "Correct biasing rules for virtual DG mode operation in SOI-MOSFETs," *IEEE Trans. on Electr. Dev.*, vol. 52, no. 1, pp. 124–125, 2005.

[4] S. Eminente, S. Cristoloveanu, R. Clerk, A. Ohata, and G. Ghibaubo, "Ultra-thin fully-depleted SOI MOSFETs: special charge properties and coupling effects," *Solid-State Electronics*, vol. 51, no. 2, pp. 239–244, 2007.

[5] N. Rodriguez, S. Cristoloveanu, and F. Gamiz, "Evidence for mobility enhancement in double-gate silicon-on-insulator metal-oxide-semiconductor field-effect transistors," *Journal of Applied Physics*, vol. 102, no. 8, p. 083712, 2007.

[6] K. Akyel, L. Ciampolini, O. Thomas, D. Turgis, and G. Ghibaudo, "UTBB FD-SOI front- and back-gate coupling aware random telegraph signal impact analysis on a 6T SRAM," in *2014 SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, Oct. 2014, pp. 1–2.

[7] J. Nishimura, T. Saraya, and T. Hiramoto, "Statistical comparison of random telegraph noise (RTN) in bulk and fully depleted SOI MOSFETs," in *Ulis 2011 Ultimate Integration on Silicon*. IEEE, Mar. 2011, pp. 1–4.

[8] R. Ranica, A. Villaret, C. Fenouillet-Beranger, P. Malinge, P. Mazoyer, P. Masson, D. Delille, C. Charbuillet, P. Candelier, and T. Skotnicki, "A capacitor-less DRAM cell on 75nm gate length, 16nm thin fully depleted SOI device for high density embedded memories," in *IEEE Symposium on VLSI technology digest of technical papers*, 2004, pp. 128–129.

[9] M. J. Uren, D. J. Day, and M. J. Kirton, "1/f and random telegraph noise in silicon metal-oxide-semiconductor field-effect transistors," *Applied Physics Letters*, vol. 47, no. 11, p. 1195, 1985.

[10] T. Nagumo, K. Takeuchi, S. Yokogawa, K. Imai, and Y. Hayashi, "New analysis methods for comprehensive understanding of Random Telegraph Noise," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009.

[11] J. Martin-Martinez, J. Diaz, R. Rodriguez, M. Nafria, and X. Aymerich, "New Weighted Time Lag Method for the Analysis of Random Telegraph Signals," *IEEE Electron Device Letters*, vol. 35, no. 4, pp. 479–481, Apr. 2014.

[12] Z. Shi, J. P. Mieville, and M. Dutoit, "Random telegraph signals in deep submicron n-MOSFET's," *IEEE Transactions on Electron Devices*, vol. 41, no. 7, pp. 1161–1168, 1994.

[13] M. J. Kirton and M. J. Uren, "Capture and emission kinetics of individual Si:SiO2 interface states," *Applied Physics Letters*, vol. 48, no. 19, p. 1270, 1986.

[14] M. Schulz, "Coulomb energy of traps in semiconductor space-charge regions," *Journal of Applied Physics*, vol. 74, no. 4, pp. 2649–2657, 1993.

[15] H.-K. Lim and J. Fossum, "Threshold voltage of thin-film Silicon-on-insulator (SOI) MOSFET's," *IEEE Transactions on Electron Devices*, vol. 30, no. 10, pp. 1244–1251, 1983.

[16] X. Ji, Y. Liao, C. Zhu, J. Chang, F. Yan, Y. Shi, and Q. Guo, "The physical mechanisms of IG Random Telegraph Noise in deeply scaled pMOSFETs," in *2013 IEEE International Reliability Physics Symposium (IRPS)*. IEEE, Apr. 2013, pp. XT.7.1–XT.7.5.

# 1/f -Noise Characteristics of AlGaN/GaN Omega shaped Nanowire FETs

Sindhuri Vodapally[1], Chul-Ho Won[1], In-Tak Cho[3],Jong-Ho Lee[3], Youngho Bae[4],
Sorin Cristoloveanu[5], Ki-Sik Im[1, 2], and Jung-Hee Lee[1]*
[1]School of Electronics Engineering and [2]Institute of Semiconductor Fusion Technology,
Kyungpook National University, Daegu 702-701, Korea
[3]School of Electrical Engineering and Computer Science, Seoul National University, Seoul 151-742, Korea
[4]Department of Electronics Engineering, Uiduk University, Gyeongju 780-713, Korea
[5]Institute of Microelectronics, Electromagnetism and Photonics, Grenoble Polytechnic Institute, Grenoble 38016, France
*Email: jlee@ee.knu.ac.kr**

***Abstract* — The AlGaN/GaN omega-shaped nanowire FETs with different nanowire widths (W) have been fabricated. The effects of varying W on the performance of AlGaN/GaN omega-shaped nanowire FETs were investigated using low frequency noise (LFN) measurement. It was found that the noise characteristics of the device with narrow W show improved noise performances due to the accumulation of electrons in the volume of the nanowire which constricts the electron trapping in GaN layer. This volume accumulation of electrons is responsible for the mobility fluctuations because it decreases the probability of channel electrons at surface being captured into the surface traps, and also high carrier concentration screens the effective trapping of electrons in the volume of the nanowire. Whereas, width increases the LFN characteristics tended to be dominated by the carrier number fluctuation because the fin is too wide for volume accumulation and are subjected to the bulk trapping.**

***Keywords— AlGaN/GaN; heterostructure; omega-FET; 1/f noise characteristics; carrier confinement***

## I. INTRODUCTION

Gallium nitride (GaN) have an excellent potential for high frequency and high voltage operations due to its outstanding material properties, such as large band gap, high critical field, and high saturation electron velocity [1]. AlGaN/GaN fin-shaped field-effect transistors (FinFETs) benefit from enhanced gate control of the channel, which results in remarkable on-state and off-state performances [2- 6]: low off-state leakage, high on-state current, low subthreshold swing (SS), and high linearity operation [6].

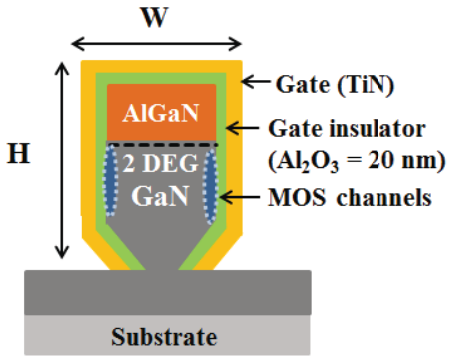
Recently, omega-shaped AlGaN/GaN FinFETs exhibiting superior off-state performances were demonstrated by our group, for the first time [7].The entire active regions of these devices were surrounded by the gate metal except the very narrow neck regions and hence effectively separated from the underlying thick GaN buffer layer, which resulted in excellent on- and off-state performances due to the greatly enhanced gate controllability. This device features 2DEG conduction at the AlGaN/GaN interface and sidewall MOS conduction along the fin sidewalls.

Low frequency noise measurements are important for reliability of semiconductor devices and also evaluating the nature of defects [8]-[9]. Several groups had already conducted the study on the *1/f* noise in AlGaN/GaN heterostructure FET (HFETs) [8]-[10], metal-oxide-semiconductor HFETs (MOSHFETs) [11] and FinFETs [12].

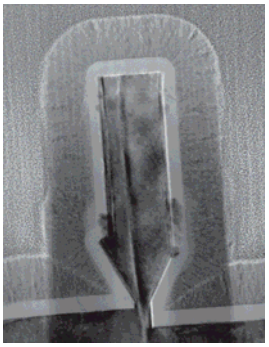
In this work, the AlGaN/GaN omega-shaped nanowire FETs with different nanowire widths (W) have been fabricated and their 1/f noise characteristics have been analyzed for the first time to understand the carrier confinement effect and the related trapping behavior in the volume of the nanowires as well as at the surface channel regions.

## II. DEVICE FABRICATION

AlGaN/GaN heterostructure was grown by metal organic chemical vapor deposition (MOCVD) on sapphire substrate. Firstly, $SiO_2$ mask was patterned by e-beam lithography on the active region of the device and then, the nanowire was defined by transformer-coupled plasma reactive ion etching (TCP-RIE) using a $BCl_3/Cl_2$ gas mixture. Then, tetramethylammonium hydroxide (TMAH) wet etching (5% of solution at 90 °C) was directly applied for 30 min. TMAH not only eliminates the plasma damage occurred during the plasma etching, but also narrows the fin width and the fin shape changed from a wide trapezoid to a narrow rectangle with very steep side-wall surfaces. ALD $HfO_2$ layer was then deposited and etched away leaving the $HfO_2$ spacer layer on the sidewalls. A second GaN etching and TMAH wet etching was employed to partially etch the GaN layer to form an omega-shaped nanowire structure. The TMAH wet etching was carried out for 10 hrs and the sidewall $HfO_2$ spacer effectively protects the narrow nanowire during long lateral etching time in TMAH solution. Then, the sidewall $HfO_2$ spacer was removed to deposit 20 nm-thick $Al_2O_3$ layer and 50 nm-thick TiN as a gate dielectric and gate metal, respectively was deposited using ALD. The schematic and TEM images of AlGaN/GaN omega-shaped nanowire FinFETs is shown in Fig. 1(a) and (b). The fabricated nanowire FETs has W from 70 to 200 nm, nanowire height (H) of 200 nm, and 36 number of nanowires.




(a)



(b)

Fig.1 (a): Schematic illustration of the omega-shaped FinFETs, (b): Cross-sectional TEM image of the omega-shaped FinFETs.

## III. Results and Discussion

The semi-log $I_{ds}$-$V_{gs}$ characteristics of the AlGaN/GaN nanowire omega-FETs with 70 and 200 nm fin width are shown in Fig. 2. Both devices exhibit extremely low off-state leakage current as low as $10^{-11}$ mA, low SS value, and high $I_{ON}/I_{OFF}$ ratio (~$10^{10}$ orders). These excellent performances attributes not only the enhanced gate controllability caused by the Ω-shaped gate structure, and fully depletion of the channel, but also the active region was completely separated from the underlying thick GaN buffer layer by a very narrow neck (5 nm) as discussed before [7]. In addition, the threshold voltage ($V_{th}$) of the nanowire FET gradually shifts to positive direction as the W becomes narrow. This attributed to high negative gate voltage is essential to deplete the channel. However, the current contribution from the sidewall MOS channel is significant when the W is narrow and the two dimensional electron gas (2DEG) channel current at the AlGaN/GaN interface dominates as the W increases [5].

Low-frequency noise (LFN) is measured with a spectrum analyzer Agilent 35670A at $V_{ds}$ = 0.1 V, varying $V_{gs}$. The study of low-frequency characteristics based on carrier number fluctuation (CNF) and carrier mobility fluctuation (CMF) models [13] in AlGaN/GaN FinFETs devices has been reported in refernce [12].

The normalized drain-current noise spectral density $(S_{Id}/I_d^2)$ as a function of nanowire width (W), measured at $V_{ds}$ = 0.1 V (ohmic region) at f = 10 Hz is shown in Fig. 3. It was found that the noise magnitude $(S_{Id}/I_d^2)$ increases as the fin W increases. This is because the number of traps increases as the volume of the active region increases [14].

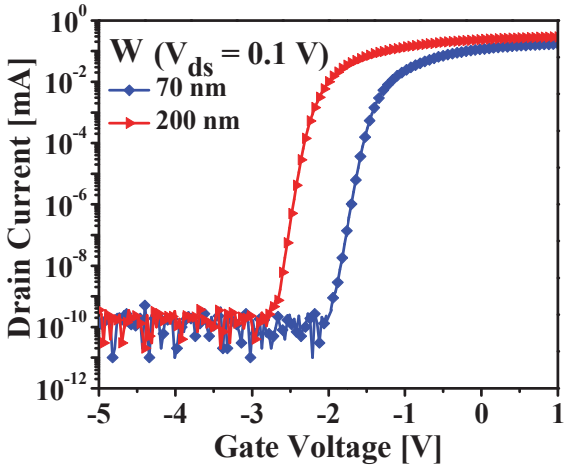



Fig.2: $I_d - V_{gs}$ characteristics according to the fin $V_{ds}$= 0.1 V.

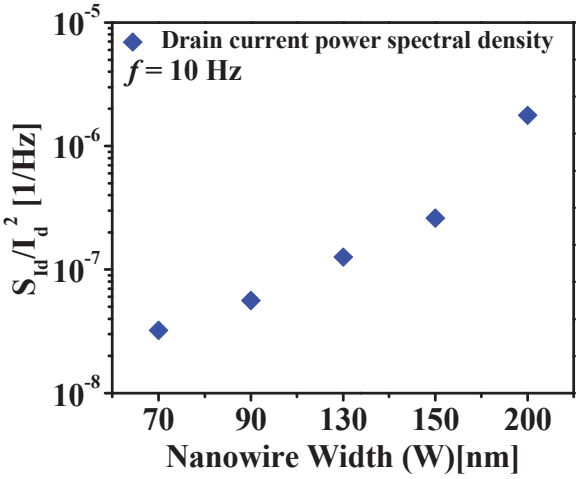



Fig.3: Normalized drain current spectral density ($S_{Id}/I_d^2$) versus frequency in the fabricated AlGaN/GaN omega-FET with different in widths ($W$) at $V_{ds}$ = 0.1 V, $V_{gs}$ - $V_{th}$ = 0.4 V.

Figure. 4 shows the apparent trap density ($N_t$) according to the fin width extracted from the Mc Whorter theory (CNF model developed by Ghibaudo) [13];

$$\frac{S_{Id}}{I_d^2} = \left(\frac{g_m}{I_d}\right)^2 S_{Vfb}$$

Where $S_{Vfb}$ is the power spectral density of flatband voltage fluctuations, with $N_T$ is the density of traps [9]. It was observed that, the effective trap density consistently increases according to the fin W, which explicitly points out that the number of traps increases as the fin width increases. A density

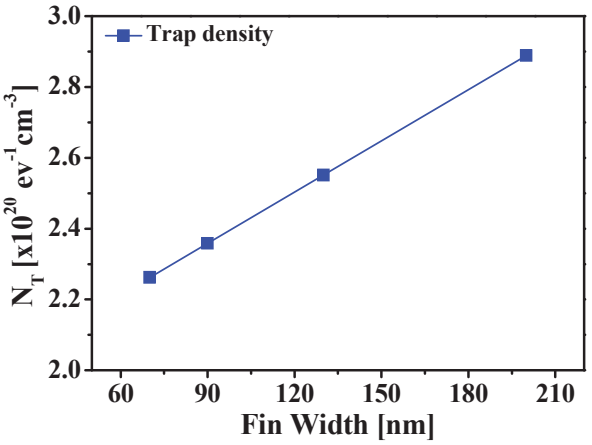



Fig.4: Effective trap density ($N_T$) versus fin width ($W$) at $V_{ds}$ = *0.1 V*.

$N_T$ of ~ $2\times10^{20}$ eV$^{-1}$ cm$^{-3}$ and $3\times10^{20}$ was extracted from the device with W= 70 nm and 200 nm devices, respectively.

In addition, Hooge parameter ($\alpha_H$) is also calculated using the equation [15],

$$\alpha_H = fWLC_{ox}\left(V_{gs} - V_{th}\right)^{S_{ID}}\Big/_{qI_d^2}$$

A value of $10^0$ was obtained for device with wide W and $10^{-1}$ for device with narrow W. The large the $\alpha_H$ indicates that the carrier number fluctuation is involved [16].

More informative results were obtained by plotting $(S_{Id}/I_d^2)$ versus $I_d$ as shown in Figure 5. It is noticed that the $(g_m/I_d)^2$ is much higher than $S_{Id}/I_d^2$ and varies proportionally with $1/I_d$ for the device with narrow W. These facts act against the CNF model and it follows that the dominant source of noise is unequivocally the carrier mobility fluctuation [17]. In the device with narrow W, the conduction band energy across the nanowire is significantly lowered due to the overlap of the energy profile belonging to each sidewall surface which results in electron accumulation in the central part of the nanowire, similar to the volume inversion observed in Si-based fin-shaped FETs (FinFETs) [18]. This volume accumulation of electrons in the body can fill the traps, thus 2DEG electrons are less subject to bulk-trapping and the screening effect by volume electrons is responsible for the mobility fluctuations.

On the other hand, the $(S_{Id}/I_d^2)$ and $(g_m/I_d)^2$ for the device with wider W (W = 200 nm) has good correlation with each other ($S_{Vfb} \approx 1$). The LFN varies as $1/I_d^2$, and the noise saturation in weak accumulation is clearly visible. This explicitly points out that the noise is due to carrier number fluctuation. Here, the fin is too wide for volume accumulation to take place, thus the 2DEG electrons have higher probability of being captured in bulk traps that are typically located in the GaN layer. It is noticed that, $S_{Vfb} \approx 1$ from W = 200 nm and results in the higher trap density.

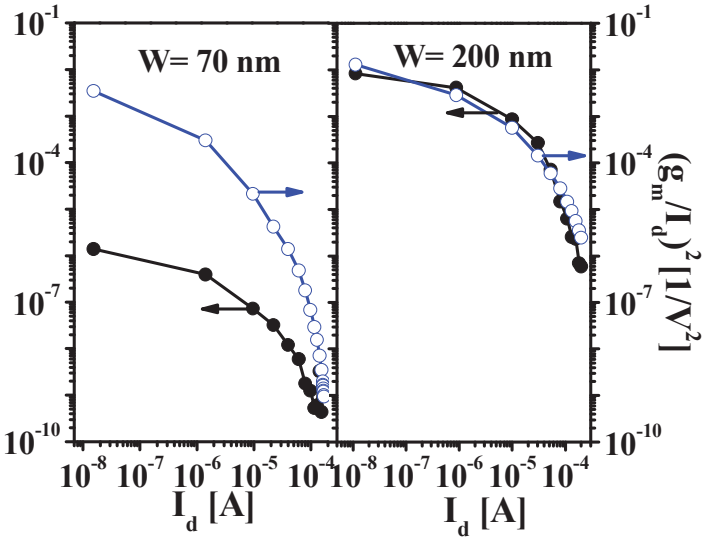



Fig.5: Averaged noise spectral density $(S_{Id}/I_d^2)$ *(black circle)* and $(g_m/I_d)^2$ *(blue circle)* versus $I_d$ at $V_{ds}$ = *0.1 V* and *f = 10 Hz.*

## IV. Conclusion

AlGaN/GaN omega-shaped nanowire FETs from 70 to 200 nm widths W have been fabricated and their *1/f* noise measurements were performed to find the W dependence on the carrier confinement. The accumulation of electrons in the volume of the nanowire constricts the trapping of electrons not only at sidewall surface, but also in the active bulk region. It was observed that the noise generated in the device with narrow W is governed by the carrier mobility fluctuations in the channel, whereas the device with wide W from the carrier number fluctuation due to the electron trapping from both the surface channel and the active bulk region. The extracted $N_T$ from the device with narrow W was noticeably less than those in wide W devices. The noise characteristics of the device with narrow W are having improved noise performances.

## Acknowledgment

This work was supported by the BK21 Plus funded by the Ministry of Education (21A20131600011), the IT R&D program of MOTIE/KEIT (10048931), and the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No. 2011-0016222, 2013R1A6A3A04057719).

## References

[1] T. P. Chow and R. Tyagi, "Wide bandgap compound semiconductors for superior high-voltage unipolar power devices," IEEE Trans. Electron Devices, vol. 41, no. 8, pp, 1481-1483, Aug. 1994.

[2] S. Takashima, Z. Li, and T. P. Chow, "Sidewall Dominated Characteristics on Fin-Gate AlGaN/GaN MOS-Channel-HEMTs," *IEEE Tans. Electron Devices,* vol. 60, no. 10, pp. 3025–3031, Oct. 2013.

[3] B. Lu, E. Matioli, and T. Palacios, "Tri-gate normally-off power MISFET," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 360-362, Mar. 2012.

[4] K.-S. Im, Y.-W. Jo, J.-H. Lee, S. Cristoloveanu, and J.-H. Lee, "Heterojunction-Free GaN Nanochannel FinFETs With High Performance," IEEE Electron Device Lett., vol. 34, no. 3, pp. 381–383, Mar. 2013

[5] K.-S. Im, R.-H. Kim, K.-W. Kim, D.-S. Kim, C. S. Lee, S. Cristoloveanu, and J.-H. Lee, "Normally off single nanoribbon Al2O3/GaN MISFET," IEEE Electron Device Lett., vol. 34, no. 1, pp. 27-29, Jan. 2013.

[6] Y.-W. Jo, D.-H. Son, C.-H. Won, K.-S. Im, J. H. Seo, I. M. Kang, and J.-H. Lee, "AlGaN/GaN FinFET with Extremely Broad Transconductance by Side-wall Wet Etch," IEEE Electron Device Lett., vol. 36, no. 10, pp. 1008–1010, Oct. 2015.

[7] K.-S. Im, V. Sindhuri, Y.-W. Jo, D.-H. Son, J.-H. Lee, S. Cristoloveanu, and J.-H. Lee "Fabrication of AlGaN/GaN Ω-shaped nanowire fin-shaped FETs by a top-down approach," Appl. Phys. Express, vol. 8, no. 6, pp. 066501-1~3, May. 2015.

[8] A. Balandin, S. Cai, R. Li, K. L. Wang, V. R. Rao, and C. R. Viswanathan, "Flicker Noise in GaN/$Al_{0.15}Ga_{0.85}N$ Doped Channel Heterostructure Field Effect Transistors," IEEE Electron Device Lett., vol. 19, no. 12, pp. 475-477, Dec. 1998.

[9] M. E. Levinshtein, S. L. Rumyantsev, R. Gaska, J. W. Yang, and M. S. Shur, "AlGaN/GaN high electron mobility field effect transistors with low 1/f noise," Appl. Phys. Lett., vol. 73, no. 8, pp. 1089~1091, Aug. 1998.

[10] S. H. Hsu, P. Valizadeh, D. Pavlidis, "Characterization and Analysis of Gate and Drain Low frequency Noise in AIGaN/GaN HEMTs", IEEE Proceedings, High Performance Devices 2002, pp. 453-460, Aug. 2002.

[11] H-Y Liu, C-S Lee, F-C Liao, W-C Hsu, B-Y Chou, J-H Tsai, and H-Y Leed, "Comparative Studies on AlGaN/GaN MOS-HEMTs with Stacked $La_2O_3/Al_2O_3$ Dielectric Structures", ECS Journal of Solid State Science and Technology, vol. 3 (8), pp. N115– N117, July 2014.

[12] V.Sindhuri, D.-H Son, D.-G Lee, S.H. Sakong, Y.-H Jeong , I.-T. Cho, J.-H. Lee, Y.-T. Kim, S. Cristoloveanu, Y.-H Bae, K.-S. Im, J.-H. Lee, "1/f Noise Characteristics of AlGaN/GaN FinFETs with and without TMAH surface treatment," Micro Electron Eng, vol. 147, pp. 134-136, Apr. 2015.

[13] G. Ghibaudo, O. Roux, CH. Nguyen-duc, F. Balestra, and J.Brini, "Improved Analysis of Low Frequency Noise in Field-Effect MOS Transistors", phys. stat. sol. (a), vol. 124, pp. 571-581, 1991.

[14] K.-I. Na, K.-H. Park, S. Cristoloveanu, J.A. Chroboczek, A. Ohata, W. Xion, J.-H. Lee, Y. Bae, "Low-frequency noise and mobility in triple-gate silicon-on-insulator transistors: Evidence for volume inversion effects," Micro Electron Eng, vol. 98, pp. 85-88, Jun. 2012.

[15] J.-M. Peransin et al., "1/f noise in MODFETs at low drain bias," IEEE Trans. Electron Devices, vol. 37, no. 10, pp. 2250–2253, Oct. 1990.

[16] SH Sakong, S-H Lee,T Rim, Y-W Jo, J-H Lee, and Y-H Jeong, "1/f Noise Characteristics of Surface-treated Normally-off $Al_2O_3$/GaN MOSFETs" IEEE Electron Device Lett., vol. 36, no.3, pp. 229–231, Oct. 2015.

[17] I.M.Hafez, G. Ghibaudo, F. Balestra, "FLICKER NOISE IN MOS TRANSISTORS OPERATED AT ROOM AND LIQUID HELIUM TEMPERATURES", Superlattices and Microstructures, Vol. 8, No. I, 1990.

[18] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, T. Elewa, "Double-gate silicon on insulator transistor with volume inversion: a new device with greatly enhanced performance". IEEE Electron Device Lett., vol. 8, no. 09, pp. 410–412, Sept. 1987.

# Simulation of Plasma Resonances in MOSFETs for THz-Signal Detection

Christoph Jungemann
Chair of Electromagnetic Theory
RWTH Aachen University
52056 Aachen, Germany
Email: cj@ithe.rwth-aachen.de

K. Bittner and H. G. Brachtendorf
Embedded Systems Research Group
University of Applied Sciences
of Upper Austria, Austria
Email: {Kai.Bittner|Brachtd}@fh-hagenberg.at

***Abstract*—We present simulations by the 2D drift-diffusion model of a quarter-micron NMOSFET at THz frequencies. The derivative of the current densities with respect to time is included in the model, which enables simulations of plasma oscillations. In contrast to the usual 1D transmission line models this approach includes all 2D effects of the device (parasitics, inhomogeneous channel, etc.). In the case of silicon the impact of plasma oscillations is found to be negligible due to the strong damping. With respect to numerics it is found that the backward differentiation formula based on trigonometric functions is very efficient for simulation of the periodic steady-state.**

## I. Introduction

Generation and detection of electromagnetic radiation in the THz range for remote sensing, security and medical applications etc. is currently a very active research field [1]. Due to the high frequencies of more than 300GHz (mm waves) the performance of semiconductor devices is very poor. By exploitation of plasma waves it might be possible to boost their performance [2]. In this work we present a new approach for the simulation of plasma waves in semiconductor devices beyond the usual transmission line approaches, where the device is described by a 1D transmission line, which is assumed to be piecewise homogeneous (e.g. [3], [4]). Both assumptions do not hold in real devices. First, the structure of a FET is at least 2D and second, the channel is not homogeneous. This is especially the case, if a DC drain bias is applied. Our approach is based on a 2D description of the electron/hole transport by the drift-diffusion (DD) model, which is sufficient to capture plasma waves in silicon devices [5].

Since in Ref. [6] quarter-micron silicon NMOSFETs are used for detection of THz signals, we investigate the impact of plasma effects in such devices.

## II. Approach

We solve in the DD model for electrons and holes in 2D [7]

$$\nabla \boldsymbol{J}_n - q\frac{\partial n}{\partial t} = 0 \tag{1}$$

$$\nabla \boldsymbol{J}_p + q\frac{\partial p}{\partial t} = 0 \tag{2}$$

$$\frac{\partial \boldsymbol{J}_n}{\partial t} + \frac{\boldsymbol{J}_n}{\tau_n} = -\frac{q^2}{m_n}\left(n\nabla\varphi - V_\mathrm{T}\nabla n\right) \tag{3}$$

$$\frac{\partial \boldsymbol{J}_p}{\partial t} + \frac{\boldsymbol{J}_p}{\tau_p} = -\frac{q^2}{m_p}\left(p\nabla\varphi + V_\mathrm{T}\nabla p\right) \tag{4}$$

together with the Poisson equation for the quasi-static potential

$$\nabla\cdot(\varepsilon\nabla\varphi) = -q\left(p - n + N_\mathrm{D} - N_\mathrm{A}\right) \ , \tag{5}$$

where $\boldsymbol{J}_n$ is the electron current density, $n$ the electron density, $q$ the positive electron charge, $\tau_n$ the macroscopic relaxation time of the electron momentum, $m_n$ the electron conductivity mass ($m_n = 0.286m_0$ and $m_p = 0.372m_0$ for silicon), $\varphi$ the quasi-stationary potential, $V_\mathrm{T}$ the thermal voltage, $\varepsilon$ the permittivity, and $N_\mathrm{D}$ the donor concentration. Corresponding hole quantities are labeled by $p$ and $N_\mathrm{A}$ is the acceptor concentration. The electron mobility is given by $\mu_n = q\tau_n/m_n$.

In order to capture plasma waves, we include in the constitutive equations for the current densities (3),(4) their time derivatives [8]. These derivatives are usually neglected in commercial simulators, because they increase the CPU time of the transient DD model significantly and the current densities can no longer be eliminated from the system of equations resulting in larger memory requirements. In the 2D case of the DD model for each grid node the electron density, hole density, the $x$- and $y$-components of the current densities and the potential have to be stored, where the current densities are defined on the edges of the grid primitives. In the case of a 2D tensor-product grid we get instead of three variables seven per grid node. The continuity equations (1),(2) are discretized with the finite volume method [9] and the constitutive equations (3),(4) are stabilized by applying the Scharfetter-Gummel scheme [10] to their right-hand sides together with the usual dimensional splitting [7]. Thus, this formulation reduces for the slowly varying case, for which the time derivatives of the current densities can be neglected ($\omega\tau_{n,p} \ll 1$), to the standard set of discrete equations. The terminal currents are evaluated with the Ramo-Shockley theorem [11].

Eqs. (1)-(4) are of the form

$$\frac{\partial u}{\partial t} = f(u,t) \ . \tag{6}$$

Three different methods for time integration are implemented. The implicit (backward) Euler scheme (BE), the second order backward differentiation formula based on polynomials (BDF2) [12] and the modified BDF2 scheme based on trigonometric functions (MBDF2) [13]. In all three cases the time derivative is approximated for a constant time step $\Delta t$ by

$$\frac{\partial u}{\partial t}|_{i\Delta t} \approx \frac{a_0u_i + a_1u_{i-1} + a_2u_{i-2}}{\Delta t} = f_i \tag{7}$$

ISBN 978-1-4673-8608-1  IEEE Catalog number CFP1649D-USB

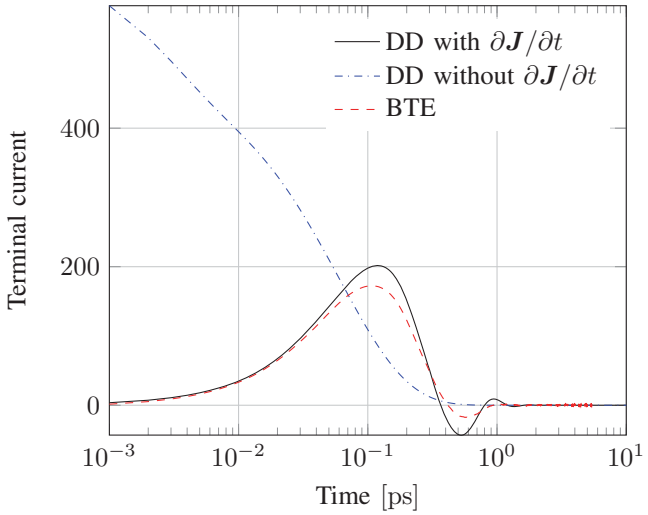



Fig. 1. Terminal current versus time for a pn junction. The bias changes abruptly from zero to 0.7V at zero seconds.

with $u(i\Delta t) \approx u_i$ and $f(u(i\Delta t), i\Delta t) \approx f_i$. The coefficients are for the BE scheme

$$a_0 = 1\ , \quad a_1 = -1\ , \quad a_2 = 0\ , \tag{8}$$

BDF2 scheme

$$a_0 = 1.5\ , \quad a_1 = -2\ , \quad a_2 = 0.5\ , \tag{9}$$

and MBDF2 scheme

$$a_0 = \frac{z\cos(2z) - z\cos(z)}{\sin(2z) - 2\sin(z)}\ , \tag{10}$$

$$a_1 = \frac{z\sin(z)}{\cos(z) - 1}\ , \tag{11}$$

$$a_2 = \frac{z}{2\sin(z)} \tag{12}$$

with $z = 2\pi/n_T$. The MBDF2 scheme is used only for the periodic steady-state and $n_T$ is the number of time steps used per period, where $n_T$ must be larger or equal to eight. All three formulas are A-stable, but show quite different spurious damping behavior in the case of plasma waves.

## III. Results

The derivation of the DD model from the Boltzmann Transport Equation (BTE) requires many approximations and it is not clear how accurately the DD model can describe plasma effects. In Fig. 1 results are shown for an abrupt pn junction simulated by the BTE, which is solved by the Monte Carlo method [8], and the DD model with and without the time derivative of the current densities. As expected, the DD model without the derivatives fails and yields the usual diffusive behavior. The DD model with the derivatives on the other hands yields plasma oscillations similar to the BTE result.

In Ref. [6] quarter-micron silicon NMOSFETs are used to detect THz radiation and we use therefore a similar device in our simulations (Fig. 2). The length of the gate contact is 250nm and the oxide thickness 3nm. The 2D structure captures the most important parasitics (e.g. the overlap capacitances between gate and source/drain). In addition, the channel is

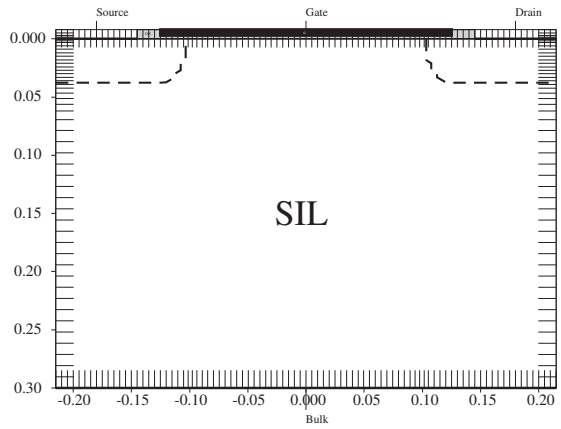



Fig. 2. The 2D structure and grid of the silicon NMOSFET. The ticks indicate the non-equidistant grid and the dashed thick lines the junctions.

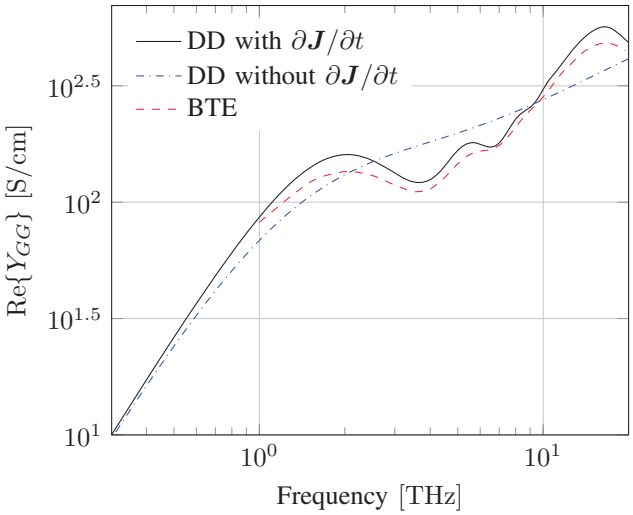



Fig. 3. Real part of the small-signal gate self-admittance at $V_G = 2.0$V, $V_D = 0.1$V and room temperature for the NMOSFET.

inhomogeneous, a fact not easily included in 1D transmission line models.

In Fig. 3 the real part of the gate self-admittance is shown as a function of the frequency for the NMOSFET. This small-signal result is calculated by the DD model with and without the time derivative of the current densities and by a spherical harmonics expansion of the BTE [14]. In this case the electron and hole mobilities are given by their respective bulk values [15] neglecting interface effects to facilitate a simpler comparison of the models. Again, the DD model and the BTE show reasonable agreement even at very high frequencies. Thus, the DD model is able to capture the most salient aspects of the plasma oscillations.

The NMOSFET is used as a passive mixer in Ref. [6] and we use an analogous circuit (Fig. 4). The RF signal is applied to the source terminal and the DC current at the drain terminal is measured. The applied DC drain/source bias is zero and a certain DC gate/source bias is chosen. The MOSFET is operated as a diode and it rectifies the RF signal, which leads to the DC current. The responsivity of the mixer is given by

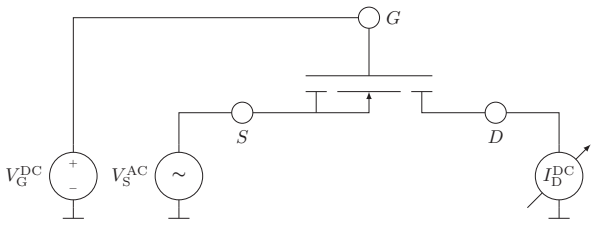



Fig. 4. A MOSFET as a passive mixer.

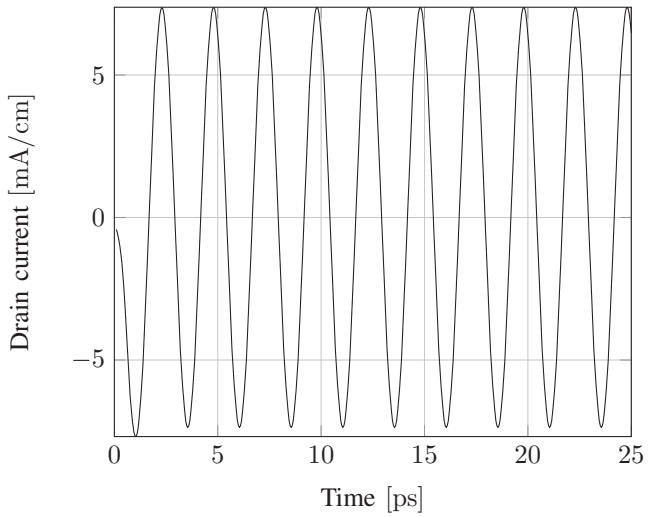



Fig. 5. Drain current at $V_G = 1.0\mathrm{V}$, $V_D = 0.0\mathrm{V}$, $V_S^{AC} = 1mV$, $f = 400\mathrm{GHz}$ and room temperature for the NMOSFET with $\mu_n = 300\mathrm{cm}^2/\mathrm{Vs}$.

the ratio of the DC drain current and RF power at the source

$$R_{\mathrm{I}} = \frac{I_{\mathrm{D}}^{\mathrm{DC}}}{P_{\mathrm{S}}^{\mathrm{AC}}} \ . \tag{13}$$

This responsivity is constant over a wide range of RF powers. Only for very large AC voltages (above 100mV) the responsivity depends on the AC power. In the circuit in Fig. 4 the drain is grounded (AC short). In some detectors the drain is kept open for the AC signal and the responsivity with respect to the voltage is calculated. It can be easily obtained by dividing $R_{\mathrm{I}}$ by the small-signal self-admittance of the drain.

In Fig. 5 the transient drain current is shown for an AC voltage of 1mV at 400GHz applied to the source calculated by the BDF2 scheme with time steps of 50fs and a constant electron mobility of $300\mathrm{cm}^2/\mathrm{Vs}$. A few periods are required to reach the periodic steady-state. In the following simulations a sufficient number of periods is used (depending on the frequency 50 to 200 periods), and the responsivity is evaluated for the last period.

In the case of very large AC amplitudes (some hundreds of Millivolts) negative electron and hole densities can occur during transient simulations. This seems to be due to the time derivatives of the current densities, which imply second derivatives with respect to time in the densities. In this case the Scharfetter-Gummel stabilization scheme is no longer sufficient to ensure positive densities. Therefore, all simulations in this work are restricted to the case of sufficiently small AC

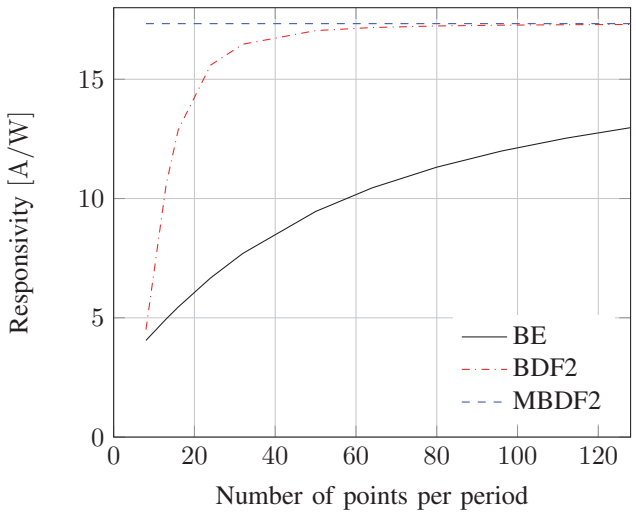



Fig. 6. Responsivity at $V_G = 1.0\mathrm{V}$, $V_D = 0.0\mathrm{V}$ and room temperature for a $0.25\mu\mathrm{m}$ NMOSFET with $\mu_n = 10000\mathrm{cm}^2/\mathrm{Vs}$ for 1THz.

amplitudes for which the densities remain always positive. In experiments the AC amplitudes are anyway small due to the high frequencies at which it is difficult to generate large RF powers.

In Fig. 6 the responsivity of the MOSFET is shown for the different time integration schemes as a function of the number of time steps per period for a very large electron mobility in order to emphasize the plasma effects. The different schemes show different levels of spurious damping. The BE scheme, which is even stable for certain poles with positive real parts, shows the usual over-damping and requires a very large number of time steps per period. Otherwise, the responsivity is strongly underestimated due to the over-damping. The standard BDF2 is more efficient than BE, and the modified one (MBDF2) requires only eight steps for a negligible error. A smaller number of steps is not possible due to numerical instabilities.

The responsivity as a function of the frequency is shown in Fig. 7 for different electron mobilities. For low mobilities no impact of the plasma waves is seen. On the other hand, for the highest mobility strong plasma effects occur, which vanish, if the time derivative of the current density is neglected. These results show, that plasma effects play no role in silicon devices with mobilities around $300\mathrm{cm}^2/\mathrm{Vs}$. In III-V or graphene devices the mobility might be sufficiently high for plasma effects and the responsivity might be higher than in silicon at high frequencies. At low frequencies the responsivity does not depend on the mobility, because the AC power at the source terminal and the DC drain current are both proportional to it.

The dependence on the gate bias and thus on the electron density is shown in Fig. 8 for a frequency of 1THz. The lower the gate bias, the lower is the resonance frequency. This leads to the resonance effects in the responsivity for the highest mobilities as a function of the gate bias. For low mobilities the peak responsivity is found near the threshold voltage, whereas at high mobilities it moves to higher voltages.

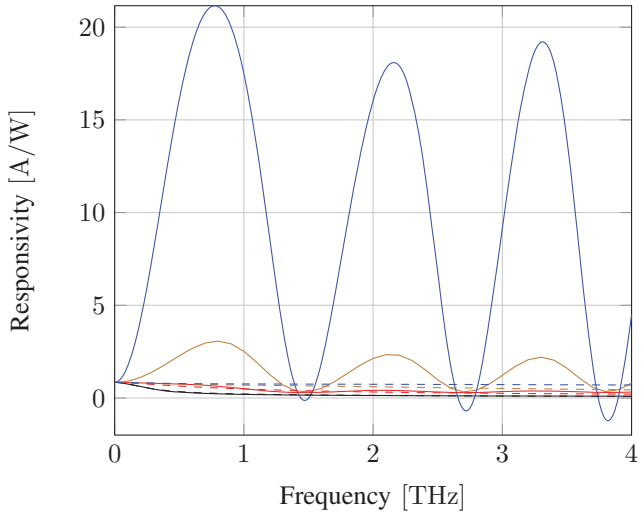



Fig. 7. Responsivity at $V_G = 1.0\mathrm{V}$, room temperature and $V_S^{AC} = 1\mathrm{mV}$ for the NMOSFET and different mobilities (black: 300, red: 1000, brown: 3000, blue: $10000\mathrm{cm}^2/\mathrm{Vs}$) with (solid) and without (dashed) the time derivative.

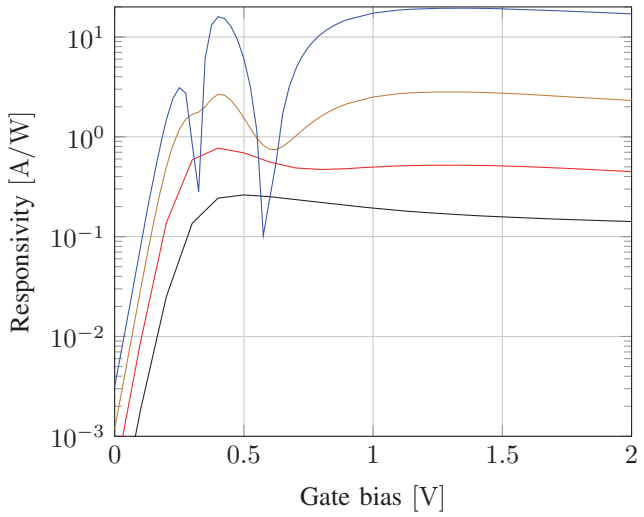



Fig. 8. Responsivity at $V_G = 1.0\mathrm{V}$, $V_D = 0.0\mathrm{V}$ and room temperature for the NMOSFET at 1THz (black: 300, red: 1000, brown: 3000, blue: $10000\mathrm{cm}^2/\mathrm{Vs}$).

## IV. Conclusion

We have demonstrated that inclusion of the time derivatives of the current densities in the constitutive equations of the DD model allows simulating plasma effects in semiconductor devices. Under periodic steady-state conditions the backward differentiation formula of the second order based on trigonometric functions (MBDF2) yields the best performance.

Due to the strong over-damping of the plasma waves by the low mobility (high scattering) plasma effects play no role in silicon devices. On the other hand, in high mobility materials plasma resonances might occur and the responsivity of such devices is largely enhanced at high frequencies.

## References

[1] H.-J. Song and T. Nagatsuma, eds., *Handbook of Terahertz Technologies: Devices and Applications*. Singapore: Pan Stanford Publishing, 2015.

[2] T. Otsuji and M. Shur, "Terahertz plasmonics: Good results and great expectations," *Microwave Magazine, IEEE*, vol. 15, pp. 43–50, Nov 2014.

[3] M. Dyakonov and M. Shur, "Detection, mixing, and frequency multiplication of terahertz radiation by two-dimensional electronic fluid," *Electron Devices, IEEE Transactions on*, vol. 43, pp. 380–387, Mar 1996.

[4] A. Lisauskas, U. Pfeiffer, E. Öjefors, P. H. Bolvar, D. Glaab, and H. G. Roskos, "Rational design of high-responsivity detectors of terahertz radiation based on distributed self-mixing in silicon field-effect transistors," *Journal of Applied Physics*, vol. 105, no. 11, 2009.

[5] W. Knap, V. Kachorovskii, Y. Deng, S. Rumyantsev, J.-Q. L, R. Gaska, M. S. Shur, G. Simin, X. Hu, M. A. Khan, C. A. Saylor, and L. C. Brunel, "Nonresonant detection of terahertz radiation in field effect transistors," *Journal of Applied Physics*, vol. 91, no. 11, pp. 9346–9353, 2002.

[6] E. Öjefors, U. Pfeiffer, A. Lisauskas, and H. Roskos, "A 0.65 THz focal-plane array in a quarter-micron CMOS process technology," *Solid-State Circuits, IEEE Journal of*, vol. 44, pp. 1968–1976, July 2009.

[7] S. Selberherr, *Analysis and Simulation of Semiconductor Devices*. Wien: Springer, 1984.

[8] C. Jungemann and B. Meinerzhagen, *Hierarchical Device Simulation: The Monte-Carlo Perspective*. Computational Microelectronics, Wien, New York: Springer, 2003.

[9] R. S. Varga, *Matrix Iterative Analysis*. Series in Automatic Computation, Englewood Cliffs, New Jersey: Prentice-Hall, 1962.

[10] D. L. Scharfetter and H. K. Gummel, "Large-signal analysis of a silicon read diode oscillator," *Electron Devices, IEEE Transactions on*, vol. ED-16, no. 1, pp. 64–77, 1969.

[11] H. Kim, H. S. Min, T. W. Tang, and Y. J. Park, "An extended proof of the Ramo-Shockley theorem," *Solid–State Electron.*, vol. 34, pp. 1251–1253, 1991.

[12] C. F. Curtiss and J. O. Hirschfelder, "Integration of stiff equations," *Proc. Nat. Acad. Sci. U.S.A.*, vol. 38, pp. 235–243, 1952.

[13] H. Brachtendorf and K. Bittner, "Grid Size Adapted Multistep Methods for High Q Oscillators," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 32, pp. 1682–1693, Nov 2013.

[14] S.-M. Hong, A. T. Pham, and C. Jungemann, *Deterministic solvers for the Boltzmann transport equation*. Computational Microelectronics, Wien, New York: Springer, 2011.

[15] D. M. Caughey and R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proc. IEEE*, vol. 55, pp. 2192–2193, 1967.

# Scaling/LER Study of Si GAA Nanowire FET using 3D Finite Element Monte Carlo Simulations

Muhammad A. Elmessary[1,3], Daniel Nagy[1], Manuel Aldegunde[4], Natalia Seoane[5], Guillermo Indalecio[5], Jari Lindberg[6], Wulf Dettmer[2], Djordje Perić[2], Antonio J. García-Loureiro[5] and Karol Kalna[1]
[1]ESDC and [2]ZCCE, College of Engineering, Swansea University, Swansea SA2 8PP, Wales, United Kingdom
[3]Dept of Mathematics & Engineering Physics, Faculty of Engineering, Mansoura University, Mansoura 35516, Egypt
[4]WCPM, School of Engineering, University of Warwick, Coventry CV4 7AL, England, United Kingdom
[5]CITIUS, Universidade de Santiago de Compostela, 15782 Santiago de Compostela, Galicia, Spain
[6]Varian Medical Systems Finland, Helsinki, Finland
Email: M.A.A.Elmessary.716902@swansea.ac.uk, Phone: +44 (0) 1792 602816

***Abstract*—$I_D$-$V_G$ characteristics of a 22 nm gate length gate-all-around (GAA) Si nanowire (NW) obtained from a 3D Finite Element (FE) Monte Carlo (MC) in-house simulation toolbox which uses anisotropic 2D Schrödinger equation based quantum corrections (SEQC) are compared against experimental data with excellent agreement at both low and high drain biases. We then scale the Si GAA NW according to the ITRS specifications to a gate length of 10 nm predicting that the scaled NW will ensure a required on-current of above 1mA/$\mu$m and superior electrostatic integrity of a nearly ideal sub-threshold slope of 66 mV/dec and a DIBL of 39 mV/V. The effects of nanowire (NW) line-edge roughness (LER) on threshold voltage and off-current are investigated by calibrated 3D FE quantum corrected (QC) drift-diffusion (DD) toolbox.**

## I. Introduction

Gate-All-Around (GAA) nanowire (NW) FETs are considered to be excellent candidates for future CMOS integration for sub-10 nm digital technology to continue transistor down-scaling [1]. The GAA NW FETs have superior electrostatics and immunity to short channel effects while still delivering a large on-current [2]–[4]. However, variability of transistor characteristics induced by material properties and by fabrication process can affect their performance in circuits. Line-edge roughness (LER) is one of such sources with a major impact on variability in NW/FinFETs [3], [5], [6]. In this work, we report on performance, scaling and variability induced by line-edge roughness (LER) [3], [5], [6] of GAA NW FETs. We use an in-house 3D Finite Element (FE) Monte Carlo (MC) toolbox which includes newly developed integrated calibration-free FE anisotropic Schrödinger equation based quantum corrections (SEQC). More details on the 3D FE MC toolbox are in Refs. [7]–[9].

## II. 3D Monte Carlo Simulations

In this work, we use the 3D FE method to accurately describe the complex 3D geometry of the nanoscale devices. The accurate description of the simulation domain in nanoscale semiconductor devices is essential in determining quantum transport at highly non-equilibrium conditions. In our case, we chosen semi-classical transport technique, a 3D ensemble MC [10], with calibration-free quantum confinement corrections, the SEQC, along the device channel. Our in-house 3D FE MC simulation toolbox employs fully anisotropic 2D FE

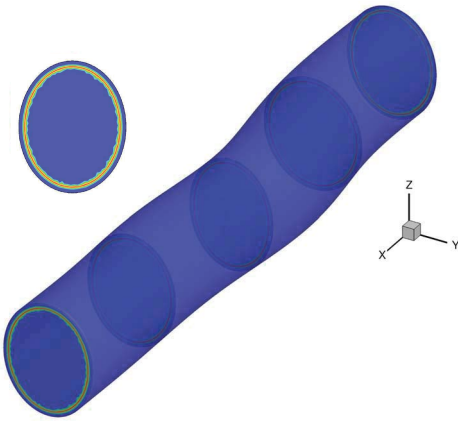



Fig. 1. Schematic of the 22 nm gate length $n$-channel Si GAA nanowire, showing LER and examples of 2D slices.

Schrödinger equation based quantum corrections (QC) which thus depends on valley orientation. The MC transport engine considers analytical anisotropic non-parabolic bandstructure model with the following scattering processes: the acoustic phonon scattering, non-polar optical phonon scattering ($g$ and $f$-processes) [11], ionized impurity scattering using the third body exclusion model by Ridley [12] and static screening model self-consistently calculating Fermi energy and electron

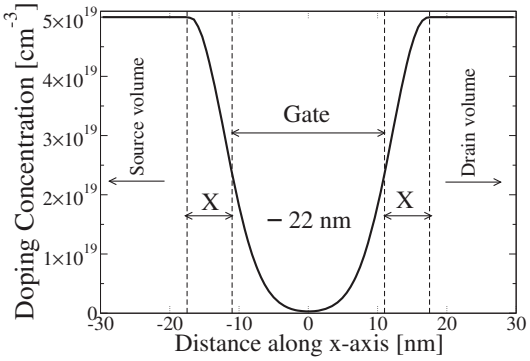



Fig. 2. Cross-section of Gaussian-like doping profile along the transport $x$-direction in the 22 nm gate length GAA NW FET.

temperature [13], and the interface roughness scattering using Andos model [14]. This combination has been shown to be a very good compromise between accuracy and speed for accurate physical simulations of carrier transport in nanodevices which are strongly quantum confined systems at highly non-equilibrium transport conditions [7]–[9].

We start by comparing results from our 3D SEQC MC toolbox against experimental data of the 22 nm gate length GAA Si NW [2] with a $\langle 110 \rangle$ channel orientation. The NW has elliptical cross-section (Fig. 1) with a shorter diameter of 11.3 nm; a longer diameter of 14.22 nm; with an effective diameter (elliptical circumference/$\pi$) $D_{NW}$=12.8 nm and EOT = 1.5 nm which can be only accurately described by the FE method.

The 3D FE quantum corrected (QC) drift-diffusion (DD) simulations using density gradient [15] were used to reverse engineer a doping profile in the sub-threshold region at $V_D$ =0.05 V and $V_D$=1.0 V as shown in Fig. 2. Fig. 3 shows examples of this engineering process from a sub-threshold region which achieved excellent agreement with a maximum doping of $5 \times 10^{19} \mathrm{cm}^{-3}$, a work function of 4.472 eV , and a S/D size of 30.8 nm. We then simulate the $I_D$-$V_G$ characteristics of the 22 nm gate GAA Si NW at low and high drain biases achieving an excellent agreement as can be seen in Fig. 4. Fig. 5 shows the potential profile in the device in on-current conditions. Fig. 6 shows the average electron velocity along the channel at the same on-current conditions. We see that the electron velocity exhibits a typical behaviour along the channel. The source injects electrons at relatively large injection velocity of about $1.5 \times 10^4$ m/s where they are quickly accelerated along the gate reaching their maximum velocity of $1.75 \times 10^5$ m/s on a drain side of the gate. Then electrons rapidly decelerate into a heavily doped drain due to enhanced optical phonon emission assisted by ionised impurity scattering [16].

We then scale the Si GAA NW according to the ITRS specifications to a gate length of 10 nm and an EOT of 0.8 nm. Fig. 7 compares the first wavefunctions of the three $\Delta$ valleys in the middle of the channel for the 22/10 nm gate length GAA NW, respectively, at $V_D$ =1.0/0.7 V and $V_G$=0.8 V (note that $\Delta 1$ and $\Delta 2$ have the same effective mass tensor in the $\langle 110 \rangle$ channel orientation, so they will have the same wavefunction). Fig. 8 shows $I_D$-$V_G$ characteristics for the scaled 10 nm gate length NW FET at $V_D$ =0.05 V and $V_D$ =0.7 V obtained from the 3D FE SEQC MC. Table I compares device operating characteristics with gate lengths of 22 nm and 10 nm predicting that the scaling to the 10 nm gate will ensure superior electrostatic integrity of a nearly ideal sub-threshold slope of 66 mV/dec and a DIBL of 39 mV/V and satisfactory on-current (even the on-current increase is relatively small, $\approx 5\%$). The sub-threshold voltage ($V_T$) for both NW is 0.3 V. The scaled GAA NW has a better sub-threshold slope (SS) at both low and high drain biases, and a better drain-induced-barrier-lowering (DIBL) of only 39 mV/V.

TABLE I. $V_T$ AND SUB-THRESHOLD SLOPE (SS) AT $V_D = 0.05$ V (LOW) AND 1.0/0.7 V (HIGH) FROM THE DD, DIBL FROM THE DD AND FROM THE MC, AND DRIVE CURRENTS ($I_{MC}$) AT $V_G$ = 1.0 V COMPARING 22 AND 10 NM GAA FETS.

| Gate length [nm] | 22 | 10 |
|---|---|---|
| $V_T$ [V] | 0.3 | 0.3 |
| $SS_{LOW}$ [mV/dec] | 74 | 66 |
| $SS_{HIGH}$ [mV/dec] | 77 | 67 |
| DIBL [mV/V] | 48 | 35 |
| $DIBL_{MC}$ [mV/V] | 64 | 39 |
| $I_{MC}$ [$\mu$A/$\mu$m] | 1150 | 1196 |

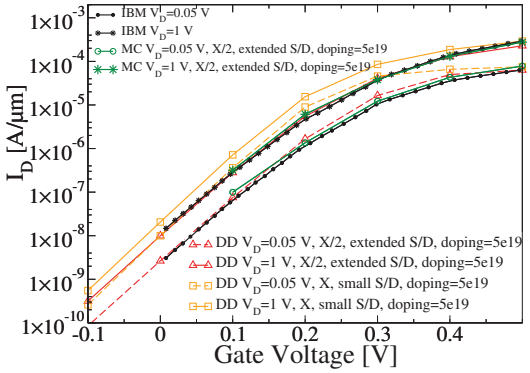



Fig. 3. Devising doping profile for the 22 nm GAA NW FET at $V_D$ = 0.05 V and $V_D$ = 1.0 V via DD simulations by changing the size of the S/D region and the doping spread $X$ (open red triangles and orange squares). Final MC simulations (green open circles and stars) are compared to experimental data (black full circles and stars).

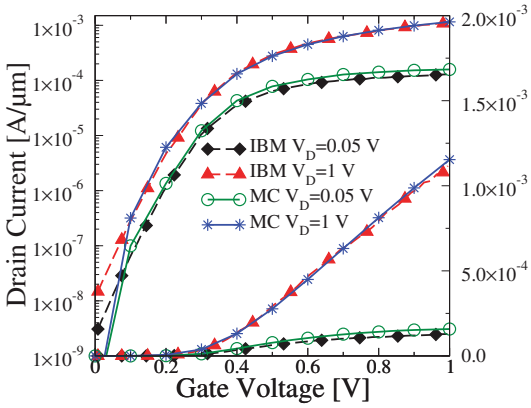



Fig. 4. $I_D$-$V_G$ characteristics for the 22 nm GAA nanowire from the 3D FE MC with anisotropic Schrödinger quantum corrections with no free parameter (full lines) compared against experimental data (dashed lines) [2].

## III. LINE-EDGE ROUGHNESS (LER)

The LER variability study in NWs as one of the major sources of device variability [17] is essential for predicting device behaviour in digital circuits. The effect of uncorrelated LER is studied using Fourier synthesis with Gaussian autocorrelation [18] implemented as described in [17], [19]. The simulations of variability for the 22 nm gate length NW are carried out using the 3D quantum corrected FE DD with a LER correlation length (CL) of 20 nm and three root mean square values (RMS=0.6, 0.7 and 0.85 nm) chosen to represent the RMS observed in experiments [2], [3]. Table II compares $V_{T,lin}$ and $I_{OFF,lin}$ variability at a low drain bias $V_D = 0.05$ V due to the LER for the 22 nm GAA nanowire as a function of the RMS height. The average value of $V_T$

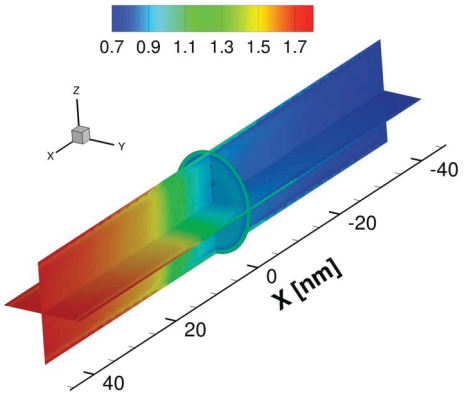



Fig. 5. Potential profile at $V_D$ = 1.0 V and $V_G$ = 0.8 V for the 22 nm gate length GAA nanowire, from drain ($+x$) to source ($-x$).

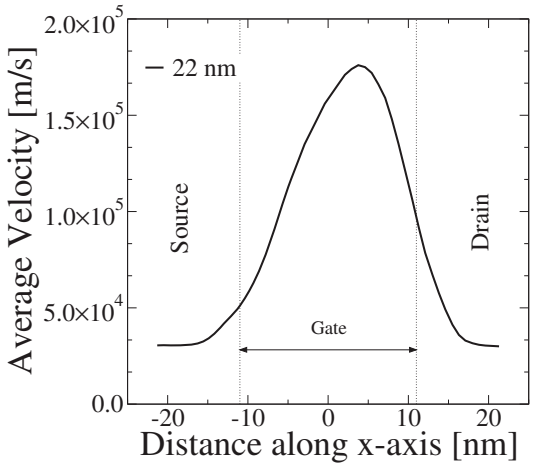



Fig. 6. Average electron velocity at $V_D$ = 1.0 V and $V_G$ = 0.8 V along the 22 nm gate length GAA nanowire (3D MC). The zero is set in the middle of the channel.

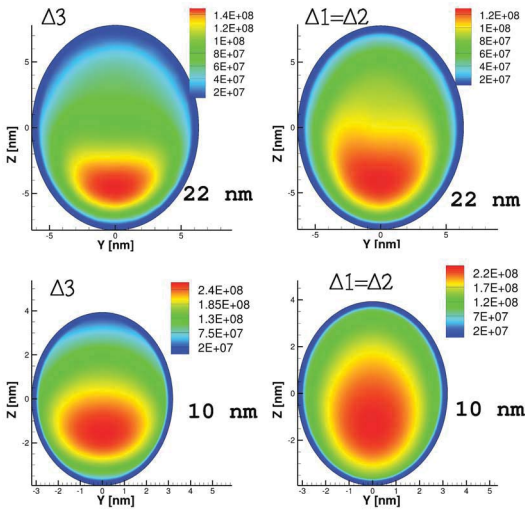



Fig. 7. The first wavefunctions of the three $\Delta$ valleys, in the middle of the $\langle 110 \rangle$ channel for the 22 nm (top, at $V_D$ = 1.0 V) and 10 nm (bottom, at $V_D$ = 0.7 V) Si GAA NW at $V_G$ = 0.8 V.

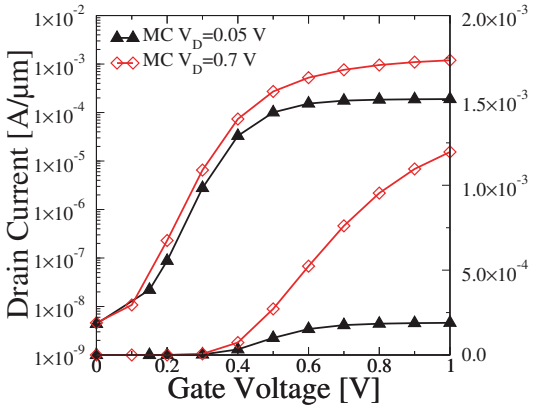



Fig. 8. $I_D$-$V_G$ characteristics for the scaled 10 nm gate length GAA nanowire predicted by the quantum corrected 3D FE MC.

and $\sigma V_T$ are increasing with increasing the RMS height. In addition, the average value of $Log_{10}(I_{OFF})$ and $\sigma Log_{10}(I_{OFF})$ are increasing with increasing the RMS height as expected.

Fig. 9 shows the scatter plots of $V_{T,lin}$ versus $V_{T,sat}$ for the 22 nm Si GAA NW with CL=20 nm and RMS=0.6 nm. The threshold voltage at low and high drain biases are strongly correlated (CC=0.997). The larger the CC value, the less sensitive the variability is to a change in the drain bias. Fig. 10 shows $I_{OFF,sat}$ vs. $V_{T,sat}$ at $V_D$=1.0 V for the 22 nm GAA nanowire with CL=20 nm and RMS=0.6 nm. The log of the off-current exhibits the typical linear dependence on the decreasing $V_{T,sat}$ suggesting near-to-Gaussian behaviour.

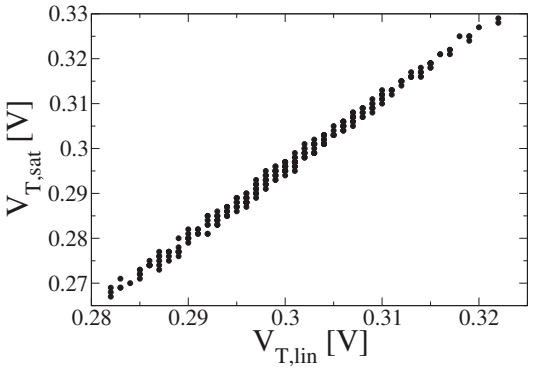



Fig. 9. Scatter plot showing the distribution of the threshold voltages at a low drain bias ($V_{T,lin}$) against the threshold voltages at a high drain bias ($V_{T,sat}$) for the 22 nm GAA nanowire with LER (CL=20 nm, RMS=0.6 nm).

TABLE II. COMPARISON OF THE $V_{T,lin}$, AND $I_{OFF,lin}$ VARIABILITY ($V_D$ = 0.05 V) DUE TO LER FOR THE 22 NM GAA NANOWIRE AS A FUNCTION OF THE RMS HEIGHT.

| RMS [nm] | 0.6 | 0.7 | 0.85 |
|---|---|---|---|
| avg. $V_T$ [mV] | 300.54 | 302.13 | 302.47 |
| $\sigma V_T$ [mV] | 8.61 | 10.12 | 12.1 |
| avg. $Log_{10}(I_{OFF})$ [A] | -10.02 | -10.06 | -10.07 |
| $\sigma Log_{10}(I_{OFF})$ [A] | 0.219 | 0.259 | 0.312 |

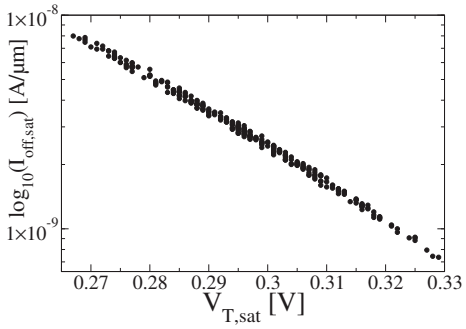



Fig. 10. $\log_{10}(I_{OFF,SAT})$ vs. $V_{T,sat}$ at $V_D$=1.0 V for the 22 nm GAA nanowire with LER (CL=20 nm, RMS=0.6 nm).

## IV. Conclusion

We have employed our 3D SEQC FE MC simulation toolbox which accurately describes the nanoscale geometry of multi-scale transistors using a completely parameter-free model of carrier transport to obtain the I-V characteristics of the 22 nm gate length GAA Si NW FET. The $I_D$-$V_G$ characteristics at low and high drain biases obtained from the 3D MC toolbox which uses fully anisotropic transport model together with fully anisotropic quantum corrections which dependent on the valley orientation (how longitudinal and transverse electron effective masses are oriented along the device channel) demonstrated exceptional agreement with experimental data [2], [3]. We have then scaled the GAA Si NW FET to the 10 nm gate length and predicted that the scaled device will deliver an on-current of 1196 $\mu$A/$\mu$m with superior electrostatic integrity of a nearly ideal sub-threshold slope of 66 mV/dec and a DIBL of 39 mV/V. Finally, we have found that the LER induced variability for the 22 nm GAA NW exhibits $\sigma V_T$ of about $0.9 - 12$ mV and that $\sigma \log_{10}(I_{OFF})$ of about $0.2 - 0.3$ A. The same $\sigma V_T$ of 12 mV has been obtained for UTB-FD-SOI transistors (with $L_G$ = 22 nm; CL = 25 nm and $3\sigma = 2$ nm) [20].

## References

[1] I. Ferain et al., "Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors," *Nature*, vol. 479, pp. 310–316, 2011.

[2] S. Bangsaruntip et al., "Density scaling with gate-all-around silicon nanowire MOSFETs for the 10 nm node and beyond," *IEDM Tech. Dig.*, pp. 526–529, 2013.

[3] S. Bangsaruntip et al., "High Performance and Highly Uniform Gate-All-Around Silicon Nanowire MOSFETs with Wire Size Dependent Scaling," *IEDM Tech. Dig.*, pp. 297–300, 2009.

[4] S. D. Suk et al., "Investigation of nanowire size dependency on TSNWFET," *IEDM Tech. Dig.*, pp. 1129–1131, 2007.

[5] T. Linton et al., "Determination of the Line Edge Roughness Specification for 34 nm Devices," *IEDM Tech. Dig.*, pp. 303–306, 2002.

[6] S. D. Kim, H. Wada, and Jason C. S. Woo, "TCAD-Based Statistical Analysis and Modeling of Gate Line-Edge Roughness Effect on Nanoscale MOS Transistor Performance and Scaling," *IEEE Trans. Semicond. Manuf.*, vol. 17 No. 2, pp. 192–200, 2004.

[7] J. Lindberg, M. Aldegunde, D. Nagy, W. G. Dettmer, K. Kalna, A. J. García-Loureiro, and D. Perić, "Quantum Corrections Based on the 2D Schrödinger Equation for 3D Finite Element Monte Carlo Simulations of Nanoscaled FinFETs," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 423–429, 2014.

[8] M. Aldegunde, A. J. García-Loureiro, and K. Kalna, "3D Finite Element Monte Carlo Simulations of Multigate Nanoscale Transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 5, pp. 1561–1567, 2013.

[9] D. Nagy, M. A. Elmessary, M. Aldegunde, R. Valin, A. Martinez, J. Lindberg, W. G. Dettmer, D. Perić, A. J. García-Loureiro, and K. Kalna, "3D Finite Element Monte Carlo Simulations of Scaled Si SOI FinFET with Different Cross-Sections," *IEEE Trans. Nanotechnol.*, vol. 14, no. 1, pp. 93–100, Jan. 2015.

[10] C. Moglestue, *Monte Carlo Simulation of Semiconductor Devices*. Wien-New York: Springer-Verlag, 1993.

[11] C. Jacoboni and P. Lugli, *The Monte Carlo Method for Semiconductor Device Simulation*. Wien-New York: Springer-Verlag, 1989.

[12] B. K. Ridley, "Reconciliation of the Conwell-Weisskopf and Brooks-Herring formulae for charged-impurity scattering in semiconductors: Third-body interference," *J. Phys. C: Solid State Phys.*, vol. 10, no. 10, pp. 1589–1593, 1977.

[13] A. Islam and K. Kalna, "Monte Carlo simulations of mobility in doped GaAs using self-consistent Fermi-Dirac statistics," *Semicond. Sci. Technol.*, vol. 26, no. 5, pp. 055007 (9pp), 2011.

[14] D. K. Ferry, *Semiconductor Transport*, Taylor & Francis, 2000.

[15] A. J. Garcia-Loureiro et al., "Implementation of the density gradient quantum corrections for 3D simulations of multigate nanoscaled transistors," *IEEE Trans. Comput-Aided Des. Integr. Circuits Syst.*, vol. 30, no. 6, pp. 841-851, 2011.

[16] A. Islam, B. Benbakhti, and K. Kalna, "Monte Carlo study of ultimate channel scaling in Si and $In_{0.3}Ga_{0.7}As$ bulk MOSFETs," *IEEE Trans. Nanotechnol.*, vol. 10, no. 6, pp. 1424–1432, Nov. 2011.

[17] N. Seoane et al., "Random Dopant, Line-Edge Roughness, and Gate Workfunction Variability in a Nano InGaAs FinFET," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 466-472, 2014.

[18] A. Asenov, S. Kaya, and A. R. Brown, "Intrinsic Parameter Fluctuations in Decananometer MOSFETs Introduced by Gate Line Edge Roughness," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1254-1259, 2003.

[19] G. Indalecio, M. Aldegunde, N. Seoane, K. Kalna and A. J. García-Loureiro, "Statistical study of the influence of LER and MGG in SOI MOSFET," *Semicond. Sci. Technol*, pp. 045005, 2014.

[20] S. Markov, A. S. M. Zain, B. Cheng and A. Asenov, "Statistical Variability in Scaled Generations of n-channel UTB-FD-SOI MOSFETs under the Influence of RDF, LER, OTF and MGG," *SOI Conference*, pp. 1–2, 2012.

# Simulation Analysis of the Electro-Thermal Performance of SOI FinFETs

L. Wang[a*], T. Sadi[a], A. R. Brown[b], M. Nedjalkov[c], C. Alexander[b], B. Cheng[b], C. Millar[b], A. Asenov[a,b]
[a] School of Engineering, University of Glasgow, Glasgow, U.K.,
[b] Gold Standard Simulations Ltd, Glasgow, U.K.,
[c] Institute for Microelectronics, TU Wien, Gußhausstraße 27-29/E360, 1040 Wien, Austria
[*]Liping.Wang @glasgow.ac.uk

***Abstract*— The GSS 'atomistic' simulator GARAND has been enhanced with a thermal simulation module to investigate the impact of self-heating on FinFET DC operation. This thermal simulation module is based on the solution of the coupled Heat Flow, Poisson, and Current Continuity Equations, which is developed for the benefit of computational efficiency. A new formula for the calculation of the thermal conductivity in the fin region is employed considering both fin shape and temperature dependencies. The heat dissipation through the gate is treated by nonhomogeneous Neumann boundary conditions. The electro-thermal simulation results for an SOI FinFET example, designed to meet the specifications for the 14/16nm CMOS technology generation, are presented. The lattice temperature profiles under different external thermal resistances connected to the gate and the corresponding Id-Vg characteristics are investigated and analysed.**

***Keywords—FinFET; thermal effects; self-heating effects***

## I. INTRODUCTION

Self-heating is one of the major concerns for nanoscale semiconductor transistors in terms of performance and reliability. As a result, there is a growing demand for the development of reliable electrothermal models and tools treating more accurately the self-heating effects in nano CMOS devices [1-3]. Simultaneously FinFETs, with their superior electrostatic integrity, performance and variability are replacing the traditional planar MOSFET [4]. However, because of its 3D architecture, the FinFETs' thermal properties are significantly degraded. Self-heating effects will be exacerbated in SOI FinFETs (a schematic of an SOI FinFET is shown in Fig. 1), due to the low thermal conductivity of the buried oxide layer beneath the fin. To maximize the benefits of FinFET technology, an enhancement of TCAD tools is required to allow accurate analysis and modelling of self-heating in FinFETs and its influence on device performance [1-2]. A progressive electro-thermal FinFET simulation study has been presented [5].

Recently, the thermal simulation module in the GSS 'atomistic' simulator GARAND [6] has been enhanced to capture accurately the fin geometry dependence of the thermal conductivity [7-8]. In this paper, GARAND is used to investigate the electro-thermal performance of SOI FinFETs under different external thermal resistances connected to the gate. The paper is organised as follows. In section II we provide a brief description of the simulation methodology, including the new approximate formula for the calculation of the thermal conductivity in the fin region, and the treatment of heat dissipation through the gate. In Section III, the electro-thermal simulation results, for an SOI FinFET example, designed to meet the specifications for the 14/16nm CMOS technology generation, are presented and analysed. The lattice temperature profiles under different external thermal resistances connected to the gate and the corresponding Id-Vg characteristics are investigated. Finally the conclusions are drawn in Section V.

The research leading to these results has received funding from the European Union Seventh Framework Programme (FP7/2007 – 2013) under grant agreement no. 318458 SUPERTHEME.

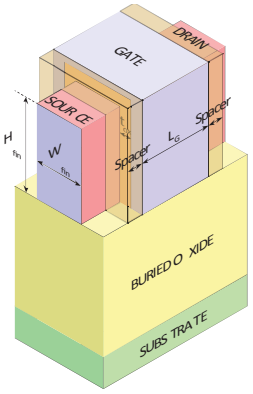



Fig. 1. Schematics of SOI FinFET.

## II. SIMULATION METHODOLOGY

### A. Coupled electro-thermal simulations

Our electro-thermal simulation module, which is implemented in the atomistic simulator GARAND, is based on the solution of the coupled Heat Flow, Poisson and Current Continuity Equations. The heat flow equation may be derived using phenomenological considerations, beginning with the Fourier law, which relates the heat current and the temperature gradient via the thermal conductivity into a linear response model, equivalent to Ohm's law. The heat flow equation can be written as:

$$\rho c \frac{\partial T_L}{\partial t} = H + \nabla(\kappa \nabla T_L), \qquad (1)$$

where $T_L$ is the lattice temperature, $\rho$ is the mass density, $c$ is the specific heat of the material, $\kappa$ is the thermal conductivity, and $H$ is the heat generation term. This assumes that the electrons and holes are in thermal equilibrium with the silicon lattice. If Joule heat is considered, the heat generation term can be written as:

$$H = J_n \cdot E_n + H_U \quad (2)$$

where $J_n$ is the electron current densitiy, $E_n$ is the electric field, $H_U$ is the lattice heating due to carrier recombination/generation. Here we focus on the self-consistent solution of the steady-state heat-flow equation. The current density has three components corresponding to a drift term, electron density gradient and temperature gradient terms:

$$J_n = qn\mu_n E_n + k\mu_n T_L \nabla n + +k\mu_n n \nabla T_L \quad (3)$$

where $n$ is the electron density, $\mu_n$ is the electron mobility, $k$ is Boltzmann constant.

### B. Thermal conduction in the fin

A special thermal conductivity model is developed considering the effects of thermal confinement in FinFETs, where the thickness and width of the fin are less than 100 nm. The thermal conductivity in the fin can be significantly reduced compared to bulk Si, due to phonon-boundary scattering. A new approximate formula is employed in our thermal module for the calculation of the thermal conductivity in the fin region, which generalises a previous 1D paradigm [9] to 2D confined structures by assuming a similar integral dependency in the second direction [7]. For a fin of height $h$ and width $w$, the thermal conductivity in the fin is given by

$$\kappa(y,z) = \kappa_0(T) \int_0^{\pi/2} \sin^3\theta \left\{1 - \exp\left(-\frac{h}{2\lambda(T)\cos\theta}\right)\cosh\left(\frac{h-2z}{2\lambda(T)\cos\theta}\right)\right\} d\theta \int_0^{\pi/2} \sin^3\theta \left\{1 - \exp\left(-\frac{w}{2\lambda(T)\cos\theta}\right)\cosh\left(\frac{-2y}{2\lambda(T)\cos\theta}\right)\right\} d\theta \quad (4)$$

where the offset of the $y$ and $z$ origins is accounted as follows: the $z$-axis is along the direction of fin height with the top and bottom surfaces of the fin being at $z$=0 and $z$=$h$, and the $y$-axis is along the direction of fin width with the surfaces of the fin being at $y$=-$w$/2 and $y$=$w$/2. Using this new calculation method the fin thermal conductivity is estimated to be 1~2 orders of magnitude lower than conventional values for bulk Si.

### C. Heat dissipation through the gate

The thermal environment, where heat is dissipated, is a large domain, including transistors, the substrate, the interconnect layers, the die, the heat sink and packaging. The bulk of the thermal resistance lies outside of the usual electrical simulation domain, which is typically restricted to the active region of the device in order to maximize computational efficiency. The inclusion of external thermal resistances to account for heat dissipation into interconnects, the wafer, the case etc. is crucial for thermal simulations.

In FinFETs, the gate almost "wraps" around the channel, which gives excellent control of the conducting channel and very little current is allowed to leak through the body when the device is in the off state. This is beneficial for optimal switching speeds and power. However, the heat dissipation through the gate is more complicated than the source and drain region, because the shape and materials of the gate stack and the surrounding region are much more complex. At thermally conducting interfaces, nonhomogeneous Neumann boundary conditions can be imposed:

$$\kappa \frac{\partial T}{\partial N} = \frac{T_a - T}{R_{th}} \quad (5)$$

where $R_{th}$ is the external thermal resistance, $T_a$ is the ambient temperature, $N$ is the unit vector in the direction of the outer normal at the interface.

## III. SOI FINFET EXAMPLE

The material and structure of the SOI FinFET used in this study are shown in Fig. 2. Its channel length is 25 nm with spacers of 6nm on both sides of the gate, while the fin width and the fin height are 12nm and 30nm respectively. A high-k metal gate stack is used. The device parameters are listed in Table I. This SOI FinFET example is designed to meet the specifications for the 14/16nm CMOS technology generation.

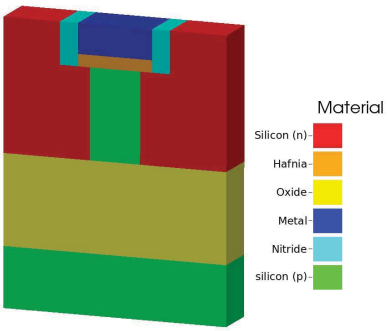



Fig. 2. Materials and structures of the bulk FinFET's electrical simulation domain, showing a cross section.

TABLE I. DEVICE PARAMETERS FOR THE SOI FINFET EXAMPLE

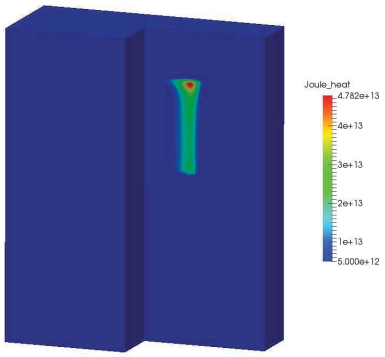
| Parameter | Value |
|---|---|
| $L_G$ | 25 nm |
| Fin Width, $W_F$ | 12 nm |
| Fin Height, $H_F$ | 30 nm |
| Spacer | 6 nm |
| highly doped drain (HDD) profile | 2nm/dec ($\sigma$=2.1nm) |
| highly doped drain (HDD) doping | $1\times10^{20}$ cm$^{-3}$ |
| Equivalent Oxide Thickness (EOT) | 0.8 nm |
| Channel doping | $1\times10^{15}$ cm$^{-3}$ |
| BOX depth | 30 nm |
| Supply Voltage | 0.9 V |

Following the progressive study of a coupled electro-thermal simulation for FinFETs [6], as a further step, in this paper we investigate the impact of external thermal resistances connected to the gate on the electro-thermal performance of the SOI FinFET. Three external resistances are used accounting for heat dissipation through the top of the gate, the front and the back of the gate. By using GARAND with the coupled thermal simulation module, five different cases with various external thermal resistances connected to the gate of the SOI FinFET example are simulated, as summarised in Table II. The external thermal resistances are user-specified parameters for the electro-thermal simulation module. The values used here demonstrate the effect and importance of the choice of relevant thermal resistances. In the simulation, a special thermal conductivity model that considers the effects of confinement in the fin is employed according to Eq. (4). Temperature dependence has been taken into account in the mobility models and saturation velocity. The Masetti model is used for doping-dependent low-field mobility, the enhanced Lombardi model is used for perpendicular field-dependent mobility and the Caughey-Thomas model is used for lateral field-dependent mobility.

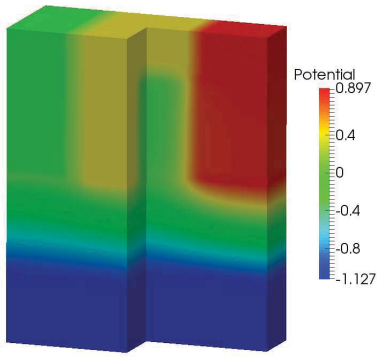
TABLE II. FIVE DIFFERENT CASES WITH VARIOUS EXTERNAL THERMAL RESISTANCES FOR 3D COUPLED ELECTRO-THERMAL SIMULATION

| | **External thermal resistance connected to** | | |
|---|---|---|---|
| | ***Top gate*** | ***Front gate*** | ***Back gate*** |
| Case 1 | 4800 | 32 | 32 |
| Case 2 | 4800 | 320 | 320 |
| Case 3 | 4800 | 3200 | 3200 |
| Case 4 | 480 | 32 | 32 |
| Case 5 | 480 | 320 | 320 |

Joule heat and potential distributions at high drain and high gate biases resulting from the 3D coupled electro-thermal simulations for "Case 1" are illustrated in Fig. 3. Lattice temperature distributions at high drain and high gate biases for five cases are illustrated in Fig.4, as well as the temperature variation according to gate voltage at high drain bias. The Id-Vg characteristics at high drain bias from the 3D electro-thermal simulations are illustrated in Fig.5. Because of the much lower thermal conductivity of the fin, a significant hot spot is produced near the drain, where the peak lattice temperature exceeds 420K in all five cases in this study, and strong temperature gradients are also generated in this region. As would be expected, the increase of external thermal resistances raises the lattice temperature. However, the external thermal resistance at different places connected to the gate has a different impact. When external thermal resistances connected to the front and the back of the gate increase by 10 times, the lattice temperature increase by approximately 30 K, and consequently the on-current decreases by 3~7%. Conversely, when external thermal resistances connected to the front and the back of the gate are fixed and external thermal resistance connected to the top of the gate is increased 10 times, there is no obvious impact on the lattice temperature and the corresponding electrical performance. Peak temperature and the average temperature in the fin at the high drain and high gate biases, and the on-current are compared in Table III.

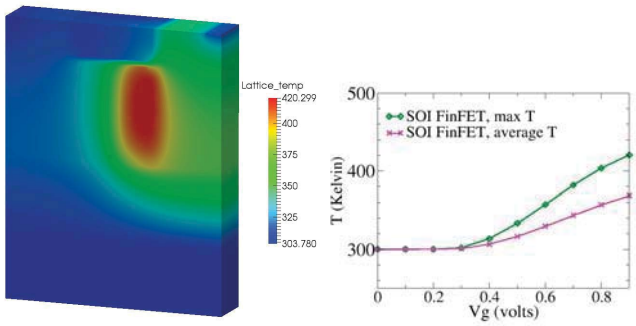



(a)

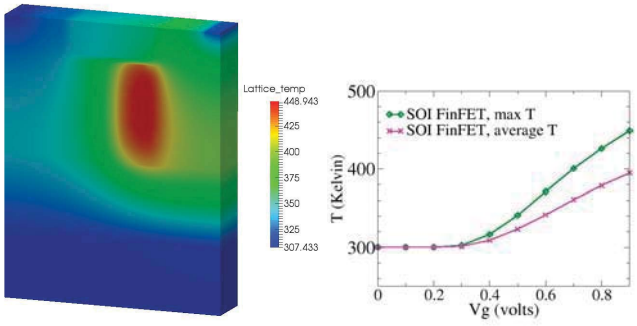



(b)

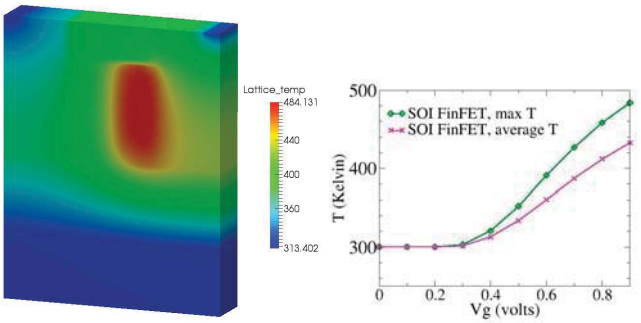
Fig. 3. (a) Joule heat and (b) potential distributions at high drain and high gate biases resulting from the 3D coupled electro-thermal simulations for "Case 1".



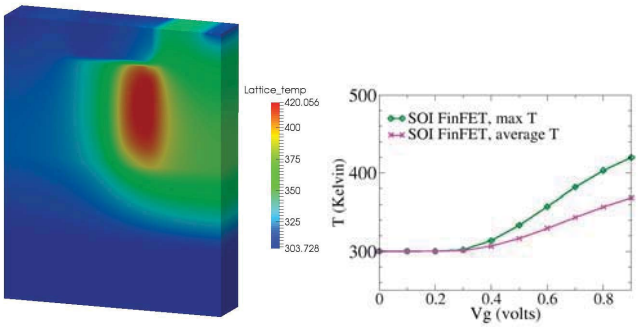

(a) Case 1



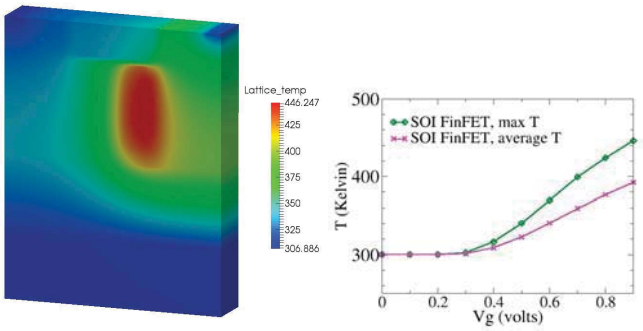

(b) Case 2




(c) Case 3




(d) Case 4




(e) Case 5

Fig. 4. Lattice temperature distributions at high drain and high gate biases (left) and the temperature variation with gate voltage at high drain (right), resulting from the 3D couped electro-thermal simulations for five cases.

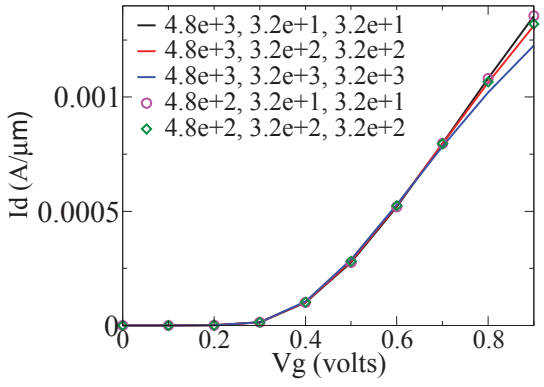



Fig. 5. Id-Vg characteristics at high drain bias from the 3D electro-thermal simulations, comparing five cases.

TABLE III. COMPARISON OF RESULTS FROM THE 3D COUPLED ELECTRO-THERMAL SIMULATION FOR THE SOI FINFET EXAMPLE AT HIGH DRAIN BIAS

| | *Peak temperature (K)* | *Average Temperature (K)* | *On-current (μA)* |
|---|---|---|---|
| Case 1 | 420.30 | 368.74 | 97.54 |
| Case 2 | 448.94 | 395.11 | 94.56 |
| Case 3 | 484.13 | 432.71 | 88.21 |
| Case 4 | 420.06 | 368.51 | 97.57 |
| Case 5 | 446.25 | 392.43 | 95.02 |

## IV. CONCLUSOINS

The electro-thermal simulation capabilities of the drift-diffusion simulator GARAND were enhanced by the development of a thermal conductivity model taking into account the effects of thermal confinement in FinFETs. The 3D coupled electro-thermal simulation results for an SOI FinFET, targeting the 14/16nm CMOS technology generation, has been presented. The lattice temperature profiles under different external thermal resistances connected to the gate and the corresponding Id-Vg characteristics are investigated and analysed. The results show a significant hot spot generated near the drain because of the much lower thermal conductivity of the fin, as the peak lattice temperature exceeds 420 K for all five cases in this study, and strong temperature gradients are also generated in this region. The impact of external thermal resistances at different places connected to the gate is different, consequently affecting the electrical performance of the SOI FinFET.

## REFERENCES

[1] I. N. Adisusilo, K. Kukita, and Y. Kamakura. “Analysis of Heat Conduction Property in FinFETs Using Phonon Monte Carlo Simulation, ” Proc. SISPAD 2014, pp.17-20, Sep. 2014.

[2] S. Kolluri, K. Endo, E. Suzuki, K. Banerjee. “Modelling and analysis of self-heating in FinFET devices for improved circuit and EOS/ESD performance,” IEDM 2007, Dec 2007.

[3] T. Sadi, R.W. Kelsall and N. J. Pilgrim, “Electrothermal Monte Carlo Simulation of Submicrometer Si/SiGe MODFETs”, IEEE Trans. Electron. Dev., Vol. 54, No. 2, pp. 332-339, 2007

[4] C. Auth, C. Allen, A. Blattner, et al. “A 22 nm high per- formance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors,” in Proc. VLSI Technol. Symp., pp. 131–132, June 2012.

[5] L. Wang, A. R. Brown, et al. “3D Coupled Electro-Thermal FinFET Simulations Including the Fin Shape Dependence of the Thermal Conductivity,” Proc. SISPAD 2014, pp.269-272, Sep. 2014.

[6] GARAND Statistical 3D TCAD Simulator [Online]. Available: http://www.GoldStandardSimulations.com/products/garand/

[7] L. Wang, A. R. Brown, et al. “Impact of Self-Heating on the Statistical Variability in Bulk and SOI FinFETs,” *IEEE Trans Electron Dev*., Vol.62, No.7, pp.2106-2112, July 2015.

[8] L. Wang, A. R. Brown, et al. “3D Electro-Thermal Simulations of Bulk FinFETs with Statistical Variations,” Proc. *SISPAD 2015,* pp.112-115, Sep. 2015.

[9] D. Vasileska, K. Raleva, S. M. Goodnick. “Electrothermal studies of FD SOI devices that utilize a new theoretical model for the temperature and thickness dependence of the thermal conductivity,” IEEE Trans. Electron. Dev., Vol. 57, No. 3, pp.726-728, March 2010.

# Space-Average Impurity-Limited Resistance and Self-Averaging in Quasi-1D Nanowires

Nobuyuki Sano
Institute of Applied Physics
University of Tsukuba
Tsukuba, Ibaraki 305–8573, Japan
Email: sano@esys.tsukuba.ac.jp

***Abstract*—The impurity-limited resistance in quasi-one dimensional (quasi-1D) nanowires is studied under the framework of the Lippmann-Schwinger theory. The resistance of a cylindrical nanowire is calculated theoretically under various spatial configurations of localized impurities with a simplified short-range scattering potential and the effects of phase interference are explicitly evaluated. The space-average resistance is then calculated under the uniform distribution of impurities and we find that the space-average resistance at room temperature is well approximated by the uncorrelated series resistance even under the fully coherent circumstances. This is closely related to the "self-averaging" and its physical origin is clarified.**

## I. Introduction

Si nanowires have been receiving great attention in the past few decades because of their possible application of future electronic and photonic devices [1], [2]. However, because of their small structures in size, the device performance often fluctuates over great ranges, depending on the configuration of localized impurities in the substrate [3], [4]. So far, theoretical studies on such variability observed in mobility or resistance of nanowires are limited with large-scale numerical simulations [5]–[10] and it has been demonstrated that the transport properties are indeed fluctuate in short channel nanowires. Clearly, the phase interference would be of crucial importance in understanding the physics behind such variability.

We would also like to point out that the phase interference plays a dominant role in averaging the transport properties such as resistance of long channel devices, in which many impurities are distributed uniformly in the substrate: Many different configurations of impurities in the substrate allows us to use the space-average impurity scattering rates, in spite of the fact that the detail impurity configuration is different for every device. This is called as "self-averaging" and the phase interference is deeply involved [11]. Despite its importance, however, almost no attention has been paid so far on the interference effects among multiple impurities in nanowires.

In this brief report, we study the interference effects associated with localized impurities on the impurity-limited resistance in the quasi-1D nanowires. This is carried out based on the theory formulated recently by the present author [12] and we clarify how and why the phase interference leads to the variability in $R_s$. Then, the physical origin of "self-averaging" emerged under the fully coherent condition is clarified.

## II. Theoretical Foundations

### A. Impurity-limited Resistance

We consider a cylindrical nanowire with the radius of $r_s = 2$ nm and the impurity density in the substrate is assumed to be uniform ($n_{imp} = 2 \times 10^{19}$ cm$^{-3}$), i.e., localized impurities are distributed uniformly in the channel region. The channel length $L$ of the wire changes in accordance with the number of impurities doped in the channel region, namely, $L = 4$ nm for one impurity, 8 nm for two impurities, etc. In addition, the extreme quantum limit, in which only the lowest subband is involved in electron transport, is assumed as the phase interference is most effective.

Theoretical expressions of the impurity-limited resistance due to localized impurities in the nanowires are derived from the Landauer formula under the linear response regime: The conductance $G$ through the doped channel region is calculated from the transmission coefficient of the in-coming electrons from the reservoirs (source and drain). The transmission and the reflection coefficients are calculated from the asymptotic forms of the scattered wave functions by solving the Lipmann-Schwinger (LS) equation [12]–[14]. It should be noted that the total resistance $R_{tot}$ given by the inverse of $G$ consists of two contributions; the contact resistance and the channel resistance [15]. The former results from the difference in the number of modes between the lead and reservoirs, whereas the latter is due to the scattering potential by ionized impurities, phonons, surface roughness, and the long-range potential modulation [12]. This potential modulation is, further, attributed to the long-range part of the Coulomb potential of ionized impurities/carriers as well as the applied gate voltage, as schematically drawn in Fig. 1. In order to extract the impurity-limited resistance from the total resistance, we consider only impurity scattering and the resistance caused by the long-range potential modulation is eliminated by assuming that the channel potential is flat along the wire axis. As a consequence, the impurity-limited resistance is obtained by subtracting the contact resistance from the total resistance, $R_s = R_{tot} - R_0$, and, thus, given by

$$R_s = \frac{\pi\hbar}{e^2}\frac{\langle R_A(E)\rangle}{1-\langle R_A(E)\rangle} = \frac{\pi\hbar}{e^2}\left\{\langle R_A(E)\rangle + \left(\langle R_A(E)\rangle\right)^2 + \cdots\right\} \quad (1)$$

ISBN 978-1-4673-8608-1

IEEE Catalog number CFP1649D-USB

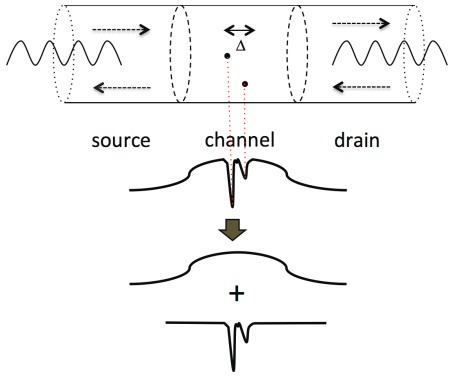



Fig. 1. Schematic drawings of the nanowire with two impurities doped in the channel and the corresponding potential profile under the applied gate voltage. The whole potential modulation is treated as a single scattering potential under the framework of the scattering theory. The impurity-limited resistance is attributed to the screened scattering potential (the lowest part of the figure).

with

$$\langle R_A(E)\rangle = \int_{-\infty}^{\infty} dE\, R_A(E) \left(-\frac{\partial f_{FD}(E)}{\partial E}\right), \qquad (2)$$

where $R_A(E)$ is the reflection coefficient of the in-coming electrons with the total energy $E$ in the lowest subband $A$. $f_{FD}(E)$ is the Fermi-Dirac distribution in the reservoirs. We assume that the chemical potential *in the reservoirs* is well above the bottom of the lowest subband in the channel. If $R_s$ is truncated by the first term in the last expression of Eq. (1), it corresponds to the usual Born approximation.

### B. Transmission and Reflection Coefficients

As for the scattering potential due to localized impurities, we employ the short-range $\delta$-function potential defined by

$$V(\mathbf{R}) = \sum_{r=1}^{N_{imp}} (v_c a S)\, \delta^{(3)}(\mathbf{R} - \mathbf{R}_{0r}), \qquad (3)$$

where $N_{imp}$ is the number of impurities in the channel, $v_c$ is the scattering potential energy, $a$ is the characteristic length along the axis direction over which the scattering potential is effective, and $S$ is the cross-sectional area of the wire. $\mathbf{R}_{0r} = (\mathbf{r}_{0r}, z_{0r})$ is the position of the $r$-th impurity ($r = 1, 2, \cdots, N_{imp}$). The exact transmission and reflection coefficients are derived from the LS equation and, respectively, given by

$$T_A(E) = \left|1 + I^-\right|^2 \quad \text{and} \quad R_A(E) = \left|I^+\right|^2. \qquad (4)$$

By employing the matrix representation with respect to the impurity site indices, $I^{\mp}$ is expressed by

$$I^{\mp} = -i\frac{m}{\hbar^2 k} \begin{pmatrix} e^{\mp ikz_{01}} & e^{\mp ikz_{02}} & \cdots & e^{\mp ikz_{0N_{imp}}} \end{pmatrix} \hat{\Xi}\left(\frac{1}{1-\hat{\Sigma}}\right) \begin{pmatrix} e^{ikz_{01}} \\ e^{ikz_{02}} \\ \vdots \\ e^{ikz_{0N_{imp}}} \end{pmatrix}. \qquad (5)$$

$$R_A(E) = \frac{\gamma_1^2 + \gamma_2^2 + 2\gamma_1^2\gamma_2^2 + 2\gamma_1\gamma_2\left\{(1-\gamma_1\gamma_2)\cos(2k\Delta) + (\gamma_1+\gamma_2)\sin(2k\Delta)\right\}}{1 + \gamma_1^2 + \gamma_2^2 + 2\gamma_1^2\gamma_2^2 + 2\gamma_1\gamma_2\left\{(1-\gamma_1\gamma_2)\cos(2k\Delta) + (\gamma_1+\gamma_2)\sin(2k\Delta)\right\}}$$

with $\gamma_r(E, \mathbf{r}_{0r}) = v_c \frac{a}{\hbar}\sqrt{\frac{m}{2(E-\varepsilon_A)}} S\left|\xi_A(\mathbf{r}_{0r})\right|^2 \quad (r = 1, 2)$

$\Delta = z_{01} - z_{02}$

Fig. 2. Exact expression for the reflection coefficient of two correlated impurities at $\mathbf{R}_{01}$ and $\mathbf{R}_{02}$ derived from the LS equation.

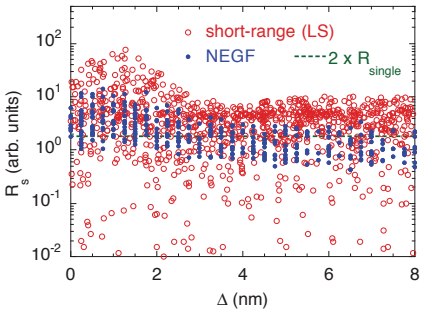



Fig. 3. Impurity-limited resistances of two impurities for 1000 different configurations as a function of the impurity separation $\Delta$ along the wire axis. The scattering potential energy is $v_c = 183$ meV. The solid symbols represent similar results from the NEGF simulations for acceptor impurities. The horizontal (green) dashed line shows $2R_s^{single}$, with $R_s^{single}$ being the single-impurity resistance averaged over the impurity configurations.

The total energy of electron is given by $E = \hbar^2 k^2/(2m) + \varepsilon_A$ and $\varepsilon_A$ is the lowest subband energy. The matrix elements of $\hat{\Xi}$ and $\hat{\Sigma}$ are, respectively, given by

$$(\hat{\Xi})_{rs} = \Xi^r \delta_{r,s} \quad \text{and} \quad (\hat{\Sigma})_{rs} = -i\frac{m}{\hbar^2 k} e^{ik|z_{0r} - z_{0s}|} \Xi^s, \qquad (6)$$

where $\Xi^r = v_c a S |\xi(\mathbf{r}_{0r})|^2$, with $\xi(\mathbf{r}_{0r})$ being the subband wavefunction at the $r$-th impurity site. As a concrete example, the exact expression for the reflection coefficient $R_A(E)$ of two correlated impurities is presented in Fig. 2.

## III. Results and Discussion

### A. Variability in $R_s$ and Phase interference

We first show the impurity-limited resistance $R_s$ of two correlated impurities for 1000 different configurations as a function of the impurity separation $\Delta$ in Fig. 3. The scattering potential energy is set at $v_c = 183$ meV, corresponding to the screening length of $\lambda_{sc} = 2$ nm. The resistances $R_s$ greatly scatter over wide ranges and such large fluctuations result from two different physical origins: The fluctuations in $R_s$ at fixed $\Delta$ are attributed to the variations in $\Xi_r$ (the subband wavefunctions), whereas the fluctuations along the wire axis direction $\Delta$ are due to the phase interference of electrons among the impurities. The former has nothing to do with the phase correlation among multiple impurities and, thus, the fluctuations diminish as the number of ensembles increases, owing to the central limit theorem [16]. On the other hand, the variations of $R_s$ along the $\Delta$ direction do not generally

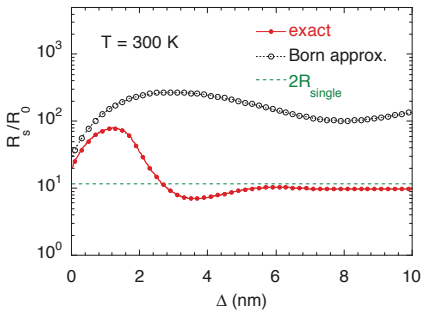



Fig. 4. Impurity-limited resistance of two impurities located on the wire axis at $T = 300$ K. $R_s$ from the exact formula (red solid line) and the Born approximations (black dotted line) are plotted. The horizontal (green) line shows $2R_s^{single}$, with $R_s^{single}$ being the single-impurity resistance located on the wire axis.

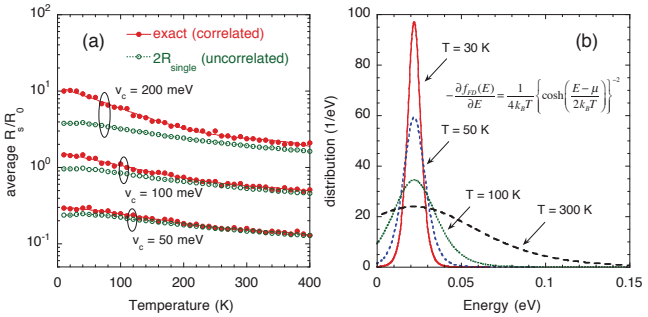



Fig. 5. (a) Ensemble average resistance of two impurities under uniform distribution as a function of temperature of the reservoirs. $2R_{single}$ represents the uncorrelated limit, where $R_{single}$ is the ensemble average resistance of the single-impurity under uniform distribution. (b) Energy dependence of the distribution $(-\partial f_{FD}(E)/\partial E)$ included in Eq. (2) at four different temperature of the reservoirs.

vanish, as noted by Kohn and Luttinger [11]. For comparison, similar results from more elaborate NEGF simulations [17], in which the screened Coulomb potential is adopted for acceptor impurities, are also shown in Fig. 3. Although the device structure employed in the NEGF simulations is a square nanowire with the side length of 3.5 nm, the difference in shape is insignificant here because the cross-sectional area is very similar in both cases. The fluctuations associated with the subband wavefunction (and the screened Coulomb potential) are greatly suppressed due to the long-range nature of the scattering potential. However, the variations of $R_s$ along the $\Delta$ direction are very similar to those calculated from the LS equation with the short-range scattering potential.

In order to eliminate the fluctuations associated with the subband wavefunctions, we carry out similar calculations by placing two impurities on the wire axis. The calculation results from the exact formula and the Born approximation are shown in Fig. 4 along with the uncorrelated value $2R_{single}$, where $R_{single}$ is the resistance of the *single-impurity* located on the axis. $R_0$ is the quantum resistance and given by $R_0 = \pi\hbar/e^2$. It is clear that the Born approximation completely breaks down and, thus, the coupling between the electron and impurity is indeed enhanced due to the confinement in nanostructures. More importantly, a large oscillatory behavior in the exact $R_s$ is observed in the first few nm. This oscillation results from the trigonometric dependence in the reflection coefficient $R_A(E)$, as shown in Fig. 2, and represents the constructive phase interference among two impurities. However, this oscillation rapidly damps and $R_s$ approaches $2R_{single}$, that is, the uncorrelated limit. This is a rather surprising result because no averaging over the configurations of impurities nor energy dissipating scattering is included in this case. In other word, the phase randomization is taking place under the fully coherent circumstances.

### B. Self-Averaging

The fact that the impurity-limited resistance of two impurities approaches the uncorrelated value of $2R_{single}$ implies that the phase correlation between the impurities is somehow washed out as the impurity separation along the wire axis becomes large, namely, larger than some phase correlation length $\Delta_{phase}$. This is expected to be true for the cases of three or more impurities. In the present case, $\Delta_{phase}$ is about 3 nm and much smaller than the channel length $L$ ($\sim 8$ nm). Therefore, if one takes an ensemble average of the resistance under the uniform impurity distribution, the space-average resistance becomes very close to the uncorrelated resistance unless the scattering potential energy $v_c$ is extremely large. In other words, the space-average resistance would be a simple sum of $\bar{R}_{single}$, where $\bar{R}_{single}$ is the space-average resistance of the *single-impurity* under the uniform impurity configurations.

In fact, the physical origin of the phase randomization along the $\Delta$ direction is closely related to the broadness of energy spectrum of the in-coming electrons from the reservoirs (source and drain). That is, $R_s$ is averaged by the in-coming electrons with many different kinetic energies (wavelengths) when the spectrum is broad (or equivalently, temperature of the reservoirs is high). Therefore, it is conjectured that at low temperature, at which the energy spectrum of the in-coming electrons is limited to be very narrow around the Fermi energy of the reservoirs, the phase coherence would last much longer distances and the average resistance would deviate from the uncorrelated resistance. This is confirmed from Fig. 5(a), in which the space-average resistance of two correlated impurities under the uniform distribution is plotted as a function of temperature of the reservoirs. The uncorrelated average resistance, $2\bar{R}_{single}$, is also shown. Figure 5(b) shows the energy spectrum of the in-coming electrons from the reservoirs, namely, the distribution $(-\partial f_{FD}(E)/\partial E)$ included in Eq. (2), at four different temperature of the reservoirs. The distribution is normalized to unity and the chemical potential of the reservoirs is assumed to be the same at each temperature for simplicity. It is clear that the space-average resistance of two impurities becomes quite close to the uncorrelated resistance (the series resistance of single-impurity, $2\bar{R}_{single}$) as temperature of the reservoirs rises.

Hence, a broad energy spectrum of the in-coming electrons leads to phase randomization among impurities and as a result, each impurity could be regarded as an independent scattering center. This allows us to apply the central limit theorem to the fluctuations in $R_s$ along the $\Delta$ direction and, thus, the fluctuations would diminish as the number of ensembles (impurity configurations) increases. This is equivalent to saying that in the long channel nanowires where many impurities are doped, the impurity-limited resistance, that is explicitly dependent of the impurity configuration, approaches the space-average resistance as the number of impurity increases. This is exactly what the "self-averaging" implies, in which the configuration-dependent quantity such as resistance could be replaced with the space-averaged quantity if the number of impurities is large. Therefore, we may claim that the "self-averaging" under the quasi-1D nanowires is attributed to the broadness of the energy spectrum of the in-coming electrons from the reservoirs.

## IV. Conclusion

We have investigated the phase interference effects on the impurity-limited resistance due to localized impurities in the quasi-1D nanowires. We have found that the space-average resistance of multiple impurities at room temperature is very close to the series resistance of the averaged single-impurity resistance and that the phase randomization is induced by the in-coming electrons from the reservoirs with a broad energy spectrum. The deviation from the uncorrelated value becomes significant as temperature of the reservoirs is lowered. In this case, the whole scattering potential associated with multiple impurities needs to be treated coherently. We have also pointed out that the phase randomization observed at room temperature is equivalent to the "self-averaging" encountered in long channel devices under uniform impurity distribution and its physical mechanism under the quasi-1D nanostructures has been clarified.

## Acknowledgment

This work was supported in part by Ministry of Education, Science, Sports, and Culture under Grant-in- Aid for Scientific Research (B) (no. 15H03983).

## References

[1] J. Appenzeller, J. Knoch, M. Bjork, H. Riel, H. Schmid, and W. Riess, "Toward nanowire electronics," *IEEE Trans. Electron Dev.*, vol. 55, no. 11, pp. 2827–2845, Nov 2008.

[2] R. Rurali, "*Colloquium* : Structural, electronic, and transport properties of silicon nanowires," *Rev. Mod. Phys.*, vol. 82, pp. 427–449, Feb 2010.

[3] N. Sano, K. Matsuzawa, M. Mukai, and N. Nakayama, "Role of long-range and short-range coulomb potentials in threshold characteristics under discrete dopants in sub-0.1 $\mu$m Si-MOSFETs," in *Technical Digest. Int. Electron Devices Meeting, IEDM'00*. IEEE, 2000, pp. 275–278.

[4] ——, "On discrete random dopant modeling in drift-diffusion simulations: physical meaning of 'atomistic' dopants," *Microelectronics Reliability*, vol. 42, no. 2, pp. 189 – 199, 2002.

[5] R. Rurali, T. Markussen, J. Sune, M. Brandbyge, and A.-P. Jauho, "Modeling transport in ultrathin si nanowires: Charged versus neutral impurities," *Nano Letters*, vol. 8, no. 9, pp. 2825–2828, 2008.

[6] M. P. Persson, H. Mera, Y.-M. Niquet, C. Delerue, and M. Diarra, "Charged impurity scattering and mobility in gated silicon nanowires," *Phys. Rev. B*, vol. 82, pp. 115318-1–115318-8, Sep 2010.

[7] Y.-M. Niquet, H. Mera, and C. Delerue, "Impurity-limited mobility and variability in gate-all-around silicon nanowires," *Appl. Phys. Lett.*, vol. 100, no. 15, pp. 153119-1–153119-4, 2012.

[8] A. Martinez, M. Aldegunde, N. Seoane, A. Brown, J. Barker, and A. Asenov, "Quantum-transport study on the impact of channel length and cross sections on variability induced by random discrete dopants in narrow gate-all-around silicon nanowire transistors," *IEEE Trans. Electron Dev.*, vol. 58, no. 8, pp. 2209–2217, Aug 2011.

[9] M. Aldegunde, A. Martinez, and J. Barker, "Study of discrete doping-induced variability in junctionless nanowire mosfets using dissipative quantum transport simulations," *IEEE Trans. Electron Dev.*, vol. 33, no. 2, pp. 194–196, Feb 2012.

[10] S. Sylvia, K. Habib, M. Khayer, K. Alam, M. Neupane, and R. Lake, "Effect of random, discrete source dopant distributions on nanowire tunnel fets," *IEEE Trans. Electron Dev.*, vol. 61, no. 6, pp. 2208–2214, June 2014.

[11] W. Kohn and J. M. Luttinger, "Quantum theory of electrical transport phenomena," *Phys. Rev.*, vol. 108, pp. 590–611, Nov 1957.

[12] N. Sano, "Impurity-limited resistance and phase interference of localized impurities under quasi-one dimensional nano-structures," to be published in *J. Appl. Phys.*

[13] R. G. Newton, *Scattering Theory of Waves and Particles*. New York: Dover, 2002.

[14] J. R. Taylor, *Scattering Theory: the Quantum Theory of Nonrelativistic Collisions*. New York: Dover, 2000.

[15] M. DiVentra, *Electrical Transport in Nanoscale Systems*. UK: Cambridge University Press, 2008.

[16] W. Feller, *An Introduction to Probability Theory and Its Applications*. Wiley, January 1968, vol. 1.

[17] N. Sano, M. R. Zulhidza, Y. Kaneno, S. Honda, A. Ueda, and K. Yoshida, "Correlation effects of localized impurities on electron transport under 1-D nano-structures," *J. Phys.: Conf. Series*, vol. 647, no. 1, pp. 012028-1–012028-4, 2015.

# Numerical Analysis and Analytical Modeling of RDF in DG Tunnel-FETs

Michael Graef[1,2,✠], Franziska Hain[1,2], Fabian Hosenfeld[1,2], Fabian Horst[1,2], Atieh Farokhnejad[1,2], Benjamín Iñíguez[2] and Alexander Kloes[1]
[1]Competence Centre for Nanotechnology and Photonics, Technische Hochschule Mittelhessen, Giessen, Germany
[2]DEEEA, Universitat Rovira i Virgili, Tarragona, Spain
[✠]michael.graef@ei.thm.de

***Abstract*—The ongoing scaling of semiconductor devices is leading to a growing influence of discrete dopants on the device electrostatics. This discretization is accompanied by an increasing dependency of the resulting device currents on the dopant distribution. Hence, the need to consider random dopant fluctuations (RDF) in compact models is a necessity to predict and understand present device current variances. In this paper a first approach is presented to predict device geometry based RDF. The model is compared to different TCAD simulation methods for RDF in DG-Tunnel-FETs. Thereby, an untypical behavior special to Tunnel-FETs is discovered, where decreasing doping levels result in higher gate voltage variances. Furthermore, a negative effect of discrete dopants on the steepness of the subthreshold slope is discussed.**

***Index Terms*—Random Dopant Fluctuation (RDF), Impedance Field Method (IFM), Randomized Profiles,Gaussian Doping Profiles, MOSFET, Double-Gate (DG) Tunnel-FET.**

## I. Introduction

Nowadays, Tunnel-FETs have become one of the most promising candidates to be the successor of the current MOSFET technology [1]. Due to the alternative current transport mechanism, tunneling currents at the channel barriers, it provides the possibility to overcome the thermionic-emission based subthreshold slope (S) limitation of 60 $\frac{mV}{dec}$. The combination of high doping concentrations in source (s) and drain (d) region of Tunnel-FETs with an intrinsic channel leads to a diffusion of dopants from s/d towards the channel region (see Fig. 1). This greatly affects the subthreshold slope as well as the maximum ON-state current of the device [2]. One downside of the transistor miniaturization nowadays is that doping concentrations are not constant within specific regions but have to be considered at discrete locations. Therefore, these discrete dopants have an increased influence on the electrostatic potential in the device. Random dopant fluctuation (RDF) hereby describes the statistical variation of discrete dopants within the channel region. The model presented in this paper captures this RDF effect on MOSFET electrostatics by an equivalent variation of the gate voltage ($V_g$). The model can be applied on different conventional double-gate (DG) transistor structures and in this case it is specifically applied to the DG Tunnel-FET.

## II. TCAD Simulation

There are two different methods to simulate the RDF-effect with a FEM simulator. For these simulations the following device geometry is used.

### A. Device Geometry

With the simulator TCAD Sentaurus a Si DG-n-Tunnel-FET is investigated. The device consists of a highly p-doped source region $N_s = 10^{20}$ cm$^{-3}$, a slightly reduced n-doped drain region $N_d = 10^{19}$ cm$^{-3}$ and an intrinsic channel. Gaussian shaped doping profiles are applied at the channel junctions (see Fig. 1) with a standard deviation $\sigma = 1, 2, 3$ nm. Exponentially distributed traps at the channel junctions are assumed with a maximum trap concentration $N_{Tmax} = 10^{12}\ cm^{-2}eV^{-1}$ [3]. Due to an improved electrostatic control on the gate region the high-$\kappa$ oxide material $HfO_2$ is used [1]. The device dimensions are chosen to be: $t_{ox} = 2$ nm, $t = 10$ nm, $l_{ch} = 22$ nm and $l_{sd} = 20$ nm. A nonlocal tunneling model was used in the simulation.

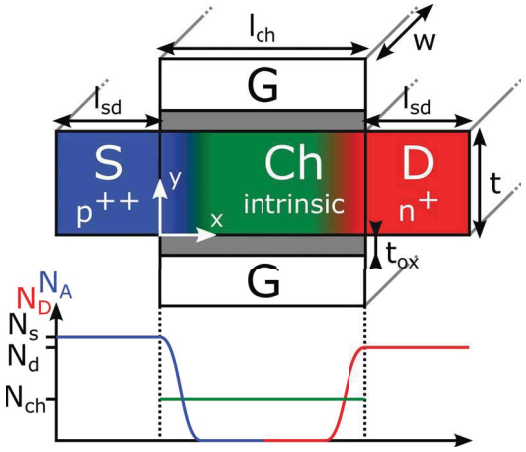



Figure 1. Geometry of a DG-n-Tunnel-FET, showing the doping profiles at the channel junctions and structural parameters.

### B. Impedance Field Method

At first RDF was simulated in 2D using the impedance field method (IFM). This method is comparable to noise modeling [4]. Hence, for each point of the device, RDF is described by the second-order statistical moments of the dopant distribution.

These moments are modeled using an analytical function. Using IFM, it is possible to describe the influence of small dopant fluctuations on the applied terminal voltages [5]. Figure 2 shows the simulation results for the device. The plot shows the device current $I_d$, its standard deviation $\sigma_{I_d}$, the relative standard deviation of the device current $rel.\sigma_{I_d} = \frac{\sigma_{I_d}}{I_d}$ and the resulting standard deviation of the gate voltage $\sigma_{V_g}$. Due to the constant current in the devices OFF-state (0.1 V$\leq V_g \leq$ 0.5 V), a small current change leads to a significant gate voltage variation $\sigma_{V_g}$.

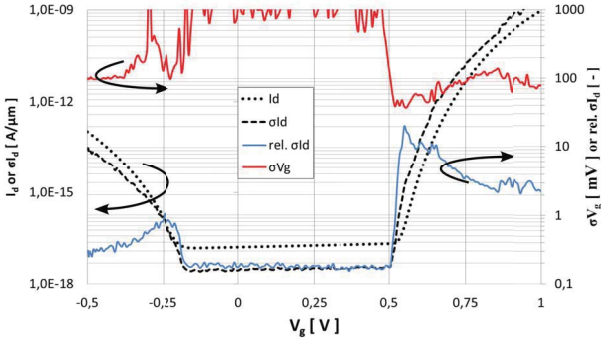



Figure 2. 2D TCAD results for a DG n-Tunnel-FET using IFM for $\sigma = 1$ nm and $V_d = 0.5$ V. The results for $\sigma_{V_g}$ are scaled for $w = 30$ nm using equation (9).

### C. Randomized Profiles

Another method of simulating RDF is with the use of randomized profiles. Therefore, the device is extended in the $3^{rd}$ dimension ($w = 30$ nm) and discrete dopants are used for the simulation. This is done for a specific number of samples $N$. The average current $I_{dAvr}$ is calculated with

$$I_{dAvr}(V_g) = \frac{1}{N}\sum_{k=1}^{N} I_d^k(V_g) \tag{1}$$

and for standard deviation of $I_d$ follows

$$\sigma_{I_d}(V_g) = \frac{1}{N}\sqrt{\sum_{k=1}^{N}\left(I_d^k(V_g) - I_{dAvr}(V_g)\right)^2}. \tag{2}$$

The standard deviation of $V_g$ can be calculated using the inverse expressions of $I_d$: $V_g(I_d)$

$$\sigma_{V_g}(V_g(I_{dAvr})) = \frac{1}{N}\sqrt{\sum_{k=1}^{N}\left(V_g^k(I_{dAvr}) - V_g(I_{dAvr})\right)^2}. \tag{3}$$

In figure 3 the results are shown for $N = 10$ random samples, therefore only general trends can be observed.

One can see that the gate voltage deviation $\sigma_{V_g}$ is much higher in the ambipolar-state in contrast to the ON-state of the device. The reduced drain doping leads to less discrete dopants, which makes their distribution much more sensitive on the device electrostatics. Therefore, dopants located near the gate oxide at the drain/channel junction (Fig. 4 a), b)) may cause a spike in the band diagram (Fig. 4 c)), which could massively reduce the tunneling distance. Note that the tunneling current has a exponential dependency on the tunneling distance [6]. The effect of an increasing $\sigma_{V_g}$ for a decreasing doping level seems to be characteristic special to Tunnel-FETs. In [7] a similar behavior was observed in a SiGe-Tunnel-FET, where a change of the tunneling direction was suspected to be the reason of the $\sigma_{V_{th}}$ increase.

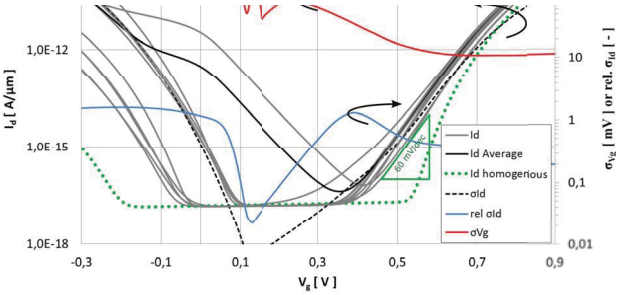



Figure 3. TCAD results for a DG n-Tunnel-FET using randomized doping profiles with $w = 30$ nm, $\sigma = 1$ nm and $V_d = 0.5$ V.

In general, fabricated devices show a worse subthreshold slope than their associated simulations. The reasons for that were suspected to be the trap assisted tunneling or doping profiles at the channel junctions. However, figure 3 shows an additional reason for an significant degradation of the subthreshold slope. Considering discrete dopants instead of homogeneous doping within the simulation could lead to more realistic simulation results for a better fitting subthreshold slope estimation.

The high $\sigma_{V_g}$ in the OFF-state is caused by the constant current in said state.

## III. Modeling Approach

The aim of the model is to capture the influence of random dopants in the channel region on the gate charge. Therefore, for every dopant, the associated gate charge is calculated, followed by an estimation of the equivalent change in $V_g$ using the oxide capacitance $C_{ox}$. This can be done discretely for every dopant or in general, using the expected dopants in a small area of the channel region. Considering the variation of the doping concentration in the discrete volume this directly leads to the variation of $V_g$. At first the channel region has to be meshed (see Fig. 5).

The expected total number of dopants can be calculated for every central point of a mesh element:

$$N = \Delta y \int_{\Delta x} N_s \cdot e^{-\frac{x^2}{\sqrt{2\sigma^2}}} \cdot dx + \Delta y \int_{\Delta x} \left( N_d \cdot e^{-\frac{(x-l_{ch})^2}{\sqrt{2\sigma^2}}} + N_{ch} \right) \cdot dx \tag{4}$$

Assuming a Poisson distribution for the dopants, the expected value $N$ equals the variance of the dopants $\sigma_N^2$ [5]. Con-

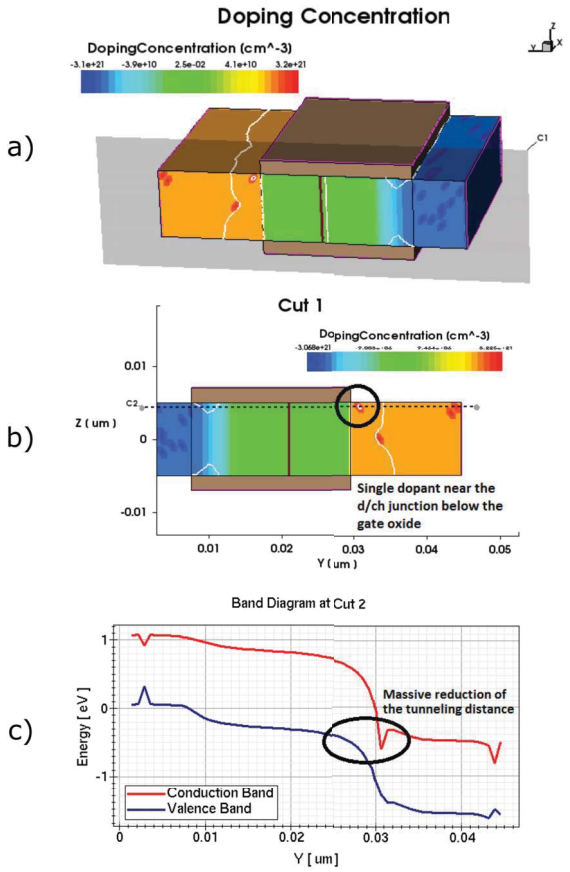



Figure 4. Influence of single dopants on the band structure at $V_g = -0.5$ V, $V_d = 0.5$ V. a) DG-Tunnel-FET device with blue source, yellow drain and green channel region, applying cut 1. b) 2D cut through the single dopant located near the drain/channel-junction and below the oxide, applying cut 2. c) Band structure along cut 2, showing the dopant caused spike and the massive reduction of the tunneling distance.

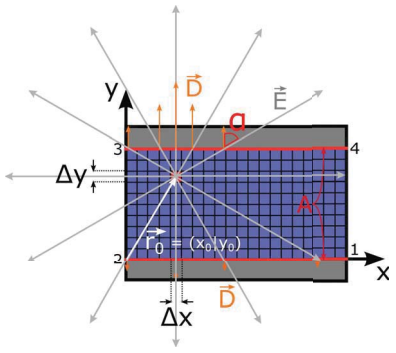



Figure 5. Meshing of the channel region and calculation of the D-field components below the gate oxides for a specific position in the channel.

sidering a point charge without boundaries, the electric field variance of these charges is given through:

$$|\sigma^2_{\vec{E}}(\vec{r} - \vec{r_0})| = \frac{q \cdot \sigma_N^2}{2\pi\epsilon|\vec{r} - \vec{r_0}|} \tag{5}$$

In order to get the equivalent charge variance $\sigma_Q^2$, the D-field variance ($\sigma^2_{\vec{D}} = \epsilon \cdot \sigma^2_{\vec{E}}$) orthogonal to the gate oxides has to be integrated (see Fig. 5) [8].

$$\sigma_Q^2(x_0, y_0) = \int_1^2 |\sigma^2_{\vec{D}}(x_0, y_0)| \cdot \cos(\alpha) \cdot dx + \int_3^4 |\sigma^2_{\vec{D}}(x_0, y_0)| \cdot \cos(\alpha) \cdot dx \tag{6}$$

Considering $cos(\alpha) = \frac{y - y_0}{|\vec{r} - \vec{r_0}|}$ and $|\vec{r} - \vec{r_0}| = \sqrt{(x - x_0)^2 + (y - y_0)^2}$ eqn. (6) simplifies to

$$\begin{aligned}\sigma_Q^2(x_0, y_0) &= \int_1^2 \frac{q \cdot \sigma_N^2}{2\pi\epsilon|\vec{r} - \vec{r_0}|} \cdot \frac{y - y_0}{|\vec{r} - \vec{r_0}|} \cdot dx + \int_3^4 \frac{q \cdot \sigma_N^2}{2\pi\epsilon|\vec{r} - \vec{r_0}|} \cdot \frac{y - y_0}{|\vec{r} - \vec{r_0}|} \cdot dx \\ &= \frac{q \cdot \sigma_N^2}{2\pi\epsilon} \int_1^2 \frac{(y - y_0)}{(x - x_0)^2 + (y - y_0)^2} \cdot dx + \frac{q \cdot \sigma_N^2}{2\pi\epsilon} \int_3^4 \frac{(y - y_0)}{(x - x_0)^2 + (y - y_0)^2} \cdot dx \\ &= \frac{q \cdot \sigma_N^2}{2\pi\epsilon} \cdot \left[\arctan\left(\frac{x - x_0}{y - y_0}\right)\right]_1^2 + \frac{q \cdot \sigma_N^2}{2\pi\epsilon} \cdot \left[\arctan\left(\frac{x - x_0}{y - y_0}\right)\right]_3^4\end{aligned} \tag{7}$$

For the calculation of the gate voltage variance $\sigma^2_{V_g}$ of the device follows from integration over all discrete point charges

$$\sigma^2_{V_g} = \int_{t_{inv}}^{t_{ch} - t_{inv}} \int_0^{l_{ch}} Q_{fit} \frac{\sigma_Q^2(x, y)}{C_{ox}} dx \cdot dy, \tag{8}$$

with $C_{ox} = \epsilon_{ox}/t_{ox} \cdot 2 \cdot l_{ch}$, the assumed inversion layer thickness $t_{inv}$ and a fit factor $Q_{fit}$, which compensates the assumed point charge without boundaries. The standard deviation of the gate voltage is then given through $\sigma_{V_g} = \sqrt{\sigma^2_{V_g}}$. The width of the device can be considered with [5]

$$\sigma^{3D}_{V_g} = \sigma^{2D}_{V_g} \cdot \sqrt{1cm/w}. \tag{9}$$

The consideration of the inversion layer thickness results in a slight increase of $\sigma_{V_g}$ in the devices ON- and ambipolar-state. Therefore, the devices threshold voltages are estimated using its band structure parameters $V_{th_{ON}} \approx 0.527$ V and $V_{th_{amb}} \approx -0.065$ V. The inversion layer is then assumed to expand linearly

$$t_{inv,ON} = \frac{t_{max,ON}}{1V - V_{th_{ON}}} \cdot (V_g - V_{th_{ON}}) \tag{10}$$

$$t_{inv,amb} = \frac{t_{max,amb}}{-0.5V - V_{th_{amb}}} \cdot (V_g - V_{th_{amb}}) \tag{11}$$

## IV. Model Verification

The model is compared to the TCAD simulation data for different standard deviations of the doping profiles $\sigma$. At first, figure 6 shows the comparison of the model with the IFM simulation data. Therefore, the device width was converted to $w = 30$ nm using equation (9). Due to the single dopant sensitivity at the drain-to-channel junction $\sigma_{V_g}$ is increased in the ambipolar region (see Fig. 6).

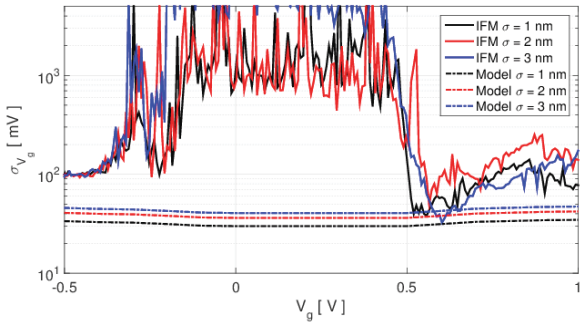



Figure 6. Comparison of the IFM TCAD Simulation data for the standard deviation of $V_g$ with the model at $V_d = 0.5$ V, $Q_{fit} = 1.4$, $t_{max,ON} = 2$ nm and $t_{max,amb} = 1$ nm. The device parameters are listed in section II-A.

As mentioned above, this is a typical effect special to TFETs, which is not yet captured in the model. Nevertheless, it is able to give a first estimation of $\sigma_{V_g}$ and predict its trend in the ON-state of the device. In Figure 7 the model is compared to the randomized profile TCAD simulation.

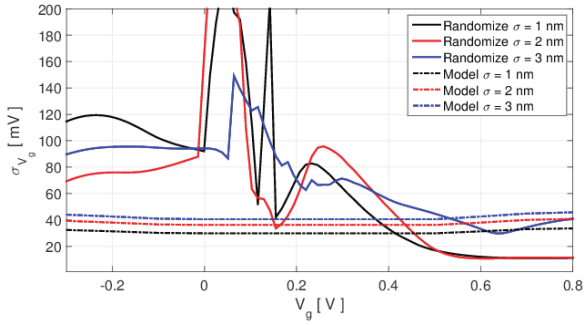



Figure 7. Comparison of the Model with the randomize simulation data at $V_d = 0.5$ V, $Q_{fit} = 1.4$, $t_{max,ON} = 2$ nm and $t_{max,amb} = 1$ nm. $\sigma_{V_g}$ calculation with eqn. (3) using N = 10 samples.

Due to the small number of samples the randomize simulation data only shows a general trend for $\sigma_{V_g}$. One can see that the reduced drain doping is also resulting in a much bigger gate voltage variation in the ambipolar-state in comparison to the ON-state of the device. In the last plot a comparison of the model with the IFM- and randomize simulation data is shown.

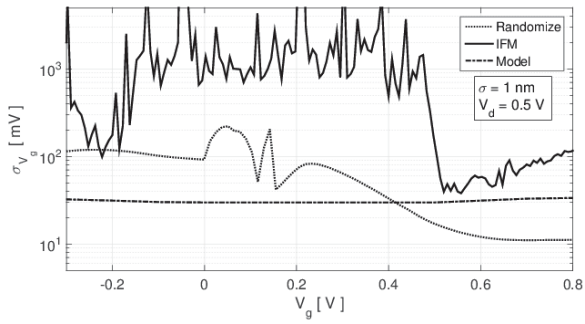



Figure 8. Comparison of the Model, IFM- and Randomize data.

In figure 8 the comparison shows an underestimation of the randomize simulation data in the ON-state, which maybe due to the small number of samples. The model is able to predict the gate voltage variation in the ON-state of the device. Since the reduced doping influence is not yet captured in the model, it is underestimating $\sigma_{V_g}$ in the ambipolar state.

## V. Conclusion

In this paper the influence of RDF in Tunnel-FETs is investigated and a first model is introduced to calculate the gate voltage variance in the ON-state of such devices.

The simulations have brought up effects, which are unique to the Tunnel-FETs RDF behavior. Firstly, a reduction of the doping in Tunnel-FETs is leading to an increasing gate voltage variation. Due to an increased single dopant sensitivity (for lower doping levels) at the channel junctions, the tunneling distance may massively decrease, thus leading to huge device current variations. This effect is not captured by IFM TCAD simulations.

The second effect is a worsening of the subthreshold slope due to discrete dopants, which again is not captured in IFM TCAD simulations. However, this slope degradation shows up in simulations with randomized discrete dopants. The tunnel current flow starting at a specific band overlap is expected to be the advantage of the Tunnel-FET, resulting in a steep switching behavior. The dopant related spikes in the band structure of the device may question this positive effect of the energy limited band-to-band tunneling at the channel junctions, thus leading to an increased subthreshold slope. The introduced model for calculating the standard deviation of the gate voltage is reproducing the general trend in the ON-state of the device.

## Acknowledgments

This work is supported by the German Federal Ministry of Education and Research under contract No.03FH001I3.

## References

[1] A. Seabaugh and Q. Zhang, "Low-Voltage Tunnel Transistors for Beyond CMOS Logic." *Proceedings of the IEEE*, vol. 98, pp. 2095 –2110, dec. 2010.

[2] M. Graef, F. Hain, F. Hosenfeld, B. Iniguez, and A. Kloes, "Analytical approach to consider Gaussian junction profiles in compact models of tunnel-FETs." in *Ultimate Integration on Silicon (EUROSOI-ULIS), 2015 Joint International EUROSOI Workshop and International Conference on*, pp. 213–216, IEEE, 2015.

[3] M. Graef, T. Holtij, F. Hain, A. Kloes, and B. Iniguez, "Two-dimensional modeling of an ultra-thin body single-gate Si Tunnel-FET." in *Ultimate Integration on Silicon (ULIS), 2014 15th International Conference on*, pp. 101–104, IEEE, 2014.

[4] F. Bonani, G. Ghione, M. R. Pinto, and R. K. Smith, "An efficient approach to noise analysis through multidimensional physics-based models." *Electron Devices, IEEE Transactions on*, vol. 45, no. 1, pp. 261–269, 1998.

[5] A. Wettstein, O. Penzin, E. Lyumkis, and W. Fichtner, "Random dopant fluctuation modelling with the impedance field method." in *Proceedings of International Conference on Simulation of Semiconductor Devices and Processes*, pp. 91–94, 2003.

[6] M. Graef, T. Holtij, F. Hain, A. Kloes, and B. Iníguez, "A 2D closed form model for the electrostatics in hetero-junction double-gate tunnel-FETs for calculation of band-to-band tunneling current." *Microelectronics Journal*, vol. 45, no. 9, pp. 1144 – 1153, 2014.

[7] N. Damrongplasit, C. Shin, S. H. Kim, R. A. Vega, and T.-J. K. Liu, "Study of random dopant fluctuation effects in germanium-source tunnel FETs." *Electron Devices, IEEE Transactions on*, vol. 58, no. 10, pp. 3541–3548, 2011.

[8] H. A. Khafaji, "Simulation and Modeling of Nanoscale Double Gate-MOSFETs." Master's thesis, Technische Hochschule Mittelhessen (THM) Gießen, 2014.

# Capacitor-less memory: advances and challenges

Francisco Gamiz
Nanoelectronics Research Group
CITIC-UGR. Universidad de Granada, 18071 Granada, Spain
E-mail: fgamiz@ugr.es

***Abstract*— Several types of floating-body capacitorless 1T-DRAM memory cells are reviewed and compared. We focus on the recently proposed concepts (MSDRAM, A2RAM and Z2FET), by addressing the device architecture and fabrication, operating mechanisms, and scaling issues. Experimental results together with numerical simulations indicate the directions for performance optimization, and their implementation in FDSOI 28nm (FD28) and FDSOI 14nm (FD14) technological nodes. These memory cells are the basis for the recently started European Project REMINDER "Revolutionary Embedded Memory for INternet of Things Devices and Energy Reduction". REMINDER aims to develop an embedded DRAM solution optimized for ultra-low-power consumption and variability immunity, specifically focused on Internet of Things (IoT) cut-edge devices.**

***Keywords—semiconductor memory; Internet-of-Things; floating-body DRAM; low-power***

## I. INTRODUCTION

The Internet of Things (IoT) is a rapidly evolving field that involves the interconnection and interaction of smart objects (objects or devices with embedded sensors, on-board data processing capability, and a means of communication) to provide automated services that would otherwise not be possible. IoT is not a single technology, but rather involves the convergence of memory, sensor, information, communication, and actuation technologies. Today, most of what we consider as IoT is a variety of largely stand-alone devices and isolated systems, such as wearable fitness monitors, home thermostats and lighting, remote video streaming, smartphones, and smart watches. Emerging IoT implementations are expected to be ubiquitous, and they will use smaller and more energy efficient embedded sensor technologies, enhanced communications, advanced data analysis, and more sophisticated actuators to collect and aggregate information and enable intelligent systems that understand context, track and manage complex interactions, and anticipate requirements. New markets involve new memory requirements that in the case of IoT should handle extreme miniaturization and radically lower energy consumption. IoT memory, sensors and processors are conceptually different from current devices because must be kept in live mode all of the time rather than in standby mode, waiting to be awakened. As a result, developers have to reconsider their design goals, by using memory in new and innovative ways. In many cases, this involves using new, or less familiar, memory technologies and examining memory much earlier in their design cycles. The vast majority of embedded memories are currently charged based (DRAM, FLASH) or flip-flop based (SRAM), the last one penalized by its huge area consumption. The other alternative storage options (which are not yet mature from and commercial perspective) can be grouped into three categories, ReRAM (resistive) or MRAM (magnetic), and body charged memories (so called floating-body DRAMs, FB-DRAM).

## II. DRAM MEMORY CELLS

### *A. Standard approach for dynamic memory storage: 1T+1C*

LPDDR4 (low power double data rate 4) DRAM [1] is the current incarnation of the traditional solution of one-transistor + one-capacitor memory (1T+1C) technology. It provides improved speed and power savings, with iterative improvements expected in the future. LPDDR4 offers up to 3200-MHz performance with a 1.2V draw with clearly outperforms the 1.5V power management of LPDDR3[2]. However, in general, the memory cell needs to become smaller, more power efficient, and more cost efficient (complicated technology process). This is the ultimate encumbrance for LPDDR4 integration in the IoT devices, since embedding 1T+1C cells inside the chip remains as a paramount challenge. The use of embedded DRAMs is accelerating due to the tremendous advantages eDRAM offers in chip functionality, chip size and bandwidth for system-on-chip applications. Logic or standalone DRAM technologies have been used to realize eDRAMs. Logic-based technologies offer the advantages of addressing high-end system design needs. They are and of being compatible with existing standard-cell libraries and cores that can just be plugged in, but suffer from high-added cost. A 25 percent cost increase, related to five to eight added masking steps, are typical for standard one-transistor, one-capacitor (1T+1C) DRAM cells integrating complex stacked or trench capacitors.

### *B. Floating-body DRAMs*

Despite Floating-Body Effects (FBE) on SOI are known since the early 90's, the application to FB-DRAM cells did not come out until 2001, when the start-up company Innovative Silicon presented the so-called ZRAM® [3] (commercial name of a FB-DRAM approach). The most appealing feature of FB-DRAMs is its compatibility with the CMOS process and materials, encompassed also with promising performance in terms of density, operation speed and low-power conduction. However, FB-DRAM is yet the most unexplored alternative, essentially because the FDSOI technology was not wide spread commercially. By exploiting the floating-body effect of silicon-on-insulator transistors a one-transistor memory cell can be integrated in a pure standard SOI technology without modifications. The data retention, device operation principles

and reliability make it ideal for high-performance embedded-DRAM [4]. In the last decade different research teams have shown that by using Fully-Depleted SOI transistors, simple capacitorless eDRAM cell can be made without adding a single process step to the CMOS technology. The resulting FB-DRAM cells have an area comparable to regular logic-based eDRAM cells but without being ballasted by and external capacitor. One of the most critical parameters of a new DRAM cell is its data retention. For standalone DRAM applications, retention times of a few hundred milliseconds to a few seconds are targeted at 85ºC. For eDRAM applications, more relaxed constraints are tolerated as a result of the substantially higher bandwidth, and retention times of a few milliseconds are targeted. This is one of the critical aspects that FB-DRAMs need to address to become a mainstream technology. Multiple approaches have shown retention time that can exceed the previous prerequisites, but they are based on relative large devices[5]. When the gate length is reduced to the decananometer range the retention time diminishes substantially[6]. However, most of the tested devices were not optimized for memory operation. It is expected that with advances in the junction and gate engineering the retention characteristics could be improved. Other concepts of single transistor memory cells have been recently proposed: ARAM, A2RAM, MSDRAM, and Z2FET [6-10]. REMINDER project will focus on the latter 3 approaches. All have been demonstrated experimentally to have great potential, albeit their merits (speed, power, scalability) may differ.

## III. 1T-DRAM MEMORY CELLS IN REMINDER

Previous attempts to introduce FB-DRAMs in industry have not been materialized for several reasons: i) insufficient performance of the preconized solution; ii) successful move to the next generation of standard 1T+1C DRAMs; and iii) immature FDSOI technology with restricted access.

However, the situation has dramatically changed and, in our opinion, at the present moment, there are two reasons that make possible the industrial development of embedded memory products based on FB-DRAM solutions:

-At the beginning of FB-DRAM, the need of ultralow power, small footprint and low cost memory was not as dramatic as nowadays is, in the rise of the IoT era. This means that existing embedded SRAM and even eDRAM were yet competitive solutions, difficult to replace, which is no longer the case.

-The first prototypes of FB-DRAM were based on standard transistors and had modest performance compared to present solutions (A2RAM, Z2FET and MSDRAM) [6-10].

### *A. A2RAM*

**Concept -** The A2RAM memory cell was proposed in 2011[7] as a new device with potential application as capacitorless DRAM. The simulation results predicted large current ratio between states '1' and '0', low-voltage operation, single-gate control and a superior scalability. Apart from these generic assets, the A2RAM features direct compatibility with SOI and bulk substrates without changes in design, whereas most of FB-DRAMs cells are tied to SOI substrates or require major modifications to bulk technology. The first preliminary demonstration came out in 2012 [8] on SOI substrate (Fig. 1a). The principle of operation of the A2RAM is summarized in Fig. 1b&c. The device is an SOI N-channel transistor (although it may also be a bulk transistor) with a buried N type layer (N-Bridge) which short-circuits the source and drain regions. A negative gate bias is applied to accumulate holes at the top interface; the presence of this accumulated charge defines the '1' state bit. Under these circumstances, the gate electric field is screened by the accumulated charge and the carrier concentration in the N-Bridge is hardly affected by the gate bias. The electron concentration in the undepleted N-Bridge corresponds to the doping level leading to a current flow between source and drain (Fig. 1b). If holes are temporarily removed from the top interface, while negative gate bias is maintained, the gate-induced field is no longer screened, affecting the electron concentration of the N-Bridge. If the device dimensions and doping concentrations are well calibrated, the N-Bridge will become fully depleted, therefore preventing any current flow between source and drain ('0' state, Fig. 1c).

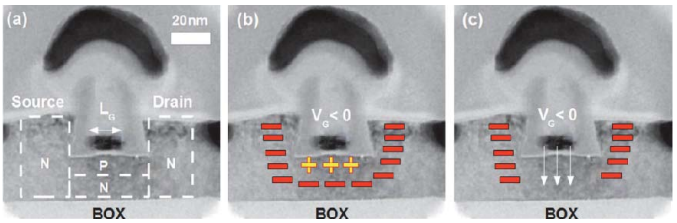



**Figure 1.** (a) TEM cross section of A2RAM cell fabricated in 22 nm SOI process with superimposed doping regions in dashed lines. (b) The accumulated holes in the top P-body screen the electric field: an electron current can flow between source and drain. (c) If the P-type body is in deep depletion, the gate electric field is no longer screened, fully depleting the N-Bridge from electrons and suppressing the drain current [7].

Three main advantages stand out immediately from this concept:

1. there is no need for biasing the bottom gate (substrate bias, $V_B = 0$ V) to create an electron channel
2. the reading of the cell state requires very low drain voltage.
3. the same concept can be extrapolated to FinFET or Nanowire technology.

**Expected performance:**

- Less than 10 ns writing time (only demonstrated by simulation).
- Retention times in the 100 milliseconds range at 85ºC (so far, only achieved with large cells or in small cells at 25ºC).
- Ultralow operation voltage (demonstrated by simulations).
- Large range between '1' and '0' states (already demonstrated experimentally)

*B. MSDRAM*

**Concept –** The MSDRAM (Meta-Stable DRAM) memory cell uses the double-gate action in regular FD SOI MOSFETs, namely the dynamic coupling between front and back interfaces which gives rise to a hysteresis in $I_D(V_G)$ curves (MSD effect, Fig. 2a). The two gates have distinct missions: frontgate voltage $V_{G1}$ is swept between accumulation and depletion, and the difference in front-surface potential is reflected, by coupling effect, in the backchannel current which is monitored. The MSD hysteresis[9] defines the programming and reading voltages[9]. The '0' state corresponds to the case where both interfaces are in depletion and the drain current is off. '1' state, defined when an inversion channel is formed at the back interface, is programmed by B2BT generation. Cell reading is performed by applying a low $V_D$ with $V_{G1}$ in the memory window (Fig. 2a), where the '0' and '1' currents can differ by more than 4 orders of magnitude. The difference between states '1' and '0' is that an accumulation region is present or not at the front interface. The accumulation layer guarantees that the back channel is inverted and since equilibrium is established, bit '1' does not require refresh. In '0' state, (Fig. 2b), the system is in non-equilibrium deep depletion and requires refresh. However, the generation of majority carriers is a slow process, meaning a 'long' retention time.

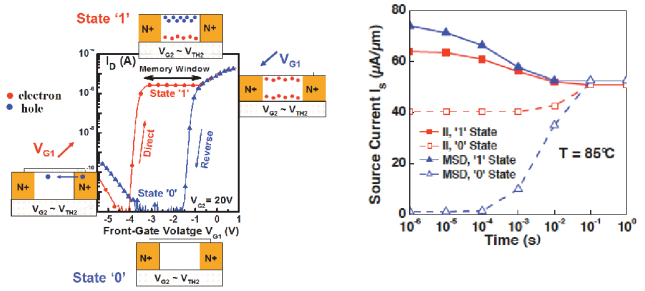



**Figure 2:** (a) Measured drain current $I_D$ versus decreasing (Reverse) and increasing (Direct) front-gate bias $V_{G1}$. (b) Experimental data retention at 85°C in 150 nm long MSDRAM cell [9].

Experimental proof-of-concept was achieved on non-optimized FD MOSFETs with channel length down to 30nm. The MSDRAM demonstrates longer retention time, negligible current in '0' state and a '1' state current level higher than those obtained with ZRAM programming methods like impact ionization (Fig.2b). The main advantages of the MSDRAM memory cell are: Wide memory window, high sense margin, negligible '0'-state current implying very low power consumption, non-destructive reading, adaptability to double-gate FinFETs and 3D nanowires.

**Expected performances**:

- 1-3ns programming time,
- up to 10s range retention time at room temperature,
- low power consumption
- large sensing margin between '0' and '1' state currents.

*C. Z2FET*

**Concept –** The Z2FET (Zero-ionization, Zero-swing FET) is a forward-biased PIN diode with the undoped channel partially covered by the front gate (Fig.3a) [10]. The front gate ($V_G < 0$) and the back gate ($V_{BG} > 0$) emulate a PNPN structure where two energy barriers block the injection of electrons and holes from terminals into the body. As $|V_D|$ increases, the device is instantly turned on due to the positive feedback between the carriers flow and the lowering of injection barriers. In reverse mode, the ON state is kept until the $|V_D|$ decreases to around 0.8V, where the device is sharply turned off. Thanks to its $V_G$-controlled hysteresis (Fig.3b), the Z2FET can be directly used as 1T-DRAM by holding the logic states at low $|V_D|$ and reading them out at higher $|V_D|$.

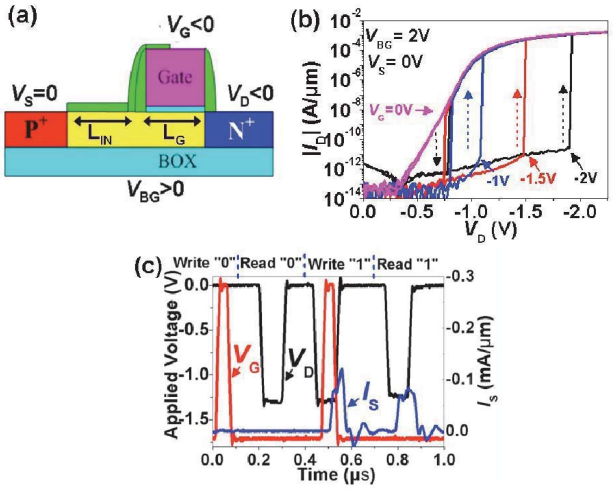



**Figure 3.** (a) Schematic view of Z2FET built on FD-SOI substrate. (b) $I_D$-$V_D$ characteristics under different $V_G$ show $V_G$-controlled hysteresis. (c) DRAM operations of the Z2FET with $L_G$=400 nm, $L_{IN}$ =500 nm, Tsi =20 nm, Tox = 3 nm $HfO_2$ and $T_{BOX}$ = 140 nm[10]

The logic states '1' or '0' are represented by the charges stored or not in the channel under the front gate. To read '1', the device is turned on by the transient current generated when the gate capacitor is discharged: the drain current $I_1$ is large (Fig.3c). In '0' state, since there is no charge stored and no transient discharging current, the transistor remains blocked ($I_0 \approx 0$). Measurements were performed on un-optimized FD SOI devices with the gate length ($L_G$) ranging from 400nm to 100nm. The retention time was 5s at room temperature. The read/write time was 100ns (as limited by equipment). Preliminary TCAD simulations showed that an accessing speed below 1ns can be reached [10]. The main advantages of the Z2FET memory cell are:

- Low operation voltage: Operation voltage as low as 1.1V has been demonstrated experimentally on long devices and can be reduced below 1V by scaling. Z2FET does not use impaction ionization or band-to-band tunnelling for programming, and thus needs lower voltage.
- Ultra-fast accessing speed: In all DRAMs, large amount of charge ΔQ is stored for direct read-out. Much less charge is needed in Z2FET, where the

feedback is triggered by the transient current ΔQ/Δt and not by ΔQ.

- Non-destructive reading.
- Long retention: While state '1' is stable in time, state'0' needs refresh. However, frequent memory reading regenerates state '0' by eliminating the parasitic population of holes under the gate.
- High current margin between '1' and '0': The readout of logic '1' turns on the Z2FET and the current is high (>100μA/μm), whereas in logic '0' the leakage OFF current is below 0.1pA/μm.
- Regarding the availability, Z2FET devices are currently being fabricated with 28FD technology at STMicroelectronics for other applications (ESD protection) and can be used for memory tests.

**Expected performance:**

- Read/write time less than 1ns and retention time above 10s.
- The Z2FET is expected to scale down to sub-40nm, as demonstrated by preliminary simulations. A possible extension is to use FinFET, PD-SOI and bulk substrates.

## IV. The EU project REMINDER

The semiconductor industry needs, more than ever, new memory paradigms to tackle with the storage, processing, energy consumption and cost demands of the integrated circuits oriented to the IoT. The project REMINDER is ultimately focused to develop an embedded DRAM solution for IoT cut-edge devices, i.e. the pursued memory block will be optimized for ultra-low-power consumption, variability immunity, and low cost, in addition to the footprint miniaturization. The pragmatic approach for quick lab-to-market demonstration is to use the established FDSOI technology, without introducing alternative materials or new steps in the fabrication process (different from the ones already necessary to fabricate the rest of blocks in the system). In parallel, we will also define longer-term FB-DRAM solutions using emerging technologies that are not yet stabilized (III-V), NWs, and SiGe). To achieve the objectives of REMINDER the project structure is founded on three main pillars:

1. Investigation (concept, design, characterization, simulation, modelling), selection and optimization of a Floating-Body memory bit cell in terms of low power and low voltage, high reliability, robustness (variability), speed, reduced footprint and cost. Fabrication of selected bit cells with FDSOI and III-V technologies.
2. Design and fabrication in FD28 and FD14 technology nodes of a memory matrix based on the optimized bit-cells developed in the first pillar. Matrix memory subcircuits, blocks and architectures will be carefully analysed from the power-consumption point of view. In addition variability tolerant design techniques underpinned by variability analysis and statistical simulation technology will be considered.
3. Demonstration of a system on chip (SoC) application using the developed memory solution and benchmarking with alternative embedded memory blocks.

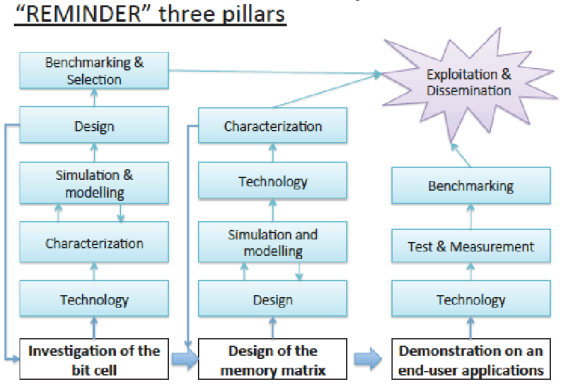



Figure 4. REMINDER project approach.

The eventual replacement of Si by strained Si/SiGe and III-V materials in future CMOS circuits would also require the redesign of different applications, including memory cells, and therefore we also propose the evaluation of the optimized bit cells developed in pillar i) in FD28 and FD14 technology nodes using these alternative materials. REMINDER consortium is composed by University of Granada, STMicroelectronis, CEA-LETI and Grenoble INP, University of Glasgow, Gold-Standard Simulations, SureCore Inc., IBM-Research, and Korea Institute of Science and Technology (KIST).

## References

[1] D. U. Lee et al, "A 1.2V 8Gb 8-Channel 128GB/s High-Bandwidth Memory (HBM) Stacked DRAM with Effective Microbump I/O Test Methods Using 29nm Process and TSV" 2014 IEEE International Solid-State Circuits Conference.

[2] J. T-Y. Oh et al, "A 3.2Gb/s/pin 8Gb 1.0V LPDDR4 SDRAM with Integrated ECC" 2014 IEEE International Solid-State Circuits Conference.

[3] S. Okhonin et al. "Ultra-scaled Z-RAM cell", In proceedings 2008 International SOI conference

[4] "Trends in Embedded DRAM, July 2014" Memory Strategies International, 16900 Stockton Drive, Leander, Texas, 78641, U.S.A.

[5] I. Ban, (2010), "Integration of Back-Gate doping for 15-nm node floating body cell (FBC) memory", Symposium on VLSI Technology, 159-160 (2010)

[6] N.Rodriguez, et al. "Experimental developments of A2RAM memory cells on SOI and bulk substrates", Solid-State Electronics, 2015

[7] N. Rodriguez, et al. (2011), "Novel Capacitorless 1T-DRAM Cell for 22-nm Node Compatible With Bulk and SOI Substrates", IEEE Trans.Elec.Dev., Vol. 58 , 2371

[8] N. Rodriguez, et al., "Experimental Demonstration of Capacitorless A2RAM Cells on Silicon-on-Insulator" IEEE Electron Device Letters, Vol. 33, No. 12, 2012.

[9] M.Bawedin, et al.(2008), IEEE Electron Device Letters, 29, pp 795-798.

[10] J. Wan, et al. (2012), " A Compact Capacitor-Less High-Speed DRAM Using Field Effect-Controlled Charge Regeneration," IEEE Electron Device Letters vol 33(2), pp 179-180

# Inverse-magnetostriction-induced switching current reduction of STT-MTJs and its application for low-voltage MRAMs

Y. Takamura, Y. Shuto, S. Yamamoto, H. Funakubo, M.K. Kurosawa, S. Nakagawa, and S. Sugahara
Tokyo Institute of Technology
Tokyo, Japan
takamura@spin.pe.titech.ac.jp

***Abstract*— A new spin-transfer torque (STT) magnetic tunnel junction (MTJ) using an inverse magnetostriction (IMS) material for the free layer is proposed for low-voltage MRAMs. The MTJ is surrounded by a piezoelectric gate structure so that a pressure for introducing the IMS effect can efficiently be applied to the free layer without any high-yield-strength support structure. During STT-induced magnetization switching, the energy barrier height for the switching can be lowered by the IMS effect, and thus a critical current density ($J_C$) for the magnetization switching can dramatically be reduced. Energy performance of a low-voltage MRAM cell using the proposed MTJ and a FinFET is also demonstrated.**

***Keywords—Magnetic tunnel junctions (MTJ), Magnetostriction materials, inverse-magnetostrictive effect, spin transfer torque, current-induced magnetization switching (CIMS)***

## I. INTRODUCTION

Low-voltage (or near-threshold voltage) operations of CMOS logic systems have attracted considerable attention owing to the ability of dramatic reduction of dynamic and static power dissipation [1]. In particular, low-voltage (~0.3-0.4V) operations can minimize the energy dissipation (or maximize the energy efficiency) of logic systems [1], and thus this operation mode is promising for always-on applications such as various wearable devices [2]. Nonvolatile data retention adaptable to low-voltage operations is highly requested for these applications. Spin-transfer torque (STT) magnetic tunnel junctions (MTJs) are expected to be a promising nonvolatile memory element for low-voltage operations owing to the current-driven operation behavior of the MTJs, i.e., as far as the critical current density ($J_C$) for their current-induced magnetization switching (CIMS) can be obtained at a desired low-voltage, there is no limitation for the (write-) operation voltage. Various efforts including perpendicular magnetic anisotropy electrodes have been paid to reduce $J_C$ [3]. However, the reduction of $J_C$ still is not enough to operate at a low-voltage for minimizing energy dissipation.

$J_C$ can be reduced by lowering the energy barrier ($E_B$) of MTJs. However, this degrades the thermal stability. Energy barrier reduction techniques applied only during CIMS would be promising for managing low $J_C$ and high thermal stability. Saito *et al*. [4] proposed a switching field reduction technique based on the inverse magnetostriction (IMS) effect for field-induced magnetization switching of MTJs using a super magnetostriction material for the free layer. This technique would also be applied to $J_C$ reduction for CIMS of STT MTJs. Note that pressures (<1 GPa) required for energy barrier deformation of the IMS layer of such MTJs would be obtained using a piezoelectric (PE) material with a low voltage bias (discussed later).

In this paper, we propose a new STT MTJ using an IMS material for the free layer (hereafter, referred to as an IMS-MTJ) and computationally investigate IMS-induced switching

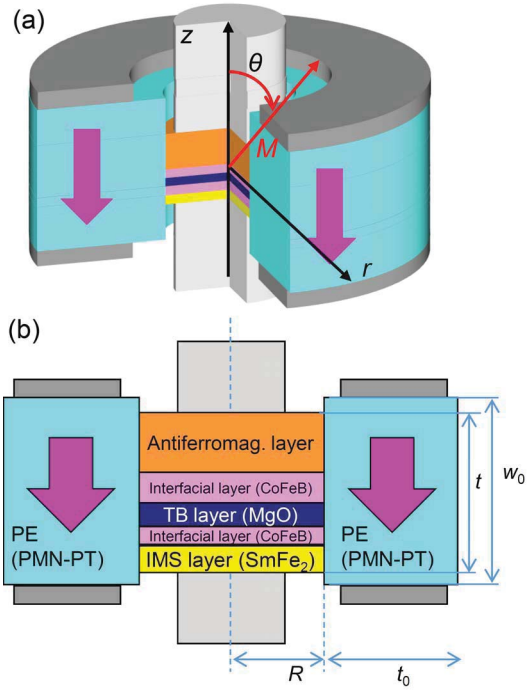



Fig. 1. (a) Schematic device structure and (b) cross section of a proposed IMS-MTJ. The dielectric polarization of the piezoelectric (PE) gate is parallel to the $z$ axis. One of possible structures consists of a CoFeB/MgO/CoFeB/$SmFe_2$ MTJ and a surrounding PMN-PT gate.

TABLE I. SIMULATION PARAMETERS FOR IMS-MTJ

| | |
|---|---|
| Tunneling magnetoresistance: TMR | 100 % |
| Resistance-area product: RA | 2 Ω·μm$^2$ |
| Voltage at half-maximum TMR: $V_{half}$ | 0.5 V |
| $J_{CT}$ without the IMS effect | 2.5×10$^6$ A/cm$^2$ |
| $J_{CT}$ with the IMS effect | 0.1×10$^6$ A/cm$^2$ |
| Resistance: $R_P(0)$ (Parallel mag.) | 6.36 kΩ |
| $R_{AP}(0)$ (Antiparallel mag.) | 12.7 kΩ |

TABLE II. MATERIAL CONSTANTS AND DEVICE PARAMETERS FOR IMS-MTJ

| MTJ part | | | | | | | | | | PE gate part | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $K_u$ (MJ/m$^3$) | $M$ (T) | $\lambda$ (ppm) | $\alpha$ | $R$ (nm) | $l_m$ (nm) | $\Delta$ | $\eta$ | $\tau_0$ (ns) | $Y_{MTJ}$ (GPa) | $Y_{PE}$ (GPa) | $\nu$ | $\varepsilon^S_{33}$ | $d_{31}$ (nm/V) |
| 0.56 | 0.64 | -1258 | 0.005 | 10 | 2 | 60 | 1 | 1 | 40 | 0 | 0.3 | 741 | -0.852 |

$K_u$: Uniaxial magnetic anisotropic energy density, $M$: Saturation magnetization, $\lambda$: Magnetostrictive constant, $\alpha$: Damping constant, $R$: Radius of the MTJ pillar, $l_m$: Thickness of the IMS layer, $\eta$: Spin transfer efficiency, $\tau_0$: Attempt time, $Y_{MTJ}$, $Y_{PE}$: Young modules of the MTJ and PE parts, $\nu$: Poisson's ratio, $\varepsilon^S_{33}$: Relative permittivity, $d_{31}$: Piezoelectric strain constant.

current reduction of the IMS-MTJ. Energy performance of a low-voltage MRAM cell using the proposed IMS-MTJ and a high performance FinFET is also demonstrated.

## II. PROPOSED IMS-MTJ

Fig. 1 shows a schematic device structure of the proposed STT MTJ using an IMS material for the free layer. The device is comprised of ferromagnetic electrodes (pinned and free layers), a tunnel barrier (TB), and a PE gate surrounding the MTJ part. The free layer consists of the IMS layer and high spin-polarization interfacial layer facing the TB. These two layers are magnetically coupled, i.e., the magnetization direction of the interfacial layer is governed by that of the IMS layer. The PE gate acts as a stressor to the free layer, which applies a compress pressure ($P$) in the free layer plane. The PE gate electrodes that apply an electric field to the PE material are also placed. In this study, $SmFe_2$ [5] is adopted as the IMS material, and a device structure consisting of a CoFeB / MgO / CoFeB / $SmFe_2$ MTJ part and a PMN-PT [6] gate surrounding it is employed.

## III. MODELLING AND CALCULATION PROCEDURE

Calculations for IMS-induced MTJ behaviour were carried out using the LLG (Landau-Lifshits-Gilbert) equation with Slonczewski's STT term [10,11]. We developed a model representing the STT term as an effective energy. The IMS effect was also treated as a magnetoelastic energy. These energies were incorporated in the LLG equation. Critical current densities for magnetization switching without/with thermally excitation [12,13] were analysed. The material constants and device parameters used in this study are shown in Tables I and II, which were determined by reference to reported data of IMS materials, perpendicular CoFeB/MgO/CoFeB MTJs, and piezo electronic devices [5-9]. Note that $\Delta$ is defined by the energy barrier height for the switching at $P$ = 0 MPa, i.e., $E_B(P{=}0) = \Delta$. Operations of proposed MRAM cells (shown later) were analysed by HSPICE with a 20-nm-technology FinFET PTM [14] and our developed MTJ macromodel [15]. This macromodel can closely fit experimentally observed electrical characteristics of ordinary MTJs within an error of 1.5% [15].

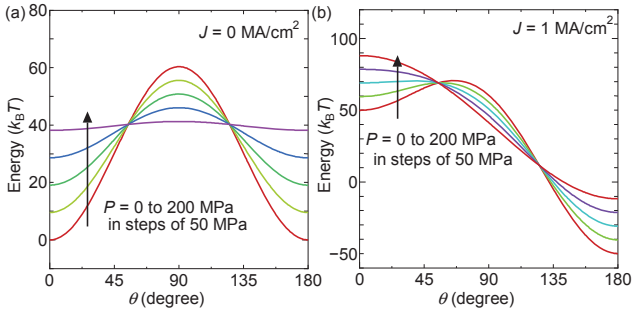



Fig. 2. Energy curves for the IMS free layer of the IMS-MTJ, in which (a) $P$ is varied with $J$ = 0, and (b) $P$ is varied with $J$ = 1 MA/cm$^2$. $J$ and $P$ represent current density passing through the device and pressure applied to the IMS layer, respectively.

## IV. IMS-MTJ CHARACTERISTICS

Fig. 2 shows the calculated effective energy barrier for the IMS free layer as a function of tilt angle $\theta$ of the magnetization (also see Fig. 1 (a)). The energy barrier can be reduced by $P$ applying to the free layer owing to the IMS effect (Fig. 2(a)). The STT magnetization switching (CIMS) occurs when the energy barrier disappears, and thus the IMS-induced barrier lowering is effective at reducing the critical current of the CIMS, as shown in Fig. 2(b). Here, the critical current density $J_{C0}$ is defined by a switching current just when the energy barrier becomes zero. Note that when $P$ = 0, this quantity is completely identical with Slonczewski's $J_{C0}$ [11]. The effective barrier decreases with $J$ depending on $P$, and $J_{C0}$ can be reduced with increasing $P$, as shown in Fig. 3(a). For ordinary STTT-MTJs, $J_{C0}$ can be reduced by lowering $\Delta$, which degrades thermal stability. However, $J_{C0}$ also diminished by $P$ without reducing $\Delta$ for the proposed IMS-MTJ. Fig. 3(b) shows CIMS efficiency of IMS-MTJs as a function of $P$. The CIMS efficiency is given by a ratio of the effective energy

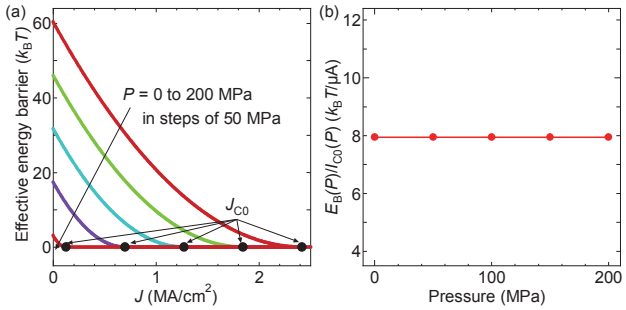



Fig. 3. (a) Energy barrier as a function of $J$, in which $P$ is varied from 0 to 200 MPa in steps of 50 MPa (b) Spin-transfer torque magnetization switching efficiency of the IMS-MTJ as a function of $P$.

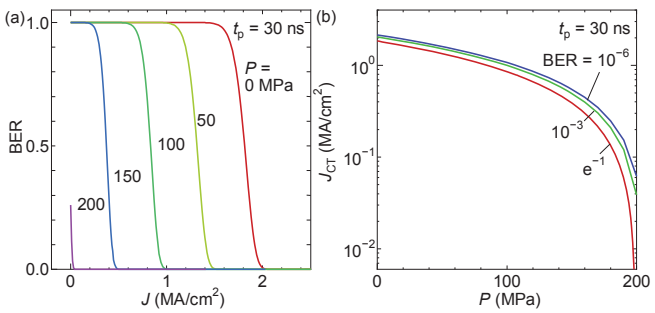



Fig. 4. (a) BER as a function of $J$, in which $P$ is varied from 0 to 200 MPa in steps of 50 MPa (b) $J_{CT}$ as a function of $P$ for various BERs. The definition of $J_{CT}$ is described in the text.

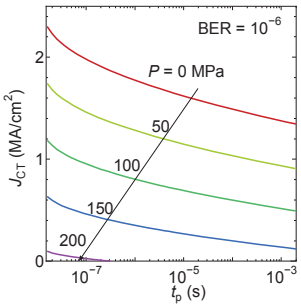



Fig. 5. $J_{CT}$ as a function of tp for BER = $10^{-6}$, in which $P$ is varied from 0 to 200 MPa in steps of 50 MPa.

barrier $E_B(P)$ for the switching to the critical current $I_{C0}(P)$. [16] The CIMS efficiency remains constant at a reasonable value regardless of $P$. To clarify the impact of the switching error rate of the IMS-MTJ on the critical current, the thermal excitation effect is included in our calculations using a model proposed by Koch et al. [12]. Fig. 4(a) shows the bit error rate (BER) as a function of $J$ at room temperature, in which $P$ is varied and the pulse width $t_p$ for $J$ and $P$ are fixed at 30 ns. The BER rapidly increases with decreasing $J$ for each $P$ condition, when $J$ is lower than $J_{C0}$. Therefore, the critical current density $J_{CT}$ determined by a given BER is important in practice and used for the following discussion. Fig. 4(b) shows $J_{CT}$ as a function of $P$, in which BER is varied. $J_{CT}$ decreases with increasing $P$ depending on BER. Fig. 5 shows $J_{CT}$ as a function of $t_p$ for BER = $10^{-6}$. The non-linear behaviour of the $J_{CT}$-$t_P$ curve appears for all the pressure conditions and $J_{CT}$ increases with decreasing $t_P$. The magnetization switching with $J_{CT}$ = 0.1 MA/cm$^2$ and BER = $10^{-6}$ can be achieved for a moderate $t_P$ (several tens of nanoseconds).

## V. Low-voltage MRAM application

Figs. 6(a) and (b) show two types of MRAM cells using an IMS-MTJ. The cell shown in Fig. 6(a) is the same configuration as conventional MRAM cells, i.e. the cell configuration with the drain-side MTJ connection (DSM cell). The cell shown in Fig. 6(b) has a configuration with the source-side MTJ connection (SSM cell), in which the connected MTJ feeds back its voltage drop to the gate of the MOSFET. Since the degree of this negative feedback depends on the resistance states of the MTJ, the cell currents of the SSM cell can be effectively controlled by the magnetization configuration of the MTJ (shown later). In this study, a FinFET is used for both the cells. Table III shows an operation architecture of these cells. Note that the IMS effect is not induced during the read operation, and it is employed only during the write operation. Fig. 6(c) shows $P$ as a function of $V_{PE}$ (that is a bias voltage of the PE gate; see Fig. 1(b)). $P$ required for the IMS-induced switching current reduction described above (several hundreds of MPa) can easily be yielded by $V_{PE}$ = 0.2 V or less. Figs. 7(a) and (b) show cell currents as a function of $V_{DD}$ for the DSM

TABLE III. Read/write operation architecture.

| | Read | Write (AP→P) | Write (P→AP) |
|---|---|---|---|
| BL | H | L | H |
| SL | L | H | L |
| WL | H | H | H |
| PE | L | H | H |

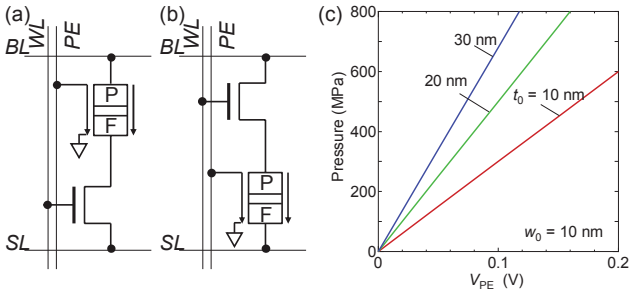



Fig. 6. Low-voltage MRAM cells using an IMS-MTJ with (a) drain-side MTJ connection (DSM) and (b) source-side MTJ connection (SSM) configurations. (c) $P$ as a function of $V_{PE}$. $V_{PE}$ represents a bias voltage of the PE gate (see Fig.1 (b)).

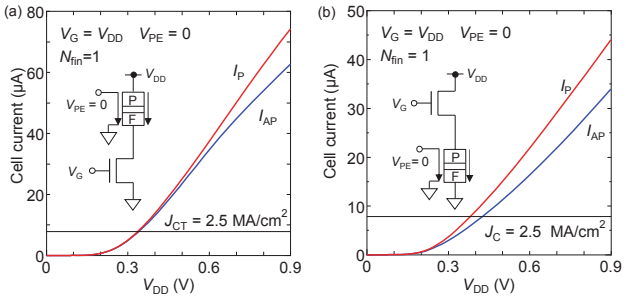



Fig. 7. Cell currents as a function of $V_{DD}$ for (a) the DSM cell and (b) the SSM cell during the read operation mode.

and SSM cells, respectively, during the read operation, in which $V_{PE}$ and $V_G$ are set to zero and $V_{DD}$, respectively. Although the cell currents of the SSM cell is lower than those of the DSM cell, its magnetocurrent ratio (that is a rate of change of the cell currents in the parallel and antiparallel configurations: $\gamma_{MC} = (I_P - I_{AP})/I_{AP}$) is sufficiently high to distinguish the parallel and antiparallel states even at $V_{DD}$ = 0.3 V, as shown in Fig. 8. In addition, the magnetocurrent ratio can be enhanced by the number of the fin channel of the FinFET (Fig. 8). On the other hand, the magnetocurrent ratio of the DSM cell is severely degraded for lower $V_{DD}$ operations. Note that when $V_{DD}$ is less than 0.4 V, the magnetization switching does not occur during the read operation (since the cell currents do not exceed $J_{CT}$ for $V_{PE}$ = 0 V; see Table II). Fig. 9 shows cell currents during the write operation for the SSM cell (in which $V_{PE}$ is applied). The cell current can exceed $J_{CT}$ for the IMS-induced switching when $V_{DD} \geq 0.2$ V. Fig. 10 shows the write energy of the SSM cell. By reducing $V_{DD}$ from 0.9 V to 0.2V, the write energy can be considerably reduced to 1/400.

## VI. Conclusion

We proposed a new STT MTJ using a super magnetostriction material for the free layer and the piezoelectric gate for applying a pressure to the free layer. The effective switching current reduction of the proposed device is theoretically revealed. A low-voltage MRAM cell using the proposed MTJ can largely reduce the write energy without degradation of the thermal stability.

## Acknowledgment

This work was partly supported by JSPS KAKENHI Grant,

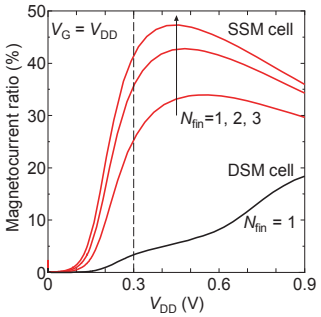



Fig. 8. Magnetocurrent ratio as a function of $V_{DD}$ for the DSM and SSM cells during the read operation mode.

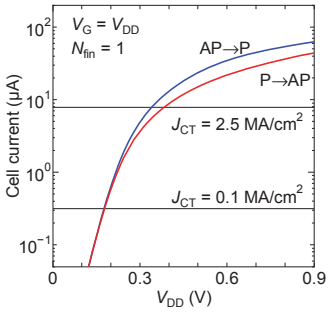



Fig. 9. Cell currents as a function of $V_{DD}$ for the SSM cell during the write operation mode.

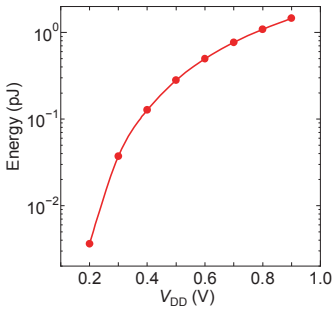



Fig. 10. Write energy as a function of $V_{DD}$ for the SSM cell.

and by Japan Science and Technology Agency.

## REFERENCES

[1] S. Jain et al., "A 280mV-to-1.2V wide-operating-range IA-32 processor in 32nm CMOS," 2012 IEEE ISSCC, paper 3.6.

[2] K. Lee, J.J. Kan, and S.H. Kang, "Unified embedded non-volatile memory for emerging mobile markets," 2014 IEEE ISLPED pp. 131-136.

[3] S. Mangin, et al., "Current-induced magnetization reversal in nanopillars with perpendicular anisotropy," Nat. Mater., vol. 5, pp. 210-215, March 2006.

[4] N. Saito, M. Yamada, and S. Nakagawa, "Improvement of stress-induced mangetization reversal process of DyFeCo thin films," J. Appl. Phys., vol. 103, pp. 07A706/1-3, January 2008.

[5] H. Samata, N. Fujiwara, Y. Nagata, T. Uchida, and M.D. Lan, "Crystal growth and magnetic properties of $SmF_2$," Jpn. J. Appl. Phys., vol. 37, pp. 5544-5548, October 1998.

[6] D. Newns, B. Elmegreen, X.H. Liu, and G. Martyna, "A low-voltage high-speed electronic switch based on piezoelectric transduction," J. Appl. Phys., vol. 111, pp. 084509/1-18, April 2012.

[7] S. Ikeda, et al., "A perpendicular-anisotropy CoFeB–MgO magnetic tunnel junction," Nat. Mater. vol. 9, pp. 721-724, July 2010.

[8] J. H. Park, et al., ", Enhancement of data retention and write current scaling for sub-20nm STT-MRAM by utilizing dual interfaces for perpendicular magnetic anisotropy," 2012 VLSI, paper 7.1.

[9] M. Gajek, et al., "Spin torque switching of 20□nm magnetic tunnel junctions with perpendicular anisotropy," Appl. Phys. Lett., vol. 100, pp. 132408/1-3, March 2012.

[10] J.Z. Sun, "Spin-current interaction with a monodomain magnetic body: A model study," Phys. Rev. B, vol. 62, pp. 570-578, July 2000.

[11] J.C. Slonczewski, "Currents and torques in metallic magnetic multilayers," J. Magn. Magn. Mater., vol. 247, pp. 324-338, March 2002.

[12] R.H. Koch, J.A. Katine, and J.Z. Sun, "Time-resolved reversal of spin-transfer switching in a nanomagnet," Phys. Rev. Lett., vol. 92, pp. 088302/1-4, February 2004.

[13] W. H. Butler et al., "Switching distributions for perpendicular spin-torque devices within the macrospin approximation," IEEE Trans. Magn. vol.48, pp. 4684-4700, December 2012.

[14] Predictive Technology Model (PTM), http://ptm.asu.edu/.

[15] S. Yamamoto, and S. Sugahara, "Nonvolatile Static Random Access Memory Using Magnetic Tunnel Junctions with Current-Induced Magnetization Switching Architecture," Jpn. J. Appl. Phys., vol. 48, pp. 043001/1-7, November 2009.

[16] G. Hu, et al., "STT-MRAM with double magnetic tunnel junctions," 2015 IEDM, paper 26.3.

# A Consistent Picture of Cycling Dispersion of Resistive States in $HfO_X$ Resistive Random Access Memory

Francesco Maria Puglisi, Paolo Pavan
Dipartimento di Ingegneria "Enzo Ferrari"
Università di Modena e Reggio Emilia
Via P. Vivarelli 10/1, 41125 Modena (MO), Italy
francescomaria.puglisi@unimore.it

***Abstract*—In this paper we present the results of a systematic study of resistive states cycling dispersion in $HfO_x$ Resistive Random Access Memory (RRAM). A wide set of experimental data is collected on several RRAM devices in different operating conditions. A compact model is exploited lo link the device electrical response to its physical characteristics, delivering a clear physical picture of cycling dispersion and of its sensitivity to operating conditions. The implications of operating voltage, current compliance, and temperature on the device reliability are clarified. Particularly, the dispersion of both $R_{HRS}$ and $R_{LRS}$ is much worsened at low current compliance, which reduces the worst-case read window establishing a trade-off between device reliability and power consumption.**

***Keywords—RRAM; Resistive Memory; Switching; Dispersion; Variability;***

## I. Introduction

The research of novel non-volatile memory technologies satisfying the stringent consumer market requirements has tremendously accelerated in the last years. Among the many proposed solutions, the Resistive Random Access Memory (RRAM) technology represents an attractive option due to its potential for low-complexity, high-density, high-speed, low-cost, low-energy non-volatile operation [1-9], which can be exploited in both embedded and stand-alone applications. Furthermore, RRAM devices can easily be integrated in the back-end of line (BEOL) thus enabling innovative logic-in-memory approaches and easier transition toward full-3D architectures [3, 9]. Within the large family of the metal-oxide-based resistance switching memories, a common characteristic is that their operating mechanisms involve the rearrangement of the dielectric material at the atomic level [10]. This is necessary to change the electrical resistance of the device between two distinct levels, i.e. the High- (HRS) and Low-Resistance-State (LRS), associated with different atomic arrangements of the dielectric material [4-11]. Here we consider transition metal-oxide (TMO) RRAM devices, specifically the bipolar TiN/Ti/$HfO_2$/TiN RRAM [6], which is very attractive since it can be easily integrated in the BEOL of the CMOS process. In addition, it offers excellent scaling perspectives – the material used for the switching layer ($HfO_2$) and for the electrodes (TiN) are already used in CMOS technology – it demonstrates excellent memory characteristics,

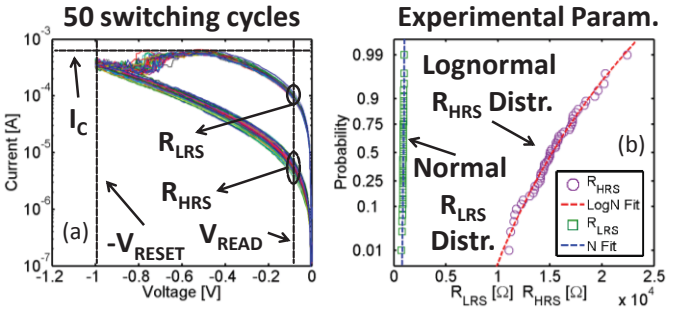



Fig. 1 – (a) Reset I-V curves of an RRAM device cycled 50 times. The current compliance, $I_C$, the read voltage, $V_{READ}$, and the reset voltage, $V_{RESET}$, are reported. The $R_{LRS}$ and $R_{HRS}$ dispersion sensed at $V_{READ}$ is shown (black circles). (b) Corresponding $R_{LRS}$ (normal) and $R_{HRS}$ (log-normal) distributions and fittings.

data retention and endurance [9] with reduced implementation costs [1, 4, 6, 10]. Still, inherent stochastic features of this technology, i.e. mainly randomness in the physical mechanisms involved in switching operations [9-11] and, secondarily, Random Telegraph Noise (RTN) [12-16], are hampering its full industrial exploitation. A major concern is represented by cycling dispersion, i.e. the variability exhibited by the resistive states during device cycling [9-11], which hinders the device scaling and multi-bit implementation. So, understanding the physical processes responsible for variability is crucial for the application-oriented [1-4, 10, 17] optimization of RRAM devices. In this paper, we systematically analyze a wide set of experimental data to perform a thorough investigation of cycling dispersion. A RRAM compact model [18-19] is used to link the device electrical response to its physical characteristics, providing a clear picture of dispersion implications on the device reliability. Results are exploited to evidence a trade-off between power dissipation and device reliability.

## II. Devices and Experiments

TiN/5nm-Ti/3.4nm-$HfO_2$/TiN RRAM devices in 1T1R configuration are measured under different operating conditions (temperature - T, reset voltage - $V_{RESET}$, current compliance - $I_C$), Fig. 1a. Initially, devices are formed using different $I_C$. This creates a conductive filament (CF) composed of oxygen vacancies, Vo [20-21]. The CF cross-section, *S* (and

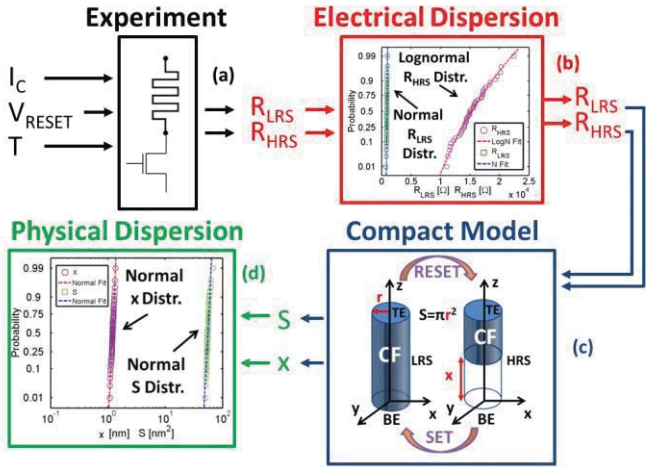
so $R_{LRS}$), is controlled by $I_C$ [22]. After forming, each device is cycled 50 times and I-V curves are measured, Fig. 1a. Each cycle includes a reset operation, driving the device from low- (LRS) to high-resistive state (HRS), and a set operation, driving the cell in LRS. Particularly, the reset operation drives the oxygen ions around the CF towards its bottom end, where they recombine with the Vo in the CF leading to the re-oxidation of its bottom tip [21]. This forms a dielectric barrier [18-21] with cross-section *S* and thickness *x* (see Fig. 2c), which can be modulated using different $V_{RESET}$ [11-24]. So $R_{HRS}$ depends on both *S* and *x* [11-24]. The set operation, performed with the same $I_C$ as in forming, causes the barrier breakdown, restoring the full CF [18-24].

## III. HRS AND LRS STATISTICS

Data are used to extract the device resistance in HRS and LRS, i.e. $R_{HRS}$ and $R_{LRS}$, at the read voltage $V_{READ}$=0.1V, Fig. 1a. The corresponding distributions reveal two different behaviors: while $R_{LRS}$ follows a normal distribution, $R_{HRS}$ is log-normally distributed, Fig. 1b, in agreement with previous studies [11] and other reports [20, 23-24]. The $R_{LRS}$ and $R_{HRS}$ dispersion is attributed to the randomness of the physical mechanisms involved in reset and set operations [21, 23]. The transition to the HRS during reset results from random recombination events, which cause variations of the barrier thickness at each cycle [18]. Similarly, the transition to the LRS during set is determined by random Hf-O bond breakage events [21] resulting in variations of *S* at each cycle [23].

## IV. RESULTS AND DISCUSSION

We exploit our compact model [18-19] to link the electrical dispersion of $R_{HRS}$ and $R_{LRS}$ to the physical variations of *x* and *S*, Fig. 2. Interestingly, the normal $R_{LRS}$ distribution corresponds to a normal *S* distribution, while the log-normal $R_{HRS}$ distribution arises from a normal *x* distribution [11], Fig. 2d. Dealing only with normal distributions can be helpful, as normal distributions are completely described by the mean μ and the standard deviation σ. This allows discussing physical variability by using four simple physical indicators, namely $\mu_x$, $\sigma_x$, $\mu_S$, and $\sigma_S$. We systematically study dispersion at different operating conditions reporting the "6σ distributions", i.e. μ±3σ, required by the industry to completely evaluate the technology potential and to determine circuit design constraints. We start the analysis discussing the influence of $V_{RESET}$ on both *x* and *S*. Fig. 3a shows the trends of $\mu_x$ and $\sigma_x$ vs. $V_{RESET}$. $\mu_x$ is increased by higher $V_{RESET}$, in agreement with the evidence [11-23] that a higher $V_{RESET}$ results in a higher $R_{HRS}$. $\sigma_x$ is instead constant, which suggests that *x* dispersion is related to the O ions availability during the reset operation [20], independently of the applied voltage. Fig. 3b shows the relative *x* immunity to variations, described by $\mu_x/\sigma_x$. Clearly, higher $V_{RESET}$ result in higher relative *x* immunity. Nevertheless higher $V_{RESET}$ does not translate in higher relative $R_{HRS}$ immunity, due to the non-linear relation between *x* and $R_{HRS}$ [11,18-24]. Fig. 4 shows the trends of $\mu_S$, $\sigma_S$, and $\mu_S/\sigma_S$ as a function of $V_{RESET}$. Conceivably, they show no dependence on $V_{RESET}$ confirming that the reset operation has




$$R_{LRS} = \rho_{Hf,CF}\frac{t_{ox}}{S} \quad \text{(e)}$$

$$R = R_{LRS}\left[\frac{t_{ox}-x}{t_{ox}} + \left(e^{\frac{x}{\kappa}}-1\right)e^{\frac{E_A}{k_B T}}\right]$$

Fig. 2 – (a) Experiments are run at given operating conditions ($I_C$, $V_{RESET}$, T), returning the $R_{LRS}$ and $R_{HRS}$ distributions over cycling (b). These are fed to the compact model (c) translating electrical quantities to physical ones (*x* and *S*), both normally distributed (d). In (c), a 3D schematic depiction of the device in LRS and HRS is reported. (e) Compact model equations: *R* is the device resistance, $t_{ox}$ (*x*) the oxide (barrier) thickness, κ a tunneling constant [3], $E_A$ the activation energy, $k_B$ the Boltzmann constant, $\rho_{Hf,CF}$ the CF resistivity, *S* its cross-section.

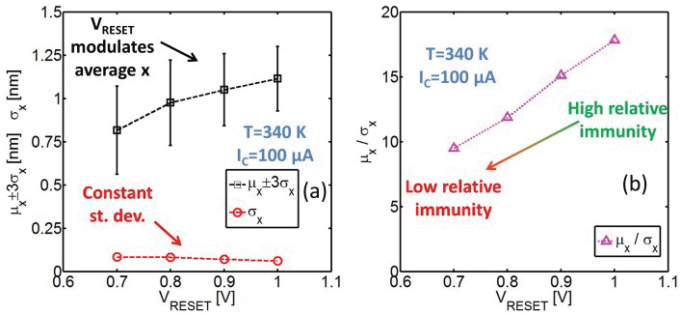



Fig. 3 – (a) Trends of $\mu_x$ (6σ distributions – black squares) and $\sigma_x$ (red circles) vs. $V_{RESET}$ for a device formed at $I_C$=100μA and cycled at T=340K. (b) Relative *x* immunity to variations ($\mu_x/\sigma_x$ – magenta triangles) vs. $V_{RESET}$ for the same device.

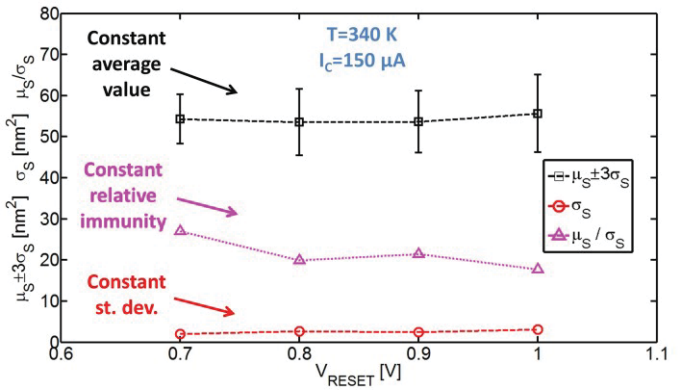



Fig. 4 – Trends of $\mu_S$ (6σ distributions – black squares), $\sigma_S$ (red circles), and $\mu_S/\sigma_S$ (magenta triangles) vs. $V_{RESET}$ for a device formed at $I_C$=150μA and cycled at T=340K.

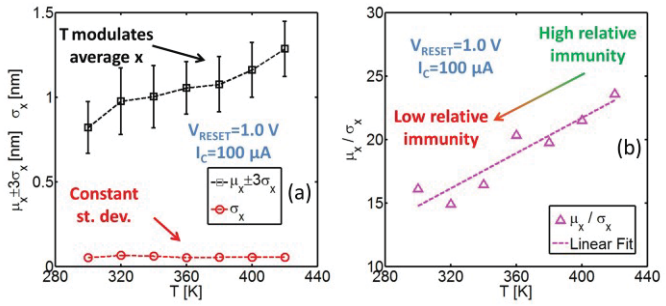



Fig. 5 – (a) Trends of $\mu_x$ (6σ distributions – black squares) and $\sigma_x$ (red circles) vs. T for a device formed at $I_C$=100µA and cycled with $V_{RESET}$=1.0V. (b) Relative *x* immunity to variations ($\mu_x/\sigma_x$ – magenta triangles) vs. T for the same device along with linear fitting.

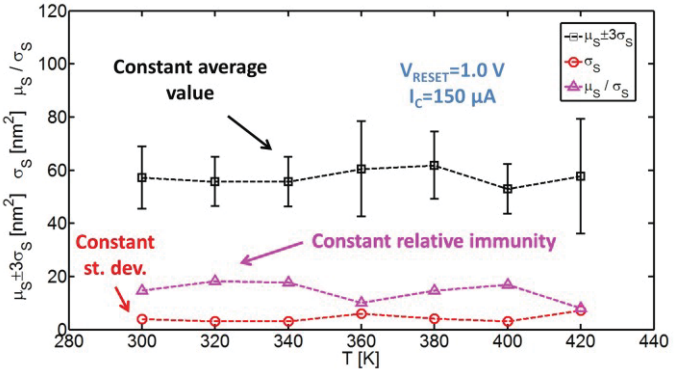



Fig. 6 – Trends of $\mu_S$ (6σ distributions – black squares), $\sigma_S$ (red circles), and $\mu_S/\sigma_S$ (magenta triangles) vs. T for a device formed at $I_C$=150µA and reset at $V_{RESET}$=1.0V.

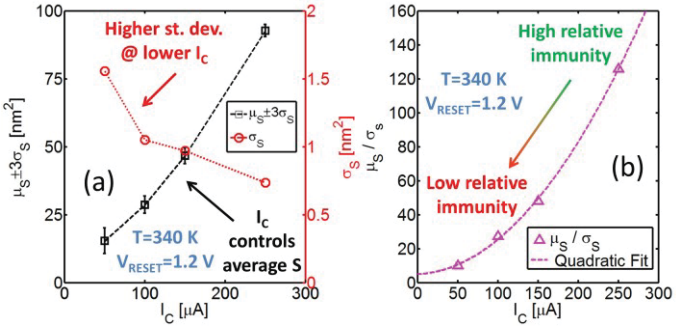



Fig. 7 – (a) Trends of $\mu_S$ (6σ distributions – black squares) and $\sigma_S$ (red circles) vs. $I_C$. All devices are cycled at $V_{RESET}$=1.2V and T=340K. (b) Relative *S* immunity to variations ($\mu_S/\sigma_S$ – magenta triangles) vs. $I_C$ with quadratic fitting.

no influence on the CF size, *S*. The analysis of dispersion at different switching temperatures, T, reveals a similar portrait, Fig. 5a. The compact model has also been proved to correctly include temperature effects [24]. A higher T during reset provides a thicker average dielectric barrier [24], while its variance is constant, Fig. 5a. A higher T implies indeed a more effective diffusion of the O ions during reset, leading to a thicker barrier. Still this has no effect on the O ions availability, which is consistent with $\sigma_x$ trend. Fig. 6 shows that a higher switching temperature has a negligible effect on $R_{LRS}$ and its dispersion, confirming that *S* is controlled solely by $I_C$.

The analysis of the impact of $I_C$ on *x* and *S* dispersion reveals interesting details. Results in Fig. 7a show that $I_C$

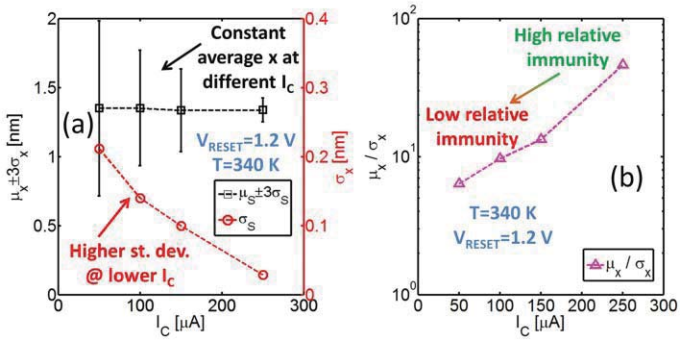



Fig. 8 – (a) Trends of $\mu_x$ (6σ distributions – black squares) and $\sigma_x$ (red circles) vs. $I_C$. All devices (same as in Fig. 7) are cycled at $V_{RESET}$=1.2V and T=340K. (b) Relative *x* immunity to variations ($\mu_x/\sigma_x$ – magenta triangles)vs. $I_C$.

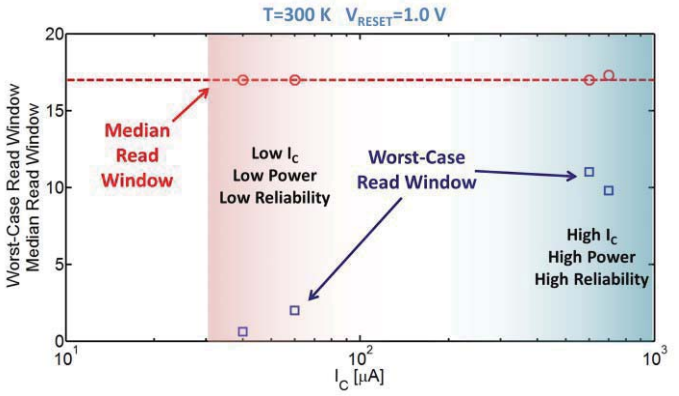



Fig. 9 – Trade-off between power consumption (proportional to $I_C$) and reliability. Small *x* and *S* dispersion at high $I_C$ (blue-shaded zone on the right) implies a small difference between the median ($R_{HRS,MED}/R_{LRS,MED}$ - red circles) and the worst-case read window ($R_{HRS,MIN}/R_{LRS,MAX}$ - blue squares). At low $I_C$ (red-shaded zone on the left), increased *x* and *S* dispersion causes a significant reduction of the worst-case read window.

controls $\mu_S$, as reported in the literature [18-22]. However, an $I_C$ reduction also produces an increased *S* (and $R_{LRS}$) dispersion, $\sigma_S$. This means that scaling $I_C$ critically lowers the relative *S* immunity to variations, $\mu_S/\sigma_S$, Fig. 7b. Moreover, $I_C$ scaling dramatically affects also *x* dispersion, Fig. 8a. While $\mu_x$ is not affected by the choice of $I_C$ (as expected), results in Fig. 8a clearly show a significant increase of $\sigma_x$ at low $I_C$. We attribute this behavior to the small *S* at low $I_C$, which enhances the effects of reset operation randomness. The recombination of each individual Vo has indeed a strong impact on the formation of the barrier when the CF is composed of few Vo's. So, small variations in the number of recombination events may induce relatively large variations of the barrier thickness, *x*. Conversely, at high $I_C$ the CF encompasses many Vo's and the relative effect of an individual recombination event on *x* is much weaker. This highlights the critical role played by $I_C$. Its reduction is largely chased by designers for low-power applications. However, reducing $I_C$ may result in a critical increase of cycling dispersion of both *x* and *S*. Notably, $I_C$ scaling affects the median values of both $R_{HRS}$ and $R_{LRS}$ (i.e. $R_{HRS,MED}$ and $R_{LRS,MED}$, respectively) leaving the median memory window (i.e. $R_{HRS,MED}/R_{LRS,MED}$) unaltered, Fig 9. However, this is a deceitful indicator of the device performance since it completely misses some critical variability issues as the increase of $\sigma_x$ at low $I_C$. A safe indicator of the device performance which fully considers cycling dispersion and its

consequences is instead the worst-case read window (i.e. the ratio between the minimum HRS resistance and the maximum LRS resistance during cycling - $R_{HRS,MIN}/R_{LRS,MAX}$), which is the true margin between HRS and LRS through the device lifetime to be considered in circuit design. As opposite to the median read window, the worst-case read window exhibits a severe degradation at low $I_C$ due to the increased variability of both *x* and *S*, as shown in Fig. 9. This highlights a trade-off between the device power dissipation (proportional to $I_C$) and the device reliability (which is associated with the worst-case read window).

## V. Conclusions

This systematic study of cycling dispersion delivers a clear picture of its sensitivity to the operating conditions in $HfO_x$ RRAM devices. Particularly, the dispersion of both $R_{HRS}$ and $R_{LRS}$ is worsened at low $I_C$, which reduces the worst-case read window. This shows a trade-off between reliability and power consumption.

## References


[1] Y.-S. Chen et al., "Highly scalable hafnium oxide memory with improvements of resistive distribution and read disturb immunity", Proc. of IEEE Electron Devices Meeting (IEDM), pp.1,4, 7-9 Dec. 2009

[2] C. Nauenheim et al., "Nano-Crossbar Arrays for Nonvolatile Resistive RAM (RRAM) Applications", NANO '08 8th IEEE Conference on Nanotechnology, pp.464,467, 18-21 Aug. 2008.

[3] A. Chen, Ionic Memory Technology, in Solid State Electrochemistry II: Electrodes, Interfaces and Ceramic Membranes, First Edition (ed V. V. Kharton), Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim, Germany. 2011. doi: 10.1002/9783527635566.ch1.

[4] B. Govoreanu et al., «10x10nm2 Hf/HfOx crossbar resistive RAM with excellent performance, reliability and low-energy operation», in IEDM Tech. Dig., Washington, DC, USA, 2011.

[5] S. L. Lee et al., «Multi-level switching of triple-layered TaOx RRAM with excellent reliability for storage class memory», Symposium on VLSI Technology (VLSIT), pp. 71 - 72, 2012.

[6] H. Y. Lee et al., «Low power and high speed bipolar switching with a thin reactive Ti buffer layer in robust HfO2 based RRAM», in IEDM Tech. Dig., San Francisco, CA, USA, 2008.

[7] B. Butcher et al., «High endurance performance of 1T1R HfOx based RRAM at low (<20μA) operative current and elevated (150°C) temperature», IEEE International Integrated Reliability Workshop Final Report (IRW), pp. 146 - 150, 2011.

[8] C. W. Hsu et al., "Self-rectifying bipolar TaOx/TiO2 RRAM with superior endurance over 1012 cycles for 3D high-density storage-class memory", Symposium on VLSI Technology, pp. 166 - 167, 2013.

[9] S. Deora et al., "Statistical assessment of endurance degradation in high and low resistive states of the HfO2-based RRAM", IEEE International Reliability Physics Symposium, pp.MY.2.1-MY.2.5, 14-18 April 2013.

[10] H.-S.P. Wong et al., "Metal–Oxide RRAM", Proceedings of the IEEE, vol.100, no.6, pp.1951,1970, June 2012.

[11] L. Larcher et al., "A Compact Model of Program Window in HfOx RRAM Devices for Conductive Filament Characteristics Analysis", IEEE Transactions on Electron Devices, vol.61, no.8, pp.2668-2673, Aug. 2014.

[12] D. Veksler et al., "Methodology for the statistical evaluation of the effect of random telegraph noise (RTN) on RRAM characteristics", IEEE International Electron Devices Meeting (IEDM) 2012, pp.9.6.1,9.6.4, 10-13 Dec. 2012.

[13] F. M. Puglisi et al., "A Complete Statistical Investigation of RTN in $HfO_2$-Based RRAM in High Resistive State", IEEE Transactions on Electron Devices, vol.62, no.8, pp.2606-2613, Aug. 2015.

[14] F. M. Puglisi et al., "RTS noise characterization of $HfO_x$ RRAM in high resistive state", Solid-State Electronics, vol. 84, pp. 160-166, Jun. 2013, ISSN 0038-1101.

[15] F. M. Puglisi et al., «Random Telegraph Signal Noise Properties of $HfO_x$ RRAM in High Resistive State», Proceedings of the IEEE Eurepean Solid-State Device Research Conference (ESSDERC), pp.274-277, 17-21 Sept. 2012.

[16] N. Raghavan et al., "RTN insight to filamentary instability and disturb immunity in ultra-low power switching HfOx and AlOx RRAM", Symposium on VLSI Technology (VLSIT) 2013, pp.T164,T165, 11-13 June 2013.

[17] S. Park et al., "RRAM-based synapse for neuromorphic system with pattern recognition function", Proceedings of the IEEE International Electron Devices Meeting (IEDM), pp.10.2.1-10.2.4, 10-13 Dec. 2012.

[18] F. M. Puglisi et al., «An empirical model for RRAM resistance in low- and high-resistance states», IEEE Electron Device Letters, vol. 34, n. 3, pp. 387-389, 2013.

[19] F. M. Puglisi, P. Pavan, A. Padovani, L. Larcher, "A compact model of hafnium-oxide-based resistive random access memory", Proceedings of IEEE International Conference on IC Design & Technology (ICICDT) 2013, pp.85,88, 29-31 May 2013

[20] D. Garbin et al., "Modeling of OxRAM variability from low to high resistance state using a stochastic trap assisted tunneling-based resistor network", Proceedings of Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), pp.125-128, 26-28 Jan. 2015.

[21] G. Bersuker et al., «Metal oxide resistive memory switching mechanism based on conductive filament microscopic properties», Journal of Applied Physics, vol. 110, p. 124518, 2011.

[22] D. Ielmini et al., "Universal Reset Characteristics of Unipolar and Bipolar Metal-Oxide RRAM", IEEE Transactions on Electron Devices, vol.58, no.10, pp.3246-3253, Oct. 2011.

[23] X. Guan, S. Yu, H.-S. P. Wong, «A SPICE Compact Model of Metal Oxide Resistive Switching Memory With Variations», IEEE Electron Device Letters, vol. 33, n. 10, pp. 1405 - 1407, 2012.

[24] F. M. Puglisi, A. Qafa, P. Pavan, "Temperature Impact on the Reset Operation in HfO2 RRAM", IEEE Electron Device Letters, vol. 36, no. 3, pp. 244-246, Mar. 2015.

# Performance and Reliability Comparison of 1T-1R RRAM arrays with Amorphous and Polycrystalline $HfO_2$

Alessandro Grossi*, Eduardo Perez†, Cristian Zambelli*, Piero Olivo*, and Christian Wenger†
*Università degli Studi di Ferrara, Dip. di Ingegneria, ENDIF, Via G. Saragat 1, 44122 Ferrara, Italy
†IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany

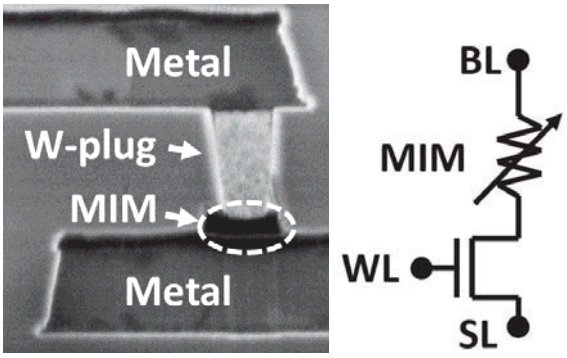
E-mail: alessandro.grossi@unife.it

***Abstract*—In this work, a comparison between 1T-1R RRAM 4kbits arrays manufactured either with amorphous or polycrystalline $HfO_2$ in terms of performance, reliability, Set/Reset operations energy requirements, intra-cell and inter-cell variability during 10k Set/Reset cycles is reported. Polycrystalline array shows higher current ratio, lower switching voltages, lower power consumption, minor endurance degradation and higher overall yield than amorphous array. The drawbacks are represented by the higher Forming voltage, the larger read current distribution after Forming and the higher Reset voltage dispersion.**

## I. Introduction

Resistive Random Access Memories (RRAM) technology gathered significant interest for several applications [1]–[3]. RRAM behavior is based on the possibility of electrically modifying the conductance of a Metal-Insulator-Metal (MIM) stack: the Set operation moves the cell in a low resistive state (LRS), whereas Reset brings the cell in a high resistive state (HRS) [4], [5]. To activate such a switching behavior, some technologies require a preliminary Forming operation [6]–[8].

The choice of a proper MIM technology for RRAM cells, exhibiting good uniformity and low switching voltages, is therefore a key issue for array structures fabrication and reliable electrical operation [9]. Such a process step is mandatory to bring this technology to a maturity level. In this work, a comparison between 1T-1R RRAM 4kbits arrays manufactured either with amorphous [5] or polycrystalline [10] $HfO_2$ is performed. In amorphous $HfO_2$ the conduction mainly occurs through a conductive filament created during the Forming operation with highly variable concentration of defects, whereas in polycristalline $HfO_2$ the conduction occurs only through grain boundaries with a very low defect concentration. These differences in terms of conduction properties and defect concentrations translate into different switching properties [9], with several implications on inter-cell (variations between cells) and intra-cell (cycle-to-cycle variations of any given cell) variability. In this work a comparison in terms of performance, reliability, Set/Reset operations energy requirements, intra-cell and inter-cell variability during 10k endurance cycles is reported.




(a) (b)

Fig. 1. Cross-sectional STEM image (a) and schematic (b) of the 1T-1R cell integrated in the arrays.

## II. Experimental Setup

The 1T-1R memory cells in the 4kbits arrays are constituted by a select NMOS transistor manufactured with a 0.25 $\mu$m BiCMOS technology whose drain is in series to the MIM stack. The wordline (WL) voltage applied to the gate of the NMOS transistor allows setting the cell current compliance. The cross-sectional Scanning Transmission Electron Microscopy (STEM) image of the cell and the 1T-1R cell schematic are reported in Fig. 1. The variable MIM resistor is composed by 150 nm TiN top and bottom electrode layers deposited by magnetron sputtering, a 7 nm Ti layer, and a 8 nm $HfO_2$ layer deposited with two different Atomic Vapour Deposition (AVD) processes resulting either in amorphous (A) or polycrystalline (P) $HfO_2$ films, respectively. The resistor area is equal to 0.4 $\mu m^2$. For amorphous films it has been integrated also a resistor with larger area that shows improved reliability and performance (i.e., 1 $\mu m^2$) [4]. The Forming/Set/Reset operations on the arrays were performed by using an Incremental Pulse and Verify algorithm [11]. The bitline (BL), sourceline (SL) and WL voltages applied during Forming, Set, Reset and Read operations are reported in Tab. I. Reset operations were performed by applying the WL voltage that allows maximizing the cells switching yield

TABLE I
FORMING, SET, RESET AND READ VOLTAGE PARAMETERS.

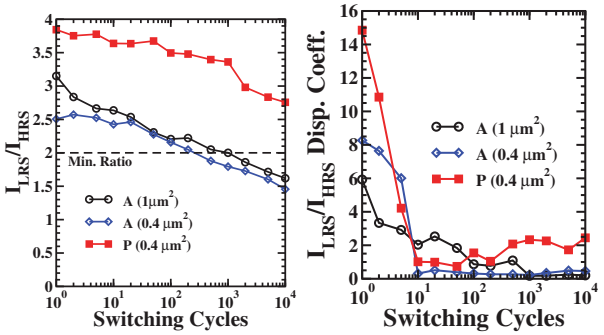
| Operation | $V_{SL}$ [V] | $V_{BL}$ [V] | $V_{WL}$ [V] |
|---|---|---|---|
| Forming | 0 | 2-3.2 | 1.5 |
| Set | 0 | 0.2-3.2 | 1.5 |
| Reset | 0.2-3.2 | 0 | 2.5 (A)/ 2.8 (P) |
| Read | 0 | 0.2 | 1.5 |

(2.8 V on array A and 2.5 V on array P) while avoiding the breakdown of the $HfO_2$ [12]. Pulses were applied during Forming by increasing $V_{BL}$ with $\Delta V_{BL}$=0.01V, whereas during Set and Reset $\Delta V_{BL}$=0.1V and $\Delta V_{SL}$=0.1V have been used, respectively. Each pulse featured a duration of 10$\mu$s, with a rise/fall time of 1$\mu$s to avoid overshoot issues. Set operation was stopped on a cell when the read-verify current reached at least 20$\mu$A, whereas Reset was stopped when reached al least 10$\mu$A. Forming, Set and Reset BL/SL voltages necessary to reach the requested read-verify current targets are extracted from the characterization data and labelled as $V_{FORM}$, $V_{SET}$, and $V_{RES}$, respectively.

## III. EXPERIMENTAL RESULTS

1T-1R cell arrays integrated with A-$HfO_2$ (A-array) with small (0.4 $\mu m^2$) and large (1 $\mu m^2$) resistor area, and P-$HfO_2$ (P-array) resulted in a Forming Yield (calculated as the cell percentage having a read verify current after forming $I_{read} \geq 20\mu$A) of 58%, 90%, and 95%, respectively. Fig. 2 shows the average current ratios between Low Resistive State (LRS) and High Resistive State (HRS) read currents ($I_{LRS}/I_{HRS}$), calculated on the entire cells population during Set/Reset cycling, and their relative dispersion coefficient. The dispersion coefficient, defined as $(\sigma^2/\mu)$, has been used to evaluate the cell-to-cell variability. The minimum current ratio that allows to correcly discriminate between HRS and LRS ($I_{LRS}/I_{HRS}$ >2) is indicated for comparison purposes [5]. Due to the faster cell degradation, the average ratios of A-arrays with resistor area of 0.4 $\mu m^2$ and 1 $\mu m^2$ cross the minimum ratio limit after 200 and 1k cycles, respectively. P-array showed higher ratio ($\approx$ 2.8) even after 10k cycles, but also a higher dispersion coefficient after Forming (i.e., cycle 1). The grain boundaries conduction mechanism in the polycrystalline $HfO_2$ structure could be the reason of the higher cell-to-cell variability in P-arrays [13]. A-array with resistor area of 1 $\mu m^2$ shows a slightly higher average ratio and a slower degradation than A-array with resistor area of 0.4 $\mu m^2$. In smaller cells the presence of defects in the $HfO_2$ stack has a stronger impact on the performance since makes the switching operations more difficult to control, speeds up the degradation and increases the overall inter-cell variability [14].

Fig. 3 shows a comparison between $I_{LRS}$ and $I_{HRS}$ cumulative distributions measured at cycle 1 and after the 10k Set/Reset cycling test: A-arrays show more compact distributions at cycle 1, however after cycling P-array shows a higher percentage of correctly switching cells reaching the Set/Reset verify targets. $I_{HRS}$ cumulative distribution in P-array shows




(a) (b)

Fig. 2. $I_{LRS}/I_{HRS}$ current ratio average values (a) and dispersion coefficients (b) calculated during cycling.

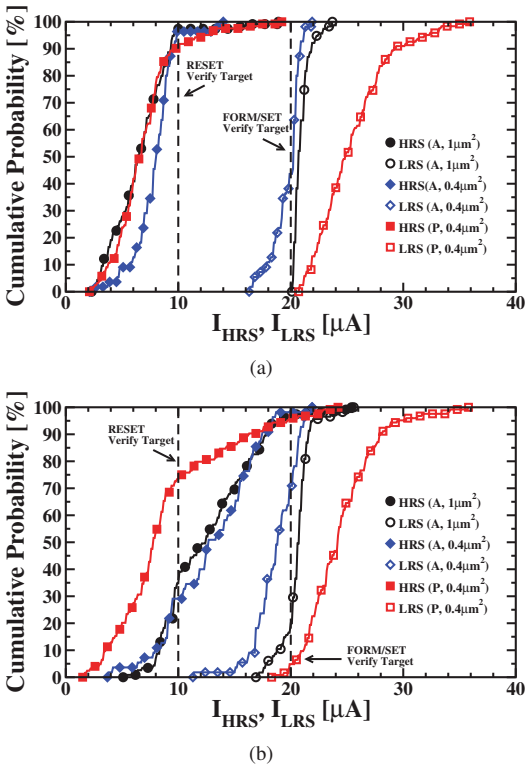



Fig. 3. $I_{HRS}$ and $I_{LRS}$ cumulative distributions at cycle 1 (a) and at cycle 10k (b).

a larger distribution tail at cycle 1 compared to A-arrays. After 10k cycles the cells degradation makes more difficult to break or re-create the filament, hence the voltage requested to reach the verify target increases as well as the number of cells not able to reach the verify target. An enlargement of the upper tail in P-array HRS distribution can be observed whereas on A-arrays a strong shift of the distributions towards higher currents occurs, since a higher number of cells is not able reach the Reset threshold. The reason of the lower ratio in A-array with small resistor area can be explained by the cumulative distributions, since they show lower $I_{LRS}$ and higher $I_{HRS}$ than cells with larger resistor area either at cycle 1 and after

ISBN 978-1-4673-8608-1

IEEE Catalog number CFP1649D-USB

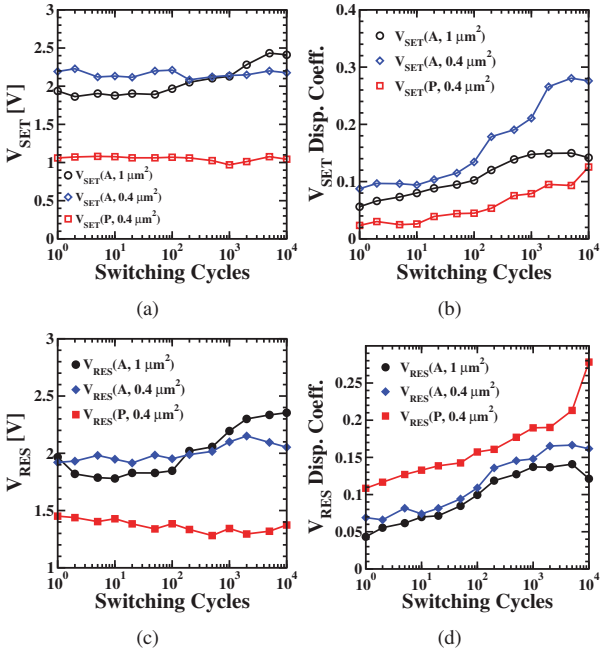



Fig. 4. $V_{SET}$ and $V_{RES}$ average values (a,c) and dispersion coefficients (b,d) calculated during cycling.

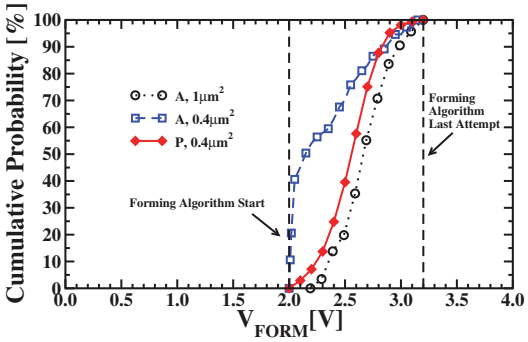



Fig. 5. $V_{FORM}$ cumulative distributions.

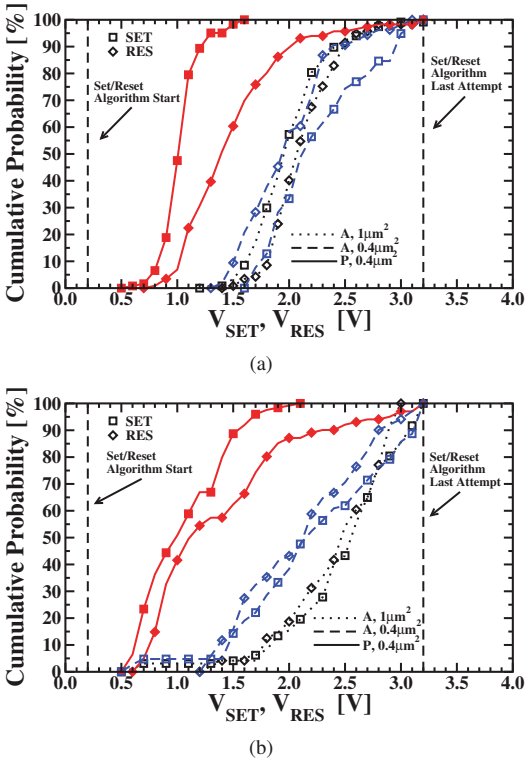



Fig. 6. $V_{SET}$ and $V_{RES}$ cumulative distributions at cycle 1 (a) and at cycle 10k (b).

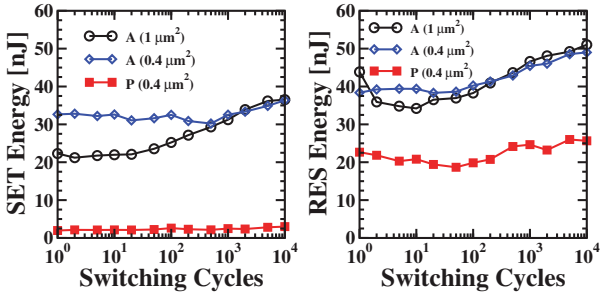
10k cycles. In $I_{LRS}$ cumulative distributions the cells not able to reach the Set verify target generate a lower tail on P-arrays after 10k cycles, whereas on A-arrays a higher number of cells is not able to reach the Set verify target especially when cells with resistor area of 0.4 $\mu$m$^2$ are considered. This results into a strong shift of the distributions towards lower currents, especially in A-array with small resistor area that shows a high number of cells not reaching the Set verify target even at cycle 1.

Fig. 4 shows the average Set and Reset switching voltages ($V_{SET}$, $V_{RES}$) and their relative dispersion coefficients: lower $V_{SET}$ and $V_{RES}$ are required on P-array which also shows no variations during Set/Reset cycling, whereas $V_{SET}$, $V_{RES}$ increase on A-arrays during cycling. $V_{RES}$ on P-array shows the highest variability: such operation is critical and very difficult to control in RRAM arrays since it strongly depends on how the filament is created: over Forming, as well as endurance degradation, can make the filament difficult to disrupt, increasing the $V_{RES}$ variability [11]. A-arrays show similar behavior of the average $V_{SET}$ and $V_{RES}$ (a lower average $V_{SET}$ is observed on A-array with larger resistor area only up to 500 cycles), while a higher $V_{SET}$ and $V_{RES}$ dispersion can be observed in A-array with smaller resistor area.

Fig. 5 shows the cumulative distributions of switching voltages during Forming, while Fig. 6 shows the Set and Reset switching voltages cumulative distributions at cycle 1 and after the Set/Reset cycling. Forming, Set and Reset incremental pulse algorithms starting point and last attempt are indicated, corresponding to the first and the last voltage pulse available in the incremental pulse and verify procedure [11]. P-array requires lower $V_{SET}$ and $V_{RES}$ but higher $V_{FORM}$ if compared to A-array with the same resistor area. A-array with larger resistor area requires higher $V_{FORM}$. Moreover, it can be observed that $\approx 40\%$ of the devices with smaller resistor area reached the forming threshold at $V_{FORM}$=2 V, corresponding to the first attempt of the Forming Algorithm. Since P-array shows a more compact distribution on $V_{SET}$ and a larger $V_{RES}$ than A-arrays, faster Set operation could be reliably used on P-array, whereas on Reset an incremental pulse with verify technique is required to ensure good reliability. A-arrays show large distributions on both $V_{SET}$ and $V_{RES}$, hence the adaptation of incremental pulse with verify techniques is mandatory on such arrays.

ISBN 978-1-4673-8608-1

IEEE Catalog number CFP1649D-USB




(a) (b)

Fig. 7. Energy required to perform Set (a) and Reset (b) operations as a function of the Set/Reset cycle number.

Fig. 7 shows the average energy required to perform Set and Reset operations on a single cell. The overall energy required to create/disrupt the conductive filament during Set/Reset operations has been calculated as [11]:

$$E = \sum_{i=1}^{n} V_{pulse,i} * I_{pulse,i} * T_{pulse} + V_{read} * I_{read,i} * T_{read} \quad (1)$$

Where $n$ is the number of reset pulses applied during incremental pulse operation, $V_{pulse,i}$ is the pulse voltage applied at step $i$, $I_{pulse,i}$ is the current flowing through RRAM cell during pulse $i$ application, $T_{pulse} = 10\mu s$ is the pulse length, $V_{read}$ =0.2 V is the read voltage applied during verify operation, $I_{read,i}$ is the current read on the RRAM during read verify step $i$, and $T_{read} = 10\mu s$ is the verify pulse length. P-array shows lower power consumption with a lower increase during cycling thanks to a lower $V_{SET}$ and $V_{RES}$. A-arrays with different resistor area show similar power consumption during Reset operation, whereas a lower consumption during Set is observed on A-array with larger resistor area only up to 500 cycles since cells with larger resistor area require lower $V_{SET}$.

## IV. Conclusions

1T-1R RRAM arrays manufactured with P-$HfO_2$ shows several advantages compared to A-$HfO_2$ even considering their improved process: higher current ratio, lower switching voltages, lower power consumption, minor endurance degradation and higher overall yield. Moreover, P-array show very low $V_{SET}$ variability, hence faster Set operation could be reliably performed. P-array disadvantages are represented by the larger HRS distribution after Forming, the higher Reset voltage dispersion and the higher $V_{FORM}$ if compared to A-array with the same resistor area, however but it must be pointed out that Forming operation is performed only once. The grain boundaries conduction mechanism in the polycrystalline $HfO_2$ structure could be the reason of the higher cell-to-cell variability in P-arrays.

## Acknowledgments

This work was supported by the European Union's H2020 research and innovation programme under grant agreement N$^o$ 640073.

## References

[1] S. Tanachutiwat, M. Liu, and W. Wang, "FPGA Based on Integration of CMOS and RRAM," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 19, no. 11, pp. 2023–2032, Nov 2011.

[2] D. Garbin, E. Vianello, O. Bichler, Q. Rafhay, C. Gamrat, G. Ghibaudo, B. DeSalvo, and L. Perniola, "HfO2-Based OxRAM Devices as Synapses for Convolutional Neural Networks," *IEEE Trans. on Electron Devices*, vol. 62, no. 8, pp. 2494–2501, Aug 2015.

[3] T. Xu and V. Leppanen, "Analysing emerging memory technologies for big data and signal processing applications," in *Digital Information Processing and Communications (ICDIPC), 2015 Fifth International Conference on*, Oct 2015, pp. 104–109.

[4] C. Zambelli, A. Grossi, D. Walczyk, T. Bertaud, B. Tillack, T. Schroeder, V. Stikanov, P. Olivo, and C. Walczyk, "Statistical analysis of resistive switching characteristics in ReRAM test arrays," in *IEEE Int. Conf. on Microelectronics Test Structures (ICMTS)*, Mar 2014, pp. 27–31.

[5] C. Zambelli, A. Grossi, P. Olivo, D. Walczyk, J. Dabrowski, B. Tillack, T. Schroeder, R. Kraemer, V. Stikanov, and C. Walczyk, "Electrical characterization of read window in ReRAM arrays under different SET/RESET cycling conditions," in *IEEE Int. Memory Workshop (IMW)*, May 2014, pp. 1–4.

[6] D. Walczyk, T. Bertaud, M. Sowinska, M. Lukosius, M. A. Schubert, A. Fox, D. Wolansky, A. Scheit, M. Fraschke, G. Schoof, C. Wolf, R. Kraemer, B. Tillack, R. Korolevych, V. Stikanov, C. Wenger, T. Schroeder, and C. Walczyk, "Resistive switching behavior in TiN/$HfO_2$/Ti/TiN devices," in *Int. Semiconductor Conf. Dresden-Grenoble (ISCDG)*, Sept 2012, pp. 143–146.

[7] P. Lorenzi, R. Rao, and F. Irrera, "Forming kinetics in $HfO_2$-based RRAM cells," *IEEE Trans. on Electron Devices*, vol. 60, no. 1, pp. 438–443, 2013.

[8] A. Grossi, D. Walczyk, C. Zambelli, E. Miranda, P. Olivo, V. Stikanov, A. Feriani, J. Sune, G. Schoof, R. Kraemer, B. Tillack, A. Fox, T. Schroeder, C. Wenger, and C. Walczyk, "Impact of Intercell and Intracell Variability on Forming and Switching Parameters in RRAM Arrays," *IEEE Trans. on Electron Devices*, vol. 62, no. 8, pp. 2502–2509, Aug 2015.

[9] K. Morgan, R. Huang, S. Pearce, and C. de Groot, "The effect of atomic layer deposition temperature on switching properties of HfOx resistive RAM devices," in *IEEE Int. Symp. on Circuits and Systems (ISCAS)*, June 2014, pp. 432–435.

[10] H.-D. Kim, F. Crupi, M. Lukosius, A. Trusch, C. Walczyk, and C. Wenger, "Resistive switching characteristics of integrated polycrystalline hafnium oxide based one transistor and one resistor devices fabricated by atomic vapor deposition methods," *Journal of Vacuum Science and Technology B*, vol. 33, no. 5, pp. 052 204.1–052 204.5, 2015.

[11] A. Grossi, C. Zambelli, P. Olivo, E. Miranda, V. Stikanov, C. Walczyk, and C. Wenger, "Electrical characterization and modeling of pulse-based forming techniques in RRAM arrays," *Solid-State Electronics*, vol. 115, Part A, pp. 17 – 25, 2016. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0038110115002828

[12] A. Grossi, C. Zambelli, P. Olivo, E. Miranda, V. Stikanov, T. Schroeder, C. Walczyk, and C. Wenger, "Relationship among current fluctuations during forming, cell-to-cell variability and reliability in RRAM arrays," in *IEEE Int. Memory Workshop (IMW)*, May 2015, pp. 1–4.

[13] V. Iglesias, M. Porti, M. Nafra, X. Aymerich, P. Dudek, and G. Bersuker, "Dielectric breakdown in polycrystalline hafnium oxide gate dielectrics investigated by conductive atomic force microscopy," *Journal of Vacuum Science and Technology B*, vol. 29, no. 1, 2011.

[14] S. Balatti, S. Ambrogio, A. Cubeta, A. Calderoni, N. Ramaswamy, and D. Ielmini, "Voltage-dependent random telegraph noise (RTN) in HfOx resistive RAM," in *IEEE Int. Reliability Physics Symposium*, June 2014, pp. MY.4.1–MY.4.6.

# Intra-device statistical parameters in variability-aware modelling of Resistive Switching devices.

A. Crespo-Yepes, J. Martin-Martinez, I. Rama, M. Maestro, R. Rodriguez, M. Nafria, X. Aymerich.

Departament d'Enginyeria Electrònica.
Universitat Autònoma de Barcelona (UAB).
08193 Bellaterra, Spain
albert.crespo@uab.cat

M. B. Gonzalez, F. Campabadal.

Institut de Microelectrònica de Barcelona.
ICM-CNM (CSIC)
08193 Bellaterra, Spain
Mireia.Bargallo@imb-cnm.csic.es

***Abstract*—Variability of the currents associated to both low and high resistance states is an inherent characteristic of the resistive switching phenomenon. This variability could be critical for the use of these devices for memory applications, so that it is necessary to develop models that account for it and help predicting its effect. In this work, we present a method based on an electrical model to reproduce the resistive switching currents, at both low and high resistive states, including variability. This allows analyzing the impact of device variability on circuit performance.**

***Keywords—Resistive Switching; variability; circuit-based model; model fititng; model parameter statistical distributions; RS array analysis tool; leakage current;***

## I. INTRODUCTION

Resistive Switching (RS) devices have become potential candidates for nonvolatile memory applications and promising basis of new reconfigurable computing architectures [1-4]. To explore circuit and memory designs based in RS devices, electrical models are needed, implementable in circuit simulation tools, to evaluate characteristics like power consumption or performance in large RS arrays [5-10]. In this scenario, one of the challenges is to develop models that account for the large variability observed in the RS devices electrical characteristics. This work is focused on the intra-device variability of the RS devices. The statistical distributions of the model parameters in an equivalent circuit model are obtained from the experimental data and their main properties have been analyzed. A procedure is developed to correctly reproduce these distributions and obtain realistic current values associated to the RS phenomenon.

## II. MODELLING OF THE RS I-V CHARACTERISTICS

RS devices suffer from large intra-device variability (cycle-to-cycle variability), both at low resistive state (LRS) and high resistive state (HRS), which must be properly accounted for in SPICE-like models. This variability is observed in the spread of the current values in each state at low voltages and also in different switching voltages in the switching events between states. In this work, we focus the attention on the current levels at low voltages (reading window). For example, Figure 1 shows typical RS current-voltage (I-V) curves obtained during 400 cycles on a Ni/$HfO_2$/$n^+$Si device structure with 20nm $HfO_2$ layer and area of 5x5µm$^2$. Note the large cycle-to-cycle variability in the device electrical characteristics, especially in the HRS.

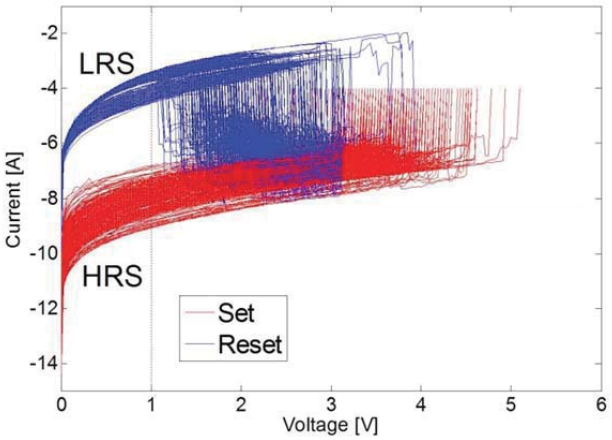



**Figure 1:** *Typical Resistive Switching I-V curves obtained during 400 cycles in Ni/$HfO_2$/$n^+$Si devices with 20nm $HfO_2$ layer and area of 5x5µm$^2$. A current limit of 100uA was used during Set to allow reset events. Large variability is observed in both states at low voltages (reading window).*

To model the RS I-V curves (at both LRS and HRS) we use a Diode-Resistor circuit (Figure 2) whose output is fully defined by three parameters: the resistance value (R), the diode saturation current (Is) and diode ideality factor (n) [11, 12].

Spanish MINECO and ERDF (TEC2013-45638-C3-1-R, TEC2014-52152-C3-1-R, and TEC2014-54906-JIN), and the Generalitat de Catalunya (2014SGR-384) have partially supported this work.

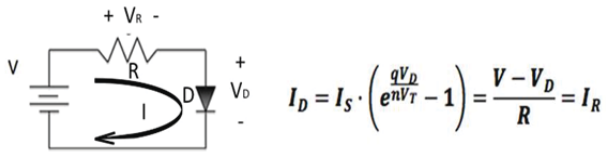



**Figure 2:** *Equivalent model for the RS device based on a Diode-Resistor circuit. Resistance value (R), saturation current (Is) and ideality factor (n) of the diode are used to fit the conduction of the RS devices at both resistive states.*

An automatized fitting process has been developed to extract the three circuit parameters corresponding to the I-V curve measured on a device during cycling (as those in figure 1), within operation regime (V≤1). Figure 3 shows several examples of fittings of the experimental I-V curves, where it can be observed that the circuit is able to correctly reproduce the measurements, regardless of the device state and current magnitude.

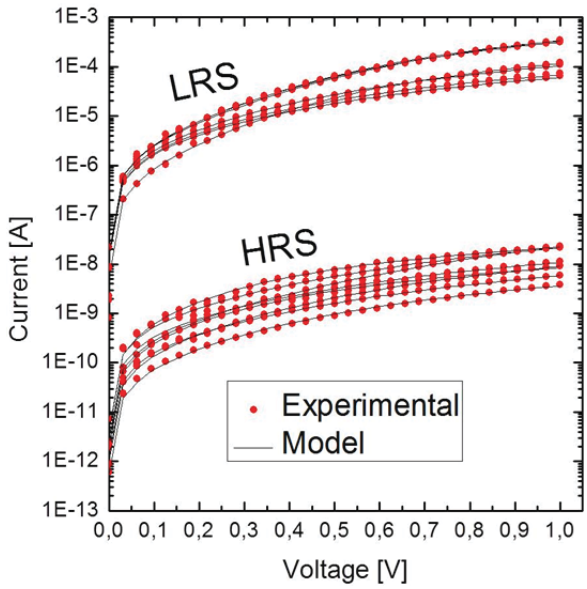



**Figure 3:** *Examples of LRS and HRS I-V curves fittings. Circles correspond to the experimental results and lines to the model fittings. With the suitable parameter sets, the model reproduces properly the experimental curves at both states.*

The fitting of all the curves (3000 for each RS state in the example shown) allows obtaining the statistical distributions of the model parameters. Dots in Figure 4 a, b and c show the experimental cumulative probability distributions of the 'R', 'Is' and 'n' parameters, respectively, for the LRS and HRS states. Clearly, two different ranges of values are obtained for the 'R' and 'Is' parameters, ascribed to the LRS and HRS. However, the 'n' parameter distributions for the HRS and LRS overlap, being the spread larger for the HRS case. This is because the fittings are very sensitive to the value of this parameter.

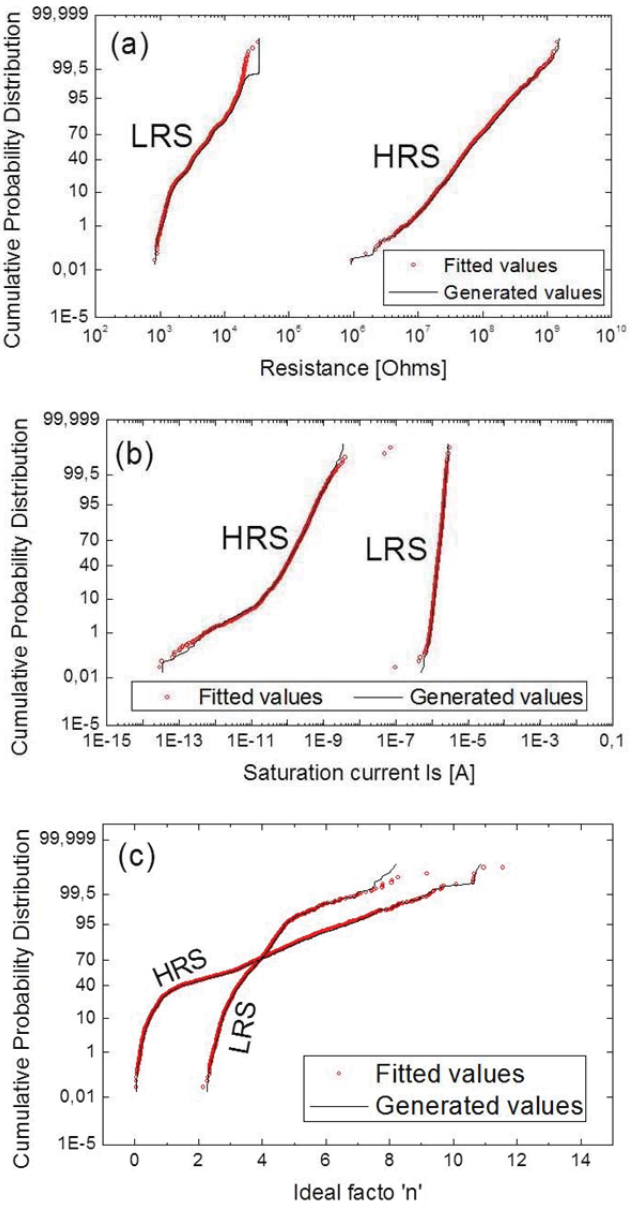



**Figure 4:** *Statistical distributions of the circuit model parameters obtained by fitting the experimental curves (dots), a) Resistance (R), b) Saturation current (Is) and c) Ideality factor (n) of the diode. In the HRS and LRS, two different ranges of values are obtained for R and Is indicating a clear change of the electrical properties of the conductive filament. Lines correspond to the distributions generated using the proposed method.*

An important point to be analyzed is the correlation between the model parameters. Figure 5 shows a 3D plot of the complete set of parameters, for the LRS (top) and HRS (bottom). The projections on the three planes show that the correlation between parameters cannot be neglected, being

larger for the HRS. This correlation between them is a key point to accurately model the current variability. Since, if it was not taken into account, larger values of current (larger variability) could be obtained. For example, not all values of the 'Is' parameter range can be included in the model, when a low 'R' is considered. If this restriction was not taken into account, an unrealistic larger current variability would be predicted. For this reason, any new set of parameters must follow the same statistical distribution, but also the same correlation between parameters than the experimental results.

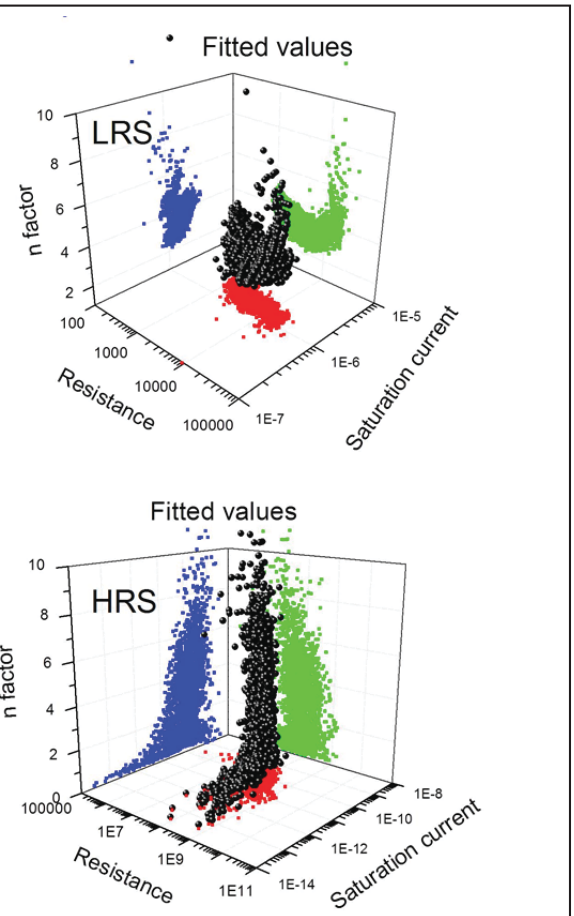



**Figure 5:** *3D plot of model parameter sets (black points) obtained from the fitting of the experimental curves for the LRS (top) and the HRS (bottom). Projections show the correlation between parameters separately. Correlation between parameters at HRS is larger than at LRS.*

## III. Statistical Generation of Model Parameter

To accurately include the RS currents variability into circuit simulators, the statistical distributions of the Resistor-Diode model parameters (Fig. 4) have to be properly described. However, the complexity of these statistical distributions makes difficult to take advantage of analytical expressions. It is because the obtained distributions are not related to typical distributions, and cannot be described by a simple equation. Then no seed for typical distributions can be considered for easily generate random values of the model parameters. For this reason, we have used a random number generator implicit method, which correctly reproduces the statistical distributions of all the parameters (black lines in Figure 4) and also the correlation between them. This method consists in obtaining a 3D discrete cumulative probability function that describes the statistics and correlation, by meshing the range of the three parameters at the same time.

Figure 6 shows the 3D plot of the generated values for LRS (top) and HRS (bottom). As it can be observed, distributions and correlations reflected in the projections in figures 5 and 6 are statistically identical. Larger set of parameters can be generated than experimentally obtained. Moreover, the extrapolation of the experimental distributions to extreme percentiles allows increasing the statistical sample size, reaching a proper statistical description even in the least probable cases of parameter combinations.

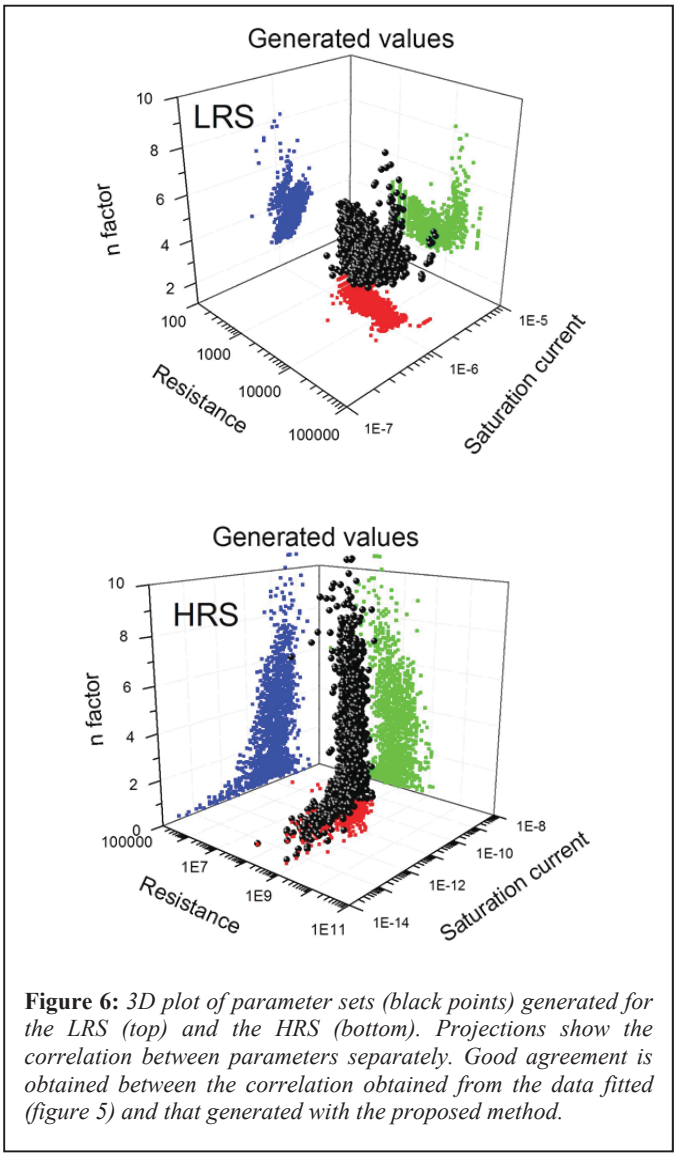



**Figure 6:** *3D plot of parameter sets (black points) generated for the LRS (top) and the HRS (bottom). Projections show the correlation between parameters separately. Good agreement is obtained between the correlation obtained from the data fitted (figure 5) and that generated with the proposed method.*

The Diode-Resistor circuit and the generated statistical parameters have been introduced into a circuit simulator, and the resulting currents have been compared to the experimental results (Figure 7). The good agreement between the experimental and simulated current distributions allows concluding that with the presented procedure the intra-device RS I-V curves variability can be properly reproduced in circuit simulators, even when complex distributions are obtained, such is the case.

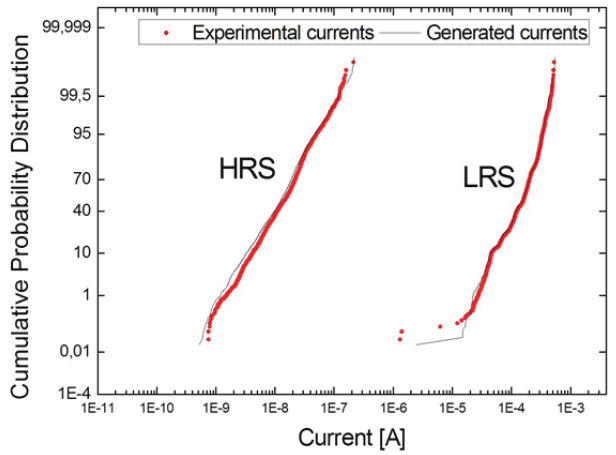



**Figure 7:** *Cumulative probability distributions of experimental (circles) and generated (lines) for LRS and HRS currents at 1V. The observed experimental variability can be properly described with the generated statistically distributed parameters sets.*

## IV. Conclusions

A diode-resistor equivalent circuit model has been used to describe the RS electrical characteristics, for both LRS and HRS. The fitting of a large number of I-V experimental curves (obtained during device cycling) has allowed evaluating the statistical distributions of the model parameters, which cannot be described by simple analytical expressions. A method has been proposed to correctly reproduce the experimental distributions, which accounts for the observed parameter correlation that must be not neglected to reproduce the observed variability. The model (and the suitable model parameters) can be introduced into circuit simulators to analyze the impact of device variability on circuit performance. Moreover, this method allows generating a large number of sets of parameter values for the analysis of a large RS device arrays.

## *References*

[1] U. Russo, D. Ielmini, C. Cagli, and A. L. Lacaita, "Filament Conduction and Reset Mechanism in NiO-Based Resistive-Switching Memory (RRAM) Devices," IEEE Transactions on Electron Device, vol. 56, issue 2, pp. 186-192, 2009.

[2] C. Schindler, S. C. P. Thermadam, R. Waser, M. N. Kozicki, "Bipolar and Unipolar Resistive Switching in Cu-Doped SiO2," IEEE Transactions on Electron Device, vol. 54, issue 10, pp. 2762-2768, 2007.

[3] R. Waser, R. Dittmann, G. Staoikoc, K. Szot, "Redox-based resistive switching memories – nanoionic mechanism, prospects, and challenges," Advanced Materials, vol. 21 issue 25-26, pp. 2632-2663, 2009.

[4] A. Sawa, " Resisitive Switching in transition metal oxides," Materials Today, vol. 11, No. 6, 2008.

[5] M. Maestro, J. Diaz, A. Crespo-Yepes, M. B. Gonzalez, J. Martin-Martinez, R. Rodriguez,M. Nafria, F. Campabadal, X. Aymerich, "A new high resolution Random Telegraph Noise (RTN) characterization method for resistive RAM," EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), pp. 133-136, 2015.

[6] E. Linn, S. Menzel, R. Rosezin, U. Bottger, R. Bruchhaus , R. Waser, "Modeling Complementary Resistive Switches by nonlinear memristive systems," IEEE conference on Nanotechnology (IEEE-NANO), pp. 1474-1478, 2010.

[7] J. J.S. Yang, D. B. Sturkov, D. R. Stewart, "Memristive devices for computing," Nature Nanotechnology, vol. 8, pp. 13-24, 2013.

[8] X. Lian, L. Shibing, C. Cagli, J. Buckley, E. Miranda, L. Ming, J. Suñe, "Quantum point contact model of filamentary conduction in resistive switching memories," International Conference on Ultimate Integrated on Silicon (ULIS), pp. 101-104, 2012.

[9] U. Russo, D. Ielmini, C. Cagli, A. L. Lacaita, "Self-Accelerated Thermal Dissolution Model for Reset Programming in Unipolar Resistive-Switching Memory (RRAM) Devices," IEEE Transactions on Electron Devices, vol. 56, issue 2, pp. 193-200, 2009.

[10] Y. Shimeng, X. Guan, H. S. P. Wong, "On the Switchin parameter variation of metal oxide RRAM – PartII: Model corroboration and device design strategy," IEEE Transactions on Electron Devices, vol. 59, issue 4, pp. 1183-1188, 2012.

[11] E. Miranda, D. Jimenez, J. Suñe, "From post-breakdown conduction to resistive switching effect in thin dielectric films," IEEE International Reliability Physics Symposium (IRPS), pp. GD.5.1-GD.5.6, 2012.

[12] J. Martin-Martinez, B. Kaczer, R. Degraeve, P. Roussel, R. Rodriguez, M. Nafria, X. Aymerich, B. Diericky, G. Groeseneken, "Circuit design-oriented stochastic piecewise modelling of the post-breakdown gate current in MOSFETs: Applications to ring oscillators," IEEE Transactions on Device and Material Reliability, vol. 12, issue 1, pp. 78-85, 2012.

# Impact of the design layout on threshold voltage in SiGe channel UTBB-FDSOI pMOSFET

R. Berthelon[1,2,3], F. Andrieu[3], S. Ortolland[1], R. Nicolas[1], T. Poiroux[3], E. Baylac[1], D. Dutartre[1], E. Josse[1], A. Claverie[2], M. Haond[1]

[1] STMicroelectronics, 850 rue Monnet, B.P. 16, F-38926 Crolles, France
[2] CEMES-CNRS, 29 Rue Jeanne Marvig 31055 Toulouse Cedex 4, France
[3] CEA-LETI, Minatec campus, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France
remy.berthelon@st.com

***Abstract*— The introduction of SiGe channel for pMOSFETs in FDSOI technology enables to achieve high performance. However, it has been demonstrated that such a global stressor induces layouts effects. In this paper, we present an exhaustive study of layout impact on threshold voltage. Especially, dissymmetric layouts, non-rectangular active areas and multifinger transistors are investigated. We propose an analytical model based on stress profile to reproduce the layout dependences. This model reproduces the experimental data with good accuracy, whatever the shape of the active area.**

***Keywords*— FDSOI; SiGe; Stress; Layout effects; Threshold voltage;**

## I. INTRODUCTION

A UTBB-FDSOI (Ultra-Thin Body and Buried oxide - Fully Depleted Silicon On Insulator) technology has been developed at the 14nm node. It highlights a -34% delay (or +50% frequency) improvement along with a 100mV supply voltage reduction (0.8V *vs.* 0.9V) over the 28nm FDSOI technology [1]. This performance is mainly achieved thanks to the introduction of a high-k metal gate first, a 6nm thin SiGe channel and SiGe sources/drains in pMOSFETs. Even if some literature papers already evidenced layout effects induced by such a global stressor [2,3,4], no exhaustive study was reported up to now about the impact of design layouts on the electrical characteristics, whatever the shape of the active area.

For this purpose, we have extracted the threshold voltage (*Vth*) of transistors down to Lg=20nm gate length as a function of several layout parameters. The length and shape of the active region, as well as the number of gate fingers have been investigated. We have developed an analytical model based on the physical mechanical behavior, which reproduces accurately the experimental data.

## II. ACTIVE EXTENSION LENGTHS

First, we have studied the effect of the active extension lengths, i.e. the gate-to-STI distances on active, called SA and SB (Figure 1a). The threshold voltage for both nMOS (Figure 2) and pMOS (Figure 3) have been extracted at a given current and here in the case of a symmetric layout (SA=SB).

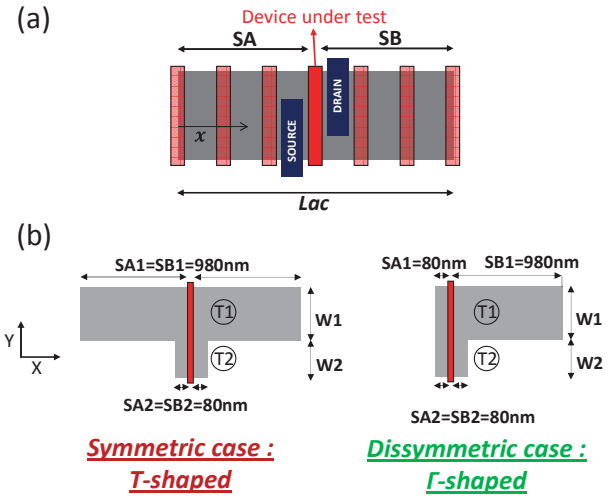



Figure 1. (a) Typical layout of tested devices. SA and SB are the distances between the gate and the active area edge on the left and right sides, respectively. (b) Scheme of non-rectangular layouts. Symmetric case (T-shaped) on the left and dissymmetric case (Γ-shaped) on the right.

The threshold voltage of nMOS devices does not depend on SA/SB, evidencing that the channel of nMOS devices is not stressed, especially by the Shallow-Trench-Isolation (STI). On the other hand, the pMOS threshold voltage strongly increases with the reduction of the active length. Unlike nMOS with silicon channel, the pMOS channel is made of $Si_{0.75}Ge_{0.25}$, obtained by enrichment process. The threshold voltage shift when active length is reduced (short SA/SB) suggests a modification of the stress in the channel of the transistor. For long and large devices, the stress from SiGe is compressive biaxial, whereas it becomes highly uniaxial for short SA/SB [2]. This change of stress configuration leads to a threshold voltage increase of 88mV from SA=SB=980nm to SA=SB=80nm. We have also extracted the $V_{th}$ for dissymmetric layouts (SA≠SB). Figure 4 shows a similar trend for SA≠SB as on Figure 3 for SA=SB. In these dissymmetric layouts, the distance from one edge of the active area (SB) is fixed at either 80nm or 980nm, whereas the distance with the

other edge (SA) varies. It demonstrates that the threshold voltage is directly limited by the shorter gate-to-STI distance, which is the minimum of SA, SB, in agreement with mechanical simulations.

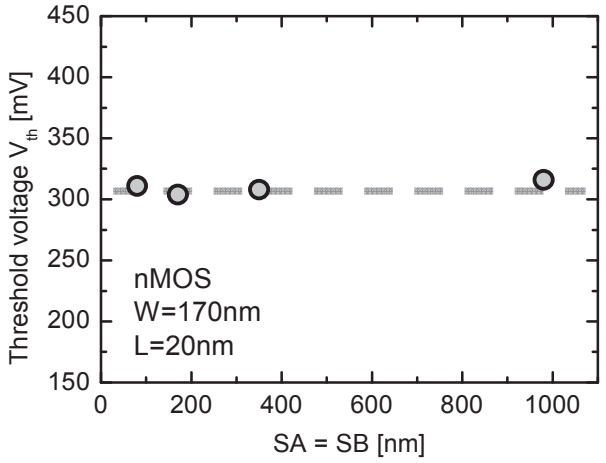



Figure 2. Threshold voltage of nMOS device as a function of SA=SB. No change of *Vth* is observed since nMOS active is made of unstrained Si and evidencing no stress from STI.

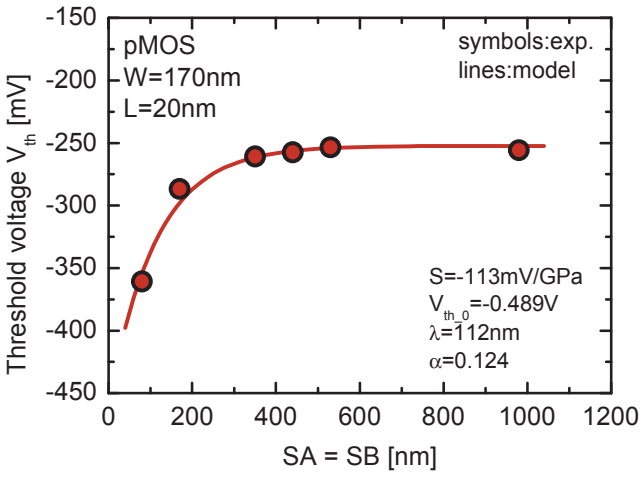



Figure 3. Threshold voltage of pMOS device as a function of SA=SB. The threshold voltage is strongly impacted by the reduction of active length. This is due to the change of SiGe channel stress configuration and level close to the active edge.

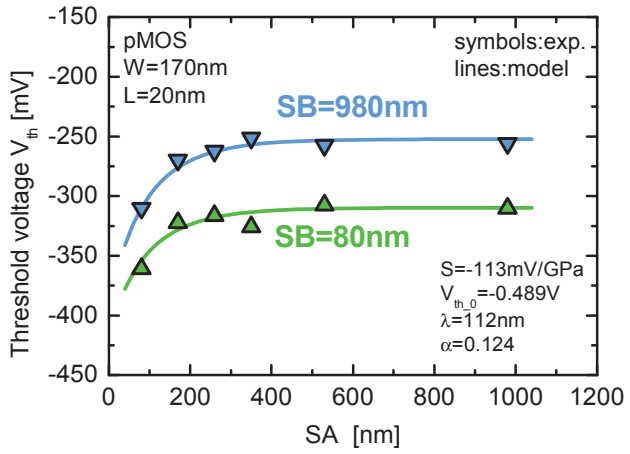



Figure 4. Threshold voltage variation *vs.* extension length for dissymmetric layouts (SA≠SB). The distance of only one edge (SA) varies while the distance of the other edge (SB) is fixed at either 80nm or 980nm from the gate. The threshold voltage value is limited by the shortest extension length.

In order to establish a model of threshold voltage variation with layout, we use a stress model similarly as in [5]:

$$\sigma(x, Lac) = \sigma_0 \left[\frac{1}{2}\left(\left(1-\exp\left(-\frac{x}{\lambda}\right)\right)^{\alpha} + \left(1-\exp\left(\frac{Lac-x}{\lambda}\right)\right)^{\alpha}\right)\right]^{1/\alpha} \quad (1)$$

where $\sigma_0$=2.1GPa is the sum of the initial level of stress from $Si_{0.75}Ge_{0.25}$ channel and the stress from $Si_{0.7}Ge_{0.3}$:B Source and Drain. $x$ is the position along the active length *Lac,* and $\lambda$ and $\alpha$ are fitting parameters, image of the impact of the edge promiscuity on stress level. The value of stress along active length is plotted on Figure 5, showing that the level of stress is impacted by edge effects when active length is reduced (SA=SB=80nm).

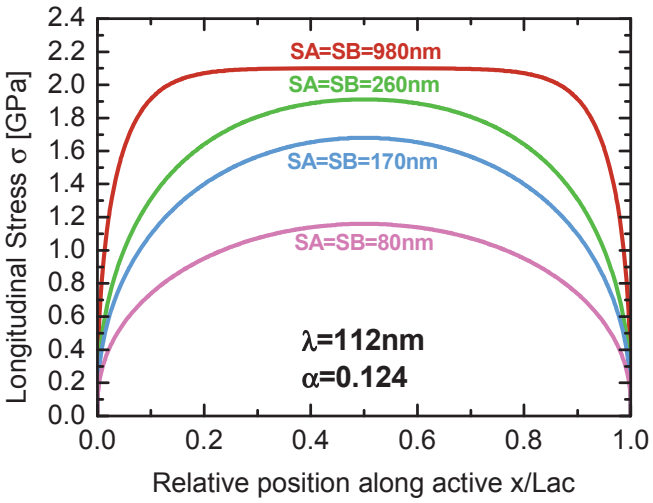



Figure 5. Stress value along the active position from the model of Eq. (1) with fitting parameters used to reproduce experimental data (λ=112nm and α=0.124). The level of longitudinal stress is impacted when extension lengths are reduced.

The threshold voltage is then derived from the model of stress, using a first order linear longitudinal stress sensibility:

$$V_{th}(SA,SB) = V_{th0} + S.\sigma_0 \left[\frac{1}{2}\left(\left(1-\exp\left(-\frac{SA+\frac{Lg}{2}}{\lambda}\right)\right)^{\alpha} + \left(1-\exp\left(\frac{SB+\frac{Lg}{2}}{\lambda}\right)\right)^{\alpha}\right)\right]^{\frac{1}{\alpha}} \quad (2)$$

where $V_{th0}$ is the threshold voltage of totally relaxed channel, $S$ is the stress sensibility (S=-113mV/GPa, extracted from our measurements). The stress value of interest is taken at the middle of the channel ($x$=SA+Lg/2), which is a relevant approximation for short channels (Lg=20nm compared to minimum active length $Lac$=180nm for the case SA=SB=80nm). As shown in Figure 3 and Figure 4, our model well reproduces the experimental data for both symmetric and dissymmetric layouts.

## III. Non-Rectangular Active Area

Non-rectangular active areas have also been studied in symmetric or non-symmetric layouts (Figure 1b). In these cases, the extension length in the X direction differs along the channel width (i.e. along the Y direction). The level of stress in such non-rectangular active area is more complex.

A first approach consists in modelling the transistor by 2 sub-transistors (T1 and T2) in parallel, whose SA/SB and width (W) are different: SA1, SB1, W1 for sub-transistor 1 (T1) and SA2, SB2, W2 for sub-transistor 2 (T2). In this so-called "2-transistor model", the weight of each sub-transistor in the total conduction is directly linked to the so-called width ratio (W ratio = W2/(W1+W2)). This model does not take into account any shear stress at T1/T2 transition. Under the assumption that the threshold voltage is extracted in the subthreshold regime and the subthreshold swing is independent of the stress, the threshold voltage of the transistor with non-rectangular area is expressed as:

$$V_{th} = -SS\ln\left[\frac{W_1}{W_1+W_2}exp\left(-\frac{V_{th1}}{SS}\right)+\frac{W_2}{W_1+W_2}exp\left(-\frac{V_{th2}}{SS}\right)\right] \quad (3)$$

where $V_{th1}$ and $V_{th2}$ are the threshold voltages of the transistors T1 and T2 with layout parameters SA1, SB1, W1 and SA2, SB2, W2, respectively (cf. Figure 1) and $SS$ is the subthreshold swing ($SS$=80mV/dec).

Another approach can be used in order to get simple netlists extracted after the Layout Versus Schematics (LVS). It consists in the extraction of only one transistor of equivalent SA and SB. Equivalent SA and SB are calculated by a Matthiessen's law in this so-called "1-transistor model" :

$$SAeq = \left(\frac{W_1}{W_1+W_2}\frac{1}{SA_1}+\frac{W_2}{W_1+W_2}\frac{1}{SA_2}\right)^{-1} \quad (4)$$

Figure 6 illustrates both approaches for modelling transistors built on non-rectangular active area.

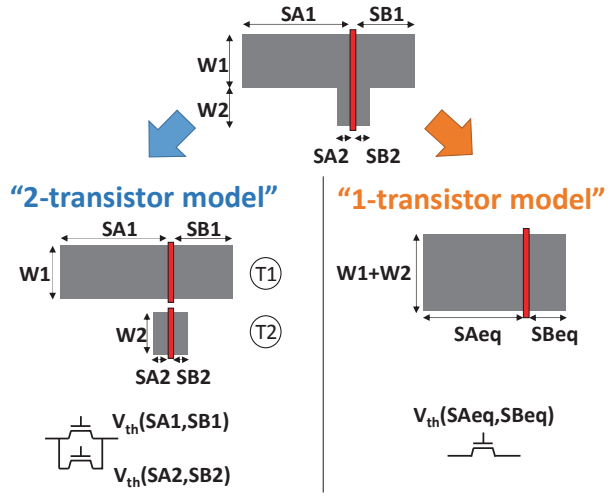



Figure 6. Illustration of the 2 approaches for non-rectangular area modelling, the "2-transistor" and "1-transistor" models.

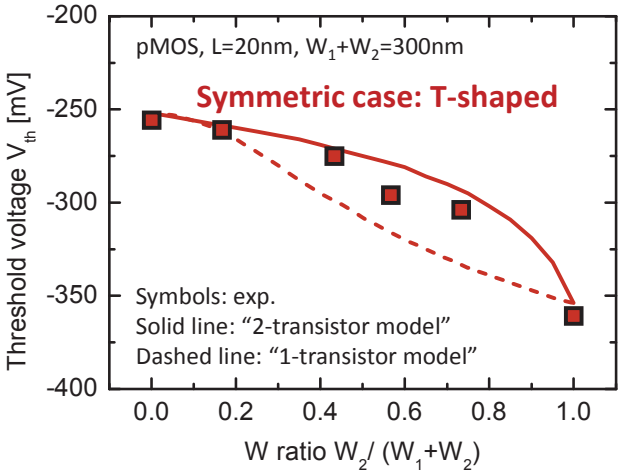



Figure 7. Threshold voltage *vs.* the width ratio of transistor 2 in the case of symmetric non-rectangular active (T-shaped). Experimental data are compared with the "2-transistor" and "1-transistor" models.

The threshold voltage increases with the W ratio for both symmetric (also called T-shaped, Figure 7) and dissymmetric (also called Γ–shaped, Figure 8) non-rectangular active areas. Indeed, the part of the channel with short gate-to-STI distance increases with the W ratio, impacting the threshold voltage of the transistor.

The "2-transistor model" allows reproducing the layout dependence with good accuracy whereas the "1-transistor" model could be a good tradeoff between model predictability and time/complexity of SPICE (Figure 7 and Figure 8).

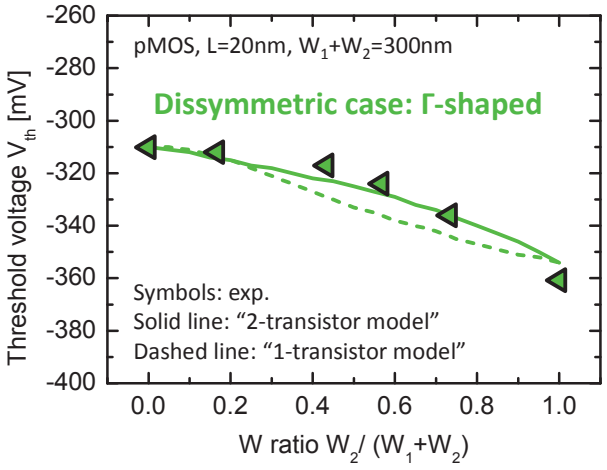



Figure 8. Threshold voltage *vs.* the width ratio of transistor 2 in the case of dissymmetric non-rectangular active (Γ-shaped). Experimental data are compared with "2-transistor" and "1-transistor" models.

## IV. Multifinger transistors

In a design, transistors can be built on a same active area. Especially, multifinger MOSFETs consist of different transistors in parallel and on the same active region, sharing Source and Drain nodes as illustrated in Figure 9. Each elementary transistor is not the same because of different extension lengths. Similar methodology as in §3 is used to model the threshold voltage of multifinger transistor (Eq. 5) and well reproduces experimental data (Figure 10). This figure shows that the transistor closest to the STI impacts the threshold voltage of the whole structure, when compared to the 1-finger transistor reference, located at the middle of the active area (SA=SB) (i.e. Figure 1a and 3).

$$V_{th}(N) = -SS \ln\left[\frac{1}{N}\sum_{i=1}^{N} exp\left(-\frac{V_{th}(SA_i, SB_i)}{SS}\right)\right] \qquad (5)$$

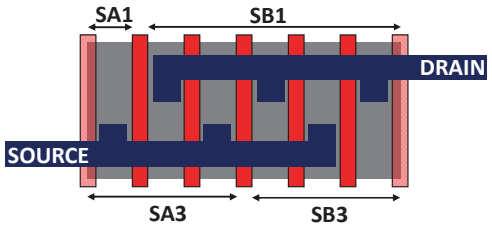



Figure 9. Illustration of multifinger transistors layout built in parallel (in this example, N=5). Each elementary transistor exhibits different extension lengths SA/SB.

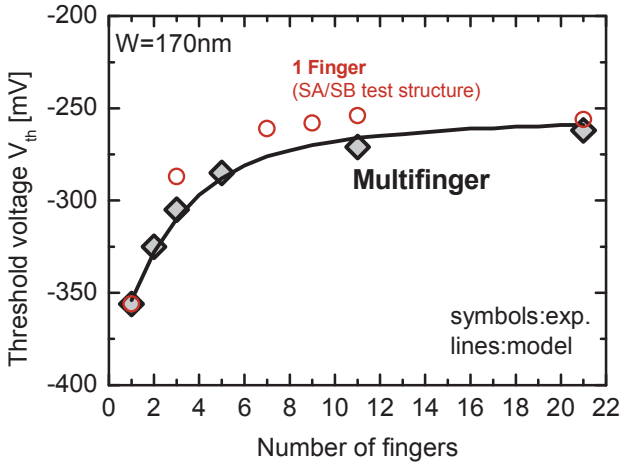



Figure 10. Threshold voltage of multifinger pMOSFETs as a function of the number of fingers. The transistor closest to the STI impacts the *Vth* of the whole structure.

## V. Conclusion

The threshold voltage of SiGe short channel FDSOI pMOSFETs with different layout parameters (active area length, shape and number of fingers) have been deeply characterized and analytically modelled. This analysis confirms the need to properly model the layout effects in order to accurately predict/assess circuit performance.

## Acknowledgements

This work was partly supported by the Catrene Dynamic-ULP, Places2be KETs and Nano2017 projects, through the French ministry of Industry.

## References

[1] O. Weber, E. Josse, F. Andrieu, A. Cros, E. Richard, P. Perreau, E. Baylac et al., "14nm FDSOI Technology for High Speed and Energy Efficient Applications," VLSI tech. Symp., 2014, pp. 16-17.

[2] B. DeSalvo, P. Morin, M. Pala, G. Ghibaudo, O. Rozeau, Q. Liu, A. Pofelski, S. Martini, M. Cassé, et al., "A mobility enhancement strategy for sub-14nm power-efficient FDSOI technologies," IEEE IEDM, p. 7.2.1 - 7.2.4, 2014

[3] K. Cheng, A. Khakifirooz, N. Loubet, S. Luning, T. Nagumo, M. Vinet et al., "High performance extremely thin SOI (ETSOI) hybrid CMOS with Si channel NFET and strained SiGe channel PFET," IEEE IEDM, p. 419, 2012.

[4] F. Andrieu, M. Cassé, E. Baylac, P. Perreau, O. Nier, D. Rideau et al., "Strain and Layout Management in dual Channel (sSOI substrate, SiGe channel) planar FDSOI MOSFETs," Proc. of ESSDERC conference, 2014, pp. 106-109.

[5] T. Poiroux et al., MOS-AK Workshop, Grenoble, 2015

# Drain Current Local Variability from Linear to Saturation Region in 28nm bulk NMOSFETs

T. A. Karatsori[a,b], C. G. Theodorou[a], S. Haendler[c], C. A. Dimitriadis[b] and G. Ghibaudo[a]

a) IMEP-LAHC, Minatec, BP257, 38016 Grenoble, France
b) Department of Physics, Aristotle University of Thessaloniki, Greece
c) STMicroelectronics, BP16, 38921, Crolles, France
*Email: theano.karatsori@imep.grenoble-inp.fr*

***Abstract* — In this work the impact of the source - drain series resistance mismatch on the drain current variability has been investigated for 28nm Bulk MOSFETs. For the first time a mismatch model including the local fluctuations of the threshold voltage, the current gain factor and the source – drain series resistance both in linear and saturation region is presented. Furthermore, it is proved that the influence of source – drain series resistance mismatch is attenuated at the saturation region, due to lower drain current sensitivity to series resistance variation. The experimental results were further verified by Monte Carlo simulation with normally distributed MOSFET parameters.**

***Keywords — mismatch; local variability; threshold voltage; gain factor; SD series resistance; modeling; 28nm BULK; CMOS***

## I. Introduction

Usually process variations are categorized into global and local variations. Concerning the global variations, the device parameters change smoothly all over the wafer. On the other hand, for local variability or mismatch, each transistor is affected differently even from its close neighbor. Mismatch is by nature an uncorrelated stochastic process, which is increasing due to the scaling down of CMOS technology. As a result a crucial issue in MOSFETs and especially in advanced nano-scaled devices is the study of drain current local variability as it affects the performance of analog but also digital circuits.

According to the first mismatch studies, the main sources of drain current, $I_D$ mismatch are the local fluctuations of the threshold voltage, $V_t$ and the current gain factor, $\beta$ [1-2]. The phenomenon of the source – drain (SD) series resistance mismatch and its impact on drain current variability was investigated in a previous work performed on FDSOI devices [3].

In this work, we studied this phenomenon on bulk NMOS transistors processed with 28nm Gate-first technology and extended for the first time the drain current local variability model to the saturation region as well.

## II. Theoretical Background

In [3] the existence of the SD series resistance mismatch and its impact on the drain current variability with regard to the other mismatch components has been verified. Indeed, it has been shown that there is a noticeable difference in the drain current between two paired transistors, whose mismatch, $\Delta I_d/I_d$, is given by,

$$\Delta I_D / I_D = \ln\left( I_{D2} / I_{D1} \right) \tag{1}$$

In the same work, as shown in Eq. 2 an expression including the SD series resistance mismatch impact was proposed for the calculation of the drain current mismatch:

$$\sigma^2\left(\Delta I_D / I_D\right) = \left(\frac{g_m}{I_D}\right)^2 \cdot \sigma^2(\Delta V_t) + (1 - G_D \cdot R_{SD})^2 \cdot \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + G_D^2 \cdot \sigma^2(\Delta R_{SD}) \tag{2}$$

where $\sigma(\Delta V_t)$ $\sigma(\Delta\beta/\beta)$ and $\sigma(\Delta R_{SD})$ are the standard deviations of threshold voltage, gain factor and SD series resistance mismatch and $g_D$ is the channel conductance in linear region.

## III. Results and Discussion

### A. Devices and Experimental Details

The devices measured in this work are bulk n-MOS transistors, issued from 28nm planar CMOS technology with channel width (W) varying from 10 down to 0.08 μm and channel length (L) varying from 5 down to 0.03 μm. The devices are fabricated by ST Microelectronics in France and present also pocket implants. A sample of 65 pairs of identical MOS transistors spaced by the minimum allowed distance and laid out in an identical environment, was necessary for matching measurements. Drain current measurements both at linear ($V_D$ = 30mV) and saturation region ($V_D$ = 1V) were performed with Agilent B1500 Semiconductor Device Analyzer.

### B. Measurement Results

In Figs. 1(a) and (b) the normalized standard deviation of the drain current mismatch, $\sigma(\Delta I_D/I_D)$, is plotted as a function of the gate voltage, $V_G$ for various geometries at the linear and saturation region, respectively. Note that, at low drain voltage, there are clearly cases at strong inversion where an increase of $\sigma(\Delta I_D/I_D)$ with $V_G$ is observed. This increase, which is not observed in all geometries, was attributed to SD series resistance variability in FDSOI devices [3]. Therefore, it appears that this phenomenon also exists in bulk devices. On the other hand, we observe that, for the same geometries, no such behavior is clearly observed at saturation region (see Fig.

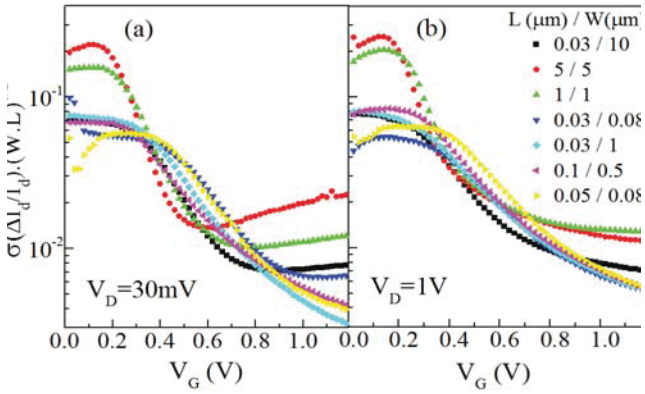



Fig. 1. Normalized standard deviation of the drain current mismatch versus gate voltage, $V_G$ for different geometries in linear (a) and saturation (b) region.

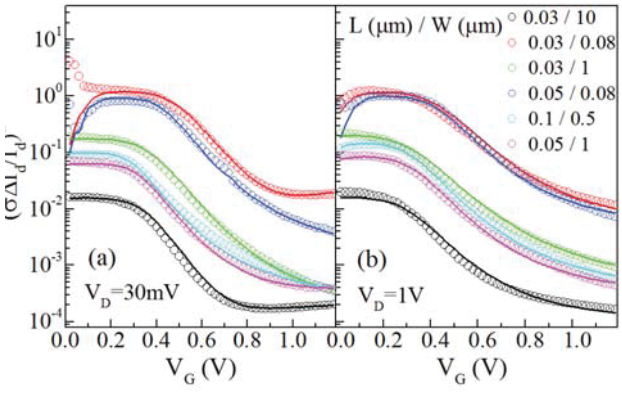



Fig. 2. Experimental results (symbols) of $\sigma^2(\Delta I_D/I_D)$ versus gate voltage, $V_G$ for small and large area devices in linear (a) and saturation (b) region and Model (lines).

1(b)). In order to interpret these results, we extended the model described in [3] so that the saturation region can be included in the calculation of the drain current mismatch (see Eq. 3).

$$\sigma^2\left(\frac{\Delta I_D}{I_D}\right)=\left(\frac{g_m}{I_D}\right)^2\cdot\sigma^2(\Delta V_t)+\left(\left(1-(g_m/2+g_d)\cdot R_{SD}\right)^2\right)\cdot\sigma^2\left(\frac{\Delta\beta}{\beta}\right) \quad (3)$$
$$+(g_m/2+g_d)^2\cdot\sigma^2(\Delta R_{SD})$$

As a result, we used Eq. 3 to fit the experimental data with 3 fitting parameters, the threshold voltage mismatch, $\sigma(\Delta V_t)$, the current gain factor mismatch, $\sigma(\Delta\beta/\beta)$ and the $R_{SD}$ mismatch, $\sigma(\Delta R_{SD})$, in all operation regions. The value of $R_{SD}$ was extracted using the Y-Function method using several gate lengths [4]. The results are displayed in Fig. 2(a). Concerning the saturation region, we extracted nearly the same values for $\sigma(\Delta V_t)$ and $\sigma(\Delta\beta/\beta)$, consistently with those of the linear region. As it is shown in Fig. 2(b) we achieved a good agreement between the experiment and the model. This indicates that the influence of $\Delta R_{SD}$ can be significantly attenuated in saturation region. This feature can be understood through the last term of Eq. 3, which is related to the drain current sensitivity to $\Delta R_{SD}$ and which indicates that $I_D$ is at least twice less sensitive to $R_{SD}$ in saturation, where $g_D$=0. This observation is confirmed in Figs. 3 (a) and (b) where the individual matching parameter $iA_{\Delta Vg}(V_G)$ (Eq. 4) is presented for various geometries at the linear and saturation region, respectively.

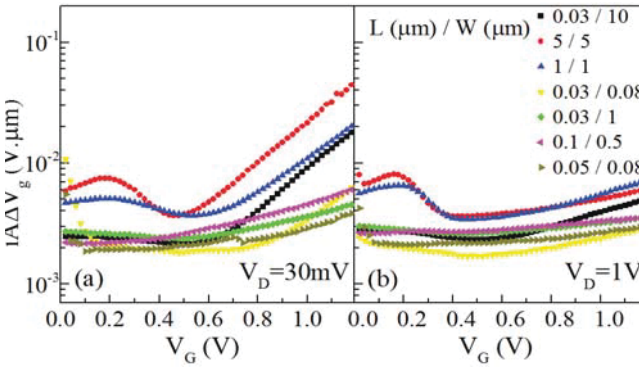



Fig. 3. Individual matching parameter $iA_{\Delta Vg}$ versus gate voltage, $V_G$ extracted by experimental data in linear (a) and saturation region (b) for different geometries.

$$iA_{\Delta Vg}=\left[\sigma\left(\frac{\Delta I_D}{I_D}\right)\Big/\left(\frac{g_m}{I_D}\right)\right]\cdot\sqrt{W\cdot L} \quad (4)$$

The plateau at low gate voltages nearly corresponds to the individual matching parameter $iA_{\Delta Vt}$ (Eq. 5).

$$iA_{\Delta Vt}=\sigma(\Delta V_t)\cdot\sqrt{W\cdot L} \quad (5)$$

As we can see in more detail in Fig. 4, $\sigma(\Delta V_t)$ has almost the same value for both linear and saturation region. The difference observed between the two regions at high $V_G$ values is because of the $\sigma\Delta R_{SD}$ difference, while the slight increase of $iA_{\Delta Vg}$ at strong inversion is due to $\sigma(\Delta\beta/\beta)$. From Fig.4 it is

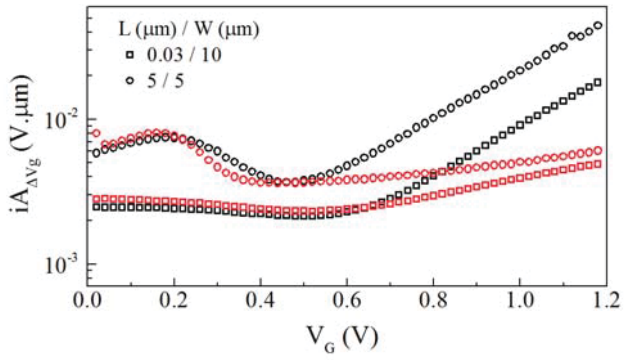



Fig. 4. Individual matching parameter, $iA_{\Delta Vg}$ versus gate voltage, $V_G$ in linear (black symbols) and saturation region (red symbols).

also clear that the parameter $iA_{\Delta Vg}$ is smaller at $V_D$=1V since there is less $\Delta R_{SD}$ impact in saturation (Eq. 3).

Figs. 5 and 6 present the individual matching parameters $iA_{\Delta Vt}$ and $iA_{\Delta\beta/\beta}$ respectively, as a function of the gate length (Eqs 5 & 6).

$$iA_{\Delta\beta/\beta}=\sigma(\Delta\beta/\beta)\cdot\sqrt{W\cdot L} \quad (6)$$

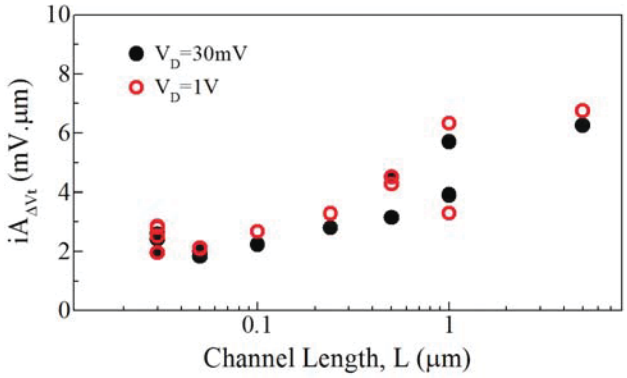



Fig. 5. $iA_{\Delta Vt}$ versus channel length, L in linear (black symbols) and saturation region (red symbols) for 28nm BULK nMOSFETs.

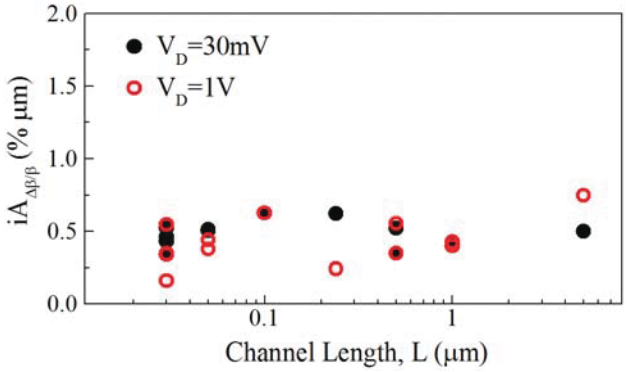



Fig. 6. $iA_{\Delta\beta/\beta}$ versus channel length, L in linear (black symbols) and saturation region (red symbols) for 28nm BULK nMOSFETs.

The values corresponding to the $iA_{\Delta Vt}$ parameter are ranging between 2 and 6.5 mV·µm, in agreement with [5] and they increase slightly with the gate length. Moreover, $iA_{\Delta\beta/\beta}$ ranges from 0.4 to 0.6 %.µm verifying that our fitting with the gain factor mismatch was correctly done. Last but not least, the standard deviation of the SD series resistance mismatch versus the channel width is presented in Fig. 7. As can be seen, the $R_{SD}$ and the $\sigma(\Delta R_{SD})$ follow the same trend and more specifically their values decrease as the channel width increases. Furthermore, a dependence on the gate length is observed at fixed width. Finally, it was found that the normalized series resistance local variability, $\sigma(\Delta R_{SD})/R_{SD}$, is around 5-15%, which is similar to FDSOI technologies [3].

### *C. Simulation Results*

To further verify the findings presented above, we performed Monte Carlo simulations. Using the MOSFET compact model based on Lambert W function [6] the variability curves of the devices were reproduced. Based on the experimentally extracted matching parameters, the MOSFET parameters were randomly generated by a Monte Carlo process using a normal distribution.

Fig. 8 shows that the smaller impact of $\Delta R_{SD}$ occurs at the saturation region, thus verifying the experimental results behavior.

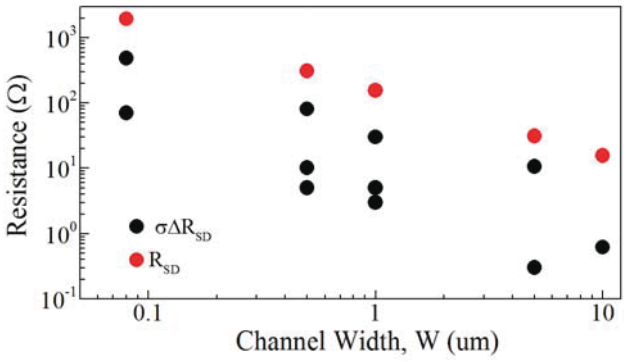



Fig. 7. Source – Drain, SD series resistance (red symbols) and its mismatch (black symbols) versus channel width, W for 28nm BULK nMOSFETs.

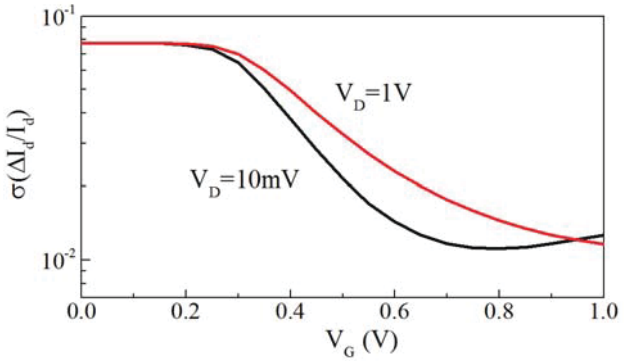



Fig. 8. Simulation results of $\sigma(\Delta I_D/I_D)$ versus gate voltage, $V_G$ for nMOS devices with channel length L=1um and channel width W=1um.

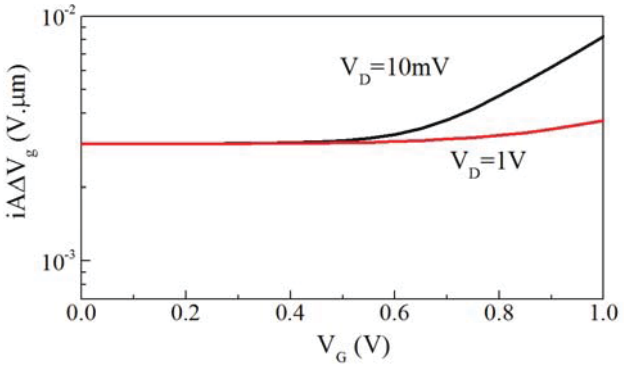



Fig. 9. Simulation results of parameter $iA_{\Delta Vg}$ versus gate voltage, $V_G$ for nMOS with channel length L=1um and channel width W=1um.

This finding is also supported by the simulated individual matching parameter, $iA\Delta V_g$ which is smaller at the saturation region (see Fig. 9).

## IV. Conclusion

The impact of the SD series resistance mismatch on the drain current variability has been investigated for 28nm Bulk MOSFETs. A mismatch model that takes into consideration the $R_{SD}$ local variability was developed and used to extract all mismatch parameters, including $\sigma(\Delta V_t)$, $\sigma(\Delta\beta/\beta)$ and $\sigma(\Delta R_{SD})$, in linear and saturation regions. This phenomenon was proved

to be reduced in saturation region for high drain voltage values, due to lower drain current sensitivity to series resistance variation. Finally, as in FDSOI devices, the SD series resistance mismatch, $\sigma(\Delta R_{SD})$, was found to scale down with gate width as $R_{SD}$, and the normalized series resistance local variability parameter $\sigma(\Delta R_{SD})/R_{SD}$ takes similar values, demonstrating very good access resistance control in bulk technology.

## ACKNOWLEDGMENT

This work has been partly supported by the ENIAC places2be and ECSEL Waytogo Fast projects.

## REFERENCES

[1] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," IEEE J. Solid-State Circuits, vol. 24, no. 5, pp. 1433-1439, October 1989.

[2] J. A. Croon, M. Rosmeulen, S. Decoutere, and W. Sansen, "An easy-to-use mismatch model for the MOS transistor," IEEE J. Solid State Circuits, vol. 37, no. 8, pp. 1056-1064, August 2002.

[3] E. G. Ioannidis, C. G. Theodorou, S. Haendler, E. Josse, C. A. Dimitriadis, and G. Ghibaudo, "Impact of Source-Drain Series Resistance on Drain Current Mismatch in Advanced Fully Depleted SOI n-MOSFETs," IEEE Electron Device Letters, vol. 36, no. 5, pp. 433-435 May 2015.

[4] G. Ghibaudo, "New method for the extraction of MOSFET parameters," Electronics Letters, vol. 24, no. 9, pp. 543-545, April 1988.

[5] L. Rahhal, A. Bajolet, J.-P. Manceau, J. Rosa, S. Ricq, S. Lassere, and G. Ghibaudo "Mismatch Trends in 20nm Gate-last bulk CMOS technology," in Proc. ULIS International Conference, April 2014, pp. 133-136.

[6] T. A. Karatsori, C. G. Theodorou, E. G. Ioannidis, S. Haendler, E. Josse, C. A. Dimitriadis, and G. Ghibaudo, "Full gate voltage range Lambert-function based methodology for FDSOI MOSFET parameter extraction," Solid State Electronics, vol. 111, pp. 123-128, September 2015.

# Investigation of BSIM4 Parameter Extraction and Characterization for Multi Gate Oxide-Dual Work Function (MGO-DWF)-MOSFET

Chika Tanaka, Kazuya Matsuzawa
Toshiba Corporation
Advanced LSI Technology Laboratory,
Corporate R&D Center
Kawasaki, Japan
Email: chika.tanaka@toshiba.co.jp

Toshitaka Miyata, Kanna Adachi,
and Akira Hokazono
Toshiba Corporation
Center for semiconductor R&D,
Semiconductor & Storage Products Company
Kawasaki, Japan

***Abstract*— We investigate the BSIM4 parameter extraction procedure for Multi Gate Oxide-Dual Work Function MOSFET by using the SPICE modeling tool. Process parameters were carefully derived from the measured and simulated data. Parameter sets for total channel length down to 130nm were obtained, as long as process parameters are well defined. Larger transconductance, smaller drain conductance, and parasitic capacitance in the drain side can be observed on the extracted parameters. The extracted parameters will be a useful tool for characterizing the circuit performance of Multi Gate Oxide-Dual Work Function MOSFET. Furthermore, our extraction procedure is applicable to extract the BSIM4 model parameters for Multi Gate Oxide-Dual Work Function MOSFET as well as other structures and materials.**

***Keywords—dual work function-MOSFET; multi gate oxide; parameter extraction; BSIM4; SPICE model***

## I. INTRODUCTION

Dual Work Function (DWF)-FETs have been proposed [1,2,3] for RF/analog circuit applications, which show a larger transconductance ($g_m$) and a smaller drain conductance ($g_d$) because of work function (WF) difference in the gate electrode.

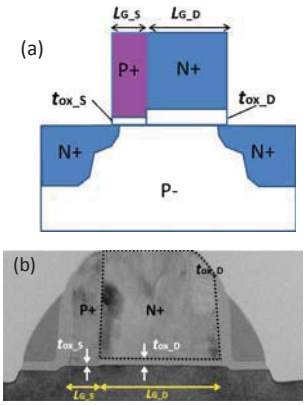



**Fig.1** (a) Schematic device structure and (b) cross sectional TEM image of MGO-DWF-FET.

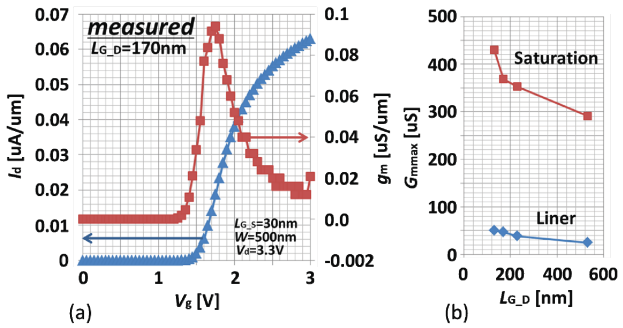



**Fig.2** (a) Measured $I_d$-$V_g$ and $g_m$-$V_g$ characteristics of n-channel MGO-DWF-FET with $L_{G\_D}$=170nm, $L_{G\_S}$=30nm and W=500nm. $V_d$=3.3V. (b) Extracted $L_{G\_D}$ dependence on $G_{mmax}$ from measurement data with $L_{G\_S}$=30nm and W=500nm. Higher $g_m$ was obtained for shorter $L_{G\_D}$ devices.

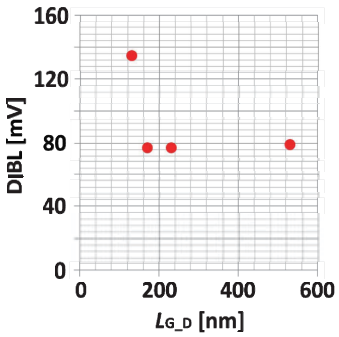



**Fig.3** Measured $L_{G\_D}$ dependence on DIBL. $L_{G\_D}$=170nm, $L_{G\_S}$=30nm, $W$=500nm. SCE immunity was guaranteed to the channel length of 200nm.

We fabricated Multi Gate Oxide (MGO)-DWF-FET with LV-MOSFET in the source side region and HV-MOSFET in the drain side region and enhancement of $F_{MAX}$ was observed in the scaled devices [4]. As for SPICE modeling, conventional MOSFET models cannot be used straightforwardly for MGO-DWF-FET due to the asymmetric source/drain (S/D) structures. In this study, we investigated BSIM4 based DC and

capacitance model parameter extraction procedure for MGO-DWF-FET with different geometries on the basis of the measurement data.

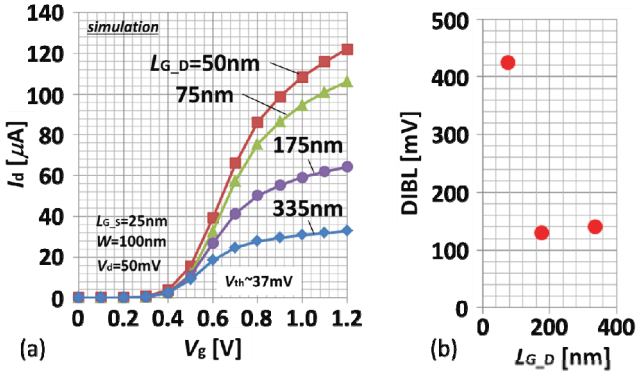



**Fig.4** Simulated (a) $I_d$-$V_g$ at liner region and (b) DIBL characteristics with $W$=100nm, $L_{G\_S}$=25nm. In this simulation, gate work function difference was a constant condition for all devices.

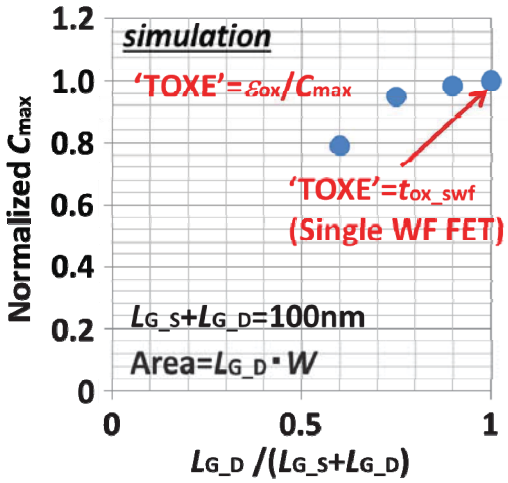



**Fig.5** Normalized $C_{max}$ extracted from simulated $CV$ curves. The device with the data for $L_{G\_D}/(L_{G\_S}+L_{G\_D})$=1 shows single work function MOSFET. $C_{max}$ has $L_{G\_D}$ dependence.

## II. Device Structure and Characteristics

We fabricated MGO-DWF-FET by using Toshiba's 65nm CMOS technology. Fig. 1 shows the schematic device structure and cross sectional TEM image. Gate oxide thickness of source side gate ($t_{ox\_S}$) was thinner than that of drain side gate ($t_{ox\_D}$), and asymmetric S/D extension was formed. Fig. 2(a) shows the measured $I_d$-$V_g$ and $g_m$-$V_g$ curves of $n$-channel MGO-DWF-FET with drain side gate length ($L_{G\_D}$) of 170nm and source side gate length ($L_{G\_S}$) of 30nm. Higher $g_m$ was obtained for shorter $L_{G\_D}$ devices, as shown in Fig. 2 (b). Fig. 3 shows $L_{G\_D}$ dependence on drain induced barrier lowering (DIBL). Short channel effect (SCE) immunity was guaranteed to the channel length of 200nm, which is corresponds to the results obtained from in-house 2D device simulation of Fig. 4.

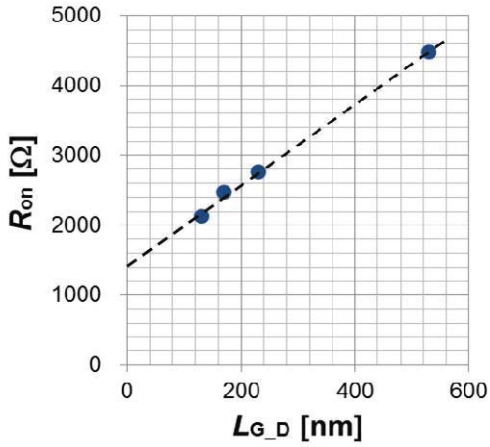



**Fig.6** $R_{sd}$ was determined from measured $R_{on}$-$L_{G\_D}$ plot with $W$=500nm, $L_{G\_S}$=30nm. $R_{sd}$ can be obtained from the y-axis intercept of the observed straight line.

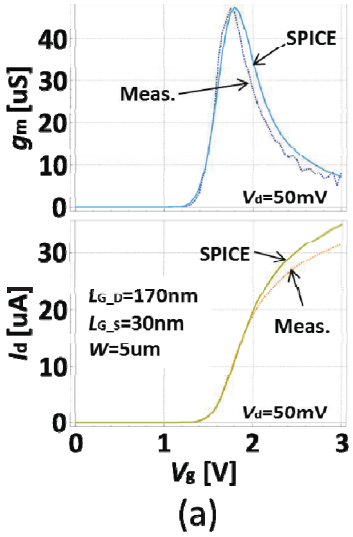



**Fig.7** (a) Typical optimization results for $g_m$-$V_g$ and $I_d$-$V_g$ curves with $V_d$=50mV (liner).

## III. DC Parameter Extraction

We applied BSIM4.6.0 [5] in order to extract the model parameter from the measurement data of MGO-DWF-FET. SPICE modeling tool, UTMOST IV [6], was used. The targeted device geometries for parameter extraction are ($L_{G\_D}$, $L_{G\_S}$) = (530, 30), (230, 30), (170, 30), (130, 30) [nm] and $W$=500nm. P+ poly/$SiO_2$ gate stack with $t_{ox\_S}$=2.0nm and n+ poly/$SiO_2$ gate stack with $t_{ox\_D}$=7.4nm were fabricated. Before the parameter extraction, process parameter of 'L' (channel length) and 'TOXE' (gate oxide thickness) were carefully derived. Although the total channel length is a sum of $L_{G\_D}$ and $L_{G\_S}$, 'L' was set to be $L_{G\_D}$ in this study. 'TOXE' was extracted from the maximum capacitance ($C_{max}$) with gate area defined by $L_{G\_D}\cdot W$. As shown in Fig.5, although the total channel length is a constant value of $L_{G\_S}$+$L_{G\_D}$=100nm for all

devices, $C_{max}$ has the $L_{G\_D}$ dependence because inversion area under n+ gate was determined by $L_{G\_D} \cdot W$.

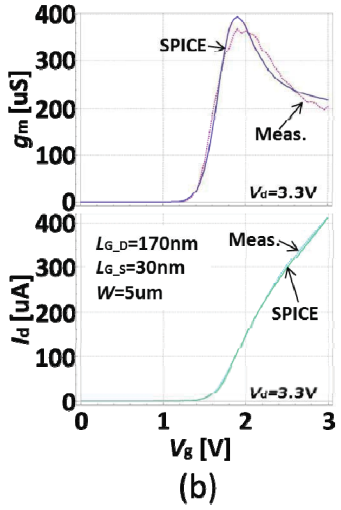



**Fig.7** (b) Typical optimization results for $g_m$-$V_g$ and $I_d$-$V_g$ curves with $V_d$=3.3V (saturation).

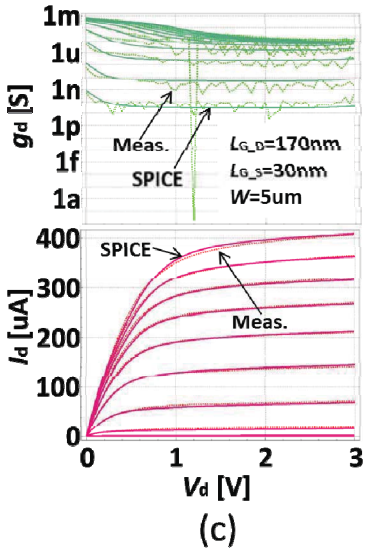



**Fig.7** (c) Typical optimization results for $g_d$-$V_g$ and $I_d$-$V_d$ curves. SPICE simulation was performed by using extracted patrameter. Good fitting with maximum error < 5% for targeted voltage range was achieved for *n*-channel MGO-DWF-FET.

Therefore, since 'TOXE' has the $L_{G\_D}$ dependence, multiple DC parameter sets for various $L_{G\_D}$ down to 130nm were obtained for *n*-type MGO-DWF-FET. In $I_d$-$V_g$ optimization procedure, initial value of 'VTH0' was obtained from the measurement data of $L_{G\_D}$=500nm. In $I_d$-$V_d$ optimization procedure, parasitic resistance ($R_{sd}$) was simply determined from $R_{on}$-$L_{G\_D}$ plot in the long channel regime, as shown in Fig. 6. $R_{sd}$ can be obtained from the y-axis intercept of the observed straight line. When 'L', 'TOXE', 'VTH0' and

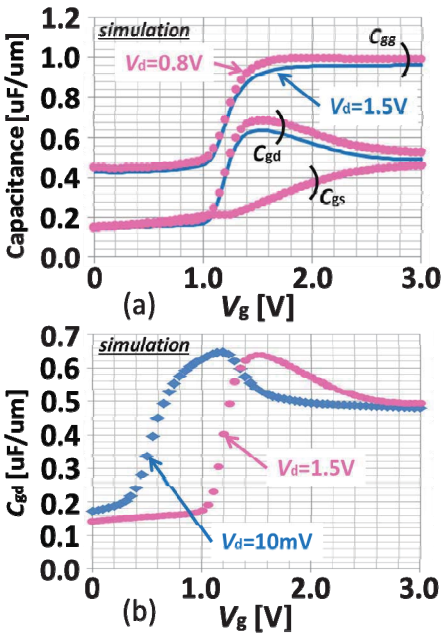



**Fig.8:** (a) Simulated gate capacitance ($C_{gg}$), gate-to-drain capacitance ($C_{gd}$) and gate-to-source capacitance ($C_{gs}$) curves with high $V_d$ and (b) $V_d$ dependence on $C_{gd}$. Unlike MOSFET, only $C_{gd}$ was increased when $V_g$ is applied.

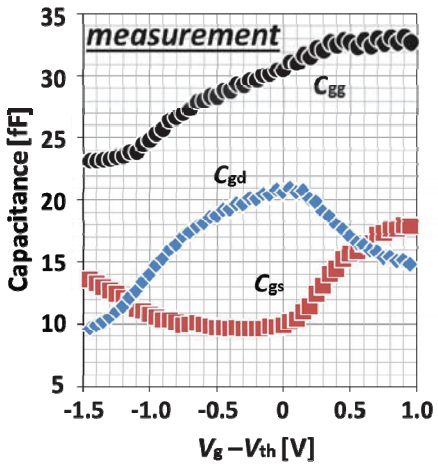



**Fig.9:** Measured *CV* characteristics of capacitor TEG for MGO-DWF-FET by using high frequency measurement [4].

$R_{sd}$ were determined, local optimization strategies and rubberband method were used for parameter extraction. Fig. 7 shows the typical results of the measured and simulated $g_m$-$V_g$, $I_d$-$V_g$ and $I_d$-$V_d$ curves. The behavior in gm curves and smaller $g_d$ characteristics were optimized to match the characteristics of MGO-DWF-FET. Good fitting with maximum error < 5% for the targeted voltage range was achieved for *n*-channel MGO-DWF-FET with sub-200nm gate length.

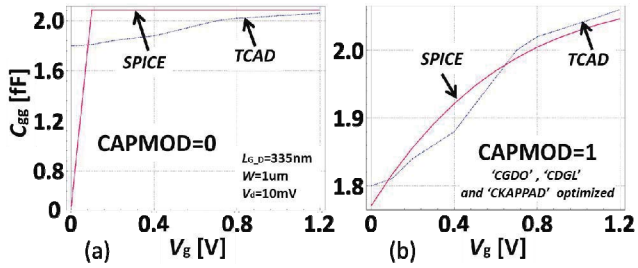



**Fig.10** TCAD and SPICE simulation results for $C_{gg}$ characteristics. (a) "CAPMOD=0" and (b) "CAPMOD=1". 'CGDO', 'CDGL' and 'CKAPPAD' were useful parameter to optimize the *CV* characteristics. When "CAPMOD=1", optimized *CV* was obtained.

## IV. Parasitic Capacitance Characterization

Figure 8 shows simulated capacitance-voltage (*CV*) characteristics of MGO-DWF-FET. Since a capacitance coupling between the gate electrode and the drain side inversion layer, which indicates an increase of parasitic capacitance ($C_{para}$) in the drain side, was observed when $V_g$ is applied, a total gate capacitance was observed before the transistor is turning on. This trend corresponds to the result obtained from measurement data (Fig. 9). $C_{gd}$-$V_g$ characteristics also have $V_d$ dependence, as shown in Fig.8 (b). Therefore, we used a bias-dependent $C_{para}$ model of BSIM4. When 'CAPMOD=1' had been selected, it was found that 'CGDO', 'CDGL' and 'CKAPPAD' were useful parameter to optimize the *CV* characteristics (Fig.10). In particular, 'CDGL' and 'CKAPPAD', which have bias-dependent in order to treat LDD structure for conventional MOSFET, show the $C_{para}$ reduction at the low-$V_g$ and $V_d$ region.

## V. Conclusion

SPICE model parameters of BSIM4 were successfully extracted for MGO-DWF-FET by using UTMOST IV. 'L' was set to be $L_{G\_D}$ and 'TOXE' were carefully derived from the maximum capacitance with $L_{G\_D}$ dependence. Parameter sets for $L_{G\_D}$ down to 130nm were obtained, as long as process parameters are well defined. Larger $g_m$, smaller $g_d$, and $C_{para}$ in the drain side can be observed on the extracted parameter. The extracted parameters will be a useful tool for characterizing the circuit performance of MGO-DWF-FET. Furthermore, our extraction procedure is applicable to extract the BSIM4 model parameters for MGO-DWF-FET as well as other structures (e.g. SOI, double gate) and materials (e.g. high-k) for MGO-DWF-FET.

## References

[1] W. Long, Ou, H., Kuo, J.-M., Chin, K.K., "Dual-material gate (DMG) field effect transistor", IEEE Trans. Electron Devices, vol. 46, issue 5, pp.865-870, 1999.

[2] T. Miyata, S. Kawanaka, A. Hokazono, T. Ohguro, and Y. Toyoshima, "Scaling Strategy for Low Power RF Applications with Multi Gate Oxide Dual Work function (DWF) MOSFETs Utilizing Self Aligned Integration Scheme", Symposium on VLSI Technology Digest of Technical Papers, pp.T144-145, 2013.

[3] K.-Y. Na, K.-J. Baek, Y.-S. Kim, "N-Channel Dual-Workfunction-Gate MOSFET for Analog Circuit Applications", IEEE Trans. Electron Devices, vol. 59, issue12, pp.3273-3279, 2012.

[4] T. Miyata, H. Tanaka, K. Kagimoto, M. Kamiyashiki, M. Kamimura, A. Hidaka, M. Goto, K. Adachi, A. Hokazono, T. Ohguro, K. Nagaoka, Y. Watanabe, S. Hirooka, Y. Ito, S, Kawanaka, K. Ishimaru, "150 GHz $F_{MAX}$ with High Drain Breakdown Voltage Immunity by Multi Gate Oxide Dual Work-Function (MGO-DWF)-MOSFET", IEDM Technical Digest, pp.656-659, 2015.

[5] BSIM, http://www- device.eecs.berkeley.edu/bsim/.

[6] Silvaco, http://www.silvaco.com/.

# Confinement Orientation Effects in S/D tunneling

C. Medina-Bailon*†‡, C. Sampedro*†, F. Gamiz*†, A. Godoy*† and L. Donetti*†
* Nanoelectronics Research Group, Universidad de Granada, 18071 Granada, Spain.
† CITIC, Universidad de Granada, 18071 Granada, Spain.
‡e-mail: cmedba@ugr.es

***Abstract*—The most extensive research of scaled electronic devices involves the inclusion of quantum effects in the transport direction as transistor dimensions approach to nanometer scales. Moreover, it is necessary to study how these mechanisms affect different transistor architectures to determine which one can be the better candidate to implement future nodes. This work implements Source-to-Drain Tunneling mechanism (S/D tunneling) in a Multi-Subband Ensemble Monte Carlo (MS-EMC) simulator showing the modification in the distribution of the electrons in the subbands, and, consequently, in the potential profile due to different confinement direction between DGSOIs and FinFETs.**

## I. Introduction

The study of alternative technical approaches for electronic devices is necessary to fulfill the requirements of power consumption, delay time and scalability demanded by ITRS [1]. On the one hand, the inclusion of quantum effects in the transport description is mandatory when the dimensions of the electronic devices are reduced. In particular, Source-to-Drain tunneling (S/D tunneling) allows electrons to go from the source to the drain through the potential barrier. It has been presented as a scaling limit effect in ballistic non-equilibrium Green's Function (NEGF) approach [2]. This phenomenon is of special interest when operation regime is near-threshold because leakage current increases and $V_{th}$ decreases [3]. On the other hand, new transistor architectures based on multiple gates [4] are considered to replace standard technology and to extend the end of the Roadmap. If we consider a double gate device, these gates can be oriented horizontally, Double-Gate Silicon-On-Insulator (DGSOI), or vertically, FinFET. This work presents a meticulous comparison between DGSOI and FinFET by means of a Multi-Subband Ensemble Monte Carlo (MS-EMC) simulator when S/D tunneling mechanism is taken into account. It will be shown the influence of the orientation on the S/D tunneling and, consequently, on the device characteristics.

## II. Simulation Set-up

The model presented in this work is included in a MS-EMC simulator which is based on the mode-space approach of quantum transport [5]. The device structure is divided into slices along the confinement direction where the 1D Schrödinger equation is solved, whereas the 2D Bolzmann Transport Equation is solved in the transport plane as showed in Figure 1. Both equations are coupled with the 2D Poisson Equation to keep the self-consistency of the simulator. This simulator has already demonstrated its capabilities studying different advanced nanodevices [6]–[9] where scattering mechanisms and quantum effects are taken into account in the simulations with a reasonable computational effort.

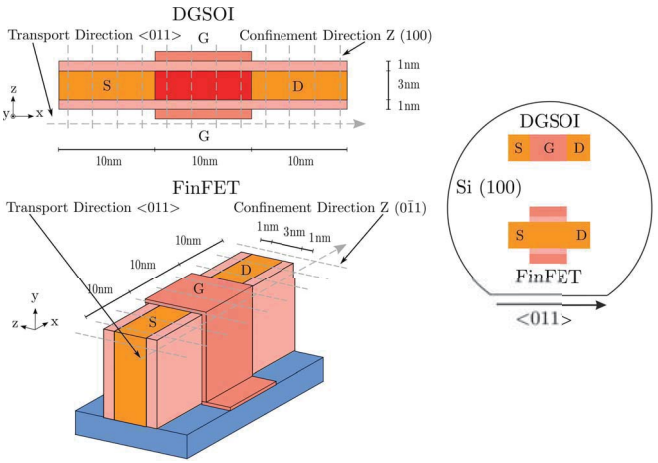



Fig. 1. DGSOI and FinFET structures analyzed in this work. 1D Schrödinger equation is solved for each grid point in the transport direction and BTE is solved by the MC method in the transport plane.

In this work, the performance of DGSOI and FinFET devices were analyzed when S/D tunneling is included in order to determine the impact of such phenomenon. The considered orientation of these devices on standard wafers changes between (100) for planar DGSOI and (0$\bar{1}$1) for vertical FinFET as the confinement direction, whereas the transport direction remains constant <011> as depicted in Figure 1. The differences in the confinement direction modify the distribution of the electrons in the subbands, and, consequently, the potential profile. Also, the carrier transport effective mass is modified [10]. Table I summarizes the masses of each device and Table II shows their numerical values. Taking into account that in silicon, $m_l = 0.916m_0$ and $m_t = 0.198m_0$ are the longitudinal and traverse effective masses, respectively, $m_0$ is the electron free-mass, $m_x$ is the transport mass, $m_z$ is the confinement mass, and $\Delta_2$ and $\Delta_4$ represent the degeneration factors of each valley $\Delta$. In addition, the lower energy subband changes from $\Delta_2$ in DGSOI to $\Delta_4$ in FinFET.

These devices have been parametrized for gate length ranging from 5 nm to 20 nm. The rest of the technological parameters remains constant, channel thickness $T_{Si}$= 3 nm, gate oxide with Equivalent Oxide Thickness EOT= 1 nm and

ISBN 978-1-4673-8608-1  IEEE Catalog number CFP1649D-USB

| Device | Valley | $m_x$ | $m_y$ | $m_z$ |
|---|---|---|---|---|
| DGSOI | $\Delta_2$ | $m_t$ | $m_t$ | $m_l$ |
| (100)<011> | $\Delta_4$ | $\frac{2m_l m_t}{m_l+m_t}$ | $\frac{m_l+m_t}{2}$ | $m_t$ |
| FinFET | $\Delta_2$ | $m_t$ | $m_l$ | $m_t$ |
| $(0\bar{1}1)$<011> | $\Delta_4$ | $\frac{m_l+m_t}{2}$ | $m_t$ | $\frac{2m_l m_t}{m_l+m_t}$ |

TABLE I
EFFECTIVE MASS IN SILICON FOR DGSOI AND FINFET DEVICES STUDIED IN THIS WORK WHERE $m_x$ IS THE TRANSPORT MASS AND $m_z$ IS THE CONFINEMENT MASS.

| Device | Valley | $m_x$ | $m_y$ | $m_z$ |
|---|---|---|---|---|
| DGSOI | $\Delta_2$ | 0.198 | 0.198 | 0.916 |
| (100)<011> | $\Delta_4$ | 0.326 | 0.557 | 0.198 |
| FinFET | $\Delta_2$ | 0.198 | 0.916 | 0.198 |
| $(0\bar{1}1)$<011> | $\Delta_4$ | 0.557 | 0.198 | 0.326 |

TABLE II
NUMERICAL VALUES OF EFFECTIVE MASS IN SILICON FOR DGSOI AND FINFET DEVICES STUDIED IN THIS WORK WHERE $m_x$ IS THE TRANSPORT MASS AND $m_z$ IS THE CONFINEMENT MASS.

work function of 4.385 eV. It should be highlighted that the FinFET is a 3D structure whereas our MS-EMC simulator make use of a 2D description. However, it was demonstrated that FinFETs with a big enough aspect ratio show similar behavior in all transport regimes when 2DMS-EMC and other 3D codes are used [11].

The fundamentals of the free-flight technique of an electron used in Monte Carlo algorithms calculate the positions of each electron after a flight. In a semiclassical approximation if the total energy of this electron was lower than the potential barrier at this position, the electron would rebound at the potential barrier. When S/D tunneling was taken into account, the electron would rebound at the potential barrier or would go from the source to the drain through it. To determine whether the electron is going to suffer this quantum effect or not, firstly, it is necessary to calculate the probability of tunneling of the electron through the barrier at a specific energy $T_{dt}$ using the WKB approximation [12]:

$$T_{dt}(E) = \exp\left\{-\frac{2}{\hbar}\int_a^b \sqrt{2m^*_{tr}(E_i(x)-E)}\,\mathrm{d}x\right\} \quad (1)$$

where $a$ and $b$ are the starting and ending points, $E$ and $m^*_{tr}$ are the energy and transport effective mass of the electron, respectively, and $E_i(x)$ the energy of the *i-th* subband. Secondly, a rejection technique is used to determinate whether the particle will tunnel or not. A uniform distributed random number $r_{dt}$ is generated and compared to $T_{dt}$. On the one hand, if $r_{dt} > T_{dt}$, the electron will turn back with $v_x = -v_x$. On the other hand, if $rdt \leq Tdt$, the electron will go through the barrier. The motion inside the barrier obeys Newton mechanics considering an inverted potential profile and ballistic transport. This classical trajectory could be found by the following steps [3]. Firstly, an imaginary particle is placed at the starting point $a$ with zero kinetic energy. Then, it accelerates in this system according to Newton's second law of motion:

$$\vec{a} = \frac{q\xi}{m^*_{tr}} \quad (2)$$

where $\xi$ is the electric field. Lastly, it reaches the ending point $b$. Thereafter, the electron continues flying into the device with the same transport properties. This simulation approach is an extension for non-local band-to-band tunneling algorithm [13].

## III. RESULTS AND DISCUSSION

A set of simulations including lineal and saturation bias condition has been performed to determine the importance of S/D tunneling on each of the devices. The modifications caused by the difference in the confinement directions in the energy profile of the lower energy subbands is shown in Figure 2 and in the carrier transport effective mass corresponds to $m_x$ in Table II. As we can extract from Equation 1, the higher exponential the smaller $T_{dt}$ is. Assuming similar energy profile (Figure 2), which means similar tunneling length at a specific starting point $a$, the higher $m^*_{tr}$ for the FinFET orientation reduces the effectiveness of this phenomenon compared to DGSOI orientation.

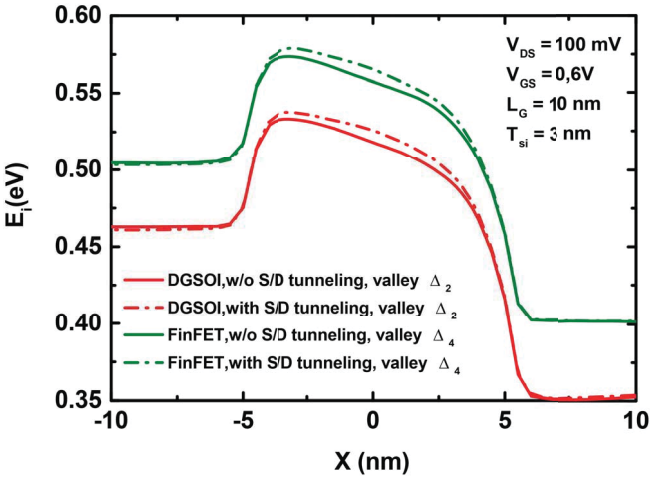



Fig. 2. Energy profile of the lower energy subband in the 10nm device for DGSOI (valley $\Delta_2$) and FinFET (valley $\Delta_4$) with and w/o S/D tunneling with $V_{GS} = 0.6V$ and $V_{DS} = 100mV$.

As a result, higher $T_{dt}$ implies higher probability of an electron suffering S/D tunneling. For this reason, the number of particles affected by S/D tunneling is higher for the DGSOI

than for the FinFET as depicted in Figure 3. The same effect is also shown in the percentage of electrons affected by S/D tunneling near the potential barrier, which is lower for FinFET (Figure 4 top) than for DGSOI (Figure 4 bottom). In addition, there is a maximum of this percentage for the FinFET due to a reduced height of the potential barrier. Consequently, the number of electrons near the potential barrier with lower energy is also reduced. By way of contrast, this maximum percentage also appears in DGSOI devices but it is shifted to higher gate voltages (not shown).

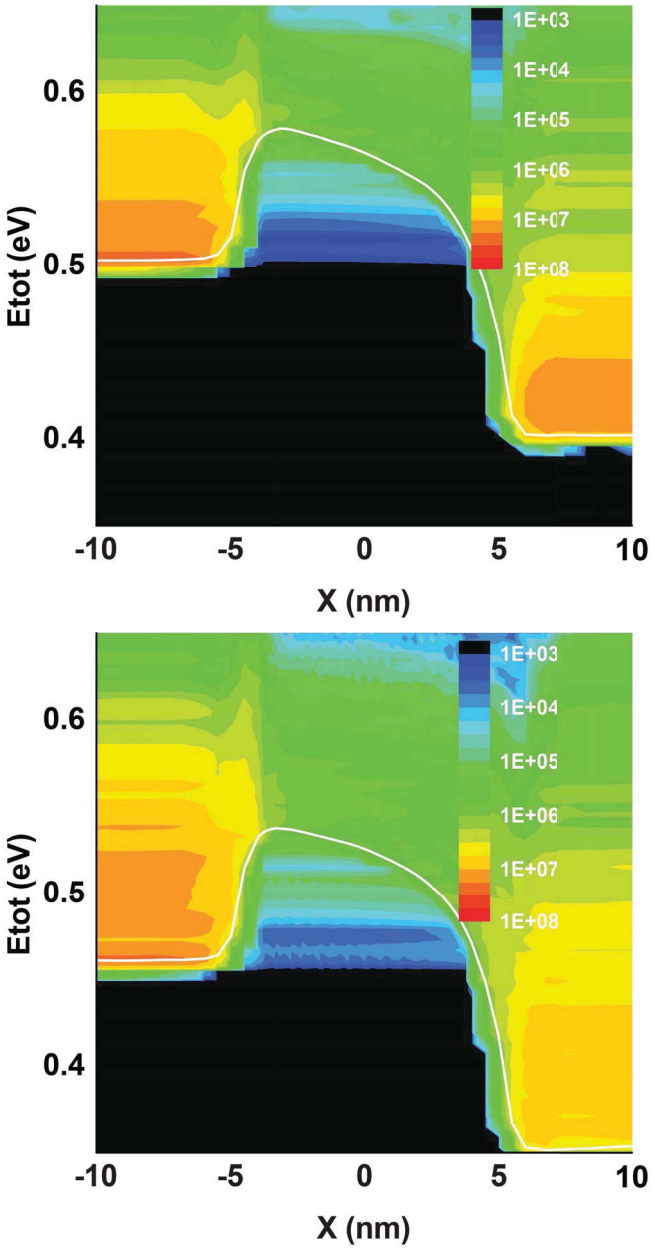



Fig. 3. Electron distribution in the lower energy subband as a function of total energy in the 10nm device including S/D tunneling for FinFET (top) and DGSOI (bottom) with $V_{GS} = 0.6V$ and $V_{DS} = 100mV$.

This quantum effect produces a noticeable modification of

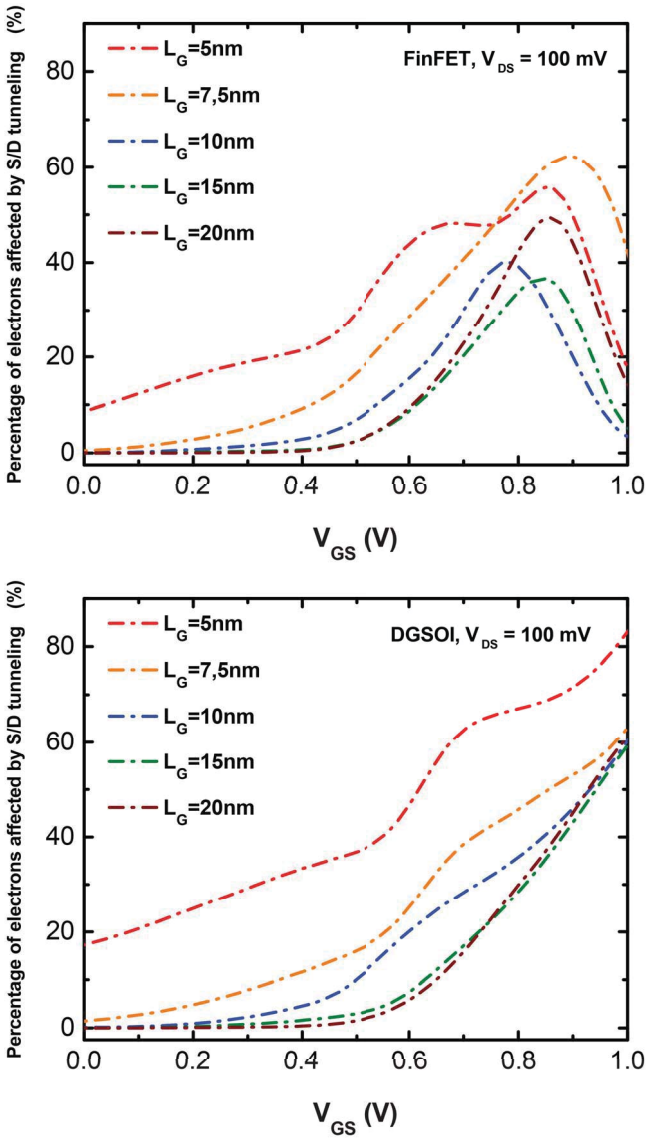



Fig. 4. Percentage of electrons affected by S/D tunneling near the potential barrier as a function of $L_G$ at low bias drain for FinFET (top) and for DGSOI(bottom).

the $I_D - V_{GS}$ characteristic (Figure 5). As it is shown, the influence of the S/D tunneling is lower in the FinFET (Figure 5 top) compared to DGSOI (Figure 5 bottom). The impact of the S/D tunneling on the threshold voltage variation $\Delta V_{th}$ of a simulation considering S/D tunneling and a simulation without taking it into account is shown in Figure 6. This effect is exacerbated as the dimensions of the device are reduced. Moreover, this phenomenon is not affected by $T_{si}$ at low bias drain.

## IV. Conclusions

This work presents the implementation of S/D tunneling in a MSB-EMC simulator for the study of its impact in DGSOI

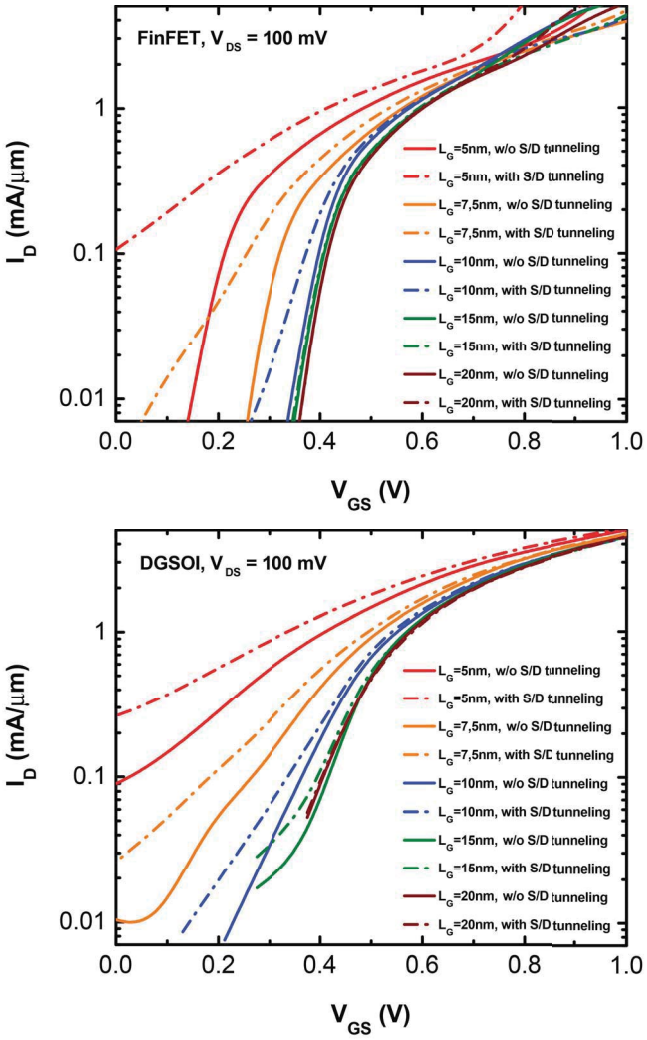



Fig. 5. $I_{DS}$vs.$V_{GS}$ as a function of $L_G$ at low bias with and w/o considering S/D tunneling for FinFET (top) and DGSOI (bottom).

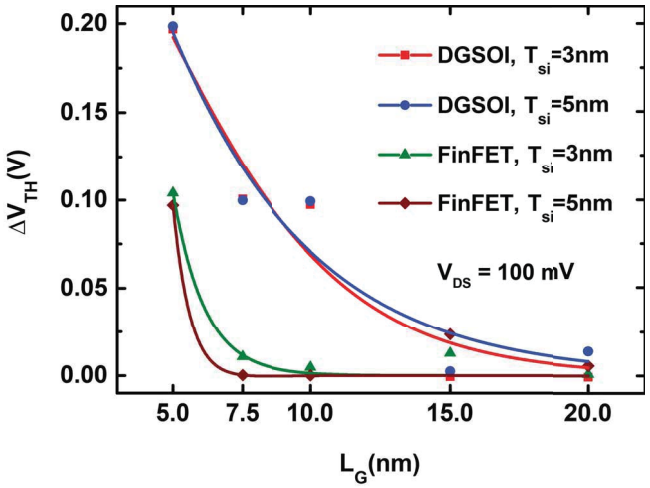



Fig. 6. Difference between the threshold voltage ($\Delta V_{th}$) of a simulation considering S/D tunneling and a simulation w/o taking it into account as a function of $L_G$ for FinFET and DGSOI.

and FinFET. Our simulations show important differences fully caused by the change in the confinement directions in both DGSOI and FinFET when S/D tunneling is taken into account due to the subband redistributions ans the variation of transport effective mass. Nevertheless, FinFET devices show less degradation in their subthreshold characteristics, and therefore are better candidates to implement future nodes, especially for ultra low power applications.

## V. Acknowledgment

The authors are grateful for the support given by the Spanish Ministry of Science and Innovation (TEC2011-28660, TEC2014-59730-R), Junta de Andalucía (P10-TIC-6902, P12-TIC-1996) and the European Commission (ECSEL-WAYTOGO FAST 662175) .

## References

[1] "The international Technology Roadmap For Semiconductors (ITRS)," http://www.itrs.net/, 2013.

[2] J. W. J. Wang and M. Lundstrom, "Does source-to-drain tunneling limit the ultimate scaling of MOSFETs?" *Digest. International Electron Devices Meeting,*, pp. 707–710, 2002.

[3] C. Medina-Bailon, C. Sampedro, F. Gámiz, A. Godoy, and L. Donetti, "Impact of S / D Tunneling in Ultrascaled Devices, a Multi-Subband Ensemble Monte Carlo Study." 2015 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), 2015, pp. 21–24.

[4] S. Cristoloveanu, "How many gates do we need in a transistor?" vol. 1. 2007 International Semiconductor Conference, 2007, pp. 3–10.

[5] R. Venugopal and Z. Ren, "Simulating Quantum Transport in nanoscale transistors: Real versus Mode-Space approaches," *J Appl Phys.*, vol. 92, no. 3730, 2002.

[6] C. Sampedro, F. Gámiz, a. Godoy, R. Valín, a. García-Loureiro, and F. G. Ruiz, "Multi-Subband Monte Carlo study of device orientation effects in ultra-short channel DGSOI," *Solid-State Electronics*, vol. 54, no. 2, pp. 131–136, 2010.

[7] C. Sampedro, F. Gámiz, a. Godoy, R. Valín, a. García-Loureiro, N. Rodríguez, I. M. Tienda-Luna, F. Martinez-Carricondo, and B. Biel, "Multi-Subband Ensemble Monte Carlo simulation of bulk MOSFETs for the 32 nm-node and beyond," *Solid-State Electronics*, vol. 65-66, no. 1, pp. 88–93, 2011.

[8] C. Sampedro, F. Gámiz, L. Donetti, and A. Godoy, "Reaching sub-32 nm nodes: ET-FDSOI and BOX optimization," *Solid-State Electronics*, vol. 70, pp. 101–105, 2012.

[9] C. Sampedro, F. Gámiz, and A. Godoy, "On the extension of ET-FDSOI roadmap for 22 nm node and beyond," *Solid-State Electronics*, vol. 90, pp. 23–27, 2013.

[10] A. Rahman, M. S. Lundstrom, A. W. Ghosh, A. Rahman, M. S. Lundstrom, and A. W. Ghosh, "Generalized effective-mass approach for n-type metal-oxide-semiconductor field-effect transistors on arbitrarily oriented wafers," *Journal of Applied Physics*, vol. 053702, no. 97, 2005.

[11] C. Sampedro, L. Donetti, F. Gámiz, and A. Godoy, "3D Multi-Subband Ensemble Monte Carlo Simulator of FinFETs and Nanowire Transistors." 2014 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), 2014, pp. 21–24.

[12] D. J. Griffiths, "Introduction to Quantum Mechanics," p. 409, 1995.

[13] C. Shen, L.-T. Yang, G. Samudra, and Y.-C. Yeo, "A new robust non-local algorithm for band-to-band tunneling simulation and its application to Tunnel-FET," *Solid-State Electronics*, vol. 57, no. 1, pp. 23–30, Mar. 2011.

# Volume and interface conduction in InGaAs junctionless transistors

L. Pirro, H. J. Park, I. Ionica,
M. Bawedin, S. Cristoloveanu
IMEP-LaHC, Minatec, Grenoble INP,
Univ. Grenoble Alpes, CNRS
Grenoble, France
pirrol@minatec.inpg.fr

L. Czornomaz, V. Djara, V. Deshpande
IBM
Ruschlikon, Switzerland

***Abstract*— Doped InGaAs were characterized using a revisited pseudo-MOSFET configuration. Two different conduction mechanisms were evidenced: volume and interface. The impact of film thickness, channel width and length is evaluated. Measurements at low temperatures complete the analysis.**

***Keywords—III-V; SOI; pseudo-MOSFET; static $I_D$-$V_G$; low-field mobility***

## I. Introduction

The extension of Moore's law and the fabrication of small devices with large carrier mobility are possible thanks to new materials that replace silicon in the transistor channel [1]–[3]. According to ITRS predictions [4], III-V compounds are promising candidates for the next generation n-type MOSFETs [5]–[7]. Furthermore, devices fabricated on semiconductor-on-insulator (SOI) substrates have better electrostatic control with decreased short channel effect and reduced leakage current [8]–[10]. Merging III-V and SOI yields III-V on insulator as starting substrate for device fabrication. In this work, $In_{0.53}Ga_{0.47}As$ layers transferred on oxide were characterized using a modified version of the well-known pseudo-MOSFET (Ψ-MOSFET) configuration [11]. Section 2 presents the characterized structure and details the measurement set-up. Section 3 shows a suitable procedure to extract the electron mobility based on extension of Y-function technique. The carrier mobility is extracted in Section 4, where also the temperature dependency is investigated.

## II. Measurement set-up

Fig. 1 shows the schematic of the tested structures. InGaAs layers with different thicknesses $t_{III\text{-}V}$ (*25 nm*, *50 nm*, *100 nm* and *200 nm*) were transferred on buried oxide (BOX composed of *10 nm* $Al_2O_3$ over *25 nm* $SiO_2$). The target doping of the III-V film was of $2{\cdot}10^{16}$ $cm^{-3}$. The technological steps are presented elsewhere [12]. The static analysis was performed by sweeping the gate bias $V_G$ applied on the substrate and measuring the resulting drain current ($I_D$) between source and drain contacts. Instead of the standard pressure probes of the Ψ-MOSFET, implanted $N^+$ regions are used as source and drain. This configuration is preferable because the impact of series resistance and probe-induced defects on the mobility is reduced. The channel dimensions are also well defined by the inter-contacts distance (representing the length $L$) and film width ($W$).

This work is supported by European projects COMPOSE$^3$ and III-V MOS.

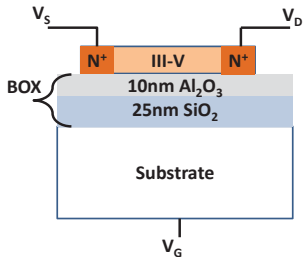



Fig. 1. Schematic view of back-biased InGaAs film on insulator, used for electrical characterization.

Fig. 2 presents the measured drain current $I_D$ versus drain bias $V_D$ for thick film ($t_{III\text{-}V}$ = *200 nm*). A linear trend is obtained, confirming the ohmic contacts present in the structure.

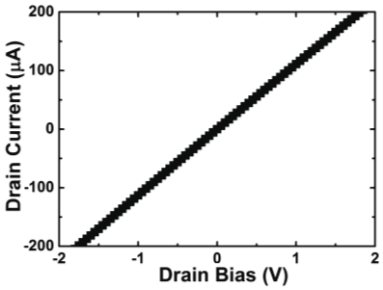



Fig. 2. Measured drain current $I_D$ versus drain bias $V_D$ for gate bias $V_G$ = *0*. $L$ = *200 μm* and $W$ = *20 μm*.

Fig. 3a shows $I_D$ (plain symbols) and associated transconductance $g_m$ (empty symbols) versus gate bias in thick InGaAs film (*200 nm*). A plateau is evidenced in $I_D(V_G)$ curve for $V_G \approx 0$ and double peaks appear in the $g_m(V_G)$ characteristic. The derivative of transconductance with respect to gate bias presents two clear peaks which lead to the extraction of flat-band voltage $V_{FB}$ and threshold voltage $V_T$ (see Fig. 3b) [13]. These signatures are a clear evidence of double conduction

mechanisms in the III-V film. Since the films are highly doped, volume conduction is possible even in absence of $V_G$. A negative gate bias induces a depletion region at the interface film-BOX, which modulates the thickness of the conduction volume. Beyond flat-band voltage ($V_G > V_{FB} \approx +1.1\ V$), an accumulation channel forms at the InGaAs-BOX interface and adds to the volume conduction.

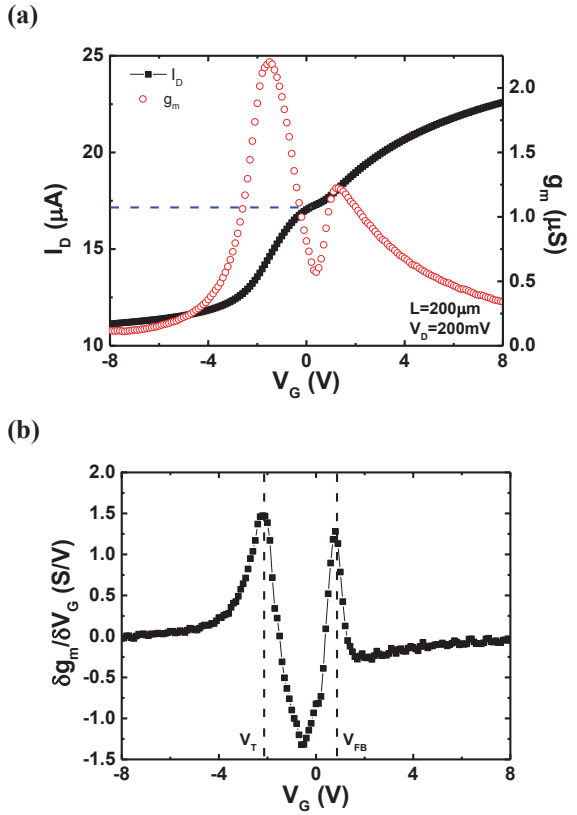



Fig. 3. (a) $I_D$ (plain symbols) and $g_m$ (empty symbols) versus gate bias. $t_{III\text{-}V} = 200\ nm$ and $W = 20\ \mu m$. The dashed line represents $I_{Vol}$. (b) Corresponding $g_m$ derivative with respect to $V_G$.

The double peak of transconductance tends to disappear in thinner films where the volume conduction is less pronounced as shown in Fig. 4.

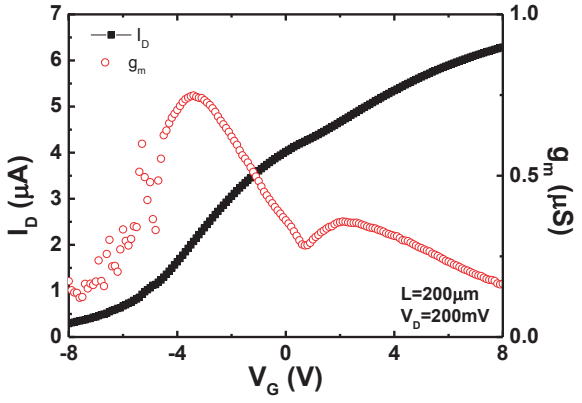



Fig. 4. $I_D$ (plain symbols) and gm (empty symbols) versus gate bias for $W = 20\ \mu m$ and $t_{III\text{-}V} = 25\ nm$.

### III. 3. Methods for Mobility Extraction

Before applying any model for mobility extraction, we need to evaluate whether the films are fully depleted or not. Knowing the doping level $N_d$, it is possible to compute the maximum width of depletion region in the III-V film [14]:

$$w_{d\_max} = \sqrt{\frac{4 \cdot \varepsilon_{III-V} \cdot k \cdot T \cdot \ln\left(\frac{N_d}{n_i}\right)}{q^2 \cdot N_d}} \quad (1)$$

where $\varepsilon_{III\text{-}V}$ and $n_i$ are the InGaAs dielectric constant and the intrinsic doping concentration. According to the film quality, $\varepsilon_{III\text{-}V}$ can vary between $13.1 \cdot \varepsilon_0$ and $14.1 \cdot \varepsilon_0$ [15], where $\varepsilon_0$ is the vacuum permittivity.

Considering $n_i = 6.3 \cdot 10^{11}\ cm^{-3}$ [15], the maximum depletion width is between *197 nm* and *205 nm*, which means that thin films ($t_{III\text{-}V} < 200\ nm$) are fully depleted. For $t_{III\text{-}V} = 200\ nm$, a light variation in the doping concentration or III-V film quality (*i.e.*, $\varepsilon_{III\text{-}V}$ variation) can modify the film status from partially depleted to fully depleted. Fig. 5 presents the measured $I_D(V_G)$ curves in devices with $t_{III\text{-}V} = 200\ nm$, same length ($L = 200\ \mu m$) and different widths. Full depletion is only reached for narrow width ($W = 2.5\ \mu m$), suggesting a 2D mechanism: depletion due to interface states from sidewalls adds to the vertical depletion induced by the gate.

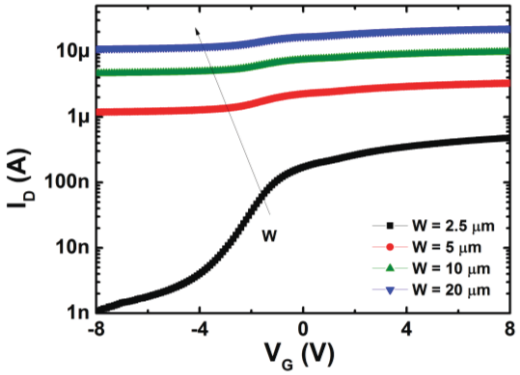



Fig. 5. Drain current $I_D$ versus gate bias $V_G$ for $t_{III\text{-}V} = 200\ nm$. The device length $L$ was $200\ \mu m$. The samples had different widths $W$: $2.5\ \mu m$, $5\ \mu m$, $10\ \mu m$ and $20\ \mu m$. $V_D = 200\ mV$.

To investigate the material quality, we used the approach proposed by Liu *et al.* [16]. In volume conduction regime, the drain current in the neutral (undepleted) region of the film can be written as:

$$I_D = \frac{W}{L} \cdot C_{BOX} \cdot \mu_{Vol} \cdot V_D \cdot (V_G - V_0) \quad (2)$$

where $C_{BOX}$ is buried oxide capacitance [12] and $V_0$ is the characteristic voltage which enables full depletion of the channel [17]:

$$V_0 = V_{FB} + \frac{q \cdot N_d}{C_{BOX}} \cdot t_{III-V} \quad (3)$$

$N_d$ is the active doping concentration and $\mu_{Vol}$ represents the volume mobility.

The surface mobility $\mu_S$ at the film-BOX interface is obtained from the Y-function ($Y_{fun}$) in accumulation regime, after removing the contribution of the volume current $I_{Vol}$ (Fig. 6 and dashed line in Fig. 3a) [17]:

$$Y_{fun} = \frac{I_D - I_{Vol}}{\sqrt{g_m}} = \sqrt{\frac{W}{L} \cdot C_{BOX} \cdot \mu_S \cdot V_D} \cdot (V_G - V_{FB}) \quad (4)$$

The slope of the linear fit performed on the $Y_{fun}(V_G)$ leads to the mobility in the accumulation channel, at the film-BOX interface:

$$\mu_S = \frac{slope^2}{\frac{W}{L} \cdot C_{BOX} \cdot V_D} \quad (5)$$

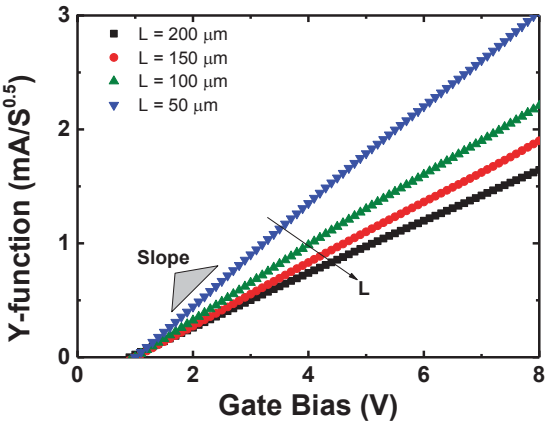



Fig. 6. Example of calculated Y-function as a function of $V_G$ for different lengths $L$: *200 µm*, *150 µm*, *100 µm* and *50 µm*. $t_{III\text{-}V}$ = *200 nm*.

## IV. Mobility Trends

The extracted $\mu_{Vol}$ (Fig. 7) is almost constant with the gate length $L$ for all devices tested. The lowest mobility is measured for $t_{III\text{-}V}$ = *25 nm*.

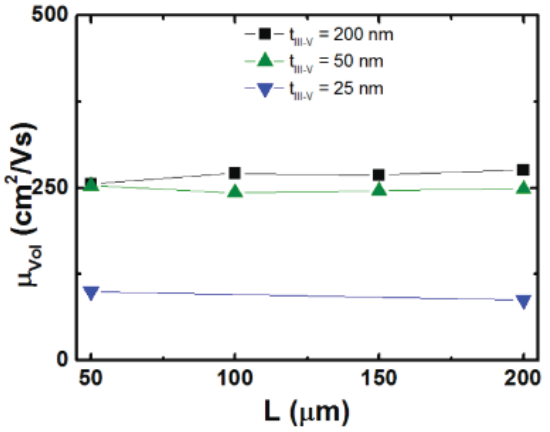



Fig. 7. Extracted volume mobility using Eq. (2) versus with different thickness, and length.

Fig. 8 shows the surface mobility $\mu_S$ versus $L$. $\mu_S$ is 20% lower than $\mu_{Vol}$ due to stronger scattering phenomena at the interface film-BOX [5], [10]. $\mu_S$ versus $L$ curves obtained for thick films ($t_{III\text{-}V}$ = *50-200 nm*) overlap showing less impact of the intrinsic field induced by the coupling between top surface and bottom interface, and suggest the unchanged interface quality between the III-V film and the BOX. This confirms the stability of the fabrication process. The lowest mobility is measured for $t_{III\text{-}V}$ = *25 nm*. Since charged defects exist on the free surface, the difference between the front and back surface potentials induces a vertical field, $E_{int} = (\Psi_{S1} - \Psi_{S2})/t_{III\text{-}V}$, that obviously increases in thinner films [18]. Even if the influence of the gate-induced field is removed in Y-function, the mobility is still affected by the intrinsic field. In other words, the low-field mobility is not accessible.

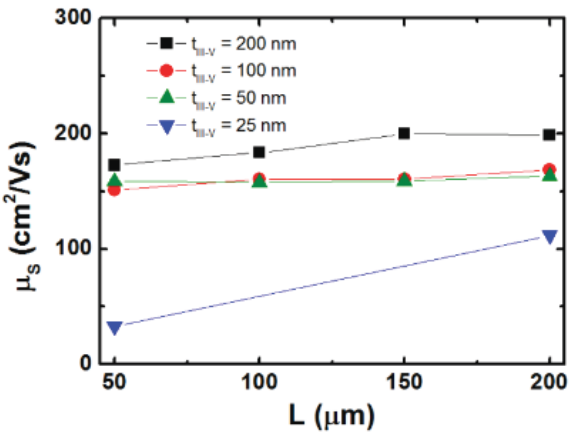
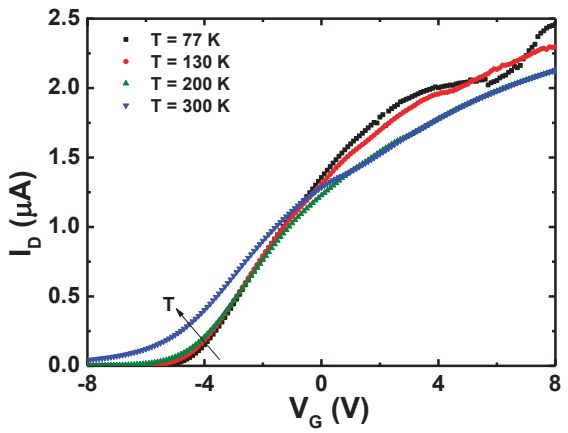



Fig. 8. Extracted surface mobility versus $L$ for different $t_{III\text{-}V}$.

Fig. 9a shows the measured drain current versus gate bias for different measurement temperatures $T$. The device had $t_{III\text{-}V}$ = *25 nm*. As reported for junctionless devices [19], [20], in accumulation regime the measured drain current increases for lower temperature because of larger mobility. At the same time, the flat-band voltage (empty symbols in Fig. 9b) decreases for higher $T$.

Fig. 9b also presents the subthreshold swing $S$ (plain symbols) versus $T$. A strong decrease of $S$ with temperature is found, as reported for undoped MOSFETs [10], confirming the dependency of subthreshold swing with temperature.

**(a)**



**(b)**

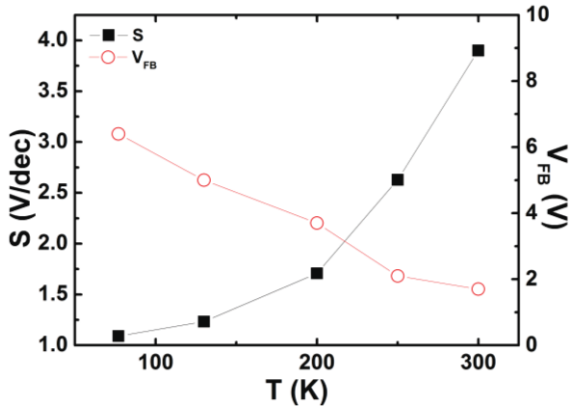



Fig. 9. (a) Drain current as a function of gate bias measured versus temperature. (b) Associated $S$ and $V_{FB}$ traced versus $T$. The device had $t_{III\text{-}V} = 25$ *nm* and $W = 5$ $\mu m$. The device length $L$ was *100* $\mu m$.

## V. Conlusions

The evidence of two conduction mechanisms (volume and interface accumulation) in InGaAs layer has been reported. The measured $I_D(V_G)$ curve presents a clear plateau followed by a current increase, proving the transition from volume conduction to surface one. Material quality was investigated for different geometry of the film structures (thickness, device width and length) pointing out their impact on the extracted carrier mobility. The volume mobility is slightly higher than the surface one. The lowest mobility is measured for $t_{III\text{-}V} = 25$ *nm* due to stronger coupling between top interface and conduction channel.

## References

[1] J. A. del Alamo, "Nanometre-scale electronics with III-V compound semiconductors," Nature, vol. 479, no. 7373, pp. 317–323, 2011.

[2] M. Egard, L. Ohlsson, B. M. Borg, F. Lenrick, R. Wallenberg, L.-E. Wernersson, and E. Lind, "High transconductance self-aligned gate-last surface channel $In_{0.53}Ga_{0.47}As$ MOSFET," in Electron Devices Meeting (IEDM), IEEE International, 2011, pp. 13.2.1–13.2.4.

[3] J. J. Gu, X. W. Wang, H. Wu, J. Shao, A. T. Neal, M. J. Manfra, R. G. Gordon, and P. D. Ye, "20-80nm Channel length InGaAs gate-all-around nanowire MOSFETs with EOT=1.2nm and lowest SS=63mV/dec," in Electron Devices Meeting (IEDM), IEEE International, 2012, pp. 27.6.1–27.6.4.

[4] ITRS 2013, "International Technology Roadmap for Semiconductors, 2013 Update Overview".

[5] N. Daix, E. Uccelli, L. Czornomaz, D. Caimi, C. Rossel, M. Sousa, H. Siegwart, C. Marchiori, J. M. Hartmann, K.-T. Shiu, C.-W. Cheng, M. Krishnan, M. Lofaro, M. Kobayashi, D. Sadana, and J. Fompeyrine, "Towards large size substrates for III-V co-integration made by direct wafer bonding on Si," APL Mater., vol. 2, no. 8, p. 086104, 2014.

[6] M. Yokoyama, T. Yasuda, H. Takagi, N. Miyata, Y. Urabe, H. Ishii, H. Yamada, N. Fukuhara, M. Hata, M. Sugiyama, Y. Nakano, M. Takenaka, and S. Takagi, "III-V-semiconductor-on-insulator n-channel metal-insulator-semiconductor field-effect transistors with buried $Al_2O_3$ layers and sulfur passivation: Reduction in carrier scattering at the bottom interface," Appl. Phys. Lett., vol. 96, no. 14, p. 142106, 2010.

[7] M. Radosavljevic, G. Dewey, D. Basu, J. Boardman, B. Chu-Kung, J. M. Fastenau, S. Kabehie, J. Kavalieros, V. Le, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, L. Pan, R. Pillarisetty, W. Rachmady, U. Shah, H. W. Then, and R. Chau, "Electrostatics improvement in 3-D tri-gate over ultra-thin body planar InGaAs quantum well field effect transistors with high-K gate dielectric and scaled gate-to-drain/gate-to-source separation," in Electron Devices Meeting (IEDM), IEEE International, 2011, pp. 33.1.1–33.1.4.

[8] J. G. Fiorenza, G. Braithwaite, C. W. Leitz, M. T. Currie, J. Yap, F. Singaporewala, V. K. Yang, T. A. Langdo, J. Carlin, M. Somerville, A. Lochtefeld, H. Badawi, and M. T. Bulsara, "Film thickness constraints for manufacturable strained silicon CMOS," Semicond. Sci. Technol., vol. 19, no. 1, pp. L4–L8, 2004.

[9] S. R. Banna, P. C. H. Chan, M. Chan, S. K. H. Fung, and P. K. Ko, "Fully depleted CMOS/SOI device design guidelines for low-power applications," IEEE Trans. Electron Devices, vol. 46, no. 4, pp. 754–761, 1999.

[10] S. Cristoloveanu and S. Li, Electrical Characterization of Silicon-on-Insulator Materials and Devices. Springer Science & Business Media, 1995.

[11] S. Cristoloveanu and S. Williams, "Point-contact pseudo-MOSFET for in-situ characterization of as-grown silicon-on-insulator wafers," IEEE Electron Device Lett., vol. 13, no. 2, pp. 102–104, 1992.

[12] L. Czornomaz, V. Djara, V. Deshpande, D. Caimi, L. Pirro, S. Cristoloveanu and J. Fompeyrine, accepted IEEE conf. EuroSOI&ULIS 2016.

[13] D.-Y. Jeon, S. J. Park, M. Mouis, M. Berthomé, S. Barraud, G.-T. Kim, and G. Ghibaudo, "Revisited parameter extraction methodology for electrical characterization of junctionless transistors," Solid-State Electron., vol. 90, pp. 86–93, 2013.

[14] S. M. Sze and K. K. Ng, Physics of Semiconductor Devices. John Wiley & Sons, 2006.

[15] E. F. Schubert, Doping in III-V Semiconductors. Cambridge University Press, 2005.

[16] F. Y. Liu, A. Diab, I. Ionica, K. Akarvardar, C. Hobbs, T. Ouisse, X. Mescot, and S. Cristoloveanu, "Characterization of heavily doped SOI wafers under pseudo-MOSFET configuration," Solid-State Electron., vol. 90, pp. 65–72, 2013.

[17] T. Ouisse, P. Morfouli, O. Faynot, H. Seghir, J. Margail, and S. Cristoloveanu, "A Detailed Investigation of the Pseudo-Mos Transistor for in Situ Characterization of Soi Wafers," in SOI Conference, 1992. IEEE International, 1992, pp. 30–31.

[18] G. Hamaide, F. Allibert, F. Andrieu, K. Romanjek, and S. Cristoloveanu, "Mobility in ultrathin SOI MOSFET and pseudo-MOSFET: Impact of the potential at both interfaces," Solid-State Electron., vol. 57, no. 1, pp. 83–86, 2011.

[19] I. M. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits," IEEE Trans. Circuits Syst. Fundam. Theory Appl., vol. 48, no. 7, pp. 876–884, 2001.

[20] D.-Y. Jeon, S. J. Park, M. Mouis, S. Barraud, G.-T. Kim, and G. Ghibaudo, "Low-temperature electrical characterization of junctionless transistors," Solid-State Electron., vol. 80, pp. 135–141, 2013.

# $V_{\mathrm{DD}}$ scaling of ultra-thin InAs MOSFETs: A full-quantum study

C. Grillet[a], M. Pala[a,b]
a. Univ. Grenoble Alpes, IMEP-LAHC, F-38000 Grenoble, France
b. CNRS, IMEP-LAHC, F-38000 Grenoble, France
E-mail: corentin.grillet@imep.grenoble-inp.fr ; marco.pala@imep.grenoble-inp.fr

***Abstract*—We performed 2D full-quantum simulations of ultra-thin InAs nMOSFETs and address a supply-voltage scaling investigation to evaluate the performance of such devices at different channel lengths. By adopting an 8×8 k · p Hamiltonian within the non-equilibrium Green's functions formalism in the presence of phonon scattering, we take into account non-parabolicity, band-to-band tunneling and strain effects, we find that at $V_{\mathrm{DS}}>$ 0.6V the transfer characteristics in the off-state are strongly deteriorated by hole-induced barrier lowering, while at $V_{\mathrm{DS}}=$ 0.5V, the simulated device reaches on-currents ($I_{\mathrm{on}}$) close to 500A/m, along with subthreshold swings (SS) as low as 65mV/dec.**

## I. Introduction

High-mobility III-V compounds are nowadays extensively investigated as channel materials to replace Si and SiGe with the aim to fulfill the ITRS requirements for the sub-10nm technological nodes [1]. Indeed, by combining materials from groups III and V of the periodic table, it is possible to obtain various compounds which present better transport properties than silicon (mainly due to their high mobility), but which also suffer from increased short channel effects (SCE). Recently, promising results have been reported in terms of $I_{\mathrm{on}}$ values and DIBL for InAs thin layer [2] [3] [4]. In this work, we will thus investigate the interest of this material as a channel material in a MOSFET device.

## II. Device

The device under investigation is similar to that of [2]. As shown in Fig. 1, it consists of an ultra-thin InAs channel of 2.4nm thickness deposited on an $In_{0.52}Al_{0.48}As$ surface. This Al molar fraction ratio allows this ternary compound to match the InP substrate lattice constant, thus avoiding dislocations. Since $a_{\mathrm{InAs}} > a_{\mathrm{InP}}$, the InAs layer undergoes *compressive* strain ($\varepsilon_{||}$=-0.0311, $\varepsilon_{\perp}$=0.0338), while the deformation of the InAlAs surface is neglected in our simulations.

The gate length ($L_{\mathrm{G}}$) ranges from 8 to 40nm, with a main focus on the 25nm gate length case. The InAs layer is doped on a 20nm length in both the source and the drain sides, with a donor concentration of $N_D$=3×10$^{19}$ cm$^{-3}$. 17nm length undoped spacers have been added on both sides of the gate to prevent source-to-drain tunneling (STDT) at small gate lengths. The gate oxide is composed of 0.5nm of $Al_2O_3$ on top of 2nm of $ZrO_2$, for an EOT of 0.52nm. All the dimensions of the device are listed in Tab. I.

TABLE I
Geometrical parameters of the studied device. The corresponding lengths are shown on the sketch of Fig. 1

| Thicknesses (nm) | | | | Lengths (nm) | | |
|---|---|---|---|---|---|---|
| $t_{\mathrm{InAs}}$ | $t_{\mathrm{InAlAs}}$ | $t_{\mathrm{Al_2O_3}}$ | $t_{\mathrm{ZrO_2}}$ | $L_{\mathrm{G}}$ | $L_{\mathrm{dop}}$ | $L_{\mathrm{sp}}$ |
| 2.4 | 100 | 0.5 | 2 | 8, 15, 25, 40 | 20 | 17 |

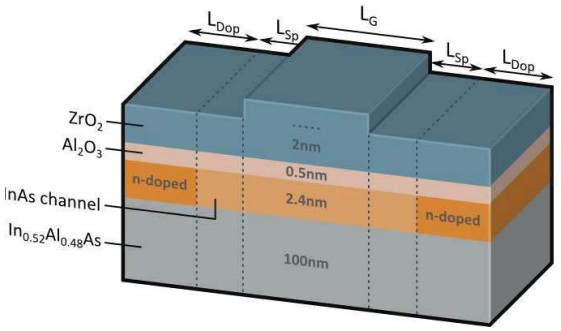



Fig. 1. Sketch of the InAs MOSFET.

## III. Model

In such structures, the small channel thickness generates a strong confinement, which leads to effects that have to be taken into account for an accurate prediction of the device behaviour. In our study, we consequently adopted a full-quantum approach to account for any leakage mechanism and quantum effect linked to the small dimensions of the device.

We use the Non-equilibrium Green's functions (NEGF) formalism, where the quantum electron transport is computed thanks to the Keldysh-Green's functions, described by a set of matrix equations which read:

$$\begin{cases} (EI - \mathcal{H} - \Sigma)G = I \\ G^{<} = G\Sigma^{<}G^{\dagger} \end{cases} \quad (1)$$

Where $G$ is the retarded Green's function, $E$ is the energy, $I$ is the identity matrix, and $\Sigma$ is the retarded self energy term. The matrices marked with the "$^{<}$" symbol represent the *lesser-than* quantities describing the carrier statistics (charge and currents) [5]. Equations (1) are solved with the coupled-mode space approach in order to reduce the computational burden [6].

ISBN 978-1-4673-8608-1  IEEE Catalog number CFP1649D-USB

To finish, $\mathcal{H}$ is the Hamiltonian of the system which is, in our study, a 8×8 bands $\mathbf{k}\cdot\mathbf{p}$ Hamiltonian [7]. Such an Hamiltonian enables us to consider transport within the Γ valley, which governs most of the carrier transport, and offers a decent balance between accuracy and computational burden. It consists in a semi-empirical approximation of the band-structure, and can be tuned to fit various III-V materials thanks to a set of parameters found in [8].

As explained in section *II*, the strain is an other phenomenon affecting the transport. To model it, we add a so-called strain interaction matrix to the 8×8 $\mathbf{k}\cdot\mathbf{p}$ Hamiltonian: $\mathcal{H}_{8,k.p} + \mathcal{H}_{8,strain}$ [9]. The deformation potentials used in $\mathcal{H}_{8,strain}$ are taken from [8]. In order to compute the value of the axial strain $\varepsilon_{||}$, we compare the lattice parameters of the stacked materials. The transverse strain $\varepsilon_{\perp}$ is then simply obtained with a macroscopic approach, using the material's Poisson's ratio ($\nu = \varepsilon_{\perp}/\varepsilon_{||}$).

To model the electrostatics of the system, this whole Hamiltonian is then coupled with Poisson's equation in a self-consistent loop. Indeed, the carrier concentrations obtained after solving Schrödinger and Green's equations is linked to the electric potential $\phi$, computed with Poisson's equation:

$$\nabla\cdot\varepsilon\nabla\phi = -q(N_D - n - N_A + p) \tag{2}$$

where $\varepsilon$ is the material permittivity and $N_D$, $n$, $N_A$ and $p$ are the donor, electron, acceptor and hole concentrations, respectively.

Scattering mechanisms are also very relevant when considering transport in nanodevices. Phonon scattering is implemented via the self-consistent Born approximation (SCBA) and local self-energies $\Sigma^{<(>)} = D_0^{<(>)}G^{<(>)}$, where $D_0^{<(>)}$ is to the Green's function of the unperturbed phonon bath [10]. Acoustic phonons are treated within the elastic approximation, whereas polar optical phonons are assumed to be dispersionless. In the NEGF formalism, the phonon scattering is modeled through the self-energy term, which can then be written $\Sigma = \Sigma_{SD} + \Sigma_{ph}$, where $\Sigma_{\mathrm{SD}}$ accounts for the interaction with the source and drain contacts, and $\Sigma_{\mathrm{ph}}$, for the electron-phonon interaction. For acoustic phonons, the corresponding *lesser-than* quantity at the *i*-th slice and for the *n*-th mode reads:

$$\Sigma^{<\,n,n}_{ph,ac}(x_i,E) = \frac{D^2_{\mathrm{ac}}k_BT}{\rho\nu_S^2}\sum_m I^{m,n}(x_i)G^{<\,m,m}(x_i,E)\,, \tag{3}$$

where $I^{m,n}(i) = \int dz|\chi_m|^2(x_i,z)|\chi_n|^2(x_i,z)$ is the form factor, $\chi_n$ the $n$-th transverse mode, $D_{\mathrm{ac}}$ stands for the acoustic deformation potential, $\rho$ is the InAs density, $\nu_S$ is the sound velocity and $k_{\mathrm{B}}T$ is the usual Boltzmann constant times temperature. Likewise, the *lesser-than* self-energy term for the optical phonons is written:

$$\Sigma^{<\,n,n}_{ph,op}(x_i,E) = \frac{\hbar D^2_{\mathrm{op}}}{2\rho\omega}\sum_m I^{m,n}(x_i)G^{<\,m,m}(x_i,E\pm\hbar\omega) \left[N_{BE}(\hbar\omega)+\frac{1}{2}\pm\frac{1}{2}\right], \tag{4}$$

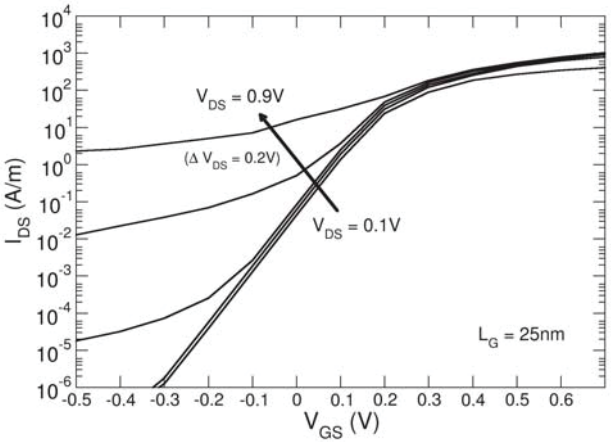



Fig. 2. Transfer characteristics at $V_{\mathrm{DS}}$=0.1, 0.3, 0.5, 0.7 and 0.9V for a device with $L_{\mathrm{G}}$=25nm. The gate work-function is chosen in order to have $I_{\mathrm{off}}$=0.1uA/um for $V_{\mathrm{DS}}$=0.5V.

where $D_{\mathrm{op}}$ is the optical deformation potential, $\omega$ is the optical phonon frequency and $N_{BE}$ is the Bose-Einstein phonon density. Deformation potentials and optical phonon frequencies have been taken from [9].

## IV. Results

Transfer characteristics for different $V_{\mathrm{DS}}$ values varying from 0.1 to 0.9 V and $L_{\mathrm{G}}$=25nm are shown in Fig. 2. This plot is characterized by a significant increase of the off-current ($I_{\mathrm{off}}$) and SS degradation as $V_{\mathrm{DS}}$ increases. To gain physical insight on this behavior, we plot, in Fig. 3, the lowest conduction (LC) and the highest valence (HV) subband for different $V_{\mathrm{GS}}$ at $V_{\mathrm{DS}}$=0.7V. We note that the effective gap is larger than in bulk InAs due to quantum-confinement and strain effects [11]. A first observation which can be made from this figure is that – for low values of $V_{\mathrm{GS}}$ – the LC subband is energetically lower than the HV subband near the channel/drain junction area. This condition enhances band-to-band-tunneling BTBT of valence electrons in the channel and conduction electrons in the drain (see also the local density of states in Fig. 5(a)). However, such a BTBT does not directly contribute to the overall $I_{\mathrm{DS}}$ current: the electrons tunneling towards the valence band balance those tunneling towards the conduction band (see the spectral current distribution in Fig. 5(b)).

Importantly, the HV subband at the source remains lower that the LC subband at the drain. Thus, this localized BTBT does not enhance direct STDT. However, it is still detrimental for the device performance, since it induces a positive charge in the channel and therefore decreases the gate control on the channel barrier, especially when $V_{\mathrm{GS}}$ is low (since the BTBT window is then larger). This hole-induced barrier lowering (HIBL) results in a degraded sub-threshold swing (SS) for $V_{\mathrm{DS}}$>0.5V [12]. As shown in Fig. 5 the $I_{\mathrm{off}}$ is therefore dominated by the thermionic component at energies higher than the top of the barrier (the conduction subband). However, the InAs MOSFET works properly at $V_{\mathrm{DS}}$<0.6V, for which

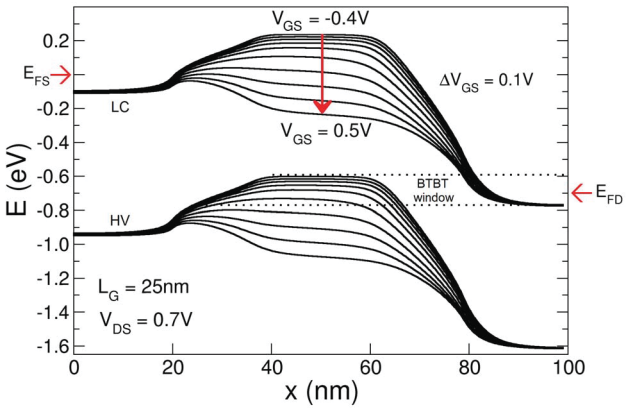



Fig. 3. Spatial profile of the highest valence subband and of the lowest conduction subband at different $V_{\rm GS}$ and $V_{\rm DS}$=0.7V for a device with $L_{\rm G}$=25nm. Dashed lines indicate the energy window where BTBT occurs. $E_{\rm FS}$ and $E_{\rm FD}$ are the Fermi levels in the source and in the drain.

the HV subband is always smaller than the LC subband for the $V_{\rm GS}$ of interest (see Fig. 4).

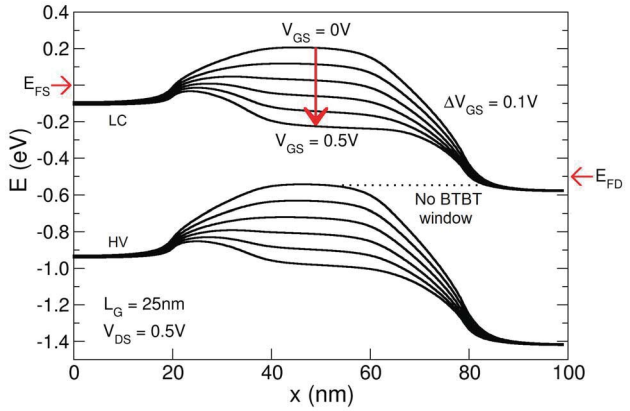



Fig. 4. Same as Fig. 3, but at $V_{\rm DS}$=0.5V. The BTBT window is smaller to non-existant, suppressing parasitic charges in the top of the HV and subsequently enhancing the gate control and the SS.

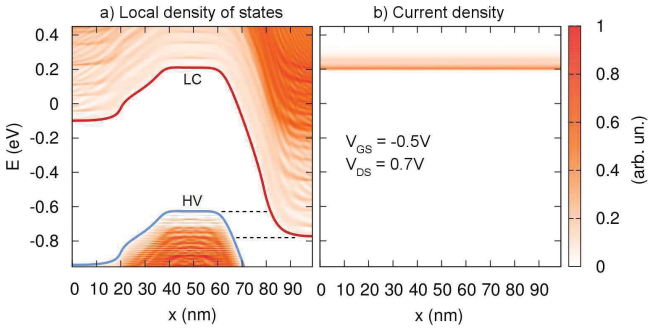



Fig. 5. (a) Local density of states and (b) spectral current density as a function of the position along the transport direction and of the energy at $V_{\rm GS}$=-0.5V and $V_{\rm DS}$=0.7V for a device with $L_{\rm G}$=25nm. The OFF-current flows normally over the top of the LC, without tunneling through the barrier.

Fig. 6 shows the output characteristics of a device with $L_{\rm G}$=25nm presenting an ideal linear behavior at small $V_{\rm DS}$ and high saturation currents, demonstrating the excellent transport properties of this ultra-thin InAs MOSFET.

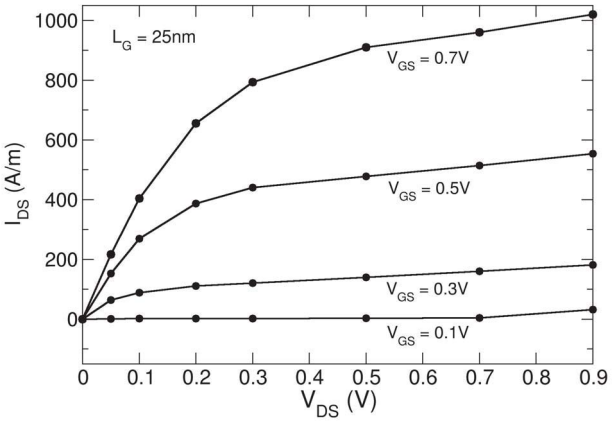



Fig. 6. Output characteristics a $V_{\rm GS}$=0.1, 0.3, 0.5 and 0.7V for a device with $L_{\rm G}$=25nm.

An optimal electrostatic integrity can be also appreciated in Fig. 7 showing the SS and the DIBL as a function of $L_{\rm G}$. Relatively acceptable SS and DIBL values are reported even at $L_{\rm G}$=8nm. These are due to the use of an aggressive oxide with an EOT=0.52nm and by the absence of significant interface traps, which otherwise can strongly degrade the SS [11], [13]. We remark that this result is consistent with the characterization data reported in [2]. In Fig. 8 we show the $I_{\rm on}$ (computed as the $I_{\rm DS}$ at $V_{\rm GS}$=$V_{\rm DS}$=$V_{\rm DD}$=0.5V) dependence on $L_{\rm G}$ for $I_{\rm off}$=0.1uA/um, which is the ITRS specification for high-performance (HP) applications. A maximal value of $I_{\rm on}$ 0.5 mA/um compatible with the experimental value measured in [2] is found. It is worthwhile to remark that the $I_{\rm on}$ decreases as $L_{\rm G}$ is essentially reduced due to the worst electrostatic integrity and the consequent SS deterioration, whereas tunneling current is negligible even at $L_{\rm G}$=8nm, mainly because of the use of large spacer regions that suppress direct source-to-drain tunneling, which is often the main source of the $I_{\rm off}$ degradation in such devices [14].

Finally, to summarize these results, we estimated the intrinsic switching time $T_{\rm sw}$ and switching energy $E_{\rm sw}$ of a digital inverter, defined as

$$T_{\rm sw} = \frac{Q_{\rm on} - Q_{\rm off}}{I_{\rm on}} \tag{5}$$

and

$$E_{\rm sw} = V_{\rm DD}(Q_{\rm on} - Q_{\rm off})\,, \tag{6}$$

where $Q_{\rm on}$ and $Q_{\rm off}$ are the channel charge at the ON and OFF states. As expected, in Fig. 9 the switching delay of the 25nm InAs MOSFET decreases with $V_{\rm DD}$, while the switching energy increases. Even if more factors, such as the parasitic capacitances, which are here neglected, should be taken into consideration to realistically predict these metrics,

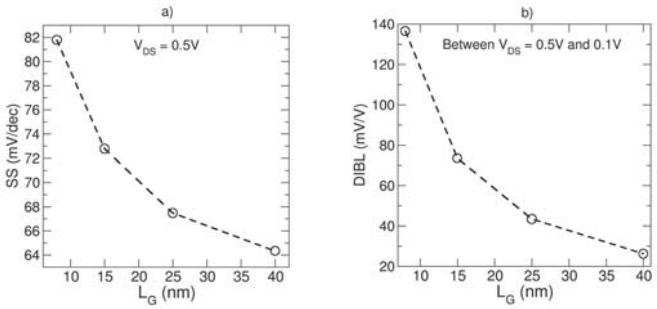



Fig. 7. (a) Sub-threshold swing (SS) evaluated at $V_{\rm DS}$=0.5V and (b) DIBL evaluated between $V_{\rm DS}$=0.5V and $V_{\rm DS}$=0.1V as a function of $L_{\rm G}$.

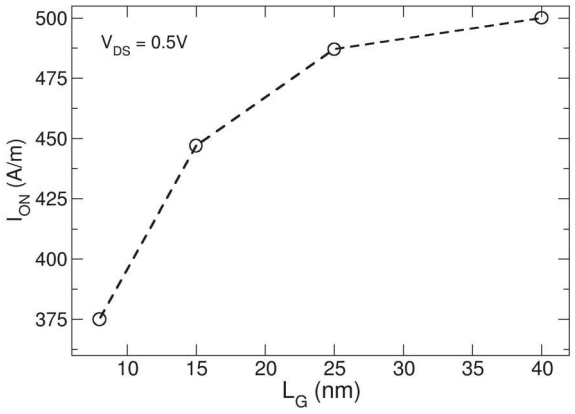



Fig. 8. On current ($I_{\rm on}$) as a function of $L_{\rm G}$ computed assuming $V_{\rm DS}$=0.5V and $I_{\rm off}$=0.1uA/um.

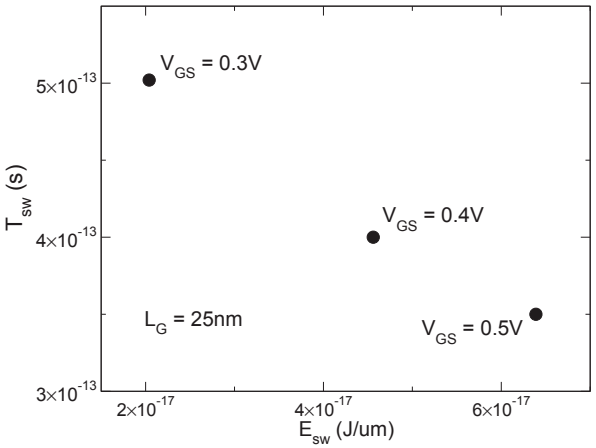



Fig. 9. Intrinsic switching time $T_{\rm sw}$ verus switching energy $E_{\rm sw}$ of a device with $L_{\rm G}$=25nm, estimated for different supply voltages and assuming $I_{\rm off}$=0.1 uA/um.

Fig. 9 shows very promising performances for HP applications at $V_{\rm DD}$=0.5V.

## V. Conclusion

Our 2D full-quantum simulations of ultra-thin InAs channel MOSFETs have shown that for $V_{\rm DS}$<0.6V such devices can provide $I_{\rm on}$ values compatible with the ITRS requirements even at small gate lengths, but they suffer from significant HIBL and BTBT, degrading their SS at larger $V_{\rm DS}$. Direct STDT is however avoided thanks to the use off spacers on both sides of the gate, which allow relatively small OFF-currents for low bias voltages.

## Acknowledgments

This work is supported by the French ANR with the Labex *MINOS* and the projects *MOSINAS* (ANR-13-NANO-0001-04) and *NOODLES* (ANR-13-NANO-0009-01).

## References

[1] (2013) International technology roadmap for semiconductors. [Online]. Available: http://www.itrs.net/2013ITRS/Summary2013.htm

[2] S. Lee *et al.*, "Record ion (0.50 ma/um at vdd = 0.5 v and ioff = 100 na/um) 25 nm-gate-length zro2/inas/inalas mosfets," in *VLSI Technology (VLSI-Technology): Digest of Technical Papers, 2014 Symposium on*, June 2014, pp. 1–2.

[3] J. Lin, X. Zhao, T. Yu, D. Antoniadis, and J. Del Alamo, "A new self-aligned quantum-well mosfet architecture fabricated by a scalable tight-pitch process," in *Electron Devices Meeting (IEDM), 2013 IEEE International*, Dec 2013, pp. 16.2.1–16.2.4.

[4] J. Lin, D. Antoniadis, and J. Del Alamo, "Novel intrinsic and extrinsic engineering for high-performance high-density self-aligned ingaas mosfets: Precise channel thickness control and sub-40-nm metal contacts," in *Electron Devices Meeting (IEDM), 2014 IEEE International*, Dec 2014, pp. 25.1.1–25.1.4.

[5] S. Datta, *Electronic Transport in Mesoscopic Systems*. Cambridge University Press, 1998.

[6] M. Shin, "Full-quantum simulation of hole transport and band-to-band tunneling in nanowires using the k·p method," *Journal of Applied Physics*, vol. 106, no. 5, p. 054505, 2009. [Online]. Available: http://dx.doi.org/doi/10.1063/1.3208067

[7] T. B. Bahder, "Eight-band $\mathbf{k}\cdot\mathbf{p}$ model of strained zinc-blende crystals," *Phys. Rev. B*, vol. 41, pp. 11 992–12 001, Jun 1990.

[8] I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, "Band parameters for III–V compound semiconductors and their alloys," *Journal of Applied Physics*, vol. 89, no. 11, pp. 5815–5875, 2001.

[9] F. Conzatti, M. Pala, D. Esseni, E. Bano, and L. Selmi, "Strain-Induced Performance Improvements in InAs Nanowire Tunnel FETs," *Electron Devices, IEEE Transactions on*, vol. 59, no. 8, pp. 2085–2092, 2012.

[10] S. Poli and M. Pala, "Channel-Length Dependence of Low-Field Mobility in Silicon-Nanowire FETs," *IEEE Electron Device Lett.*, vol. 30, no. 11, pp. 1212 –1214, nov. 2009.

[11] M. Pala and D. Esseni, "Interface Traps in InAs Nanowire Tunnel-FETs and MOSFETs – Part I: Model Description and Single Trap Analysis in Tunnel-FETs," *Electron Devices, IEEE Transactions on*, vol. 60, no. 9, pp. 2795–2801, 2013.

[12] M. Luisier, M. Lundstrom, D. Antoniadis, and J. Bokor, "Ultimate device scaling: Intrinsic performance comparisons of carbon-based, ingaas, and si field-effect transistors for 5 nm gate length," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, Dec 2011, pp. 11.2.1–11.2.4.

[13] D. Esseni and M. Pala, "Interface Traps in InAs Nanowire Tunnel FETs and MOSFETs – Part II: Comparative Analysis and Trap-Induced Variability," *Electron Devices, IEEE Transactions on*, vol. 60, no. 9, pp. 2802–2807, 2013.

[14] D. Esseni, M. Pala, and T. Rollo, "Essential physics of the off-state current in nanoscale mosfets and tunnel fets," *Electron Devices, IEEE Transactions on*, vol. 62, no. 9, pp. 3084–3091, Sept 2015.

# Contact Resistances in Trigate Devices in a Non-Equilibrium Green's Functions Framework

Léo Bourdet*†, Jing Li*†, Johan Pelloux-Prayer†‡, François Triozon†‡, Mikaël Cassé†‡, Sylvain Barraud†‡, Sébastien Martinie†‡, Denis Rideau§, and Yann-Michel Niquet*†¶
*CEA, INAC-SP2M, L_Sim, Grenoble, France
†Université Grenoble Alpes, Grenoble, France
‡CEA, LETI, Minatec Campus, Grenoble, France
§STMicroelectronics, Crolles, France
¶Email: yniquet@cea.fr

***Abstract*—We compute the contact resistances in Trigate and FinFET devices using a Non-Equilibrium Green's Functions approach. Electron-phonon, surface roughness and Coulomb scattering are taken into account. We show that the contact resistance represents a significant part of the total resistance of devices with sub-30 nm gate lengths. The analysis of the quasi-Fermi level profile reveals that the spacers between the heavily doped source/drain and the gate are major contributors to the contact resistance. We analyze the impact of different design parameters (cross section and doping profile in the contacts) on the electrical performances of the devices. The simulations are compared to experimental data.**

## I. Introduction

As the gate length $L$ of field-effect transistors is reaching the sub-20 nm range, the contact resistances are increasingly limiting the electrical performances of the devices. The "apparent" contact resistance $R_c$ can be defined as the extrapolation to zero gate length of the total resistance of the device, $R(L) = V_{ds}/I_{ds}$, where $I_{ds}$ is the drain current and $V_{ds}$ the source-drain voltage. In the low $V_{ds}$ regime, this contact resistance is dominated by i) the quality of the metal-semiconductor contact, ii) the transport through the lowly doped regions of the devices such as the spacers, and iii) the ballistic resistance of the channel [1], [2]. Although the latter can be intrinsic to the channel, it is usually mixed into the apparent contact resistance as it is independent on the gate length.

While the transport through the transistor channel has been extensively studied, there is much less literature on the contact resistances [3], [4], [5], [6]. Most models are based on drift-diffusion equations needing carrier mobilities as input, which might not be well characterized in the very inhomogeneous source/drain extensions.

In this work, we compute components ii) and iii) of the contact resistance in Fully-Depleted Silicon-on-Insulator (FDSOI) Trigate and FinFET devices in a Non-Equilibrium Green's Functions (NEGF) framework [7], which explicitly accounts for confinement and scattering by phonons, surface roughness, and dopants in the inhomogeneous source and drain. The contact resistance extraction is based on the $R(L)$ data extrapolation. It can be supplemented with a quasi-Fermi level analysis, which highlights where the potential drops in the device. It shows, in particular, that the contact resistance is dominated by the lowly doped spacers between the source/drain and the channel. We next discuss the impact of some design parameters (channel cross section and doping profile) on the contact resistance. We finally provide experimental support for the main conclusions of this work.

## II. Simulation methodology

### A. Devices

The channel is a rectangular [110] oriented silicon nanowire with width $W$ and height $H$ in the 4 to 24 nm range, etched in a (001) SOI layer [8]. It is lying on a 25 nm thick buried oxide (BOX) and a n-doped Si substrate (donor concentration $N_d = 10^{18}$ cm$^{-3}$). The gate stack is made of 0.8 nm $SiO_2$ and 2.2 nm $HfO_2$. The gate is separated from bulk source and drain contacts by 6 nm long $Si_3N_4$ spacer regions (see Fig. 1). Planar devices corresponding to the limits $W \to \infty$ (FDSOI) and $H \to \infty$ (double gate) are also considered.

Point-like dopants are added to the source and drain according to the different target distributions plotted in Fig. 2, in order to capture impurity scattering in these regions. Surface roughness, Remote Coulomb Scattering (RCS) in the channel, and electron-phonon interactions are also included in the simulations. The interface roughness parameters for the top and bottom interfaces are chosen to reproduce the experimental mobility in planar FDSOI devices (along the lines of Ref. [9]). The parameters of the side facets as well as the density of RCS trapped charges are chosen to reproduce the experimental mobility in $W = 10 \times H = 10$ nm Trigate devices.

### B. The NEGF approach

The current is computed in a self-consistent NEGF framework [7] within the effective mass approximation. The NEGF equations are solved in a fully coupled mode space approach. Details can be found in Ref. [10]. Electron-phonon scattering is described by an acoustic deformation potential $D_{ac} = 14.6$ eV, and by the three $f$ and three $g$ inter-valley processes of Ref. [11]. One of the main advantages of NEGF is that all structural scattering mechanisms (SR, impurity and RCS scattering) are treated explicitly. There is no need for models for the interactions with these disorders. As a matter of fact,

ISBN 978-1-4673-8608-1  IEEE Catalog number CFP1649D-USB

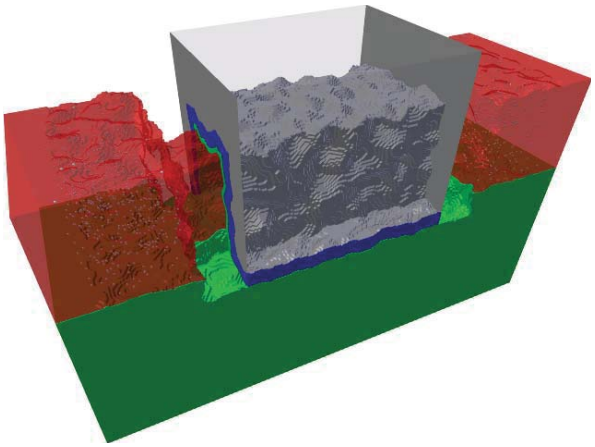


Fig. 1. A $W = 10 \times H = 10$ nm Trigate device, with overgrown source and drain contacts. Silicon is in red, $SiO_2$ in green, $HfO_2$ in blue and the gate in gray. The dots in the contacts are single dopant impurities. The spacers are 6 nm long.

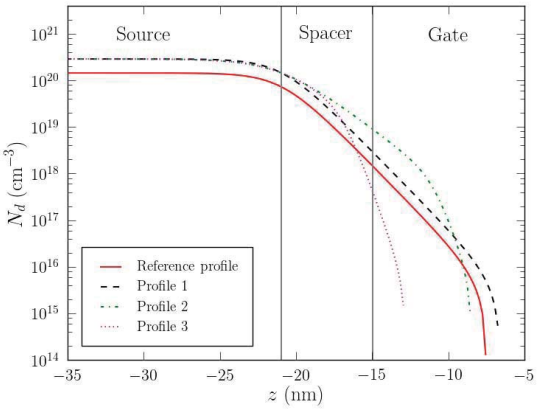



Fig. 2. Target doping profiles in the source of Fig. 1 (doping profiles are symmetric in the drain). They are used to generate random dopant distributions.

such models are still missing under the spacers, which are very inhomogeneous but critical regions on the resistive path. Also, at variance with most previous NEGF calculations, the source and drain contacts are chosen wide enough with respect to the channel to act as bulk reservoirs (with a 3D-like density of states). This is essential for a quantitative description of the contact resistances.

### C. Contact resistance extraction

At the low drain bias $V_{ds} = 10$ mV chosen in the simulations, the resistance $R(L)$ of the devices is linear with $L$ in the 20-100 nm range and can therefore be extrapolated to $L = 0$ (Fig. 3) to obtain the contact resistance $R_c$. Also, the long channel mobility is deduced from the slope of $R(L)$. To perform the $R(L)$ fits, we prepare a series of devices with lengths $L = 30$, 60, and 90 nm, sharing the same contacts (source/drain/spacers geometry and dopant distributions). In order to limit the noise on the $R(L)$ data that might arise from

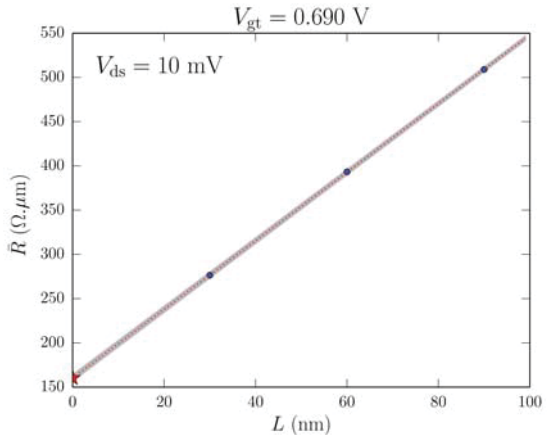



Fig. 3. The resistance $\bar{R}(L)$ as a function of channel length $L$ for a particular realization of the "Reference" doping profile of Fig. 2. The carrier density in the channel is $n = 10^{13}$ cm$^{-2}$. The contact resistance is the extrapolated $\bar{R}_c = \bar{R}(L \to 0)$, while the slope gives an estimate of the carrier mobility in the channel.

different disorders at different $L$'s, we repeat the 30 nm long sample of surface roughness and RCS charges along the 60 and 90 nm long channels. We can extract that way the resistance of the chosen contact geometry and dopant distribution very accurately. We then average the contact resistance over 3 to 5 surface roughness profiles and dopant distributions in order to assess local variability. In order to ease the comparison between devices with different cross sections, the carrier densities $n_{2d} = n_{1d}/W_{eff}$ and the resistances $\bar{R} = RW_{eff}$ are normalized to the total effective width of the channel $W_{eff} = W + 2H$.

## III. Contact resistance of a $W = 10 \times H = 10$ nm Trigate device

The contact resistance $\bar{R}_c$ in a $10 \times 10$ nm Trigate is plotted as a function of the carrier density in the channel in Fig. 4 (red line with dots), for the "Reference" doping profile of Fig. 2. It is compared to the ballistic resistance of the channel (no scattering), and to the contact resistance extracted in a device without surface roughness nor impurity scattering in the source/drain (continuous background dopant distributions). The contact resistance is much larger than the ballistic resistance, and is clearly limited by scattering by dopant impurities and surface roughness. It represents a significant part of the total resistance of a $L = 30$ nm long device (green line with diamonds).

The physical origins of the contact resistance are further clarified by a quasi-Fermi level analysis, which highlights where the potential drops in the system. At low bias, the local distribution function $f(\mathbf{r}, E)$ of the carriers remains close to a Fermi-Dirac distribution. The quasi-Fermi level $\epsilon_f(\mathbf{r})$ is defined as the chemical potential that reproduces the NEGF carrier density $n(\mathbf{r})$ assuming local Fermi-Dirac statistics. It is plotted in Fig. 5 for the $10 \times 10$ nm Trigate with gate length $L = 30$ nm, at different gate voltages. The potential drop is

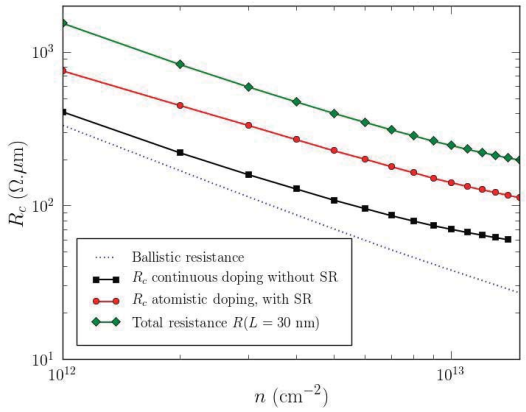



Fig. 4. The normalized contact resistance $\bar{R}_c$ extracted from Fig. 3 as a function of the carrier density $n$ in the channel. It is compared to the ballistic resistance of the channel, to the contact resistance extracted without surface roughness nor impurity scattering, and to the total resistance of a $L = 30$ nm long device.

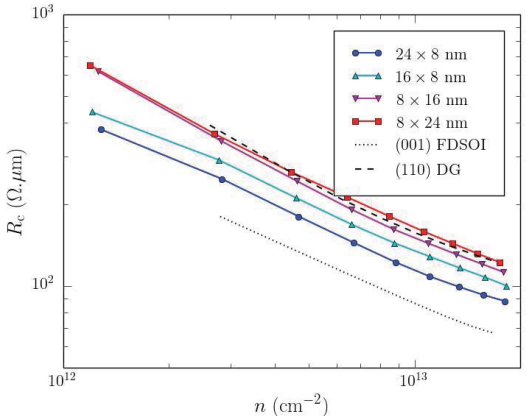



Fig. 6. The normalized contact resistance $\bar{R}_c$ as a function of $n$ for different nanowire cross sections $W \times H$. The target doping profile is the "Reference" profile of Fig. 2. The data are compared with reference (001) FDSOI ($H = 8$ nm, $W \to \infty$) and (110) double gate devices ($W = 8$ nm, $H \to \infty$).

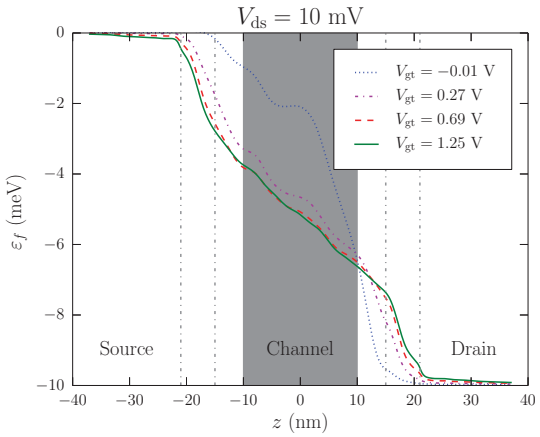



Fig. 5. Quasi-Fermi level in a 30 nm long, $W = 10 \times H = 10$ nm Trigate device with the reference doping profile of Fig. 2, at different gate overdrives. The drain bias is $V_{ds} = 10$ mV. The shaded gray area delimits the segment where the slope $d\epsilon_f/dz$ of the quasi-Fermi level is nearly constant.

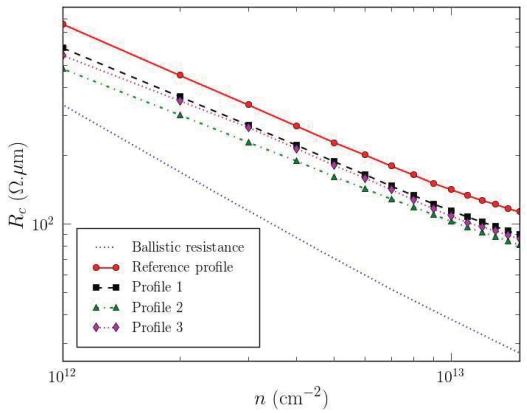



Fig. 7. The normalized contact resistance $\bar{R}_c$ as a function of $n$ for the different doping profiles of Fig. 2.

much larger under the spacers than in the highly-doped source and drain regions. Hence the spacer regions give the main contribution to the contact resistance. At moderate to high inversion, the regular slope of the quasi-Fermi level in the channel (gray region in Fig. 5) indicates a diffusive transport regime. Moreover, the mobility extracted from this slope is close to the mobility extracted from the $R(L)$ fit. Hence the concept of mobility remains relevant here.

## IV. Influence of Technological Parameters on the Contact Resistance

### A. Channel cross section

The normalized contact resistances for different nanowire cross sections are plotted in Fig. 6. The results can be largely explained by the transition from volume carrier density under the spacers to surface inversion (at high gate overdrive) in the channel region. The contribution of the spacer regions to the contact resistance is basically proportional to the cross sectional area $S = WH$. Hence FinFET devices, which maximize the effective width $W_{eff} = W + 2H$ at a given $S$, show a larger normalized contact resistance $\bar{R}_c = R_c W_{eff}$.

### B. Doping profile

The contact resistances for the different doping profiles of Fig. 2 are plotted in Fig. 7. Slower decay of doping under the spacers slightly decrases the contact resistance, at the expense of a larger drain-induced barrier lowering at high bias. The problem of contact resistances at high field is, however, beyond the scope of the present work and will be discussed in another paper.

## V. Comparison with Experimental Data

The simulations are compared with experimental data on Trigate devices fabricated at CEA/LETI [12]. The contact

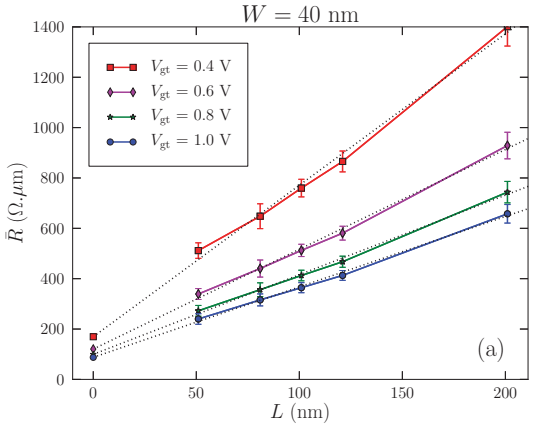



Fig. 8. Total resistance measured as a function of length in $W = 40 \times H = 12$ nm Trigate devices, for different gate overdrives.

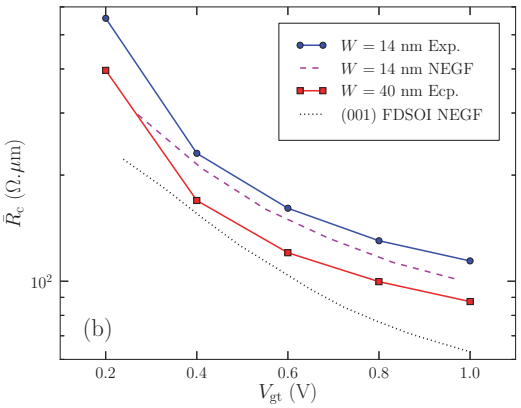



Fig. 9. Measured contact resistances in $W = 40 \times H = 12$ nm and $W = 14 \times H = 12$ nm Trigate devices, as a function of gate overdrive. They are compared with simulations for a planar (001), 12 nm thick FDSOI device and for a $W = 14 \times H = 12$ nm Trigate device.

resistances are extracted using the same $R(L)$ method as in the simulations, in the $L = 50-200$ nm range. The fits at different gate overdrives $V_{gt}$ are shown in Fig. 8. The mobilities obtained from the $R(L)$ slopes are in very good agreement with the long channel mobilities measured on similar Trigate devices and with NEGF simulations. The obtained contact resistances are plotted in Fig. 9 for $W = 40 \times H = 12$ nm and $W = 14 \times H = 12$ nm devices. They are compared to simulations performed for these specific devices, which have 9 nm thick spacers. The experimental data show the same near $1/V_{gt}$ dependence as the simulations. The quantitative agreement between experiments and simulation is pretty good for the $W = 14$ nm device. The simulations miss the metal/semiconductor contact resistance, which is expected to appear as a rigid shift. The experimental data for the $W = 40$ nm device lie, as expected, between the simulations for the $W = 14$ nm device and for the planar (001) FDSOI device. The experimental data therefore support the main conclusions of this work about the dependence of the contact resistance on the gate bias and on the cross section.

## VI. Conclusion

We have computed the contact resistance $R_c$ of Trigate and FinFET devices using Non-Equilibrium Green's Functions. At low drain bias, $R_c$ can represent a very large fraction of the total resistance of these devices. The spacers between the heavily doped source/drain and the gate are the most resistive parts. The conductance under the spacers is typically limited by the poor electrostatic control over the charge density in these areas. As a consequence, the resistance of the spacers has a near $1/V_{gt}$ dependence, which, if not properly accounted for, can partly explain the apparent dependence of the channel mobility on length in short devices [13], [14], [15]. We have investigated the impact of the channel width $W$ and height $H$, and the impact of the source/drain doping profiles on the device performances.

## Acknowledgment

This work was supported by the French National Research Agency (ANR) project Noodles. The calculations were run on the TGCC/Curie machine thanks to allocations from PRACE and GENCI.

## References

[1] S. Datta, F. Assad, and M. Lundstrom, Superlattices and Microstructures 23, 771 (1998).
[2] M. Shur, IEEE Electron Device Letters 23, 511 (2002).
[3] S.-D. Kim, C.-M. Park, and J. Woo, IEEE Transactions on Electron Devices 49, 457 (2002).
[4] S. J. Park, D.-Y. Jeon, L. Monts, S. Barraud, G.-T. Kim, and G. Ghibaudo, Semiconductor Science and Technology 28, 065009 (2013).
[5] J.-S. Yoon, E.-Y. Jeong, S.-H. Lee, Y.-R. Kim, J.-H. Hong, J.-S. Lee, and Y.-H. Jeong, Japanese Journal of Applied Physics 54, 04DC06 (2015).
[6] S. Berrada, M. Bescond, N. Cavassilas, L. Raymond, and M. Lannoo, Applied Physics Letters 107, 153508 (2015).
[7] M. P. Anantram, M. S. Lundstrom, and D. E. Nikonov, Proceedings of the IEEE 96, 1511 (2008).
[8] R. Coquand, M. Cassé, S. Barraud, D. Cooper, V. Maffini-Alvaro, M. Samson, S. Monfray, F. Boeuf, G. Ghibaudo, O. Faynot, and T. Poiroux, IEEE Transactions on Electron Devices 60, 727 (2013).
[9] V. Nguyen, Y. Niquet, F. Triozon, I. Duchemin, O. Nier, and D. Rideau, IEEE Transactions on Electron Devices 61, 3096 (2014).
[10] Y.-M. Niquet, V.-H. Nguyen, F. Triozon, I. Duchemin, O. Nier, and D. Rideau, Journal of Applied Physics 115, 054512 (2014).
[11] C. Jacoboni and L. Reggiani, Reviews of Modern Physics 55, 645 (1983).
[12] R. Coquand, S. Barraud, M. Cass, P. Leroux, C. Vizioz, C. Comboroure, P. Perreau, E. Ernst, M.-P. Samson, V. Maffini-Alvaro, C. Tabone, S. Barnola, D. Munteanu, G. Ghibaudo, S. Monfray, F. Boeuf, and T. Poiroux, Solid-State Electronics 88, 32 (2013).
[13] D. Rideau, F. Monsieur, O. Nier, Y. Niquet, J. Lacord, V. Quenette, G. Mugny, G. Hiblot, G. Gouget, M. Quoirin, L. Silvestri, F. Nallet, C. Tavernier, and H. Jaouen, in 2014 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) (2014) pp. 101-104.
[14] M. Zilli, D. Esseni, P. Palestri, and L. Selmi, IEEE Electron Device Letters 28, 1036 (2007).
[15] V. Barral, T. Poiroux, D. Munteanu, J. Autran, and S. Deleonibus, IEEE Transactions on Electron Devices 56, 420 (2009).

# Analysis and Modelling of Temperature Effect on DIBL in UTBB FD SOI MOSFETs

A. S. N. Pereira[1,2], G. de Streel[1], N. Planes[3], M. Haond[3], R. Giacomini[2], D. Flandre[1] and V. Kilchytska[1]
[1]ICTEAM, Université catholique de Louvain, Louvain-la-Neuve, Belgium
[2]Department of Electrical Engineering, Centro Universitário da FEI, São Bernardo do Campo, Brazil
[3]STMicroelectronics, Crolles, France
*Email: ariannesoares@fei.edu.br*

***Abstract*— The Drain Induced Barrier Lowering (DIBL) behavior in Ultra-Thin Body and Buried oxide (UTBB) transistors is investigated in details in the temperature range up to 150ºC, for the first time to the best of our knowledge. The analysis is based on experimental data, physical device simulation, compact model (SPICE) simulation and previously published models. Contrarily to MASTAR prediction, experiments reveal DIBL increase with temperature. Physical device simulations of different thin-film fully-depleted (FD) devices outline the generality of such behavior. SPICE simulations, with UTSOI DK2.4 model, only partially adhere to experimental trends. Several analytic models available in the literature are assessed for DIBL vs. temperature prediction. Although being the closest to experiments, Fasarakis' model overestimates DIBL(T) dependence for shortest devices and underestimates it for upsized gate lengths frequently used in ULV (ultra-low-voltage) applications. This model is improved in our work, by introducing a temperature-dependent inversion charge at threshold. The improved model showed very good agreement with experimental data, with high gain in precision for the gate lengths under test.**

***Keywords*— *Fully-Depleted Silicon-On-Insulator (FD SOI); UTBB; DIBL; temperature dependence.***

## I. Introduction

The Ultra-Thin Body and Buried oxide (UTBB) SOI MOSFET is widely considered for future technology nodes thanks to its improved electrostatic and variability control [1]. The scalability of UTBB devices can reach the 8 nm node, considering DIBL (Drain Induced Barrier Lowering) values < 100 mV/V as the electrostatic criterion [1].

Studying the temperature effects in UTBB SOI MOSFETs is important even for room-temperature applications, as these devices can be affected by self-heating with channel temperature reaching ~ 100ºC under normal operation conditions [2-3]. In [4-5], the DIBL of 0.4-1.5 µm-long bulk Si MOSFETs showed increase with temperature and stronger dependence for shorter devices. For 28 nm long UTBB devices [6], an increase of DIBL by about 20 mV/V over 100°C was observed. However, in-depth analysis of DIBL evolution with temperature in such devices was not performed.

A.S.N. Pereira and R. Giacomini would like to thank FAPESP (process 2014/11627-7) and CNPq for the financial support. The work is partially funded by FNRS (Belgium), Eniac Places2be and Ecsel WAYTOGO FAST projects.

The present work investigates the experimental DIBL behavior and compares the observed results to physical simulations (Atlas), compact modelling (SPICE) and several published analytical models. In order to reproduce the experimental DIBL dependence on temperature, an upgrade of the most adequate model to date is proposed.

## II. Experimental Devices

The experimental devices were fabricated at ST Microelectronics [7], with a BOX thickness ($t_{BOX}$) of 25 nm and silicon body ($t_{Si}$) of 7 nm. The metal gate stack is composed of 2.3 nm of HfSiON with an equivalent oxide thickness ($t_{OX}$) of 1.3 nm. The measured devices are n-channel MOSFETs with gate lengths (L) from 34 to 500 nm and channel width (W) of 1 µm. The channel is left undoped. Both standard $V_T$ (STDVT) and low $V_T$ (LVT) devices were measured up to 150ºC.

## III. Results and Discussion

Fig. 1 shows the experimental DIBL as a function of temperature. The DIBL values were calculated from $\Delta V_G/\Delta V_D$, where $V_G$ is the gate voltage at the constant current value of $10^{-7}$.(W/L) for low drain voltage ($V_{DL}$) of 50 mV or high drain voltage ($V_{DH}$) of 1 V. The increase of DIBL with temperature can be clearly observed for both LVT and STDVT transistors. Moreover, this increase is stronger in shorter devices. DIBL values calculated using MASTAR software [8] are plotted on the same graph for the sake of comparison and are independent of temperature.

Fig. 2 presents the DIBL for different thin-film FD structures simulated with Atlas [9]. This simulation analysis aims at verifying whether some particular process features could generate such DIBL behavior. An ideal double gate (DG) structure was also studied to remove any possible channel position and substrate depletion effects. For all structures, the trend is the same as for experimental results of Fig. 1, highlighting that this DIBL behavior is physical and not specific to the measured UTBB devices.

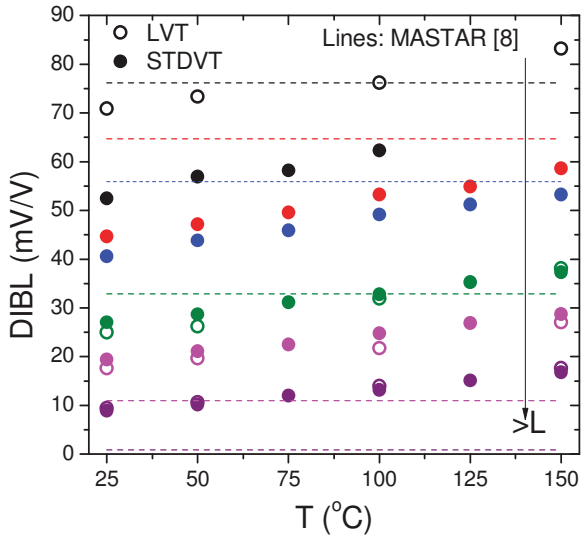



Fig. 1. Measured DIBL as a function of temperature for STDVT and LVT devices of different lengths.

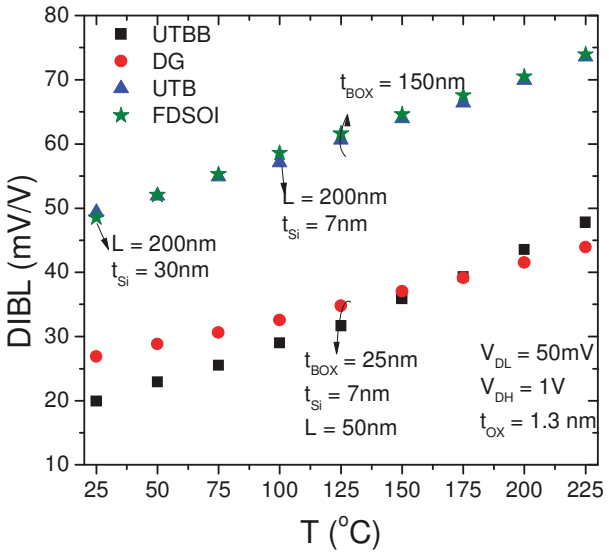



Fig. 2. DIBL as a function of temperature from Atlas simulations of different SOI structures.

Fig. 3 shows the DIBL variation with temperature from circuit-level simulations using UTSOI DK2.4 model from ST Microelectronics [10] compared to experimental data for devices with L of 42 and 60 nm. The UTSOI DK2.4 model qualitatively reproduces the experimental DIBL dependence on temperature for L = 60nm. However, the modeled DIBL(T) incorrectly lowers with reduced L and is underestimated for L=42nm.

We then assessed the ability of different analytic models to reproduce DIBL vs. temperature increase in UTBB devices. Fig. 4 shows the DIBL as a function of L for different models published in literature, for T = 25ºC (Fig. 4(a)) and T = 150ºC (Fig. 4(b)). Three models are considered: 1°) MASTAR software [8], which is based on Voltage Drop Transformation (VDT) model [11]; 2°) Arshad's model [12] an improved version of MASTAR model, which takes into account the effective length ($L_{EFF}$) and the mean channel position in the thin film ($Y_{MEAN}$); 3°) Fasarakis' model [13] which is a threshold voltage model, defining the DIBL as the difference between the $V_T$ for low and high drain voltage. Though MASTAR software can calculate the drain current and SCE (Short-Channel Effects) as a function of temperature, the DIBL equation does not include dependence on temperature (Fig. 1). Arshad's model can be adapted for different T by considering $L_{EFF}(T)$ and $Y_{MEAN}(T)$ extracted from simulations. The $Y_{MEAN}$ shifts towards bottom interface and $L_{EFF}$ becomes shorter with T increase. Both these trends naturally result in DIBL increase at higher T. However, incorporation of these dependences is not sufficient to reproduce actual DIBL(T) results. Fasarakis' model has a good accuracy for room temperature but deviates at higher temperature.

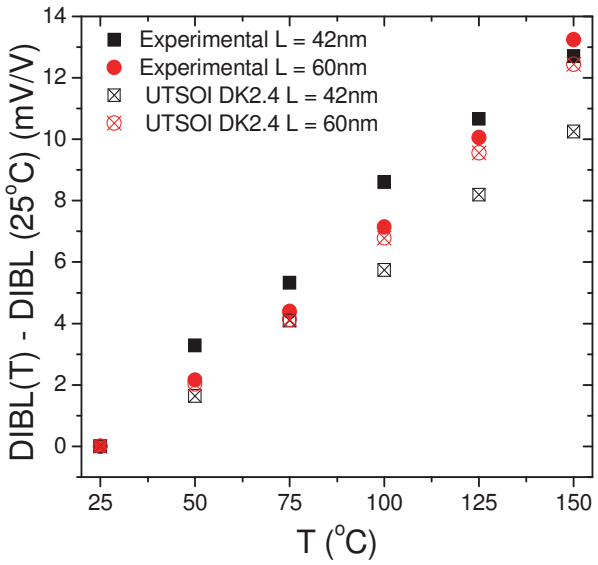
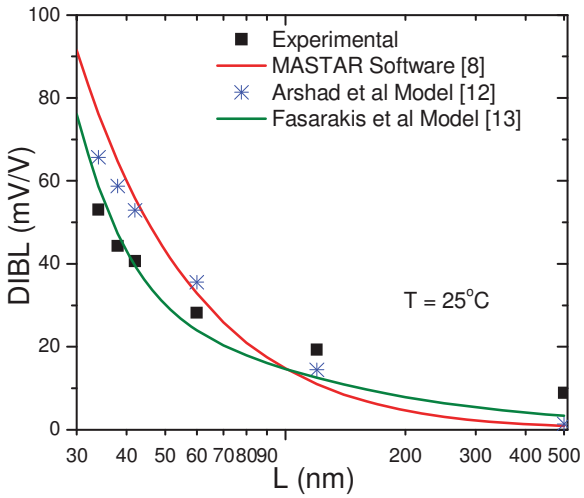


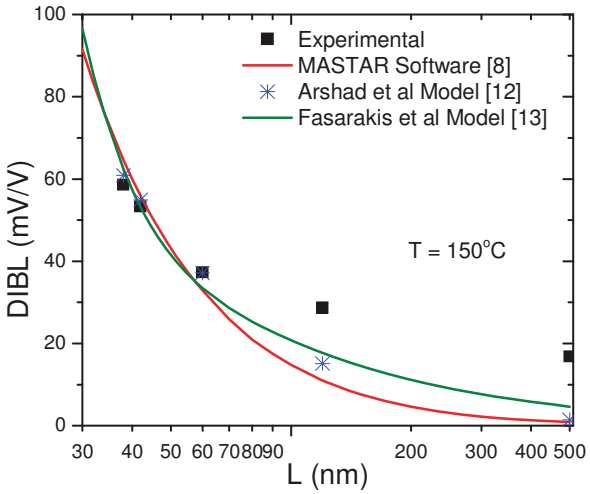

Fig. 3. DIBL increase with temperature for lengths of 42 and 60 nm from measurements and SPICE simulations.

Fig. 5 shows the ΔDIBL/ΔT as a function of L for measurements and the analytic models presented in Fig. 4. It can be noticed that both Arshad's and Fasarakis' model describe the trends, featuring enhanced DIBL vs T increase with L shortening. Fasarakis' model shows better results comparing to other models. However, it gives stronger dependence than experimentally observed one, particularly overestimating ΔDIBL/ΔT values in shorter devices and underestimating in long ones. The reason is that the temperature dependence of the inversion charge defined at the threshold condition ($Q_{TH}$) in Fasarakis' model was not taken into account. Hence, our proposal in this work is to extract the $Q_{TH}$ from Atlas electron concentration taking into account the $Y_{MEAN}$ for each temperature considering low and high drain biases. Then, we introduce these values in Fasarakis' original

model. The result is shown in Fig. 5, referred as "Fasarakis et al + $Q_{TH}$(T) dependence". It can be observed that the proposed upgraded model reproduces well the experimental data in the whole L range under consideration and can be used to estimate the temperature dependence of DIBL with temperature for UTBB devices. In some applications, especially ULV, the use of channel lengths above the minimal length of the technology is common to minimize current leakage [14] and to have better analog performance [15].




(a)




(b)

Fig. 4. DIBL as a function of channel length for temperatures of (a) 25ºC and (b) 150ºC.

Fig. 6 shows the comparison between Fasarakis' model and its improved version for the devices with L of 38 and 120nm. Notice that the proposed improvement is the most accurate with experimental data, presenting a precision gain of 35% for L=120nm. Such results show that the $Q_{TH}$ is significantly temperature dependent.

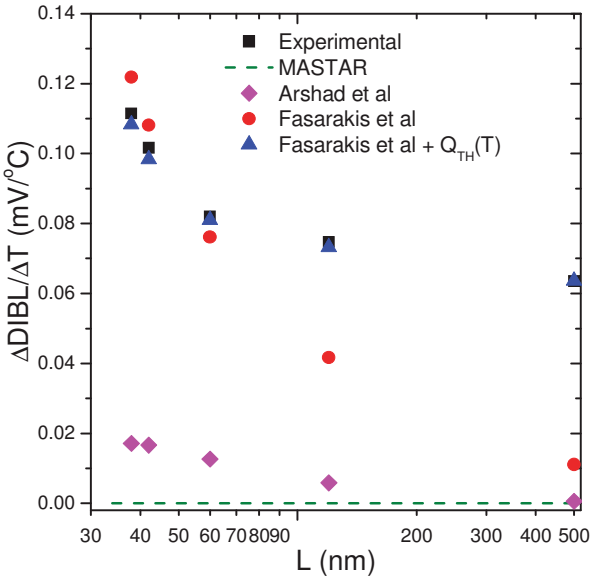



Fig. 5. ΔDIBL/ΔT up to 150ºC as a function of channel length.

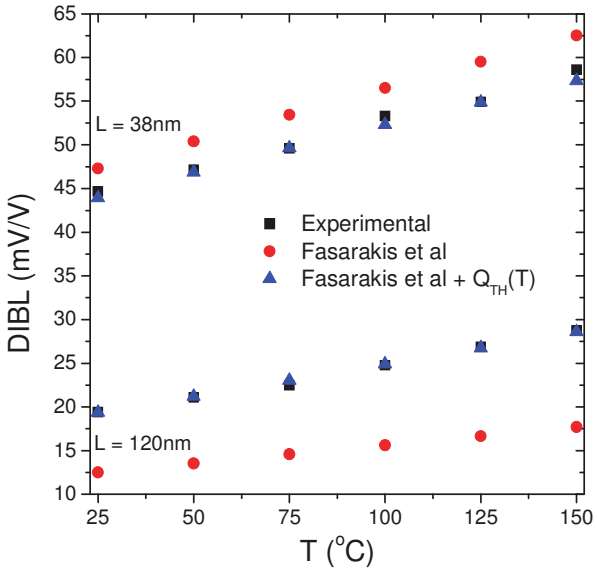



Fig. 6. DIBL as a function of temperature for the devices with L=38 and 120nm.

Fig. 7 shows the inversion charge ($Q_{TH}$) as a function of temperature for Fasarakis' model (lines) and the extracted values from simulations (symbols) used to generate DIBL values presented in Fig. 6. It can be observed that the $Q_{TH}$ values from Fasarakis' model do not have temperature

dependence. However, the extracted $Q_{TH}$ values are different for each temperature.

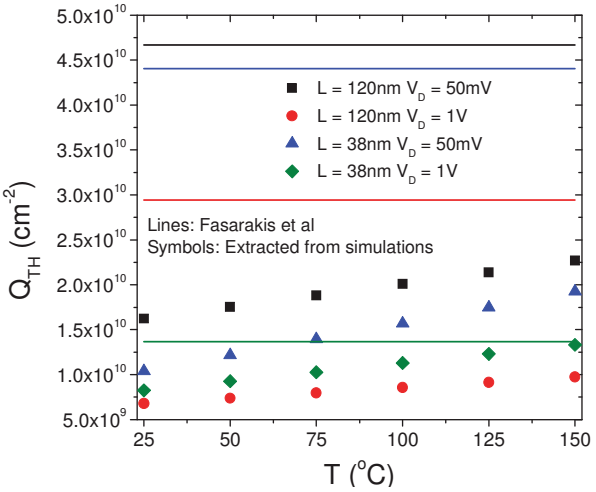



Fig. 7. $Q_{TH}$ as a function of temperature for Fasarakis' model and extracted from simulations for L = 38 and 120nm.

## IV. Conclusions

The DIBL dependence on temperature in UTBB FD SOI MOSFETs was analyzed. The experimental results revealed increase of DIBL with temperature. This trend is confirmed by both physical and SPICE simulations. The fact that physical devices simulation of different thin-film architectures provides the same trends emphasizes generality of such DIBL temperature behavior. Existing models, however, do not allow to reproduce DIBL(T) dependence properly. We proposed a way to upgrade the voltage model of Fasarakis et al, by including inversion charge (accounting for channel position) dependence on temperature in order to correctly reproduce/predict DIBL variation with temperature for devices with different lengths. The obtained results show very good agreement with experimental data and significant gain of precision for both shortest devices and for longer ones with channel lengths in the range used for low leakage ULV digital or good output conductance analog applications for this technology.

## References

[1] O. Faynot, F. Andrieu, O. Weber, C. Fenouillet-Béranger, P. Perreau, J. Mazurier, T. Benoist, O. Rozeau, T. Poiroux, M. Vinet, L. Grenouillet, J-P. Noel, N. Posseme, S. Barnola, F. Martin, C. Lapeyre, M. Cassé, X. Garros, M-A. Jaud, O. Thomas, G. Cibrario, L. Tosti, L. Brévard, C. Tabone, P. Gaud, S. Barraud, T. Ernst and S. Deleonibus. Planar Fully depleted SOI technology: A powerful architecture for the 20nm node and beyond, IEEE International Electron Devices Meeting (IEDM), p. 3.2.1-3.2.4, 2010.

[2] S. Makovejev, J.-P. Raskin, M. K. Md Arshad, D. Flandre, S. Olsen, F. Andrieu and V. Kilchytska. Impact of self-heating and substrate effects on small-signal output conductance in UTBB SOI MOSFETs, Solid State Electronics, vol. 71, p.93-100, 2012.

[3] M. A. Karim, Y.S. Chauhan, S. Venugopalan, A. B. Sachid, D. D. Lu, B. Y. Nguyen, O. Faynot, A. M. Niknejad and C. Hu. Extraction of Isothermal Condition and Thermal Network in UTBB SOI MOSFETs, IEEE Electron Device Letters, vol. 33, p.1306-1308, 2012.

[4] H. El Ghitani. DIBL Coefficient in Short-Channel NMOS Transistors, 16th National Radio Science Conference, p. D4.1-D4.5, 1999.

[5] B. Jharia, S. Sarkar and R. P. Agarwal. Controlling Factors of Drain Induced Barrier Lowering Coefficient in Short Channel MOSFET, WSEAS Transactions on Electronics, vol. 1, p.252-255, 2004.

[6] S. Makovejev, B. Kazemi Esfeh, J.-P. Raskin, D. Flandre, V. Kilchytska and F. Andrieu. Threshold Voltage Extraction Techniques and Temperature Effect in Context of Global Variability in UTBB MOSFETs, Proceedings of ESSDERC, p. 194-197, 2013.

[7] N. Planes, O. Weber, V. Barral, S. Haendler, D. Noblet, D. Croain, M. Bocat, P. Sassoulas, X. Federspiel, A. Cros, A. Bajolet, E. Richard, B. Dumont, P. Perreau, D. Petit, D. Golanski, C. Fenouillet-Beranger, N. Guillot, M. Rafik, V. Huard, S. Puget, X. Montagner, M.-A. Jaud, O. Rozeau, O. Saxod, F. Wacquant, F. Monsieur, D. Barge, L. Pinzelli, M. Mellier, F. Boeuf, F. Arnaud and M. Haond. 28nm FDSOI technology platform for high-speed low-voltage digital applications, Symposium on VLSI Technology (VLSIT), p. 133-134, 2012.

[8] T. Skotnicki et al. MASTAR 4 User's Guide, ST Microelectronics, 2011.

[9] Atlas User's Manual. Santa Clara: Silvaco, v. 5.16.3.R, 2010.

[10] O. Rozeau, M.-A. Jaud, T. Poiroux and M. Benosman. UTSOI Model 1.1.4 – Model Description, CEA-Leti, 2012.

[11] T. Skotnicki, C. Fenouillet-Beranger, C. Gallon, F. Boeuf, S. Monfray, F. Payet, A. Pouydebasque, M. Szczap, A. Farcy, F. Arnaud, S. Clerc, M. Sellier, A. Cathignol, J.-P. Schoellkopf, E. Perea, R. Ferrant and H. Mingam. Innovative materials, devices, and CMOS technologies for low-power mobile multimedia, IEEE Transactions on Electron Devices, vol. 55, p. 96–130, 2008.

[12] M. K. M. Arshad, J.-P. Raskin, V. Kilchytska, F. Andrieu, P. Scheiblin, O. Faynot and D. Flandre. Extended MASTAR Modeling of DIBL in UTB and UTBB SOI MOSFETs, IEEE Transactions on Electron Devices, vol. 59, p. 247-251, 2012.

[13] N. Fasarakis, T. Karatsori, D. H. Tassis, C. G. Theodorou, F. Andrieu, O. Faynot, G. Ghibaudo and C. A. Dimitriadis. Analytical Modeling of Threshold Voltage and Interface Ideality Factor of Nanoscale Ultrathin Body and Buried Oxide SOI MOSFETs With Back Gate Control, IEEE Transactions on Electron Devices, vol. 61, p. 969-975, 2014.

[14] D. Bol, G. de Streel and D. Flandre. Can We Connect Trillions of IoT Sensors in a Sustainable Way? A Technology/Circuit Perspective, IEEE S3S Conference, 2015.

[15] B. Kazemi Esfeh, V. Kilchytska, N. Planes, M. Haond, D. Flandre and J.-P. Raskin. Comparative Study of Parasitic Elements on RF FoM in 28 nm FD SOI and Bulk Technologies, IEEE S3S Conference, 2015.

# Using One-Dimensional Radiosity to Model Neutral Particle Flux in High Aspect Ratio Holes

Paul Manstetten*, Lado Filipovic†, Andreas Hössinger‡, Josef Weinbub*, and Siegfried Selberherr†
*Christian Doppler Laboratory for High Performance TCAD at the
†Institute for Microelectronics, TU Wien, Gußhausstraße 27-29/E360, 1040 Wien, Austria
‡Silvaco Europe Ltd., Compass Point, St Ives, Cambridge, PE27 5JL, United Kingdom
Email: manstetten@iue.tuwien.ac.at

***Abstract*—We present a computationally inexpensive one-dimensional method to model the neutral flux in high aspect ratio holes for three-dimensional plasma etching simulations. The benefit of our approach lies in the fact that the computational costs of a three-dimensional plasma etching simulation are, for the most part, determined by calculating the surface flux of the relevant species. We propose a one-dimensional radiosity model for the neutral flux by assuming an ideal cylindrical shape as well as ideal diffuse sources and surfaces. Our model reproduces the results obtained by a three-dimensional ray tracing simulation and is therefore suited to be used as a drop-in replacement for cylinder-like hole structures to speed up three-dimensional plasma etching simulations.**

## I. Introduction

During a plasma etching simulation the local fluxes of the etching species are used to model the surface reactions. The local flux must be recalculated for each simulation time step, because the interface positions are changing due to the evolving surface. For high aspect ratio (HAR) features, the local flux originating from re-emission is predominant and the local flux rates can easily vary by orders of magnitude along the feature depth.

Considering the computational costs of a three-dimensional plasma etching simulation, the calculation of the local flux is dominant. The efficient calculation of the neutral flux is therefore essential, especially considering the fact that HARs further increase this dominance, because with a high aspect ratio the average number of re-emission events per particle is also increased.

Common approaches for three-dimensional flux calculation are Monte Carlo ray tracing [1] and radiosity based [2] methods. Ray tracing supports bi-directional reflectance distribution functions, whereas radiosity inherently favors diffusely reflecting surfaces. The rotational symmetry allows to use a one-dimensional radiosity method which is intended to be a drop-in replacement for modeling the neutral flux in cylinder-like hole structures in three-dimensional simulations, with the benefit of decreased computational complexity.

In this work we consider an ideal cylindrical shape of the feature, a neutral flux source with an isotropic distribution, ideal diffuse reflections, and a flux-independent sticking probability $s$. Ballistic transport is assumed for the neutral particles. The diffuse re-emission mechanism is a common assumption for neutral particles [3] and cylinder-like shapes are a key prerequisite for HAR holes in the context of, for instance, three-dimensional NAND flash cell processing [4].

In the following sections, we first define our simulation domain with all relevant parameters (II-A) and explain the applied discretization (II-B); subsequently we describe how to adopt the general radiosity method to our problem (II-C) and how we compute the relevant view factors (II-D). We apply the Jacobi method to solve the resulting linear system of equations (II-E) and apply a normalization to the resulting flux distributions (II-F). Finally, we discuss the results (III) of our model and compare them with results obtained using a three-dimensional ray tracing simulation [5].

## II. One-Dimensional Radiosity for Cylindrical Holes

### A. Simulation Domain

The simulation domain (Fig. 1a) is a circular cylinder with its aspect ratio (AR) defined by $\frac{\text{depth}}{\text{diameter}}$. We model the source of neutral particles by an ideal diffusely-emitting disk closing the cylinder at the top without re-emission ($s = 1$). The wall of the cylinder is an ideal diffuse reflector with a constant sticking probability ($s = s_w$). The bottom of the cylinder does not have any re-emission ($s = 1$). This setup is a reasonable approximation for the neutral flux in a HAR plasma etching environment.

### B. Domain Discretization

Our approach is based on a subdivision of the cylinder into rotationally symmetric surface elements (Fig. 1b): The inner surface of the cylinder wall is sliced into $n_w$ cylinder rings with height $\frac{\text{depth}}{n_w}$ and the disk closing the cylinder at the bottom is divided into $n_b$ annuli with ring width $\frac{\text{radius}}{n_b}$. The disk closing the cylinder at the top is not subdivided, as it is fully adsorbing and the distribution of the flux leaving the cylinder at the top is not of interest.

### C. Applying the Radiosity Method

Our assumptions, particularly that all sources/surfaces are ideal diffuse and that the transport of the neutral particles is ballistic, allows to employ the radiosity method. By assuming a constant flux and a constant sticking probability over each surface element, the problem can be formulated using the

ISBN 978-1-4673-8608-1  IEEE Catalog number CFP1649D-USB

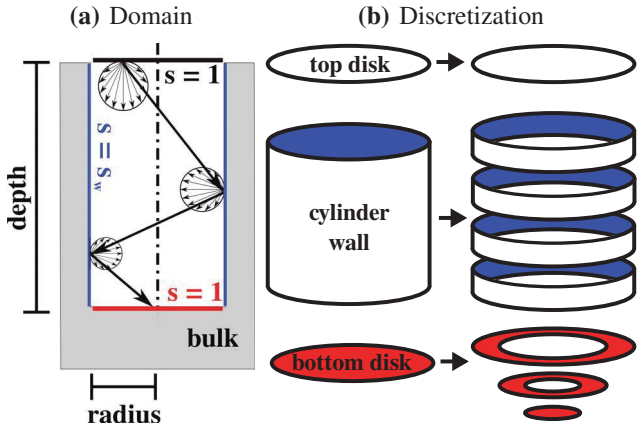



Fig. 1. (a) The simulation domain is decomposed into a fully adsorbing source (black), a partly adsorbing wall (blue), and a fully adsorbing bottom (red). (b) The wall and bottom are subdivided into ring elements. The top disk is not subdivided as the flux distribution leaving the cylinder is irrelevant.

discrete radiosity equation: for a surface element $i$ the equation reads

$$B_i = E_i + (1 - \alpha_i) \sum_j (F_{j \to i} B_j), \tag{1}$$

where $B$ is the radiosity (sum of emitted and reflected energy), E is the emitted energy, $\alpha$ is the absorptance and $F_{j \to i}$ is the view factor (proportion of the radiated energy which leaves element $j$ and is received by element $i$). We adapt (1) to our problem by substituting the absorptance $\alpha$ by the sticking probability $s$ and identifying the local flux as the adsorbed energy A. The radiosity $B$ is then related to the adsorbed energy $A$ by

$$A_i = (B_i - E_i) \frac{s_i}{1 - s_i}. \tag{2}$$

Since we are also interested in the adsorbed flux at the fully adsorbing bottom, (1) and (2) are not applicable because $\lim_{s_i \to 1} A_i = \infty$. For this reason we use the following formulation for the received energy $R$:

$$R_i = \sum_j (E_j F_{j \to i}) + \sum_j ((1 - s_j) R_j F_{j \to i}), \tag{3}$$

where the relation to the adsorbed energy is

$$A_i = R_i s_i. \tag{4}$$

Rewritten in matrix notation and resolved for the vector of received energies $R$ we obtain

$$\begin{aligned} \mathbf{F}^T \cdot E + \operatorname{diag}(1 - \mathbf{s})\, \mathbf{F}^T \cdot R &= R, \\ \left(\mathbf{I} - \operatorname{diag}(1 - \mathbf{s})\, \mathbf{F}^T\right) \cdot R &= \mathbf{F}^T \cdot E, \end{aligned} \tag{5}$$

with vectors of source energies $E$, a vector of sticking probabilities $\mathbf{s}$, and a matrix of view factors $\mathbf{F}$ (where entry $F_{ij}$ is the view factor from $i \to j$).

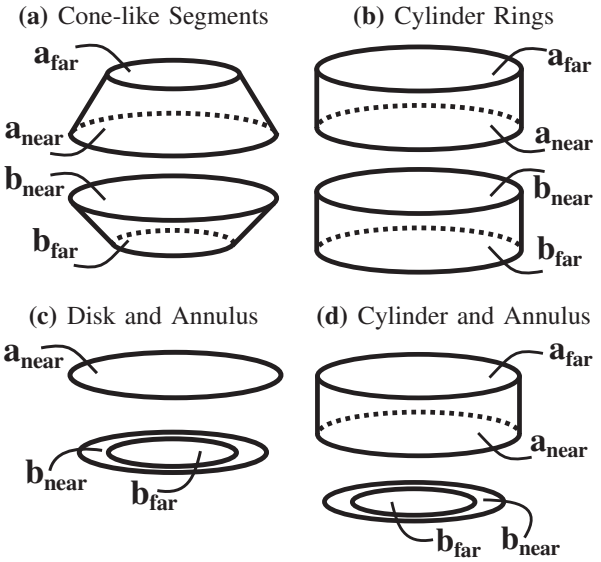



Fig. 2. (a) Configuration of two cone-like segments opened towards each other. The inner surfaces are mutually completely visible. (b) Configuration of two coaxial cylinder rings with the same radius. (c) Configuration of a disk and an annulus. (d) Configuration of a cylinder element and a annulus. The outer radius of the annulus is not greater than the cylinder radius.

### D. Computing the View Factors

To assemble the matrix $\mathbf{F}$ we need to evaluate the view factors between all possible pairs of surface elements. The view factor between two coaxial disks at a distance $z$ of unequal radii $r_1$ and $r_2$ is defined by

$$F_{1 \to 2} = \frac{1}{2} \left( X - \sqrt{X^2 - 4(R_1/R_2)^2} \right), \tag{6}$$

where $R_i = r_i/z$ and $X = 1 + (1 + R_2^2)/R_1^2$ [6]. Using this relation and the reciprocity theorem of view factors

$$S_1 \cdot F_{1 \to 2} = S_2 \cdot F_{2 \to 1} \quad (\text{with } S_i = Area_i), \tag{7}$$

we derive a general formula for a view factor between two cone-like segments whose surfaces are mutually completely visible.

$$F_{b_x \to a} = F_{b_x \to a_{near}} - F_{b_x \to a_{far}} \tag{8}$$

$$F_{a \to b_x} = \frac{S_{b_x}}{S_a} \cdot F_{b_x \to a} \tag{9}$$

$$F_{a \to b} = F_{a \to b_{near}} - F_{a \to b_{far}} \tag{10}$$

Fig. 2a shows the geometric configuration of two cone-like segments opened towards each other with mutually completely visible surfaces; the four limiting disks which enter Eqs. (8)-(10) are designated. Fig. 2b, Fig. 2d and Fig. 2c show the main types of configurations as they occur in our problem.

The view factors on the diagonal of $\mathbf{F}$ (i.e., the view factors of the elements to themselves) are computed by

$$F_{a \to a} = 1 - F_{a \to a_{near}} - F_{a \to a_{far}}. \tag{11}$$

If the element is a disk or annulus, the view factor to itself is zero.

To reduce the computational costs for assembling $\mathbf{F}$ we can make use of the fact that the cylinder rings are regular and the $(n_w)^2$ view factors amongst them can be affiliated with only $n_w$ different view factors, as only the relative distance matters. Reciprocity (7) allows the computation of the view factors in the upper triangle of $\mathbf{F}$ by using the view factors in the lower triangle and the element areas.

To prove a closed domain and as indicator for correctly computed view factors we compute the sum for each row of $\mathbf{F}$, which must always result in one.

### *E. Solving the Linear System of Equations*

We approximate the solution of the resulting diagonally-dominant linear system of equations (5) using the Jacobi method. Each iteration of the Jacobi method can be imagined as a concurrent diffuse re-emission of each element to all other elements. The adsorbed flux $A$ is obtained by multiplying the entries in the solution for $R$ with the corresponding sticking probability $s$ of the element (4). To reveal computational mistakes and to have an indicator for an equilibrium state the relation $\| A \| - \| E \| = 0$ can be applied; it holds for closed surfaces, e.g., our domain (the inner surface of a cylinder closed with two disks at the top and bottom).

### *F. Normalization*

To provide a good qualitative comparability we normalize the results to only depend on the aspect ratio of the hole and the sticking probability. The adsorbed flux $A$ is divided by the area of the element ($A_i^n = \frac{A_i}{S_i}$) and normalized to the flux which a surface of the same sticking probability would absorb if it is fully planar-exposed to the source ($A_i^{n_{src}} = \frac{A_i^n}{E_{i_{src}}^n \cdot s_i}$).

## III. Results

To evaluate the quality of our one-dimensional radiosity model, we analyze different simulation setups where we vary the sticking probability between $s_w = 0.02$ and $s_w = 0.2$; the top disk (source) and bottom disk are fully adsorbing for all of the following results.

Fig. 3 plots the normalized flux distribution along the wall and the at bottom for holes with ARs 5 and 45. The results show that the flux along the wall of a HAR hole decreases by several orders of magnitude, e.g., about five orders for AR=45 and one order for AR=5. The non-continuity of the sticking probability causes a jump at the wall-bottom interface. The effect of the fully adsorbing bottom is also visible in the wall flux distribution, which is most prominent for $AR = 45$ and $s = 0.02$, where a strong decrease towards the bottom interface is visible.

Fig. 4 compares the flux distributions for $AR = 5$ obtained using the proposed one-dimensional radiosity approach with results generated with a reference Monte Carlo ray tracing tool [5]. Similarly, Fig. 5 compares the flux distributions for $AR = 45$. The results show a good agreement, besides the deviation at the wall-bottom interface, caused by the discretization which is used in the ray tracing simulation. In Fig. 5a two flux distributions are plotted for the ray tracing results along the wall: they represent the minimum and maximum along the cylinder radius. The separation of the flux distributions, particularly visible for $s_w = 0.2$ (Fig. 5a), and the visible noise in Fig. 5b, reflect the stochastic nature of the ray tracing approach.

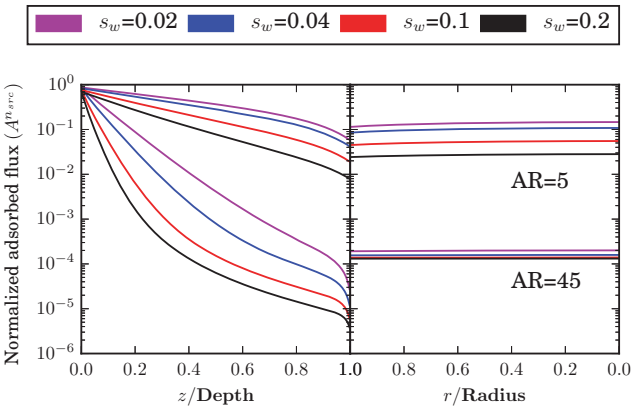



Fig. 3. Normalized flux distribution along the wall (left) and the bottom (right) of holes with aspect ratios AR=5 (upper group) and AR=45 (lower group). The sticking probability of the wall $s_w$ is varied from 0.02 to 0.2.

## IV. Summary and Outlook

We provide an approximation of the local neutral flux in three-dimensional plasma etching simulations of HAR holes using a one-dimensional radiosity approach. A radiosity formulation from a receiving perspective (3) is derived, which allows to model fully adsorbing surface elements. We compute all relevant view factors by establishing a general formula (10) between coaxial cone-like segments. Comparing the results for cylinders with ARs 5 and 45 using a rigorous three-dimensional Monte Carlo ray tracing simulation shows good agreement (Fig. 4a and Fig. 5b). Our radiosity model thus serves as a computationally inexpensive drop-in replacement for three-dimensional simulations.

Our approach allows for an extension of the model to handle any rotationally symmetric convex features.

## Acknowledgment

The financial support by the *Austrian Federal Ministry of Science, Research and Economy* and the *National Foundation for Research, Technology and Development* is gratefully acknowledged.

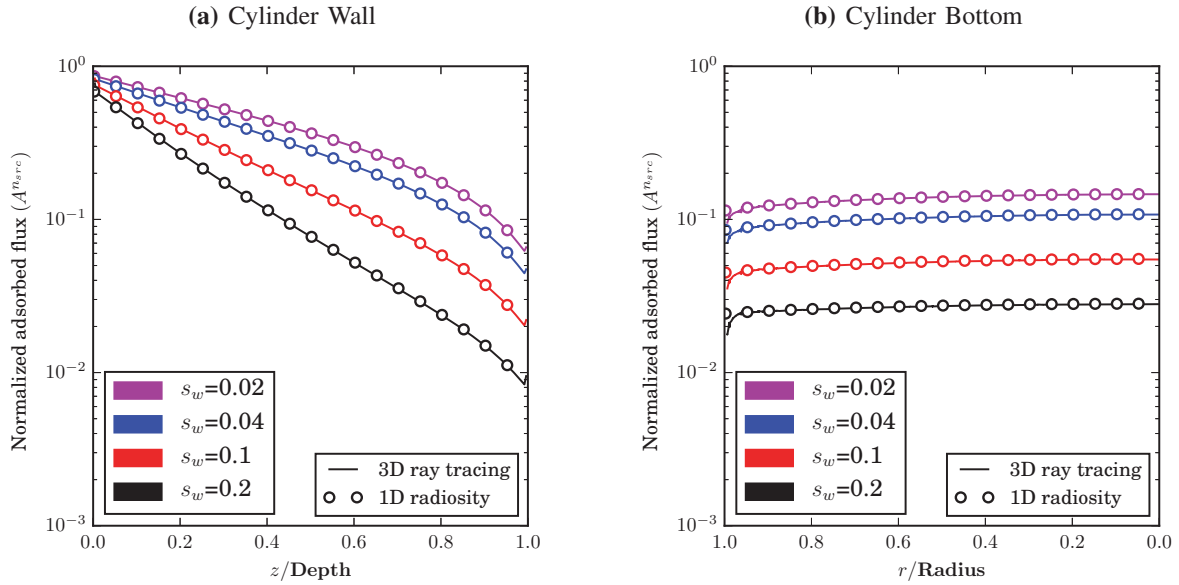



Fig. 4. Comparison of the results obtained by one-dimensional radiosity and three-dimensional raytracing for a hole with aspect ratio 5. The sticking probability of the wall $s_w$ is varied between 0.02 and 0.2. The differences are visible near the wall-bottom interface. (a) Normalized flux distribution along the wall. (b) Normalized flux distribution at the bottom.

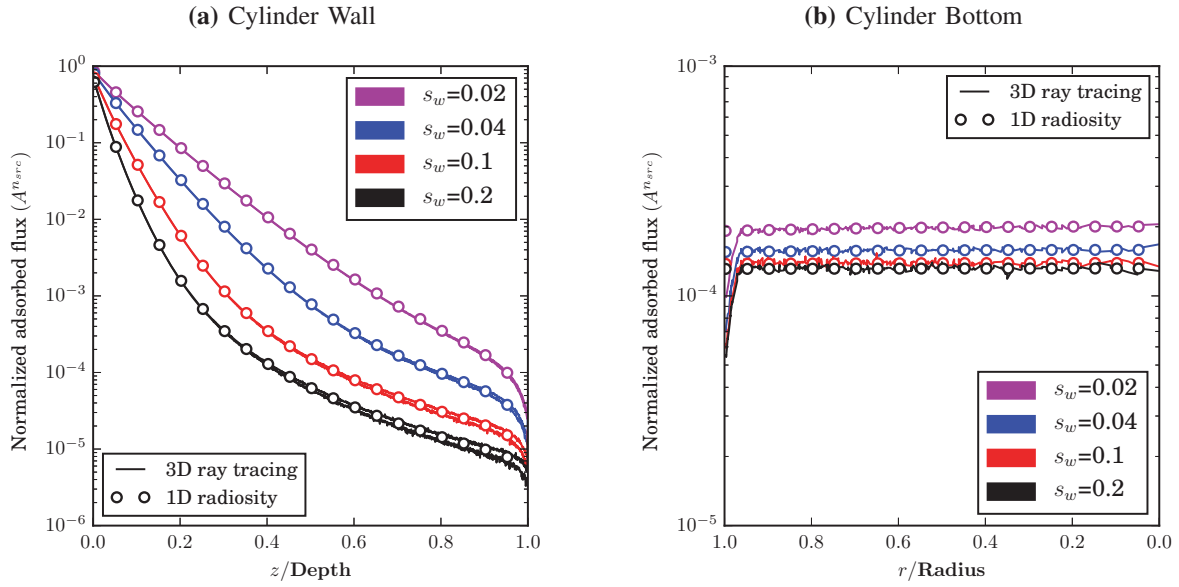



Fig. 5. Comparison of results obtained by one-dimensional radiosity and three-dimensional raytracing for a hole with aspect ratio 45. The sticking probability of the wall $s_w$ is varied between 0.02 and 0.2. The differences are visible near the wall-bottom interface. The ray tracing results reveal noise over the entire domain. (a) Normalized flux distribution along the wall. Along the depth, the minimum and maximum ray tracing results are plotted; the difference increases towards the bottom interface. (b) Normalized flux along the bottom.

## References

[1] O. Ertl and S. Selberherr, "Three-Dimensional Level Set Based Bosch Process Simulations Using Ray Tracing for Flux Calculation," *Microelectronic Engineering*, vol. 87, no. 1, pp. 20–29, 2010.

[2] T. Ikeda, H. Saito, F. Kawai, K. Hamada, T. Ohmine, H. Takada, and V. Deshpande, "Development of $SF_6/O_2$/Si Plasma Etching Topography Simulation Model Using New Flux Estimation Method," in *Proceedings of the 2011 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, 2011, pp. 115–118.

[3] G. Kokkoris, A. G. Boudouvis, and E. Gogolides, "Integrated Framework for the Flux Calculation of Neutral Species Inside Trenches and Holes During Plasma Etching," *Journal of Vacuum Science & Technology A*, vol. 24, no. 6, pp. 2008–2020, 2006.

[4] P. Dimitrakis, *Charge-Trapping Non-Volatile Memories: Volume 1 – Basic and Advanced Devices*. Springer, 2015.

[5] O. Ertl, L. Filipovic, and J. Weinbub, "ViennaTS," https://github.com/viennats/viennats-dev, 2015.

[6] M. F. Modest, *Radiative Heat Transfer*. Academic Press, 2013.

# SOI platform for spin qubits

S. De Franceschi, R. Maurand, A. Corna, D. Kotekar-Patil, X. Jehl, M. Sanquer
*Univ. Grenoble Alpes, F-38000 Grenoble, France & CEA, INAC-PHELIQS, F-38000 Grenoble, France*

R. Lavieville, L. Hutin, S. Barraud, M. Vinet
*CEA/LETI, MINATEC Campus, F-38000 Grenoble, France*

Y.-M. Niquet
*Univ. Grenoble Alpes, F-38000 Grenoble, France & CEA, INAC-MEMS, F-38000 Grenoble, France*

***Keywords—Silicon on Insulator; Spin Qubits; Quantum Computation***

The first few decades of the previous century have witnessed a revolution in the physical sciences due to the advent of quantum mechanics. Now, a hundred years later, quantum mechanics is about to drive a new revolution in technology. As a matter of fact, quantum mechanical phenomena have already found numerous applications in different areas (metrology, sensing, imaging, etc.). Atomic clocks and superconducting quantum interference devices (used for magnetometry), are just a few examples of commercial quantum devices. Yet these examples can be regarded as basic-level quantum technology. The next step is to exploit the inherent complexity of quantum systems, whose origin lies in the basic principle of superposition, namely the property of a quantum object to be simultaneously in two or more possible states. If we consider the simplest case of a quantum particle, e.g. an electron, with two possible states, say state '0' and state '1', the superposition principle allows for that particle to be in both 0 and 1 at the same time (see Fig. 1 and corresponding caption). In a way, a quantum particle can thus encode much more information than a classical device (e.g. a transistor) with only two possible states. A second key property of quantum particles is their ability to couple among each other without necessarily requiring reciprocal interaction. This property, known as quantum entanglement together with the principle of superposition, forms the key elements of quantum information processing. They result in a naturally built-in parallelism that could be exploited to achieve computational powers unaffordable by any classical computer.

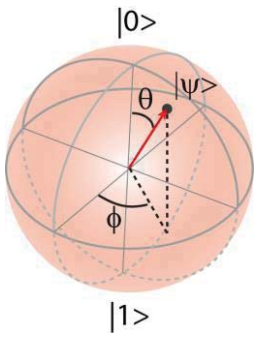



Figure 1: Geometric representation of a spin qubit state. In a magnetic field, say along the z axis, the two-fold spin degeneracy of a spin-1/2 particle, say an electron, is lifted resulting in two energy states, $|0\rangle$ and $|1\rangle$, corresponding to parallel and antiparallel orientation of the particle magnetic moment, respectively. The energy splitting between $|0\rangle$ and $|1\rangle$, the so-called Zeeman energy, is equal to $|g\mu_B B|$, where $g$ is the particle gyromagnetic factor, $\mu_B$ the Bohr magneton, and B the magnetic field amplitude. Quantum mechanics allows for the particle spin state $|\psi\rangle$ to generically be in an arbitrary combination of $|0\rangle$ and $|1\rangle$, i.e. $|\psi\rangle = a_0|0\rangle + a_1|1\rangle$, where $a_0$ and $a_1$ are complex numbers that can be expressed in terms of the polar coordinates $(\theta,\varphi)$. (Note: $|a_0|^2$ and $|a_1|^2$ correspond to the probabilities of finding the qubit in state $|0\rangle$ and $|1\rangle$, respectively. Therefore, $|a_0|^2 + |a_1|^2 = 1$.) As a result, a quantum two-level system such as a spin-1/2 particle carries much more information than a classical two level system, whose states can be represented by a single binary digit.

What could one do with a quantum computer? Since the concept of quantum computing was proposed in the early eighties, this basic question has been the subject of intensive studies. In 1994, Peter Shor proposed an algorithm that would allow a quantum computer to factorize large integer numbers, in principle much larger than those affordable by the most powerful classical computer [1]. This apparently futile application of quantum computing may have a significant impact on society, since integer factorization is currently at the core of most cryptography systems (e.g. the RSA cryptosystem). As suggested by Nobel Prize winner Richard Feynman, a quantum computer would allow the simulation of quantum phenomena (e.g. chemical processes), well beyond what can be afforded by classical computers [2]. This would likely have many applications, e.g. providing guidelines for the development and engineering of new materials, chemical reactions, etc. The list of already known possible applications of quantum computation could be continued with several other examples. However the entire impact that quantum computer may actually have remains hard to predict. In his well-known, visionary lecture about "nanoscience", entitled "There is plenty of room at the bottom" [3], Richard Feynman said at some point: "I can't see exactly what would happen, but I can hardly doubt that when we have some control of the arrangement of things on a small scale we will get an enormously greater range of possible properties". A similar argument holds for the quantum computer, since it is very likely that we will discover its full potential only after getting it to work.

Quantum computation and quantum communication represent the holy grail of quantum technology, and hence one of the most ambitious technological challenges today. Their realization, regardless of the approach or type of material system, implies putting together many different quantum

ingredients and facing a variety of new problems at both scientific and engineering level. If up till now quantum computing devices have been a matter for basic experimental research, it is fair to say that we have reached the point where their further development requires resources well beyond those owned by small academic-level laboratories. The increasing complexity of quantum circuits demands larger scale research efforts combining a wide range of competences, from quantum science to material science, nanotechnology, engineering, circuit design, etc.

What do we need to make a quantum computer? This question is addressed in an article by David DiVincenzo, where he identifies five key requirements, now known as the DiVincenzo criteria [4]:

1. A scalable physical system with well characterized qubits
2. The ability to initialize the state of the qubits to a simple fiducial state
3. Long relevant decoherence times, much longer than the gate operation time
4. A "universal" set of quantum gates enabling the implementation of any quantum algorithm.
5. Individual qubit readout, i.e. the ability to measure specific qubits.

Qubits can be made out of a large variety of material systems. When it comes to a crucial issue such as large-scale integration, however, the range of possible choices becomes much narrower. To this respect, solid-state qubits are in principle well positioned. Among solid-state approaches, qubits based on superconducting elements have so-far reached the most advance level of development. Recently, research teams at UCSB-Google, QuTech, and IBM were able to implement the first fault-tolerant devices consisting of 9, 5, and 4 superconducting qubits, respectively [5-7]. These devices, in which quantum errors can be detected and corrected, may become the building blocks of larger scale quantum computing architectures.

An alternative solid-state approach relies on semiconducting elements. Here the elementary bit of quantum information is encoded in a spin degree of freedom, such as the magnetic moment of an electron or that of a nucleus [8,9]: Though the development of spin qubits has been lagging behind, recent experimental breakthroughs have sparked a renewed interest. Last year, an Australian research team showed that an electron spin qubit defined in an isotopically purified $^{28}$Si crystal exhibits exceptionally long coherence times, $T_2$, ranging from 30 ms to 0.5 s! [10, 11] (This is much larger than in superconducting qubits where the coherence time, limited by energy relaxation processes, is at most around 100 μs). In essence, $T_2$ is the characteristic time over which a spin, thought of as a (quantum) oscillator, loses its (quantum) phase due to uncontrolled interactions with its environment. For electron-spin qubits the critical interactions come from the nuclear magnetic moments of the host crystal, which explains the enormous benefit of isotopic purification ($^{28}$Si, which happens to be by far the most abundant isotope, has zero nuclear spin thereby causing no hyperfine interaction).

In addition to long coherence times, silicon spin qubits have other potential advantages. The first one is size: a spin qubit with its readout device can be comfortably fitted within a square micron (superconducting qubits are typically made of superconducting waveguide resonators whose size is about a square millimeter). The second advantage lies in the inherent compatibility with silicon technology. The exceptional control on the fabrication processes of silicon devices is definitely an asset for qubit large-scale integration. In addition, qubits may be straightforwardly coupled to CMOS-based on-chip electronics for qubit driving and readout. Owing to the above-mentioned properties, silicon spin qubits provide one of the most promising pathways to scalable quantum computers.

Silicon-based spin qubit devices reported so far were fabricated on either bulk silicon [10-12] or SiGe heterostructures [13, 14]. In all cases, several metal electrodes were deposited on the semiconductor surface in order to define and electrically control the qubit. Extending these approaches to large-scale integrated quantum circuits will imply exporting the developed device fabrication processes onto an industrial silicon technology platform.

Our approach towards silicon spin-qubit devices is different. It consists in using an industry-standard CMOS platform from the start. More specifically, we rely on the 300-mm silicon-on-insulator (SOI) technology available in Grenoble. As a first important step, we aim at elaborating on the design and fabrication processes of silicon nanowire transistors in order to transform them into fully functional spin qubit devices. Low device complexity with minimal control and readout overhead will be a leading paradigm in the development of CMOS spin qubits. We believe this is important for future up scaling to complex quantum computing circuits. Minimizing the number of gates per qubit down to one or two is desirable and, to our view, feasible.

The ability to couple qubits to each other and to tune their coupling in time is another essential requirement for the realization of a quantum computer. In the first instance, tunable coupling is required for the implementation of two-qubit quantum gates. So far, direct spin-spin coupling was shown for the case of two electron spins sitting on adjacent silicon quantum dots [12], up to the recent demonstration of the first silicon-based C-NOT quantum gate [15]. In this case, the spin-spin coupling mechanism relies on direct (short-range) exchange interaction. Some ideas for long-range coupling schemes have been proposed but remain to be experimentally tested. In the prospect of developing spin qubit devices, some important progress has been made over the last few years. We have shown that:

1. At low temperature (i.e. below a few degree Kelvin), tri-gate nanowire transistors can be operated as quantum dots hosting only one or a few electrons [16](see Fig. 2). This achievement is relevant to the first DiVincenzo's criterium.

ISBN 978-1-4673-8608-1  IEEE Catalog number CFP1649D-USB

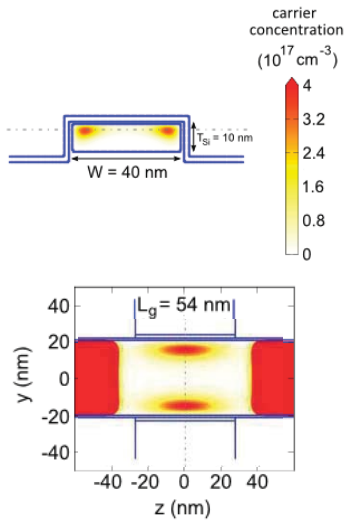



Figure 2: Calculated carrier distribution in the channel of a trigate SOI transistor showing charge accumulation in the upper edges of the channel. Top panel: cross-sectional view perpendicular to the channel axis. Bottom panel: top view. The calculation, based on self-consistent nonequilibrium Green' s functions and the effective-mass approximation, is carried out for a gate voltage just above threshold yielding an integrated carrier density of only one electron in the channel volume. For a channel width W = 40 nm the two electron 'pockets' have negligible overlap (top panel). In the case of long spacers, electrons are confined also along the longitudinal axis resulting in

2. In the specific case of hole-confinement quantum dots, a promising possibility exists for performing fast electrically driven spin resonance. This possibility, which is pertinent to the forth DiVincenzo's criterium, arises from the anisotropy and the gate dependence of hole g-factors [17]. More details are given in Fig. 3 and relative caption.

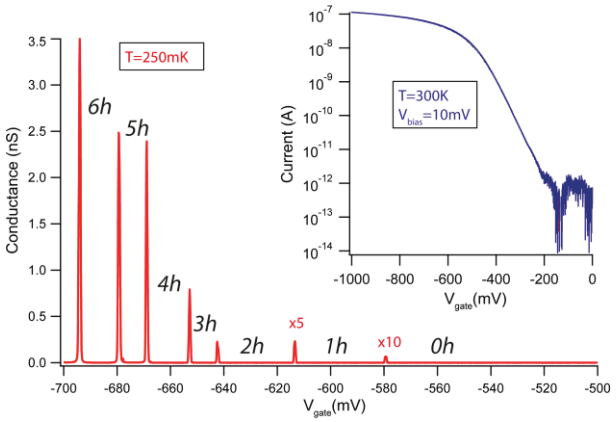



Figure 3: Hole transport in a p-type trigate transistor. Measured differential conductance taken at zero bias as a function of gate voltage (Vg) at a temperature of T = 4 K showing Coulomb oscillations (×5 and ×10 indicate that the corresponding current peaks have been multiplied by, respectively, 5 and 10 times for visibility). Inset shows the transistor characteristic, current versus Vg at room temperature at Vb = 10 mV. The subthreshold slope close to 60 mV per decade indicates an excellent electrostatic control.

3. Both n-type and p-type dual-gate transistors (such as the one shown in Fig. 4) can be tuned to a regime where they operate as double dot devices. Some first signatures of the Pauli spin blockade effect, useful for spin read-out, have been observed (unpublished).

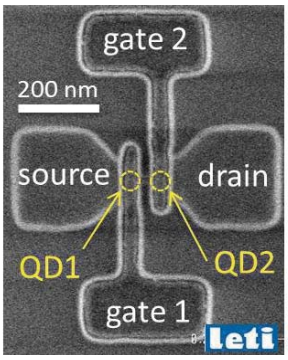



Figure 4: SEM micrograph of a dual-gate transistor. The gates have been fabricated with e-beam lithography. At low temperature, two quantum dots can be formed by charge accumulation below gates 1 and 2.

## ACKNOWLEDGMENT

The authors acknowledge financial support from the European Community's Seventh Framework under the Grants No. 323841 (http://www.sispin.eu/), No. 610637 (http://www.the-siam-project.eu/), and the ERC Starting Grant HybridNano. The NEGF calculations were run at the TGCC/Curie machine using allocations from PRACE and GENCI.

## REFERENCES

[1] P. W. Shor, Proc. Found. Comput. Sci. 124 (1994).
[2] R. P. Feynman, Int. J. Theor. Phys. **21**, 467 (1982).
[3] R. P. Feynman, Engineering and Science 22–36 (1960)
[4] D. P. Divincenzo, Fortschr. Phys. **48**, 771 (2000).
[5] J. Kelly et *al.*, Nature **519**, 66 (2015).
[6] D. Ristè et *al,* Nat. Commun. **6**, 6983 (2015).
[7] A. D. Córcoles et *al.,* Nat. Commun. **6**, 6979 (2015).
[8] D. Loss and D. P. Divincenzo, Phys. Rev. A **57**, 120 (1998).
[9] B. E. Kane, Nature **393**, 133 (1998).
[10] M. Veldhorst et *al.*, Nat. Nanotechnol. **9**, 981 (2014).
[11] J. T. Muhonen et *al.*, Nat. Nanotechnol. **9**, 986 (2014).
[12] J. J. Pla et *al.*, Nature **489**, 541 (2012).
[13] B. M. Maune et *al.*,Nature **481**, 344 (2012).
[14] E. Kawakami et *al.*, Nat. Nanotechnol. **9**, 666 (2014).
[15] M. Veldhorst et al., Nature 0 (2015).
[16] B. Voisin et *al.*, Nano Lett. **14**, 2094 (2014).
[17] B. Voisin et al., Nano Lett. **16**, 88 (2016).

# First RF Characterization of InGaAs Replacement Metal Gate (RMG) nFETs on SiGe-OI FinFETs Fabricated by 3D Monolithic Integration

V. Deshpande, V. Djara, E. O'Connor, D. Caimi, M. Sousa, L. Czornomaz and J. Fompeyrine
IBM Zurich Research Laboratory,
Säumerstrasse 4, CH-8803 Rüschlikon,
Switzerland

P. Hashemi, K. Balakrishnan

IBM T.J.Watson Research Center,
1101 Kitchawan Rd., Route 134 Yorktown Heights, NY,
USA

***Abstract*— We report the first RF characterization of short-channel replacement metal gate (RMG) InGaAs-OI nFETs built in a 3D Monolithic (3DM) CMOS process. This process features RMG InGaAs-OI nFET top layer and SiGe-OI fin pFET bottom layer. We demonstrate state-of-the-art device integration on both levels. The bottom layer SiGe-OI pFETs are fabricated with a Gate-First (GF) process with fins scaled down to ~15 nm width and featuring epitaxial raised source drain (RSD) and silicide. The top layer InGaAs nFETs are fabricated with a RMG process featuring a self-aligned epitaxial raised source drain (RSD). We show that the 3D monolithic integration scheme does not degrade the performance of the bottom SiGe-OI pFETs owing to an optimized thermal budget for the top InGaAs nFETs. From the RF characterizations performed (post-3D monolithic process) on multifinger-gate InGaAs-OI nFETs, we extract a cut-off frequency ($F_t$) of 16.4 GHz at a gate-length ($L_g$) of 120 nm. Measurements on various gate lengths shows increasing cut-off frequency with decreasing gate-length.**

***Keywords—3D Monolithic; InGaAs; RMG; High-frequency; FinFET***

## I. INTRODUCTION

3D Monolithic (3DM) integration is attracting much attention owing to density scaling benefits and the potential to stack independently optimized multifunctional layers at transistor level [1]. However, due to the inherently high thermal budget of Si MOSFET process, Si(Ge)-on-Si 3DM integration scheme faces major challenges in top layer optimization without degrading bottom layer performance. This necessitates development of low temperature top layer Si/SiGe process which presents further challenges to obtaining high-performance MOSFETs on top layer. As the InGaAs MOSFET processing thermal budget is significantly lower, it is well-suited to be used as the top layer channel material. Moreover, InGaAs also has higher mobility which enables high performance at lower voltages and is also a widely used material for high-frequency devices. This aspect is of great interest as it can enable RF devices required for high-frequency analog or mixed signal circuits integrated on top of Si/SiGe MOSFETs and can provide transistor level granularity. As a step towards such a multi-functional 3D monolithic integration, here, we show RF characteristics of InGaAs nFETs fabricated with RMG process on top of SiGe-OI finFETs. We perform RF characterization of InGaAs-OI nFETs of various gate-lengths designed with optimized 'multi-finger gate' layout to enable efficient characterization. We demonstrate a cut-off frequency of 16.4 GHz for gate length ($L_g$) of 120 nm. Also, cut-off frequency is shown to increase with decreasing gate-lengths. We also demonstrate that the impact of 3DM integration on the bottom pFET performance is negligible, despite the top nFET RMG process featuring a self-aligned raised source drain epitaxy (with relatively high thermal budget). Thus we demonstrate the robustness of the InGaAs-on-SiGe 3DM integration.

## II. DEVICE FABRICATION

The 3DM process flow is shown in Fig. 1. Firstly, bottom layer SiGe-OI fin pFETs are fabricated with a gate-first (GF) process as in [2, 3]. The process begins with thinning of silicon layer of an 8 inch SOI wafer followed by Ge condensation to obtain SiGe-OI layer (with ~25% Ge content). Then active pFET areas are patterned and gate stack (with high-k dielectric and metal gate) is deposited. This is then followed by gate patterning and spacer deposition. After forming the spacers with anisotropic dry etching, in-situ doped SiGe epitaxy is carried out to form self-aligned raised source drain (RSD) regions. Then NiPt salicidation (self-aligned

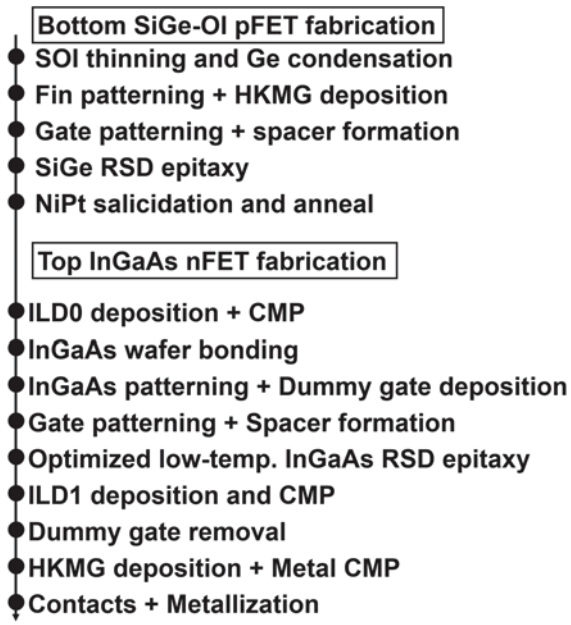



Fig. 1. InGaAs-on-SiGe 3D Monolithic integration process flow.

silicidation) is performed to obtain low contact resistivity on the pFETs. This silicide sets the thermal budget limit for the top nFET processing. The top layer nFET fabrication starts after this silicidation step of SiGe-OI finFET process. It begins with InGaAs layer transfer on top of processed pFETs. Firstly, the inter-layer oxide is deposited and chemical-mechanical-polish (CMP) planarization is carried out. The InGaAs layer is transferred on to this oxide with direct wafer bonding from 2 inch InP donor wafers [4]. InGaAs nFET fabrication is now performed with the RMG process described in [5]. This involves patterning the active transistor regions followed by a dummy gate stack deposition. After patterning the dummy gate, spacers are formed on either side similar to the bottom pFET process. Then comes the critical step of self-aligned in-situ doped InGaAs epitaxy to form RSD regions. This step has relatively high thermal budget and therefore, has been optimized to minimize the process temperature while obtaining high doping in the layer as described in [6]. RMG process steps follow thereafter. An oxide layer is first deposited and planarized to expose the top of dummy gate. Then the dummy gate stack is selectively etched out. An optimized high-k/metal gate stack [5] is deposited followed by metal CMP. Finally, oxide encapsulation is deposited and contact holes are opened to both top and bottom layers. Metallization is completed to create contact pads for both layers.

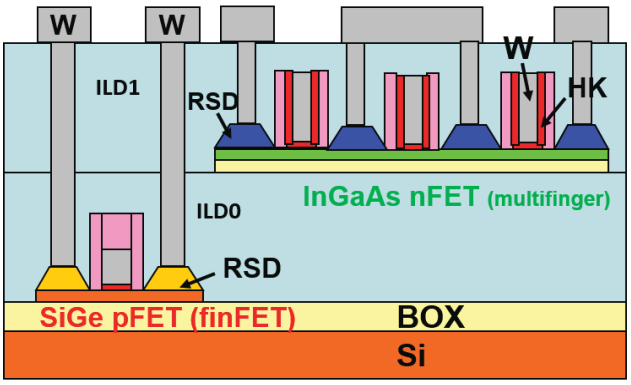



Fig. 2. Schematic of the InGaAs-on-SiGe 3DM stack showing multi-finger gate nFETs on top layer.

The schematic of the so completed 3D monolithic stack is shown in Fig. 2.

The layout of InGaAs nFETs on top layer used for RF characterization features multi-finger gate structures as shown in Fig. 2. This allows lowering the gate-resistance owing to multiple parallel gates. Also, the layout of devices characterized in this work has dense features with gate-to-contact spacing of 100 nm.

## III. Electrical Characterization

Fig. 3 shows the DC $I_d$-$V_g$ characteristics of a top InGaAs planar nFET with $L_g$ = 120 nm. This device features 10 finger gates in parallel and is so designed to enable RF characterization with coplanar waveguide pad structures. DC characteristics show competitive electrostatic control with drain-induced-barrier-lowering (DIBL) of 100 mV/V and $SS^{sat}$ = 100 mV/dec due a scaled high-k gate stack with CET of 1.6 nm and low $D_{it}$ [5]. Fig. 4 shows the $I_d$-$V_d$ characteristics for the same device. Fig. 5

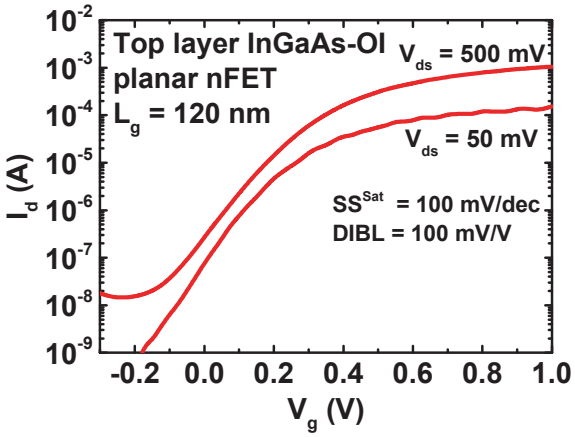



Fig. 3. DC $I_d$-$V_g$ characteristics of top layer InGaAs-OI planar nFET with $L_g$ = 120 nm.

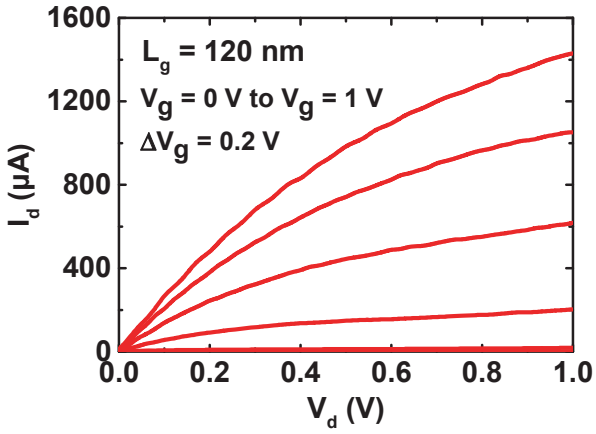



Fig. 4. DC $I_d$-$V_d$ characteristics of InGaAs-OI top layer planar nFET with $L_g$ = 120 nm.

shows the $I_d$-$V_g$ characteristics of the bottom layer SiGe-OI finFET with $L_g$ = 36 nm and fin width ~ 15 nm, before (black-dash) and after (blue-solid) top nFET fabrication. Owing to the lower thermal budget of the top layer InGaAs process, very minimal impact is observed on the bottom pFET, even for a scaled gate length. Nearly the same drain current ($I_d$) is maintained at both linear and saturation regime in the pFET indicating no degradation of the bottom silicide. RF characterization of the top nFET is performed on the devices with 10 parallel finger gates, each with a width of 2 µm (= total width of 20 µm), and having a ground-signal-ground (GSG) pad configuration. LRRM calibration with a vector-network-analyzer (VNA) is first carried on a standard reference calibration substrate, to move the reference plane to probe tips. Dedicated on-chip 'open' pad structures are used to de-embed the device. S-parameters are measured from 45 MHz to 40 GHz. From the measured S-parameters, current gain (|h21|) is calculated and shown

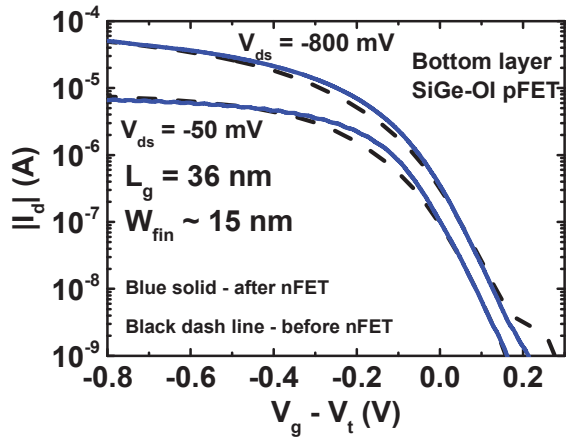



Fig. 5. Comparison of $I_d$-$V_g$ characteristics of bottom layer SiGe-OI pFET before and after top nFET fabrication.

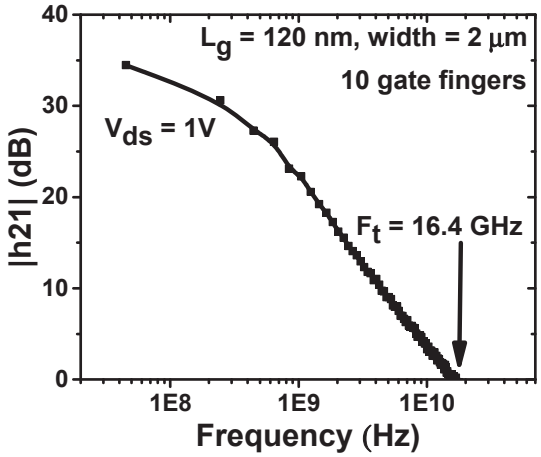



Fig. 6. Measured current gain (|h21|) vs. frequency for a InGaAs nFET (top layer) with $L_g$ = 120 nm and 10 parallel gate fingers. Cut-off frequency ($F_t$) of 16.4 GHz is obtained for $V_{ds}$ = 1V.

in Fig. 6, for a device with $L_g$ = 120 nm. A cut-off frequency ($F_t$) of 16.4 GHz is obtained for $V_{ds}$ = 1V. Lower $F_t$ value is probably due to higher access resistance in the device and high parasitic capacitance between the gate-source/drain contacts due to short separation of 100 nm. Cut-off frequency vs. $L_g$ plotted in Fig.7 shows an increase in cut-off frequencies with decreasing $L_g$. Scaling down $L_g$ further, along with improving access resistance and a relaxed gate-contact spacing could provide a way to increase the cut-off frequency.

## IV. Conclusion

We show, for the first time, RF characterization of InGaAs RMG nFETs fabricated on top of SiGe-OI finFETs in 3D Monolithic integration. A cut-off

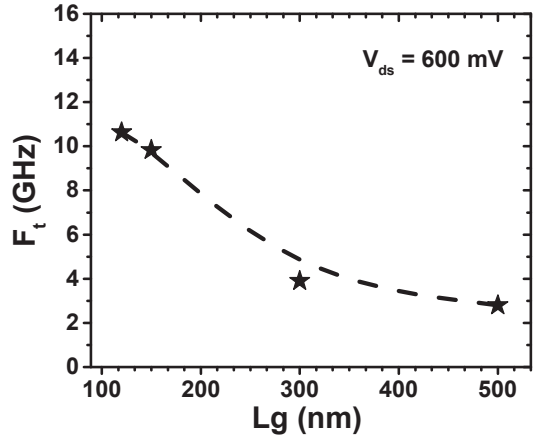



Fig. 7. Cut-off frequency vs. gate length ($L_g$) for top InGaAs nFETs for $V_{ds}$ = 600 mV.

frequency of 16.4 GHz is obtained for $L_g$ = 120 nm nFET with negligible impact on the bottom pFET performance. The InGaAs nFETs also feature a scaled gate stack and tight pitch design (gate-contact spacing = 100 nm). Thus we demonstrate the benefit of InGaAs-on-SiGe 3D monolithic integration, showing that independently optimized multi-functional layers can be fabricated exploiting the advantages of both device layers.

## ACKNOWLEDGMENT

Funding from the EU is acknowledged under the following EU and Marie-Curie projects: ICT-2013-11 COMPOSE3, ICT-2013-11 IIIVMOS, H2020-ICT-2015-688784-INSIGHT and PEOPLE-2013-IEF FACIT. Authors also acknowledge the IBM MRL and BRNC staff as well as management support at both sites.

## REFERENCES

[1] P. Batude, *et al.*, pp. 166-167, VLSI Tech. Symp. (2009).
[2] P. Hashemi, *et al.,* pp. 66-71, VLSI Tech. Symp. (2013).
[3] P. Hashemi, *et al.,* pp.1-2, VLSI Tech. Symp. (2014).
[4] L. Czornomaz, *et al.*, pp. 23.4.1 - 23.4.4, IEDM (2012).
[5] V. Djara, *et al.*,pp. T176 – 177,VLSI Tech. Symp. (2015).
[6] V. Deshpande, *et al.*, 8.8, IEDM (2015).

# A Sharp-Switching Gateless Device ($Z^3$-FET) in Advanced FDSOI Technology

H. El Dirani [1, 2], Y. Solaro [2], P. Fonteneau [1], C. A Legrand [1], D. Marin-Cudraz [1], D. Golanski [1], P. Ferrari [2], S. Cristoloveanu [2]
[1] STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles Cedex, France
[2] Univ. Grenoble Alpes, IMEP-LAHC, Grenoble INP Minatec, CNRS, F-38000 Grenoble, France
*hassan.eldirani1@st.com*

***Abstract*—A systematic study of a novel band modulation device ($Z^3$-FET: Zero gate, Zero swing slope and Zero impact ionization) fabricated in most advanced Fully Depleted Silicon-On-Insulator technology is presented. Since the device has no front gate, the operation mechanism is controlled by two buried ground planes. Characteristics such as sharp switching, low leakage, and controllable triggering are measured and discussed. We explore several variants (thin and thick silicon film) and show promising results in terms of high current and switching performance.**

***Keywords—Fully Depleted Silicon-On-Insulator (FDSOI); Zero Impact Ionization, Zero Gate and Zero subthreshold slope FET ($Z^3$-FET); Sharp Switch; Electro-Static Discharge (ESD).***

## I. Introduction

Devices with ultra-thin silicon film on insulator (UTSOI) attract increasing attention for RF and IoT applications. Fully Depleted Silicon On Insulator technology (FDSOI) features high performance by reducing the parasitic capacitances, varying the threshold voltage with back-gate biasing, improving the leakage, mobility and subthreshold swing (SS) [1, 2]. In addition, this technology benefits from simpler (planar) manufacturing process than FinFETs, offering lower power consumption at reduced cost [3, 4]. First introduced at the CMOS 28 nm node [1], the $Z^3$-FET [5] (Zero gate, Zero swing slope and Zero impact ionization) is a band-modulation device, like FED [6–8] and $Z^2$-FET [9–11], but without top gates. It exhibits vertical switch, low leakage current ($I_{Leak}$), tunable triggering voltage ($V_{t1}$), and high ON current ($I_{ON}$). For better electrostatic control, improved power consumption and pursuing the CMOS scaling down, it has been proposed in [12] to decrease the BOX and silicon film thickness with some constraints on the electrodes (S/D). The impact of these parameters on our devices will be discussed. The device has no front gate and is operated with the back-gate voltage applied on two independent ground planes (GP).

The paper is organized as follows. First, the architecture description and the operation principle of $Z^3$-FET, in advanced FDSOI technology [12], are presented. Then, we discuss the performance of our device with DC measurements. Finally, the high current performance is explored by TLP measurements.

## II. Device Structure and Operation Principle

The $Z^3$-FET is a forward biased P-I-N diode with an undoped ultra-thin silicon film ($t_{Si}$ = 6 nm, Fig. 1a). The source ($N^+$ doped) is grounded and the drain ($P^+$ doped) is positively biased ($V_A$ > 0 V). Sharp switching is controlled by two separated ground planes that act as back-gates (GP-N/P in Fig. 1). The heavily doped GPs are respectively positively (GP-N) and negatively (GP-P) biased, which keeps the device in OFF state by forming potential barriers and blocks the injection of electrons (from $N^+$ source) and holes (from $P^+$ drain) into the body. The two GPs induce 'electrostatic' doping within the body which emulates a virtual NPNP thyristor structure. The placement and the biasing of the two ground planes is selected to form adequate injection barriers while maintaining the buried $N^+/P^+$ diode underneath the BOX in reverse mode for low leakage current. The triggering is achieved by increasing the anode voltage. When $V_A$ reaches $V_{t1}$, a positive feedback mechanism occurs due to the flow of carriers from the anode to the cathode and vice versa, leading to a sudden collapse of barriers. This band-modulation mechanism results in remarkable sharp transition from low to high current, enabling an $I_{ON}/I_{OFF}$ ratio of 8 decades (Figs. 2, 4). Comparing to $Z^2$-FET, the $Z^3$-FET does not have high-k metal gate stack which eliminates any issues related to high voltage reliability. The free surface can be functionalized for various applications like bio and light sensing. Another important feature of $Z^3$-FET that benefits from the BOX as a gate oxide is the ability of sustaining high back-gate bias.

Three variants have been fabricated. The first one has an ultra-thin silicon film ($t_{Si}$ = 6 nm), Fig. 1a. The second (Fig. 1b) and the third (Fig. 1c) variants feature thicker Si film ($t_{Si}$ = 12 nm). The $L_n$ part of the third variant received light doping. All structures have thin buried oxide ($t_{BOX}$ = 20 nm) and fixed width (300 µm).

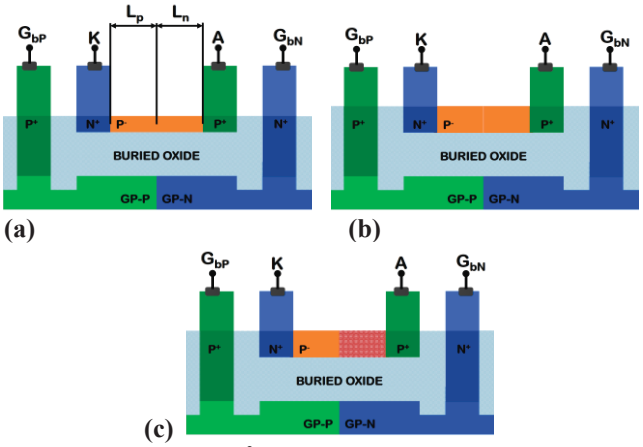



**Fig. 1.** Schematic of $Z^3$-FET architecture in advanced FDSOI technology: (a) $t_{Si}$ = 6nm, (b) $t_{Si}$ = 12nm and (c) partially N-doped channel.

## III. DC Leakage Characteristics and Triggering

Typical output characteristics with sharp switch, low leakage current and tunable $V_{t1}$ are presented in Figs. 2-4. The ultrathin device features a very low leakage current ($I_{Leak} < 10^{-11}$ A) in OFF state but no sharp switch (SS = 60 mV/dec, Fig. 2a). The feedback between the barriers is affected by the silicon film thickness. In this case, the recombination rate of carriers increases, as dominated by the interfaces, and the effective carrier lifetime decreases. Numerical simulations with reduced carrier lifetime confirm the degradation of switch sharpness [5]. In order to consolidate the barriers and recover the feedback mechanism between them, the film thickness has been increased from 6 nm up to 12 nm leading to a steep switch (Fig. 2b). Moreover, the GPs serve in tuning the triggering voltage. In long devices ($L_p = L_n = 200$ nm) with ultrathin film, the $L_p$ barrier is strong enough even at $V_{GbP} = 0$ V preventing the injection of electrons (Fig. 2a), while with thicker $t_{Si}$ it is needed to reinforce the electrons barrier by negatively biasing the GP-P ($V_{GbP} = -2$ V), as shown in Fig. 2b.

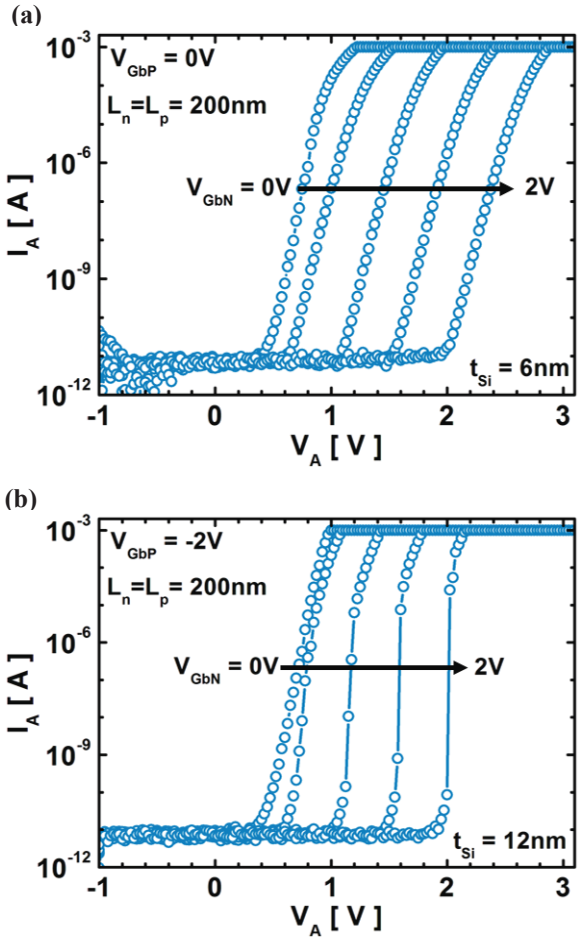



**Fig. 2.** Experimental DC $I_A$-$V_A$ characteristics for variable GP-N voltage and $V_{GbP} = -2$V. $Z^3$-FET ($L_n = L_p = 200$nm) with (a) $t_{Si} = 6$nm (slow switch) and (b) $t_{Si} = 12$nm (sharp switch).

As $V_{GbN}$ increases, the holes injection barrier is stronger, hence a higher $V_{t1}$ is needed to turn on the device. The evolution of triggering voltage with $V_{GbN}$ is presented in Figs. 3a-b, showing that $V_{t1}$ is very sensitive to the back-gate bias ($\Delta V_{t1}/\Delta V_{GbN} = 900$ mV/V). For ultrathin $t_{Si}$, the device length has a modest effect on the triggering voltage $V_{t1}$ (Fig. 3a). On the other side, short devices with thicker $t_{Si}$ are blocked at $V_{GbP} = -2$ V and feature a sharp switch in long devices but with reduced triggering voltage $V_{t1}$.

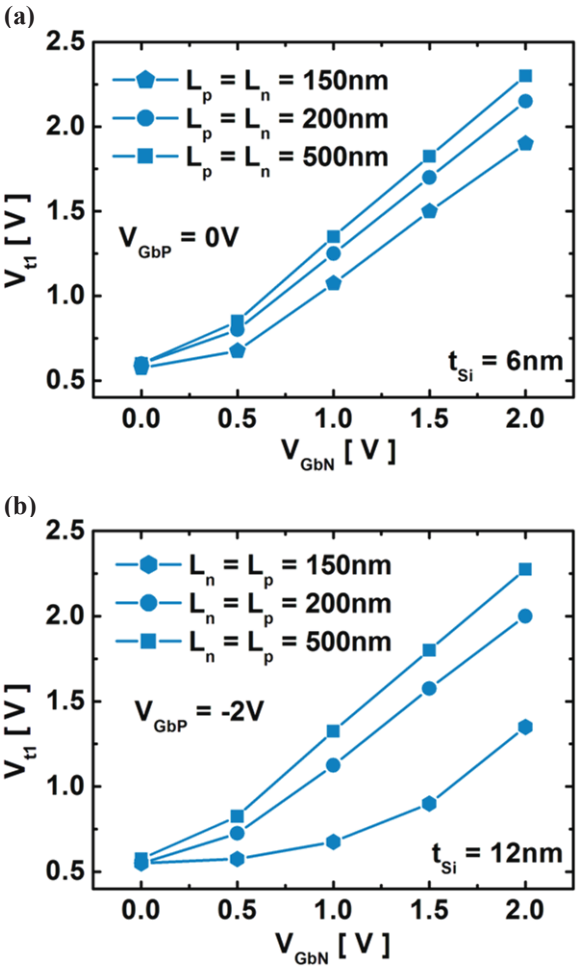



**Fig. 3.** Variation of triggering voltage $V_{t1}$ with GP-N bias for (a) $t_{Si} = 6$nm at $V_{GbP} = 0$V and (b) $t_{Si} = 12$nm at $V_{GbP} = -2$V.

The $I_A$-$V_A$ characteristics of the doped variant are presented in Fig. 4. The $L_n$ part of the channel is highly doped (N-type) forming a natural strong injection barrier avoiding the positive bias of the GP-N. By contrast, the $L_p$ region is left undoped and shows a strong dependence on GP-P bias (Fig. 4b). Thanks to the channel doping, the device is blocked without back-gate bias. In short devices, the GP-N barrier is narrow and cannot prevent completely the pass of holes into the cathode. Since at $V_{GbP} = 0$ V the GP-P barrier is weak the leakage current is higher. In order to decrease the leakage, two solutions are used. The first one is by increasing the device length (Fig. 4a). The second is by negatively biasing the GP-P (Fig 4b). In long devices, where the barriers are broader and higher, the triggering voltage increases as shown in Fig. 4a.

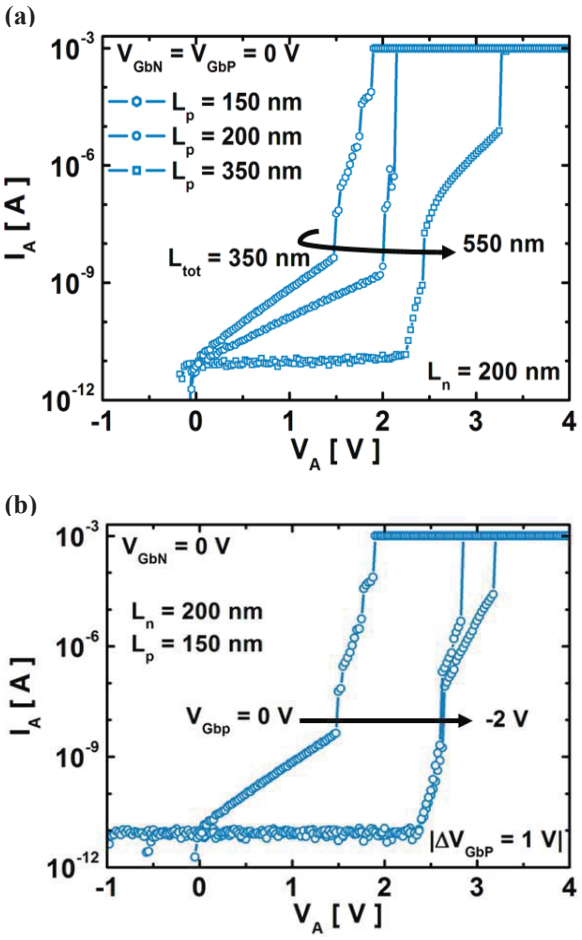



**Fig. 4.** Current versus drain voltage measured (a) for different geometries at $V_{GbN} = V_{GbP} = 0V$ and (b) for $L_n = 200nm$, $L_p = 150nm$ at $V_{GbN} = 0V$ and various $V_{GbP}$. Doped $Z^3$-FETs with $t_{si} = 12nm$.

## IV. TLP Measurements

The ESD behavior was investigated with transmission line pulse characterizations (TLP) [13, 14] for different pulse width ($t_{PW}$ = 5&100 ns) and native rise time (~300 ps) in OFF state. The high current regime is dominated by self-heating where the temperature rise limits the mobility and eventually leads to thermal runaway causing device breakdown. As noticed in Fig. 5, the heating is reduced for shorter pulse widths, where the failure current $I_{t2}$ of short $Z^3$-FET ($L_p = L_n$ = 200 nm) is improved from 4.9 mA/µm for $t_{pw}$ = 100 ns up to 7.6 mA/µm for $t_{pw}$ = 5ns. The maximum current value and the triggering voltage $V_{t1}$ change from a device to another according to its length. Shorter devices show improved performance: easier triggering with smaller $V_{t1}$ and higher current capability (Fig. 5).

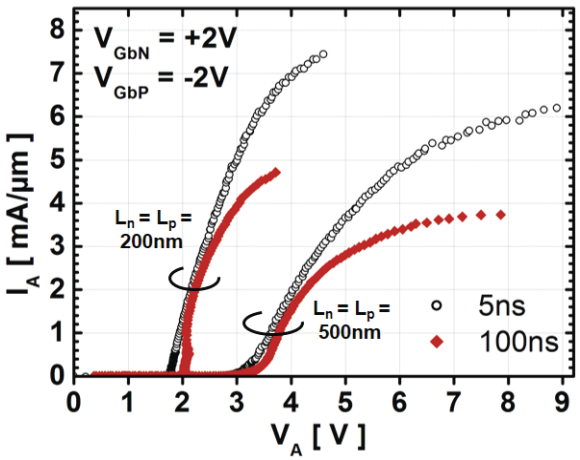



**Fig. 5.** TLP characterization results ($I_A$-$V_A$) for 5ns pulse width (open symbols) and 100ns (closed symbols) with native rise time (~300ps). $L_p = L_n$ is 200nm and 500nm. $V_{GbN}$ = 2V and $V_{GbP}$ = -2V. $t_{Si}$ = 12nm.

Fig. 6 shows an S-shaped negative-resistance characteristic for the partially N-doped device with no back-gate bias which is an important feature for ESD chip designers. Compared to undoped device with the same length ($L_p = L_n$ = 200 nm), the doped $Z^3$-FET exhibits a higher triggering voltage ($V_{t1}$ = 2.5 V in Fig. 6) but slightly reduced failure current $I_{t2}$ = 7.2 mA/µm. Regrettably, the dynamic resistance $R_{ON}$ is increased in doped devices due to the high recombination rate in the channel.

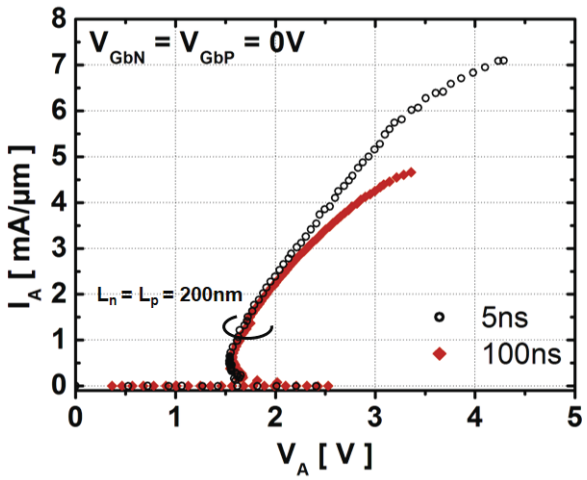



**Fig. 6.** TLP $I_A$-$V_A$ characteristics for 5ns and 100ns pulse width and native rise time ~300ps. N-doped $Z^3$-FET with $L_p = L_n$ = 200nm and $V_{GbN} = V_{GbP} = 0V$. $t_{Si}$ = 12nm.

Fig. 7 confirms that the triggering voltage of the device is tunable by GP bias and device length. The barrier formed by GP-N is strengthened at $V_{GbN}$ = 2 V and the higher the $|V_{GbP}|$ bias, the larger the triggering voltage. Thus our devices are able to fulfill the ESD design window requirements, showing ultra-low leakage current and adjustable triggering voltage capability.

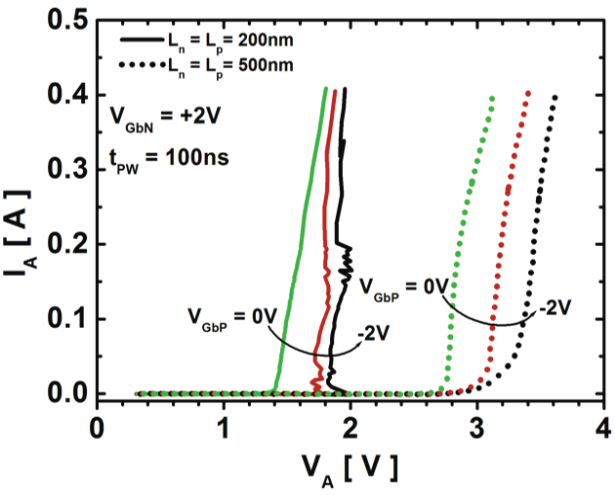



**Fig. 7.** Non-destructive TLP measurements for 100ns pulse width with ~ 300ps rise time: $I_A$-$V_A$ for $V_{GbN}$ = 2V and various $V_{GbP}$. $Z^3$-FET with $L_p = L_n = 200nm$ (solid lines) and $L_p = L_n = 500nm$ (dotted lines). $t_{Si}$ = 12nm.

## V. Conclusion

For the first time, a gateless band-modulation device ($Z^3$-FET) was demonstrated experimentally in most advanced FDSOI technology. Several variants with different silicon film thickness and doping level were studied. Performances in terms of triggering, leakage current and failure current have been reported. Thanks to the absence of the top gate, the $Z^3$-FET can serve as a robust ESD protection element and also as ion-sensitive, photo-sensitive and memory devices.

## Acknowledgment

The layout, process and ESD/LU teams of STMicroelectronics are thanked for helpful support and fruitful discussions. We also thank the European project WayToGoFast for financial support.

## References

[1] N. Planes, O. Weber, V. Barral, S. Haendler, D. Noblet, et al., "28nm FDSOI technology platform for high-speed low-voltage digital applications," *Dig. Tech. Pap. - Symp. VLSI Technol.*, vol. 33, no. 4, pp. 133–134, 2012.

[2] O. Faynot, F. Andrieu, O. Weber, C. Fenouillet-Béranger, P. Perreau, et al., "Planar fully depleted SOI technology: A powerful architecture for the 20nm node and beyond," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 50–53, 2010.

[3] S. Y. Wu, C. Y. Lin, M. C. Chiang, J. J. Liaw, J. Y. Cheng, et al., "A 16nm FinFET CMOS technology for mobile SoC and computing applications," *Int. Electron Devices Meet.*, pp. 9.1.1–9.1.4, 2013.

[4] F. Arnaud, N. Planes, O. Weber, V. Barral, S. Haendler, et al., "Switching energy efficiency optimization for advanced CPU thanks to UTBB technology," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 48–51, 2012.

[5] Y. Solaro, P. Fonteneau, C. A. Legrand, P. Ferrari, and S. Cristoloveanu "A sharp-switching device with free surface and buried gates based on band modulation and feedback mechanisms," *Solid-State Electron.,* in press

[6] F. Raissi, "A brief analysis of the field effect diode and breakdown transistor," *IEEE Trans. Electron Devices*, vol. 43, no. 2, pp. 362–365, 1996.

[7] Y. Yang, A. A. Salman, D. E. Ioannou, and S. G. Beebe, "Design and optimization of the SOI field effect diode (FED) for ESD protection," *Solid. State. Electron.*, vol. 52, no. 10, pp. 1482–1485, 2008.

[8] Y. Yang, A. Gangopadhyay, Q. Li, and D. E. Ioannou, "Scaling of the SOI Field Effect Diode (FED) for memory application," *2009 Int. Semicond. Device Res. Symp. ISDRS '09*, pp. 9–10, 2009.

[9] J. Wan, S. Cristoloveanu, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu "A feedback silicon-on-insulator steep switching device with gate-controlled carrier injection," *Solid. State. Electron.*, vol. 76, pp. 109–111, 2012.

[10] Y. Solaro, J. Wan, P. Fonteneau, C. Fenouillet-Beranger, C. Le Royer, A. Zaslavsky, P. Ferrari, and S. Cristoloveanu, "Z2-FET: A promising FDSOI device for ESD protection," *Solid. State. Electron.*, vol. 97, pp. 23–29, 2014.

[11] H. El Dirani, Y. Solaro, P. Fonteneau, P. Ferrari, and S. Cristoloveanu, "Sharp-Switchin $Z^2$-FET Device in 14 nm FDSOI Technology," in *European Solid-State Device Conf. ESSDERC*, pp. 250–253, 2015.

[12] O. Weber, E. Josse, F. Andrieu, A. Cros, E. Richard, P. Perreau, E. Baylac, N. Degors, C. Gallon, E. Perrin, S. Chhun, E. Petitprez, S. Delmedico, J. Simon, and G. Druais, "14nm FDSOI Technology for High Speed and Energy Efficient Applications," *Vlsi*, pp. 14–15, 2014.

[13] J. E. Barth, K. Verhaege, L. G. Henry, and J. Richner, "TLP calibration, correlation, standards, and new techniques," *Electron. Packag. Manuf. IEEE Trans.*, vol. 24, no. 2, pp. 99–108, 2001.

[14] T. Maloney and N. Khurana, "Transmission Line Pulse Technique For Circuit Modeling of ESD Phenomena," in *proc; 7th EOS/ESD Symposium, 1985, pp. 49-54*

# Robust EOT and Effective Work Function Extraction for 14 nm node FDSOI technology

B. Mohamad[1,2], C. Leroux[1], D. Rideau[3], M. Haond[3] ,G. Reimbold[1], G. Ghibaudo[2]
[1]CEA-Leti, MINATEC Campus, 38054 Grenoble Cedex 9, France
[2]Univ. Grenoble Alpes, IMEP-LAHC, MINATEC/INPG, CS 50257, 38016 Grenoble, France
[3]STMicroelectronics, BP 16, 38920, France, Email: blend.mohamad@cea.fr

***Abstract*—Effective work function and equivalent oxide thickness are fundamental parameters for technology optimization. In this work, a comprehensive study is done on a large set of FDSOI devices. The extraction of the gate stack parameters is carried out by fitting experimental CV characteristics to quantum simulation, based on self-consistent solution of one dimensional Poisson and Schrodinger equations. A reliable methodology for gate stack parameters is proposed and validated. This study identifies the process modules that impact directly the effective work function from those that only affect the device threshold voltage, due to the device architecture. Moreover, the relative impacts of various process modules on channel thickness and gate oxide thickness are evidenced.**

***Keywords—Effective work function; equivalent oxide thickness; channel thickness; buried oxide thickness; fully depleted silcon on insulator.***

## I. INTRODUCTION

The effective Work function ($WF_{eff}$) and the Equivalent Oxide thickness (EOT) are key parameters for FDSOI device characterization. They directly influence Capacitance Equivalent thickness (CET), Threshold voltage ($V_T$) and therefore on-current. Both are strongly related to the process: dielectric thickness, metal gate work function and dielectric interface dipole [1]. Former methodologies [2, 3] for automatic and statistical extraction of $WF_{eff}$ and EOT were fitted for bulk but no longer sufficient for FDSOI technology. Capacitance–Voltage extraction of the flat band voltage ($V_{FB}$) in the accumulation region has traditionally been the method for the $WF_{eff}$ extraction for the bulk technology. The absence of CV signal in the accumulation and flat band regions compared to standard bulk capacitance pushes us for alternative solution of $WF_{eff}$ and EOT extraction. Indeed the inversion region ($V_T$) still available in FDSOI can be exploited to extract the $W_{eff}$ and EOT. The extraction difficulties come out with the complexity of the FDSOI structure (Fig. 1) and the strong influence on $V_T$ of several technological parameters such as: channel thickness $t_{si}$, buried oxide (BOX) thickness $t_{box}$ and well doping level of substrate at BOX backside. We will present a comprehensive study on numerous devices (Table I) combining the process modules on metal gate, dielectric, channel material (Si & SiGe) and well implantation type (P & N doped). Reliable parameter extraction is presented by comparison between quantum simulations and experimental CV characteristics allowing the identification of the process modules that really influence EOT and $WF_{eff}$.

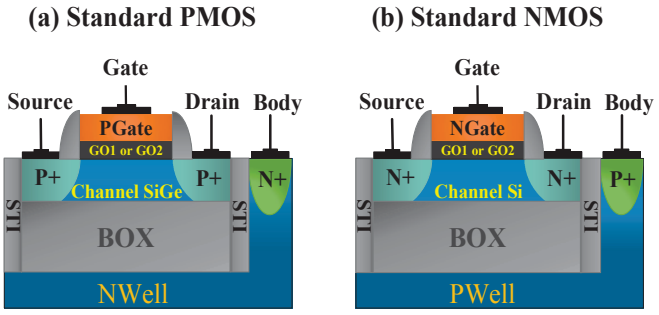



Fig. 1 Standard (a) PMOS and (b) NMOS FDSOI devices: both feature a gate stack TiN+Poly on a bilayer oxide HfON+SiON but (a) with SiGe channel and N-Well substrate and (b) with Si channel and P-Well substrate.

| | *Device Definition (GO1 & GO2)* | | | *GO1* | *GO2* |
|---|---|---|---|---|---|
| **Device** | **Channel** | **Metal** | **Well** | **ΔVt [mV]** | **ΔVt [mV]** |
| **NMOS** | Si | N | P | Ref. | Ref. |
| | Si | N | N | 45 | 115 |
| | Si | P | P | 90 | 45 |
| **PMOS** | SiGe | P | N | Ref. | Ref. |
| | SiGe | N | P | 60 | 90 |
| | SiGe | N | N | 100 | 45 |
| | Si | P | N | 320 | 250 |
| | Si | N | N | × | 295 |

TABLE I

Set of different FDSOI devices featured by combining different process modules on metal gate, dielectric, channel (Si & SiGe) and well (P & N doped). The 4th and 5th columns report on the $\Delta V_T$ shift evidenced in figs. 2 and 3.

## II. PROCESS TECHNOLGY AND EXPERIMENTAL RESULTS

Fig.1 shows two standard FDSOI MOS devices (P (a) & N (b) MOS) that feature a gate stack characterized by a metal bilayer (Poly and TiN) on the top of oxide bilayer (High-k dielectric HfON & SiON). To get such devices, the process starts from an ultra-thin silicon body over a buried oxide. The strained $Si_{0.75}Ge_{0.25}$ channel (cSiGe) is selectively processed in PMOS areas by epitaxy growth process followed by a Ge condensation, before shallow trench isolation (STI) are patterned and the back side wells are implanted. The channel thickness is around 6-8 nm of Si or $Si_{0.75}Ge_{0.25}$ over a 20 nm BOX with a P or N-Well with $10^{18}cm^{-3}$ doping level at its backside. Two different interlayer (SiON) dielectrics, can be

deposited corresponding to two different final oxide thicknesses: EOT=1 nm for GO1 and EOT=3 nm for GO2. The bilayer high-k HfON/SiON is deposited by Atomic Layer Deposition, Metal Organic Vapor deposition and decoupled plasma nitridation. To obtain N and P gate types, before the final metal gate, a sacrificial gate is deposited, specifically to each N or P gate type. Sacrificial gates includes specific additives which are diffused by thermal annealing in order to adjust dipole at oxide bilayer inner interface [1, 4]. After final gate etching, the Source-Drain implantations (specific to each FDSOI MOS type) are carried out, followed by final annealing. From these standard FDSOI MOS, a wide set of devices has been obtained by combining the process modules on metal gate, dielectric, channel and well type (Table I). Their relative gate to channel capacitances (Cgc) are reported in Fig. 2 for GO1 devices and Fig. 3 for GO2 devices. $V_T$ shift with respect to the reference architecture are evidenced and summarized in the last two columns of Table I.

## III. Simulations and Extraction

The extraction of gate stack parameters (EOT and $WF_{eff}$) of these devices (Table I) is obtained by fitting Quantum Simulation to experimental capacitance-voltage characteristics (CV). The simulations are based on the self-consistent solutions of one dimensional Poisson and Schrodinger equations (PS), carried out by TCAD Simulator (UTOXPP [5]). To qualify the quality of parameter extraction, various hypotheses on physical parameters ($t_{box}$, $t_{si}$) have been compared on the same experimental device (Standard PMOS GO2). A good fit can be obtained for the three different set of parameters (Fig. 4) leading to three different values for EOT and $WF_{eff}$. Whereas, EOT is found to be independent of $t_{box}$ and $t_{si}$ values (with precision below 0.01 nm), a precision on $WF_{eff}$ below 5 mV is questionable. Such a result evidences the importance of a previous extraction on $t_{box}$ and $t_{si}$ in order to accurately extract $WF_{eff}$. To extract $t_{box}$, we have recently proposed a new CV measurement with back side wafer contact as Gate [6]. Fig. 5 shows the experimental configuration of the back-gate-to-channel capacitance.

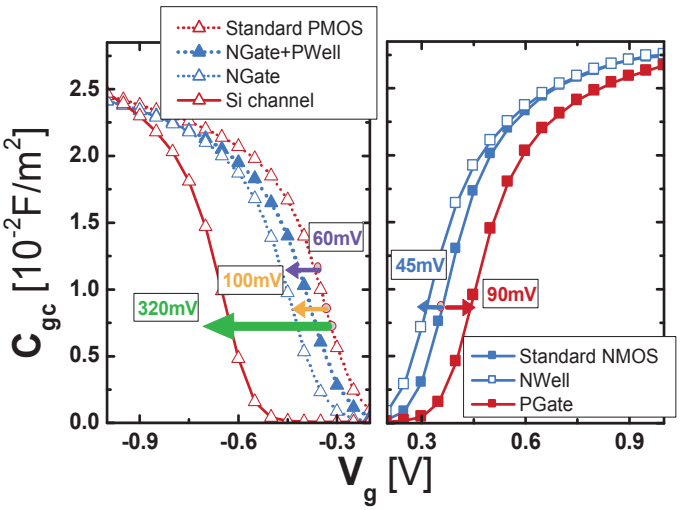



Fig. 2 Gate to channel capacitance at back bias Vb=0V for PMOS and NMOS FDSOI GO1 with $V_T$ shift to reference architecture.

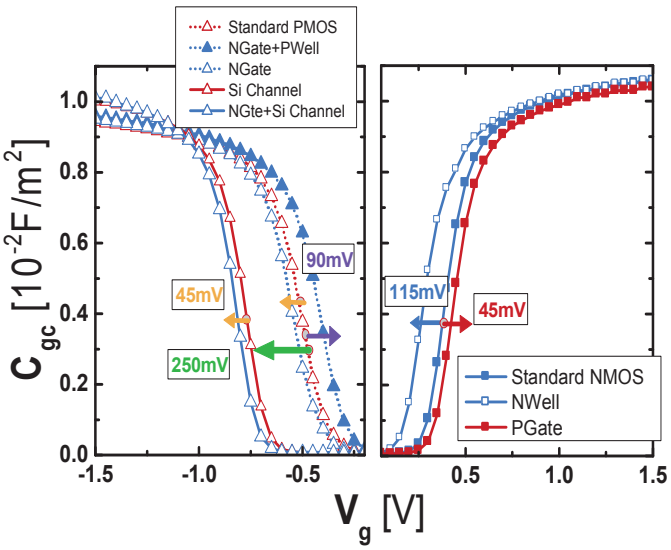



Fig. 3 Gate to channel capacitance at back bias Vb=0V for PMOS and NMOS FDSOI GO2 with $V_T$ shift to the reference architecture.

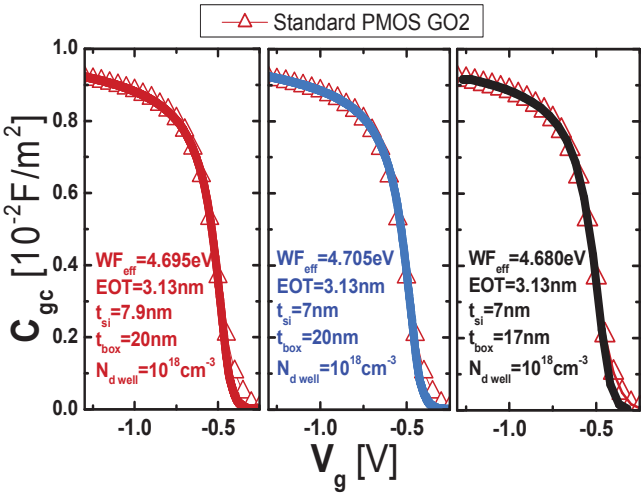



Fig. 4 Standard PMOS GO2 Gate to channel capacitance compared with Simulation (UTOXPP) with different channel and BOX thicknesses (each fit leads to a certain $WF_{eff}$ and EOT extraction).

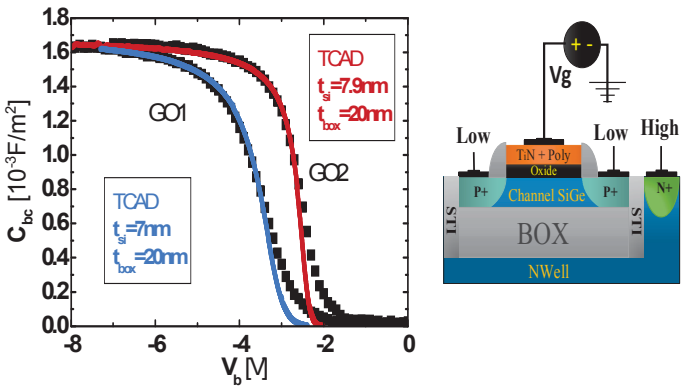



Fig. 5 Experimental standard PMOS GO1 & GO2 back-gate-to-channel capacitance compared to Simulation (UTOXPP) leading to $t_{box}$ extraction.

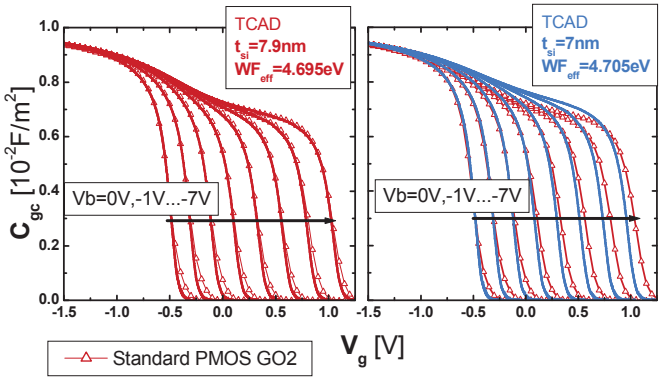



Fig. 6 Standard PMOS GO2 Gate to channel capacitance vs Simulation (UTOXPP) with two different channel thicknesses (7.9 nm $t_{si}$ is mandatory for fitting all CV's).

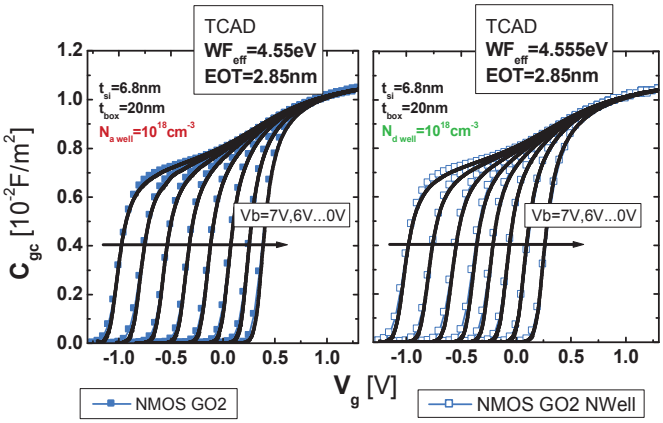



Fig. 7 Fitting between simulations and experiments for two MOS devices having two different well types at back side of buried oxide.

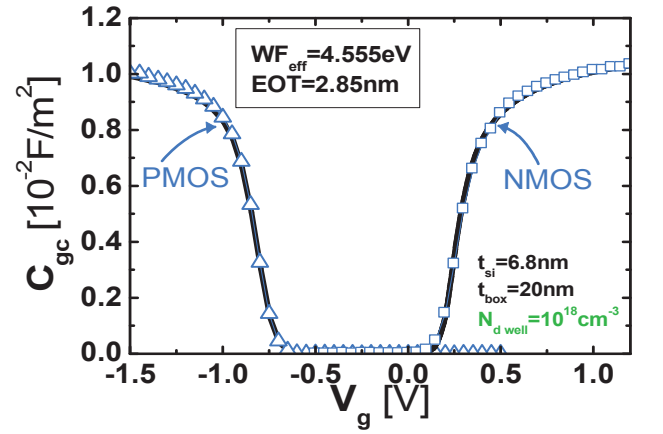



Fig. 8 Fitting between simulation and experimental for two different MOS having a same gate stack and two different Source and Drain implantation (GO2 NMOS with N-Well & GO2 PMOS with N-Well and N-Gate metal and Si channel).

The low bias contact of the capacitance meter is connected to Source-Drain terminals, the high bias contact at the well (Body) terminal and finally the offset bias contact at the Gate terminal. The corresponding CV for GO1 and GO2 (Fig. 5) shows similar characteristics to the standard gate-to-channel capacitance but significantly at a lower level. Adjustment with quantum simulation makes possible a reliable extraction of the box thickness, independently of $t_{si}$ and EOT [6]. A 20 nm box thickness is necessary in order to fit $C_{bc}$ capacitances for both the standard PMOS (GO1 and GO2). Concerning $t_{si}$, it can be obtained by comparison between simulations and experiments on a large set of CV characteristics for which back biases vary from 0V to large back interface inversion (Fig. 6). We can notice that there is only one channel thickness that takes into account the proper capacitance deformation for large back interface inversion. If $t_{box}$ and $t_{si}$ are expected to shift $V_T$ but also $WF_{eff}$, Source and Drain type as well as back substrate well should only impact $V_T$. Indeed, during the device fabrication, the implantation of the Source-Drain as well as the back substrate well are carried out without any influence on the of the MOS stack (Metal/Oxide/Semiconductor). A reliable parameter extraction must verify the independence of $WF_{eff}$ and EOT with variations on Source and Drain implantation or Well implantation types. It has been confirmed on three different MOS devices, corresponding to two different well types (Fig. 7) and two different MOS types (Fig. 8).

## IV. Results

In Fig. 9, $WF_{eff}$ and EOT extraction for the fifteen different tested MOS devices (Table I and figs. 2-3) are summarized. The agreement reported above on $WF_{eff}$ & EOT for three different MOS (Fig. 7-8) is identified in Fig. 9 with a blue arrow. Among the fifteen different devices, other configurations correspond to same gate stack and channel material but different Source and Drain or back side well types. They all lead to a good agreement which are identified with green arrows on Fig. 9.

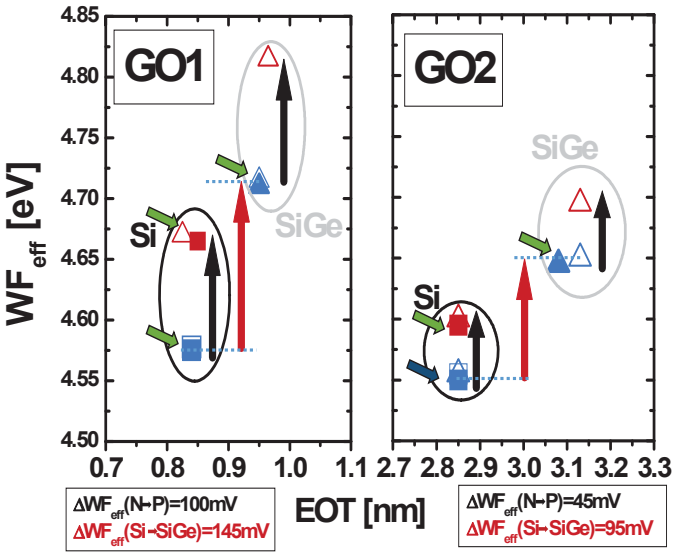



Fig. 9 $WF_{eff}$ versus EOT for different structures PMOS and NMOS FDSOI. Impact of Ge and sacrificial Metal gate and coherence of $WF_{eff}$ and EOT extraction are shown.

$t_{box}$ is not reported on these figures. In fact, $t_{box}$ is found at the same 20 nm value for all the different MOS devices, a value corresponding to the target of the SOI substrate.

We report on Fig. 10 the dependence of $t_{si}$ with EOT. It appears to depend only on channel and oxide type. Indeed it is equal to 6.1 nm for Si and 7 nm for SiGe for all GO1 devices and 6.8 nm for Si and 7.9 nm for SiGe for all GO2 devices. SiGe channel is found to be 1 nm thicker than Si channel and in both cases, GO2 process leads to less channel consumption.

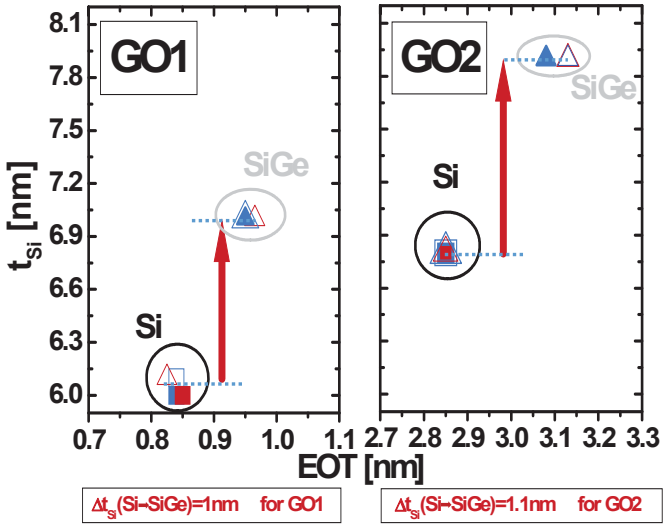



Fig. 10 $t_{si}$ versus EOT for different structures PMOS and NMOS FDSOI. Impact of Ge and coherence of $t_{si}$ and EOT extraction are shown.

EOT is reported in Fig. 9-10. It depends primarily on oxide type (GO1 and GO2) but also on channel material. As already evidenced in previous studies [7], gate oxide formation leads to a slight interlayer regrowth on SiGe substrate. We notice here an interlayer regrowth around 0.12 nm for GO1 and 0.3 nm for GO2.

$WF_{eff}$ appears to depend on gate type, channel material and oxide (GO1 and GO2). Considering first GO1, we notice an average shift of 100 mV from N to P metal gate. It is the expected effect of Al dipole created at HfON/SiON interface by the sacrificial gate process [1]. With SiGe channel, $WF_{eff}$ report an additional shift of 145 mV. In fig. 2 we can notice that $V_T$ shift with SiGe channel reaches 320 mV. It is partially explained by the shift of valence band for SiGe semiconductor, but an addition $WF_{eff}$ shift of 145 mV is required to account of the whole $V_T$ shift. It has been identified as an interface dipole at SiGe/SiON interface [7]. For GO2, both dipoles at HfON/SiON and SiGe/SiON device interfaces decrease respectively of 45 and 95 mV.

## V. Conclusion

Robust EOT and $WF_{eff}$ extractions on FDSOI devices have been proposed through a methodology based on comparison between experimental CV characteristics and simulations. To be reliable, it requires a first identification of buried oxide thickness ($t_{box}$) and channel thickness ($t_{si}$). It has been validated on a large set of devices. Such analysis evidence the relative impact of process modules on $t_{si}$, EOT and $WF_{eff}$. Channel thickness and equivalent oxide thickness appear to depend on the channel material and the gate oxide interlayer process. Whereas effective work function is a combined effect of interlayer, channel interlayer and sacrificial gate type.

## Acknowledgment

The authors would like to thank MINOS Laboratory of French ANR and PLACES2BE Project for their support for this work.

## References

[1] C. Suarez-Segovia, C. Leroux, P. Caubet, F. Domengie, G. Reimbol G. Romano O. Gourhant V. Joseph, G. Ghibaudo "Effective Work Function modulation by *sacrificial* gate aluminum diffusion on HfON-based 14nm NMOS devices," Microelec. Eng. 2015, (147), p. 113–116.

[2] C. Leroux, S. Baudot, M. Charbonnier, A. Van Der Geest, P. Caubet, A. Toffoli, Ph. Blaise, G. Ghibaudo, F. Martin, G. Reimbold "Investigating doping effects on high-jmetal gate stack for effective work function engineering," Microelec. Eng. 2007, (84), p. 2408-2411.

[3] A. Soussou, C. Leroux, D. Rideau, A. Toffoli, G.Romano, C. Tavernier, G. Reimbold, G. Ghibaudo, "Parameters extraction in SiGe/Si pMOSFETs using split CV technique," Proc. of ULIS Conf., Cork (Ireland), 2013, p. 41-44.

[4] Carlos Suarez-Segovia, C. Leroux, F. Domengie, K. Dabertrand, V. Joseph, G. Romano, P. Caubet, S. Zoll, O. Weber, G. Ghibaudo, G. Reimbold and M. Haond, "Effective work function engineering by sacrificial lanthanum diffusion on HfON-based 14 nm NFET devices," Solid State Device Research Conference (ESSDERC), 14-18 Sept. 2015 45th European, p. 246 – 249.

[5] D. Garetto, D. Rideau, C. Tavernier, Y. Leblebiciand, A. Schmid, H. Jaouen, "Advanced physics for simulation of ultrascaled devices with UTOXPP Solver," Proc. of NTSI-Nanotech 2011, Boston (USA) p. 607-610.

[6] B. Mohamad, G. Ghibaudo, C. Leroux, E. Josse, G. Reimbold, "Full Front and Back Split C-V characterization of CMOS devices from 14nm node FDSOI technology," Proc. of S3S Conf., Rohnert Park (USA), 2015, section 9a.4.

[7] A. Soussou, C. Leroux, D. Rideau, A. Toffoli, G. Romano, O. Saxod, G. Bidal, D. Barge, D. Pellissier-Tanon, F. Abbate, C. Tavernier, G. Reimbold, G. Ghibaudo, "Understanding Ge impact on VT and VFB in Si1−xGex/Si pMOSFETs," Microelec. Eng. 2013, (109), p. 282–284

# Benchmarks of a III-V TFET technology platform against the 10-nm CMOS technology node considering 28T Full-Adders

*S. Strangio[1,2,*], P. Palestri[1], M. Lanuzza[2], D. Esseni[1], F. Crupi[2], L. Selmi[1]*
[1]DIEG, Università degli Studi di Udine, Via delle Scienze 206, 33100 Udine, Italy.
[2]DIMES, Università della Calabria, Via P. Bucci, 42C, 87036 Arcavacata di Rende (CS), Italy.
*email: seb88str@gmail.com; phone: +39 329 8227198

***Abstract*** *— This paper presents a benchmark of a virtual III-V TFET nanowire technology platform against the predictive models of CMOS FinFETs for the 10-nm technology node. The standard 28T full adder and the 32-bits ripple carry adder are used as vehicle circuit/architecture for the comparison, respectively. Figures-of-merit including delays, energy and energy-delay plots are discussed.*

***Keywords — TFET, III-V compounds, VLSI , full adder.***

## I. Introduction

Tunnel field-effect-transistors (TFETs) featuring a potential sub-threshold-swing SS < 60 mV/decade have been proposed as an alternative to conventional MOSFETs [1-4].

A virtual III-V TFET technology platform has been recently designed by using 3D full-quantum simulations [1,2], and benchmarked against a future CMOS technology [5,6] considering inverters [2]. Since the full quantum modeling approach used in [2] does not allow to perform circuit simulations, inverter figures-of-merit have been extracted through approximate estimations, by considering the device drain current characteristics and assuming effective capacitive loads instead of the bias-dependent device capacitance.

In this paper, we use TCAD device modeling and circuit simulations to extend such a benchmark to standard 28T Full-Adders (FAs) [7].

## II. Methodology

The proposed analysis relies on a multi-level simulation approach, including device and circuit simulations. TCAD *Sentaurus Device* [8] has been used to bridge these levels of abstraction, in the sense that the full-quantum simulation results in [2] have been used to calibrate the parameters of the AlGaSb/InAs hetero-structure simulated in TCAD. Then $I_D$-$V_{GS}$-$V_{DS}$, $C_{gs}$-$V_{GS}$-$V_{DS}$ and $C_{gd}$-$V_{GS}$-$V_{DS}$ look-up-tables (LUTs) were setup using the TCAD results and finally imported as Verilog-A models in the *Cadence* simulation environment.

## III. Devices

As shown in Fig. 1, the III-V TFET technology platform [2] consists of AlGaSb/InAs TFET nanowires (NWs). Due to quantum confinement in the 7×7 nm$^2$ square cross-section of the NWs, parameters as the *energy-gap* ($E_G$), the *electron affinity* ($\chi$), the *effective valence and conduction band density of states* ($N_V$ and $N_C$), and the dynamic nonlocal-path Band-to-Band Tunneling (BtBT) model parameters ($A_{path}^{dir}$ and $B_{path}^{dir}$, see [8]) need to be recalibrated.

The calibrated TCAD models have allowed us to reproduce the $I_D$-$V_{GS}$ in [2] (parameters in Table.I [1,8,9]), as illustrated in Fig.2 by the matching of our TCAD simulations (lines) to reference simulations from [2] (symbols).

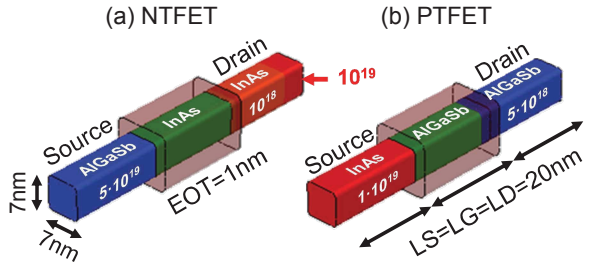



**Fig.1**: *AlGaSb/InAs TFET structures implemented in the TCAD to reproduce the full-quantum simulations of the devices proposed in [2]. Dimensions, materials, and doping levels (in cm$^{-3}$) are the same as in [2].*

| Parameter | $Al_{0.05}Ga_{0.95}Sb$ | InAs |
|---|---|---|
| $E_G$ (eV) | 1.04 | 0.59 |
| $\chi$ (eV) | 4.01 | 4.9 |
| $A_{path}$ (cm$^{-3}$s$^{-1}$) | $1.51{\cdot}10^{20}$ | $1.44{\cdot}10^{20}$ |
| $B_{path}$ (V/cm) | $9.54{\cdot}10^{6}$ | $2.94{\cdot}10^{6}$ |
| $N_C$ (cm$^{-3}$) | $1.26{\cdot}10^{18}$ | $5.22{\cdot}10^{17}$ |
| $N_V$ (cm$^{-3}$) | $1.8{\cdot}10^{19}$ | $6.6{\cdot}10^{18}$ |

**Table I**: *Parameters used to calibrate the TCAD simulation deck. $E_G$ and $\chi$ are extracted from [1], the BtBT model parameters $A_{path}$ and $B_{path}$ are computed using effective masses from [9]. $N_C$ and $N_V$ are used as fitting parameters.*

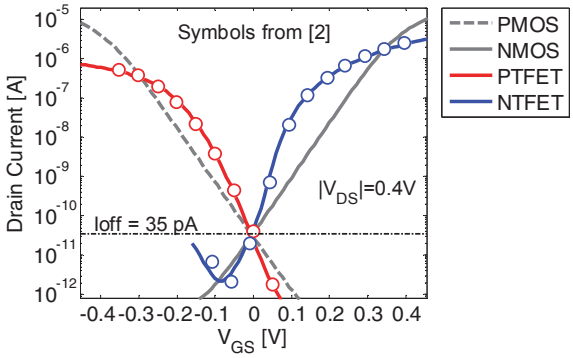



**Fig.2**: *Simulated $I_D$-$V_{GS}$ for the TFETs in Fig.1 (red and blue lines) and for the 10 nm node CMOS FinFETs of the predictive models [6] (grey). The full-quantum TFET simulations from [2] are indicated by bullets. $V_{DS}$=0.4V.*

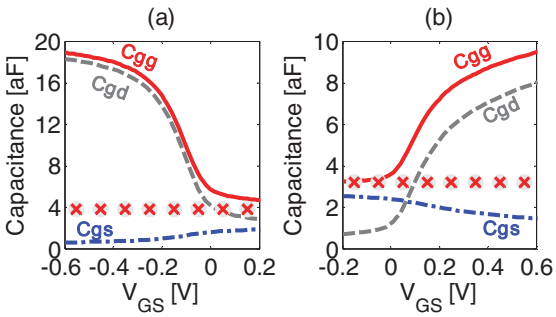



**Fig.3**: *Simulated TFET capacitances versus $V_{GS}$ at $V_{DS}$=0V for the (a) PTFET and (b) NTFET. The symbols in the plot represents the total gate capacitances ($C_{GG}$) reported in [2], estimated as $C_{GG} = (Q_{ON}-Q_{OFF})/V_{DD}$.*

For the same off-current ($I_{OFF}$) of 35 pA (corresponding to an $I_{OFF}/side^{NW}$ = 5 nA/μm, in agreement with the LOP target of the ITRS [10]), the PTFET features a lower on-current ($I_{ON}$) (about 1/4) than the NTFET at $V_{DD}$ = 400mV. Despite this asymmetry, we keep a 1/1 ratio between the size of the NTFETs and PTFETs in the following circuit analysis.

Regarding the MOSFET counterparts, we consider FinFETs projected to the 10 nm node: *spice Predictive-Technology-Models of Multi-Gate transistors* (PTM-MG) have been presented in [5] and are available in [6]. The PTM-MG $I_D$-$V_{GS}$ curves are also reported in Fig.2 (grey lines), where all the transfer characteristics have been aligned to the same $I_{OFF}$ current (in A, not in A/μm) to assure a fair comparison. Unlike TFETs, the n- and p-MOSFET characteristics are practically symmetric.

Fig.3 shows the capacitance characteristics ($C_{gs}$-$V_{GS}$, $C_{gd}$-$V_{GS}$ and the total $C_{gg}$-$V_{GS}$). The symbols in the plot represent the $C_{gg}$ reported in [2], which have been estimated as the net charge difference between the on and off states divided by $V_{DD}$ ($C_{gg} = (Q_{ON}-Q_{OFF})/V_{DD}$). The resulting values have been used in [2] to calculate the total input capacitance of an inverter ($C_{in}$).

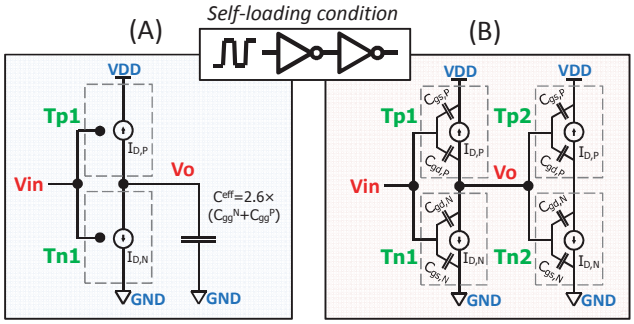



**Fig. 4**: *Inverter self-loading condition. (A) Only the $I_D$-$V_{GS}$-$V_{DS}$ Verilog-A LUTs of Tp1 and Tn1 (driving inverter) are considered, whereas the $C_{in}$ of the load and the Miller capacitances of the driver are replaced by an equivalent effective capacitor. (B) Full description of the devices (full $I_D/C_{gs}/C_{gd}$-$V_{GS}$-$V_{DS}$ LUTs activated).*

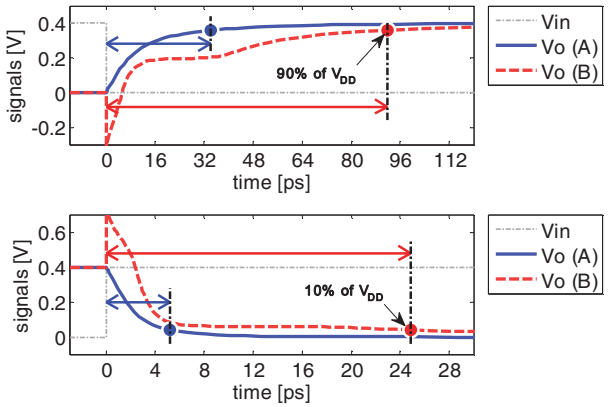



**Fig. 5**: *Rise and fall transient simulations for the (A) and (B) test conditions sketched in Fig.4. Delays are extracted considering the time at which the output voltage crosses the 90% (10%) of $V_{DD}$ for the low-to-high (high-to-low) transitions.*

## IV. Inverter Delay

Fig.4 sketches the self-loading condition for an inverter whose load is an inverter equal to the inverter under study. Here, we have simulated such a circuit with two approaches, as sketched in Fig.4: (A) follows the approximations in [2], where a constant load is representative of both the loading inverter $C_{in}$ and the Miller capacitance ($C_M$) of the driving inverter; (B) describes the self-loading condition by taking into account the actual bias dependence of the device capacitance (i.e. employing current and capacitance LUTs for each device).

Fig.5 shows the transient voltage waveforms for both the simulation options sketched in Fig.4. The output waveforms simulated with the approximated approach (A) differs considerably than the ones simulated with the approach (B), which show voltage under/overshoots as well as plateaus due to Miller effect and input-to-output coupling.

ISBN 978-1-4673-8608-1

IEEE Catalog number CFP1649D-USB

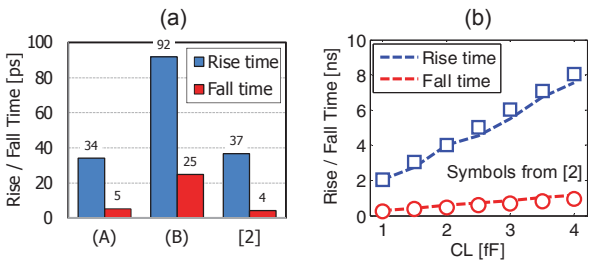



**Fig. 6**: (a) *Rise and fall times for the self-loading case computed either as in Fig.4(A) or as in Fig.4(B). (b) Rise and fall times for the constant loading case as a function of the capacitance of the load.*

Fig.6a compares the rise and fall times extracted from transient simulations in Fig.5 with the ones reported in [2]. The rise/fall times simulated for (A) match well with the data in [2], but in the following of this paper we will use the approach (B), that we judge more accurate in the description of the overall time dependent waveforms. Fig.6b reports the rise/fall times as a function of an external constant capacitance load much larger than the intrinsic capacitances. In this case, since $C_L \gg C_{in}$ ($C_M$), the dynamic response is dominated by the external load and our simulations match well with results in [2].

## V. Full Adders

Schematic circuits reproducing the standard 28T FA topology in Fig.7 have been implemented with TFETs, by means of the Verilog-A models extracted from the TCAD deck, as well as with the spice models for the 10-nm PTM-MG FinFETs.

The test-bench in Fig.8 allows simulating a FA (the green box is the circuit under test) under normal operating conditions, since it is placed in a framework including driving and loading blocks. The AN, BN and CN signals consist of random binary waveforms with a length of 100 bits, each bit is held for a bit-time ($T_{bit}$) of 100 ns. For such a $T_{bit}$, the TFET (CMOS) circuit operates down to a $V_{DD}$ of 75 mV (175 mV).

Fig.9 reports the worst-case delay for sum (S) and carry-out (Co) bits versus $V_{DD}$. For each transition of S, the delay is computed taking as a reference the specific input signal triggering the transition (i.e. the latest switching signal among A, B and C). The delay of Co is calculated for different cases: propagation of '1' or '0' (P1 and P0), generate (G), delete (D). In the "propagate" mode (i.e. when A≠B), Co follows the value of C. In the "generate" and "delete" modes (i.e. when A=B), we have Co=A=B, regardless of the value assumed by C. Thus, for each transition of Co, the delay is computed taking as a reference either C (when the Co transition happens in the "propagate" mode) or the latest signal to flip between A and B (when the Co transition happens in the "generate" or "delete" modes). The propagation delay ($t_{Prop.}$), corresponding to the worst case delay between Co(P1) and Co(P0), is the bottleneck for an n-bit FA in the Ripple-Carry-Adder (RCA) implementation [7], since the theoretical minimum clock-period $T_{bit}$ is given approximately by $n \times t_{Prop.}$.

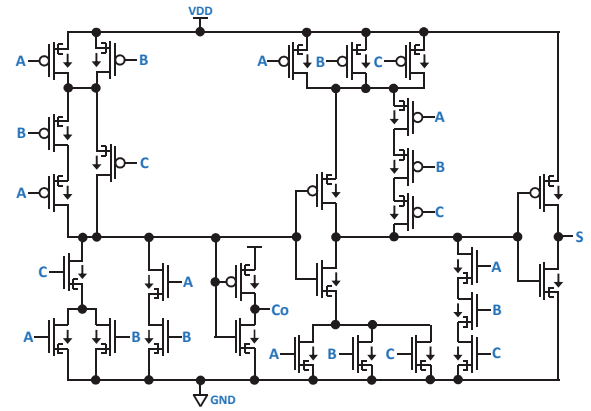



**Fig. 7**: *Standard 28T full-adder topology.*

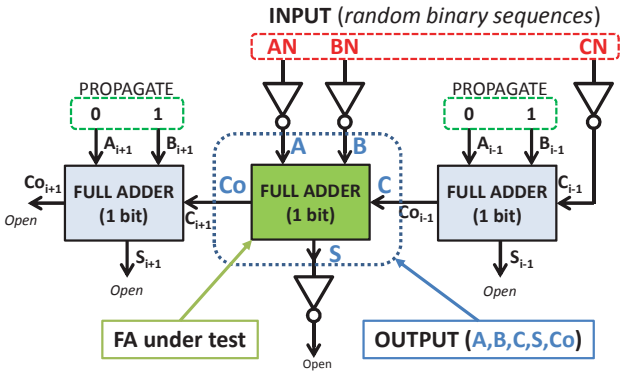



***Fig. 8***: *Test-bench for 1-bit full adders (FAs). Besides the FA under test (green box), the overall test-system is implemented with two further FAs and four inverters. The FA on the right and the three inverters on the top are employed to feed the FA under test with realistic waveforms, whereas the FA on the left and the inverter at the bottom are used as realistic loads. Both the driving and the loading FAs are kept in the "propagate" mode.*

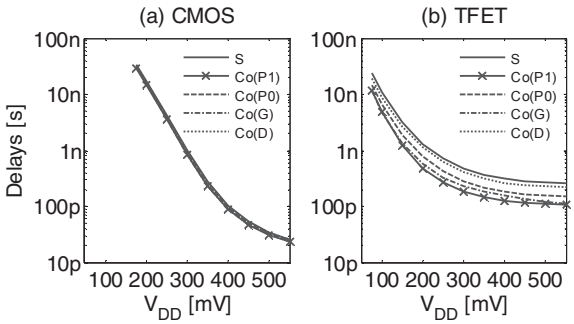



**Fig. 9**: *Sum (S) and carry-out (Co) delays as a function of $V_{DD}$ for the standard 28T FA implemented either in (a) CMOS or (b) TFET. The delay of the Co is reported for different cases: P1/P0 (propagation of 1/0), D (delete), G (generate).*

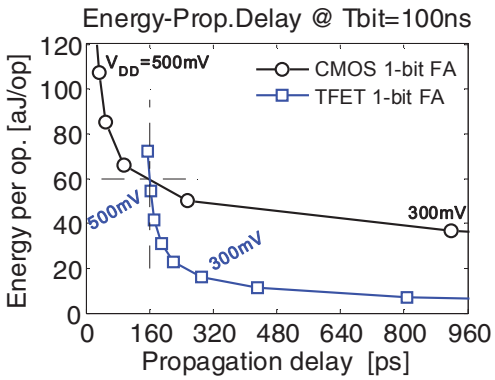



**Fig. 10**: *Energy per operation - propagation delay plot computed at $T_{bit}$ = 100 ns for 1-bit FA blocks. Points correspond to different $V_{DD}$ (steps of 50 mV).*

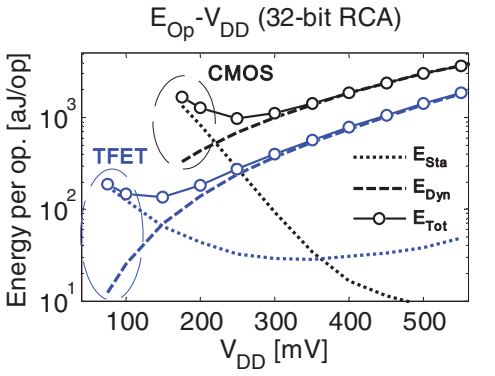



**Fig. 11**: *Energy per operation as a function of $V_{DD}$ projected for 32-bit ripple carry adders. The energy is evaluated at the minimum $T_{bit}$ for each $V_{DD}$.*

Focusing on limited energy budget applications, pure performance figures-of-merit are less important than the overall energy necessary to complete one operation. The energy per operation versus the propagation delay computed at $T_{bit}$ = 100 ns for 1-bit FA blocks is reported in Fig.10. Here, for simplicity $T_{bit}$ is kept constant over the whole $V_{DD}$ range, rather than adjusting it to the minimum value fixed by $t_{Prop.}$. Taken as a single instance, the TFET FA features a much lower minimum energy point (<10 aJ/cycle) than its CMOS counterpart, that is however more energy efficient in applications with more stringent timing constraints (i.e. $t_{Prop.}$ < 160 ps).

In Fig.11, 1-bit FA simulation results are projected to 32-bit RCAs to compute the minimum energy necessary to complete a sum operation ($E^{Op}$) between two 32-bit words. Such projection is performed by separating the static and dynamic energy components (SE and DE, respectively) for each $V_{DD}$. Then the SE is re-scaled relying on the minimum $T_{bit}$ at which the 32-bit RCA can operate, whereas the DE is essentially independent of $T_{bit}$. In the CMOS case, there is a Minimum Energy Point (MEP) at $V_{DD}^{MEP,CMOS}$ = 250 mV, since a further scaling of $V_{DD}$ below $V_{DD}^{MEP}$ results in a higher energy consumption because the SE contribution becomes dominant. At any $V_{DD}$ the $E^{Op}$ is much lower in the TFET implementation (it is dominated by the DE component down to $V_{DD}$ = 200 mV), basically because the increase of $t_{Prop.}$ is less pronounced than the reduction of the leakage current with the $V_{DD}$ scaling. Thus, the MEP in the 32-bit TFET RCA corresponds to a lower $V_{DD}$ ($V_{DD}^{MEP,TFET}$ = 150 mV).

## VI. Conclusions

A III-V TFET technology platform has been benchmarked against the predictive models for the 10 nm node CMOS FinFETs considering full-adders as test circuits. Concerning 1-bit full adders, taking into account both energy per operation and propagation-delay figures-of-merit, the one implemented with TFETs features a much lower minimum energy per operation (below 10 aJ/op.), whereas the CMOS one is more energy efficient in fast applications requiring $t_{Prop.}$ < 160 ps. Considering 32-bit ripple carry adders, the TFET architecture allows to save energy at any $V_{DD}$ in the considered range; from 550 mV down to 300 mV, for the same $V_{DD}$ (but different propagation delay), there is more than a factor of 2 for the energy consumed per operation between the two implementations. Furthermore, a minimum energy point of 135 aJ/op is found at $V_{DD}$ = 150 mV for the TFET case, well below the minimum energy point of 976 aJ/op (at $V_{DD}$ = 250 mV) for the CMOS implementation. The effects of device variability, not included in this study, may become however relevant at such low $V_{DD}$s.

## Acknowledgment

The research leading to these results has received funding from the European Community's Seventh Framework Programme under grant agreement No. 619509 (project E2SWITCH) and from the Italian MIUR through the Futuro in Ricerca project RBFR10XQZ8.

## References

[1] E. Baravelli, E. Gnani, R. Grassi, A., Gnudi, S., Reggiani, G., Baccarani, *IEEE Transactions on Electron Devices*, v.61, n.1, pp.178-185, 2014.

[2] E. Baravelli, E. Gnani, A. Gnudi, S. Reggiani, G. Baccarani, *IEEE Transactions on Electron Devices*, v.61, n.2, pp.473-478, 2014.

[3] S. Strangio, P. Palestri, D. Esseni, L. Selmi, F. Crupi, S. Richter, Q.-T. Zhao, S. Mantl, *IEEE Journal of the Electron Devices Society*, v.3, n.3, pp.223-232, 2015.

[4] M. Lanuzza, S. Strangio, F. Crupi, P. Palestri, D. Esseni, *IEEE Transactions on Electron Devices*, v.62, n.12, pp.3973-3979, 2015.

[5] S. Sinha, G. Yeric, V. Chandra , B. Cline, Y. Cao, *Proc. 49th ACM/EDAC/IEEE DAC*, pp. 283-288, 2012.

[6] URL: http://ptm.asu.edu.

[7] M. Alioto, G. Palumbo, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, v.10, n.6, pp.806-823, 2002.

[8] TCAD Sentaurus Device U.G., version G-2012.06, 2012.

[9] URL: http://www.ioffe.ru/SVA/NSM/Semicond/.

[10] International Technology Roadmap for Semiconductors (ITRS), Process Integration, Devices, and Structures (PIDS) Chapter, 2011. URL: http://www.itrs.net.

# *Improved voltage gain in mechanically stacked bilayer graphene field effect transistors*

Himadri Pandey[a], Satender Kataria[a], Vikram Passi[a], Mario Iannazzo[a,b], Eduard Alarcon[b] , Max C. Lemme[a,*]
[a]University of Siegen, School of Science and Technology, Hölderlinstr.3, 57076 Siegen
[b]Technical University of Catalonia, Department of Electronics Engineering, UPC, 08034 Barcelona, Spain
*Email: max.lemme@uni-siegen.de

***Abstract*— Dual gated graphene field effect transistors (GFETs) were fabricated using mechanically stacked large area chemical vapor deposited (CVD) graphene bilayer. The devices were characterized in ambient conditions at various back gate voltages. Higher induced carrier densities were observed in the device channels at increasingly negative back gate voltages. Also, enhanced tendency to saturation was observed. These observations indicate that mechanically stacked bilayer GFETs can be potential candidates for future graphene circuit applications where a lower output conductance is desired for maximum intrinsic voltage gain.**

***Keywords*— CVD graphene; GFET, intrinsic voltage gain, mechanically stacked bilayer, saturation.***

## I. INTRODUCTION

Graphene has attracted much attention of the device research community since its earliest experimental demonstrations as graphene field effect transistors [1], [2]. Many recent advancements in this direction have led to proposed analog applications of graphene into circuits, with results being reported both theoretically [3]–[5] as well as experimentally [6]. This requires good current saturation, which in turn may lead to an improved intrinsic voltage gain. Intrinsic voltage gain $A_{v0}$, defined as the ratio of transconductance $g_m$ to output conductance $g_d$, is an important device parameter from the view point of circuit applications of GFETs. However, poor current saturation in GFETs due to the absence of a band gap (and thus ambipolar channels) has been a bottleneck in realizing high performance circuit applications. Several approaches have been proposed in literature to improve current saturation in GFETs, such as using Bernal stacked bilayer graphene with an electrically tunable band gap [7] or using graphene nano-ribbons (GNR) as the channel material [8]. However, large area CVD growth of Bernal stacked bilayer graphene is still in infancy, mostly because of the polycrystalline nature of growth [9] which leads to mixed orientations of the graphene layers. The fabrication of very narrow GNRs has been demonstrated, but there are severe challenges in manufacturability and process control, as sub-5 nm ribbons would be required for a sizeable band gap [10]. These difficulties in achieving practical solutions towards a scalable large area GFET fabrication scheme with saturating characteristics point towards the need of an alternate and feasible approach. In this paper, we explore experimentally the performance potential of mechanically stacked CVD graphene bilayer GFETs (BIGFETs).

## II. DEVICE FABRICATION

Thermally oxidized (85 nm) p-Silicon <100> wafers with a Boron doping concentration of $3x10^{15}$ $cm^{-3}$ were used as starting substrates. The samples were cleaned in acetone, followed by isopropyl alcohol (IPA) and finally rinsed with deionized water (DI water). Followed by this in-house grown CVD graphene monolayer was transferred using an electro-delamination method with PMMA support layers [11]. The PMMA layers were then dissolved in acetone, followed by subsequent transfer of a second monolayer graphene sheet on top of it, resulting in a randomly oriented bilayer stack. Fig. shows the optical micrograph of the stacked bilayer graphene after transfer onto silicon-dioxide/silicon substrate. Channels were defined using optical lithography and patterned using oxygen plasma based reactive ion etching. Thermal evaporation of a 10 nm/90 nm Cr/Au stack followed by a lift off in warm acetone was used to define source-drain contact pads. 10 nm $SiO_2$ was e-beam evaporated as the top gate oxide. Thermal evaporation of 100 nm Al gate metal and another subsequent lift off in acetone completed the device fabrication. Another similar set of devices was fabricated using atomic layer deposition of $Al_2O_3$ gate dielectrics with effective oxide thickness (EOT) of approximately 10 nm, with all other fabrication steps remaining the same as above.

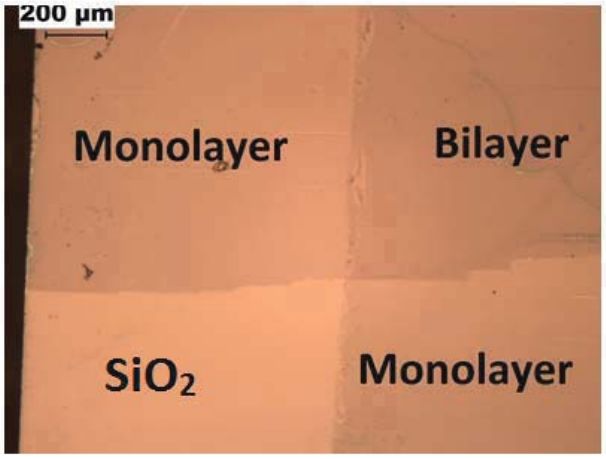



Fig. 1. Optical micrograph of mechanically stacked bilayer graphene,

including two regions of the respective monolayers.

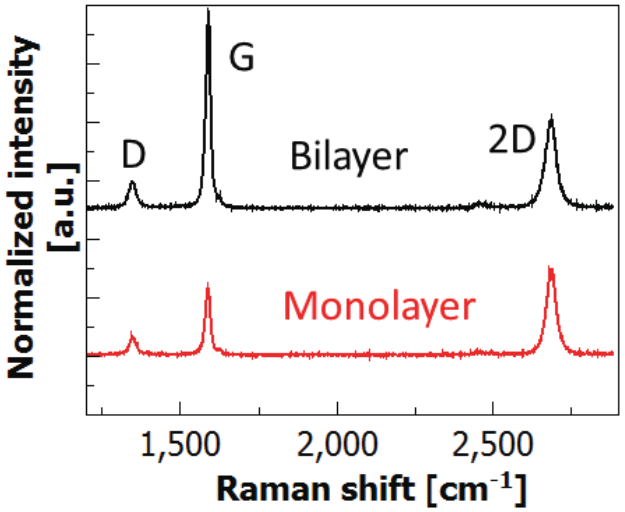



Fig. 2. Raman spectra of stacked bilayer graphene compared to monolayer graphene.

## III. RESULTS & DISCUSSION

Bilayer stacks were first characterized using Raman spectroscopy. Fig. 2 shows typical Raman spectra of monolayer and bilayer regions obtained using a 532 nm laser. It can be seen that 2D and G bands show a different behavior in the bilayer region as compared to monolayer graphene with an enhancement in G band intensity and a broadened 2D band. This indicates the presence of a weak electrostatic coupling between the two stacked layers [12]. The D peak which indicates the presence of defects remains nearly unchanged between the monolayer and stacked bilayer regions, which shows that during the stacking process, no substantial defects were introduced in the graphene stack. Fig. 3(a) shows the optical micrograph of a typical fabricated device. The device was characterized in ambient conditions using a Karl Süss probe station connected to a Keithley 4200-SCS parameter analyzer. Fig. 3(b) shows the output and transfer (inset) characteristics of a device at zero back gate voltage ($V_{BG}$). At each back gate voltage, several transfer and output characteristics were measured and maximum DC transconductance ($g_{m,max}$) as well as minimum output conductance ($g_{d,min}$) values were analyzed. The transconductance ($g_m$) defines how well the local gate modulates the device channel, however in this study we only focus on minimization of output conductance values ($g_d$) which defines the quantum of saturation tendency. For this reason, all the devices in this paper have been fabricated with conventionally used Cr/Au stacks for contacts. A comparison of performance of two of our devices with literature reports of monolayer and Bernal stacked bilayer GFETs is shown in Fig. 4. It was observed that $g_{m,max}$ (Fig. 4a) values follow a trend similar to that of monolayer GFETs whereas $g_{d,min}$ (Fig. 4b) values were of lower magnitude at increasingly negative $V_{BG}$. This results in an improved voltage gain figure ranging between 2.5 to 28.84, with an average gain figure between 6 and 10, without any special steps taken during device fabrication like self-alignment [13], special substrates [14] or ultra-clean processes [15].

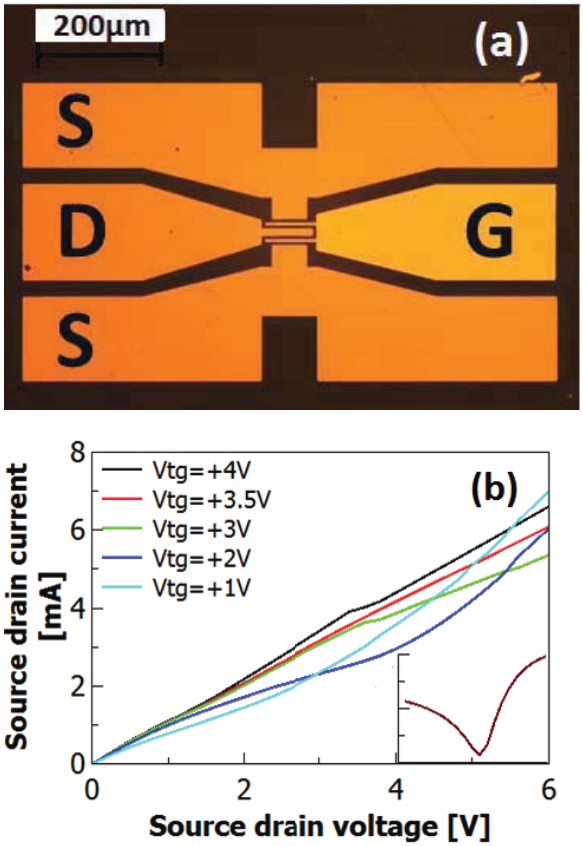



Fig. 3. (a) optical micrograph of the fabricated BIGFET; (b) the output characteristics of the fabricated device at zero back-gate voltage ($V_{BG}$ = 0 V) and the inset shows the transfer characteristic at a source drain bias of 0.1V. Device width and gate length are 50 µm and 12 µm, respectively.

The $g_{m,max}$ values of BIGFETs are observed to be lower than the values reported for both exfoliated monolayer and bilayer GFETs, which can be understood by the fact that the BIGFET channel consists of stacked CVD graphene monolayers. Average $g_m$ values of CVD graphene monolayer GFETs are lower than values reported for exfoliated pristine graphene monolayer GFETs [16]. In contrast to stacked bilayer GFETs, Bernal stacked bilayer GFETs demonstrate an increasing $g_{m,max}$ trend because of the electrically tunable band gap [7], which is absent in stacked bilayer channels of a BIGFET.

Fig. 5 compares several of the measured BIGFETs in terms of $g_{m,max}$ and $g_{d,min}$ values at various back gate voltages. Devices with different gate lengths ($L_g$), channel widths (W) and top gate dielectrics ($SiO_2$ and $Al_2O_3$) were analyzed. Independent of the gate dielectric, we observe a back gate voltage dependence of $g_{m,max}$ that is weaker than in Bernal stacked bilayer devices [7]. No clear trend is observable for the output conductance $g_{d,min}$. Table 1 summarizes the observations about intrinsic voltage gain $g_{m\_max}/g_{d\_min}$ in BIGFETs compared to the reported literature data in [7].

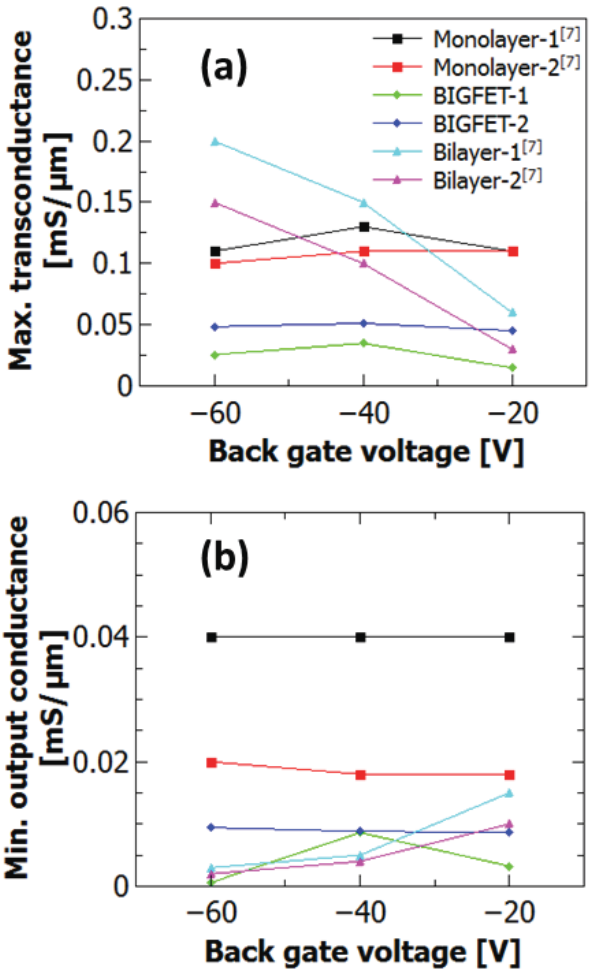



Fig. 4. (a) Maximum DC transconductance and (b) minimum output conductance values measured at different back gate voltages for BIGFETs with a gate length of 12 μm and channel width of 60 μm each. The data, normalized per unit width, is compared with monolayer and bilayer GFETs reported in [7]. Both the monolayer and bilayer graphene in [7] were exfoliated whereas the devices reported in this work were fabricated from CVD graphene. The magnitude of minimum output conductance values was observed to be closer to Bernal stacked bilayer GFET case.

TABLE I. COMPARISON OF MAXIMUM INTRINSIC VOLTAGE GAIN FIGURES FOR VARIOUS DEVICE TYPES

| Device type | Maximum intrinsic gain (dB) |
|---|---|
| Monolayer GFET | 6 [7] |
| BIGFET | Between 2.5 to 28.84 |
| Bilayer GFET | 35 [7] |

Using the simple model proposed in [17] for monolayer graphene FETs, the carrier densities were calculated from transfer characteristics with reference to the measured Dirac point voltage. For initial studies the same equation was assumed valid for the mechanically stacked bilayer case as well. The peak carrier density, in a BIGFET channel, was found to increase by an order of magnitude from ~$10^{12}$ to ~$10^{13}$ $cm^{-2}$ with applied $V_{BG}$. A summary of the calculated maximum induced carrier density values are shown in Table 2. According to drift-diffusion transport model, an increased carrier density would mean a decrease in carrier velocity in the channel, which might be one of the possible reasons for enhanced saturation tendency observed in these devices.

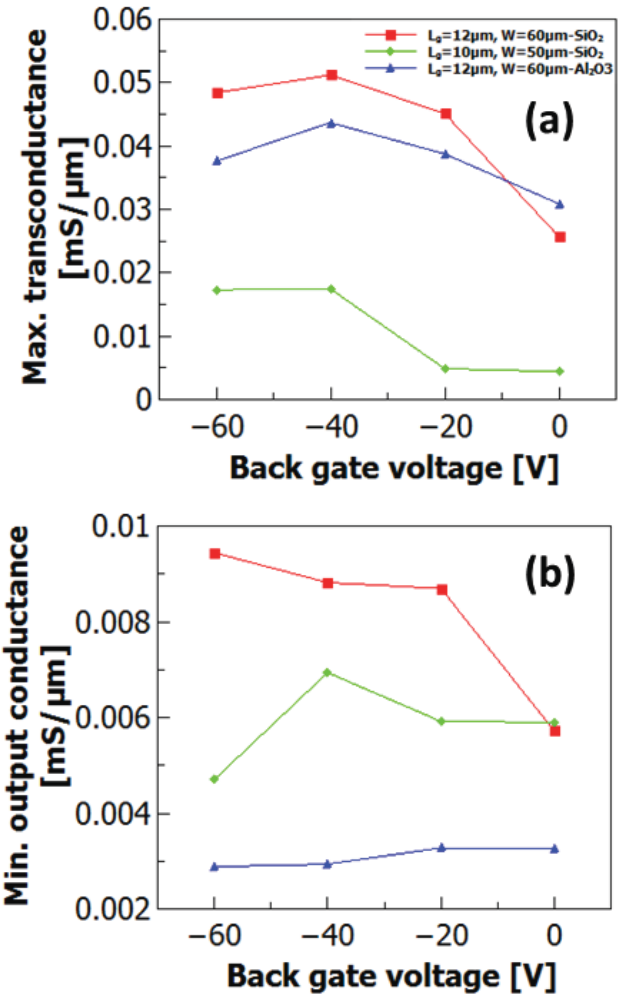



Fig. 5. (a) Maximum DC transconductance and (b) minimum output conductance values measured at different back gate voltages for BIGFETs with different gate lengths & channel widths. The data is normalized per unit width in order to make it comparable with each other. One GFET with $Al_2O_3$ gate dielectric is also compared. It was observed that devices with $Al_2O_3$ dielectric demonstrated smoother trends than devices with $SiO_2$ dielectrics.

TABLE II. COMPARISON OF MAXIMUM INDUCED CARRIER DENSITIES IN BIGFET CHANNELS

| Device | Back gate voltage [V] | Maximum induced carrier density [$cm^{-2}$] |
|---|---|---|
| *BIGFET-1* | *-60* | *$2x10^{13}$* |
| *BIGFET-2* | *-60* | *$1.79x10^{13}$* |
| *BIGFET-3* | *-60* | *$1.64x10^{13}$* |

## IV. CONCLUSIONS

Randomly stacked bilayer graphene FETs have been experimentally investigated with regards to the intrinsic voltage gain as a figure-of-merit for analog circuit design. We observe back gate tunable $g_{m,max}$ behavior, which is much less

pronounced when compared with Bernal stacked bilayer FETs [7]. Nevertheless, the intrinsic voltage gain is higher than in monolayer GFETs, which may offer an improved maximum oscillation frequency ($f_{max}$) performance in radio frequency GFETs. In conclusion, these preliminary results indicate that stacked bilayer graphene can be a potential candidate for analog circuits working at higher operation frequencies. Nevertheless, further experiments and analysis will be needed to gain more insight into the observed saturation tendency in BIGFETs.

## ACKNOWLEDGMENT

This work is supported by German Research Foundation (DFG, LE 2440/1-1 & 2-1), by an ERC starting grant (InteGraDe, 307311) and by Spanish Ministry of Science & Innovation under projects RUE CSD2009-00046 and TEC2010-15765.

## REFERENCES

[1] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric Field Effect in Atomically Thin Carbon Films," *Science*, vol. 306, pp. 666–669, 2004.

[2] M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz, "A Graphene Field-Effect Device," *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 282–284, Apr. 2007.

[3] M. Iannazzo, V. Lo Muzzo, S. Rodriguez, H. Pandey, A. Rusu, M. Lemme, and E. Alarcon, "Optimization of a Compact I-V Model for Graphene FETs: Extending Parameter Scalability for Circuit Design Exploration," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3870–3875, Nov. 2015.

[4] S. Rodriguez, S. Vaziri, A. Smith, S. Fregonese, M. Ostling, M. C. Lemme, and A. Rusu, "A Comprehensive Graphene FET Model for Circuit Design," *IEEE Trans. Electron Devices*, vol. 61, no. 4, pp. 1199–1206, Apr. 2014.

[5] T. Zimmer and S. Fregonese, "Graphene Transistor-Based Active Balun Architectures," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 3079–3083, Sep. 2015.

[6] Y.-M. Lin, A. Valdes-Garcia, S.-J. Han, D. B. Farmer, I. Meric, Y. Sun, Y. Wu, C. Dimitrakopoulos, A. Grill, P. Avouris, and K. A. Jenkins, "Wafer-Scale Graphene Integrated Circuit," *Science*, vol. 332, no. 6035, pp. 1294–1297, Jun. 2011.

[7] B. N. Szafranek, G. Fiori, D. Schall, D. Neumaier, and H. Kurz, "Current Saturation and Voltage Gain in Bilayer Graphene Field Effect Transistors," *Nano Lett.*, vol. 12, no. 3, pp. 1324–1328, Mar. 2012.

[8] M. C. Lemme, L.-J. Li, T. Palacios, and F. Schwierz, "Two-dimensional materials for electronic applications," *MRS Bull.*, vol. 39, no. 08, pp. 711–718, Aug. 2014.

[9] H. Zhou, W. J. Yu, L. Liu, R. Cheng, Y. Chen, X. Huang, Y. Liu, Y. Wang, Y. Huang, and X. Duan, "Chemical vapour deposition growth of large single crystals of monolayer and bilayer graphene," *Nat. Commun.*, vol. 4, Jun. 2013.

[10] M. Y. Han, B. Ozyilmaz, Y. Zhang, and P. Kim, "Energy Band-Gap Engineering of Graphene Nanoribbons," *Phys. Rev. Lett.*, vol. 98, pp. 206805–4, 2007.

[11] S. Kataria, S. Wagner, J. Ruhkopf, A. Gahoi, H. Pandey, R. Bornemann, S. Vaziri, A. D. Smith, M. Ostling, and M. C. Lemme, "Chemical vapor deposited graphene: From synthesis to applications: Chemical vapor deposited graphene," *Phys. Status Solidi A*, vol. 211, no. 11, pp. 2439–2449, Nov. 2014.

[12] A. C. Ferrari, J. C. Meyer, V. Scardaci, C. Casiraghi, M. Lazzeri, F. Mauri, S. Piscanec, D. Jiang, K. S. Novoselov, S. Roth, and A. K. Geim, "Raman Spectrum of Graphene and Graphene Layers," *Phys. Rev. Lett.*, vol. 97, no. 18, Oct. 2006.

[13] J. Bai, L. Liao, H. Zhou, R. Cheng, L. Liu, Y. Huang, and X. Duan, "Top-Gated Chemical Vapor Deposition Grown Graphene Transistors with Current Saturation," *Nano Lett.*, vol. 11, no. 6, pp. 2555–2559, Jun. 2011.

[14] I. Meric, C. Dean, A. Young, J. Hone, P. Kim, and K. L. Shepard, "Graphene field-effect transistors based on boron nitride gate dielectrics," 2010, pp. 23.2.1–23.2.4.

[15] Z. H. Feng, C. Yu, J. Li, Q. B. Liu, Z. Z. He, X. B. Song, J. J. Wang, and S. J. Cai, "An ultra clean self-aligned process for high maximum oscillation frequency graphene transistors," *Carbon*, vol. 75, pp. 249–254, Aug. 2014.

[16] F. Schwierz, J. Pezoldt, and R. Granzner, "Two-dimensional materials and their prospects in transistor electronics," *Nanoscale*, vol. 7, no. 18, pp. 8261–8283, 2015.

[17] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field-effect transistors," *Nat. Nanotechnol.*, vol. 3, no. 11, pp. 654–659, Nov. 2008.

# Simulation Study on the Feasibility of Si as Material for Ultra-Scaled Nanowire Field-Effect Transistors

Z. Stanojević, O. Baumgartner, M. Karner, F. Mitterbauer, H. Demel, and C. Kernstock
Global TCAD Solutions GmbH, Landhausgasse 4/1a, 1010 Wien, Austria
(z.stanojevic|o.baumgartner|m.karner|h.demel|c.kernstock)@globaltcad.com

***Abstract*—We present a simulation framework which allows thorough performance evaluation of ultra-scaled devices. Our simulation approach is based on the full solution of the Boltzmann transport equation (BTE) on subbands as calculated from a k·p-Hamiltonian and including all relevant scattering mechanisms which occur in semiconductors at room temperature. We employ the simulation framework to investigate the performance limits of silicon-based technology for ultra-scaled field-effect transistors in logic applications.**

## I. Introduction

⟨110⟩-oriented channels have been reported to exhibit superior performance due to their lower transport-effective-mass and thus higher *low-field* mobility compared to ⟨100⟩-orientation channels - both for electrons [1] and holes [2]. However, ⟨110⟩-oriented channels also exhibit higher non-parabolicity which counteracts the mobility enhancement when *high-field* transport is considered.

The first objective of this study attempts to give a more comprehensive comparison between ⟨100⟩ and ⟨110⟩-oriented, based on device characteristics rather than channel mobilities.

The second objective of this study is to shed some light on the prospective device performance of silicon as channel material towards the end of scaling, exploring what the limits to silicon-based transistors can be expected down the road.

## II. Modeling Tools

The simulation framework is based on our previous work on mobility modeling in nano-device channels [3, 4, 5], where we developed the representation of the full scattering operator in **k**-space based on either an effective-mass or a **k**·**p** subband structure.

We have also extended the above methods to non-Si materials and to include entire devices using a channel-slicing technique combined with low-field coupling [6]. However, low-field coupling is not sufficient to model current at high source-drain bias and, in particular, the on-current of a device.

To enable the simulation of the high-$V_{DS}$ characteristics of a device, one additional ingredient to the simulation framework has been developed: a subband-BTE solver. The solver operates in *phase space*, i.e. tensor product of real and **k**-space. For a nano-device, the effective dimension is reduced by confinement; e.g. for a nanowire-device both real and **k**-space are 1D, comprising a 2D phase space.

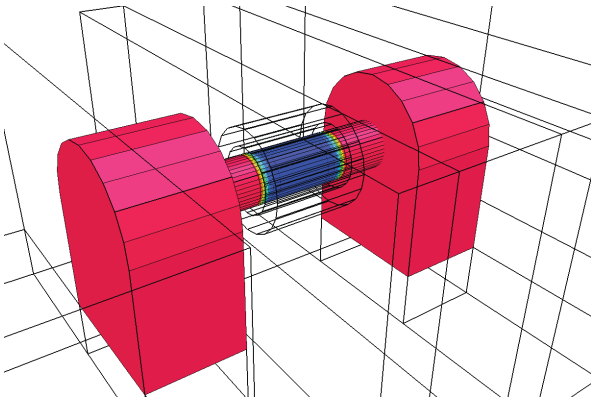


Fig. 1. Test device - a gate-all-around nanowire transistor; the gate stack is comprised of $SiO_2$/$HfO_2$ layers and a metal gate. The colors indicate doping which is $1 \times 10^{20}\,\mathrm{cm}^{-3}$ in the source and drain regions and $1 \times 10^{12}\,\mathrm{cm}^{-3}$ in the channel.

The BTE is discretized on the phase-space grid using **k** rather than energy as coordinate. The phase-space formalism allows simulation on any numerically obtained dispersion relation, such as one provided by a **k**·**p** or tight-binding subband structure tool. The **k**-space discretization also applies to the scattering operator. This accurately captures a number of band-structure-related effects: (i) anisotropy of band structure, (ii) non-monotonicity or *subband warping* commonly occurring in valence subbands, and (iii) strain effects on subband energies and curvatures within **k**·**p** theory.

Non-polar phonon scattering (acoustic and optical), polar-optical phonon scattering, remote phonon scattering, ionized impurity scattering, remote Coulomb scattering, and surface roughness scattering can be included.

All the involved components - subband structure, scattering operator, subband-BTE, self-consistent iteration - have been implemented in the simulators Minimos-NT [7] and VSP [8, 9] as provided by GTS Framework [10].

## III. Results

We examined Si nanowire transistors of both NMOS and PMOS type, as depicted in Fig. 1. The channels are 4 nm wide, 8 nm long, and fitted with a $SiO_2$/$HfO_2$/metal gate stack.

ISBN 978-1-4673-8608-1  IEEE Catalog number CFP1649D-USB

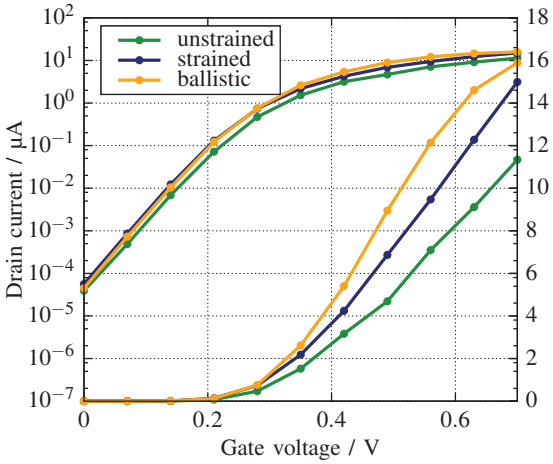



Fig. 2. Transfer characteristic of the n-type device at $V_{DS} = 0.7\,V$; applying *tensile* stress of 1.5 GPa along the ⟨110⟩ channel reduces the transport mass and thus increases on-current. The unstrained ballistic current is also shown for reference.

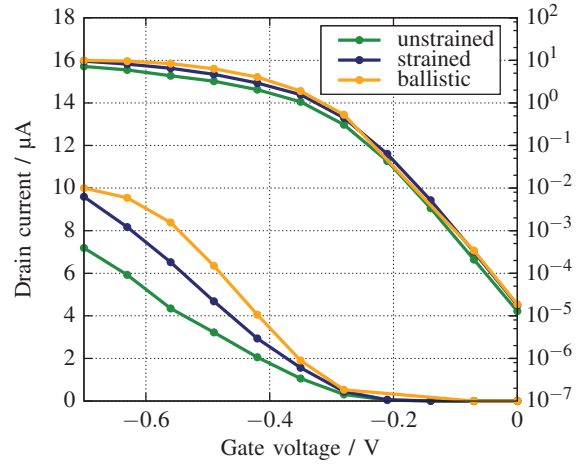



Fig. 3. Transfer characteristic of the p-type device at $V_{DS} = -0.7\,V$; applying *compressive* stress of 1.5 GPa along the ⟨110⟩ channel reduces the transport mass and thus increases on-current. The unstrained ballistic current is also shown for reference. Although ⟨110⟩ channel orientation improved PMOS performance, the improvement is not sufficient to match the NMOS device.

Two channel orientations, ⟨100⟩ and ⟨110⟩, were considered for both types of devices.

The transfer characteristics for ⟨110⟩-oriented devices of both n and p-type, computed at a source-drain bias of 0.7 V, are shown in Figs. 2 and 3. The calculations were done self-consistently with the electrostatic potential. For both devices, the characteristic was obtained (i) for an unstrained device including scattering (non-polar phonons, impurities, surface roughness), (ii) for the ballistic limit of the unstrained device, and (iii) for a device with 1.5 GPa stress applied along the channel axis - *tensile* for NMOS, *compressive* for PMOS.

The distribution functions at $V_G - V_{th} = 0.05\,V$ are shown in Figs. 4 and 5 for n and p-type device, both with and without scattering.

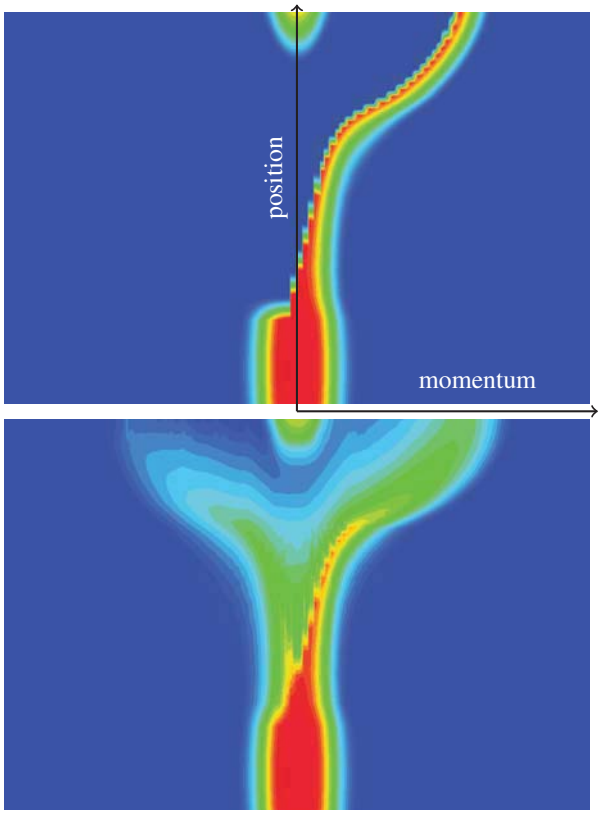



Fig. 4. Phase-space plot of the distribution function in the lowest subband for the ⟨110⟩-oriented **n-type** transistor; gate bias is set to 0.05 V above threshold. The ballistic (top) and dissipative (bottom) transport regimes are shown. The horizontal axis corresponds to momentum or **k**, while the vertical axis corresponds to the position along the channel.

### *A. Strain-induced current enhancement*

Figures 2 and 3 shows that in both cases the applied stress along the ⟨110⟩-oriented channel increases the output current, although the question remains whether there is a mechanically stable way to apply compressive stress to a nanowire channel. The on-current increase for both types of devices is roughly 20 % at 1.5 GPa stress. However, even with the increase, the PMOS current is below that of the NMOS device by roughly a factor of two. To achieve a balanced CMOS circuit, two PMOS transistors are required to complement one NMOS.

### *B. Scaling behavior*

To investigate the limits of integration for silicon-based gate-all-around transistors, a series of differently sized transistors were simulated. Both device types, NMOS and PMOS, were considered, as well as both channel orientations, ⟨100⟩ and ⟨110⟩. The ratio of channel length to channel diameter was kept constant at 2:1 to preserve behavior in the off-state.

Figures 6 and 7 show the ballistic and dissipative on-currents of the n and p-type devices, respectively, as a function of channel length. As the channel length (and, proportionally, the channel diameter) becomes smaller the on-current in the device degrades. It is important here to separate the current

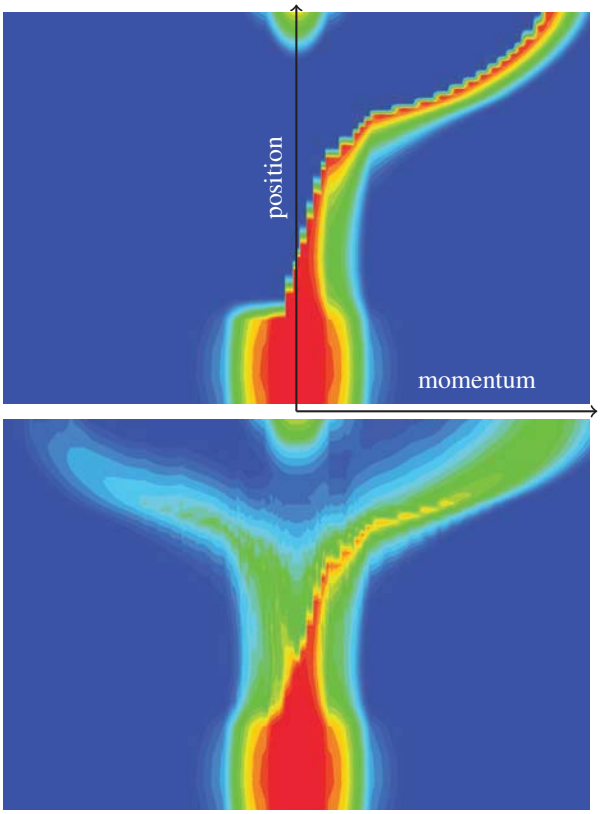



Fig. 5. Phase-space plot of the distribution function in the lowest subband for the ⟨110⟩-oriented **p-type** transistor; gate bias is set to 0.05 V above threshold. The ballistic (top) and dissipative (bottom) transport regimes are shown. The horizontal axis corresponds to momentum or **k**, while the vertical axis corresponds to the position along the channel.

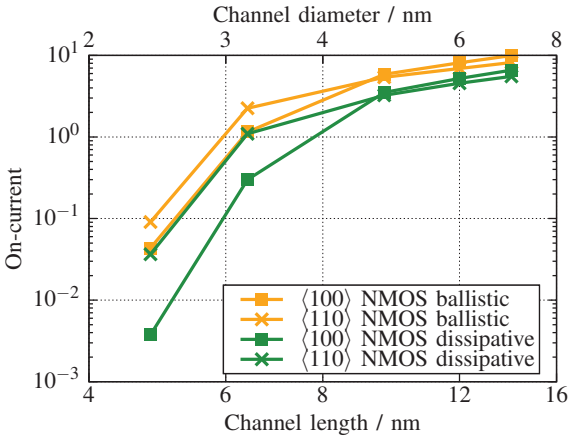



Fig. 6. Drain current of the NMOS transistors for different channel lengths

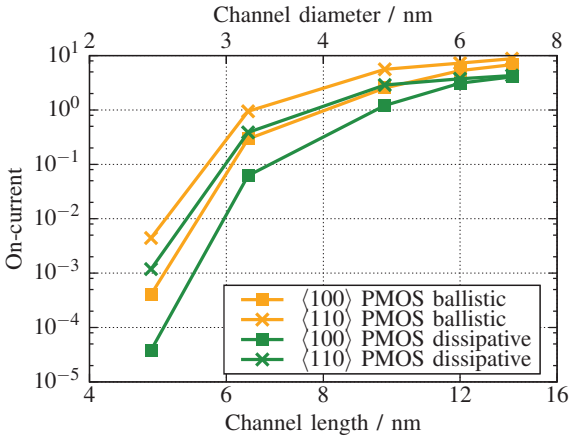



Fig. 7. Drain current of the PMOS transistors for different channel lengths

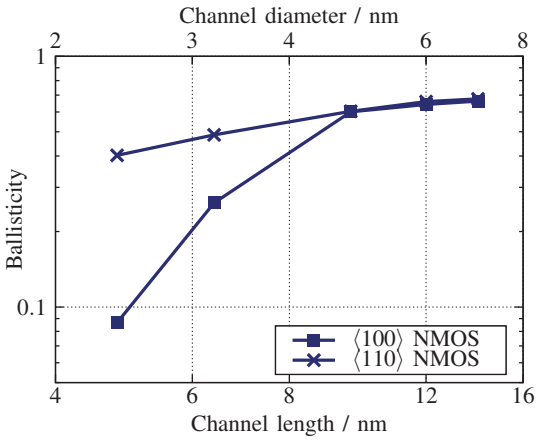



Fig. 8. Ballisticity of the NMOS transistors for different channel lengths

degradation from a shift in threshold voltage. The latter occurs due to an increase of the ground state energy as the channel diameter decreases. To avoid the confusing the two effects all devices were biased well beyond their respective threshold voltages and kept at high saturation.

Both the ballistic and dissipative currents degrade with decreasing device size, which means that scattering is not the main source of degradation. Figures 8 and 9 show the ballisticity or ballistic ratio, i.e. the ratio of dissipative to ballistic current, for the NMOS and PMOS devices, respectively, where ballisticity is also shown to degrade for very small devices. However, the ballisticity degradation happens at a different rate than the overall current degradation and appears to peak around 15 nm channel length (10 nm for ⟨110⟩ PMOS). Also, the ballisticity degradation is much stronger for ⟨100⟩-oriented than for ⟨110⟩-oriented channels in both the NMOS and PMOS case. ⟨110⟩-oriented PMOS transistors show less ballisticity degradation but a lower peak ballisticity the ⟨100⟩-oriented ones.

Generally, for 12 nm channel length and above ⟨100⟩-oriented devices show equal or slightly better on-current than their ⟨110⟩-oriented counterparts. However, below 12 nm, the ⟨110⟩-oriented device exhibit a significant performance advantage.

ISBN 978-1-4673-8608-1

IEEE Catalog number CFP1649D-USB

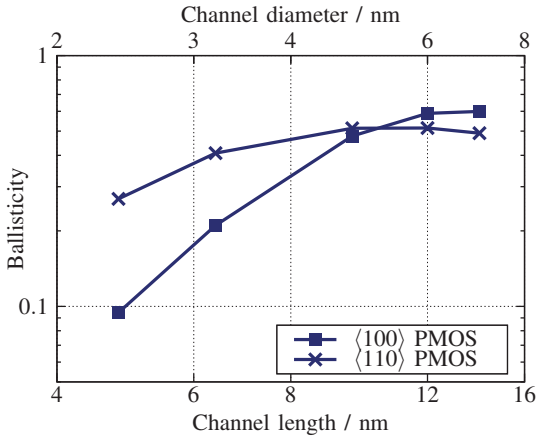



Fig. 9. Ballisticity of the PMOS transistors for different channel lengths

## IV. Discussion

The on-current degradation effects described in the previous section are a result of decreasing density of states for shrinking channel diameters. The effect is also known as *quantum resistance* and has been discussed in [11]. Experimental evidence of this effect has been reported for InGaAs [12] and Si [13] channels.

In the ballistic limit, each populated subband contributes a *conductance quantum* of $2q_0^2/h$. Thus the quantum resistance of the channel wiht $N$ subbands reads

$$R_{\mathrm{q}} = \frac{h}{2Nq_0^2}.$$

This is consistent with our observations for the ballistic current. Here ⟨110⟩-oriented channels show somewhat less degradation than the ⟨100⟩-oriented channels - for both electrons and holes. This can be explained by the closer energy-spacing between subbands for ⟨110⟩-oriented channels compared to ⟨100⟩-oriented channels [14], resulting in more populated subbands.

## V. Conclusion

First, we presented a novel computational framework that includes all relevant band structure, scattering, and high-field transport effects in a self-consistent simulation. The purpose of the developed framework is the predictive evaluation of device current at high source-drain biases. The capabilities of the framework have been demonstrated on the examples of next-gen Si NMOS and PMOS transistors.

Second, we have investigated the performance limits for ultra-scaled silicon-based GAA MOSFETs. We demonstrated that while on-current degrades for all devices due to quantum resistance, ⟨110⟩-oriented channels provide a significant performance advantage compared to ⟨100⟩-oriented devices below 12 nm channel length.

## References

[1] Z. Stanojevic, M. Karner *et al.*, "Exploring the Design Space of Non-Planar Channels: Shape, Orientation, and Strain," in *Intl. Electron Device Meeting*, 2013, pp. 332–335.

[2] N. Neophytou and H. Kosina, "Large Enhancement in Hole Velocity and Mobility in p-Type [110] and [111] Silicon Nanowires by Cross Section Scaling: An Atomistic Analysis," *Nano Letters*, vol. 10, no. 12, pp. 4913–4919, 2010.

[3] Z. Stanojević, O. Baumgartner *et al.*, "Consistent low-field mobility modeling for advanced MOS devices," *Solid-State Electronics*, vol. 112, pp. 37 – 45, 2015, selected Papers from EuroSOI'2014 Conference.

[4] Z. Stanojevic, O. Baumgartner *et al.*, "On the Validity of Momentum Relaxation Time in Low-Dimensional Carrier Gases," in *SISPAD*, 2014, pp. 181–184.

[5] Z. Stanojevic and H. Kosina, "Surface-Roughness-Scattering in Non-Planar Channels – the Role of Band Anisotropy," in *Intl. Conf. on Simulation of Semiconductor Processes and Devices*, 2013, pp. 352–355.

[6] Z. Stanojević, M. Karner *et al.*, "Predictive Physical Simulation of III/V Quantum-Well MISFETs for Logic Applications," in *Proceedings of the ESSDERC 2015*, 2015, pp. 310–313.

[7] Global TCAD Solutions, "Minimos-NT," http://www.globaltcad.com/minimos-nt.

[8] O. Baumgartner, Z. Stanojevic *et al.*, "VSP–a quantum-electronic simulation framework," *J. Comput. Electron.*, vol. 12, pp. 701–721, 2013.

[9] Global TCAD Solutions, "Vienna Schrödinger-Poisson," http://www.globaltcad.com/vsp.

[10] Global TCAD Solutions, "GTS Framework," http://www.globaltcad.com/framework.

[11] N. Neophytou, Z. Stanojevic *et al.*, "Full Band Calculations of Low-field Mobility in p-type Silicon Nanowire MOSFETs," in *Proceedings of the 18th International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, 2013, pp. 81–84, talk: International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Glasgow, Scotland, United Kingdom; 2013-09-03 – 2013-09-05.

[12] N. Neophytou, T. Rakshit *et al.*, "Performance Analysis of 60-nm Gate-Length III-V InGaAs HEMTs: Simulations Versus Experiments," *Electron Devices, IEEE Transactions on*, vol. 56, no. 7, pp. 1377–1387, July 2009.

[13] Runsheng Wang, Hongwei Liu *et al.*, "Experimental Investigations on Carrier Transport in Si Nanowire Transistors: Ballistic Efficiency and Apparent Mobility," *Electron Devices, IEEE Transactions on*, vol. 55, no. 11, pp. 2960–2967, Nov 2008.

[14] Z. Stanojevic, O. Baumgartner *et al.*, "Electronic band structure modeling in strained Si-nanowires: Two band k·p versus tight binding," in *Computational Electronics (IWCE), 2010 14th International Workshop on*, Oct 2010, pp. 1–4.

# GDNMOS: A new high voltage device for ESD protection in 28nm UTBB FD-SOI technology

S. Athanasiou[1,2], Charles-Alexandre Legrand[1], S. Cristoloveanu[2], Ph.Galy[1]
[1]STMicroelectronics, 850 rue Jean Monnet, 38920 Crolles, France
[2] IMEP, 3 Parvis Louis Néel, CS 50257, 38016 Grenoble Cedex 1, France

***Abstract*— We propose a novel device (GDNMOS: Gated Diode merged NMOS) fabricated with 28nm UTBB FD-SOI high-k metal gate technology. Variable electrostatic doping (gate-induced) in diode and transistor body enables reconfigurable operation, in particular in thyristor mode. This innovative architecture demonstrates excellent capability for high-voltage protection while maintaining a latch-up free behavior.**

***Index Terms* - ESD, FD-SOI, Gated Diode, MOSFET, Thyristor, SOI, CMOS**

## 1. Introduction

Recent advances in Fully Depleted SOI (FD-SOI) technology [1] continue to shrink the design window [2] of ElectroStatic Discharge (ESD) protection devices, reducing supply voltage $V_{dd}$ and decreasing breakdown voltage $V_{Br}$. This window is highly dependent on the type of devices to be protected, as well as on the region of operation. Contrary to the typical SOI-Bulk hybridization techniques [3] the focus of this work is on FD-SOI. Previous studies have been conducted on thin film BiMOS device [4, 5, 6] or band modulation devices [7] for protection of circuits operating in typical voltage range for FD-SOI technology.

In this work, we present an original structure for high voltage protection that combines diode and MOSFET mechanisms. Electrical measurements prove the flexibility, robustness and functionalization of the GDNMOS. 3D TCAD [8] simulations reveal the details of the operation mechanisms.

## 2. Device structure and properties

GDNMOS is composed of a typical FD-SOI nMOSFET merged with an FD-SOI p-i-n gated diode. There is a common n-type area which acts as the diode cathode and as the MOSFET drain. The ultrathin bodies of the diode and transistor can be electrostatically doped ($N^+$ or $P^+$, by attracting different types of carriers in the 'intrinsic' region below the gate) via the gates or back-plane bias.

During a stress, the trigger voltage is dependent on the sum of the common base current gain (α) of the 2 bipolar transistors. In a typical n-p-n device the common base current gain can be defined as [9]:

$$\alpha = \frac{i_C}{i_E}, \alpha_{NPN} = \gamma_E * a_T * \gamma_C \quad (1)$$

where $\gamma_E$ is the emitter efficiency, $a_T$ is the base transport factor, and $\gamma_C$ is the collector efficiency:

$$\gamma_E = \alpha_E = \frac{J_n(0)}{J_n(0)+J_p(0)} = \frac{D_{nB}L_{pE}n_{iB}^2 N_{DE}}{D_{nB}L_{pE}n_{iB}^2 N_{DE}+D_{pE}W_B n_{iE}^2 N_{AB}} \quad (2)$$

where L and D are the diffusion length and constant for a type of carrier, $n_i$ is the intrinsic carrier density and N is the doping concentration. All of the aforementioned values are indicated with a subscript for a specific area of the BJT: E (Emitter), B (Base), C (Collector). In order to increase the thyristor efficiency we have to enhance the emitter efficiency for each BJT. This can be done by shrinking the gate length (by design) or by lowering the acceptor doping in base area (by biasing).

Our main purpose is to take advantage of such reconfigurable behavior for emulating a PNPN thyristor structure: positively biased $P^+$ anode, floating $N^+$ drain, P MOSFET body, grounded $N^+$ source (Fig. 1). Test devices (Fig. 2) were fabricated with the 28nm FD-SOI STMicroelectronics process featuring an ultra-thin silicon film of 7nm, ultra-thin BOX of 25nm, high-k metal gate stack and p-type backplane (p-BP). The devices were processed with different gate stack options: Standard Gate (SG, EOT=1.1nm) and Extended Gate (EG, EOT=3.4nm). In DEV1, 2, 3 structures the MOS gate and the diode gate were interconnected, while in DEV4, 5, 6 they were independent. In the mixed gate stack devices, the gate oxide of the diode was always selected to be thick (EG), for increased robustness to the stress applied to anode. Minimum process-compliant gate dimensions were selected and compared to longer gates.

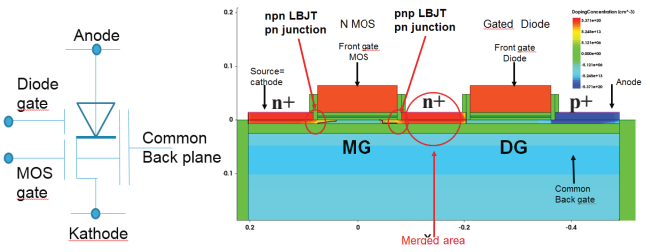
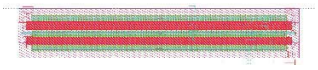



Figure 1: Schematic (left) and cross-section (right) of GDNMOS structure.



| | MOS Gate | Diode Gate | Lg1 | Lg2 | MG-DG2 | Biasing |
|---|---|---|---|---|---|---|
| DEV1 | SG | SG | 45nm | 45nm | conn | 2V |
| DEV2 | SG | EG | 30nm | 150nm | conn | 4V |
| DEV3 | EG | EG | 150nm | 150nm | conn | 4V |
| DEV4 | SG | SG | 45nm | 45nm | separ | 2V |
| DEV5 | SG | EG | 30nm | 150nm | separ | 4V |
| DEV6 | EG | EG | 150nm | 150nm | separ | 4V |

Figure 2: **Top**: typical GDNMOS layout. **Bottom:** different device configurations fabricated.

### 3. Simulation results

The 28nm FD-SOI GDNMOS was meshed in 3D (Fig. 1) for different gate stack configurations. We consider phonon scattering, Coulomb scattering in doped materials, and mobility degradation due to high field saturation and high temperature. Other active modules include avalanche model as well as Auger recombination model. For the simulation study, the surge is an ACS stress with 1A max current and 100ns rise time, which is equivalent to the transmission line pulse (TLP) test for human body model (HBM) [10].

Fig. 3 shows typical I-V characteristics resulting from ACS simulation. The differentiation between the mixed SG-EG gate stacks and EG-EG gate stacks is observed as well as the effect of floating versus grounded/biased gate terminals. At the end of the stress, current density reaches the maximum value with conduction through the whole film (volume inversion, Fig.4).

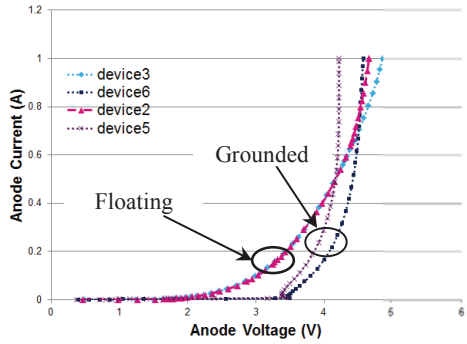



Figure 3: ACS I-V TCAD simulation for devices 2, 3, 5 and 6.

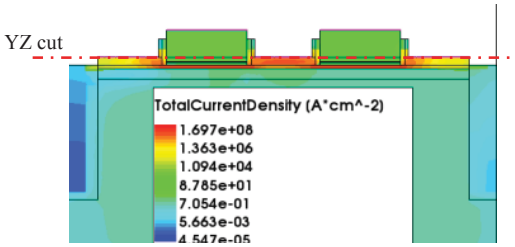



Figure 4: Current density extracted at the end of ACS stress for device 6, grounded gates. Volume conduction is visible.

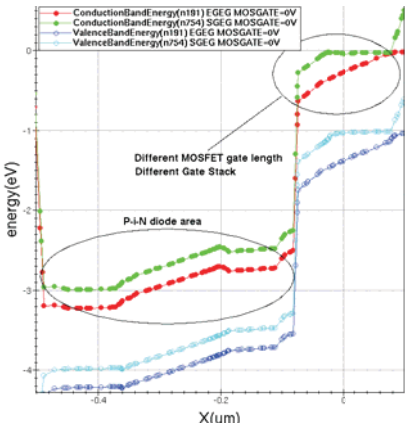



Figure 5: Energy band diagram (YZ cut) at the end of ACS I-V TCAD simulation for devices 5 and 6.

Figure 5 shows the band diagram at the end of an ACS stress for grounded nMOSFET gate and diode gate. There is a significant bending of the bands due to the high drop voltage (more than 4V). Also we observe the difference due to using different gate stacks for the nMOSFET with different lengths. This band bending is especially pronounced between the merged area and the nMOSFET gate, leading to increased band-to-band tunneling (Fig. 6).

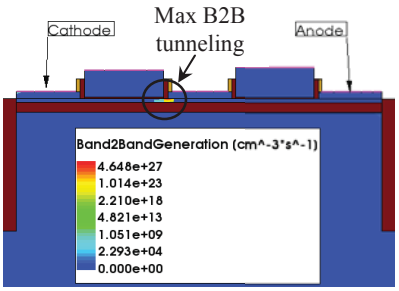



Figure 6: Band-to-Band tunneling generation at the end of ACS stress.

### 4. Measurements and discussion

The devices were tested in static and TLP [11] modes under different conditions. TLP measurements had duration of 100ns or 10ns and native or 10ns rise time. The stress was applied on anode, while cathode was grounded. The gates were either grounded or floating. Our primary goal is to investigate the ESD behavior of the various structures and evaluate the efficiency of the floating-body (without base contact) lateral thyristor.

For the first type of devices (Fig. 7, 8, 9) with the two gates connected, we observe clear snapback characteristics. The fluctuations on I-V response are attributed to the coupling during the transient TLP stress between the two different gate stacks. This effect is not observed in devices (Fig. 10, 11, 12) that have separate MOS and diode gates, even for identical biasing conditions. For these structures there is no systematic differentiation between 100ns and 10ns TLP I-V curves. No strong snapback behavior is observed primarily due to the lack of direct control on the Emitter-Base p-n junctions of the Lateral Bipolar Junction Transistors (LBJT between source and drain) as well as the relatively high doping of LBJT base in the merged area. The selection of gate stack affects strongly the breakdown voltage of the device (Fig. 13) with EG gate stack devices exhibiting higher breakdown voltage and lower leakage (Fig. 14, 15). In terms of performance DEV5, 6 provide the best performance with higher $I_{t2}$, lower leakage and higher breakdown voltage.

Additionally, by utilizing variable biasing on MOS gate (MG) we can achieve different behavior during a TLP stress as seen in Fig. 16. By biasing the nMOSFET gate we modulate the nMOSFET lateral BJT gain. The combined gain of the 2 BJTs is limited due to the high doping in the merged area (BJT base), resulting in a lower gain for the BJT formed with the gated diode. We show that doping calibration as well as gate and backplane biasing schemes modulate the thyristor operation leading to further improvement of the ESD stress responses. We benchmark its performance with that of alternative devices proposed for ESD protection in ultrathin FD-SOI.

ISBN 978-1-4673-8608-1

IEEE Catalog number CFP1649D-USB

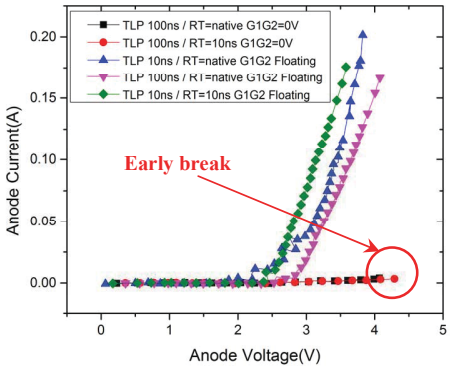



Figure 7: Device1 TLP measurements for different rise times: 100ns and 10ns.

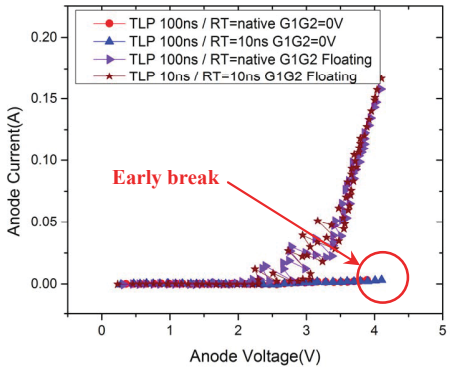



Figure 8: Device2 TLP measurements for different rise times: 100ns and 10ns.

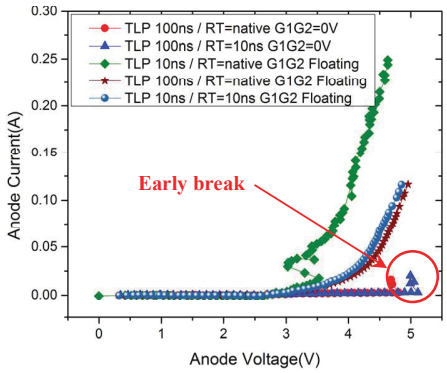



Figure 9: Device3 TLP measurements for different rise times: 100ns and 10ns.

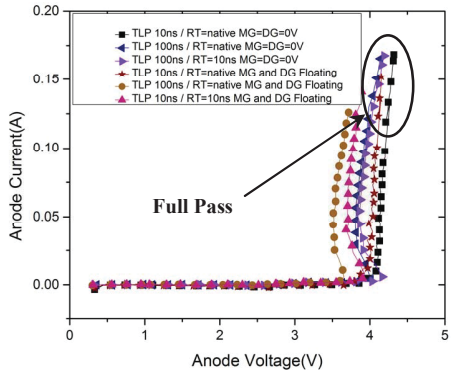



Figure 10: Device4 TLP measurements for different rise times: 100ns and 10ns.

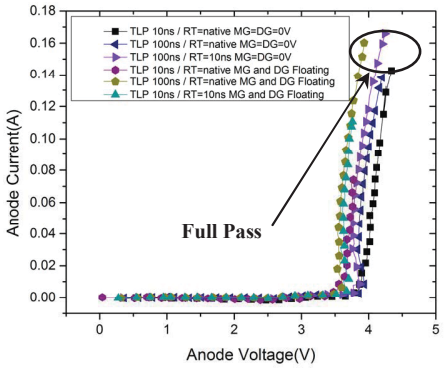



Figure 11: Device5 TLP measurements for different rise times: 100ns and 10ns.

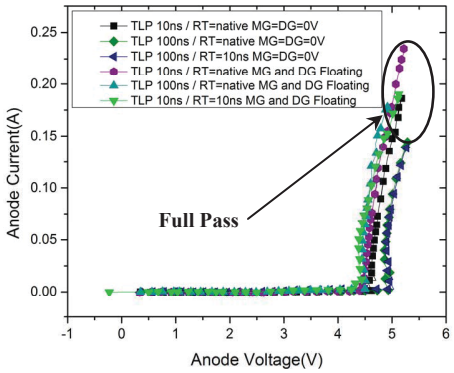



Figure 12: Device6 TLP measurements for different rise times: 100ns and 10ns.

| | Vt1 | It1 | It2 | Vhold | $V_{BR}$ |
|---|---|---|---|---|---|
| DEV1 GND | NA | NA | <20mA | NA | 3.1V |
| DEV1 FLT | NA | NA | <180mA | NA | NA |
| DEV2 GND | NA | NA | <20mA | NA | 4.2V |
| DEV2 FLT | NA | NA | <180mA | NA | NA |
| DEV3 GND | NA | NA | <20mA | NA | 4.8V |
| DEV3 FLT | NA | NA | <120mA | NA | NA |
| DEV4 GND | 4V | NA | >160mA | 4V | 4.3V |
| DEV4 FLT | 4V | NA | >140mA | 4V | NA |
| DEV5 GND | 3.5V | NA | >160mA | 3.5V | 4.3V |
| DEV5 FLT | 3.5V | NA | >140mA | 3.5V | NA |
| DEV6 GND | 4.5V | NA | >160mA | 4.5V | 4.9V |
| DEV6 FLT | 4.3V | NA | >140mA | 4.3V | NA |

Figure 13: Extracted results for different gate biasing and configurations. We observe the improved performance with last 3 implementations. These devices exhibit higher $I_{t2}$, improving robustness during an ESD event.

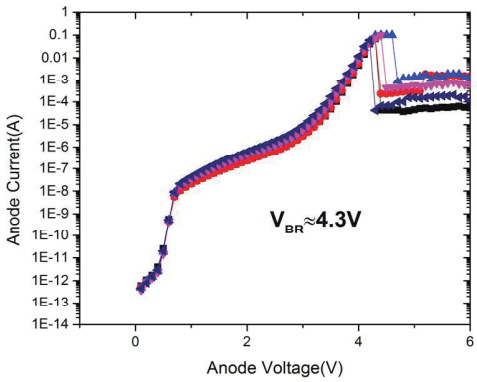



Figure 14: Device5 DC sweep with grounded MG and DG for breakdown voltage extraction at room temperature.

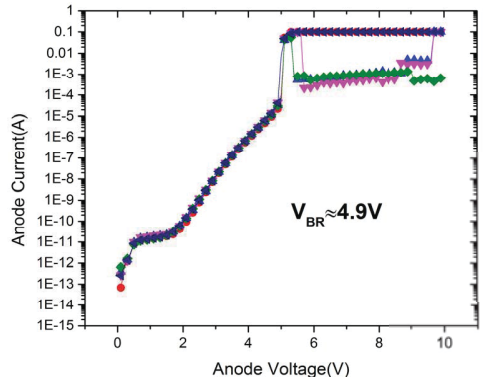



Figure 15: Device6 DC sweep with grounded MG and DG for breakdown voltage extraction at room temperature.

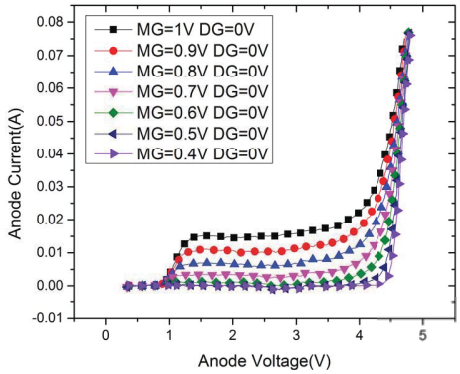



Figure 16: Device6. TLP 100ns, 10ns rise time with different MG biasing.

Furthermore, it is possible to show that one of the critical parameters in this device is the doping concentration of the merged area. This area acts like the base of the first p-n-p type BJT of the thyristor with its doping and width reversely proportional to bipolar gain, as seen in equation 2. TCAD simulations show a remarkable shift of the I-V curve with snapback behavior, when this doping is decreased (Fig. 17). The reason for this shift is the increase in emitter efficiency and base transport factor of the gated diode BJT.

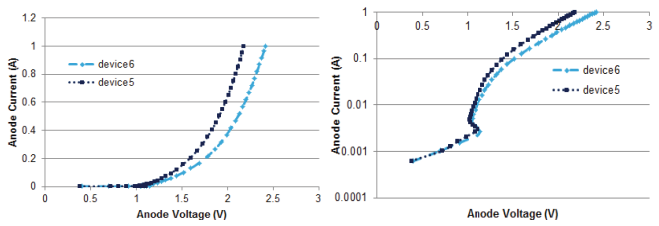



Figure 17: ACS I-V TCAD simulation for devices 5 and 6. Left: Linear plot, Right: Semi log plot

## 5. Conclusion

In this work, we present the ultrathin film GDNMOS device whose behavior was evaluated using both simulations and measurements. No latch-up is observed and the device can be used for high-voltage protection due to its simple integration on thin film and process compliance. The GDNMOS shows promising characteristics and remarkable versatility for adoption in the FD-SOI technology.

## 6. Acknowledgements

We would like to thank N. Planes for FD-SOI wafer fabrication and procurement, Dr. Olivier Bon and the rest of ST mask generation team for support. We would also like to thank our colleagues Dr. J. Bourgeat, B. Heitz and Dr. Nicolas Guitard for insight and expertise that proved beneficial for this project. Support from EU project WayToGoFast was highly appreciated.

## References

[1] N. Planes et al, “28nm FDSOI Technology Platform for High-Speed Low-Voltage Digital Applications”, Symposium on VLSI Technology (VLSIT), Jun 2012, Honolulu, US, pp. 133 – 134

[2] T. Benoist et al., “Experimental investigation of ESD design window for fully depleted SOI N-MOSFETs,” Microelectronic Engineering, vol. 88, no. 7, pp. 1276–1279, 2011.

[3] D. Golanski et al., “First demonstration of a full 28nm high-k/metal gate circuit transfer from Bulk to UTBB FDSOI technology through hybrid integration,” in Symposium on VLSI Technology (VLSIT), 2013, pp. T124–T125

[4] Ph. Galy et al. “BIMOS transistor in thin silicon film and new solutions for ESD protection in FDSOI UTBB CMOS technology”, EurosoiUlis 2015 Italy.

[5] S. Athanasiou et al, “Impact of back plane on the carrier mobility in 28nm UTBB FDSOI devices, for ESD applications”, EurosoiUlis 2015 Italy.

[6] S. Athanasiou et al, “Preliminary 3D TCAD Electro-thermal Simulations of BIMOS transistor in thin silicon film for ESD protection in FDSOI UTBB CMOS technology”, ICICDT 2015.

[7] Yohann Solaro et al, “Innovative ESD Protections for UTBB FD-SOI Technology”, Electron Devices Meeting (IEDM), 2013, Washington, US

[8] Synopsis Sentaurus TCAD, ver G-2012.06

[9] B. Jayant Baliga , “Fundamentals of Power Semiconductor Devices,” , Springer Publishing Company, Incorporated, 2008

[10] Ph. Galy et al. “Numerical evaluation between Transmission Line Pulse (TLP) and Average Current Slope (ACS) of a submicron gg-nMOS transistor under Electrostatic Discharge (ESD)”, Workshop EOS/ESD/EMI, LAAS-CNRS Toulouse, 2002

[11] T. Maloney and N. Khurana "Transmission line pulsing techniques for circuit modeling of ESD Phenomena", EOS/ESD Symposium Proceedings (1985), pp.49

# Operation of Suspended Lateral SOI PIN Photodiode with Aluminum Back Gate

Guoli Li[1,2], Nicolas André[1], Olivier Poncelet[1], Pierre Gérard[1], Syed Zeeshan Ali[3], Florin Udrea[3,4], Laurent A. Francis[1], Yun Zeng[2], and Denis Flandre[1]
[1]ICTEAM Institute, Université catholique de Louvain, 3 Place du Levant, 1348, Louvain-la-Neuve, Belgium
[2]School of Physics and Electronics, Hunan University, Changsha 410082, China
[3]Cambridge CMOS Sensors Ltd., Deanland House, Cowley Road, CB4 0DL, Cambridge, United Kingdom
[4]Department of Engineering, University of Cambridge, 9 JJ Thomson Avenue, CB3 0FA, Cambridge, United Kingdom
*Email:* guoli.li@uclouvain.be denis.flandre@uclouvain.be

***Abstract*—In this paper, we report a lateral silicon-on-insulator (SOI) $P^+P^-N^+$ (PIN) photodiode suspended on a micro-hotplate platform, with aluminum (Al) layer deposited on backside. Voltage applied to the Al back gate can modify the depletion condition in the intrinsic (I) region. The device output photocurrent reaches a maximum under fully-depleted (FD) condition achieved by the positive back-gate bias. Moreover, the backside Al acts as a excellent reflector, which for specific wavelength ranges (around 500, 600, 770 nm) significantly boosts optical response of the SOI PIN photodiode. Over 2~3× improvements of responsivity (up to *R* = 0.1 A/W at 590 nm) have been achieved and validated in the measurements at 490, 590, 760 nm. Full optoelectronic two-dimensional (2-D) device simulations are conducted in Atlas software to comprehensively validate the device performance and improvement.**

***Keywords—silicon-on-insulator (SOI); lateral PIN photodiode; fully-depleted (FD) condition; back gate; aluminum reflector; numerical simulation; Atlas.***

## I. INTRODUCTION

A wide interest emerges from monitoring systems in environmental [1] and biomedical [2] fields, for high-responsivity photodetectors embedded in CMOS integrated circuits. In silicon-on-insulator (SOI) technology, thin-film lateral $P^+/P^-/N^+$ (PIN) photodiode was often presented as an efficient photodetector to specifically absorb low wavelengths [3]. In such device, a PN junction is separated by an intrinsic (I) region which corresponds in practice to a weakly p-type doping.

Since light absorption of the thin-film SOI photodiode dramatically decreases with the increasing light wavelength (e.g. above 450 nm for 100 nm film thickness) [4], several methods have been proposed to improve device optical response: attaching gold nanoparticles for SOI lateral photodiode within 400-800 nm wavelength range [5], anti-reflective coating (ARC) on the front surface of device [6], resonant cavity effect (RCE) enhanced photodetector with a buried $SiO_2$ reflector [7] (achieving a peak responsivity of about 50 mA/W at 650 and 709 nm).

A lateral SOI PIN photodiode suspended on a micro-hotplate platform was presented in [8] and further investigated in [9], where a method using a standard device package with a gold finish layer was proposed to improve optical response of the suspended photodiode. In this work, we present the suspended lateral SOI PIN photodiode with Aluminum (Al) layer deposited on backside, where the backside Al is used as a gate electrode and also a back reflector.

The operation of the PIN photodiode, i.e. generation and collection of charge carriers, is strongly influenced by the depletion condition present in the I-region and also affected by the reflectance of the backside Al. Depletion regime in the I-region is induced by both positive back-gate voltage (i.e. vertical depletion region from the bottom to the top of silicon film) and reverse anode bias (i.e. lateral depletion region from the $P^-N^+$ junction) [10]. Carriers generated by light radiation in the I-region can be collected efficiently under fully-depleted (FD) conditon, maximizing the device output photocurrent. Taking advantage of excellent reflection of Al across the visible spectrum [11], the Al layer is also expected to act as a backside reflector and reflect light back into the active silicon film to improve light absorption.

Performances of the suspended lateral SOI PIN photodiode with backside Al layer deposited are comprehensively investigated in this paper, including electrical (with back gate bias) and optical (with backside reflection) characteristics. Full optoelectronics two-dimensional (2-D) device simulations are performed to further analyze and validate the device performance and potential improvement.

## II. DEVICE FABRICATION

The micro-hotplate platform was originally designed for gas [12] and humidity [13] sensing with interdigitated electrodes and specific sensing layers implemented at the device surface. A schematic cross section of lateral SOI PIN photodiode suspended on the micro-hotplate platform is depicted in Fig. 1, with Al layer deposited on device backside. Table I lists the superposed materials and their thicknesses. The PIN photodiode and micro-heater are embedded in a thick $SiO_2$ membrane (~5 μm) which was released by a post-CMOS deep reactive ion etching (DRIE) of the silicon substrate, where the 1 μm-thick buried oxide (BOX) acts as an effective etch-stop layer [14], ensuring high membrane uniformity. The additional 1 μm-thick Al layer was deposited on the backside of device samples in UCL clean rooms (WINFAB).

The photodetectors consist of several PIN finger diodes interdigitated in parallel over a given sensing area, with device geometries specified in Table II. Photodiodes with 3 different intrinsic lengths ($L_i$ = 5, 10 and 20 µm) are investigated in this paper, with 6, 4 and 2 parallel finger PIN diodes, respectively.

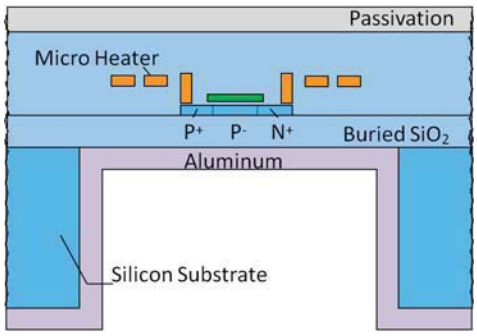



Fig. 1. Cross sectional view of SOI diode suspended on a micro-hotplate platform with Al back gate.

TABLE I. LIST OF MATERIALS AND THICKNESSES

| Function | Material | Thickness |
|---|---|---|
| Passivation | $Si_3N_4$ PECVD | 550 nm |
| Membrane | $SiO_2$ PECVD | 2.5 µm |
| Heater | Aluminum | 500 nm |
| Implantation protection | Polysilicon | 300 nm |
| Gate dielectric | $SiO_2$ | 25 nm |
| Active thin film | Silicon | 250 nm |
| BOX | $SiO_2$ | 1 µm |
| Substrate | Silicon | 375 µm |

TABLE II. PHOTODIODE GEOMETRIES

| Devices | $L_i$ (µm) | Fingers | $W_{fingers}$ (µm) | Effective area (µm × µm) | Total area (µm × µm) |
|---|---|---|---|---|---|
| M5 | 5 | 6 | 60 | 30 × 60 | 58 × 60 |
| M10 | 10 | 4 | 60 | 40 × 60 | 60 × 60 |
| M20 | 20 | 2 | 60 | 40 × 60 | 52 × 60 |

## III. EXPERIMENTAL CHARACTERIZATION

Device chips were mounted in a dual-in-line (DIL) 16 ceramic package and embedded in a printed circuit board (PCB) for the test. Muller LXH 100 light source and a monochromator were used to select single wavelength λ illumination with bandwidth of ~10 nm and light power density on the level of $10^{-5}$ W/cm$^2$. For the electrical measurements, we used semiconductor parameter analyzer (Agilent, HP4156) and low leakage switch mainframe (Agilent, E5250A) to obtain the current-voltage curves at room temperature (RT).

### A. Fully-Depleted (FD) Condition by Back-Gate Voltage

Fig. 2 presents the measured photocurrents, normalized for one finger of each suspended photodiode (M5, M10, M20 with $L_i$ = 5, 10, 20 µm), as a function of the applied back-gate voltage ($V_G$), under 590 nm incident light and different reverse anode bias ($V_D$). The variation of $V_G$ modifies the operation mode of the active silicon film back interface, from accumulation to depletion and inversion for negative to positive bias, leading to FD condition in the I-region. It is clearly seen that, to the first order, the photocurrents are modulated by the vertical depletion width $W_D$, i.e. roughly with the square root of positive $V_G$ above flat band voltage $V_{FB}$ [15] (i.e. in this case, $W_D \propto \sqrt{V_G - V_D - V_{FB}}$), and achieve a maximum under FD condition whose value is directly proportional to $L_i$ as is expected from carrier collection over the full I-region volume.

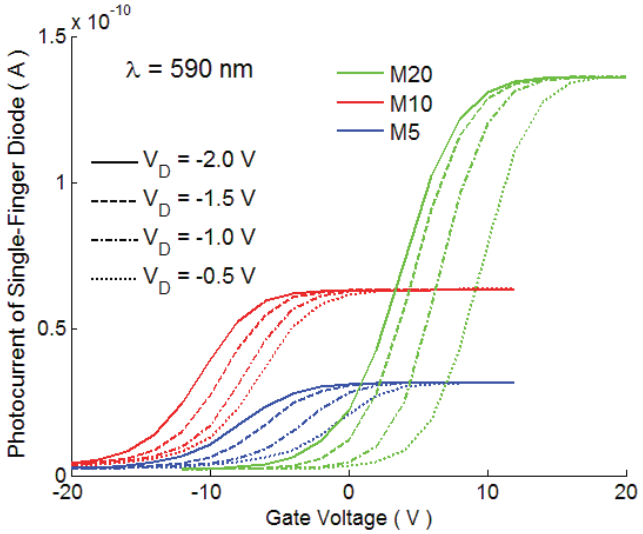



Fig. 2. Normalized photocurrent for single-finger diode as a function of applied back-gate voltage with 590 nm illumination (at 8.92×10$^{-5}$ W/cm$^2$), under different reverse anode bias $V_D$.

### B. Non-Fully-Depleted (NFD) Regime

The diode photocurrents also vary with reverse anode bias ($V_D$), but only in the non-fully-depleted (NFD) intermediate regime. In this case, Fig. 3 shows that at constant $V_G - V_D$ (to avoid modulating the vertical depletion width from back interface with $V_D$), the photocurrent indeed increases with the lateral depletion width $L_{zd}$ (as indicated by black dashed curve in Fig. 3) at the $P^-N^+$ blocked junction, which is roughly following the square root of $V_0 - V_D$ (i.e. $L_{zd} \propto \sqrt{V_0 - V_D}$) where $V_0$ is the built-in contact potential [3]. This cannot occur anymore once FD condition is achieved by increasing $V_G$ (Fig. 2) or when very negative $V_G$ (e.g. M20 at -12.0 V, M10 and M5 at -20.0 V in Fig. 2) impedes carriers collecton. Similar behaviors, i.e. current-voltage characteristics with back-gate and reverse anode voltages, were observed at all wavelengths in the visible spectrum.

### C. Responsivity at Room Temperature (RT)

Under FD condition, responsivities $R$ (i.e. $R = I_{ph}/P_{in}$ where $I_{ph}$ is the device photocurrent flowing through the I-region and $P_{in}$ is the optical power incident to the total device area) of M20 at RT for 3 different wavelengths (490, 590 and 760 nm) are 0.07, 0.1, 0.05 A/W respectively. Compared to the photodiodes lying on substrate [9] and the suspended photodiodes without Al, more than 2~3× responsivity has been achieved in the suspended photodiode with back Al, due to the

efficient collection of photo-generated carriers under the FD condition and the improvement of light absorption from the backside Al layer. Moreover $R$ increases with $L_i$ (0.061, 0.079, 0.1 A/W at 590 nm for device M5, M10, M20, respectively), due to the increasing percentage of photo-sensitive area (defined by $L_i$) over the total device area (including $P^+$ and $N^+$ contact regions).

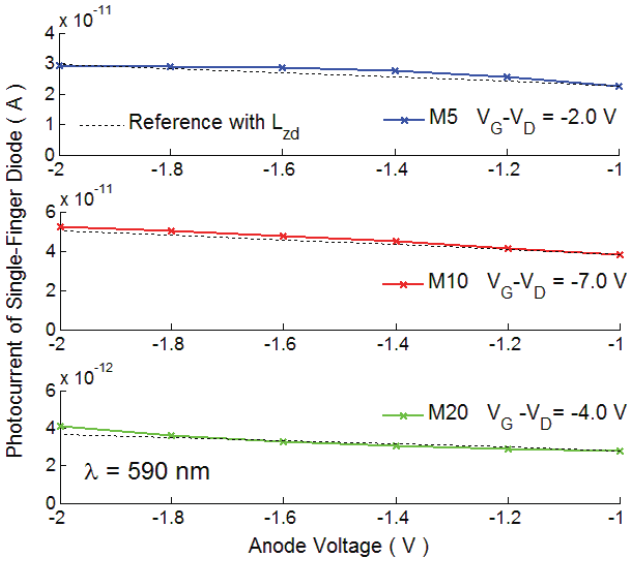



Fig. 3. Photocurrent for single-finger diode as a function of reverse anode voltage, under non-fully-depleted operation at proper back-gate bias $V_G$.

## IV. Numerical Analysis

To get further insight in the investigation and analysis of the experimental device performances, full two-dimensional (2-D) numerical simulations were conducted in Atlas software [16] from SILVACO Int., on a 2-D physical device model with $L_i$ = 10 µm. A schematic view of device under study is depicted in Fig. 4, showing notably 300 nm-thick polysilicon layer and 250 nm-thick silicon film. The intrinsic ($P^-$), $P^+$ and $N^+$ doping levels are about $5\times10^{15}$, $1\times10^{20}$, $1\times10^{20}$ $cm^{-3}$, respectively. Ohmic contacts are implemented onto the anode and cathode electrodes, while Schottky contact is specified for the back gate electrode with Al workfunction of 4.10 eV. No fixed oxide charge, nor interface charge density, is specified at this stage.

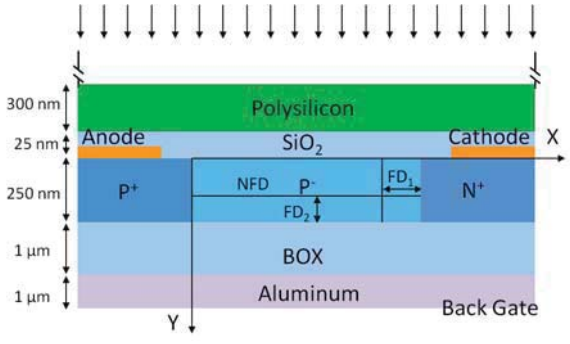
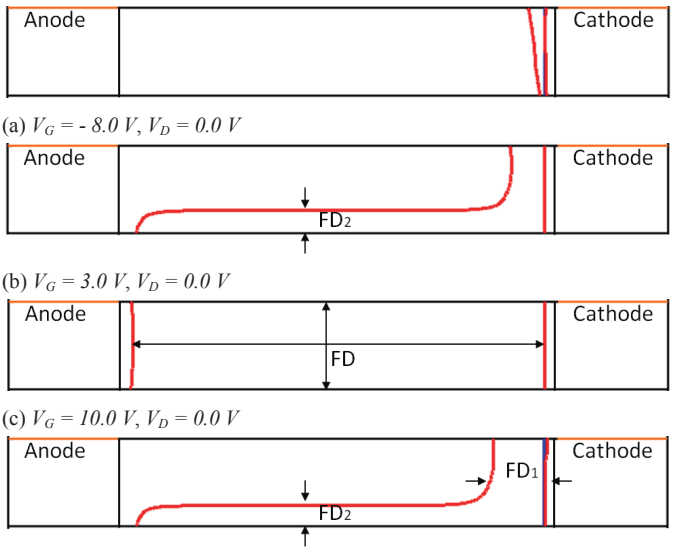



Fig. 4. Schematic view of lateral SOI PIN diode under study: $FD_1$ = region depleted by reverse anode bias, $FD_2$ = region depleted by back-gate voltage, NFD = undepleted part.

### A. Depletion Regime

Depending on the back gate $V_G$ and anode $V_D$ biases, the I-region features an undepleted zone (NFD) and two main depletion zones, one arising from $P^-N^+$ junction ($FD_1$), one from BOX interface ($FD_2$) (Fig. 4).

Fig. 5 presents the simulated depletion conditions in the I-region at temperature of 300 K, where the red curve represents the depletion region edge. Negative $V_G$ (-8.0 $V$) suppresses the depletion region $FD_2$ in (a); increasing $V_G$ to positive (3.0 $V$), $FD_2$ develops in (b) and full depletion in (c) is achieved under sufficiently positive $V_G$ (10.0 $V$), which confirms the first-order interpretation of our measurements in Fig. 2. However the depletion region is affected by positive $V_G$ and reverse $V_D$, from cases (a) and (b) we observe that $V_G$ also influences $FD_1$ extension, while from (b) and (d) with the same $V_G - V_D$, reverse $V_D$ modulates $FD_2$.




(d) $V_G$ = *1.0 V*, $V_D$ = *-2.0 V*, with the same $V_G - V_D$ as (b)

Fig. 5. Depletion region edges (red curves) modulated by back-gate $V_G$ and anode $V_D$ biases.

### B. Light Absorption

Setting optical index and thickness of all the materials and layers into the device model as obtained from ellipsometry measurements [17] [18], light absorption in the active silicon film of the lateral SOI PIN photodiode was simulated within the 450-900 nm range. Fig. 6 shows the detailed results of absorption averaged over a bandwidth of 10 nm, for the suspended diode with 1 µm-thick backside Al layer (blue curve), for the diode lying on substrate (green) and for the suspended photodiode without Al (brown). Light absorption below 480 nm is impaired due to high absorption in the 300 nm-thick polysilicon layer that is used here to protect the I-region of the PIN photodiode from implantation in SOI CMOS technology. In comparison with the two other diodes (i.e. with light reflected from the silicon substrate or air), light absorption in the suspended diode with Al appears obviously boosted at specific wavelength ranges, e.g. around 500, 600 and 770 nm, due to the excellent reflectance from the back Al reflector. A strong responsivity increase (over 2~3×

improvement) has been observed and validated in our measurements at 490, 590, and 760 nm.

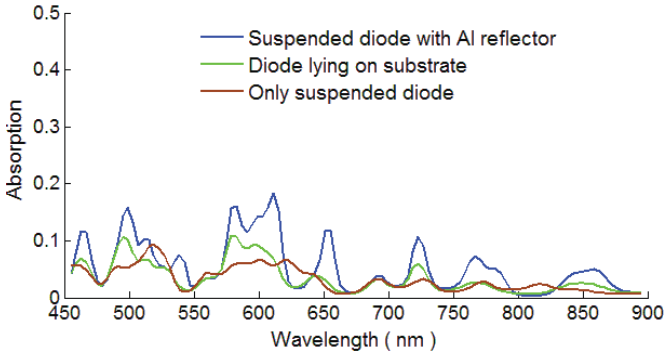



Fig. 6. Light absorption averaged on a bandwidth of 10 nm for the suspended diode with backside Al (blue curve), the diode lying on substrate (green curve) and the suspended diode without Al (brown curve) with $L_i$ = 10 µm.

## V. CONCLUSIONS

With 1 µm-thick Al deposited on the backside of suspended SOI PIN photodiodes, electrical and optical performances of the photodiode have been improved and optimized. Photodiode output photocurrents indeed reach a maximum under the FD condition achieved by the positive voltage applied to the Al back gate. The device optical response appears significantly boosted for specific wavelength ranges (e.g. around 500, 600, 770 nm) due to the excellent reflectance of the backside Al layer. Under FD condition, more than 2~3× improvements of responsivity (up to 0.1 A/W at 590 nm) have been achieved experimentally at 490, 590, 760 nm wavelengths. Optoelectronic 2-D device simulations are performed to fully validate the device performances and improvement.

## ACKNOWLEDGMENT

We are grateful to André Crahay for the aluminum deposition process. And the UCL authors would like to acknowledge the FP7 EU SOIHITS project for funding the device fabrication.

## REFERENCES

[1] C.K. Ho, A. Robinson, D.R. Miller, M.J. Davis, "Overview of sensors and needs for environmental monitoring," Sensors, vol. 5, pp. 4-37, 2005.

[2] O. Bulteel, A. Afzalian, D. Flandre, "Fully integrated blue/UV SOI CMOS photosensor for biomedical and environmental applications," Analog Integrated Circuits and Signal Processing, vol. 65, no. 3, pp. 399-405, 2010.

[3] A. Afzalian, D. Flandre, "Physical modeling and design of thin-film SOI lateral PIN photodiodes," IEEE Trans. Electr. Dev., vol. 52, no. 6, pp. 1116-1122, 2005.

[4] S.M. Sze, K.K. Ng, Physics of Semiconductor Devices, 3rd ed., U.S.: Wiley Interscience, 2007, pp. 676-684.

[5] A. Ono, Y. Matsuo, H. Satoh, H. Inokawa, "Sensitivity improvement of silicon-on-insulator photodiode by gold nanoparticles with substrate bias control," Appl. Phy. Lett. vol. 99, no. 062105, 2011.

[6] Z.T. Han, J.K. Chu, F.T. Meng, R.C. Jin, "Design and simulation of blue/violet sensitive photodetectors in silicon-on-insulator," J. Semiconductors, vol. 30, no. 104008, pp. 1-4, 2009.

[7] V.S. Sinnis, M. Seto, G.W. Hooft, Y. Watabe, A.P. Morrison, W.Hoekstra, W.B. Boer, "Silicon-based resonant-cavity-enhanced photodiode with a buried $SiO_2$ reflector," Appl. Phy. Lett., vol. 74, no. 9, pp. 1203-1205, 1999.

[8] N. Andre, G.L. Li, P.Gérard, O. Poncelet, Y. Zeng, S.Z. Ali, F. Udrea, L.A. Francis, D. Flandre, "Wide Band Study of Silicon-on-Insulator Photodiodes on Suspended Micro-Hotplates Platforms," in IEEE Int. Conf. on IC Design & Technology (ICICDT), pp. 1-4, Belgium, June 2015.

[9] G.L. Li, N. Andre, O. Poncelet, P.Gérard, S.Z. Ali, F. Udrea, L.A. Francis, Y. Zeng, D. Flandre, "Silicon-on-Insulator Photodiode on Micro-Hotplate Platform with Improved Responsivity and High-Temperature Application," unpublished.

[10] C. Novo, R. Giacomini, A. Afzalian, D. Flandre, "Operation of lateral SOI PIN photodiodes with back-gate bias and intrinsic length variation," in 223rd ESC Transactions Meeting, Brazil, May 2013.

[11] Website: http://www.photonics.com/EDU/Handbook.aspx?AID=25501.

[12] F. Udrea, J.W. Gardner, D. Setiadi, J.A. Covington, T. Dogaru, C.C. Lu, W.I. Milne, "Design and simulations of SOI CMOS micro-hotplate gas sensors," Sens. Actuators B, Chem., vol. 78, pp. 180-190, 2001.

[13] N. André, G. Pollissard, N. Couniot, P.Gérard, S.Z. Ali, F. Udrea, L.A. Francis, D. Flandre, "A silicon-on-insulator platform functionalized by atomic layer deposition for humidity sensing," in Int. Meeting on New Sensing Technologies and Modelling for Air-Pollution Monitoring, Portugal, October 2014.

[14] P.K. Guhaa, S.Z. Ali, C.C.C. Lee, F. Udrea, W.I. Milnea, T. Iwakib, J.A. Covingtonb, J.W. Gardnerb, "Novel design and characterization of SOI CMOS micro-hotplates for high temperature gas sensors," Sens. Actuators B, Chem., vol. 127, pp. 260-266, 2007.

[15] S.M. Sze, K.K. Ng, Physics of Semiconductor Devices, 3rd ed., U.S.: Wiley Interscience, 2007, pp. 293-346.

[16] Atlas User's Manual: Device Simulation Software, Silvaco Inc., U.S.: Santa Clara, November 2014.

[17] N. Ren, Z. Liu, Q. Wang, "Investigating the effects of microstructure on optical properties of different kinds of polysilicon thin films," Phy. Lett. A, vol. 379, pp.1153-1160, 2015.

[18] A. Gorin, A. Jaouad, E. Grondin, V. Aimez, P. Charette, "Fabrication of silicon nitride waveguides for visible-light using PECVD: a study of the effect of plasma frequency on optical properties," Optics Express, vol. 16, no. 18, pp. 13509-13516, 2008.

# *RF SOI CMOS Technology on 1st and 2nd Generation Trap-Rich High Resistivity SOI Wafers*

B. Kazemi Esfeh[1], V. Kilchytska[1], D. Flandre[1], J.-P. Raskin[1]
[1]ICTEAM, Université catholique de Louvain, 1348
Louvain-la-Neuve, Belgium
*Email: Babak.kazemiesfeh@uclouvain.be, Tel: (+32) 10478386*

***Abstract*—In this work 3 different types of UNIBOND™ Silicon-on-Insulator (SOI) wafers including one standard and two types of trap-rich high resistivity HR-SOI substrates provided by SOITEC are studied. The DC and RF performances of these wafers are compared by means of passive and active devices, coplanar waveguide (CPW) lines and partially-depleted (PD) SOI MOSFETs, respectively.**

***Keywords—High resistivity silicon; trap-rich high resisitivity silicon; substrate effective resistivity; Silicon-on-Insulator; DC and RF performance; Partially-depleted (PD) SOI MOSFETs.***

## I. INTRODUCTION

During last decades, CMOS technology scaling-down has enabled millimeter wavelength operation and low-cost integration of digital, analog and RF systems on the same wafer for system-on-chip or in system-in-package applications [1-3]. In this context, the most special advantage of SOI CMOS compared to bulk Si is the availability of high-resistivity silicon (HR-Si) substrate to achieve low crosstalk between passive and active devices and high-quality passive elements thanks to effective reduction of substrate coupling and losses in RF circuits [4-5]. Moreover, SOI technology has simpler fabrication process than bulk and hence is more cost-effective. However, HR-SOI substrate suffers from resistivity degradation due to the formation of parasitic surface conduction (PSC) beneath the buried oxide layer (BOX) [6-9] due to fixed oxide charges ($Q_{ox}$) within the oxide. One of the most efficient techniques to overcome this problem is to introduce a trap-rich layer at the $Si/SiO_2$ interface compatible with industrial SOI wafer production and thermal budget of standard CMOS process [8] which captures the free carriers forming the PSC and thus makes the substrate retrieving its nominal high resistivity. Since thermal resistance is proportional to the square root of the BOX thickness, BOX thinning is desired to improve thermal properties. Moreover, threshold voltage control by means of back-gate biasing voltage $V_{bg}$ could be a useful feature provided by thin BOX in fully depleted devices [10]. Therefore, trap-rich HR-SOI with thinner BOX could be considered as a promising candidate.

## II. DEVICES DESCRIPTION

In this work two types of trap-rich HR-SOI substrates denoted eSi1 and eSi2 as 1st and 2nd generations with 400nm and 200nm-thick BOX respectively and one standard HR-SOI with 1 µm BOX (all provided by SOITEC) are characterized and compared for non-linearity effects and DC/RF MOSFET behaviors. The test structure devices include 0.52 µm-thick CPW lines and PD SOI nMOSFETs fabricated using TowerJazz 0.18µm SOI CMOS process. The dimensions of the CPW lines are respectively 20, 18 and 100 µm for the central conductor, slot space and ground plane. The PD SOI MOSFETs have 145 nm of thin active silicon film of 10 Ω-cm resistivity and 5 nm of gate oxide thickness. The studied RF body-tied MOSFET has a 0.24 µm gate length ($L_g$) with 16 gate fingers of 2 µm each ($W_f$). The studied single finger DC MOSFET has a 0.26 µm of gate length ($L_g$) with 1.5 µm width ($W_f$).

## III. MEASUREMENT RESULTS

### *A. PD SOI RF and DC MOSFETs*

The DC/RF on-wafer measurements have been done using an Agilent N5242A for high-frequency measurement from 10 MHz to 26.5 GHz and Agilent B1500 for DC measurements. As shown in Fig. 1, the $I_D$-$V_G$ and $g_m$-$V_G$ curves in linear regime for DC transistor on the 3 different wafers are very close. To eliminate the threshold voltage variations effect and fairly compare these results, $g_m/I_D$ ratio versus $I_D/(W/L)$ curves for the same transistors are plotted in Fig. 2. Similar DC characteristics are obtained for all substrate types. Fig. 3 shows a good similarity of current cut-off frequency $f_T$ as one of the main RF figures of merit as expected on all 3 wafers.

### *B. Substrate Effective Resistivity and Harmonic Distortion*

By means of a 2100 µm-long CPW line S-parameters measurement, the effective resistivity ($\rho_{eff}$) and total loss ($\alpha$) on the 3 different types of substrate, plus quartz, considered as the best reference, have been extracted. Fig. 4 shows that as stated before, due to the formation of PSC, the standard HR SOI substrate loses

its nominal high resistivity and shows an effective resistivity of only 200 Ω.cm, whereas in 1st and 2nd generations of trap-rich HR-SOI, the substrate has kept its high resistivity of more than 2 kΩ.cm and 3 kΩ.cm respectively, after CMOS processing. The interesting point that can be seen in this figure is that despite its thinner BOX, the eSi2 substrate shows higher $\rho_{eff}$ and lower α compared to eSi1 which could be explained by the better process and quality of the trap-rich layer in 2nd generation. Fig. 5 illustrates the 2nd and 3rd harmonics of a 900 MHz signal at the output of the CPW line on all different wafers. Compared to HR-SOI wafer, a reduction of 24 and 35 dB is measured on both generations of trap-rich HR-SOI for respectively, 2nd and 3rd harmonics. From Fig. 4 and 5 it can be clearly seen that the level of the harmonics are reversely proportional with the substrate resistivity. Fig. 6 demonstrates the RF performance insensitivity of trap-rich HR-SOI substrates to the applied bias voltages. It can be seen that under different bias conditions, the maximum variation of 2nd harmonics in HR-SOI wafer is 3 times higher compared to second generation trap-rich substrate.

## IV. CONCLUSION

In HR SOI wafers by applying a trap-rich layer underneath the BOX, the substrate recovers its high-resistivity properties resulting in higher effective resistivity, lower losses, lower crosstalk and higher linearity (which was demonstrated by lower harmonics level), all conserved after CMOS processing. It was shown that the presence of a trap-rich layer does not change the DC and RF characteristics of the MOSFET transistors. Moreover, by applying enhanced 2nd generation trap-rich HR SOI substrate having thinner BOX of 200 nm, improved thermal properties could be achievable. Therefore, this technology can be considered as a good candidate for SoC applications.

## ACKNOWLEDGMENT

The authors acknowledge SOITEC for providing the wafers and TowerJazz for the fabrication of CPW lines and PD SOI CMOS devices.

## REFERENCES

[1] K. Ben Ali, C. Roda Neve, A. Gharsallah, J.-P. Raskin, "RF SOI CMOS technology on commercial trap-rich high resistivity SOI wafer," Proc. of IEEE International SOI Conference, pp. 112-113, 2012.

[2] K. Ben Ali, C. Roda Neve, A. Gharsallah, J.-P. Raskin, "Impact of crosstalk into high resistivity silicon substrate on the RF performance of SOI MOSFET," Journal of Telecommunications and Information Technology vol. 4, pp. 93-100, 2010.

[3] J. -P. Raskin, "Silicon-on-insulator MOSFETs models in analog/RF domain," International Journal of Numerical Modelling Electronic Networks Devices and Fields vol. 27, 2014.

[4] B. Vanada, "Study of Floating Body Effect in SOI Technology," International Journal of Modern Engineering Research., vol. 3, pp. 1817-1824, 2013.

[5] J. –P. Raskin, A. Viviani, D. Flandre, J. Colinge, "Substrate crosstalk reduction using SOI technology", IEEE Transactions on Electron Devices, vol. 44, no. 12, pp. 2252-2261, 1997.

[6] K. Ben Ali, C. Roda. Neve, A. Gharsallah, J. -P. Raskin, "RF Performance of SOI CMOS Technology on Commercial 200-mm Enhanced Signal Integrity High Resistivity SOI Substrate," IEEE Transaction on Electron Devices, vol. 61, no. 3, pp. 722 - 728 2014.

[7] D. Lederer, J. -P. Raskin, "New substrate passivation method dedicated to high resistivity SOI wafer fabrication with increase substrate resistivity," IEEE Electron Device Lett., vol. 26, pp. 805-807, 2005.

[8] D. Lederer, J. -P. Raskin, "RF Performance of a Commercial SOI Technology Transferred Onto a Passivated HR Silicon Substrate," IEEE Transaction on Electron Devices, vol. 55, no. 7, pp. 1664 - 1671, 2008.

[9] C. R. Neve, J. -P. Raskin, "RF Harmonic Distortion of CPW Lines on HR-Si and Trap-Rich HR-Si Substrates," IEEE Transaction on Electron Devices, vol. 59, no. 4, pp. 924 - 932, 2012.

[10] S. Makovejev, J.-P. Raskin, M.K. Md Arshad, D. Flandre, S. Olsen, F. Andrieu, V. Kilchytska, "Impact of self-heating and substrate effects on small-signal output conductance in UTBB SOI MOSFETs", Solid State Electronics, vol. 71, pp. 93-100, 2012.

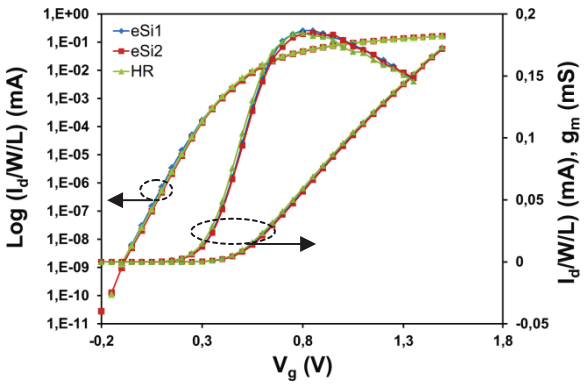



Fig. 1. Normalized $I_d$-$V_g$ (linear and logarithmic) and $g_m$-$V_g$ characteristics in linear regime ($V_{DS}$ = 50mV) of DC transistor for 3 different wafers of 1st generation of trap-rich high resistivity SOI (eSi1), 2nd generation of trap-rich high resistivity SOI (eSi2) and high resistivity SOI (HR).

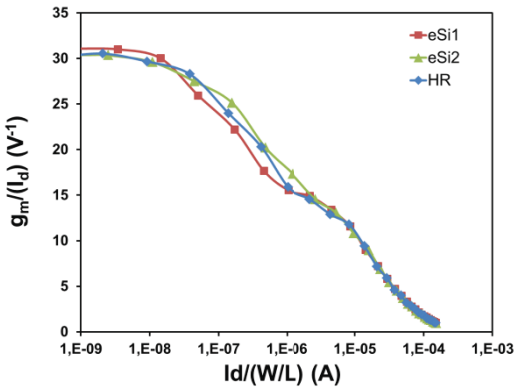



Fig. 2. $g_m$ / $I_d$ ratio versus $I_d$ /(W/L) DC transistor on 3 different wafers of 1st generation of trap-rich high resistivity SOI (eSi1), 2nd generation of trap-rich high resistivity SOI (eSi2) and high resistivity SOI (HR).

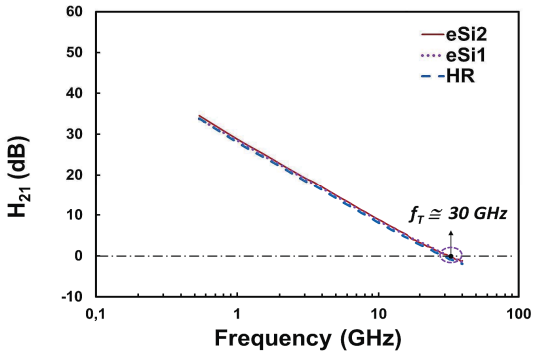



Fig. 3. Current gain cutoff frequency $f_T$ at $V_{DS}$ = 1.2 V and $V_{GS}$ at which $g_m$ (transconductance) is maximum for body-tied RF transistor for 3 different wafers of 1st generation of trap-rich high resistivity SOI (eSi1), 2nd generation of trap-rich high resistivity SOI (eSi2) and high resistivity SOI (HR).

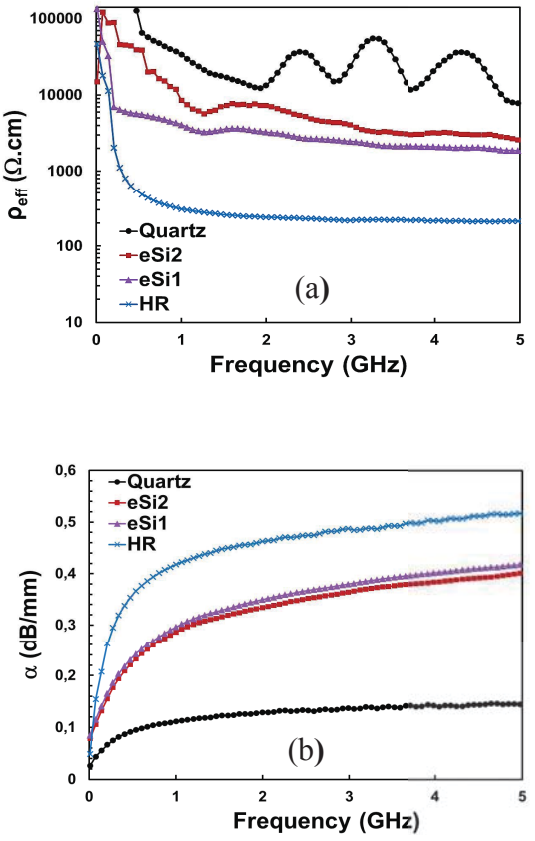



Fig. 4. (a) Effective resistivity (b) Total Loss (Conductor and substrate) of 3 different substrates of 1st generation of trap-rich high resistivity SOI (eSi1), 2nd generation of trap-rich high resistivity SOI (eSi2) and high resistivity SOI (HR). Quartz has been considered as a reference.

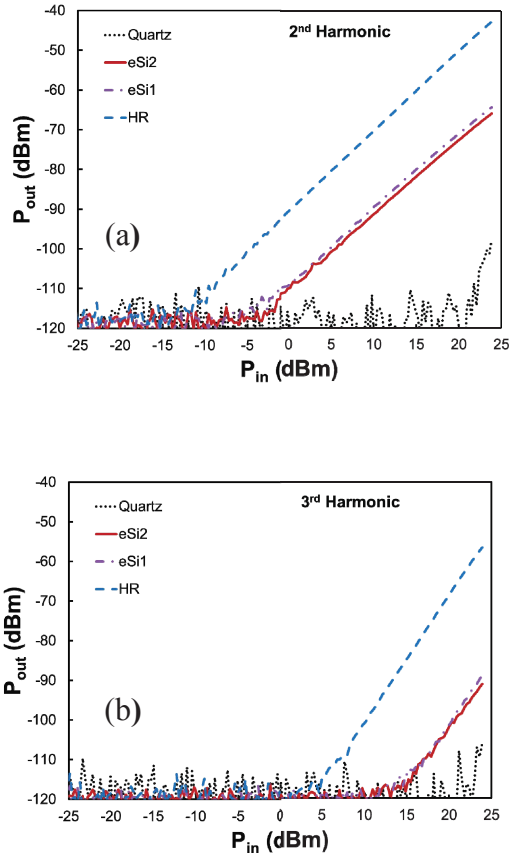



Fig. 5. (a) 2nd and (b) 3rd harmonics distortion measured by CPW lines on 3 different wafers of 1st generation of trap-rich high resistivity SOI (eSi1), 2nd generation of trap-rich high resistivity SOI (eSi2) and high resistivity SOI (HR). Quartz has been considered as a reference.

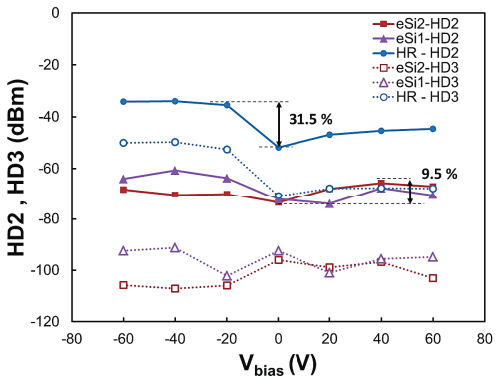



Fig. 6. The variation of 2nd harmonic distortion (HD2) and 3rd harmonic distortion (HD3) with bias changing from -60V to +60 V at input power $P_{in}$ = 20 dBm for 3 different wafers of 1st generation of trap-rich high resistivity SOI (eSi1), 2nd generation of trap-rich high resistivity SOI (eSi2) and high resistivity SOI (HR).

# *Effective Hole Mobility and Low-Frequency Noise Characterization of Ge pFinFETs*

A.V. Oliveira[#], P. G. D. Agopian, J. A. Martino
LSI/PSI/EPUSP,
University of Sao Paulo
Sao Paulo, Brazil
avo.eng@gmail.com

E. Simoen, J. Mitard, L. Witters, R. Langer, N. Collaert, C. Claeys[&] and A. Thean
[#]also Imec, Leuven, Belgium
[&]also E. E., ESAT, KU Leuven, Belgium

***Abstract*— Germanium pFinFETs are evaluated from the viewpoint of effective hole mobility and low frequency noise performance. These parameters are measured for different fin widths and backside substrate bias in order to get a better insight in the underlying scattering mechanisms. For narrow devices, it was found that the peak effective mobility and the Coulomb scattering coefficient are limited due to the charges in the gate oxide sidewalls or interface layer, resulting in similar effective mobility values for narrow and planar-like devices. On the other hand, the substrate biasing played a role only in planar-like devices, which moves the effective mobility and Coulomb scattering coefficient values toward the opposite direction.**

***Keywords—Ge pFinFET; effective mobility; low-frequency noise; fin width; substrate biasing***

## I. INTRODUCTION

Many research efforts have been spent recently for alternative high-mobility materials for the channel region, regarding especially future high-performance applications, i.e., germanium (Ge) and III/V instead of silicon [1]. Ge is particularly relevant for p-channel devices thanks to the 4 times higher bulk hole mobility than Si [2]. On the other hand, there are some challenging issues that must be overcome to optimize the Ge transistor performance [2]. Apart from that, considering the fact that the main semiconductor industries have been investing in multiple gate devices, such as e.g. FinFET triple-gate (3D-transistors) [3] [4], thanks to their electrostatic improvements and short-channel effect control [5], it is very relevant evaluating the combination of a future candidate channel material with the current mainstream device architecture.

Therefore, this work analyses the effective hole mobility and low frequency noise behavior for different fin widths of inversion-mode Ge pFinFETs, which are schematically represented in Fig 1.

## II. EXPERIMENTAL DETAILS

The main fabrication steps are summarized in Fig. 2. The p-type strained germanium FinFET devices used in this work have been fabricated at imec/Belgium on 300 mm Si (100) wafers via the Shallow Trench Isolation (STI) first process. The main FinFET device dimensions are fin widths ($W_{fin}$) of 20 nm; 30 nm; 50 nm and 100 nm, a geometric channel length ($L_G$) of 1.03 µm and a fin height ($H_{fin}$) of 20 nm. The channel and n-type in situ doped relaxed buffer ($Si_{1-x}Ge_x$ x=75 %) have a doping concentration of around $1\times10^{17}$ $cm^{-3}$ and $5\times10^{18}$ $cm^{-3}$, respectively. The gate stack is composed by 0.7 nm $SiO_2$, 2.5 nm $HfO_2$ and 5 nm TiN. The work is based only on experimental data, which were obtained from measurements with an HP 4146C - Semiconductor Device Parameter Analyzer, Agilent E4980 A – High frequency CV and the hardware/software systems from ProPlusSolution for IV, CV and low frequency noise measurements, respectively. The peak effective mobility and Capacitance Equivalent Thickness (CET) were extracted by the split CV technique [6], while the threshold voltage is derived at [7]. The input-referred voltage noise spectral density was determined from the ratio drain current noise spectral density over square of the transconductance, i.e., $S_{VG} = S_{ID}/gm^2$.

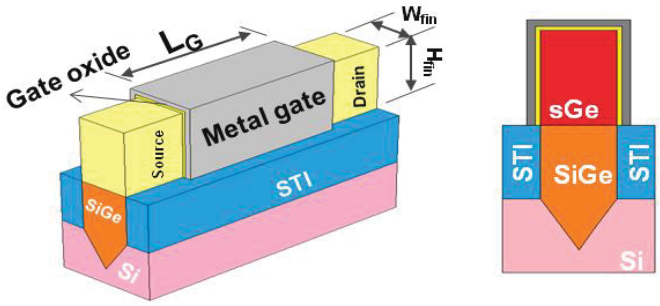



Fig. 1: Germanium FinFET structure (A) and cross section in the middle of the fin (B).

- Si recess in STI
- SiGe75% epitaxial growth + Phosphorus in-situ doping+anneal
- Strained Ge epitaxial growth
- Dummy gate definition
- S/D SiGe 75% epitaxial growth
- Boron implantation +anneal
- Spacer formation
- ILD0 (field oxide) formation + CMP
- Dummy gate removal and Si passivated/high-k/MG/W fill + CMP

Fig. 2: Process flow description of the Ge pMOSFET studied in this work.

## III. Results and Discussion

Fig. 3 presents the threshold voltage as a function of fin width. It clearly reveals a $W_{fin}$ dependency of the threshold voltage ($V_T$). First of all, it is a consequence of a higher leakage current underneath the channel from source to drain regions for the narrow devices. Moreover, it is associated with a negative charge in either the gate oxide or interface layer, since the $V_T$ is shifted towards more positive values [8]. In addition, the $V_T$ behavior is quite consistent with the frequency normalized noise Power Spectral Density (PSD), showing Lorentzian components with a $V_{GS}$-dependent corner frequency. This originates from $V_{GS}$ dependent generation-recombination (GR) noise, which indicates the presence of traps in the gate dielectric, owing to a strong relation between the $V_{GS}$ and the SRH lifetime [9].

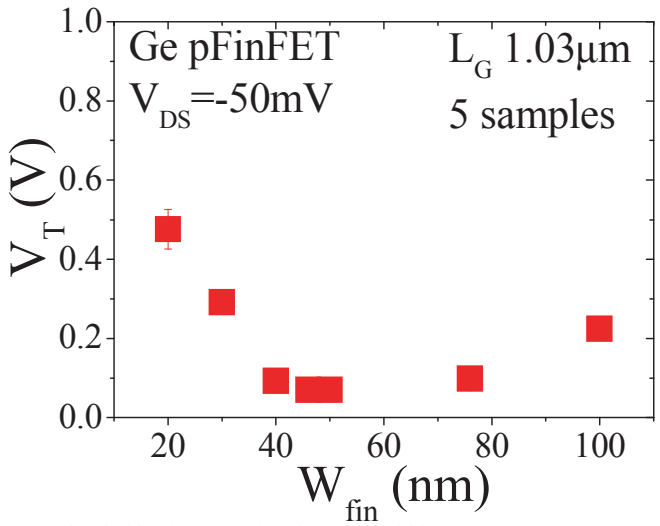



Fig. 3: Threshold voltage as a function of fin width.

Fig. 4 shows the Capacitance Equivalent Thickness (CET) as a function of fin width for longer channel length device ($L_G$=1µm).

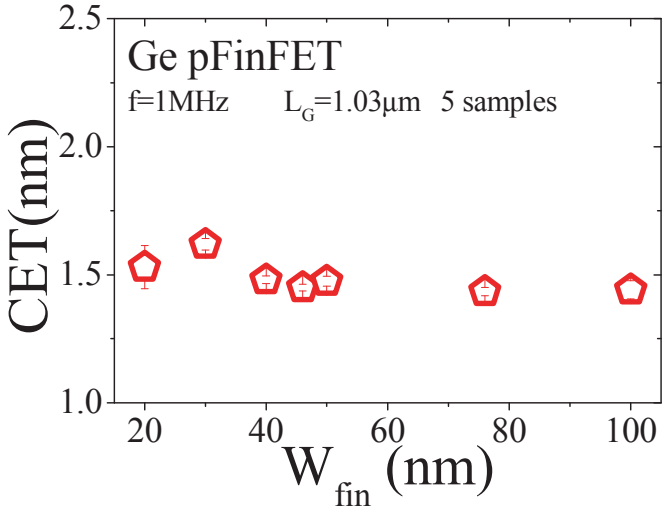



Fig. 4. Capacitance equivalent thickness as a function of fin width.

The CET has a mean value around 1.5 nm for the studied fin width range, taking into account five samples for each width. It points to a relatively good uniformity of the gate stack dielectric for the process under evaluation.

Fig. 5 presents the peak effective hole mobility as a function of fin width. It noticeably shows that the average effective hole mobility ($\mu_{eff}$) is quite $W_{fin}$ independent. On the other hand, the $\mu_{eff}$ should be higher for small $W_{fin}$ compared with planar-like pMOSFETs, since the low-field hole mobility of the FinFET <110> sidewalls is superior over the value for the top <100> plane [10]. The fact that there is no $W_{fin}$ dependence of $\mu_{eff}$ is related to a higher oxide trap density in the sidewalls, which limits the $\mu_{eff}$ for narrow devices.

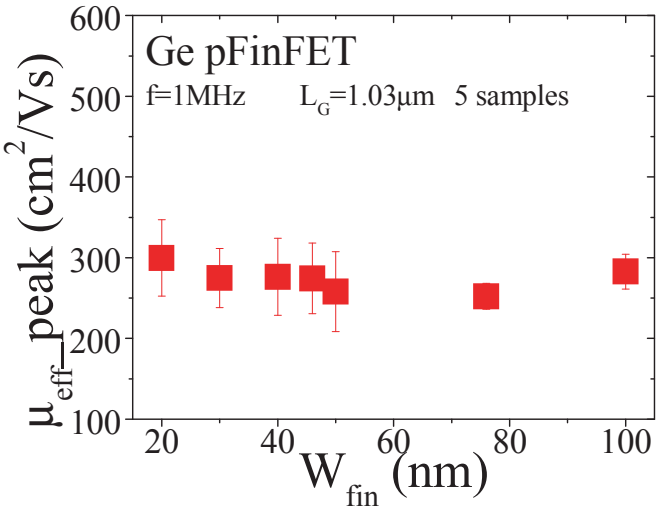



Fig. 5: Peak of effective mobility as a function of fin width.

Fig. 6 shows the peak effective hole mobility as a function of temperature. It is possible to observe that the $\mu_{eff}$ presents only a slight temperature dependence, which indicates that the surface roughness scattering might be dominant, since it is known that the dominant mobility scattering mechanism plays a role in the $\mu_{eff}$ value.

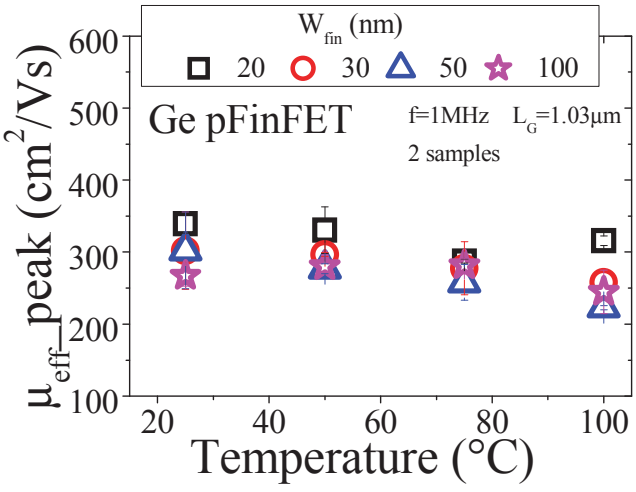



Fig. 6. Peak of effective hole mobility as a function of temperature for different $W_{fin}$.

The drain current noise power spectral density ($S_{ID}$) as a function of the frequency presented in Fig. 7 for different fin widths and it tells that the flicker noise ($1/f^{\gamma}$) is dominant in the frequency range evaluated. Furthermore, the $\gamma$ factor is around one for all $W_{fin}$. The observed $1/f^{\gamma}$ can be modeled in terms of the carrier number and correlated mobility fluctuations [11]. From the input-referred voltage noise ($S_{VG}$) one can extract the Coulomb scattering coefficient ($\alpha_{SC}$) and the slow oxide trap density ($N_t$), at flat-band voltage region [12] as presented in (1). Where gm is the transconductance, $\mu$ is the effective mobility and $C_{EOT}$ is the capacitance density. On top of that, the narrowest device ($W_{fin}$ = 20 nm) presents Generation-Recombination (GR) noise component, which is not studied in this work.

$$S_{VG} = S_{VGfb}(1+\alpha_{SC}\,\mu\,C_{EOT}\,\frac{I_{DS}}{gm})^2 \qquad (1)$$

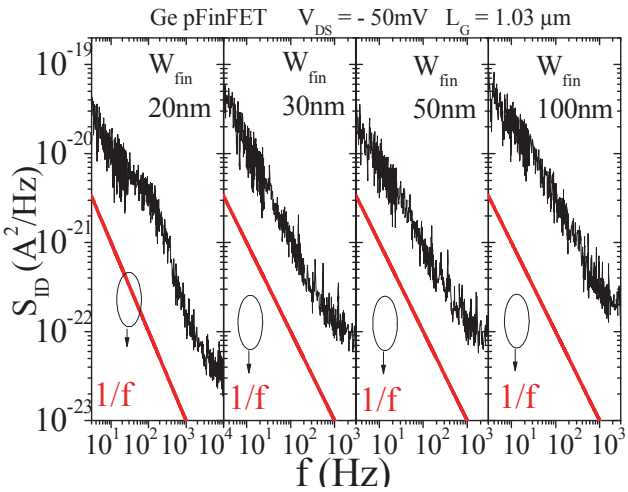



Fig. 7. Power spectral density as a function of frequency for different $W_{fin}$.

Fig. 8 presents the effective mobility ($\mu_{eff}$) and the Coulomb scattering coefficient ($\alpha_{SC}$) as a function of the substrate bias ($V_{BS}$).

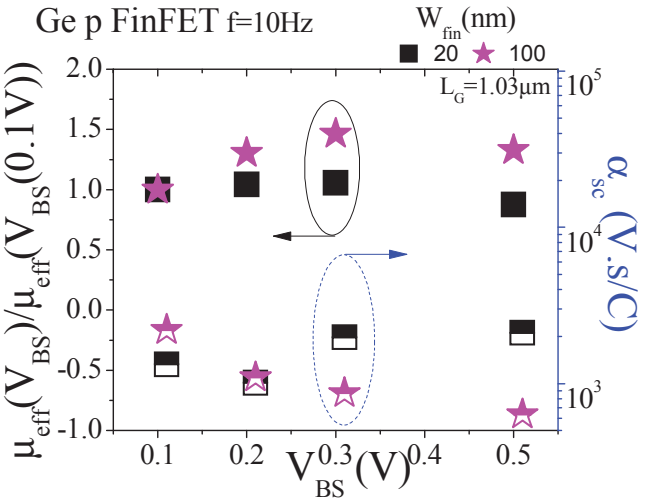



Fig. 8. Normalized effective mobility and scattering coefficient as a function of substrate bias.

As the backside $V_{BS}$ increases, the $\alpha_{SC}$ of the planar-like device ($W_{fin}$ = 100 nm) decreases, demonstrating that $\alpha_{SC}$ is less efficient, since the distance between the interface with the gate stack and the inversion layer charge centroid becomes larger, resulting in the increase of $\mu_{eff}$, as in planar Ge MOSFETs [13]. On the other hand, there is no significant impact of $V_{BS}$ on $\mu_{eff}$ and $\alpha_{SC}$ for narrow devices, due to the strong electrostatic coupling, which is confirmed in Fig. 9, where the $V_T$ for narrow devices is $V_{BS}$-independent for the studied channel length range.

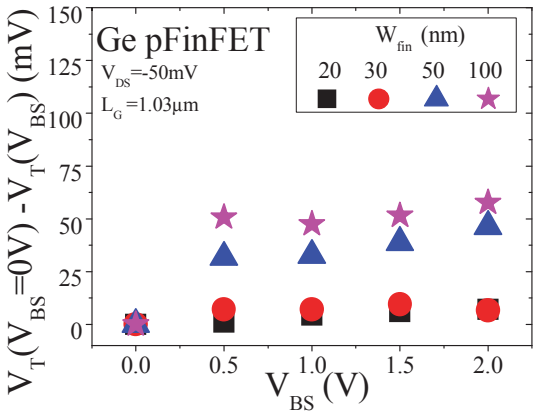



Fig. 9. Threshold voltage shift as a function of substrate voltage.

The oxide trap density ($N_t$) is proportional to the input-referred voltage noise at flat-band voltage region ($S_{VGfb}$). The latter can be calculated as in (2). Where $k_BT$ is the thermal energy, $W_{eff}$ is the is the effective width, $L_G$ is the geometric channel length, f is the frequency and $\alpha_t$ is the attenuation tunneling parameter noise.

$$S_{VGfb} = \frac{q^2 k_B T N_t}{W_{eff} L_G \alpha_t C_{EOT}^2 f} \qquad (2)$$

Fig. 10 presents the normalized input-referred voltage noise spectral density in the flat-band voltage region as a function of threshold voltage. It is noticeable that there is a correlation between the $N_t$ and the $V_T$.

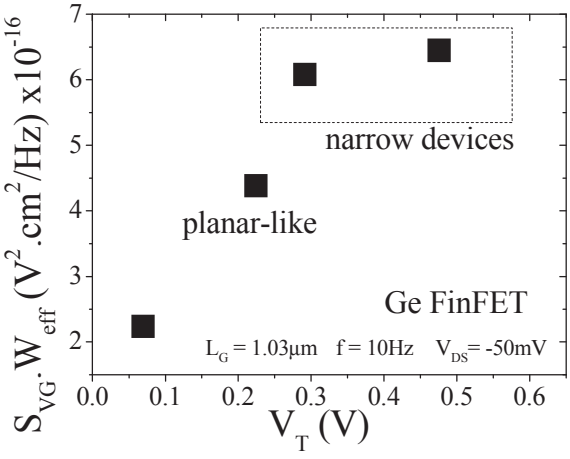



Fig. 10. Normalized input-referred voltage noise spectral density as a function of threshold voltage.

Moreover, the narrower the device, the higher is the oxide trap density, resulting in a hole mobility degradation, which is consistent with the results presented in Fig. 5 (the narrow devices), when higher $\mu_{eff}$ values were expected due to the FinFET <110> sidewalls predominance.

## IV. Conclusions

Ge pFinFETs with a 1.5 nn-CET using a conventional STI-first scheme have been characterized and reported in this work. Instead that the effective mobility follows the expected behavior, i.e., higher for narrow devices than for planar-like ones due to the higher $\mu_{eff}$ of the <110> sidewalls, this work revealed that the $\mu_{eff}$ was limited due to the predominance of charges in the gate oxide sidewalls or interface layer, which also degraded the threshold voltage for narrow devices. Considering the low-frequency-noise behavior, it is shown that a $1/f^{\gamma}$ behavior ($\gamma$~1) is observed for all fin widths. Moreover, the Coulomb scattering coefficient ($\alpha_{SC}$) showed to be dependent on the substrate bias ($V_{BS}$) only for the planar-like devices, resulting in a $\mu_{eff}$ increase and $\alpha_{SC}$ reduction, as a consequence of a larger distance between the interface with the gate stack and the inversion layer charge. The oxide trap density ($N_t$) presented a correlation with the threshold voltage, which reinforces the effective hole mobility limitation for narrow devices by the $N_t$.

## Acknowledgment

The authors would like to thank CAPES, CNPq, FAPESP, FWO and the Logic IIAP program for the support. This work has been performed in the frame of the imec Core Partner program on Ge devices.

## References

[1] S. Takagi et al., "High mobility CMOS technologies using III–V/Ge channels on Si platform," Solid-State Electron., vol. 88, pp. 2-8, October 2013.

[2] E. Simoen et al., "Challenges and opportunities in advanced Ge pMOSFETs," Mater. Sci. Semiconduc. Proc., vol. 15, pp. 588–600, December 2012.

[3] S. Natarajan et al., "A 14nm logic technology featuring 2nd-generation FinFET , air-gapped interconnects, self-aligned double patterning and a 0.0588 $m^2$ SRAM cell size," Proc. Intern. Electron Devices Meeting, USA, p. 3.7.1, 2014.

[4] T. Hook, "SOI FinFET versus bulk FinFET for 10nm and below," Proc. SOI 3D Subthreshold Microelectron. Tech. Unified Conf., USA, p.1, 2014.

[5] T. Chiarella et al., "Benchmarking SOI and bulk FinFET alternatives for planar CMOS scaling succession," Solid-State Electron., vol. 54, no. 9, pp. 855–860, May 2010.

[6] Q. Hubert et al., "All regimes mobility extraction using split *C–V* technique enhanced with charge-sheet model," Solid-State Electron., vol. 111, pp. 52-57, September 2015.

[7] G. Ghibaudo, "New method for extraction of MOSFET parameters", Electon. Lett., vol. 24, no. 9, pp. 543-545, April 1988.

[8] K. Yamamoto et al., "Dramatic enhancement of low electric-field hole mobility in metal source/drain Ge p-channel metal-oxide-semiconductor field-effect transistors by introduction of Al and Hf into $SiO_2$/$GeO_2$ gate stack", Appl. Phys. Lett., vol. 103, pp. 122106(1-4), September 2013.

[9] E. Simoen et al., "Low frequency-noise investigation of n-channel bulk FinFET developed for one-transistor memory cells, IEEE Trans. Electr. Dev., vol 59, no. 5, pp. 1242-1278, May 2012.

[10] I-. Wong et al., "Fabrication and low temperature characterization of Ge (110) and (100) p-MOSFETs", IEEE Trans. Electr. Dev., vol. 61, no. 6, pp. 2215-2219, June 2014.

[11] E. Ioannidis et al., "Improved analysis and modeling of low-frequency noise in nanoscale MOSFETs," Solid-State Electron., vol. 76, pp. 54-59, October 2012.

[12] E. Simoen et al., "Low-frequency noise characterization of strained germanium pMOSFETs, " IEEE Trans. Electr. Dev., vol. 58, no. 9, pp. 3132-3139, September 2011.

[13] W. Fang et al., "Low-frequency noise characterization of $GeO_x$ passivated germanium MOSFETs," IEEE Trans. Electr. Dev., vol. 62, no. 7, pp. 2078-2083, June 2015.

# A novel 3D pixel concept for Geiger-mode detection in SOI technology

M. M. Vignetti* [a], F. Calmon [a], P. Lesieur [a], F. Dubois [a], T. Graziosi [a], A. Savoy-Navarro [b]

[a] *Institut des Nanotechnologies de Lyon, Université de Lyon, France*
[b] *Laboratoire d'AstroParticule et Cosmologie, Université Paris-Diderot, Paris, France*

***Abstract* — In this paper, a novel SPAD architecture implemented in Silicon-On-Insulator (SOI) CMOS technology is proposed. Thanks to its intrinsic 3D structure, the proposed solution is expected to allow very small pixels while enabling a very high fill factor. Furthermore, the pixel read-out electronics as well as the whole detector electronics can benefit of the well-known advantages brought by SOI technology with respect to bulk CMOS, such as higher speed and lower power consumption. TCAD simulations based on realistic process parameters provided by the foundry are carried out in order to optimize and validate the avalanche diode architecture for an optimal electric field distribution in the device and to obtain a first order estimation of the main parameters of the SPAD, such as the breakdown voltage, the avalanche triggering probability and the dark count rate.**

***Keywords* — 3D pixel, SOI, FDSOI, geiger-mode, avalanche diode, SPAD, dark count rate, TCAD simulations.**

## I. Introduction

Single-Photon Avalanche Diodes (SPADs) have been extensively studied and implemented for the detection of weak optical signals in the visible and near-infrared spectrum range [1] and, during the last few years, in the field of High Energy Physics and Medical Physics for the detection of ionizing particles in tracking applications [2]. A SPAD consists of a p-n junction which is reverse biased above the breakdown voltage $V_{bd}$ by an excess bias $V_{ex}$. When an electron-hole pair (EHP) is generated in the space charge region (SCR) of the junction, a self-sustained charge multiplication process by impact ionization could be triggered, giving rise to a macroscopic electric current. Such a high current usually translates into a high current density which could cause permanent damages in the device. For this reason, every pixel needs suitable "quenching" electronics responsible for interrupting the multiplication process right after the avalanche build-up by promptly lowering the reverse bias of the junction below the breakdown threshold. The electronics will also restore the junction to the initial bias (reset phase) after a certain dead-time (hold-off time) during which the pixel is "blind" to any incoming photon. The whole quench / recharge cycle provides the information that an event has occurred [1].

In this work, a novel SPAD architecture consisting of a 3D pixel with associated quenching electronics is presented. The pixel is conceived for advanced Silicon-On-Insulator (SOI) CMOS technology and it is suitable for the detection of ionizing particles as well as light (visible and near-infrared range) in backside illumination (BSI) mode. Thanks to its 3D structure, the proposed solution is expected to allow very small pixels (down to a few $\mu m^2$) while enabling high fill factor. Moreover, the pixel read-out electronics as well as the whole detector electronics can benefit of the well-known advantages brought by SOI technology such as higher speed and lower power consumption with respect to bulk CMOS. To the best of the authors' knowledge, this is the first time that a 3D monolithic SPAD integrated in a standard SOI CMOS process is proposed and studied by means of TCAD simulations.

## II. 3D pixel concept for SPAD in SOI technology.

Compared to SPAD architectures conceived for SOI technology so far [3-5], the pixel proposed in this work has a monolithic 3D structure consisting of an avalanche diode beneath the Buried Oxide (BOX) and dedicated electronics in the SOI layer (Figure 1). The pixel has been designed according to the features of an advanced Fully-Depleted (FD) SOI technology, by exploiting the available implantations and diffusions that are normally meant to provide different back-biasing strategies for the transistors (Figure 1). The diode sensitive region is defined in the SCR of a p-well/deep n-well junction. Premature Edge Breakdown (PEB) risk is prevented thanks to a guard-ring placed around the sensitive area. A low doped p-type region can indeed be obtained thanks to the retrograde doping of the deep n-well in the epitaxial p-type substrate. Such a region is responsible for smoothing down the electric field at the junction edge that otherwise would be too intense to allow Geiger-mode operation. The diode can be connected to its associated electronics thanks to back-gating contacts featured by the adopted SOI technology (originally meant to enable threshold "tuning"). Two different biasing options are possible for the avalanche diode, depending on whether the output node is the anode (diode TOP) or the cathode (diode BOTTOM) as shown in Figure 2. It is important to point out that the p-well placed below the BOX (the avalanche diode's anode) acts as a back-gate for the transistors' channel in the SOI, i.e. the threshold voltage is affected by the bias chosen for the anode. It is therefore recommended to bias the p-well at ground in order to prevent any threshold variation for the transistors. In the "diode BOTTOM" configuration (chosen for the TCAD study discussed in Section III) the output is sensed at the cathode, i.e. the deep n-well in Figure 1, while the anode (according to the above discussion) is biased at ground avoiding any transistor's threshold variation.

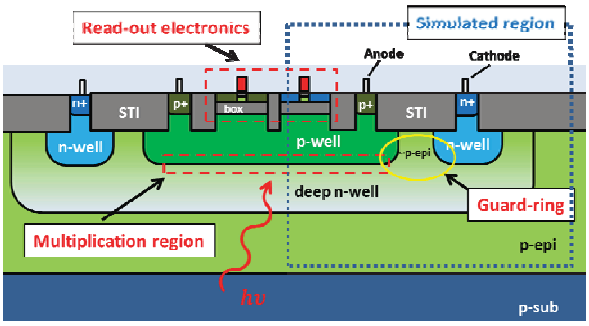



Fig. 1: Schematic representation of the proposed 3D pixel based on an advanced FDSOI technology.

*(*) ESR supported by the 2012-FP7-ITN, n° 317446, INFIERI EU*

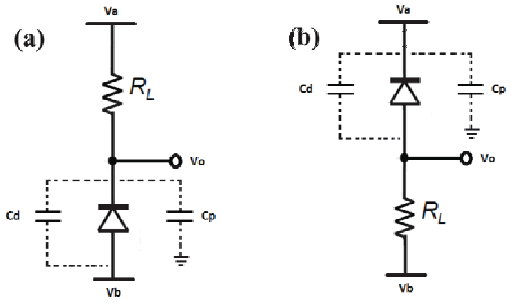



Figure 2: Schematic circuit (simplified) of a) "diode BOTTOM" configuration showing all the capacitive contributions b) "diode TOP" configuration. Observe that $C_d$ and $C_p$ are the p-well/deep-n-well and deep n-well / p-substrate space charge capacitances respectively.

However, under this configuration, the output voltage falls within the range $V_{bd} \leftrightarrow V_{bd} + V_{ex}$ which is not compatible with standard digital voltage levels, i.e. $0 \leftrightarrow V_{dd}$. This requires an additional DC decoupling capacitor between the output of the avalanche diode and the pixel electronics. In the "diode TOP" configuration, the p-well bias cannot be stuck at ground since the anode is the output node, swinging within the voltage range $0 \leftrightarrow V_{ex}$ which is compatible with standard voltage levels if $V_{ex}^{max} = V_{dd}$. During every avalanche event the transistors in the SOI layer would thus experience higher or lower threshold voltages with respect to the "quiescence state" ones, depending on the channel type. For this reason such a configuration requires pixel electronics insensitive to back-gating effects.

## III. Simulation Methodology

Simulations represent an important step to validate the avalanche diode architecture, especially the effectiveness of the guard-ring in preventing premature breakdown at the edge of the device sensitive region. They also provide a first order estimation of the main parameters of a SPAD, such as the breakdown voltage $V_{bd}$, the avalanche triggering probability $P_{tr}$ and the dark count rate (DCR), which is a very important figure of merit for this king of device. TCAD simulations of the 3D pixel have been thus carried out based on realistic process parameters provided by the foundry. The pixel has been modeled as a two-dimensional geometry representing the radial cut of an avalanche diode with cylindrical symmetry. This allowed emulating the geometry of a 3D device while dramatically reducing the overall computational time. Carrier transport in the device has been described by the drift-diffusion equation, accounting for the Fermi-Dirac statistics for the electrons and holes distribution in the semiconductor. The TCAD physical model considered the doping dependence of the carriers' mobility thanks to the Masetti model whose parameters for Silicon are based on the experimental data reported in [6]. The avalanche charge multiplication process depends on the ionization coefficients for electrons and holes, $\alpha_e$ and $\alpha_h$ respectively, which have been calculated according to the "van Overstraeten – De Man" model based on experimental data reported in [7]. Shockley-Read-Hall (SRH) and band-to-band (B2B) tunneling processes have been considered as the main contributors for the evaluation of the EHP generation-recombination within the avalanche diode

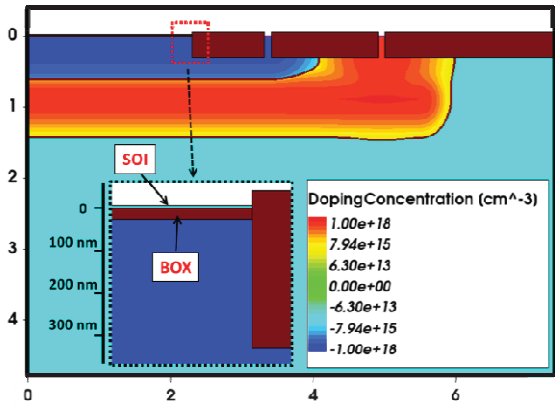



Fig. 3: TCAD geometrical model of the 3D SOI pixel. The insert shows the ultra-thin silicon layer over the buried oxide. (Positive values refer to n-type doping. Spatial scales are in µm).

sensitive volume. The SRH model accounts for the presence of deep defect levels in the Silicon energy gap, while the B2B one considers the electrons and holes generation enhancement due to the potential barrier thinning along the multiplication region when the diode is reverse biased above the breakdown voltage. The SRH process is strongly dependent on the carriers' lifetime $\tau_{n,p}$ that in turn depends on many factors such as impurity and doping concentration. Typical values of $\tau_{n,p}$ range from 1ms to 1 $\mu s$ depending on silicon purity, and fall down to about 10ns only in case of extremely high doping levels where Auger recombination plays a crucial role [8]. For this reason the authors decided to evaluate the SRH generation process under two different scenarios, one accounting for a doping dependent carrier lifetime according to the "Scharfetter model" [9], the other considering constant carrier lifetimes $\tau_n = 10\mu s$ and $\tau_p = 3\mu s$, for electrons and holes respectively [10]. Band-to-Band tunneling has been modeled with the field-enhanced Schenk model neglecting the phonon-assisted tunneling contribution since the electric field peak in the avalanche diode is not expected to exceed the value of $8x10^5$ V/cm [11]. Both the physical models as well as their parameters are provided by the TCAD software. In the present study the authors have chosen to keep the value proposed by the simulation tool for the model parameters [10].

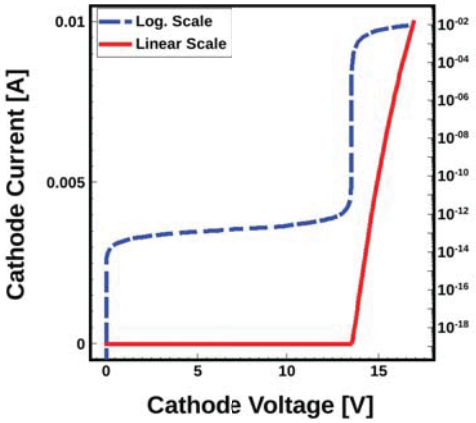



Fig.4: TCAD Simulation: Reverse bias I-V curve of the avalanche diode. (Sensitive area diameter D = 7µm)

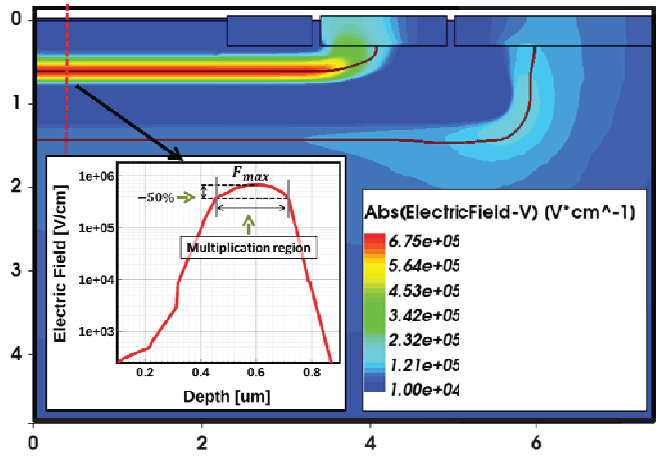



Fig.5: TCAD Simulation: Electric field color map of the pixel, when the avalanche diode is reverse biased at $V_{rev} = 16.5$ V (Spatial scales are in µm)

## IV. Results and Discussions

The simulated reverse bias $I-V$ curve of avalanche diode is plotted in Figure 4, showing a breakdown voltage $V_{bd} = 13.5V$. Unfortunately there are no experimental data available for the adopted technology that would allow validating the obtained results. Moreover it is important to point out that the ionization coefficients leading to such a value have been calculated under the assumption that the electric field can be considered constant over the ionization path [8]. This condition is generally not true for SPAD realized in very deep sub-micrometer CMOS technology since the electric field is sharply distributed along the diode SCR due to the typically abrupt and highly doped pn junction defining the avalanche multiplication region. However the SPAD proposed in the present study could be considered to satisfy (to some extent) such an assumption thanks to the "linearly graded" p-well / deep n-well junction, leading to a quite smooth electric field distribution within the multiplication region (see insert in Figure 5). The simulated results are therefore expected to not differ too much from experimental data. TCAD simulations of the 3D pixel have thus been carried out for several excess bias $V_{ex}$ above the extracted breakdown voltage, within the range 0 V ↔ 3V. Figure 5 shows the electric field color map of the pixel when the avalanche diode is reverse biased at $V_{rev} = 16.5\ V$ (i.e. an excess bias of $V_{ex} = 3\ V$) with grounded anode. As expected, the retrograde n-type doping in the deep n-well effectively acts as guard-ring preventing any peripheral breakdown at the p-well edges and thus defining an uniformly distributed electric field all over the device active region. Figure 6 shows the two main EHP generation mechanisms occurring in the avalanche diode under the same bias adopted for Figure 5 ($V_{ex} = 3\ V$). The curves have been extracted from a cut-line within the device active region, along the vertical direction with respect to the geometry shown in Figure 3. Provided that the cutline is taken at a horizontal position sufficiently distant from the guard-ring, it is indeed possible to consider the EHP generation profiles to be constant along the horizontal direction (1D symmetry). According to Figure 6, SRH generation seems to be the dominant generation

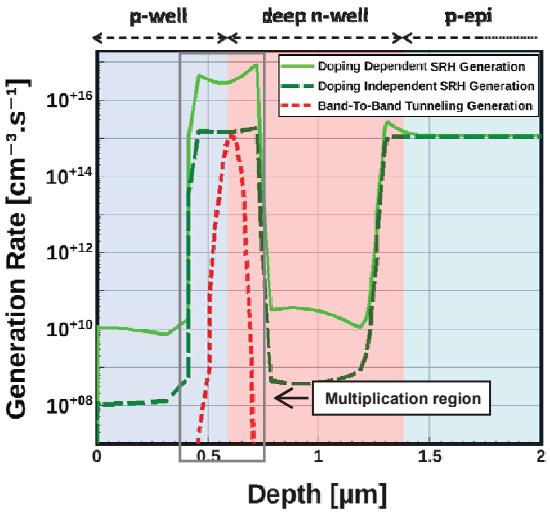



Fig.6: TCAD Simulation: EHP generation mechanisms in the multiplication region of the diode at $V_{rev} = 16.5V$.

mechanisms in the avalanche diode sensitive region. Even if tunneling generation peaks to a value very close to the doping independent SRH generation, the former is very narrowly distributed along the junction, leading to a minor contribution to the overall EHP generation. This result, if confirmed with experimental data, might be very important since it would indicate that the physical source of the device DCR is only temperature dependent, and does not degrades with the electric field. Moreover a field-enhanced-free generation process indicates that a low DCR could be attained with the adopted FDSOI technology. The ionization coefficients for the electrons and holes, $\alpha_e$ and $\alpha_h$ respectively, have been extracted along the same cutline considered for Figure 6. This allowed extracting the "avalanche triggering probability" $P_{tr}$ as a function of the excess bias voltage, by implementing a numerical method based on reference [12] (Figure 7). This latter parameter represents the probability that an EHP generated in the multiplication region can successfully trigger an avalanche, and can provide an estimation of the SPAD DCR if combined with the EPH generation rate, as follows:

$$DCR = \int_0^W P_{tr}(x) G_{EHP}(x)\, dx \qquad (1)$$

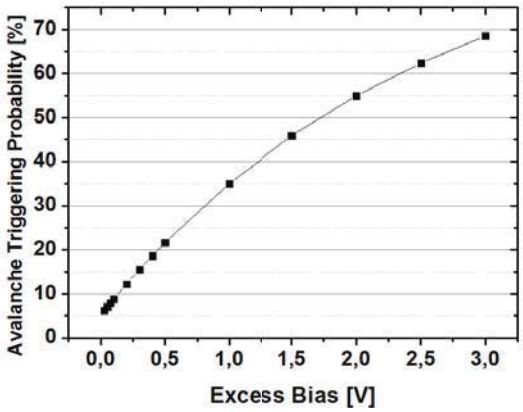



Fig.7: Avalanche triggering probability calculated according to reference [12].

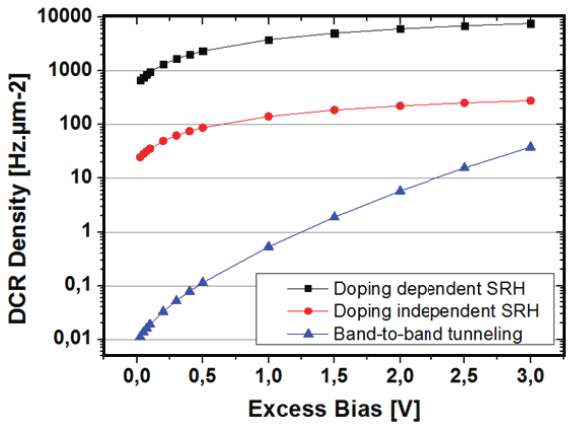



Fig.8: Estimated DCR per unit surface for the simulated avalanche diode.

where $W$ is the SCR width (active area) of the SPAD, while $P_{tr}(x)$ and $G_{EHP}(x)$ are the avalanche triggering probability and the EHP generation rate, respectively, as a function of the position $x$ within the diode SCR. The device DCR as a function of the excess bias has been finally calculated according to equation (1), by considering either a doping dependent or a doping independent SRH generation mechanism. The curves resulting from the two models are shown in Figure 8, and look widely vertically shifted between them by more than one order of magnitude. Based on these results one can imagine that the device DCR would be probably somewhere in between the two curves, even if the latter model provides results that are closer to what can be found in literature for avalanche diodes having similar breakdown voltages, i.e. $DCR \sim 150\, Hz/\mu m^2$ for $V_{ex} = 1V$[4]. In reality it is really hard to make any conclusion without any support coming from experimental data, which is not available at the present moment. Therefore a deeper study on the adopted models and their parameters would be really of crucial importance to better calibrate the adopted models and get any accurate clue about the device DCR.

Figure 9 shows finally two possible matrix arrangements for the proposed pixel. Solution (a) provides shielding of the pixel electronics by grounding the p-well. The output is thus sensed

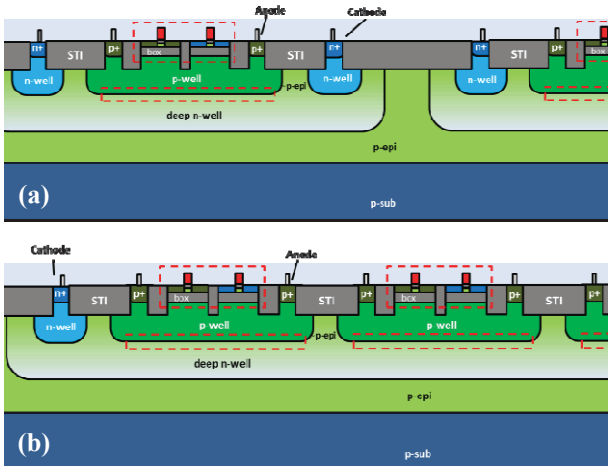



Fig.9: Possible matrix arrangements for the proposed pixel. Solution (a): grounded anode. Solution (b): common deep n-well

at the cathode which penalizes the fill-factor as every pixel needs an independent deep n-well. Solution (b) enables higher fill factor (common deep n-well) but the electronics need to be insensitive to back-gating effects.

## V. Conclusions

In this paper, a novel 3D pixel architecture consisting of a SPAD with associated electronics has been introduced together with possible matrix arrangements for imaging systems. The pixel has been conceived for advanced SOI technology and thanks to its 3D structure, is expected to allow very small pixels while enabling high fill factor. TCAD simulations based on realistic process parameters allowed validating the avalanche diode architecture for an optimal electric field distribution in the device active area. Simulations provided as well first order information about the main parameters of the SPAD, especially the breakdown voltage and the dark count rate. However these parameters need to be validated with experimental data or re-evaluated after a deeper study on the adopted physical models and parameters to better calibrate the TCAD environment and get more precise results.

## Acknowledgments

This project has been funded from the European Union's 7th Framework Program for research, technological development and demonstration under grant agreement n° 317446

## References

[1] S. Cova et al. "Avalanche photodiodes and quenching circuits for single-photon detection", App. Opt., Vol. 35, No. 12, April 1996

[2] E. Vilella et al. "A gated single photon avalanche diode array fabricated in a conventional CMOS process for triggered systems", Sens. Actuators A: Physical, Vol. 186, pp. 163-168, October 2012

[3] Y. Zou et al. "Backside illuminated wafer-to-wafer bonding single photon avalanche diode array" 10th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), 2014

[4] M.J. Lee et al. "A first single-photon avalanche diode fabricated in standard SOI CMOS technology with a full characterization of the device" Opt. Exp., Vol. 23, No. 10

[5] P. Sun et al. "A Flexible Ultrathin-Body Single-Photon Avalanche Diode With Dual-Side Illumination" IEEE Journal of Selected Topics in Quantum Electronics, vol.20, no.6, pp.276-283, 2014

[6] G. Masetti et al. "Modeling of Carrier Mobility Against Carrier Concentration in Arsenic, Phosphorus, and Boron-Doped Silicon," IEEE Transactions on Electron Devices, vol. ED-30, no. 7, pp. 764–769, 1983

[7] R. van Overstraeten and H. de Man, "Measurement of the Ionization Rates in Diffused Silicon p-n Junctions," Solid-State Electronics, vol. 13, no. 1, pp. 583–608, 1970.

[8] Gulinatti et al. "Modeling photon detection efficiency and temporal response of single photon avalanche diodes" *Proc. SPIE* 7355, Photon Counting Applications, Quantum Optics, and Quantum Information Transfer and Processing II, 73550X, May 2009

[9] D. J. Roulston et al. "Modeling and Measurement of Minority-Carrier Lifetime versus Doping in Diffused Layers of n+p Silicon Diodes" IEEE Transactions on Electron Devices, vol. ED-29, no. 2, pp. 284–291, 1982

[10] Sentaurus Device User Guide

[11] A. Schenk "Rigorous Theory and Simplified Model of the Band-to-Band Tunneling in Silicon," Solid-State Electronics, vol. 36, no. 1, pp. 19–34, 1993

[12] R. J. McIntyre "On the Avalanche Initiation Probability of Avalanche Diodes above the Breakdown voltage", IEEE Transactions on Electron Devices, Vol. ED-20, No. 7, pp. 637-641, July 1973

# Analog Performance of n- and p-FET SOI Nanowires Including Channel Length and Temperature Influence

Bruna Cardoso Paz and Marcelo Antonio Pavanello
Department of Electrical Engineering
Centro Universitário da FEI
São Bernardo do Campo, Brazil
bcpaz@fei.edu.br

Mikaël Cassé, Sylvain Barraud, Gilles Reimbold, Maud Vinet and Olivier Faynot
Département des Composants Silicium – SCME/LCTE
CEA-LETI Minatec
Grenoble, France

***Abstract*—This work aims to present the analog performance of silicon n-type and p-MOSFET SOI nanowires. Analog parameters are shown at room temperature for both n- and p-type, long and short channel devices with different channel width. Results for long channel n-MOS nanowires are investigated for the first time for low temperatures down to 100K. Moreover, an analysis is shown comparing the intrinsic voltage gain in nanowires and quasi-planar transistors. The mobility dependence on the temperature is found to be the key parameter to describe the behavior of both transconductance and output conductance when decreasing temperature.**

***Keywords—analog performance; nanowires; low temperature; mobility dependence***

## I. INTRODUCTION

The scaling of transistors is a request for the continuity of the CMOS roadmap. Reducing the short channel effects is then a matter of necessity to allow good performance of the devices. Following this idea, multiple gate field effect transistors have been developed in order to improve the gate electrostatic control over the channel charges, allowing scaling beyond the limits imposed by usual planar devices [1].

Due to their excellent performance recently reported [2, 3], nanowires (NWs) have shown to be of great interest. Many works have demonstrated their efficiency concerning digital applications [4], transport characteristics [5] and fabrication process [3], but not much attention has been paid concerning analog applications [6]. The study of analog performance is important for integration of such ultimate devices in mixed analog-digital circuits.

In this work we extend the results of [6] and present for the first time an experimental study of analog properties for both n- and p-MOS SOI NWs with long (L = 10μm) and short (L = 40nm) channel lengths as a function of the fin width ($W_{FIN}$), where the long channel n-MOS are analyzed down to 100K. The analog performance of NWs and quasi-planar MOSFETs are compared through the following figures of merit: transconductance ($g_m$), output conductance ($g_D$), intrinsic voltage gain ($A_V$), transconductance over drain current ratio ($g_m/I_{DS}$) and Early voltage ($V_{EA}$). Moreover, effective mobility ($\mu_{eff}$) as a function of temperature is also explored in order to justify the behavior observed for $g_m$ and $g_D$.

Acknowlegdements to the IBM/STMicroelectronics/Leti Joint Development Alliance, CNPq, CAPES and FAPESP.

## II. DEVICES AND MEASUREMENTS

The studied transistors are silicon [110]-oriented triple gate NWs fabricated at CEA–Leti. Devices were fabricated using Silicon-On-Insulator (SOI) substrate with 145nm thick buried oxide. A multi finger structure with 50 fins in parallel is implemented. Gate stack is composed by HfSiON/TiN (EOT = 1.4nm) and silicon thickness ($t_{Si}$) is found to be around 11nm. Details about the fabrication of the transistors can be found in [2] and [7]. Fig. 1 presents a cross-section TEM image and a schematic of the studied Si NW FET.

The drain current normalized by effective channel width ($W_{ef} = 2t_{Si} + W_{FIN}$) as a function of gate voltage ($V_{GS}$) with drain voltage ($V_{DS}$) of 40mV for long channel n-MOS NWs ($W_{FIN}$ = 14.5nm) and quasi-planar ($W_{FIN}$ = 10μm) devices from room temperature down to 100K are shown in Fig. 2. At 300K, long channel n- and p-type devices present subthreshold slope (S) of 61mV/dec. For the narrow n-MOS, S is equal to 28mV/dec at 100K and the threshold voltage variation with temperature ($\Delta V_{TH}/\Delta T$) is around 0.6mV/K, while S = 25mV/dec at 100K and $\Delta V_{TH}/\Delta T$ = 0.74mV/K for the quasi-planar n-MOS. From Fig. 2, from 100K to 300K, it is observed higher $I_{DS}/W_{ef}$ for the quasi-planar n-MOS in comparison to the NW, due to the higher $\mu_{eff}$. Table 1 reports results for n-MOS at 300K and 100K of $\mu_{eff}$, extracted at $N_{INV} = 0.8\times10^{13}cm^{-2}$ through the split C-V method [8], and series resistance ($R_S$), extracted according to [9]. From Table 1, it is observed that $\mu_{eff}$ of quasi-planar is 31% and 34% higher in comparison to the NW, at 300K and 100K, respectively.

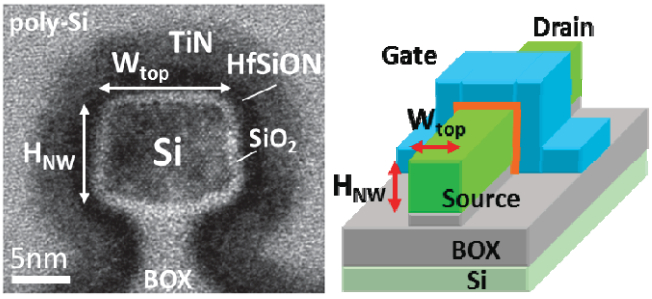



Fig.1. Si SOI NW cross section TEM image and schematic.

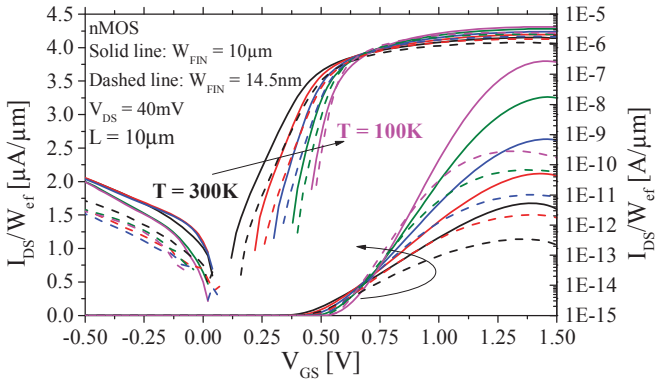



Fig.2. $I_{DS}/W_{ef}$ as a function of $V_{GS}$ for n- MOS at $|V_{DS}| = 40mV$.

TABLE I. EFFECTIVE MOBILITY AT $N_{INV} = 0.8\times10^{13}CM^{-2}$ AND SERIES RESISTANCE FOR N-MOS AT 100K AND 300K.

| | $\mu_{eff}$ [cm²/V.s] | | $R_S$ [kΩ] | |
|---|---|---|---|---|
| ***W_FIN*** | ***100K*** | ***300K*** | ***100K*** | ***300K*** |
| ***10µm*** | 626 | 283 | 0.9 | 1.8 |
| ***14.5nm*** | 466 | 216 | 8.7 | 14.8 |

Fig. 3 shows the $I_{DS} \times L$ for long (L = 10µm) and short (L= 40nm) channel p-MOS devices with narrow $W_{FIN}$ of 15nm and 25nm at room temperature. For p-MOS with L = 40nm and $W_{FIN}$ = 15nm, S is slightly degraded to 71mV/dec, while S = 83mV/dec for $W_{FIN}$ = 25nm. As $W_{FIN}$ increases, the short channel effects increase as well, due to the lower electrostatic control. The $V_{TH}$ roll-off from L = 10µm to 40nm is similar for both $W_{FIN}$ = 15nm and 25nm, being around 115mV. The short channel devices present lower $I_{DS} \times L$ than long channel p-MOS as $|V_{GS}|$ increases, indicating strong influence of series resistance effects.

## III. RESULTS AND DISCUSSION

### *A. Channel Width Influence for n- and p-MOS*

Fig. 4 presents both transconductance ($g_m/W_{ef}$) (A) and output conductance ($g_D/W_{ef}$) (B), normalized by the effective channel width, as a function of $W_{FIN}$. Devices operate in saturation regime with $|V_{DS}| = 0.9V$, and gate voltage overdrive ($V_{GT} = V_{GS} - V_{TH}$) of 0, 200 and 400mV, at room temperature, for L = 10µm.

From Fig. 4.A, one can note higher values of transconductance for n- than in p-MOS and a decreasing of $g_m$ (degradation) for n-MOS as $W_{FIN}$ is reduced, in comparison to p-MOS results. These effects are related to the electrons and holes mobility. While the effective mobility of holes is higher in (110)/[110], the effective mobility of electrons is higher in (100)/[110]. Being (110) the surface related to the fin height and (100) related to the fin width, reducing $W_{FIN}$ favors mobility in (110) plan in comparison to (100) plan [10]. For this reason p-MOS nanowires show improvements (increase)

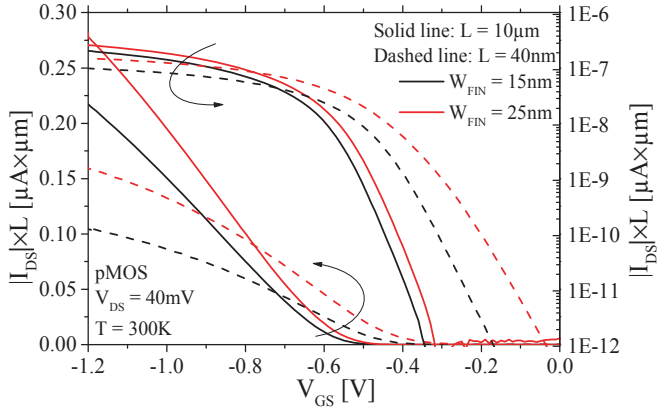



Fig.3. $|I_{DS}|\times L$ as a function of $V_{GS}$ for p-MOS at $|V_{DS}| = 40mV$.

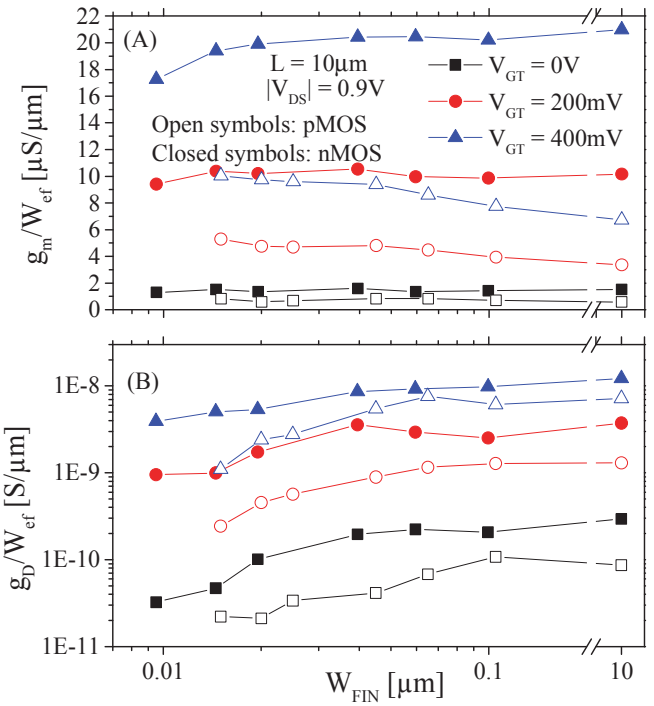



Fig.4. $g_m/W_{ef}$ (A) and $g_D/W_{ef}$ (B) as a function of $W_{FIN}$ for n- and p-MOS, L = 10µm, $|V_{DS}| = 0.9V$, $|V_{GT}| = 0$, 200 and 400mV.

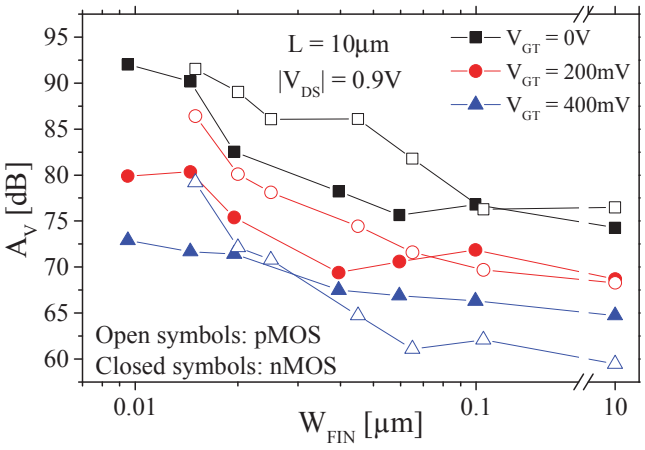



Fig.5. $A_V$ as a function of $W_{FIN}$ for n- and p-MOS at 300K, L = 10µm, $|V_{DS}|$ = 0.9V, $|V_{GT}| = 0$, 200mV and 400mV.

on the transconductance over wide planar FETs, while n-MOS show the opposite behavior. For n-MOSFETs, $g_m$ degradation is 19% and for p-MOSFETs the improvement is 52%, comparing the narrowest and the widest transistors for $V_{GT}$ equal to 400mV.

Fig. 4.B shows the decreasing of the output conductance (which means an improvement of $g_D$) as $W_{FIN}$ is reduced for both n- and p-MOS. Comparing the narrowest and the widest transistors, this improvement almost reaches one order of magnitude. As $g_D$ indicates the relation between $I_{DS}$ and $V_{DS}$ ($g_D = \delta I_{DS}/\delta V_{DS}$), its behavior is mainly related to the channel modulation effect (CME), where CME is expected to be reduced in NWs in comparison to planar transistors due to the better electrostatic gate control over the charges.

From $g_m$ and $g_D$, the intrinsic voltage gain has been calculated through the $g_m/g_D$ ratio and the results for $A_V$ as a function of $W_{FIN}$, at $|V_{DS}|$ = 0.9V, and $|V_{GT}|$ = 0, 200 and 400mV is shown in Fig.5 for L = 10µm and in Fig.6 for L = 40nm. Due to the behavior of $g_m$ and $g_D$, it is observed an strong improvement for nanowires in comparison to wide transistors. As $A_V$ follows the trend of the inverse of $g_D$, for both n-type and p-MOS, it is observed an increase of $A_V$ decreasing $W_{FIN}$. The narrowest NWs allow an intrinsic voltage gain 20dB higher than the wide planar device for both n- and p-MOS with L = 40nm.

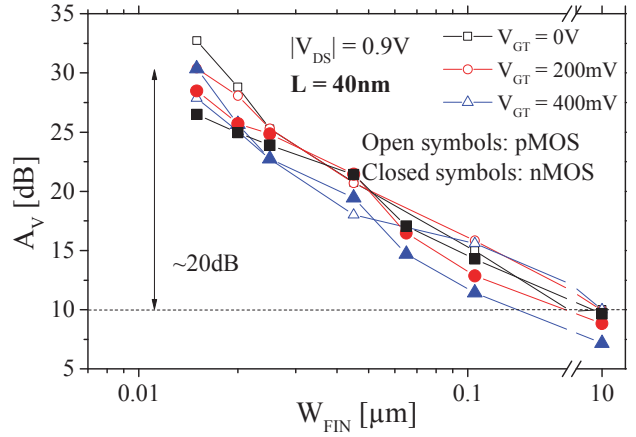



Fig.6. $A_V$ as a function of $W_{FIN}$ for n- and p-MOS at 300K, L = 40nm, $|V_{DS}|$ = 0.9V, $|V_{GT}|$ = 0, 200mV and 400mV.

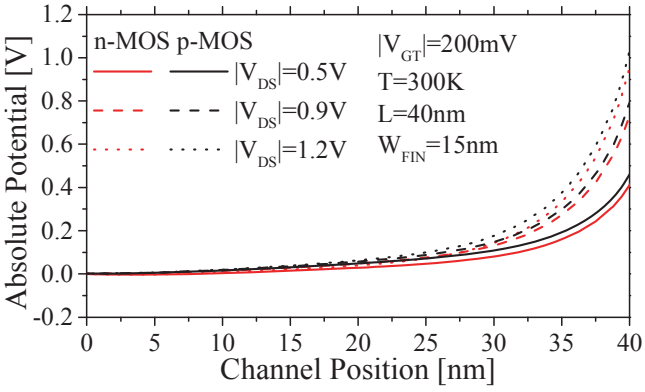



Fig.7. Simulation results for the potential along the channel length for n- and p-MOS at 300K, L = 40nm, $W_{FIN}$ = 15nm, $|V_{GT}|$ = 200mV, $|V_{DS}|$ = 0.5, 0.9 and 1.2V.

Although n-type and p-MOS present different values for $g_m$, their results obtained for $g_D$ are close, mainly for short channel transistors, which leads to similar values for $A_V$, varying $W_{FIN}$. In order to explain this effect, tridimensional numerical simulations have been performed with Sentaurus Device Simulator, from Synopsys [11]. In Fig. 7 it is presented the simulated results for the potential extracted at the interface $SiO_2$/Si of n- and p-MOS with L = 40nm and $W_{FIN}$ = 15nm, varying $V_{DS}$ from 0.5 to 1.2V. It is observed that the potential distribution inside the channel is similar for both n- and p-MOS, varying $V_{DS}$, suggesting similar CME, which can explain the fact that $g_D$ and, as a consequence, $A_V$ behaves similarly comparing n- and p-MOSFETs.

## B. *Temperature Influence*

In Fig. 8, $g_m/I_{DS}$ is presented as a function of $V_{GT}$ for long channel n-MOS, at $V_{DS}$ = 0.9V. Wide and NW FETs are compared from 300K to 100K. It is observed an increase of $g_m/I_{DS}$ by reducing either temperature or $W_{FIN}$ from 10µm to 14.5nm. According to [10], $g_m/I_{DS}$ at saturation regime can be estimated by

$$\left(\frac{g_m}{I_{DS}}\right)\Bigg|_{sat} = \frac{2}{V_{GT}} \times \left[\frac{1+\frac{(R_S \mu_{eff} C_{ox} W_{ef} V_{GT})}{2L}}{1+\frac{(R_S \mu_{eff} C_{ox} W_{ef} V_{GT})}{L}}\right] \quad (1)$$

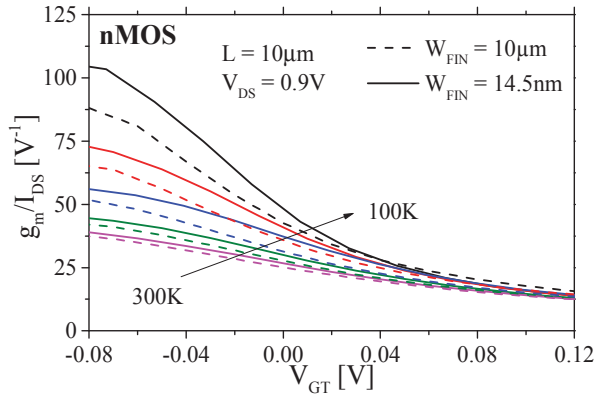



Fig.8. n- MOS, L = 10µm, results for $g_m/I_{DS}$ as a function of $V_{GT}$ at $V_{DS}$ = 0.9V.

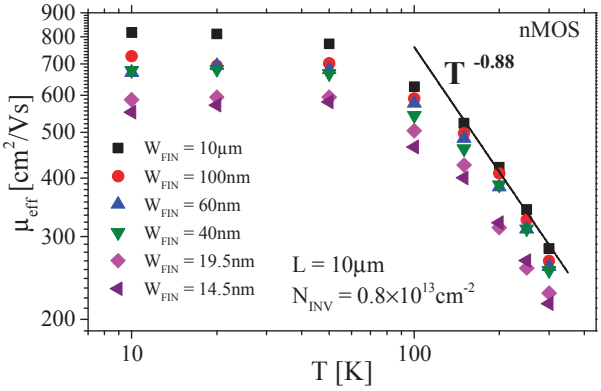



Fig.9. $\mu_{eff}$ as a function of T at $N_{INV} = 0.8\times10^{13}cm^{-2}$.

The parameters that are $W_{FIN}$ dependent are $R_S$, $\mu_{eff}$ and $W_{ef}$. From Table I, it is observed a variation for $R_S$ of a factor close to 10 for n-MOS, as $W_{FIN}$ goes from 10µm down to 14.5nm. This decrease of the series resistance with temperature is associated to the effective mobility increase [12]. The increase of $\mu_{eff}$ while increasing $W_{FIN}$ is smaller than a factor of 2. On the other hand, $W_{FIN}$ reduces almost 3 orders of magnitude, being the key parameter in (1), where it is observed that $g_m/I_{DS}$ varies with the inverse of $R_S \times \mu_{eff} \times W_{ef}$. This is why NWs show higher $g_m/I_{DS}$ than wide planar FETs.

Fig. 9 presents $\mu_{eff}$ as a function of T, for long channel n-MOS with several values of $W_{FIN}$, extracted at $N_{INV} = 0.8\times10^{13}cm^{-2}$. The temperature dependence coefficient of $\mu_{eff}$ is found to be around 0.88 for all devices, above 100K, where phonon scattering is dominant at moderate inversion.

Fig. 10 presents both $g_m/W_{ef}$ (A) and $g_D/W_{ef}$ (B) as a function of T, extracted at $V_{DS}$ = 0.9V and $V_{GT}$ = 400mV, for long channel n-MOS. By decreasing temperature, it is observed an increase of $g_m$ and $g_D$ with similar rate for both parameters,

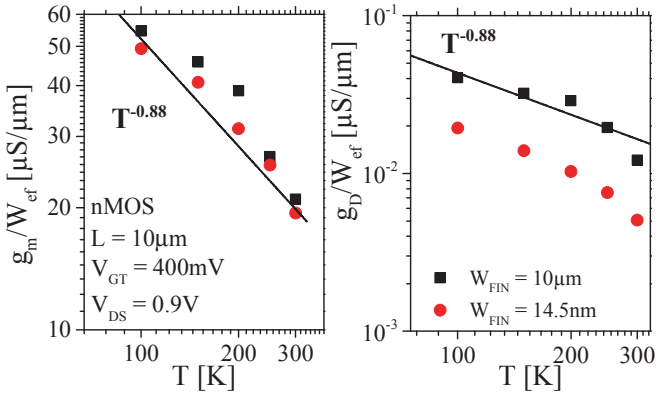



Fig.10. $g_m/W_{ef}$ (A) and $g_D/W_{ef}$ (B) as a function of T for n-MOS, L = 10µm, at $V_{DS}$ = 0.9V and $V_{GT}$ = 400mV.

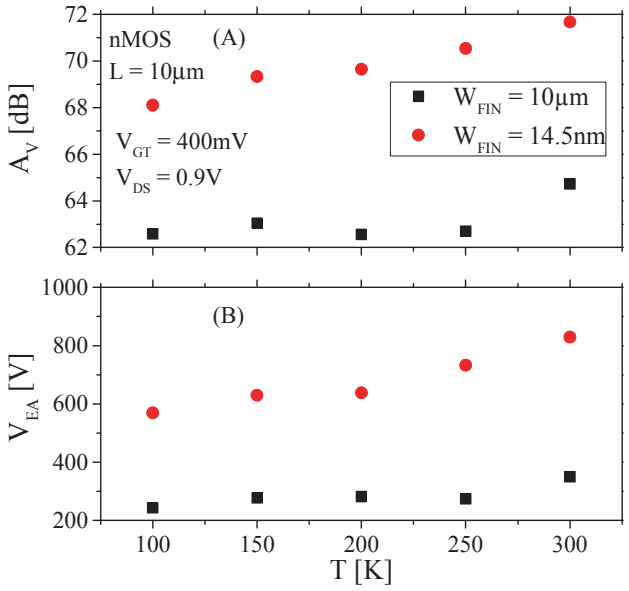



Fig.11. $A_V$ (A) and $V_{EA}$ (B) as a function of T for n-MOS, L = 10µm, at $V_{DS}$ = 0.9V and $V_{GT}$ = 400mV.

which is close to the same 0.88 factor obtained for the effective mobility dependence with T, in Fig. 9. It means that the most part of the variation of $g_m$ and $g_D$ with temperature is due to the effective mobility behavior.

As a result, in Fig. 11 we observe that the influence of T in $g_m$ and $g_D$ is almost annulated one by each other and $A_V$ shows a soft increase with T. As $g_D$ decreases with a rate higher than $g_m$, increasing T from 100K to 300K, $A_V$ shows an increase of 3.6dB and 2.1dB for $W_{FIN}$ = 14.5nm and 10µm, respectively. The Fig. 11 also shows high values of Early Voltage ($V_{EA} = I_{DS}/g_D$) for n-type NWs due to smaller CME.

## IV. Conclusions

This work has presented an experimental analysis of analog parameters for nanowires SOI MOSFETs considering long and short channel devices, n- and p-type devices and temperature down to 100K.

It was observed great improvements on the performance of NWs in comparison to wide planar transistors concerning $A_V$, due to improvements on the output conductance. The intrinsic voltage gain is similar for both n- and p-MOS varying $W_{FIN}$. $A_V$ is around 30dB for both short channel n- and p-MOS with $W_{FIN}$ = 15nm at room temperature.

Concerning temperature decrease, the effects on the effective mobility variation change both $g_m$ and $g_D$ with the same rate, leading to values approximately constant for the intrinsic voltage gain.

## References

[1] J. P. Colinge, "Multiple-gate SOI MOSFETs", Solid-State Electronics, vol. 48, pp. 897–905, 2004.

[2] R. Coquand et al., "Strain-induced performance enhancement of tri-gate and omega-gate nanowire FETs scaled down to 10nm width", Symposium on VLSI Technology, pp. 13–14, 2012.

[3] R. Coquand et al., ""Scaling of high-k/metal-gate Trigate SOI nanowire transistors down to 10nm width", 13th International Conference on Ultimate Integration on Silicon (ULIS), pp. 37–40, 2012.

[4] S. Bangsaruntip et al., "High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling", IEEE International Electron Devices Meeting (IEDM), pp. 1–4, 2009.

[5] M. Koyama et al., "Study of carrier transport in strained and unstrained SOI tri-gate and omega-gate silicon nanowire MOSFETs", Solid-State Electronics, vol. 84, pp. 46–52, 2013.

[6] V. Kilchytska, S. Makovejev, S. Barraud, T. Poiroux, J.-P. Raskin, D. Flandre, "Trigate nanowire MOSFETs analog figures of merit", Solid-State Electronics, vol. 112, pp. 78–84, 2015.

[7] S. Barraud et al., "Performance of omega-shaped-gate silicon nanowire MOSFET with diameter down to 8 nm", IEEE Electron Device Letters, vol. 33, pp. 1526–1528, 2012.

[8] A. Ohata et al., ULIS Dig (2006). 2006, p.133–136.

[9] A. Dixit, A. Kottantharayil, N. Collaert, M. Goodwin, M. Jurczak, K. De Meyer, "Analysis of the parasitic S/D resistance in multiple-gate FETs", IEEE Transactions on Electron Devices, vol. 52, pp.1132–1140, 2005.

[10] J. P. Colinge, Silicon-on-Insulator Technology: Materials to VLSI. 3ª Boston Edition, Kluwer Academic Publishers, 2003.

[11] Sentaurus Device User Guide, Version C-2009.06, 2009.

[12] M. A. Pavanello, J.A. Martino, E. Simoen, C. Claeys, "Cryogenic operation of FinFETs aiming at analog applications", Cryogenics, vol. 49, pp. 590–594, 2009.

# *Body factor scaling in UTBB SOI with supercoupling effect*

K.R.A.Sasaki[1,*] and J.A.Martino[1]
LSI/PSI/USP
University of Sao Paulo
Sao Paulo, Brazil
*katia@lsi.usp.br

C.Navarro[2,3], M.Bawedin[2], F. Andrieu[3] and S.Cristoloveanu[2]
[2]IMEP-LAHC, [3]CEA-LETI
MINATEC
Grenoble, France

***Abstract*—Focusing on the channel length scalability, this paper analyzes the coupling coefficient (body factor) in thick (25nm) and thin (7nm) UTBB SOI devices. Experimental data and simulations demonstrate that the supercoupling effect further improves the device scalability and operation in thin silicon films. The impact of thinning the gate oxide and body on the inter-channel coupling is also documented.**

***Keywords—UTBB SOI, supercoupling, body factor, coupling coefficient, channel length***

## I. Introduction

UTBB (ultrathin body and buried oxide) SOI device has been considered a good candidate for the sub-28nm technology node [1-4]. The body and buried oxide (BOX) thinning, together with a ground plane (GP) implantation beneath the BOX, improves the channel control. Enhanced inter-gate coupling occurs, offering a more efficient threshold voltage tuning by the back-gate bias ($V_{G2}$) and reduced source- and drain- fringing field effects [5-6]. UTBB devices can also operate with lower voltage for better power efficiency [3,4,7-8].

Si-film thinning below 10 nm enables extreme inter-gate coupling effects, like the supercoupling, to develop. Supercoupling prevents the independent operation of the front and back interfaces [9-11]. Reference [10] shows the channel length impact on the critical thickness, i.e., the thickest silicon film at which the supercoupling effect is present. Differently, the following analysis investigates the dependence of the coupling coefficient with the gate length to demonstrate that supercoupling helps to mitigate short-channel effects (SCE) in UTBB devices enabling a more aggressive downscaling.

## II. Device Characteristics

The UTBB SOI transistors under test were processed at LETI and STMicroelectronics. The SOI wafers have a 25nm-thick BOX. The silicon film thickness ($t_{Si}$), effective oxide thickness (EOT) of the high-k/metal gate stack, channel length (L) and channel doping ($N_{CH}$) of the measured and simulated devices are presented in Table I. The simulations parameters follow the characteristics of the measured devices, considering quantum model.

TABLE I. Measured devices details

| From | $t_{Si}$ (nm) | EOT (nm) | L (nm) | $N_{CH}$ ($cm^{-3}$) |
|---|---|---|---|---|
| LETI | 25 | 3.1 | 50-1000 | $2x10^{17}$ |
| ST | 7 | 1.3 | 30-1000 | $1x10^{15}$ |
| 2D-Numerical Simulations | 25 | 3 | 50-1000 | $2x10^{17}$ |
| | 7 | 1 and 3 | 20-1000 | $1x10^{15}$ |

## III. Results and Analysis

Fig. 1 presents the experimental front-channel threshold voltage ($V_{T1}$) as a function of the back-gate bias ($V_{G2}$) for thick and thin silicon films. Fig. 2 shows the simulated front $V_{T1}(V_{G2})$ (figs. 2C and 2D) and the back $V_{T2}(V_{G1})$ (figs. 2A and 2B) coupling curves. Experimental and simulated $V_{T1}$ are extracted by the 2nd derivative method. The slope yields the coupling coefficients ($\alpha_1=\Delta V_{T1}/\Delta V_{G2}$ and $\alpha_2 = \Delta V_{T2}/\Delta V_{G1}$), which are compared in figs. 3A and 3B for different channel lengths and body thicknesses. Figs. 2 and 3 show that the coefficient $\alpha_2$ is higher than $\alpha_1$ because of the thinner front oxide compared to the BOX.

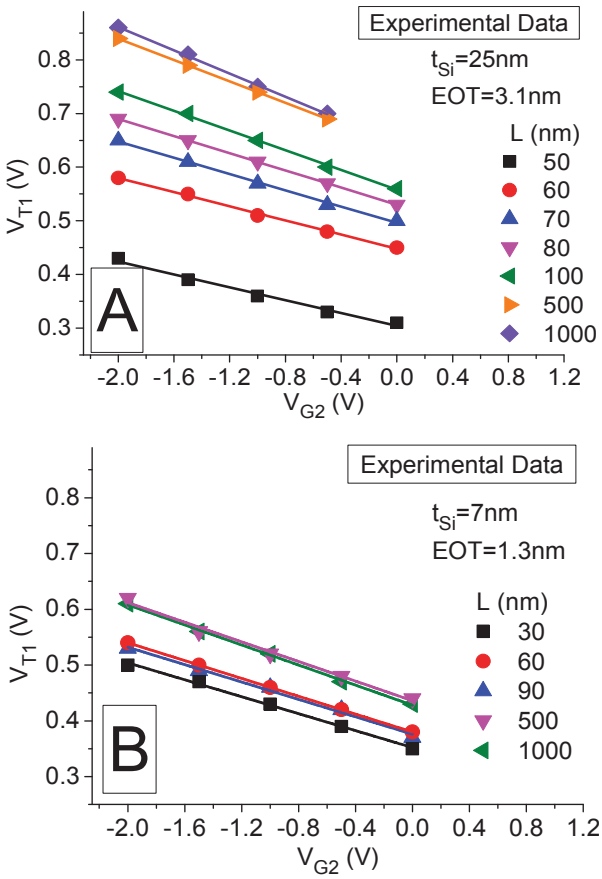



Fig. 1. Measured front-gate threshold voltage as a function of the back-gate bias for various channel lengths in thick (A) and thin (B) Si-films.

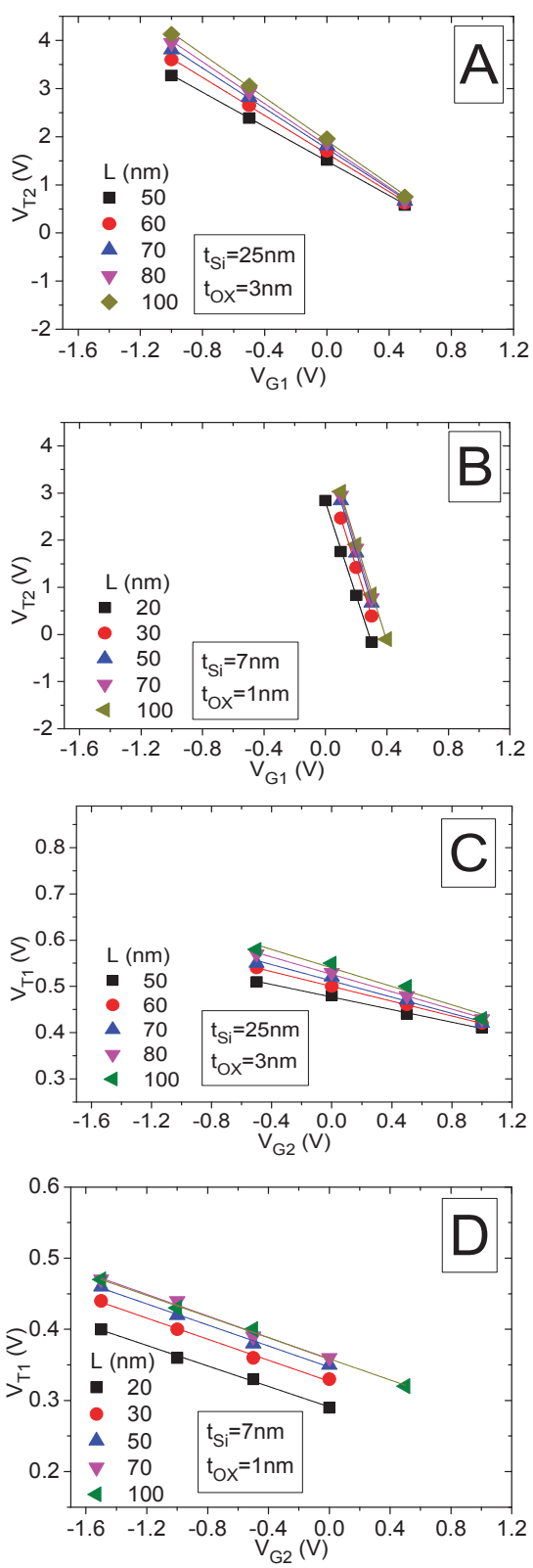



Fig. 2. Simulated threshold voltage of the back (A and B) and front (C and D) channels versus front (A and B) and back (C and D) gate biases for various channel lengths in thick (A and C) and thin (B and D) films.

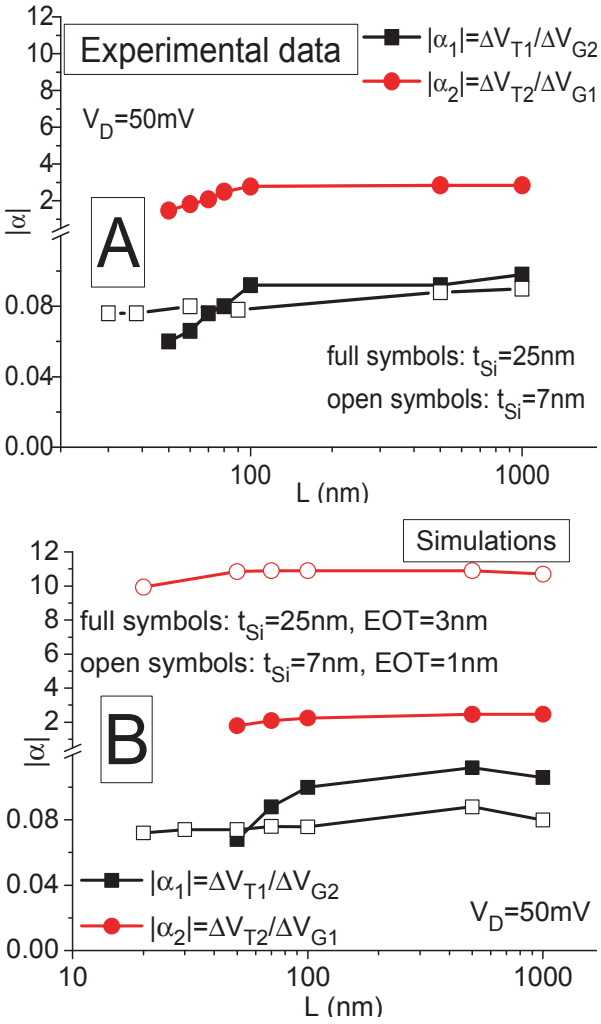



Fig. 3. Front and back coupling coefficients (α1, α2) versus channel length for thick ($t_{Si}$=25nm) and thin ($t_{Si}$=7nm) devices obtained by measurements (A) and simulations (B).

As the device length is downscaled, a reduction in $V_{T1,2}$ and coupling coefficients is observed due to SCEs (figs.1-3). This drop is more remarkable in thick SOI devices. For ultrathin Si-films, although the roll-off is still present, the coupling coefficient remain almost constant (figs.1-3), indicating that UTBB transistors can be further scaled down. This constant body factor is a consequence of the supercoupling effect.

The lower coupling coefficient α1 for thinner Si-film (see figs. 1-3) can be explained by fig. 4. The thinner front-gate oxide (open symbols), which is the case of the measured samples, degrades the back-gate impact on the $V_{T1}$. If the Si-film thickness were the only difference between the samples (half-filled and full symbols), the coupling would be stronger for thinner device. It follows that both, the front- and back-gate oxide, should be downscaled together to keep the coupling coefficient constant.

ISBN 978-1-4673-8608-1

IEEE Catalog number CFP1649D-USB

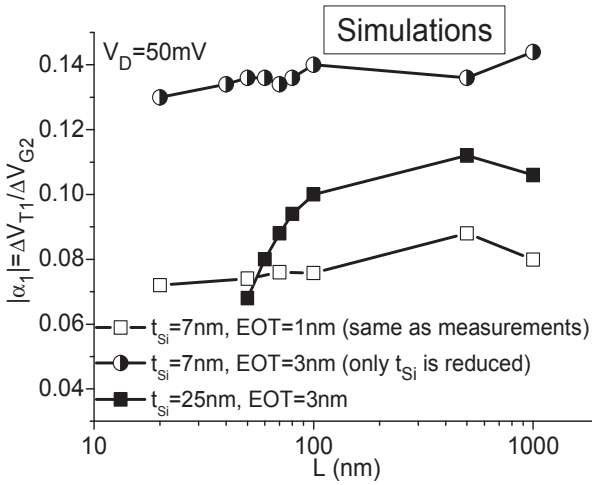



Fig. 4. Simulated coupling coefficient α1 as a function of channel length.

In order to analyze how the supercoupling benefits the scalability, the potential along the structure (at mid-channel from front to back gate) can be seen in fig. 5 for various channel lengths at $V_{G1}=V_{T1}$. For 25nm Si-film (fig. 5A), the potential at the back interface is enhanced in shorter channels due to the threshold voltage roll-off. The loss of the back interface control is caused by the fringing field spreading through the BOX.

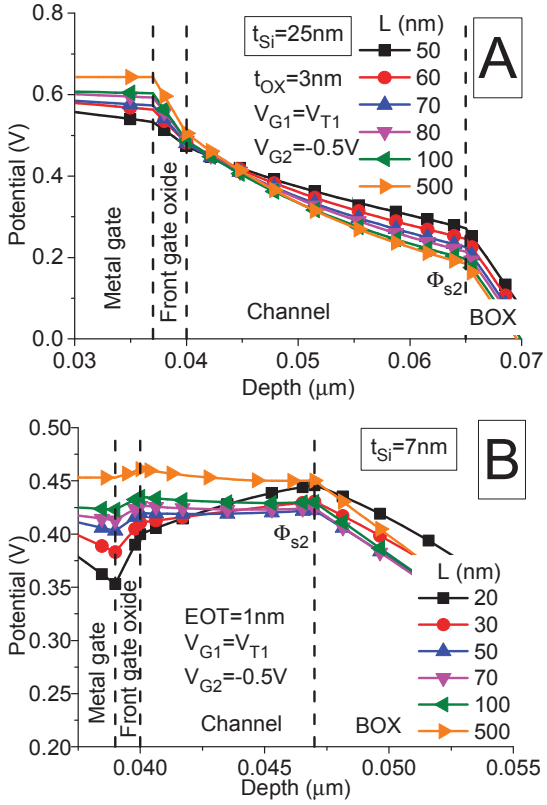



Fig. 5. Simulated potential for various channel lengths in 25nm- (A) and 7nm-thick (B) Si-film at mid-channel from front to back gate.

On the other hand, figs. 5B and 6 show that the front-gate coupling increases in thin SOI devices and the back interface tends to follow the potential at the front one, counteracting the fringing field impact. The result are: (i) a higher back-interface potential ($\Phi_{S2}$) than for 25nm-thick transistor, (ii) a $\Phi_{S2}$ reduction as the channel length is decreased down to 60nm and (iii) a slight increase in $\Phi_{S2}$ for channel lengths shorter than 60nm. Fig. 6 demonstrates how UTBB devices are more resilient against short-channel effects thanks to the limited source and drain charge sharing but also to the supercoupling effect.

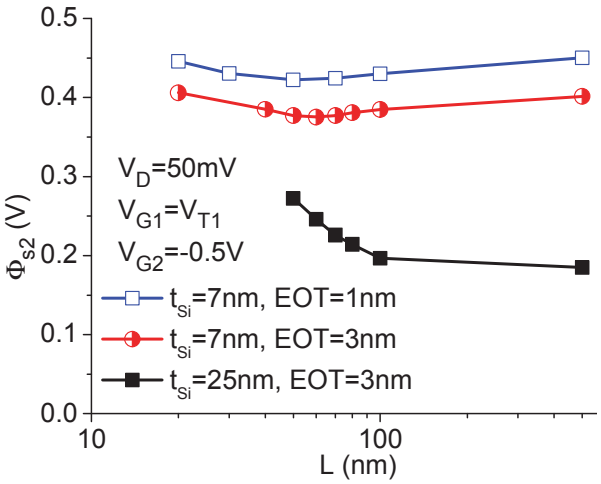



Fig. 6. Simulated back surface potential versus gate length for thick (25nm) and thin (7nm) films.

## IV. Conclusions

Measurements and simulations show the supercoupling impact on the back-surface potential as well as the variation of the coupling coefficient in UTBB SOI for different gate lengths. A stronger coupling in thin Si-films was observed by maintaining the same front-gate oxide thickness. Therefore, the thinner silicon film is a more scalable structure due to the limited charge sharing but also to the supercoupling effect.

## Acknowledgments

The authors acknowledge FAPESP, CNPq, ANR AMNESIA project (ANR 2011 JS03 001 01), Place2be, Way-to-go-fast, and Compose3 European projects for the financial support.

## References

[1] C. Fenouillet-Beranger et al., "FDSOI devices with thin BOX and ground plane integration for 32nm node and below", Solid-State Electronics, vol. 53, p. 730, 2009

[2] B.Y. Nguyen and C. Maleville, “FD-SOI: back to basics for best cost energy efficiency and performance”, 2014, in: www.advancedsubstratenews.com.

[3] S. Kimura, “Overview of ultra-low power devices, focus on SOTB”, Short Course of the IEEE S3S Conference, p. 79, 2014.

[4] Global Foundries (white paper), “FD-SOI Technology Innovations Extend Moore’s Law”, 2015, in: globalfoundries.com

[5] T. Ernst, C. Tinella, C. Raynaud and S. Cristoloveanu, “Fringing fields in sub-0.1µm fully depleted SOI MOSFETs: optimization of the device architecture”, Solid-State Electronics, vol. 46, n. 3, p. 373, 2002.

[6] W. Xiong and J.P. Colinge, “Self-aligned implanted ground-plane fully depleted SOI MOSFET”, Electronics Letters, vol. 35, n. 23, p. 2059, 1999.

[7] L. Le Pailleur, “Fully-Depleted-Silicon-On-Insulator From R&D Concept to Industriual Reality”, IEEE International SOI Conference, p.14, 2013.

[8] S. Nakamura, J.Kawasaki, Y. Kumagai and K.Usami, “Measurement of the minimum energy point in silicon on thin-BOX (SOTB) and bulk MOSFET”, Proceedings of EUROSOI-ULIS, p. 193, 2015.

[9] S. Eminente, S. Cristoloveanu, R. Clerc, A. Ohata and G. Ghibaudo.“Ultra-thin fully-depleted SOI MOSFETs: special charge properties and coupling effects,” Solid-State Electronics, vol. 51, n. 2, p. 239, 2007.

[10] C. Navarro, M. Bawedin, F. Andrieu, B. Sagnes, F. Martinez and S. Cristoloveanu. “Supercoupling effect in short-channel ultrathin fully depleted silicon-on-insulator transistors”. Journal of Applied Physics, vol. 118, p. 184504, 2015

# Current Mirrors with Strained Si Single Nanowire Gate All Around Schottky Barrier MOSFETs

K. Narimani, G. V. Luong, C. Schulte-Braucks,
S. Trellenkamp, Q.T. Zhao, S. Mantl
Peter-Grünberg-Institut (PGI 9-IT) and JARA-FIT
Forschungszentrum Jülich
Jülich, Germany
k.narimani@fz-juelich.de

M. F. Chowdhury
Cambridge CMOS Sensors
160 Cowley Road, Cambridge, CB4 0DL, UK

***Abstract*— In this work, we present a simple current mirror based on two single nanowire strained silicon Schottky barrier (SB) MOSFETs with gate-all-around (GAA) structure. $B^+$ implantation into $NiSi_2$ with dopant segregation at source and drain was used to decrease the Schottky barrier height for holes at the metal/channel junctions. The current mirror shows a very good Mirror Ratio MR = 0.99 and high output resistance of 100MΩ.**

***Keywords—Si nanowire schottky barrier MOSFET, $NiSi_2$, Implantation into silice, analog performance, current mirror***

## I. INTRODUCTION

As MOSFET reaches its physical scaling limit, new device concepts are required to overcome scaling problems in CMOS technology. One candidate is Schottky barrier (SB) MOSFET using metallic contacts that have lower parasitic source/drain (S/D) resistances with abrupt junctions at silicon/metal interfaces which overcome scaling limitations for short channel devices[1]. This can also improve energy efficiency over conventional MOSFETs. Moreover, replacing S/D with silicide requires low thermal budget and is silicon process compatible. One of the issues concerning this technology is optimization of line edge roughness quality of the silicide to prevent contact property variation, especially for analog circuits that need high matching between devices to perform properly. Improved control over silicide/channel interface by introducing ultra thin silicides on different SOI substrates has been exhibited [2], [3]. It has been shown that $NiSi_2$ is a promising candidate due to its small lattice mismatch with respect to silicon, high temperature stability and lower contact resistivity compared to NiSi and $Ni_{1-x}Pt_xSi$ [2]. However, these contacts still suffer from large SB heights that result in comparatively low on current and poor subthreshold swing. It has been shown that dopant implantation into silicide (IIS) can be used to tune Schottky barrier height (SBH) [4], [5], while preventing dopant diffusion far into the channel, the so-called dopant segregation [6]. Electrical properties of SBMOSFETs fabricated with IIS for planar [3] and NW-array gate-all-around (GAA) [7], [8] devices have been already investigated, showing improved current and sub-threshold slope for both n-type and p-type by dopant segregation. In this work, we aim to analyze the analog circuit performance of single NW strained silicon GAA SBMOSFETs by fabricating a simple current mirror based on two connected transistors. We demonstrate SBMOSFETs with high on-currents and good slopes. We also extract mirror ratio and output resistance of the fabricated current mirror circuit. It is shown that using SBMOSFETs, simple current mirrors with high output resistance can be fabricated, eliminating the need for more complex current mirror designs to achieve the same performance.

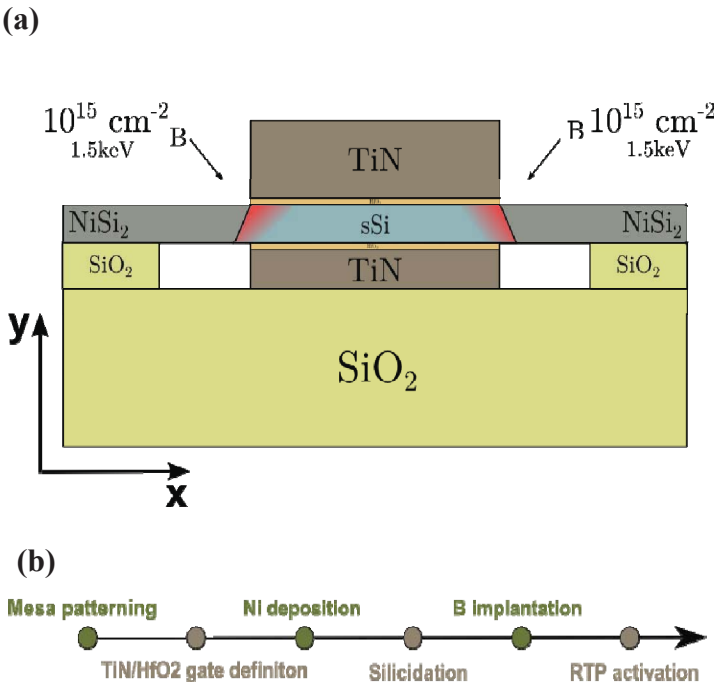
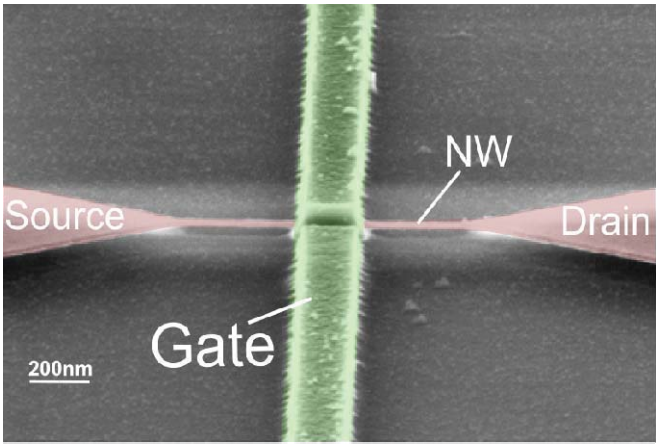



Fig.1: (a) cross section schematic of the single NW sSi SBMOSFET with $TiN/HfO_2$ – gate stack and tilted IIS-process of Boron for source and drain. (b) The process flow of the device.

**(a)**




**(b)**

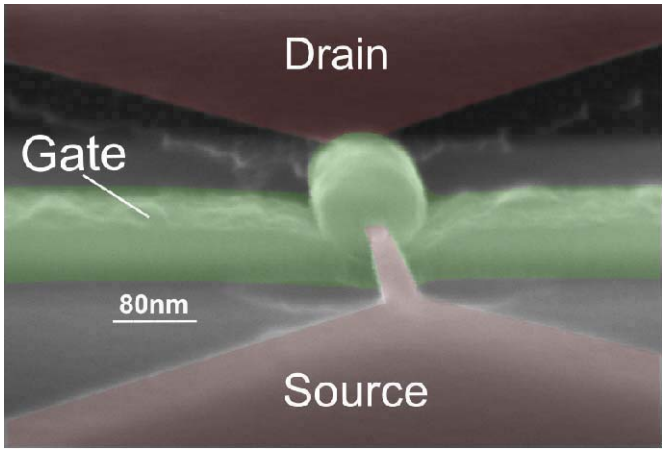



Fig.2: (a) SEM image of a single sSi NW SB MOSFET with TiN/HfO2 gate stack. The gate length is 150 nm. (b) SEM image of the device from a different view.

## II. SBMOSFET FABRICATION PROCESS

Single nanowire SB-MOSFETs were fabricated on 15nm thick biaxial tensely strained sSOI ($\varepsilon_{biax}$ = 0.8%) substrates with 145 nm BOX using electron beam lithography and dry etching technique. After mesa definition and RCA cleaning, a 3nm thick $HfO_2$ layer was grown by atomic layer deposition (ALD), followed by atomic vapor deposition (AVD®-process) of 40nm TiN. The gate was defined by E-beam lithography and etched back using dry and wet etching. 2nm Ni was deposited using sputter deposition. Epitaxial $NiSi_2$ layers at S/D areas were formed by annealing the samples at 550°C in forming gas for 30 seconds. Excessive Ni was then removed by selective wet etching. Ref.[3] shows that $NiSi_2$ formation with this method has good gate alignment with no encroachment of the silicide into the channel region. Then $B^+$ ion implantations (1e15cm$^{-2}$, 1.5keV) at titled angle of 45° and 135° were performed for both source and drain junctions as shown in Fig.1(a), followed by a low temperature anneal at 450°C for 10s in RTP in $N_2$ environment to drive out the dopants out of the silicide and make dopant pockets by dopant segregation. Fig.2 shows the SEM images of fabricated device viewed from different position. The gate is marked in green while the silicide and the NW are marked in red. It is clear that the nanowire is suspended and is completely wrapped by the high-k/MG stack.

## III. SBMOSFET CURRENT MIRROR

### *A. Circut layout*

Using the fabrication method explained in the previous section, simple current mirrors based on two connected transistors were fabricated as exhibited in Fig.3. The source contacts of both transistor M1 and M2 are directly connected through the silicide and both M1 and M2 share the same gate contact with each other using the gate fingers. The drain and gate contacts of transistor M1 are connected through an aluminum contact fabricated with a lift-off process to form the diode connected transistor M1. The Aluminum was deposited using evaporation process.

### *B. Biasing scheme*

The transistors were biased according to the biasing scheme shown in Fig.4. $V_{DD}$ was connected to the source of both transistors. To drive the diode connected transistor M1, a current input, $I_{REF}$, was applied to the drain of the transistor. $I_{REF}$ was increased step by step for each consecutive measurement. Output current $I_{out}$ was measured while sweeping the drain voltage of transistor M2.

## IV. DEVICE CHARACTERISITICS

Fig.5 shows the transfer characteristics at $V_{ds}$=0.1 V of the fabricated sSi GAA single NW SB MOSFETs with and without IIS shown by the blue and red curves, respectively. The minimum off current is shifted to positive $V_{gs}$ because the silicon channel is slightly p-doped (1e16 cm$^{-3}$) and the unadjusted workfunction of the gate. To compensate this voltage shift work function engineering would be needed. It is evident that IIS increases the drain current and improves the inverse subthreshold slope of the device from 135mV/dec to 80mV/dec, which is constant over a wide range of $I_d$ values. This is due to reduction of Schottky Barrier Height (SBH) for holes by the boron dopant segregation at $NiSi_2$/Si channel interface. The transistor shows a high $I_{on}/I_{off} > 10^6$. The ambipolar behavior in both cases is relatively small because the SBH for electrons is higher than SBH for holes for $NiSi_2$ on SOI substrate.

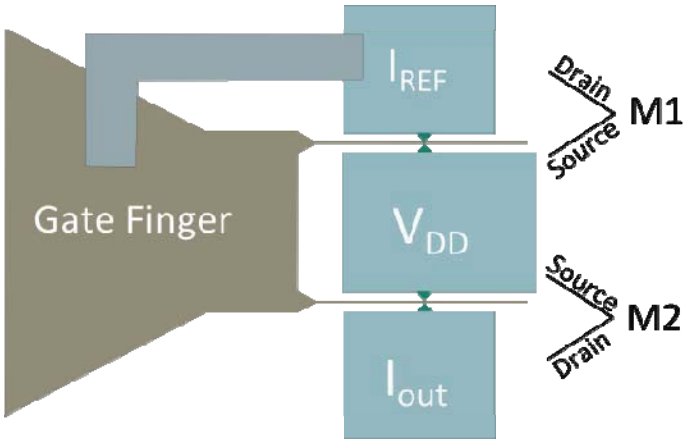



Fig.3: Circuit layout of the single sSi NW SB MOSFET current mirror. The drain and gate of M1 are connected through an Al contact.

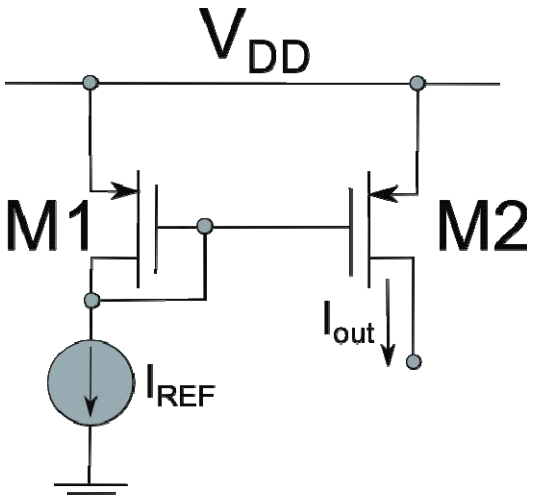



Fig.4: Biasing scheme of the p-SB MOSFET based current mirror.

The output characteristics of the current mirror is shown in Fig.6. Here Vout represents the Vds of transistor M2. Blue curves exhibit Iout and red curves correspond to $I_{REF}$ current values. As it is shown, by increasing $I_{REF}$, the output current also increases and exhibits good saturation at the respective $I_{REF}$ value. The super-linear characteristics of $I_{out}$ at small absolute $V_{out}$ indicate that the effective SB height can be further improved by optimization of the annealing process for the dopant segregation. The Mirror Ratio (MR) = $I_{out}/I_{REF}$ was calculated to be 0.99 at $I_{REF}$ = 1uA which indicates both transistors are well matched.

The mirror ratio is close to 1, because the junction between epitaxial $NiSi_2$ and the channel has high quality with low edge roughness. This means that the Schottky barrier height is highly uniform along source/drain contacts and is reproducible.

Another important figure of merit of a current mirror is the output resistance Ro. A high output resistance is essential to achieve stable output currents under different load conditions. One can represent the small signal model of a diode-connected SBMOSFET by a resistor of value $1/g_{m1}$. In this arrangement the output resistance of current mirror is the output resistance of transistor M2 (Fig.7).

It is possible to calculate $R_o$ from the output characteristics of the current mirror. Fig.8 shows a zoomed view of the output curve for $I_{REF}$ = 1uA. As shown in the figure, the inverse slope of the output curve in the saturation region is the output resistance of the current mirror. The output resistance of current mirror was calculated to be more than 100MΩ at $I_{REF}$ = 1uA. Due to high output resistance, a cascade current mirror can be replaced with simple current mirror which allows for lower supply voltage [9].

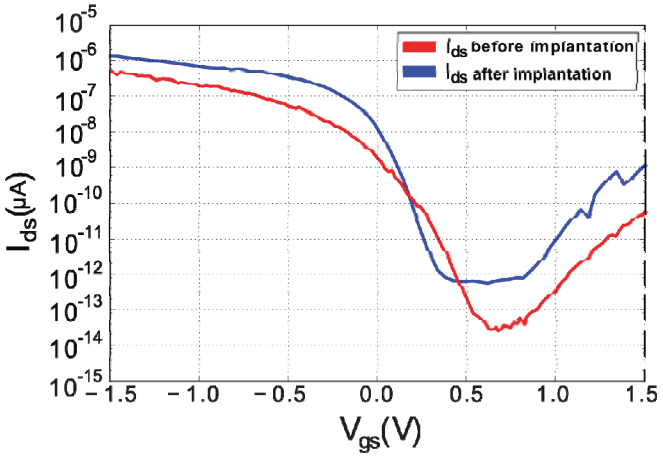



Fig.5: Transfer characteristics of a SB MOSFET before (red) and after (blue) $B^+$ implantation into silicide and annealing, showing improved performance of the device by IIS and dopant segregation.

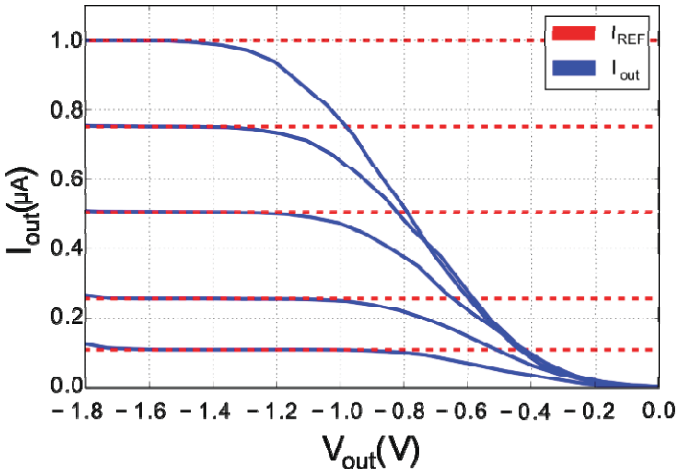



Fig.6: Output characteristics of the current mirror. The red line shows the $I_{REF}$ value. The output current exhibits good saturation at $I_{REF}$ values, indicating a very good match of both transistors.

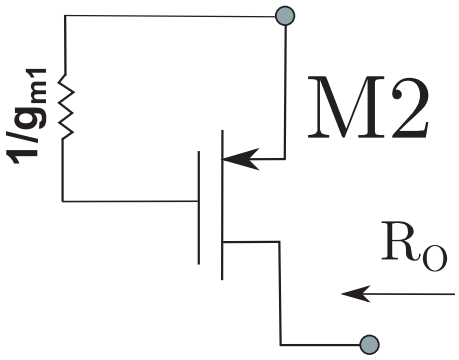



Fig.7: Equivalent circuit for output resistance of the p-SBMOSFET current mirror.

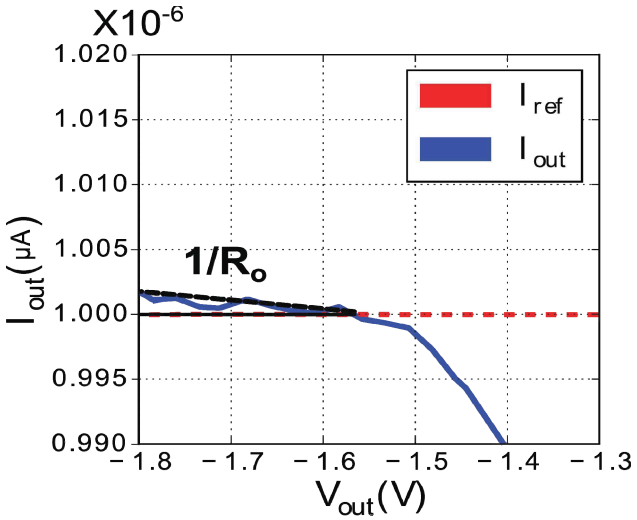



Fig.8: Zoomed view of the output characteristics in the saturation region for $I_{REF}$ = 1uA. Ro is the inverse slope in the saturation region as indicated.

## V. CONCLUSION

We have fabricated single NW sSi GAA SB MOSFETs with $B^+$ implantation into $NiSi_2$ source/drain and dopant segregation. The lowered effective SBH for holes by dopant segregation increases the on-current and improves the subthreshold swing. A simple current mirror employing two transistors exhibits a good MR of 0.99 and high output resistance of 100MΩ. These properties and low operating voltages of fabricated SB MOSFETs makes them suitable for low-power analog circuit applications

## *Acknowledgement*

This work is partially supported by the BMBF project UltraLowPow (16ES0060K) and the European project E2SWITCH.

## *References*

[1] J. M. Larson and J. P. Snyder, "Overview and status of metal S/D Schottky-barrier MOSFET technology," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1048–1058, 2006.

[2] L. Knoll, Q. T. Zhao, S. Habicht, C. Urban, B. Ghyselen, and S. Mantl, "Ultrathin Ni Silicides With Low Contact Resistance on Strained and Unstrained Silicon," *IEEE Electron Device Lett.*, vol. 31, no. 4, pp. 350–352, Apr. 2010.

[3] L. Knoll, Q. T. Zhao, R. Luptak, S. Trellenkamp, K. K. Bourdelle, and S. Mantl, "20nm Gate length Schottky MOSFETs with ultra thin NiSi/epitaxial NiSi<inf>2</inf> source/drain," in *Ulis 2011 Ultimate Integration on Silicon*, 2011, vol. 9, no. 111, pp. 1–4.

[4] Z. Qiu, Z. Zhang, M. Östling, and S. L. Zhang, "A comparative study of two different schemes to dopant segregation at NiSi/Si and PtSi/Si interfaces for Schottky barrier height lowering," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 396–403, 2008.

[5] G. Larrieu, E. Dubois, R. Valentin, N. Breil, F. Damneville, G. Dambrine, J. P. Raskin, and J. C. Pesant, "Low temperature implementation of dopant-segregated band-edge metallic S/D junctions in thin-body SOI p-MOSFETs," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, no. 1, pp. 147–150, 2007.

[6] C. Urban, M. Emam, C. Sandow, J. Knoch, Qing-Tai Zhao, J. Raskin, and S. Mantl, "Radio-Frequency Study of Dopant-Segregated n-Type SB-MOSFETs on Thin-Body SOI," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 537–539, Jun. 2010.

[7] L. Knoll, A. Schafer, S. Trellenkamp, K. K. Bourdelle1, Q. T. Zhao, and S. Mantl, "Nanowire and planar UTB SOI Schottky Barrier MOSFETs with dopant segregation," *Ulis 2012 Ultim. Integr. Silicon*, no. March 2015, pp. 45–48, 2012.

[8] G. V. Luong, S. Strangio, A. Tiedemannn, S. Lenk, S. Trellenkamp, K. K. Bourdelle, Q. T. Zhao, and S. Mantl, "Experimental demonstration of strained Si nanowire GAA n-TFETs and inverter operation with complementary TFET logic at low supply voltages," *Solid. State. Electron.*, pp. 8–15, 2015.

[9] B. Sedighi, X. S. Hu, S. Member, H. Liu, S. Member, J. J. Nahas, and M. Niemier, "Analog Circuit Design Using Tunnel-FETs," vol. 62, no. 1, pp. 1–10, 2014.

# A method for combined characterization of MOSFET threshold voltage and junction capacitance eliminating channel current effect

Daniel Tomaszewski, Grzegorz Głuszko, Jolanta Malesińska
Division of Silicon Microsystem and Nanostructure Technology
Instytut Technologii Elektronowej (ITE)
ul. Okulickiego 5E, 05-500 Piaseczno, Poland
e-mail: dtomasz@ite.waw.pl, ggluszko@ite.waw.pl, jmales@ite.waw.pl

***Abstract*—A method for an extraction of a MOSFET threshold voltage has been proposed. It is based on an analysis of the MOSFET source-bulk junction capacitance behavior along the gate-source voltage variation. A channel current effect on the threshold voltage extraction is fully eliminated. In parallel the junction capacitance and its planar and sidewall components are determined. A non-iterative method for extraction of the junction capacitance has been proposed. The proposed method operation has been demonstrated using series of MOS transistors.**

***Keywords—MOSFET, threshold voltage, junction capacitance***

## I. INTRODUCTION

MOSFET threshold voltage ($V_{th}$) models are typically based on a 1D solution of a Poisson equation in the MOSFET below the gate. In this approach the current flow is neglected. On the other hand standard threshold voltage extraction methods are based on measured I-V characteristics [1]. So an electric field effect on mobility and a voltage drop at the source and drain resistances in real devices affect $V_{th}$ extraction. Methods aimed at minimization of these effect have been proposed, e.g. in [2,3]. However they do not fully eliminate the channel current effect on $V_{th}$ extraction.

In the presented work we describe a method based on measurements of the MOSFET source-bulk (SB) junction capacitance $C_{bs}$ vs the gate-source voltage $V_{GS}$. The drain terminal remains open, so the channel current effect is eliminated.

## II. DESCRIPTION OF THE METHOD

A potential distribution in a space charge area of the SB junction below the gate is different than in the area outside the gate. Simulation results from Silvaco Atlas for a simplified p-channel structure are shown in Fig. 1. As the $V_{GS}$ voltage varies the potential distribution below the junction remains constant, whereas below the gate changes. At the accumulation below the gate it is rather insensitive to gate bias, so the $C_{bs}$ capacitance does not change with $V_{GS}$. However at the onset of strong inversion a channel is formed as an expansion of the source. It is followed by a steep increase of the $C_{bs}$ capacitance. This observation is a basis of the proposed method.

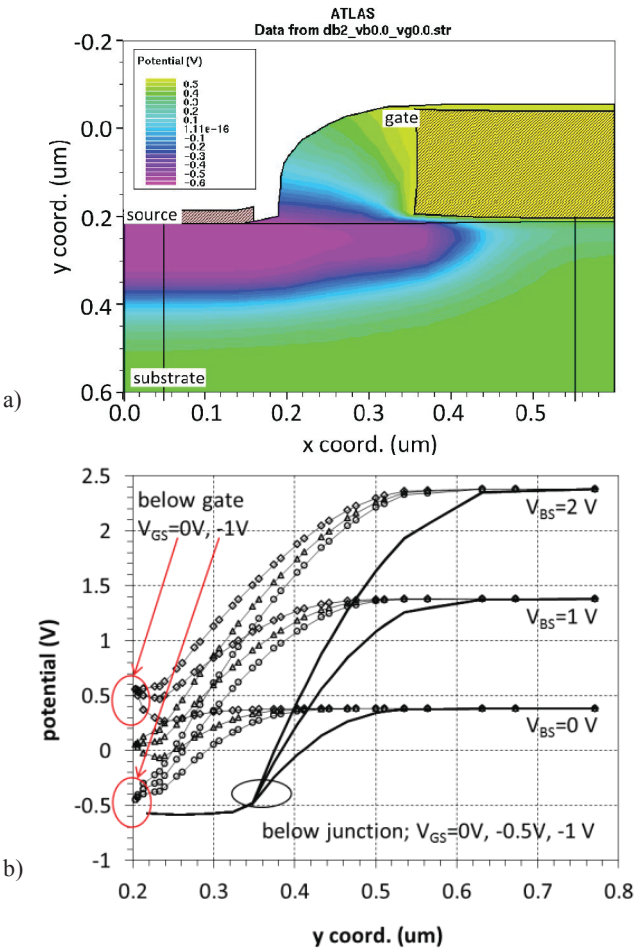



Fig. 1. a) Potential distribution in p-channel MOSFET for $V_{BS}$=$V_{GS}$=0V; b) Potential distributions along lines as in a) for $V_{BS}$=0, 1, 2V, $V_{GS}$=0, -0.5, -1V

The method consists in measurement of the $C_{bs}(V_{BS})$ characteristics for a series of $V_{GS}$ voltages. Next $C_{bs}(V_{GS})$ characteristics are constructed. At the accumulation and depletion below the gate the $C_{bs}$ capacitance should be constant irrespective to $V_{GS}$ variation. It is expected, that on the

$C_{bs}(V_{GS})$ curves there is a clearly visible transition point between the accumulation/depletion and inversion ranges.

## III. EXPERIMENTAL RESULTS

For the experimental validation of the method described in the previous section the n- and p-channel MOSFETs fabricated in a single p-well, polysilicon gate CMOS process have been used. The $C_{bs}(V_{BS})$ characteristics of a number of large size devices have been measured using a Keithley 4200-SCS parametric analyzer equipped with a 4200-CVU card. The size of the devices, in particular the size of SB junction areas is limited by the LCZ meter minimum range which is 1 pF. The $C_{bs}(V_{BS})$ characteristics of the p-channel MOSFET, W=50µm, L=50µm measured for different $V_{GS}$ voltages are shown in Fig. 2. As expected, a strong influence of the gate voltage variation is clearly visible. Enlarged bottom parts of these curves are shown in the inset. Though in a full-scale plot they appear to be constant, however if enlarged a noticeable curvature is revealed. An "envelope" of the whole family has been calculated as a mean of $C_{bs}$ capacitances measured for a series of four $V_{GS}$ voltage corresponding to the accumulation/depletion conditions below the gate ($0\ V \le V_{GS} \le -0.5\ V$). It corresponds to the $C_{bs}(V_{BS})$ characteristics of the BS junction including its edge.

Based on the $C_{bs}(V_{BS})$ curve family, $C_{bs}(V_{GS})$ characteristics with $V_{BS}$ as a parameter have been constructed. They are shown in Fig. 3. As expected, three regions may be distinguished in these curves. In the first region the $C_{bs}$ capacitance is the lowest and does not depend on the gate voltage. In this gate bias range the area below the gate is accumulated or depleted and the $C_{bs}$ capacitance is determined only by the space charge of the SB junction. If the gate voltage becomes more negative and exceeds the threshold voltage, a steep increase of the $C_{bs}$ capacitance is observed. This effect is caused by the expansion of the source region in a form of a highly conductive inversion layer. Similarly to the real source area, below the gate-induced virtual source there is also a depletion area which separates the source plate from the bottom quasi-neutral substrate. In the inset in Fig. 3 four curves

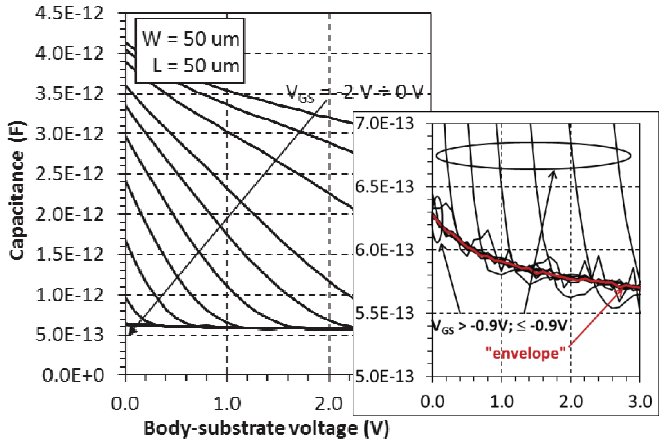



Fig. 2. $C_{bs}(V_{BS})$ characteristics for p-channel MOSFET, W=50µm, L=50µm; $V_{GS}$=-2..0 V

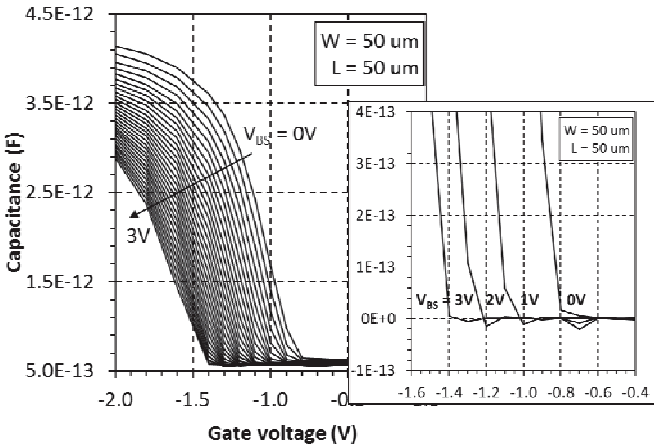



Fig. 3. $C_{bs}(V_{GS})$ characteristics for p-channel MOSFET retrieved from data in Fig.2; in the inset the "envelope" is subtracted; points of the strong inversion onset are clearly visible

are plotted after subtracting the "envelope" value taken from Fig. 2. Points of the $C_{bs}(V_{GS})$ sharp increase are clearly visible.

The $C_{bs}(V_{GS})$ characteristics allow to derive the $V_{th}(V_{BS})$ characteristics of the MOSFETs. On each $C_{bs}(V_{GS})$ curve the threshold voltage is determined as the $V_{GS}$ value, at which the $C_{bs}$ capacitance rapidly changes. The accuracy of this method is limited by the gate voltage step size. So a direct measurement of the $C_{bs}(V_{GS})$ characteristics where the gate voltage is swept while the substrate bias $V_{BS}$ is stepped is a better solution. However, in the frame of this work we have used a simpler approach involving $C_{bs}(V_{BS})$ measurements for a reasonably dense series of the $V_{GS}$ voltages. In Fig. 4a the $V_{th}(V_{BS})$ data obtained using the proposed method are set together with the $V_{th}(V_{BS})$ curves obtained using the standard current-based methods, namely a linear extrapolation of $I_D$-$V_{GS}$ characteristics at transconductance $g_m$ maximum, and a linear extrapolation of $I_D/g_m^{0.5}$-$V_{GS}$ characteristics [2]. It has been found that the proposed C-V based approach gives results very close to the standard method based on the linear extrapolation of $I_D$-$V_{GS}$ characteristics at transconductance $g_m$ maximum. This observation is illustrated in Fig. 4b. In Fig. 4c there are plots correlating directly [4] the threshold voltage values determined using the methods mentioned above. The threshold voltages for a set of substrate bias are listed in Table 1.

In Fig. 4a,c several "humps" are visible on the $V_{th}(V_{BS})$ curves corresponding to C-V based method for $V_{th}$ extraction. They are due to too coarse grid of the $V_{GS}$ voltage. This confirms a need for the mentioned above direct measurement of the $C_{bs}(V_{GS})$ characteristics with the stepped $V_{BS}$ voltage.

TABLE I. THRESHOLD VOLTAGE EXTRACTED VALUES

| $V_{BS}$ | Method | | |
|---|---|---|---|
| | $I_D$-$V_G$ | $I_D/g_m^{0.5}$-$V_G$ | $C_{bs}$-$V_G$ |
| 3.0 | -1.425 | -1.457 | -1.402 |
| 2.0 | -1.283 | -1.318 | -1.283 |
| 1.0 | -1.107 | -1.146 | -1.097 |
| 0.0 | -0.860 | -0.892 | -0.845 |

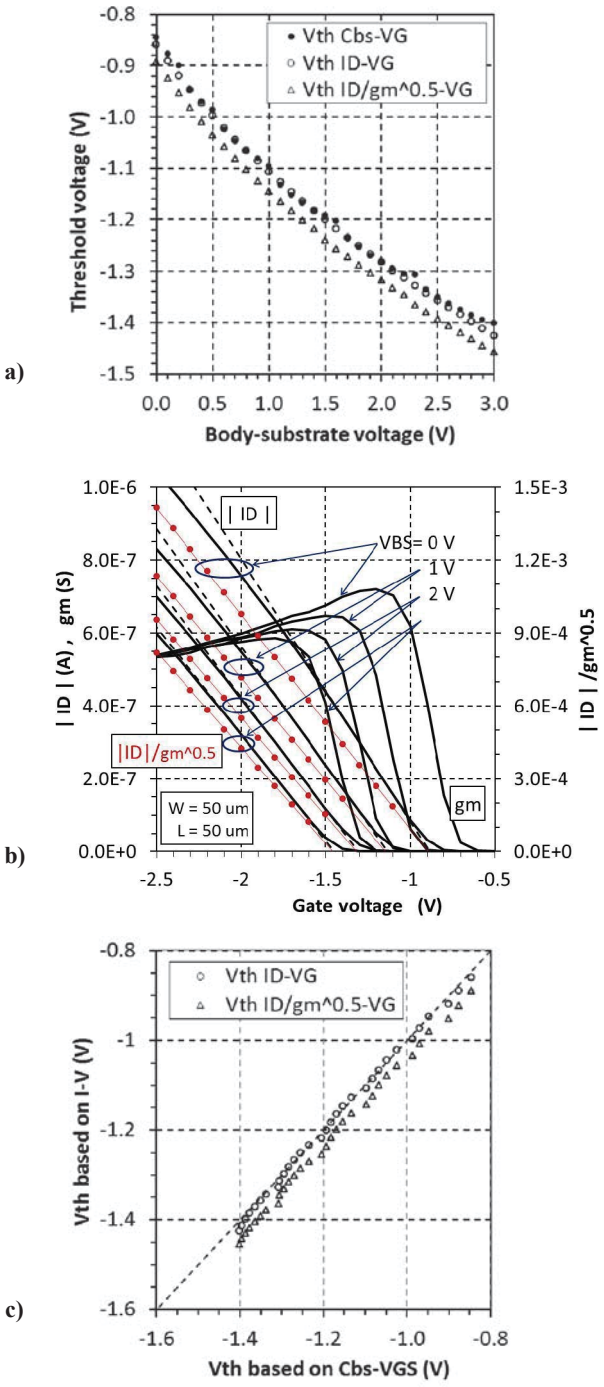



Fig. 4. Threshold voltage extracted with three methods: a) dependence on $V_{BS}$ voltage, b) extraction of Vth based on I-V characteristics, c) direct comparison between $V_{th}$ values extracted with different methods

## IV. Parameter Extraction

In the case of the long-channel enhancement-mode MOSFETs the threshold voltage $V_{th}$ is given by a well known formula (1).

$$V_{th}=V_{th,0} + t\cdot\gamma\cdot[\,(2\phi_F - t\cdot V_{BS})0.5 - (2\phi_F)^{0.5}\,] \qquad (1)$$

where $V_{th,0}$ – threshold voltage at $V_{BS}$=0 V, $\gamma$ – body factor, $2\phi_F$ – double Fermi voltage. A variable t is a switch determined by the MOSFET type, namely t=+1 for the nMOSFETs, t=-1 for the pMOSFETs. Using a method described in [5] for $V_{th}(V_{BS})$ data, parameters of $V_{th}$ in (1) may be determined with (2a) and (2b), which is subject to a linear regression between terms $V_{th}$-$V_{th,0}$ and $(dV_{th}/dV_{BS})^{-1}$.

$$V_{th,0} = V_{th}(0) \qquad (2a)$$

$$V_{th} - V_{th,0} = -0.5\cdot t\cdot\gamma^2 \Big/ \frac{d\,V_{th}}{d\,V_{BS}} - t\cdot\gamma\cdot\sqrt{2\,\phi_F} \qquad (2b)$$

The regressions for the $V_{th}(V_{BS})$ data extracted using two I-V based and $C_{bs}$-$V_{GS}$ methods are illustrated in Fig. 5. The threshold voltage parameter values have been calculated based non the fittings (Table II). The parameters $\gamma$ and $2\phi_F$ have rather low values due to the fact that the doping concentration in the substrate of the devices was rather low (order of $10^{15}$ $cm^{-3}$). Significant differences between the $\gamma$ and $2\phi_F$ values are noticeable, including those which have been extracted based on the $C_{bs}$-$V_{GS}$ data. The extraction of $\gamma$ and $2\phi_F$ based on the latter characteristics is not fully reliable because of a large spread in the $V_{th}$-$V_{th,0}$ = f [ $1/(dV_{th}/dV_{BS})$ ] data set. It is due to the mentioned above humps on the $C_{bs}$-$V_{GS}$ characteristics. So a better method for extraction of the threshold voltage based on these characteristics is needed.

TABLE II. Threshold Voltage Parameters

| Parameter | Method | | |
|---|---|---|---|
| | $I_D$-$V_G$ | $I_D/g_m^{0.5}$-$V_G$ | $C_{bs}$-$V_G$ |
| $V_{th,0}$ (V) | -0.860 | -0.892 | -0.845 |
| $\gamma$ ($V^{0.5}$) | 0.498 | 0.473 | 0.460 |
| $2\phi_F$ (V) | 0.573 | 0.443 | 0.383 |

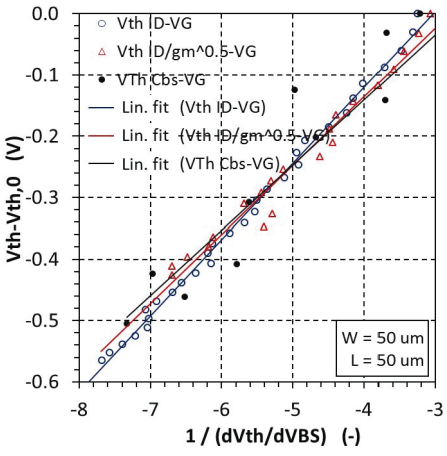



Fig. 5. Linear fits (2) corresponding to the pMOSFET $V_{th}(V_{BS})$ data extracted using two I-V and $C_{bs}$-$V_{GS}$ based methods.

The proposed method allows for analysis of the $C_{bs}$ capacitance in the MOSFETs. The red "envelope" of the $C_{bs}(V_{BS})$ characteristics family measured for different $V_{GS}$ voltages (Fig. 2) represents the total $C_{bs}$ capacitance of the MOSFET SB junction including its plane and sidewall components. Modeling of such a characteristics is based on a well known formula (3).

$$C_{bs} = C_J \cdot (1 - t \cdot V_{BS}/V_{bi})^{-MJ} \tag{3}$$

where $C_J$ is the capacitance at $V_{BS}$=0 V, $V_{bi}$ is a built-in voltage, and $M_J$ is a grading coefficient, which is 0.5 for an ideal abrupt junction and 0.33 for an ideal linearly graded junction. The $C_J$ parameter is easily determined as $C_{bs}(V_{BS}$=0 V). The remaining two parameters are typically extracted using an iterative procedure. Here we propose a non-iterative approach, which is based on (4).

$$\begin{aligned} dC_{bs} / dV_{BS} &= C_J \cdot t \cdot M_J/V_{bi} \cdot (1 - t \cdot V_{BS}/V_{bi})^{-MJ-1} \\ &= C_{bs} \cdot t \cdot M_J/V_{bi} / (1 - t \cdot V_{BS}/V_{bi}) \end{aligned} \tag{4}$$

After a simple transformation of (4) the following method (5) for the junction capacitance parameter extraction may be proposed, where (5b) is subject to a linear regression between $V_{BS}$ and $C_{bs}$ / ($dC_{bs}/dV_{BS}$) terms.

$$C_J = C_{bs}\ (0) \tag{5a}$$

$$V_{BS} = t \cdot V_{bi} - M_J \cdot C_{bs} / (\, dC_{bs}/dV_{BS}\,) \tag{5b}$$

The linear fit used for the $C_{bs}(V_{BS})$ data corresponding to the "envelope" is illustrated in Fig. 6. A rather poor quality of this fit is related to noisy small values of the measured capacitances. This makes some problems for the parameter extraction. If the iterative procedure were used it would probably fail. Our approach is not so sensitive to the data quality. The calculated parameter values are as follows: $C_J$=6.3$^{-13}$ F, $V_{bi}$=0.22 V, $M_J$=0.04. Such small valuae of $V_{bi}$, and $M_J$ are very probably related to the fact that $C_{bs}(V_{BS})$ data

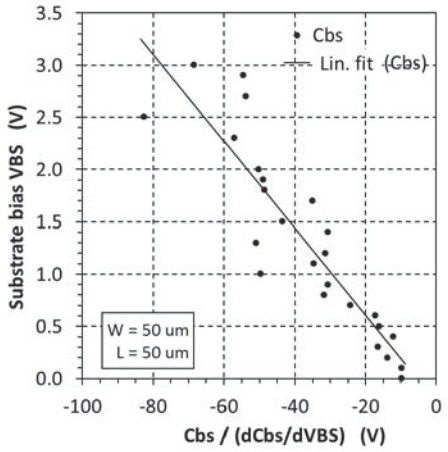



Fig. 6. Extraction of the junction capacitance parameters (5)

contain their plane and sidewall components. The sidewall capacitance is much less sensitive to $V_{BS}$ voltage, so it affects the parameter extraction. The $C_{bs}(V_{BS})$ data for MOSFETs of different channel widths may be used to solve this problem. C-V curves for two pMOSFETs are shown in Fig. 7. Based on the device layout (inset in Fig. 7) the $C_{bs}$ capacitance may be expressed by (6).

$$\begin{aligned} C_{bs} &= W \cdot [\, L_S \cdot C_{bs,A}(V_{BS}) + \\ &+ C_{bs,SW}(V_{BS}) + C_{bs,G}(V_{GS}, V_{BS})\, ] + \quad 2 \cdot L_S \cdot C_{bs,SW}(V_{BS}) \end{aligned} \tag{6}$$

By using (6) it is theoretically possible to separate the bulk and sidewall components $C_{bs,A}$, $C_{bs,SW}$ of the $C_{bs}(V_{BS})$ characteristics. This method is currently under investigation.

## V. Summary

The presented method allows for parallel extraction of the MOSFET threshold voltage and junction capacitance parameters. The threshold voltage extraction procedure requires a fine sweep of the gate voltage during the capacitance measurement. New non-iterative methods for the threshold voltage and capacitance models have been also proposed.

## References

[1] D. Schroder, "Semiconductor material and device characterization", 3rd Ed., Wiley Interscience, 2006

[2] G. Ghibaudo, "New method for the extraction of mosfet parameters", Electronics Letters, 28th April 1988, vol. 24 no. 9, pp.543-545

[3] D. Flandre, V. Kilchytska, T. Rudenko, "gm/Id method for threshold voltage extraction applicable in advanced MOSFETs with nonlinear behavior above threshold", IEEE El. Dev. Letters, vol. 31, no. 9, pp. 930-932, Sept. 2010

[4] D. Tomaszewski, G. Głuszko, M. Zaborowski, J. Malesinska, K. Kucharski, "A simple multi-purpose method for compact model evaluation", Proc. 21st Int. Conf. Mixed Design of Integrated Circuits & Systems (MIXDES), 19-21, 2014, Lublin, Poland, pp. 74-78

[5] D. Tomaszewski, J. Malesińska, G. Głuszko, "Simple methods of threshold voltage parameter extraction for MOSFET models", Proc. 22nd Int. Conf. Mixed Design of Integrated Circuits & Systems (MIXDES), June 25-27, 2015, Torun, Poland, pp.222 – 226

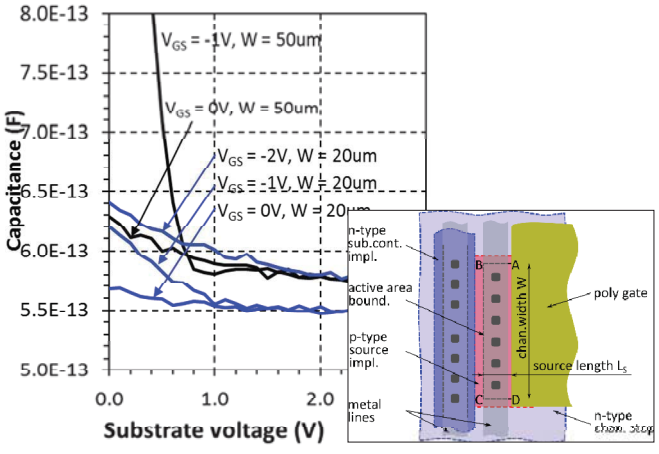



Fig. 7. $C_{bs}(V_{GS})$ characteristics for p-channel MOSFETs of different widths

# Gated SiGe PIN Diodes Exposed to Visible Light Spectrum and Heavy-Ion Radiation

R. T. Bühler, C. D. Novo, M. A. G. Silveira, R. Giacomini
Department of Electrical Engineering
Centro Universitário da FEI
São Bernardo do Campo, Brazil
buhler@fei.edu.br

***Abstract* — This paper studies gated PIN diodes designed at Centro Universitário da FEI and fabricated at Global Foundries in the GF0.13 technology, using SiGe substrate and four gate setups. The analysis is made through experimental measurements and numerical simulations of PIN diodes in dark condition, illuminated with visible light or exposed to heavy-ion radiation. Particle beam radiation present in hazard environments may cause circuit malfunctions due to interference in the device response. This paper conducts a brief, but depth study of how these variables impact the PIN diode performance, important to space and sensor applications.**

***Keywords* — *PIN diode; Visible Light; Heavy-Ion; Numerical Simulation***

## I. Introduction

Several dimensional variations in the PIN diode structure or differences in SiGe alloy can occur as result of differences in fabrication process steps with direct impact on device response. However, environmental variables – such as exposition to visible light – and hazards – such as heavy-ion radiation – also interfere in the device response, causing circuit malfunctions if their behavior is not fully understood in order to be correctly predicted with success. An experimental setup to verify radiation damages in electronic structures is very complex and it is not always possible to identify the damaging mechanisms that occurs. For that, the numerical simulations used in this work can return important information on how the studied device behave when exposed to light or radiation.

## II. Experimental Gated PIN Diodes

The experimental cascades of gated PIN devices are fabricated by Global Foundries in the GF0.13 technology [1], using layout developed at Centro Universitário da FEI, experimentally characterized and also numerically simulated through Sentaurus Device TCAD Simulator [2]. Grown on top of the silicon standard bulk substrate is the active SiGe layer with doping level P- of $10^{15}$ $cm^{-3}$ and peak acceptor doping concentration of $2.3549x10^{17}$ $cm^{-3}$ near interface. Anode P+ and cathode N+ doping regions are both $5x10^{19}$ $cm^{-3}$ and 0.1 µm depth. The intrinsic region is 11 µm long, with gate oxide dielectric EOT of 3.2 nm and a thick silicon oxide layer covering the device. Four devices are measured, each containing different gate length and position. One PIN diode with full gate of $L_g$ = 11 µm and three PIN diodes with partial gate of $L_g$ = 6 µm placed in three positions on top of the intrinsic region: left, center and right. Fig. 1 shows the schematic representation of the experimental bulk PIN diode with the p-type SiGe region in the full gate configuration.

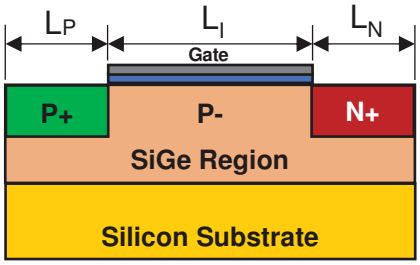



Fig. 1. Bulk PIN diode with p-type substrate and full gate.

The simulation's initial mobility, recombination and electric field models for Si and Ge were adjusted based on experimental measurements.

## III. Dark and Illuminated Experimental Devices

The electrical characterization was conducted using the Keithley 4200 in both dark and illuminated conditions, with the visible light spectrum (from 430 nm to 770 nm) used for the illuminated situation. Fig. 2 to Fig. 5 present the absolute cathode, anode, gate and bulk (substrate) currents in dark and illuminated conditions as a function of the anode ramp voltage Van from -1 V to +1 V, for the full, left, center and right gate devices in three gate $V_g$ biases: -0.5 V, 0 V and +0.5 V, with cathode and bulk set to 0 V.

The light incidence increased the cathode $I_{cat}$ and gate $I_g$ current in several orders of magnitude with reverse bias applied due to photogeneration process and virtually no $I_{an}$ or $I_{bulk}$ variance, as anticipated. The bulk current falls in the expected level to the bias adopted in this work. Larger increase were noted for smaller gate lengths, which have wider windows available for light incidence, resulting in higher generated photocurrent [3]. For the full gate with $V_{an} < -0.5$ V, an up to four-decade rise in the anode current $I_{an}$ and $I_{cat}$ occurs for $V_g$ = +0.5 V. Left and center gates presented similar results, with right gate having excessively high $I_g$, rivaling to $I_{an}$ and $I_{cat}$ and almost no dependence with light incidence.

This work is supported by FINEP, CNPq, CAPES and MOSIS.

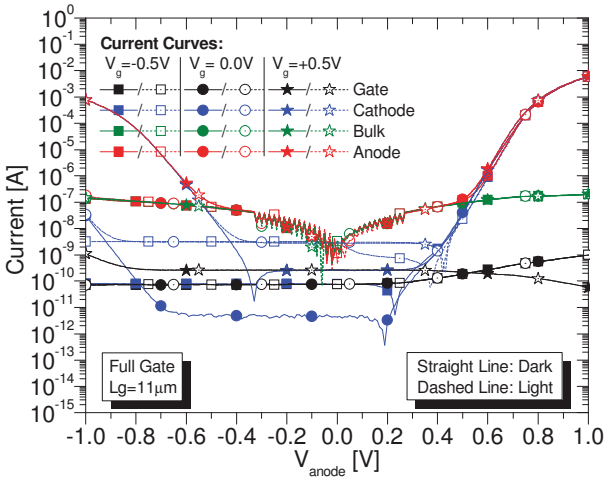



Fig. 2. Electrical current as a function of anode ramp for full gated PIN diodes.

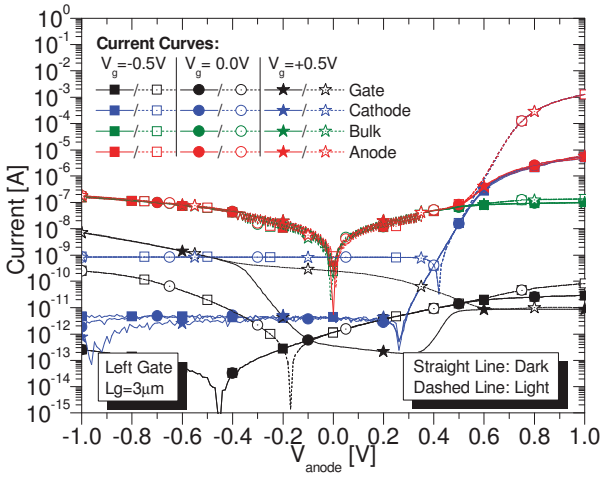



Fig. 3. Electrical current as a function of anode ramp for left gated PIN diodes.

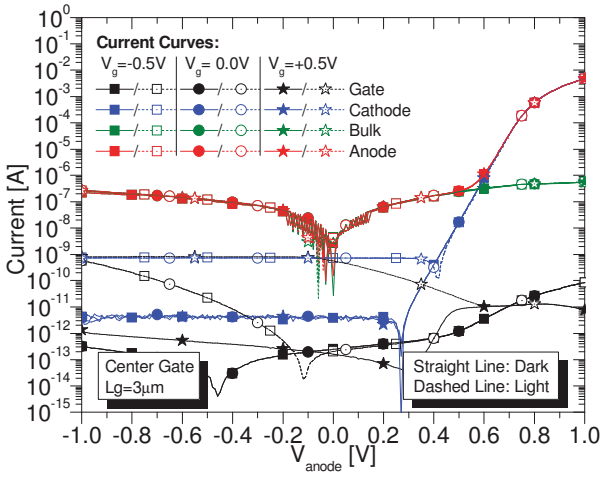



Fig. 4. Electrical current as a function of anode ramp for center gated PIN diodes.

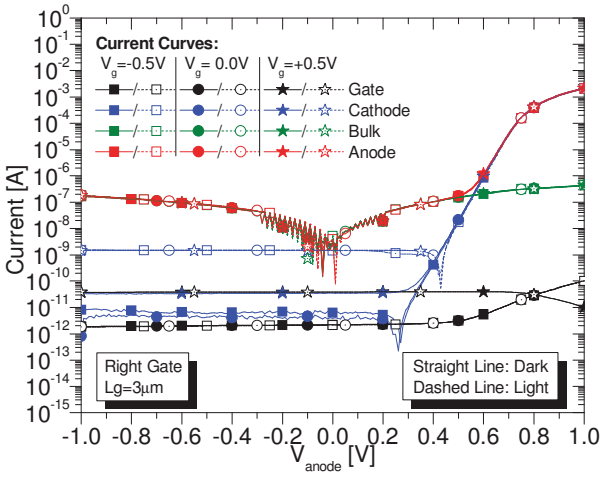



Fig. 5. Electrical current as a function of anode ramp for right gated PIN diodes.

## IV. Process Variation Simulations

Numerical TCAD simulation models were compared and adjusted with experimental data, as presented in Fig. 6.

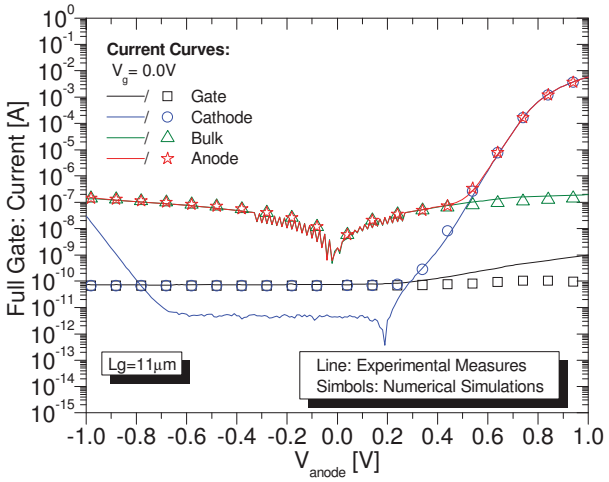



Fig. 6. Measured and numerically simulated currents as a function of $V_{anode}$ for full gated PIN.

After simulation validations, a batch of simulations were performed introducing process anomalies that replicate possible problems during fabrication process. Variation in the $Si_{1-x}Ge_x$ alloy concentrations during its epitaxial growth changes the height of barrier between semiconductor and oxide, resulting in displacement of direct bias voltage start in Ian, with possible compromising of correct operation mode of PIN diode, presented in Fig. 7 (a), changing the Ge proportion from 10 % to 30 %, causing the $I_{an}$ shift to lower $V_{an}$ value. The anode/cathode junction depth variation from 0.1 µm to 0.01 µm shifts the $I_{an}$ direct bias to lower $V_{an}$ and reduces the $I_{an}$ peak value. The variation from 0.1 µm to 0.5 µm shifts the $I_{an}$ in the opposite trend, as seen in Fig. 7 (b).

ISBN 978-1-4673-8608-1

IEEE Catalog number CFP1649D-USB

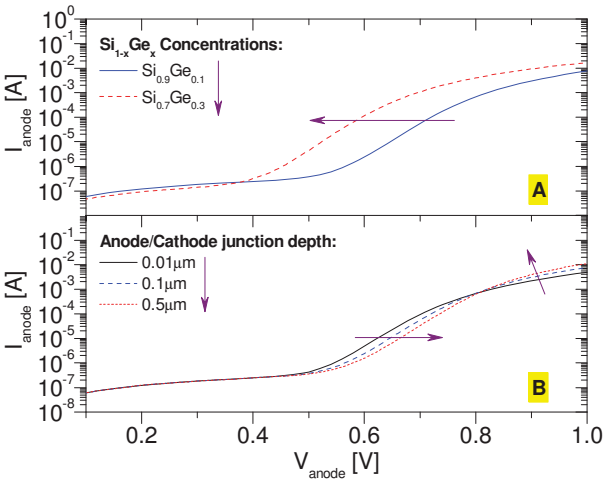
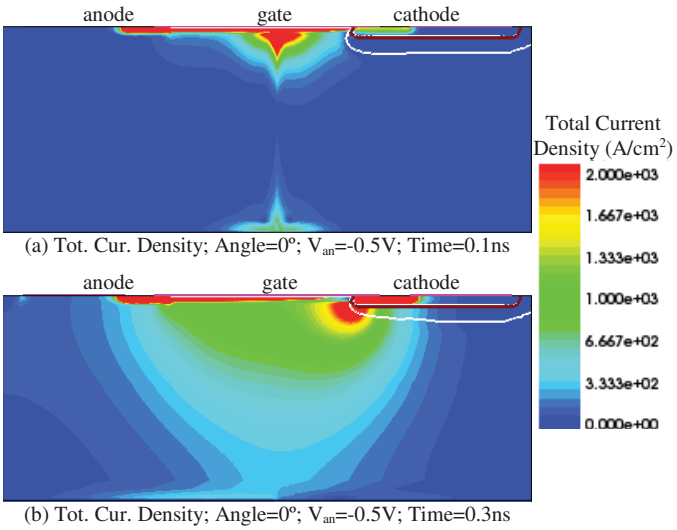



Fig. 7. Variations in (a) $Si_{1-x}Ge_x$ concentration and (b) anode/cathode junction depth.

## V. Heavy-Ion Radiation Simulations

The study of heavy-ion radiation through numerical simulations were made, applying a LET of 10 MeV.cm$^2$/mg [4] with radius of 50 nm [5] and $V_{an}$ of -0.5 V and +0.5 V. The particle incidence takes place at 0.1 ns and the $I_{cat}$ peak occurs at ~0.3 ns and latter decays. The ionizing particle creates electron-hole pairs inside the active region and part of them recombines, while the remaining charge drifts, interfering on the electrical behavior of the device. Fig. 8 presents the total current density for the incidence angle of 0º at 0.1 ns and at 0.3 ns, showing that at first a thin layer of current is formed near gate interface. Next, most of the current generated is captured by the cathode and the peak in $I_{cat}$ occurs (Fig. 8b).

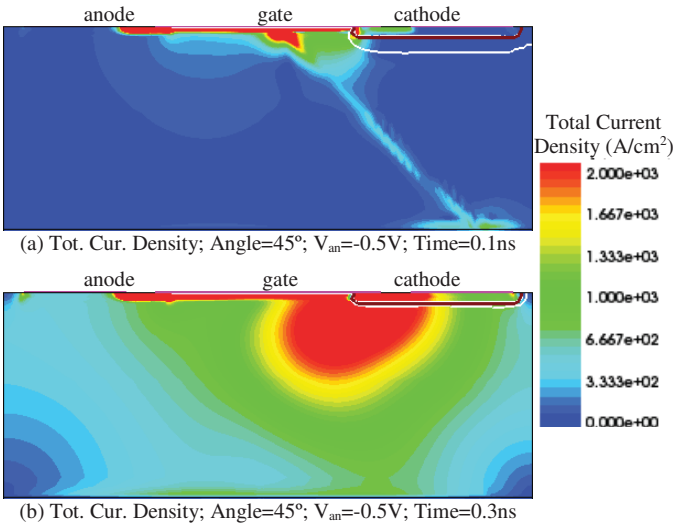



(a) Tot. Cur. Density; Angle=0º; $V_{an}$=-0.5V; Time=0.1ns

(b) Tot. Cur. Density; Angle=0º; $V_{an}$=-0.5V; Time=0.3ns

Fig. 8. Total current density for the incidence angle of 0º at 0.1 ns and at 0.3 ns with $V_{an}$ = -0.5 V.

In the incidence angle of 45º, the total current density is presented in Fig. 9 at 0.1 ns and at 0.3 ns, with rise in the total current density with the change in incidence angle and thicker current layer near gate interface.




(a) Tot. Cur. Density; Angle=45º; $V_{an}$=-0.5V; Time=0.1ns

(b) Tot. Cur. Density; Angle=45º; $V_{an}$=-0.5V; Time=0.3ns

Fig. 9. Total current density for the incidence angle of 45º at 0.1 ns and at 0.3 ns with $V_{an}$ = -0.5 V.

With the new incidence angle, the generated electron-hole pairs are now closer to the depletion region from cathode than for 0º angle and more susceptible to its electrostatic potential, rising almost two orders of magnitude in total current.

The simulated current captured by the cathode as a function of the time with the anode biased in -0.5 V and +0.5 V, result of the incidence of the heavy-ion beam, is presented in Fig. 10 for both incidence angles.

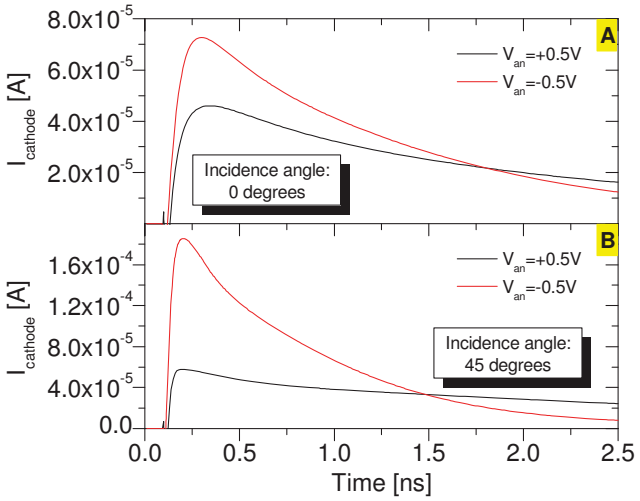



Fig. 10. Simulated cathode current as a function of time for incidence angle of 0º and 45º, with anode bias of -0.5 V and 0.5 V.

The simulation results presented in Fig. 10 shows that a 36.7 % smaller $I_{cat}$ peak with the anode polarized in +0.5 V than with it in -0.5 V in the perpendicular incidence angle, as less electron-hole pairs generated by the heavy-ion beam are captured and a 68.8 % smaller $I_{cat}$ peak with the 45º incidence angle, changing $V_{an}$ from -0.5 V to +0.5 V. The change in the incidence angle from 0º to 45º increases the cathode current peak in 155 % with $V_{an}$ = -0.5 V and 26 % with $V_{an}$ = +0.5 V.

ISBN 978-1-4673-8608-1

IEEE Catalog number CFP1649D-USB

## VI. Conclusions

Multiple PIN diode structures with gate placed in different positions were measured and the structure with gate placed in the right side of the intrinsic region, next to the cathode region, returned as the less favorable situation, with gate leakage current levels that equals or surpasses the anode or cathode current. The center gate diode returned as a promising candidate for photodetection with gate bias of -0.5 V or 0.0 V, combining the larger cathode current sensitivity to visible light with the lowest gate leakage current. Calibrated numerical simulation models allowed to predict possible source of problems from fabrication process that can result in the shift of direct bias voltage start and current overshoots following heavy-ion radiation in different angles. The gated PIN diode developed at Centro Universitário da FEI shows promising results as photodetector and with room to be implemented as a SEE radiation sensor in the near future.

## References

[1] MOSIS Integrated Circuit Fabrication Service, "Multi Project Wafer," [Online]. Available: http://www.mosis.com.

[2] Synopsys Inc, Synopsys TCAD Device User Guide, 2015.

[3] D. Renker and E. Lorenz, "Advances in solid state photon detectors," *Journal of Instrumentation,* vol. 4, April 2009.

[4] E. L. Petersen and et al, "Rate Prediction for Single Event Effects - a Critique," *IEEE Transaction On Nuclear Science,* vol. 39, pp. 1577-1599, December 1992.

[5] M. Murat, Y. Soreq NRC, A. Akkerman and J. Barak, "Electron and Ion Tracks in Silicon: Spatial and Temporal Evolution," *IEEE Transactions on Nuclear Science,* vol. 55, no. 6, pp. 3046-3054, 2008.

# Recrystallization and oxidation - competing processes during PECVD ultrathin silicon layer high temperature annealing

Romuald B. Beck and Kamil Ber
Institute of Microelectronics and Optoelectronics
Warsaw University of Technology
Koszykowa 75, Warsaw, Poland
r.beck@imio.pw.edu.pl

***Abstract*—In this work we have studied relations between three competing effects that take place during high temperature annealing of PECVD ultrathin silicon layer, namely: amorphous silicon recrystallization, amorphous silicon oxidation and oxidation of just received crystalline silicon in the first few minutes of this process. Understanding very complex relations between these kinetics is essential to allow for conscious manipulating of annealing and/or oxidation parameters in order to achieve different results, depending on the application in mind. The presented below results are, to our knowledge, the first attempt to address these issues.**

***Keywords—PECVD silicon; ultrathin silicon films; nanodots; silicon recrystallization; thermal oxidation.***

## I. Introduction

Depending on application, different requirements on physical structure and properties of silicon ultrathin layer in double oxide barrier structure can be given. The most intriguing case is possibility of obtaining silicon nano-crystals (nanodots) in the dielectric (oxide) matrix, which can be achieved by very careful recrystallization and oxidation processes [e.g. 1-7]. As both of these processes require high temperature, they can take place at the same time, simultaneously, providing appropriate conditions are satisfied. The main difference between the conditions needed for them is presence of oxygen which obviously is required for oxidation process. It has to be realized that oxygen free conditions are very difficult to achieve. Hence, even in neutral gas annealing case this process can be expected. This work is supposed to provide grounds for practical use of annealing and/or oxidation of PECVD ultrathin silicon layers to fabricate different nanoelectronic and nanophotonic devices.

## II. Experimental

### A. Sample preparation and technology

In the experiment, Si (100) 5-9 Ωcm boron doped wafers were used as substrates. Atomic flat conditions of silicon wafer surface were ensured by sacrificial oxidation followed by selective oxide etch-off. Then, ultrathin layer silicon PECVD deposition was performed. Optimum conditions of this process were determined in previous works (e.g. [8, 9]). Basing on the previous results [2] we have narrowed the temperature range to between 700°C and 1000°C and limited significantly annealing time to maximum 5 minutes only.

For the PECVD processing, Oxford PlasmaTechnology 80+ system was used. Deposition of a-Si layers were performed using $SiH_4$ (2%):He. In order to reduce the deposition kinetics, argon was used for farther dilution of reaction gas in the reaction chamber. High temperature annealing was performed in typical semiconductor high temperature furnace in quartz tube. Argon of 5N (99.999%) purity was used for this purpose.

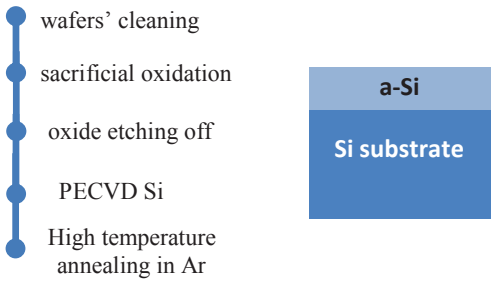



***Fig. 1** Studied structure and its formation process flow*

### B. Characterization of the obtained structures and results of annealing

The results of structures manufacturing was then examined by spectroscopic ellipsometry study (UVISEL-NIR by Jobin-Yvon). This method has proved already before [e.g. 2, 3, 9, 10] to be very sensitive and reliable, while fast and non-destructive, capable not only of evaluation of individual layer thickness in this multilayer structure, but, providing it is used carefully, allowing to obtain also information on the composition of the measured layers. Achieved results of fitting optical models to measured ellipsometric data within

In few individual cases, the results were also farther verified by HR-TEM observations. They did not, however, serve for collecting quantitative data on content of crystalline

This work was funded via National Grants by National Science Centre – DEC-2011/03/B/ST702595 (UMO-2011/03/B/ST7/02595).

phase, keeping in mind that smaller than 3 nm nanocrystals cannot be successfully observed in TEM (as discussed also in [2]).

## III. Results and Analysis

In high temperatures as-deposited Si can undergo recrystallization. During the same process presence of oxygen inevitably leads to silicon oxidation process. Obtained results prove that this effect cannot be ignored. This, in turn, complicates behavior of the studied system during annealing process. Consequently, amorphous silicon phase (a-Si) can either be subject of recrystallization or to oxidation (oxidation#1). It has to be realized that silicon nanocrystals (c-Si) are also prone to oxidation. Thus, this effect also has to be taken into consideration (oxidation#2). In order to understand the experimentally obtained results of annealing of structure of interest, we have to study kinetics of all three processes potentially involved shown schematically in Fig. 2.

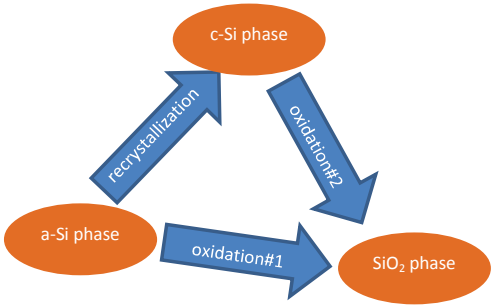



***Fig. 2*** *Schema of effects competing during high temperature processes for PECVD silicon ultrathin layer containing structures.*

The experiments were performed on structures with original thickness of as-deposited silicon layer thickness equal to 53 Å.

According to spectroscopic ellipsometry results (confirmed by HR-TEM), the as-deposited PECVD Si layer contains amorphous silicon phase (a-Si), as well as (limited fraction) nanocrystalline silicon phase (c-Si) and, interestingly – also - silicon oxide phase ($SiO_2$). In order to represent potential oxidation of top surface of ultrathin Si layer during annealing - (result of oxidation#1 or #2), additional $SiO_2$ layer was included in the optical model analysis (see Fig. 2). It is important that in all this study, ellipsometric measurements were fitted to these models with RMS<0.1 for the whole spectrum of measured wave lengths and the measurements were performed in multiple locations on the samples to verify for non-uniform distribution. Thus, we have all the reasons to consider the obtained results reliable and accurate (within the limits of the method).

The exemplary results shown in Figs.3-5 point out that in the studied annealing conditions we can observe competition of all of the expected effects.

### A. Silicon oxdation

Despite using 5N purity argon few sources of oxygen in the annealing system can be named. These are:

- natural silicon oxide layer located between the silicon monocrystalline substrate and PECVD Si;
- water vapor adsorbed on sample surface before their loading into high temperature furnace;
- diffusion through the wall of quartz tube in the high temperature furnace used for annealing, (which can be fully prevented only by double wall quartz tube system and strongly temperature dependent).

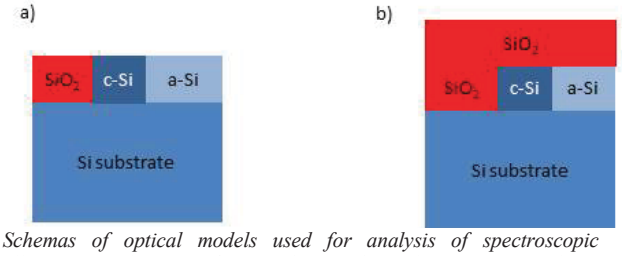



***Fig. 2*** *Schemas of optical models used for analysis of spectroscopic ellipsometry data: a) for as deposited single PECVD Si layer parameters determination, b) for evaluation of structure properties after annealing process.*

Hence, in our study, we have to take into consideration all options shown schematically in Fig. 2.

### B. Silicon recrystllization

In the former experiments, we have experimentally verified wide range of annealing temperatures and times. - temperatures from 350°C up to 1100°C and times from few minutes to almost half an hour. The obtained results have already been published in [2]. Basing on these results we have narrowed the temperature range to between 700°C and 1000°C and limited annealing time to 5 minutes only. Recrystallization effects can be observed by changes of a-Si to c-Si ratio in the PECVD Si ultrathin layer.

### C. Discussion on temperature dependencies

As can be seen in Fig. 4a the lowest annealing temperature – 700°C is too low to get recrystallization effects within the PECVD Si film. This is in agreement with results of studies presented before for various methods of layers deposition (e.g. [11]). On the contrary, during first minute - the originally observed crystalline phase of this layer (c-Si) disappears almost completely. Interestingly, the silicon oxide phase within the PECVD Si layer remains almost constant during annealing, while oxide on top of the structure grows. The oxide growth is slow and tends to saturate for annealing times longer than 3 minutes.

For 800°C, we still can see, the initial period (first minute) during which c-Si disappears (see Fig. 4b). In this case, however, from this moment noticeable recrystallization occurs.

Recrystallization process behaves differently for 900°C. We no more observe amorphization of originally observed c-Si phase during the first minute of this high temperature process. Instead, we can see, that in this temperature PECVD Si get practically completely recrystallized during this first minute. As regards oxide formation oxide thickness tends to saturate despite the fact that c-Si is still available for oxidation. This could potentially mean that there is not enough oxygen in the system to continue oxidation. The oxide growth is higher than in 800°C which is in agreement with oxidation kinetics theory.

In 1000°C (see Fig. 4c) during 1 minute all a-Si is gone. Due to high rate of oxidation, also most of c-Si is also oxidized. After 2 minutes of annealing, practically we can observe only slow but continuous growth of oxide. As we have all Si PECVD is already consumed it is believed that we observe oxidation of Si substrate then.

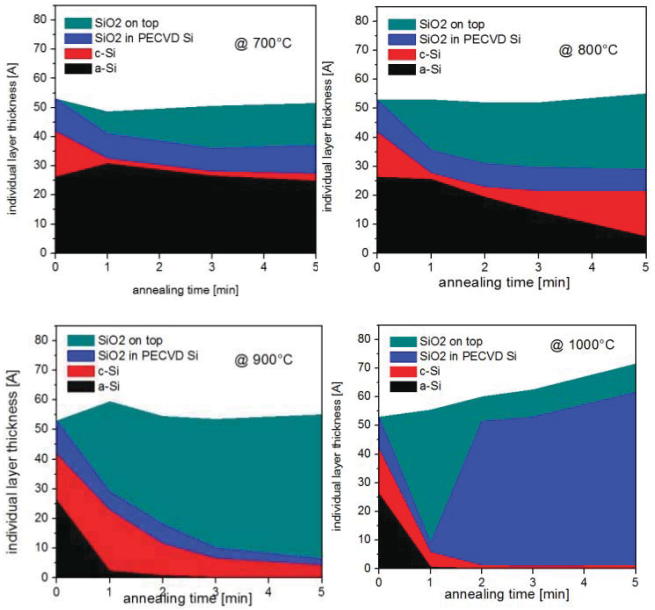



***Fig. 4*** *Individual layers' and phases' reaction to annealing in pure argon in different temperature of PECVD Si layer. PECVD Si layer consists of a-Si, c-Si and SiO2 in PECVD Si phases. SiO2 on top is determined as separate layer.*

In the Fig. 5 the oxide growth is presented for all studied annealing temperatures. For this purpose "SiO2 on top" has been added to "SiO2 in PECVD Si". Although obtained relation resembles classical oxidation kinetics temperature dependence. More careful analysis is needed, but temperature dependence in our study is certainly smaller than that for unlimited oxidant case. On the other hand, within such short oxidation time (< 5 min) no saturation would be expected for temperatures higher than 900°C [12]. There could be two potential reasons for the latter observation, namely lack of free oxygen for farther oxidation or deficiency of silicon. Regarding the latter case – one has to remember that in our study PECVD Si film is deposited directly on top of monocrystalline silicon substrate. Thus, oxidation could potentially continue by consuming monocrystalline silicon substrate. If it does not – which is the case - the potential reason for oxide growth saturation is rather deficiency of oxidant.

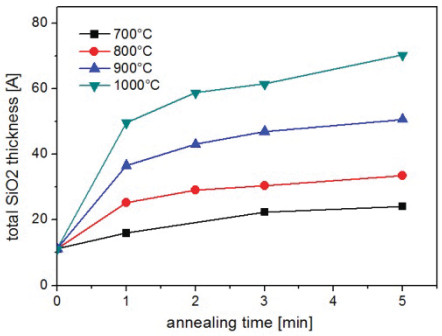



***Fig. 5*** *Total oxide thickness ("SiO2 on top" + "SiO2 within PECVD Si") changes during high temperature annealing.*

Consequently, we have to realize that oxidation behavior may vary depending on available in the system sources of oxidant species. Hence, for example, introduction of oxide layer between substrate and PECVD Si film can change this picture. Moreover, the influence of this oxide layer can differ depending on the stoichiometry of the layer or its thermal stability. Consequently, silicon oxide layer with deficiency of silicon in it could be considered as potential additional source of oxygen to PECVD Si film oxidation, while one with deficiency of oxygen – not. Similarly, unstable in high temperatures hafnium oxide could be also considered as potential source of oxygen for this reaction in ultrathin silicon films.

In Fig. 6 we presented behavior of total free silicon phase (a-Si + c-Si) in the studied structure vs annealing time and temperature. From this figure it becomes clear that for 1000°C annealing the deposited silicon PECVD layer gets completely practically consumed in very short time, i.e. in 2 minutes. Hence, it is reasonable to assume that oxidation observed since then is most probably already consuming monocrystalline silicon substrate.

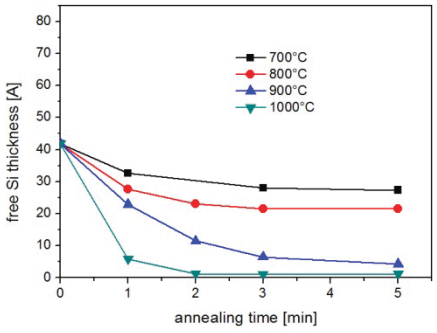



***Fig. 6*** *Total free silicon (a-Si + c-Si) changes during high temperature annealing.*

## IV. Conclusions

From the experiments performed within the framework of this study it becomes evident, that:

- regarding the recrystallization issues:
  - as a result of recrystallization during high temperature annealing, the silicon layer structure is transformed into the polycrystalline form, i.e. it consists of nanocrystals of sizes comparable to the overall final silicon layer thickness;
  - although in 700°C is temperature high enough to decompose nanocrystals that are present in as-deposited silicon layer, this temperature is too low to achieve later its recrystallization in the examined timeframe;
  - from 800°C on, decomposition of initial nanocrystals after annealing as short as 1 minute is followed by recrystallization which saturates after affecting majority of the silicon layers volume (regardless its initial thickness);
  - from 900°C on, however, we observe almost complete recrystallization of amorphous silicon layer in time as short as 1 minute;
- regarding the oxidation issues:
  - oxidation takes place during high temperature annealing although it is performed in the neutral atmosphere of pure argon, which indicates that oxygen needed for this process is supplied from some other sources (natural silicon oxides or some other external sources);
  - for 700°C oxidation rate is very low and oxide growth saturates prior to consumption even very thin amorphous silicon layer;
  - for 800°C oxide growth also saturates after 2 minutes only, despite availability of free silicon;
  - for 900°C oxidation saturates after consumption of certain thickness of silicon layer;
  - for 1000°C oxidation consumes practically completely silicon layer of initially and farther oxidation takes place at the expense of monocrystalline silicon substrate;

The conclusions described above show that for temperatures between 700°C and 900°C and annealing times between 1 minute and 5 minutes there exists a significant chance of finding a technological window allowing to promote either recrystallization or oxidation depending on the requirements of the technology of different structures or devices.

It also seems justified to conclude that PECVD Si ultrathin layers manufactured for the purpose of this study exhibit much smaller internal strain than the ones fabricated by magnetron sputtering method. This results in turn in lower crystallization temperature favoring this process vs oxidation.

## References


[1] K. Ber and R.B. Beck, “Analysis of competing processes of oxidation and recrystallization of amorphous silicon layers inn double dielectric barrier ultra-thin structures”, presented at 18th Workshop in Microelectronics - WODIM 2014 in Cork, 9-11 June 2014;

[2] S. Hazra, I. Sakata, M. Yamanaka, E. Suzuki, “Stress as governing parameter to control the crystallization of amorphous silicon films by thermal annealing”, App.Phys.Lett. vol. 80 (2002) pp. 4115-7;

[3] S. Charvet, et al., “Spectroscopic ellipsometry analysis of sputtered Si/SiO2 nanostructures”, J.Appl.Phys.vol. 85 (1999) pp. 4032-9;

[4] D.J. Lockwood, G.F. Grom, L. Tsybeskov, P.M. Fauchet, H.J. Labboe, J.P. McCarrey, B. White Jr., “Self-organization and ordering in nanocrystalline Si=SiO2 superlattices”, Physica E **11** (2001) pp. 99-103;

[5] M. Y. Chan and P. S. Lee, “Fabrication of Silicon Nanocrystals and its Room Temperature Luminescence Effects”, International Journal of Nanoscience vol. 5, Nos. 4 & 5 (2006) pp. 565-570;

[6] L. Tsybeskov, et al., “Nanocrystalline silicon superlattices: building blocks for quantum devices”, Material Science and Engineering B 69-70 (2000) pp. 303-8;

[7] M. Zacharias and P. Streitenberger, “Crystallization of amorphous superlattices in the limit of ultrathin films with oxide interfaces”, Physical Review B 62 (2000) pp. 8391-6;

[8] R. Mroczynski and R. B. Beck, “Application of plasma enhanced chemical vapor deposition silicon oxynitride layers in nonvolatile semiconductor memory devices”, Journal of Vacuum Science & Technology B **27** (2009) pp. 494-497;

[9] K. Ber and R.B. Beck, “Formation of ultrathin silicon layers by PECVD and their modification for nanoelectronic and nanophotonic applications”, Electron Technology Conference 2013 Proc. of SPIE vol. 8902 (2013) pp.1-7;

[10] A.H. Jayatissa, et al., ”Ellipsometric study of thermal and laser annealed amorphous and mirocrystalline silicon films”, Applied Surface Science vol. 92 (1996) pp. 300-5;

[11] M. Zacharias et al, “Thermal crystallization of amorphous Si/SiO2 superlattices”, App.Phys.Lett., vol. 74 (1999) pp. 2614-6;

[12] R.B. Beck, “Formation of ultrathin silicon oxides – modeling and technological constraints”, Materials Science in Semiconductor Processing, vol. 6 (2003) pp. 49-57.

# Effect of Inner Interface Traps on High-K Gate Stack Admittance Characteristics

A. Mazurak, J. Jasiński, B. Majkusiak
Institute of Microelectronics and Optoelectronics
Warsaw University of Technology
Poland
a.mazurak@imio.pw.edu.pl

***Abstract*—Admittance parameters analysis can give useful information on traps located at the inner interface in high-k gate stacks. The presented study reveals that conductance characteristics are more valuable for characterization procedure then capacitance ones. It particularly considers structures in which tunnel communication via traps cannot be neglected.**

***Keywords—tunnelling; inner interface traps; border traps; high-k gate stack; admittance characterization; MIS structures***

## I. INTRODUCTION

Due to thermodynamic stability and electrical quality requirements for the substrate interface, a typical high-k gate stack comprises an interfacial silicon dioxide layer beneath the high-k layer. In this paper, the effect of tunneling through traps located at the inner interface inside the high-k gate stack on the small-signal admittance parameters of the multilayer gate stack MIS tunnel diode is investigated by means of a theoretical model.

## II. THEORETICAL MODEL

The band diagram of the considered structure is presented in Fig. 1. The applied theoretical model of the MIS tunnel diode, described in [1] [2], is based on the steady-state analytical model [3] and a three-phase procedure utilized to determine the small-signal response. The model was expanded by including a small-signal response of the insulator traps located at the inner interface inside the gate stack, which are charged and discharged by processes of tunneling from/to the gate electrode (current $J_{ST}$) and processes of thermally activated elastic tunneling from/to the semiconductor conduction band (current $J_{trC}$) and the valence band (current $J_{trV}$) as depicted in Fig. 2. The calculation procedures for tunnel currents between the substrate and the gate electrode ($J_{VT}$, $J_{CT}$) utilize an analytical formula for tunneling probability through a double-layer barrier presented in [4].

## III. DISCUSSION

The simulations were performed for gate stacks formed of metal gate, hafnium oxide and a silicon dioxide interfacial layer. The single-energy level traps were located at the inner interface (i.e. between the high-k layer and the interfacial layer). The effect of relative location of the inner interface

This work was supported by National Science Centre Poland upon decisions no. DEC-2012/07/N/ST7/03233 and DEC-2011/03/B/ST7/02595.

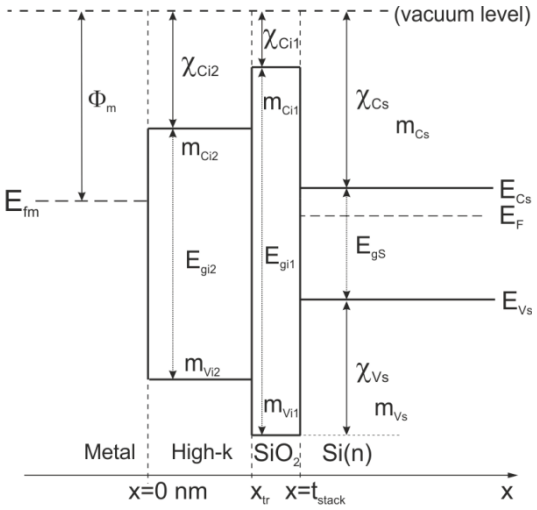



Fig. 1. Band diagram of considered multilayer gate stack MIS tunnel diode.

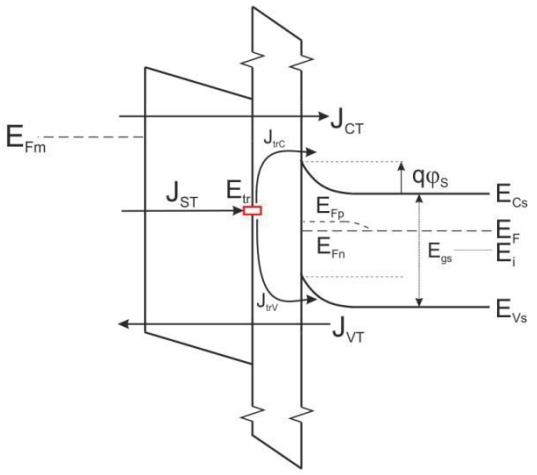



Fig. 2. Currents flow implemented in the model.

($x_{tr}$ / $t_{stack}$) on small-signal admittance parameters of the considered structure are presented in Fig. 3 and Fig. 4.
The parallel conductance ($G_{Pm}$) and capacitance ($C_{Pm}$) refer to the parallel equivalent circuit used in capacitance-voltage

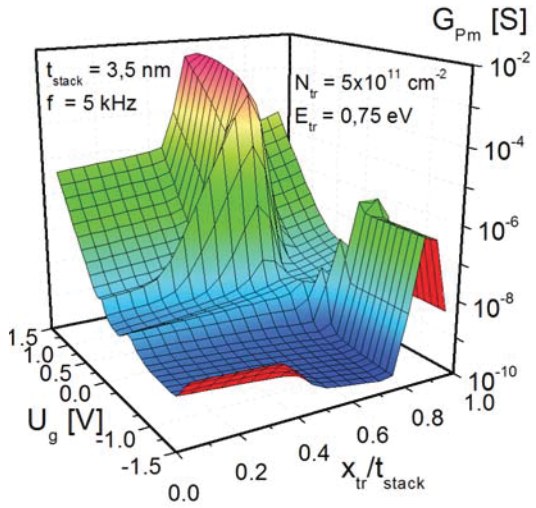



Fig. 3. Simulated gate voltage dependencies of the parallel conductance $G_{Pm}$.

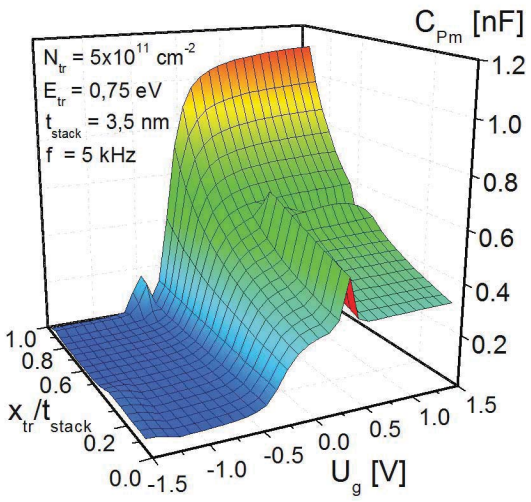



Fig. 4. Simulated gate voltage dependencies of the parallel capacitance $C_{Pm}$.

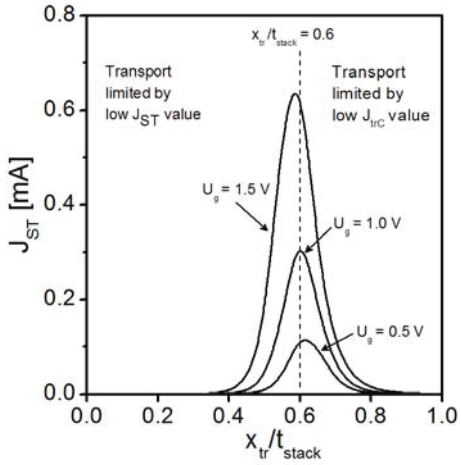



Fig. 5. Simulated current via traps located at the gate stack inner interface.

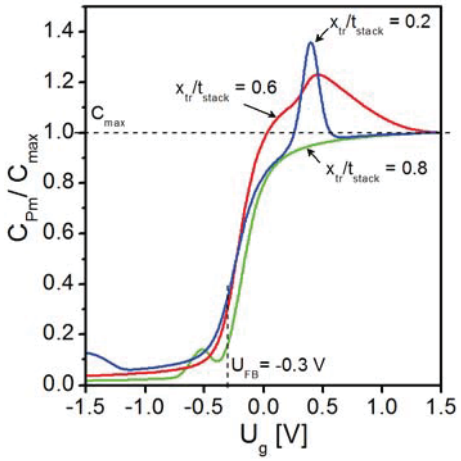



Fig. 6. Normalized gate voltage dependencies of the parallel capacitance $C_{Pm}$. with $x_{tr}/t_{stack}$ as a parameter.

measurements. There is a significant peak of conductance at $x_{tr}/t_{stack} = 0.6$ (Fig. 3) at the accumulation bias range (i.e. $U_g > 0.5$ V). It reflects the maximum efficiency of the tunnel current transport across the gate stack. In that case the current through the traps reaches its maximum (Fig. 5) and it is much more efficient then direct tunneling ($J_{VT}$, $J_{CT}$). Since the currents continuity is preserved at the trap node, for $x_{tr}/t_{stack} < 0.6$ the transport is limited by low $J_{ST}$ value (due to the thick high-k layer). In the opposite case ($x_{tr}/t_{stack} > 0.6$), the thick interfacial layer (and thus low $J_{trC/V}$) limits the transport efficiency. If both insulator layers were made of the same material, the peak conductance would be obtained for $x_{tr}/t_{stack} = 0.5$ [5].

If the interfacial layer is very thin (i.e. $x_{tr}/t_{stack} \rightarrow 1$) the inner interface traps act as they were substrate interface traps and their small-signal response can be observed in the inversion region (-0.8 V < $U_g$ < -0.4 V) of the C-V (Fig. 4) and G-V (Fig. 3) characteristics.

For thick high-k layers ($x_{tr}/t_{stack} > 0.7$) there is no noticeable impact of the traps on C-V curves in the accumulation region (i.e. $U_g > 0.2$ V). As in the aforementioned case of $G_{pm}$ characteristics (Fig. 3), traps effect the C-V characteristic most significantly when $x_{tr}/t_{stack} = 0.6$ (Fig. 6). The discrepancies between $C_{pm}$ and the maximum value of capacitance in the accumulation region can be clearly seen for the bias range above the flat band voltage (Fig. 6). In the case of a thin high-k layer ($x_{tr}/t_{stack} < 0.3$), there is a good agreement between $C_{pm}$ and the maximum value of capacitance in the accumulation

region, except a narrow bias range of 0.3 V < $U_g$ < 0.5 V. The sharp peak of C-V characteristic in the above mentioned bias range reflects enhanced small-signal communication between inner interface traps and the metal gate.

In order to investigate the effect of the tunnel communication via traps on admittance characteristics, simulations for $t_{stack}$ = 4.5 nm were performed. For the assumed thickness, the overall gate current is dominated by $J_{ST}$, which is several orders of magnitude higher than ($J_{CT} + J_{VT}$) - Fig. 7. The parallel conductance ($G_{Pm}$) value in the inversion region results directly from the $J_{ST}$ current value. The $J_{ST}$ current level reflects the traps density according to the model presented in [6]. In consequence, higher traps densities lead to higher $G_{Pm}$ values for the considered gate voltages (Fig.8). The simulation results obtained with a model which does not comprise $J_{ST}$ tunnel current, prove that this transport mechanism has a significant impact on $G_{Pm}$ and cannot be neglected, especially for higher traps densities (Fig. 9).

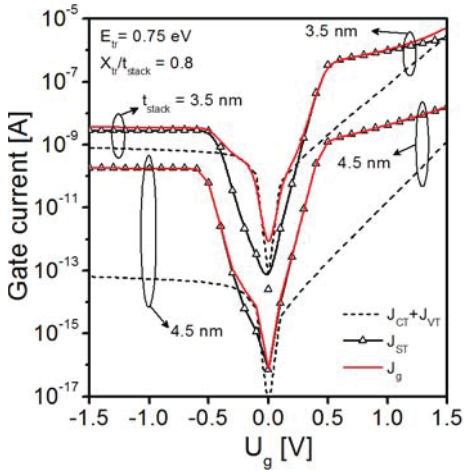



Fig. 7. Simulated current-voltsge characteristics for $t_{stack}$ = 3.5 nm and $t_{stack}$ = 4.5 nm.

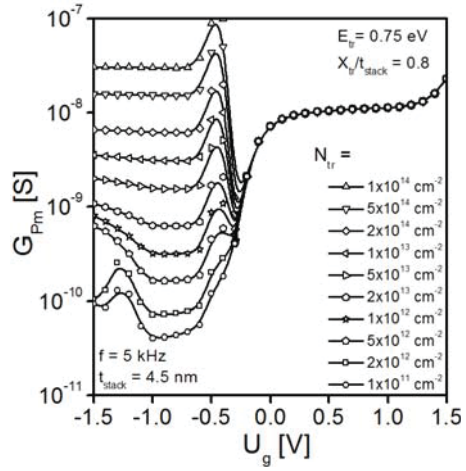



Fig. 8. Simulated gate voltage dependencies of the parallel conductance $G_{pm}$ with inner interface traps density $N_{tr}$ as a parameter.

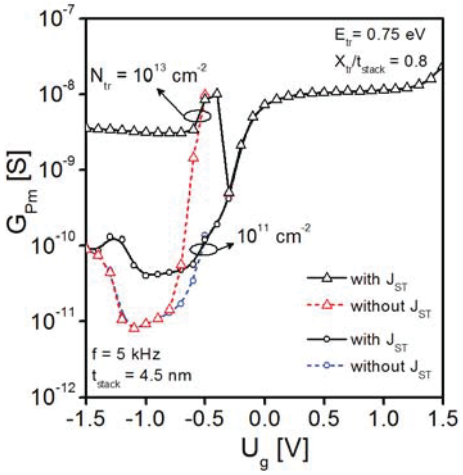



Fig. 9. Simulated $J_{ST}$ tunnel current impact on parallel conductance $G_{pm}$ vs. $V_g$ characteristics.

Moreover, there is a range of the inner interface position ($x_{tr}$ / $t_{stack}$) for which parallel conductance is a linear function of traps density ($N_{tr}$), as presented in Fig. 10.

The simulations presented in this paper were performed with the standard values of material parameters for silicon and silicon dioxide. The hafnium oxide parameters values used for the simulations are presented in Tab. 1.

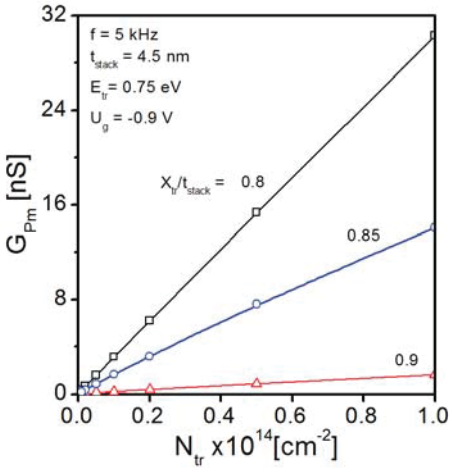



Fig. 10. Simulated parallel conductance $G_{pm}$ dependency of the inner interface traps density $N_{tr}$ .

TABLE I. HAFNIUM OXIDE PARAMETERS

| | |
|---|---|
| Band gap | 5.8 eV |
| Electron affinity | 1.9 eV |
| Electron effective mass | 0.2 |
| Hole effective mass | 0.6 |
| Dielectric constant | 20 |

## IV. Conclusion

The presented discussion proved that the tunnel communication between the inner interface traps inside the high-k gate stack and both the gate electrode and the semiconductor substrate in many cases is significant and cannot be neglected in modelling small-signal admittance parameters of the multilayer gate stack devices

## References

[1] J. Jasiński, A. Mazurak, R. Mroczyński, and B. Majkusiak, "Small-signal admittance model of multi-traps distributed over energy and space in the insulator of MIS tunnel structures", Microelectron. Eng., vol. 147, pp. 349-353, May 2015.

[2] J. Jasiński and B. Majkusiak, "Small-signal admittance model as a characterization tool of the MOS tunnel diode", J. Vac. Sci. Technol. B, vol. 31, issue 1, pp. (01A111-1)-7, January 2013.

[3] B. Majkusiak and A. Strojwas, "Influence of oxide thickness nonuniformities on the tunnel current-voltage and capacitance-voltage characteristics of the metal-oxide-semiconductor system", J. Appl. Phys., vol. 74, issue 9, pp. 5638-5647, November 1993.

[4] B. Majkusiak, "Analytical modeling of the tunneling probability through the double-layer gate stacks", J. Vac. Sci. Technol. B: Microelectronics and Nanometer Structures, vol. 27, issue 1, pp. 346-351, January/February 2009.

[5] J. Jasiński, A. Mazurak and B. Majkusiak, "Study of the effect of tunneling through the traps inside the insulator on small-signal admittance of the MOS structure", Microelectron. Eng., vol. 109, pp. 1-4, September 2013.

[6] L. B. Freeman and W. E. Dahlke, "Theory of tunneling into interface states", Solid-State Electronics, vol. 10, pp. 865-873, 1967.

# Comparative study of vertical GAA TFETs and GAA MOSFETs in function of the inversion coefficient

V. B. Sivieri, P. G. D. Agopian, J. A. Martino
LSI/PSI/USP
University of Sao Paulo
Sao Paulo, Brazil
victor.sivieri@gmail.com

R. Rooyackers, A. Vandooren, E. Simoen, A. Thean and C. Claeys
Imec
E.E. Dept., KU Leuven
Leuven, Belgium

***Abstract*— In this work, a comparative study between vertical silicon GAA TFETs and silicon GAA MOSFETs was realized, focusing on relevant analog parameters, as transistor efficiency, Early voltage, intrinsic voltage gain, unity gain frequency, and the product of the transistor efficiency multiplied by the unity gain frequency. The key parameter of comparison is the inversion coefficient (IC). The analysis was performed considering the different conduction regimes (weak, moderate and strong). MOSFETs have presented a higher transistor efficiency and a lower value of Early voltage in comparison with TFETs. In contrast, the latter technology presents a higher intrinsic voltage gain for the whole range of extracted ICs. Some other figures of merits, as the unity gain frequency and the product of the unity gain frequency and the transistor efficiency were obtained. A plateau was observed for the MOSFETs, but the TFETs transconductance and product only increase with the gate voltage.**

***Keywords: TFET; inversion coefficient, analog parameters***

## I. INTRODUCTION

In order to overcome the technological limitations of conventional MOSFETs, devices with a new operation principle have been researched. The tunneling field effect transistors (TFETs) arise in this category as a promising candidate to substitute the conventional MOS devices and are based on band-to-band tunneling as the main conduction mechanism, in contrast to the drift/diffusion mechanisms of MOSFETs. This new technology presents as advantages a lower off-current and a subthreshold swing (SS) theoretically lower than 60 mV/dec, since they do not have the MOS limit due to the different operation principle [1–4].

Despite the mentioned advantages, the TFETs show a lower on-current level at high gate voltages, in comparison to the conventional devices. Therefore, new materials and new structures have been researched [5–6]. The structure studied in this work is the gate-all-around (GAA), which presents a stronger electrostatic coupling between the gate and the channel carriers in relation to the planar structure.

Although TFETs have been proposed mainly for digital applications, it has been observed that their analog behavior can be better if compared with the MOS transistors. [7–11]

In this work, the analog behavior of vertical gate all around TFETs is compared with vertical gate all around MOSFETs in terms of transistor efficiency, unity gain frequency, Early voltage and intrinsic voltage gain. The analysis was performed considering the different conduction regimes (inversion coefficient).

## II. DEVICE CHARACTERISTICS

The studied devices were fabricated at imec, Belgium and are silicon gate-all-around (GAA) nTFETs and nMOSFETs, which use a top down vertical process flow. The gate stack consists of 3nm $HfO_2$ on 1nm $SiO_2$. The gate electrode is composed by TiN and α-silicon. Regarding their dimensions, the TFETs have a physical gate length (LG) of 150 nm, a gate/source overlap (LGS) of 30 nm, a gate/drain underlap (LGD) of 50 nm and a channel length of 170 nm. The MOSFETs have a physical gate length (LG) of 250 nm, a gate/source overlap (LGS) of 140 nm, a gate/drain underlap (LGD) of 50 nm and a channel length of 180 nm. The source and the drain region are doped with $1.10^{20}$ at.cm$^{-3}$ boron (in the case of TFETs) and $2.10^{19}$ at.cm$^{-3}$ As, respectively. The channel is doped with $1.10^{16}$ at.cm$^{-3}$ As. The measured devices contain 100 nanowires in parallel and have 160 nm of diameter. The difference between the MOSFETs and the TFETs process resides in the source doping process. The source of the nMOS devices is doped with $2.10^{20}$ at.cm$^{-3}$ As. The structure of the studied devices is shown in figure 1.

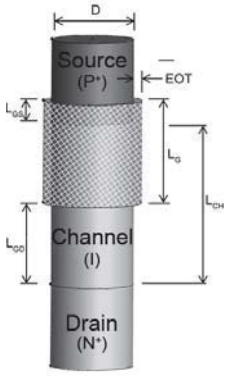



**Fig. 1** – Structure of the devices.

## III. Experimental Results and Discussion

Figure 2 shows the transfer characteristic curves of both the tunneling and MOS transistors. As expected for silicon devices, the current level of the TFETs is approximately 4 orders of magnitude lower than the one of the MOSFETs due to the different conduction mechanisms (Band To Band Tunneling - BTBT). Since silicon has a high bandgap value, the BTBT onset voltage is high, i.e., a sufficiently high gate voltage needs to be applied to the gate in order to reach the BTBT dominated regime at the gate/source junction.

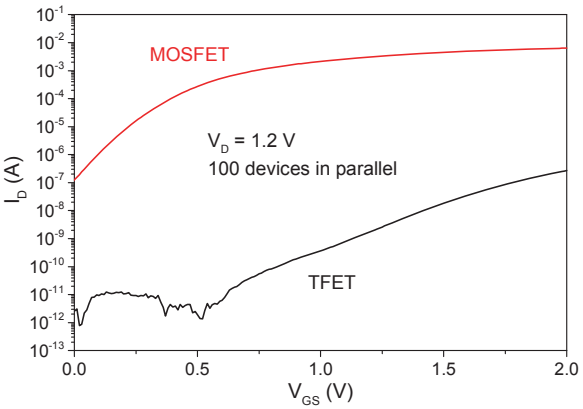



**Fig. 2** – Experimental $I_D$ and gm as a function of $V_{GS}$ for GAA nTFETs and GAA nMOSFETS.

Aiming to compare the device behavior, the analog parameters analysis was performed as a function of the inversion coefficient (IC). The inversion coefficient is the normalized drain current in relation to the transition current [12]. This ratio depends on the difference between $V_{GS}$ and the threshold voltage ($V_T$). Figure 3 shows the relation between the overdrive voltage ($V_{GS} - V_T$) and the inversion coefficient for the GAA MOSFET. In the case of MOSFETs, the extracted $V_T$ is 0.48V. In the case of TFETs, the value used was the one corresponding to the BTBT onset voltage, which is equal to 1.9V. More details for the extraction method of this value can be found in [7, 13].

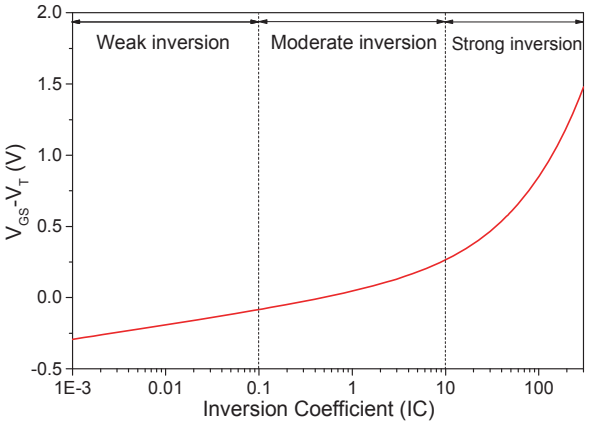



**Fig. 3** – Experimental $V_{GS}$-$V_T$ vs IC for a GAA MOSFET indicating the different conduction regimes.

The first of the analyzed parameters is the transistor efficiency ($gm/I_D$). This parameter indicates the device capability of producing a high gain at the same power dissipation level. Figure 4 shows the experimental transistor efficiency as a function of the inversion coefficient for both technologies. One can notice that the maximum value of IC obtained for the TFET is approximately 1, due to the high value used for its threshold voltage. It is possible to observe that both technologies follow the same trend in terms of efficiency, i.e., its value decreases with the increase of IC, but the MOS devices present a higher $gm/I_D$ than their tunneling counterparts. This occurs because the transconductance of MOSFETs is higher than the transconductance of TFETs.

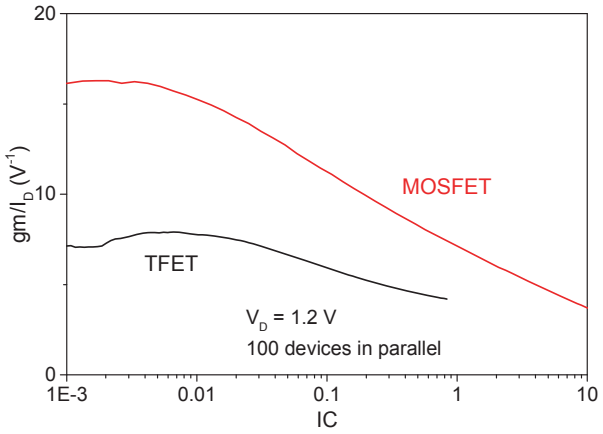



**Fig. 4** – Experimental $gm/I_D$ as a function of IC for GAA TFET and GAA MOSFET.

The second analyzed parameter is the Early voltage ($V_{EA}$), which indicates the "quality" of the device output characteristic. As the tunneling mechanisms present a weaker dependence on drain voltage than the drift ones, TFETs present a better output characteristic at high $V_D$ (higher $V_{EA}$). Figure 5 shows the Early voltage as a function of the gate voltage for TFET and MOSFET devices. The nMOS transistors presented $V_{EA}$ values around -10V (almost constant over the $V_{GS}$ range studied).

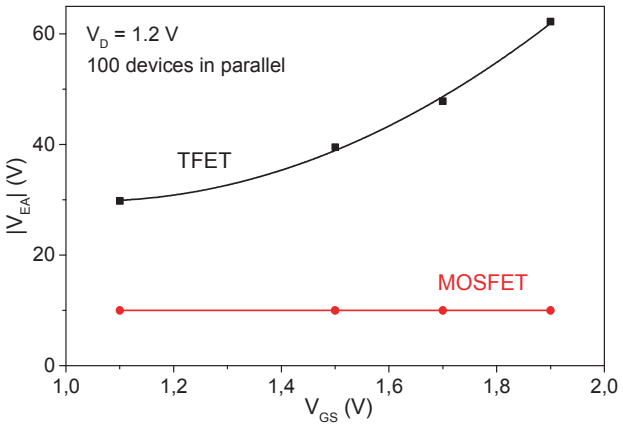



**Fig. 5** – Experimental $V_{EA}$ as a function of $V_{GS}$ for GAA TFET and GAA MOSFET.

The intrinsic voltage gain ($A_V$) of both technologies was calculated using the following equation:

$$A_V \approx gm/g_D \approx V_{EA} * gm / I_D$$

Based on this calculation, the curves of $A_V$ as a function of IC, shown in figure 6, were obtained. It is possible to observe that in spite of the non-ideal behavior of the TFET in terms of Ion current and subthreshold slope, the intrinsic voltage gain is higher for all the conduction regimes in comparison with MOS technology. This effect happens because the Early voltage of TFETs is higher than the one of MOSFETs and compensates the lower values of transistor efficiency.

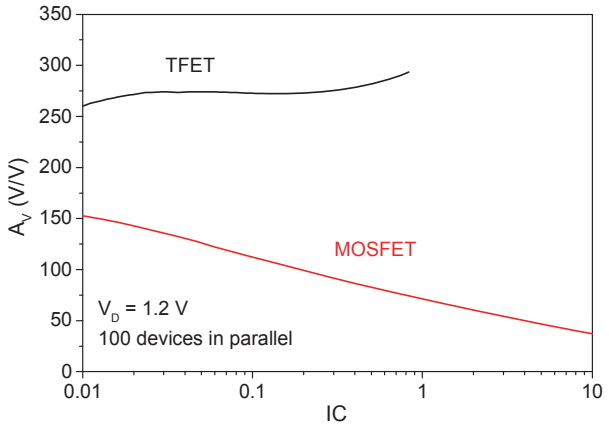



**Fig. 6** – Experimental $A_V$ as a function of IC for GAA TFET and GAA MOSFET.

The unity gain frequency was also analyzed and was calculated using the following equation:

$$f_T = gm/2\pi C_{gg}$$

where $C_{gg}$ is the total gate capacitance.

Figure 7 shows the curves of the unity gain frequency as a function of the inversion coefficient. The dashed curve corresponds to the simulated result. The simulation was performed in order to analyze the TFET behavior for IC > 1. It is noticeable that the $f_T$ value of the MOSFET is higher than the one of the TFET. The difference in the trend resides in the transconductance behavior variation (figure 8) for each technology. While gm suffers a degradation at high gate voltages for the MOS devices, it increases exponentially for TFETs.

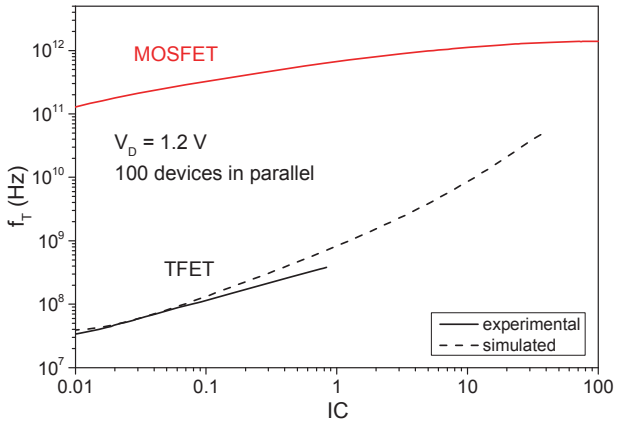



**Fig. 7** – Experimental and simulated $f_T$ as a function of IC for GAA TFET and GAA MOSFET.

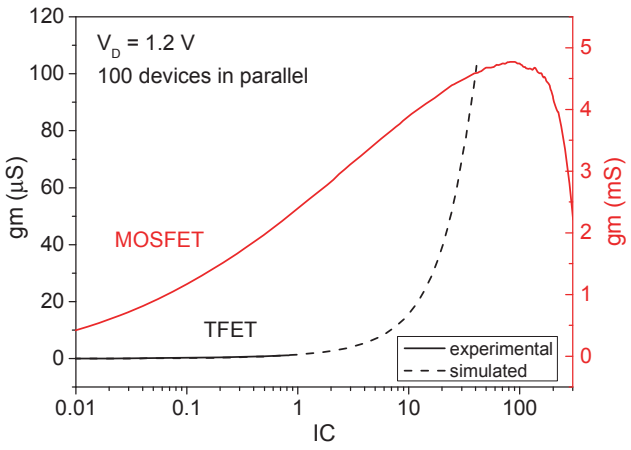



**Fig. 8** – Experimental and simulated gm as a function of IC for GAA TFET and GAA MOSFET.

One FoM (Figure of Merit) used in this work is the unity gain frequency multiplied by the transistor efficiency, presented in figure 9. The GAA MOSFET presents an optimun region (plateau) around IC = 1, while the GAA TFET presented no plateau region. It increases with IC, which is only observed for TFET devices.

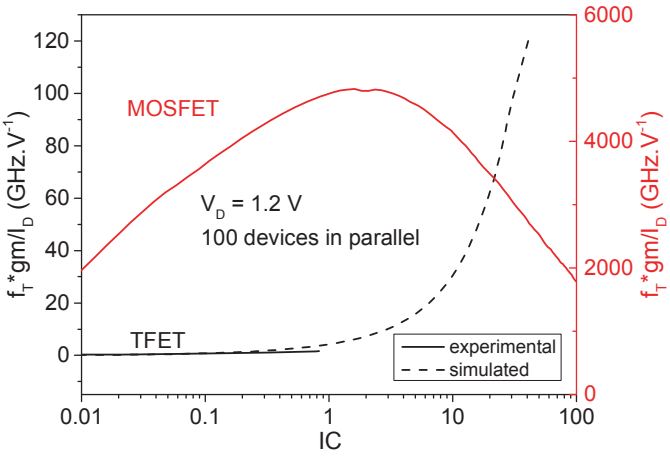



**Fig. 9** – Experimental and simulated $f_T$ x gm/$I_D$ as a function of IC for GAA TFET and GAA MOSFET.

## IV. Conclusions

In this work, a comparative study between GAA MOSFETs and GAA tunneling devices was presented. The analysis focused on analog parameters, such as the transistor efficiency, the Early voltage, the intrinsic voltage gain and the unity gain frequency. The parameters were compared considering the different conduction regimes. For this purpose, the inversion coefficient was utilized in the analysis.

Although the MOSFET efficiency is higher, its intrinsic voltage gain is lower in comparison with the TFET for all of the conduction regimes, due to the better output characteristic of the tunneling technology.

The MOS transistors presented a higher value of unity gain frequency for all of the analyzed inversion coefficients. Though, a decrease of the product $f_T$ x $gm/I_D$ was observed for the MOS technology at higher current levels, while this product of TFETs only increased.

## ACKNOWLEDGMENT

The authors would like to thank CAPES, FAPESP, CNPq and FWO for the financial support. The devices were processed in the frame of imec's Core Partners Program on Advanced Logic Devices.

## REFERENCES

[1] W. Reddick et al., *Appl. Phys. Lett*., 67, 494-496, (1995).

[2] A. Verhulst et al., *J. Appl. Phys*., 104(6), (2008).

[3] T. Krishnamohan et al., *Techn, Dig. IEDM*, 947-950, (2008).

[4] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches", *Nature*, 329-337, (2011).

[5] J. Knoch and J. Appenzeller, "Modeling of High-Performance p-Type III–V Heterojunction Tunnel FETs", IEEE Elec. Dev. Letters, 31, 305-307, (2010).

[6] S. Sasaki et al., "Encapsulated gate-all-around InAs nanowire field-effect transistors", *Appl. Phys. Lett.*, 103, p. 213502, (2013).

[7] M. Martino et al., "Analog performance of vertical nanowire TFETs as a function of temperature and transport mechanism", *Solid-State Electronics*, 112, 51-55 (2015).

[8] P. Agopian, "Influence of the Source Composition on the Analog Performance Parameters of Vertical Nanowire-TFETs", *IEEE TED*, 62, 16-22, (2014).

[9] A. Mallik et al., "Tunnel Field-Effect Transistors for Analog/Mixed-Signal System-on-Chip Applications", *IEEE TED*, 59, n.4, 888-894, (2012).

[10] P. Agopian et al., "NW-TFET analog performance for different Ge source compositions", *Proc. IEEE S3S Conference*, (2013).

[11] P. Agopian et al., "Experimental Comparison Between Trigate p-TFET and p-FinFET Analog Performance as a Function of Temperature", *IEEE TED*, 60, 2493 (2013).

[12] W. M. C. Sansen, "Analog Design Essentials", *Springer*, (2006).

[13] A. Vandooren et al., "Analysis of trap-assisted tunneling in vertical Si homo-junction and SiGe hetero-junction Tunnel-FETs", *Solid-State Electronics*, 83, 50 (2013).

# Influence of Spin Relaxation on Trap-assisted Resonant Tunneling in Ferromagnet-Oxide-Semiconductor Structures

Viktor Sverdlov and Siegfried Selberherr
Institute for Microelectronics, TU Wien, Gußhausstraße 27-29, A-1040 Wien, Austria
e-mail: {Sverdlov|Selberherr}@iue.tuwien.ac.at

***Abstract*—Spin-dependent resonant tunneling in ferromagnet-oxide-semiconductor structures is currently of great interest due to the promising potential of semiconductors and silicon in particular for spin-driven applications. Trap-assisted tunneling explains the larger than predicted signal in three-terminal spin-injection experiments. However, for realistic comparison to experiments at elevated temperatures the master equation describing the occupation and spin evolution at an electron trap coupled to the contacts must be augmented to include spin relaxation and dephasing. A short spin relaxation time suppresses the "spin blockade", thus reducing the magnetoresistance modulation. However, intensive dephasing does not strongly affect the magnetoresistance. The substantial magnetoresistance modulation is present at an arbitrary trap position relative to the contacts. Finally, an unusual non-monotonic dependence of the magnetoresistance half-width as a function of the perpendicular magnetic field with dephasing increased is observed.**

***Keywords*—Spin, trap-assisted tunneling, master equation, spin relaxation, spin dephasing, tunneling magnetoresistance***

## I. Introduction

Silicon, the main material of microelectronics, is perfectly suited for spin-driven applications due to its weak spin-orbit interaction and long spin lifetime [1,2]. Spin injection from a ferromagnetic electrode into n-silicon was claimed at room temperature [3] and also at elevated temperatures [4]. However, the amplitude of the signal extracted from a three-terminal injection method [3,4] is orders of magnitude larger than that predicted by a theory [1], provided the signal is caused by spin accumulation in silicon. Possible reasons for this discrepancy are currently heavily debated [1,5-8]. An alternative interpretation of the three-terminal signal magnitude based on spin-dependent magnetoresistance due to trap-assisted resonant tunneling was proposed [5]; however, the effects of spin dynamics and spin relaxation [6], which are important at room temperature, were not taken properly into consideration. Our goal has been to investigate the role of the spin dynamics on a trap including spin relaxation and decoherence in order to determine the trap-assisted tunneling magnetoresistance.

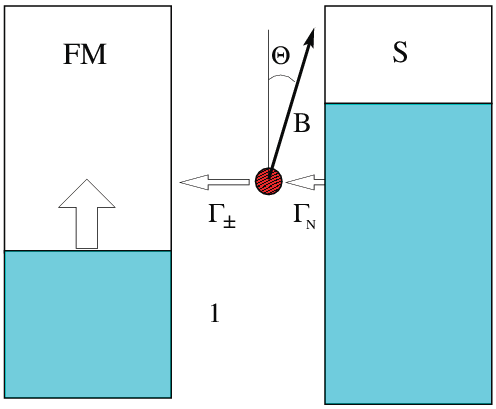



Fig. 1. An electron tunnels with the rate $\Gamma_N$ on the trap and $\Gamma_\pm$ to the ferromagnet. A magnetic field **B** defines the trap spin quantization axis OZ', which is at an angle Θ to the magnetization orientation OZ in the ferromagnetic contact.

## II. Method

To highlight the role of spin relaxation and decoherence on the impurity we introduce the corresponding relaxation terms into a Lindblad equation for the density matrix evolution of spin on a trap. Without these relaxation terms included the master equation for the spin density matrix $\rho_{\sigma\sigma'}$ $(\sigma, \sigma' = \pm)$ was recently derived in [5] from the Anderson impurity model in the limit of large on-site interaction. In the basis with the quantization axis chosen along the magnetization direction (Fig.1) in the ferromagnetic contact the corresponding equations are [5]:

$$\frac{d}{dt}\rho_{\sigma\sigma} = \frac{\Gamma_N}{2}(1-\alpha) - \Gamma_\sigma \rho_{\sigma\sigma} + \omega_L \sin(\Theta)\,\mathrm{Im}\,(\rho_{-\sigma\sigma})\,, \qquad \sigma = \pm \quad (1)$$

$$\frac{d}{dt}\rho_{\sigma-\sigma} = i\omega_L(\sin(\Theta)\ (\rho_{-\sigma-\sigma} - \rho_{\sigma\sigma})/2 \pm \cos(\Theta)\rho_{\sigma-\sigma}) - \frac{\Gamma_\sigma + \Gamma_{-\sigma}}{2}\ \rho_{\sigma-\sigma}\ , \qquad -\sigma = \mp \quad (2)$$

Here the tunneling rate $\Gamma_N$ from silicon to a trap does not depend on spin, while the tunneling rate from the trap to a

ferromagnet depends on the spin projection σ = ± on the magnetization direction:

$$\Gamma_{\pm} = \Gamma_F(1 \pm p) \quad (3)$$

The current polarization at the interface of the ferromagnet $p \leq 1$ is defined as

$$p = \frac{\Gamma_+ - \Gamma_-}{2\Gamma_F}. \quad (4)$$

The external magnetic field **B** at the impurity position applied in the XZ plane is assumed to form an angle Θ with the magnetization direction in the ferromagnetic lead. The magnetic field **B** enters into the equations (1,2) via the spin Larmor precession frequency

$$\omega_L = |\boldsymbol{\omega}_L| = \left|\frac{e\mathbf{B}}{mc}\right|, \quad (5)$$

where *e* and *m* are the electron charge and the mass, *c* is the velocity of light. In (1) Im denotes the imaginary part and in (2) *i* is the imaginary unit.

Let us briefly discuss the terms appearing on the right-hand side of the equations (1,2). The time dependence of the diagonal elements of the density matrix (1) is governed by the balance of the first influx term from the normal electrode on the trap and the second outflux term to the ferromagnet The influx term is proportional to the tunneling rate $\Gamma_N$ multiplied by the probability

$$P_0 = 1 - \alpha \quad (6)$$

that the site is empty, where $0 \leq \alpha \leq 1$ is the probability of the trap to be occupied. The one-half coefficient in the first term is due to the fact that the electron tunneling from the normal electrode can occupy the site with equal probabilities for the spin projection σ to be up or down.

The second outflux term is proportional to the probability that the state with a certain spin projection is occupied multiplied by the corresponding tunneling rate. It is also assumed for simplicity that a relatively high voltage *U* is applied between the electrodes, so the trap is located at such an energy *E* that the corresponding state in the normal electrode is always occupied, while the state in the ferromagnet is empty. A generalization to lower voltages and finite temperatures is straightforwardly accomplished by weighting the tunneling rates $\Gamma_N$ and $\Gamma_\sigma$ with the Fermi distribution $f(E)$ and $(1 - f(E+U))$, respectively.

In order to interpret the third term in the right-hand side of (1) let us express the density matrix ρ in terms of the spin projections $s_x$, $s_y$, and $s_z$, on the coordinate axis X, Y, and Z, correspondingly, in the form

$$\rho = \frac{1}{2}\left(\alpha I + s_x\sigma_x + s_y\sigma_y + s_z\sigma_z\right), \quad (7)$$

where *I* is the unity matrix and $\sigma_i,\ i = x, y, z$ are the Pauli matrices. The difference of the equations (1) for σ = ± can be written as:

$$\frac{d}{dt}s_z = -\Gamma_F s_z - p\Gamma_F\alpha - \omega_L\sin(\Theta)s_y \quad (8)$$

For completeness we also provide the equation for the site occupation probability $\alpha$ following from summing up the equations (1):

$$\frac{d}{dt}\alpha = \Gamma_N(1-\alpha) - \Gamma_F\alpha - p\Gamma_F s_z \quad (9)$$

In case $p = 0$ one obtains the standard balance equation for the occupation decoupled from the spin. The non-zero spin polarization of the drain electrode involves the spin degree of freedom into the equation for the site occupation, thus affecting the current which results in the resistance dependence on the magnetic field.

Similarly, the sum and difference of equations (2) produce the following equations:

$$\frac{d}{dt}s_x = \omega_L\cos(\Theta)s_y - \Gamma_F s_x \quad (10)$$

$$\frac{d}{dt}s_y = -\omega_L\cos(\Theta)s_x + \omega_L\sin(\Theta)s_z - \Gamma_F s_y \quad (11)$$

The last terms in equations (10), (11) describe the escape probabilities of the spin being in the XY plane into the ferromagnet. Because the XY plane is perpendicular to the magnetization orientation in the ferromagnet along the OZ axis, the escape probability is the sum of the two probabilities $\frac{\Gamma_+}{2}$ and $\frac{\Gamma_-}{2}$ to tunnel into the states with the spin up and spin down in the ferromagnet, respectively. Their sum $\frac{\Gamma_+ + \Gamma_-}{2}$ results, according to (3) in the total rate $\Gamma_F$. The equations (9-11) are conveniently written in the vector form

$$\frac{d}{dt}\mathbf{s} = -\Gamma_F\mathbf{s} - \mathbf{p}\Gamma_F\alpha + [\mathbf{s}\times\boldsymbol{\omega}_L], \quad (13)$$

where $\mathbf{s} = (s_x, s_y, s_z)$ and $\mathbf{p} = (0, 0, p)$. Equation (13) describes the dynamics of the spin in the presence of a magnetic field on the impurity coupled to the leads, one of which is ferromagnetic. Without the terms proportional to $\Gamma_F$ the equation resembles the Bloch equation for spin dynamics, however, without relaxation and dephasing included. Spin relaxation and dephasing can become quite important, especially at elevated temperatures, where experiments on spin injection in semiconductor by pushing the electrical current through a ferromagnet-oxide-semiconductor structure are performed. Similar to the Bloch equation, one can generalize (13) to include the spin lifetime $T_1$ and the dephasing time $T_2$.

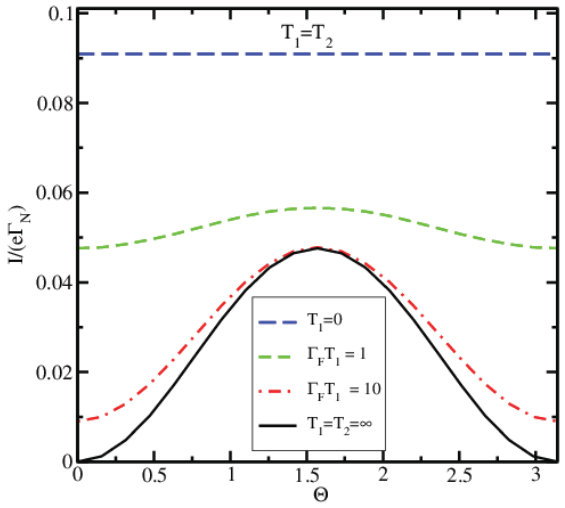



Fig. 2. Current in units of $e\Gamma_N$ as a function of Θ for $p$=1 $\Gamma_N/\Gamma_F$ = 10, $\omega_L/\Gamma_F$ = 1, and several values of $T_2$=$T_1$

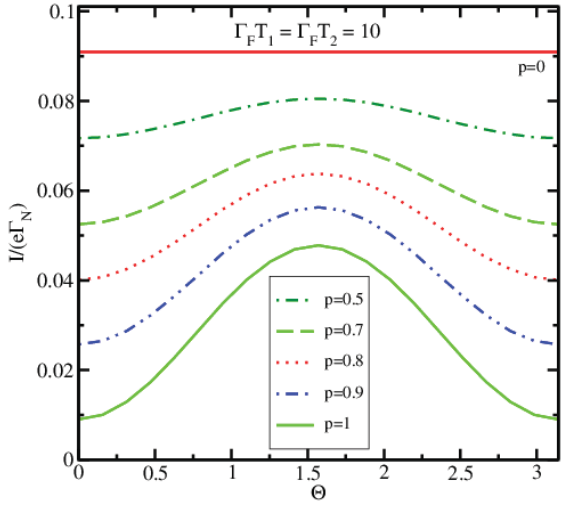



Fig. 3. Current as a function of Θ, for $\Gamma_N/\Gamma_F$ = 10, $\omega_L/\Gamma_F$ = 1, $\Gamma_F\, T_1 = \Gamma_F\, T_1$ = 10, and several values of $p$.

The spin dynamics is then described by

$$\frac{d}{dt}\mathbf{s} = -\Gamma_F\mathbf{s} - \mathbf{p}\Gamma_F\alpha + [\mathbf{s}\times\boldsymbol{\omega}_L] - \left(\frac{1}{T_1}-\frac{1}{T_2}\right)\frac{(\mathbf{s}\cdot\boldsymbol{\omega}_L)}{\omega_L}\frac{\boldsymbol{\omega}_L}{\omega_L} + \frac{1}{T_1}s_0\frac{\boldsymbol{\omega}_L}{\omega_L} - \frac{1}{T_2}\mathbf{s} \qquad (14)$$

Thereby it is guaranteed that the spin component along the magnetic field **B** relaxes with the time $T_1$ to an equilibrium value $s_0$, while the perpendicular component dephases with the time $T_2$. The master equation (14) includes the spin lifetime $T_1$ and coherence time $T_2$. Typically $T_2 \leq T_1$, however, at elevated room temperature $T_2 \cong T_1$.

In order to analyze (14), we assume that the temperature is high compared to the Zeeman energy $kT \gg \hbar\omega_L$ so that one can neglect $s_0$. It is also more convenient to change the basis to *x',y',z'* axes so that the *z'* axis is along the direction of the magnetic field on the trap. The density matrix in this basis is written as

$$\rho = \alpha I + a\sigma_x' + b\sigma_y' + c\sigma_z' \qquad (15)$$

with *a, b, c* being the spin expectation value projections on the axes *x',y',z'*. To find a stationary solution of (14) we set $\frac{d}{dt}\mathbf{s} = 0$. Then (14) results in the following equations

$$b\omega_L + c\left(\frac{1}{T_2}+\Gamma_F\right) = 0\,, \qquad (16a)$$

$$c\,\omega_L\cos(\Theta) - a\sin(\Theta)\left(\frac{1}{T_1}+\Gamma_F\right) - b\cos(\Theta)\left(\frac{1}{T_2}+\Gamma_F\right) = 0\,, \qquad (16b)$$

$$b\sin(\Theta)\left(\frac{1}{T_2}+\Gamma_F\right) - a\cos(\Theta)\left(\frac{1}{T_1}+\Gamma_F\right) - c\,\omega_L\sin(\Theta) = p\Gamma_F\alpha\,, \qquad (16c)$$

while (9) after setting $\frac{d}{dt}\alpha = 0$ results in

$$(\Gamma_F+\Gamma_N)\alpha + p\Gamma_F(a\cos(\Theta) - b\sin(\Theta)) = \Gamma_N. \qquad (16d)$$

The current *I* due to tunneling via a trap is computed as

$$I = e\,\Gamma_F(1-\alpha). \qquad (17)$$

## III. RESULTS

Solving equations (16,17) results in the following expression for the current:

$$I = e\frac{\Gamma_F(\Theta)\,\Gamma_N}{\Gamma_F(\Theta)+\Gamma_N} \qquad (18a)$$

$$\Gamma_F(\Theta) = \Gamma_F\left(1 - p^2\,\Gamma_F T_1\left\{\frac{\cos^2\Theta}{\Gamma_F T_1+1} + \frac{T_2}{T_1}\frac{\sin^2\Theta(\Gamma_F T_2+1)}{\omega_L^2 T_2^2 + (\Gamma_F T_2+1)^2}\right\}\right) \qquad (18b)$$

The current *I* differs from $I_0 = \Gamma_F\,\Gamma_N / (\Gamma_F + \Gamma_N)$, the current value when both electrodes are nonmagnetic metals. It depends on the angle Θ between the spin quantization axis and the magnetization orientation.

In the case $T_1$=$T_2\to\infty$, when relaxation and dephasing are ignored, one obtains

$$\Gamma_F(\Theta) = \Gamma_F\left(1 - p^2\left\{\cos^2\Theta + \frac{\sin^2\Theta}{\omega_L^2/\Gamma_F^2+1}\right\}\right). \qquad (19)$$

With this result the corresponding expression for the current obtained in [5] is reproduced.

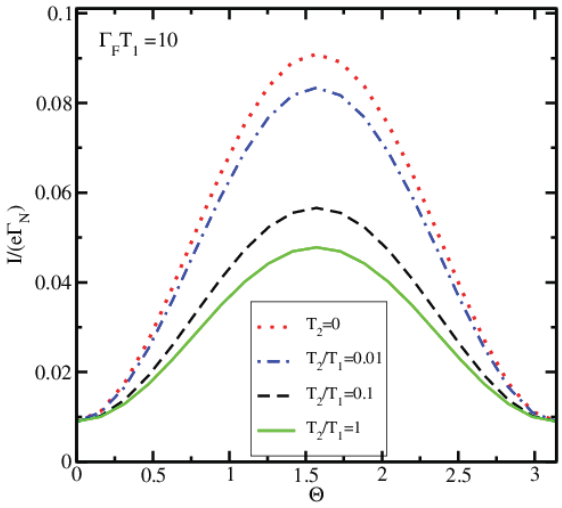



Fig. 4. Current as a function of Θ, for $p$=1, $\Gamma_N/\Gamma_F$ = 10, $\omega_L/\Gamma_F$ = 1, $\Gamma_F T_1$ = 10, and several values of $T_2/T_1$.

Complementary to [5], (18) includes the effects of spin relaxation. When $\Gamma_F T_1 = \Gamma_F T_2 \ll 1$, the resistance dependence on the magnetic field is a Lorentzian function with the half-width determined by the inverse spin lifetime. A short spin relaxation time suppresses the "spin blockade" [5], which appears at small Θ (Fig.2), in a similar fashion as the reduction of spin current polarization $p$ (Fig.3). Due to the suppression of the last term in (19) at short $T_2$ with $T_1$ fixed, the amplitude of the current $I(\Theta)$ modulation with Θ becomes more pronounced (Fig.4), in contrast to the intuitive expectation that strong decoherence should reduce the effect. At finite $T_1$ the modulation of $I(\Theta)$ is present at an arbitrary trap position relative to the contacts (Fig.5), complementary to [5]. Finally, with $T_2$ decreasing an unusual non-monotonic dependence of the magnetoresistance as a function of the perpendicular magnetic field **B**, with the linewidth decreasing, at shorter $T_2$ is shown in Fig.6.

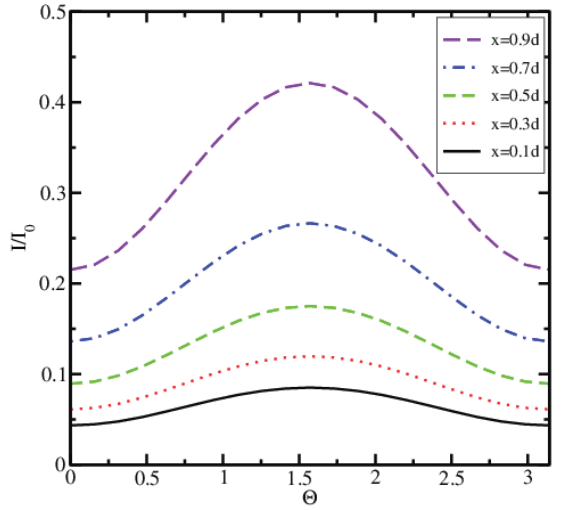



Fig. 5. *Normalized current as a function of the position x*, for $p$=1, $\Gamma_N=\Gamma_0 \exp(-x/d)$, $\Gamma_F=\Gamma_0 \exp(-(d-x)/d)$, $T_2=T_1$, $\omega_L T_2 = \Gamma_0 T_2 = 10$,

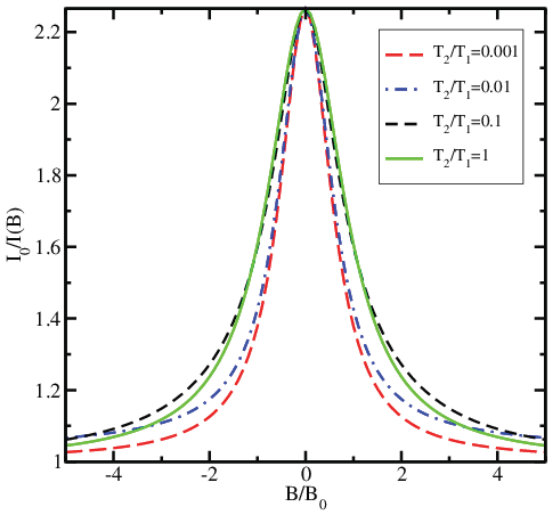



Fig. 6. Magnetoresistance signal as a function of the perpendicular magnetic field **B** for several $T_2/T_1$, for $p$=0.8 and $\Gamma_F T_1$=10. The field $\mathbf{B}_0$ is parallel to the magnetization in the ferromagnet.

## IV. Summary

The master equation describing the dynamics of the electron spin on a trap in oxide sandwiched between a ferromagnetic and a normal metal contact is augmented to include the spin relaxation and dephasing. Strong spin relaxation reduces the magnetoresistance modulation, however, strong dephasing has a lower effect on the magnetoresistance. At finite spin relaxation the substantial magnetoresistance modulation is present at an arbitrary trap position relative to the contacts. An unusual non-monotonic dependence of the magnetoresistance as a function of dephasing is observed.

This work is supported by the ERC grant #247056 MOSILSPIN.

[1] R. Jansen, "Silicon Spintronics", Nature Materials, vol.11, pp. 400-408, 2012

[2] V. Sverdlov and S. Selberherr, "Silicon Spintronics: Advances and Challenges", Physics Reports, vol.585, pp. 1-40, 2015

[3] S.P. Dash, S. Sharma, R.S. Patel, M.P. de Jong, and R.Jansen "Electrical Creation of Spin Polarization in Silicon at Room Temperature", Nature, vol.462, pp. 491-484, 2009

[4] C.H. Li, O.M.J. van 't Erve, and B.T. Jonker "Electrical Injection and Detection of Spin Accumulation in Silicon at 500 K with Magnetic Metal/Silicon Dioxide Contacts", Nature Communications, vol.2, art.245, 2011

[5] Y. Song and H. Dery, "Magnetic-Field-Modulated Resonant Tunneling in Ferromagnetic-Insulator-Nonmagnetic Junctions", Physical Review Letters, vol.113, art.047205, 2014

[6] V.Sverdlov and S.Selberherr, "Spin-dependent Trap-assisted Tunneling Including Spin Relaxation at Room Temperature", in Program and Abstract Book of the 8th International School and Conference on Spintronics and Quantum Information Technology (SPINTECH), 10-13 August 2015, Basel, Switzerland, p.114

[7] A. Spiesser, H. Saito, R. Jansen, Sh. Yuasa, and K. Ando, "Large Spin Accumulation Voltages in Epitaxial $Mn_5Ge_3$ Contacts on Ge without an Oxide Tunnel Barrier", Physical Review B, vol.90, art.205213, 2014

K.-R. Jeon, H. Saito, Sh. Yuasa, and R. Jansen, "Energy Dispersion of Tunnel Spin Polarization Extracted from Thermal and Electrical Spin Currents", Physical Review B, vol.91, art.155305, 2015

# Modeling Heat Dissipation in an SOI Device

## Finite Element Analysis at Semiconductor Die Level

George P. Hosey
ON Semiconductor
Corporate Research & Development
East Greenwich, Rhode Island, USA
George.Hosey@onsemi.com

**As the semiconductor market continues to drive toward increased power in smaller area, the industry will face new challenges in terms of materials and process integrations. These new challenges include power metallurgies, GaN, and a host of other materials. With increasing complexity and increased wafer costs, multiple iterations of experimental silicon are becoming more costly and more time consuming. As a result, the ability to simulate and predict material and geometry responses becomes all the more valuable. Finite element analysis (FEA) is often used for package level simulations, but has gone largely unused at wafer and die level. FEA offers numerous opportunities to explore the effects of temperature, stress, and strain and to evaluate possible solutions. This paper examines use of FEA to evaluate heat dissipation in a buried N+ resistor in an SOI technology and the factors impacting temperature. "DC" and transient simulations varying current, buried oxide thickness, contact materials, contact areas and substrate thickness, provide information on how heat is dissipated in an SOI power structure without requiring costly and time consuming silicon fabrication.**

**Keywords—Semiconductor on Insulator, SOI, Heat Dissipation**

### I. Introduction

As semiconductor devices shrink, heat dissipation becomes ever more challenging. While the task is already difficult in bulk silicon devices, it takes on even greater difficulty in a silicon-on-insulator (SOI) device. In bulk silicon, the heat can travel through the silicon to the package lead frame. In SOI devices, however, the buried oxide and oxide trenches surrounding the device act as heat insulation, trapping the generated heat within the SOI tub. The thermal resistance of SOI devices has been seen to be as much as an order of magnitude higher than that for bulk silicon devices. [1] A model was thus constructed to examine the heating and cooling of such an SOI structure.

### II. The Model

The model "device" used in the simulations was drawn in ANSYS Design Modeler © and is a buried N+ doped resistor in an SOI structure. As shown in Fig.1 and Fig. 2, the N+ resistor resides in a P- doped epitaxial layer over buried oxide (BOX) and a P+ doped substrate with copper back metal. A thick oxide covers the epitaxial layer. N+ plugs contact the resistor, and metal contacts connect the resistor to mock pads with simulated bond wires. The structure is surrounded by an oxide-filled trench.

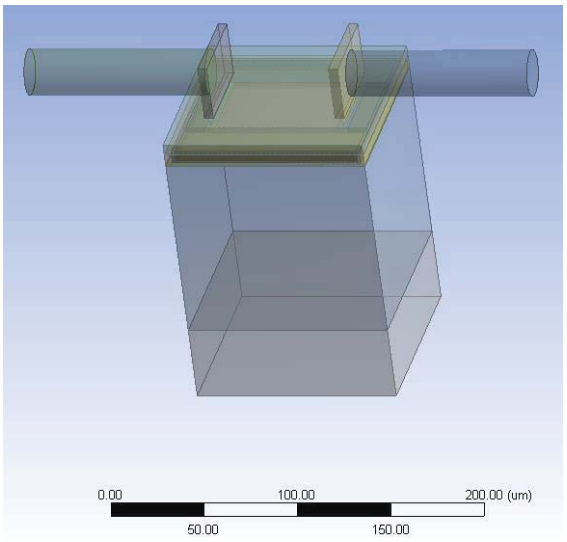



Fig. 1. The test structure

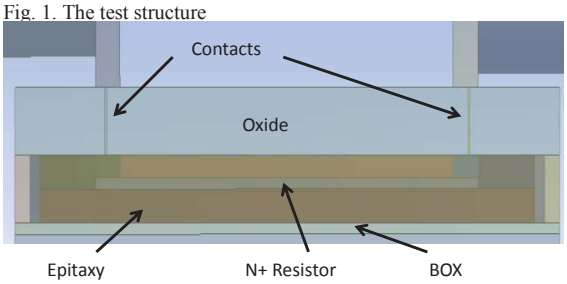



Fig. 2. Test Structure Cross-Section

### III. Experimentation

Using ANSYS Mechanical © 15.0, static ("DC") and transient thermal-electrical simulations were run to examine the relationship between the temperature response in the resistor versus four model parameters:

- Current applied
- BOX thickness
- Contact material

- Contact opening area
- Substrate thickness

For the simulations, a current was applied to one bond wire while the other wire was set to ground. A temperature of 30c was applied to the far ends (ie: "the lead frame end") of both bond wires and to the bottom of the copper back metal.

## IV. DC Results

In all simulations, it is seen that the temperature reaches its maximum value in the center of the resistor and radiates outward (Fig. 3). In the first experimental simulations, the applied current was varied from 50mA to 500mA. As expected, the temperature rose with increased current.

Of more interest were the results of simulations varying the thickness of the buried oxide. The BOX was increased from 0.1um to 1.5um in 1000A steps. Increased BOX thickness resulted in greater retention of heat in the resistor and surrounding epitaxial layer. Thinner BOX permitted more of the heat to be dissipated through the P+ substrate and away from the resistor. The maximum temperature as a function of BOX thickness is shown in Fig. 5 and is seen to follow a second-order polynomial. This is consistent with previous research showing thermal resistance to be proportional to the square root of the BOX thickness. [2][3][4]

The next question examined was whether the contact material would significantly impact the heat dissipation. Three contact metals were modeled, aluminum, tungsten, and copper. As shown in Table 1, the contact material had little effect on the maximum temperature of the device. Al and W contacts behaved nearly identically, and the Cu contacts dissipating slightly more heat.

TABLE 1. Temperature for Various Contact Materials

| Contacts | Al | Cu | W |
|---|---|---|---|
| Max Temp | 228.24 | 219.66 | 227.8 |

This is consistent given the nearly identical thermal conductivities of Al and W and the higher conductivity of Cu.

Simulations increasing the contact area also had minimal impacts to the maximum temperatures seen in the device. A doubling of the total contact area (using aluminum contacts) yielded only a few degrees drop in maximum temperature, and subsequent increases in area yielded smaller reductions (Fig. 6).

One final parameter examined was the thickness of the underlying P+ silicon substrate. Would thinning the substrate, thereby reducing the path of resistance to the back metal heat sink, result in significant heat dissipation?

The substrate thickness was varied from 25um to 150um in 25um intervals with the temperature results shown in Fig. 7.

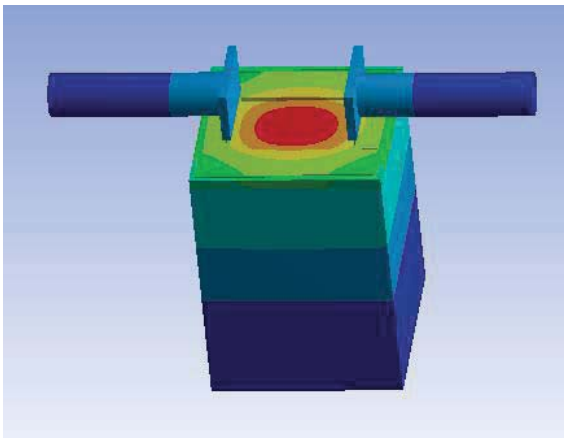


Fig. 3. Example result showing "hot spot" in the center.

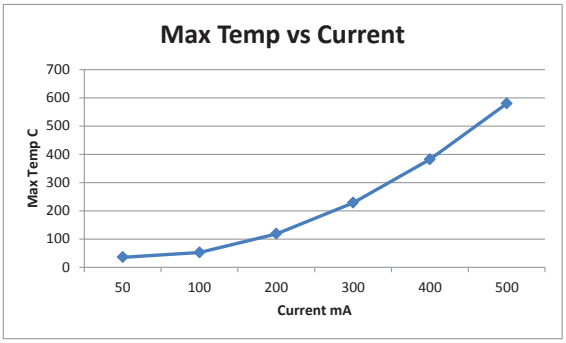



Fig. 4. Maximum temperature as a function of DC current

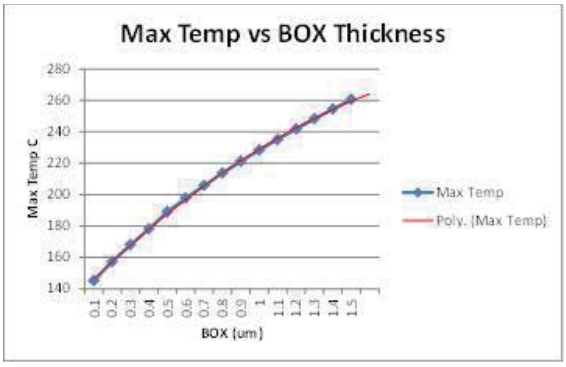



Fig. 5. Maximum temperature as a function of BOX thickness with polynomial trend line

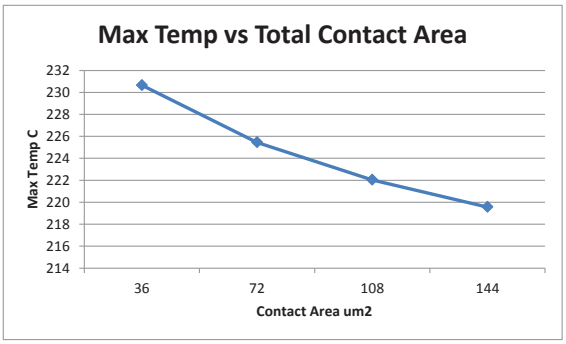



Fig. 6. Maximum temperature as a function of Contact Area

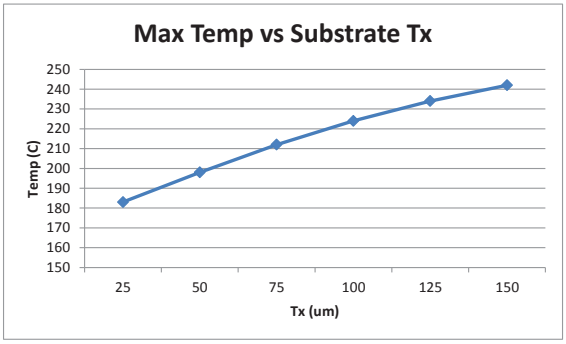



Fig. 7. Maximum temperature as a function of P+ Substrate Thickness

## V. Transient Results

The analysis type was then changed to "transient" to look at the overall temperature response over time as these same parameters were exercised.

In the transient analyses, a 300us pulse of current as applied to the test structure in the same manner as described for the DC analysis. The applied current was again varied from 50mA to 500mA to observe the predicted temperature response. For each iteration of current, the temperature is seen to spike up to about two-thirds of the way to the maximum value in the first few micro-seconds before rising more slowly to its maximum value. Once the current is shut off, the temperature ramps down quickly in the initial micro-seconds and tapers down to room temperature within 200us.

Fig. 9 shows the temperature response as a function of BOX thickness. While thinner BOX thickness results in more heat dissipated through the BOX to the substrate, and thus lower temperature in the resistor, there is no indication that the BOX thickness has any significant impact on the rate of cooling of the resistor once the current is removed.

As was seen in the DC models, the contact area and contact material had little impact on the temperature response of the device (Fig. 10a and 10b).

As with the other parameters, transient analysis was performed with varying thicknesses of P+ substrate. The thickness was again varied form 25-150um in 25um intervals. The results, depicted in Fig. 11, show the temperature variation seen in DC analysis and roughly identical rates of heating and cooling regardless of thickness.

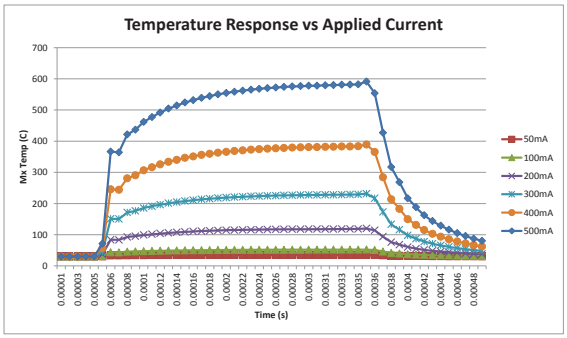



Fig. 8. Temperature Response versus Current

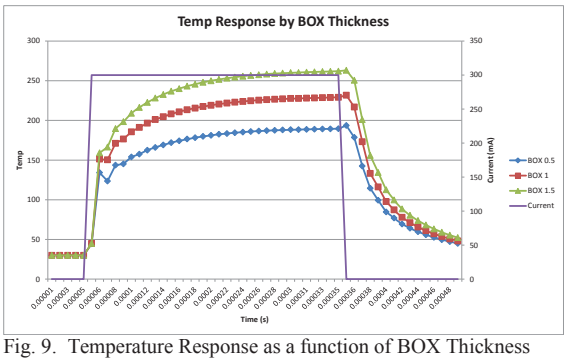
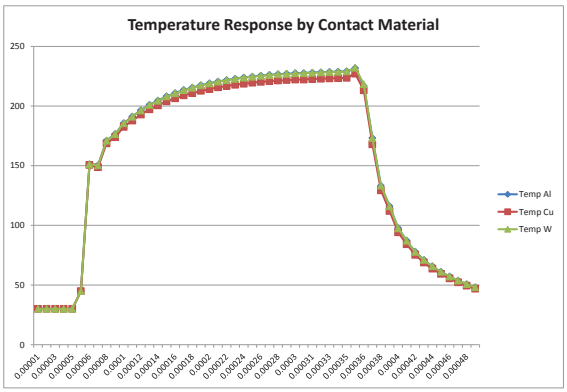



Fig. 9. Temperature Response as a function of BOX Thickness



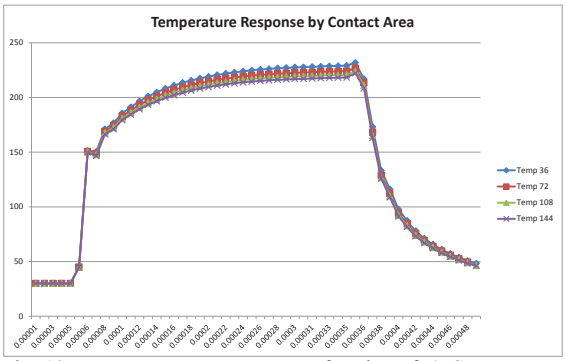




Fig. 10. Temperature Response as a function of a) Contact Material and b) Contact Area

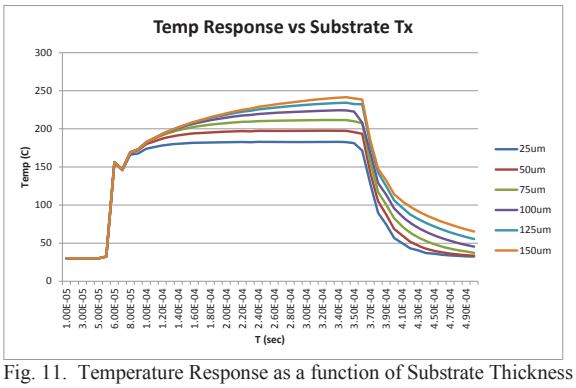



Fig. 11. Temperature Response as a function of Substrate Thickness

## VI. SAFE OPERATING AREA

Given the results of these analyses, it would only follow that one could also perform FEA in an effort to predict safe operating areas.

Single pulses of 1us were applied to the geometry to determine the maximum allowable current under which the device would not exceed a predetermined temperature (125c for this example). The max allowable current was determined to be 525mA as shown in Fig. 12.

## VII. CONCLUSIONS AND FURTHER DISCUSSION

It is seen that finite element analysis (FEA) can be used to predict device behavior at wafer and die level , thereby alleviating the need to fabricate test silicon costing thousands of dollars and reducing cycle time of results from weeks to hours.

Of the physical device parameters examined for this SOI device structure, BOX thickness and P+ substrate thickness clearly have the greatest impacts in terms of device heating and cooling. Future work should center around refining the model and optimizing the device design in terms of these two parameters. Contact material and contact area, on the other hand, were seen to have only negligible impacts.

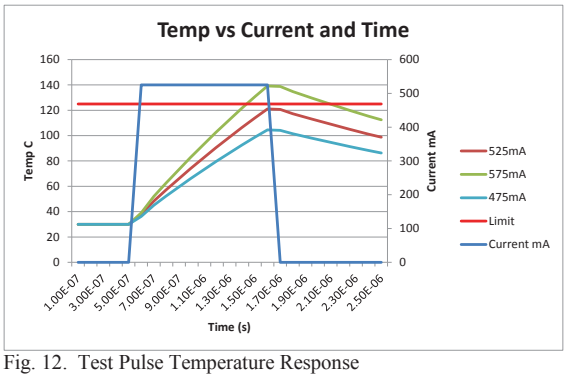



Fig. 12. Test Pulse Temperature Response

## ACKNOWLEDGMENT

The author gratefully acknowledges several contributors to this paper - Carroll Casteel, Mark Griswold, and Mark Nelson of ON Semiconductor for guidance in the direction of the research and review of the analyses; Roger Stout and Dave Billings, also of ON Semiconductor, for training assistance with the Design Modeler and Mechanical software; and John Higgins and Bill Bulat of ANSYS for technical assistance with aspects of the modeling.

## REFERENCES

[1] Pop, et al. Energy Dissipation and Transport in Nanoscale Devices. This article is published with open access at Springerlink.com. 2009.

[2] Raskin JP. Silicon-on-insulator MOSFETs models in analog/RF domain. INTERNATIONAL JOURNAL OF NUMERICAL MODELLING: ELECTRONIC NETWORKS, DEVICES AND FIELDS Int. J. Numer. Model. 2014; 27:707–735

[3] Andrieu F, Weber O, Mazurier J,Thomas O, Noel J-P, Fenouillet-Béranger C, Mazellier J-P, Perreau P, Poiroux T, Morand Y,Morel T, Allegret S, Loup V,Barnola S, Martin F, Damlencourt, JF, Servin I, Casse M, Garros V, Rozeau O, Jaud M-A, CibrarioG, Cluzel J, Toffoli A, Allain F, Kies R, Lafond D, Delaye V, Tabone C, Tosti L, Brevard L, Gaud P, Paruchuri V, Bourdelle, KK, Schwarzenbach W, Bonnin O, Nguyen BY, Doris B, Boeuf F, Skotnicki T, Faynot O. Low leakage and low variability ultrathin body and buried oxide (UT2B) SOI technology for 20nm low power CMOS and beyond. 2010 Symposium on VLSI Technology (VLSIT), 2010; 57–58.

[4] Su, Chung, Antoniadis, Goodson, and Flik. Measurement and Modeling of Self-Heating in SOI NMOSFET's. IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 41. NO. I . JANUARY 1994.

# Conductivity type switching in semiconductor nanowires

Ashkhen Yesayan
Institute of Radiophysics and Electronics, NAS RA,
0203 Ashtarak, Armenia
ashye@irphe.am

Stepan Petrosyan
Russian-Armenian (Slavonic) University, Yerevan,
Institute of Radiophysics and Electronics,
Ashtarak, Armenia

Fabien Prégaldiny
ICube, Université de Strasbourg - CNRS,
67412 Illkirch Cedex, France

***Abstract*—The radius dependent n-p conductivity type switching in semiconductor NWs occurred due to the high density of surface traps is theoretically analyzed. The analytical model is derived for the potential and charge distribution in NWs affected by surface traps. The results are validated with numerical solution of Poisson equation including fixed charges and both type of mobile charges (electrons and holes). The results are compared also with available experimental data.**

***Keywords—Nanowires, p-n switching, surface traps, Poisson equation***

## I. INTRODUCTION

Nanowires (NWs) currently are one of the most implemented structures in CMOS and non CMOS applications: field-effect transistors, sensors, solar cells, photo-detectors, switches. The NW structures have unique properties which are not essential in bulk or thin film semiconductors. Due to the large surface-to-volume ratio the surface traps may play very important role in electrical characterization of NWs [1-4]. Moreover recently it was experimentally approved that due to the surface traps the conductivity can be controlled by the variation of NW diameter and at certain wire diameter the conduction type of NW changes from p- to n-type [5]. Thus in general NW underlies surface morphology and size-dependent tunable electronic properties.

The appearance of p- to n-type switching effect in a single NW controlled by surface roughness or states can be achieved by different ways. For instance, partially covering the surface of a compound NW with wide band-gap passivation layer, to avoid the NW depletion in this covered part [6], and leaving the rest of the NW surface length free of this layer thus influenced by surface traps and external factors, e.g. chemicals. This type of NW p-n-switching diodes can serve as sensitive sensors. Other way to modulate surface roughness causing p-n- switching in NW is the sharp modulation of the NW radius. However, for accurate design the dependence of NW characteristics on surface trapped charges should be well described. Recently several methods were proposed to model the influence of interface traps on NW based device characteristics [3,4], but neither of them is accounted for minority carriers formation in NW channel.

In this paper we will theoretically study the phenomena of surface traps induced space charge penetration into the NW volume resulting for the small diameters to the full depletion and leading to the inversion in conductivity type.

## II. ANALYTICAL ANALYZES OF P-N-SWITCHING IN NWS

We consider n-type NW with radius (R) and acceptor type surface traps. All donor impurities in NW volume are assumed to be fully ionized. Surface active states trapped electrons from NW volume over the existing near-surface band bending. Therefore, the depletion layer forms near the surface which may spread deep inside the NW. When NW radius is larger than the thickness of near surface space charge layer the main contribution to NW conductivity is given by majority carriers from quasi-neutral n-channel near the NW core. The surface traps' effect becomes more pronounced for smaller diameters and large density of surface states when the NW becomes fully depleted and intrinsic conductivity is predicted. By further reducing the NW radius although all the mobile electrons from NW volume were transferred to the surface states they can fill the acceptor like surface traps only partially, and the remaining part of surface traps start to capture electrons from valence band at given temperature. Consequently, the density of holes increases near the surface and for some critical radius the total number of holes in the whole volume of NW can be more than the total number of electrons (so an inversion and conductivity type switching becomes possible). To analyze the conductivity variation with NW parameters at high density of surface states ($N_s$) the Poisson equation with consideration of both type of mobile charges and ionized donors should be solved. The surface trapped charge will be reflected in Neumann boundary condition (BC). We consider NWs with very high aspect ratio, so that only radial distribution of potential is important and we consider 1D Poisson equation:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \varphi}{\partial r}\right) = -\frac{q}{\varepsilon_{sc}}(N_D - n(r) + p(r)), \qquad (1)$$

where  is the electrostatic potential, $q$-is an elementary charge, $\varepsilon_{sc}$ is the semiconductor permittivity, $N_D$ is the uniform donor concentration, $n(r)$ and $p(r)$ are electron and hole concentrations, respectively. As a reference point we chose the position of intrinsic Fermi level in a deep volume of thick NW. Then the Fermi level is defined as $E_F = kTln(N_D/n_i)$, where $kT$ is the thermal energy and $n_i$ is the intrinsic concentration. We assume that the effective density of states for electrons and holes in conduction and valence bands are almost the same. Thus the concentrations of electrons and holes under the assumption of Boltzmann statistics are

$$n(r) = N_D \exp\left(\frac{e\varphi(r)}{kT}\right), \quad (2)$$

$$p(r) = \frac{n_i^2}{N_D}\exp\left(-\frac{e\varphi(r)}{kT}\right). \quad (3)$$

Now by susbstituting (2) and (3) into (1) and by defining normalised variables as: $x = r/R$, $u(x) = \frac{e\varphi(x)}{kT}$, we get the unitless form of Poisson equation:

$$\frac{1}{x}\frac{\partial}{\partial x}\left(x\frac{\partial u}{\partial x}\right) = K\rho(u), \quad (4)$$

Where $K = \frac{q^2 N_D R^2}{\varepsilon_{sc} kT}$ and $\rho(u) = \left(e^u - \frac{n_i^2}{{N_D}^2}e^{-u} - 1\right)$.

In this stage of development we consider single discrete levels of surface traps. The occupation probability of interface traps is defined as [7]: $f(E_t) = \frac{1}{1+\exp\left((E_t - E_F)/kT\right)}$. The ionization energy of traps is determined as $E_s = E_c(R) - E_t$, and bearing in mind that $\frac{E_c(r)-E_F}{kT} = \frac{N_c}{N_D}\exp(-e\varphi(r)/kT)$ the density of trapped electrons on the surface in unitless variables can be written as follows:

$$n_s = \frac{N_S}{1+\frac{N_c}{N_D}\exp\left(-u(1)-\frac{E_S}{kT}\right)} \quad (5)$$

The Neumann boundary conditions in terms of normalized variables in the center of NW and on the surface, respectively, are defined as follows: $\left.\frac{\partial u}{\partial x}\right|_{x=0} = 0$ and $\left.\frac{\partial u}{\partial x}\right|_{x=1} = -\frac{K}{N_D R}n_s$.

The above form of Poisson equation does not admit to any closed form analytical solution. The exact solution of (4) with defined BCs can be done only numerically. Instead an approximate solution can be obtained using regional approach.

### *A. Aproximate Analitical Solution*

To derive the analytical solution for Poisson equation we rely on the linearization of the electric potential in the regions where appreciable content of mobile charges (electrons or holes) is present. This method was already used to solve the Poisson equation in [8], with taking into account only electronic mobile charge whereas in our case we should take into account also the holes.

We use a regional approach which divides the electrostatics of NW into three regions along the NW radius and apply different simplifying assumptions for each regions. First we consider an inversion region close to the surface ($x_1 \le x \le 1$) where holes are the majority of mobile charges and electronic mobile charge is negligible, so $\rho(u) = \left(-\frac{n_i^2}{{N_D}^2}e^{-u} - 1\right)$, then follows the region $x_o \le x \le x_1$ where the mobile charges are assumed to be negligible and the full depletion approximation is applicable $\rho(u) = -1$, finally in the third region close to the center of NW $0 \le x \le x_o$, where the mobile charge mainly consists from electrons: $\rho(u) = (e^u - 1)$. The coordinates $x_o$ and $x_1$ are variables which can be defined self-consistently by solving the above described system of equations imposing the continuity of solution at these points. The position of these points depend on NW parameters $(R, N_D, N_s)$ and even the situation can occur when they are not within the NW at all, which means that the NW behaves like a p-type semiconductor.

The potential distribution in the middle region where the full depletion approximation is applicable can be derived easily. Whereas to get the closed form solution for the other two regions we expand exponential terms in $\rho(u)$ into the Taylor series close the most important points.

For the first region: $x_1 \le x \le 1$, by expanding $e^{-u}$ around its value at the surface $e^{-u(1)}$ we got:

$$\rho(u) = \frac{n_i^2}{{N_D}^2}e^{-u(1)}\cdot u(x) - \frac{n_i^2}{{N_D}^2}e^{-u(1)}\big(1+u(1)\big) - 1. \quad (6)$$

For the third region: $x_0 \le x \le 0$, by expanding $e^u$ around its value at the center of NW we got:

$$\rho(u) = e^{u(0)}\cdot u(x) + e^{u(0)}\big(1-u(0)\big) - 1. \quad (7)$$

Finally between these two regions, for $x_o \le x \le x_1$, there is a region of full depletion: $\rho(u) = -1$.

The continuity of $\rho(u)$ imposes:

$$u(x_1) = 1 + u(1), \quad (8)$$

$$u(x_o) = u(0) - 1. \quad (9)$$

Thus the Poisson equation (4) should be solved with right hand side defined by (6-7) and with the following boundary conditions:

$$\left.\frac{\partial u}{\partial x}\right|_{x=1} = -\frac{K}{N_D R}n_s \quad (10)$$

$$\left.\frac{\partial u}{\partial x}\right|_{x=0} = 0. \quad (11)$$

This set of equations allow us to get the continues potential distribution in a radial direction throughout the whole NW. Meantime we should take into account that the points $x_1$, $x_0$ are floating and so the BC (11) should be fulfilled for all three regions.

By substituting (6) into (4) we got the following expression for the normalized potential:

$$u(x) = 1 + u(1) + \frac{{N_D}^2}{n_i^2}e^{u(1)} - \left(\frac{{N_D}^2}{n_i^2}e^{u(1)} + 1\right)\frac{I_o(\sqrt{A_1}x)}{I_o(\sqrt{A_1})} \quad (12)$$

where $x_1 \le x \le 1$, $A_1 = K\frac{n_i^2}{{N_D}^2}e^{-u(1)}$ and $I_o$ is the modified Bessel function of the first kind.

Further we calculate the electric field at the surface from (12) using BC (10) and got the following equation for the surface potential $u(1)$:

$$\left(\frac{N_D}{n_i}e^{\frac{u(1)}{2}} + \frac{n_i}{N_D}e^{-\frac{u(1)}{2}}\right)\frac{I_1(\sqrt{A_1})}{I_0(\sqrt{A_1})} = \frac{qN_S}{\sqrt{N_D\varepsilon_{sc}kT}}\frac{1}{1+\frac{N_C}{N_D}e^{\left(-u(1)-\frac{E_S}{kT}\right)}}. \quad (13)$$

By substituting (8) into (12) we define the equation from where $x_1$ can be calculated:

$$I_0\left(\sqrt{A_1}x_1\right) = \frac{I_0(\sqrt{A_1})}{1+\frac{n_i^2}{{N_D}^2}e^{-u(1)}}. \quad (14)$$

In the region fully depleted from mobile charges $x_o \le x \le x_1$, using (8) and (11), the $u(x)$ takes the form:

$$u(x) = \frac{K}{4}({x_1}^2 - x^2) + u(1) + 1. \quad (15)$$

By substituting (7) into (4), and considering (11) and (9) we determine the expression for normalized potential in the $x_0 \le x \le 0$ region:

$$u(x) = u(0) - 1 + e^{-u(0)} + \left(1 - e^{-u(0)}\right)I_o\left(\sqrt{K}e^{\frac{u(0)}{2}}x\right) \quad (16)$$

From (9) and (15) we specify the expression for $u(0)$:

$$u(0) = \frac{K}{4}({x_1}^2 - {x_o}^2) + u(1) + 2. \quad (17)$$

Further by substituting (17) and (9) into (16) we define the equation to calculate $x_o$:

$$e^{-u_0} = (e^{-u_0} - 1)I_o\left(\sqrt{K}e^{\frac{u_0}{2}}x_o\right). \quad (18)$$

The derived equations (12), (15) and (16) describe the potential distribution along the NW radius.

## III. Model Validation and Discussion

To validate the accuracy of the derived approximate solution we numerically solve (1) with its boundary conditions in Wolfram Mathematica and compare our analytical calculations with these data. The comparison of analytical and numerical calculations are shown in Fig. 1. The potential distributions for NWs with different diameters are depicted. Calculations are done for GaAs NWs with radii varying from 10nm to 120nm. Doping density is set to $N_D = 10^{17}\text{cm}^{-3}$. We consider discrete surface trap level located close to mid-gap. The density of surface traps is set to $N_s = 10^{12}cm^{-2}$. It is seen that the effect of surface traps becomes relevant especially for NWs with smaller radii. As smaller is the radius of NW as higher is central potential by its absolute value. For NWs with R=30nm and less the central potential even is higher than the surface potential of NWs with radii larger than 100nm.

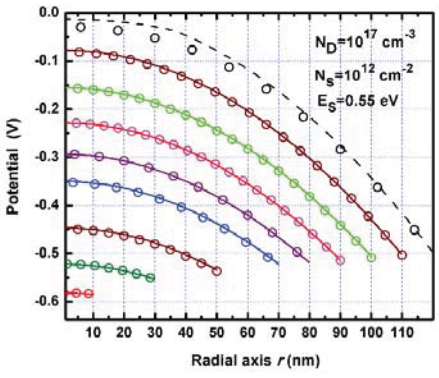



Fig. 1. Potential distribution in radial direction for NWs with radiuses varying from 10nm to 120nm. Lines: approximated analytical model, circles: numerical calculations.

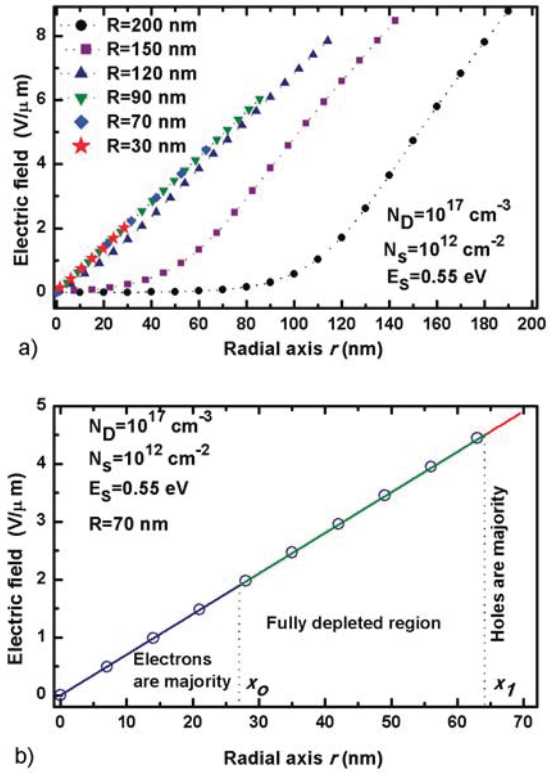



Fig. 2. Electric field in NWs with different radii calculated from exact solutions in Wolfram Matematica (a). Electric field in NW with 70 nm radius, line: analytical model, circles: numerical calculations.

It is seen that the developed analytical model well predicts the potential distribution over the large range of NW radii. The mismatch between the analytical and numerical calculations occurs only for NWs with R=120nm and more. However, NWs with such large radii are not in our interest as the p-n-switching effect cannot occur at these diameters. It is seen that when the NW radius is larger than 100nm at given parameters ($N_D$, $N_s$) the central part of NW is not influenced by surface traps (see Fig. 1) and there is a quasi-neutral channel in the core, which provides the n-type conductivity. This situation is more observable in Fig. 2 (a), where the electric field in NWs is calculated from accurate solutions of (1) in Wolfram Mathematica for different NWs radii. It is seen that for NWs with radii $R$=150, 200nm the electric field is already zero far away from the NW center, thus only a shallow space-charge depletion results from the surface states and the central part of NW is not affected. Whereas for NWs with R<100nm the depletion region covers the total nanowire at given parameters.

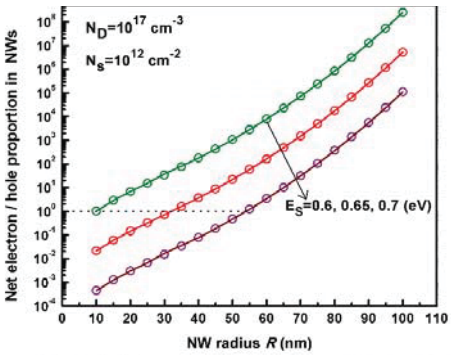



Fig. 3. Net electron/hole ratio versus NWs radii calculated at different trap energies. Circles: numerical calculations, lines: derived analytical model.

To confirm that the derived regional approach is accurate also for derivatives we plot the electric field calculated analytically from (12), (15) and (16) as $E = -\frac{\partial \varphi}{\partial r}$ and then compare with numerical data. The calculations for NW with $R$=70nm are illustrated in Fig. 2(b). The dotted lines show the positions of $x_o$, $x_1$, calculated using (14) and (18), and divide the NW into three regions: the region close to the surface where the holes are already majority, the fully depleted region and the region inhabited with electrons close to NW center. It is evident that the approximate analytical model is accurate, continues and well predicts not only the potential distribution but also the electric field and consequently the charge distribution in NW. Once the analytical model is validated, to calculate the distribution of electrons and holes we substitute the derived potential profile in the exponential terms of (2) and (3). The conductivity type of uniformly doped bulk semiconductor can be described by referring to mobile charge local concentration. But speaking about the NW conduction type we cannot define it referring simply to mobile carriers' local concentration, as the carrier concentration, even at uniform doping density, can have a great variation from the surface to the NW center due to large band bending effect. Thus to define the conduction type of NW we should compare the integrated concentrations of electrons and holes over the NW radius or in other way we have to inspect the sign of the total mobile charge. The ratio of net mobile electrons over the net holes in NWs calculated for the radii varying from 10nm to 100nm is illustrated in Fig. 3. Calculations are done by

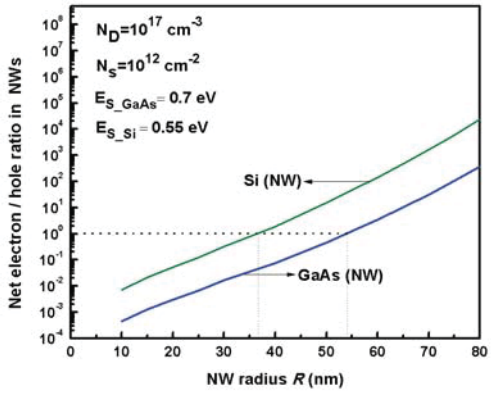



Fig. 4. Net electron/hole ratio calculated for Si and GaAs NWs with derived analytical model versus NWs radii.

TABLE 1. COMPARISON OF DATA FROM [5] AND OUR CALCULATIONS

| Conduction type | p- type | Ambipolar | n-type |
|---|---|---|---|
| Experimental data, GaAs NW FE [4] | R≤20nm | 20nm<R<40nm | R>40nm |
| Analytical model ($E_s$≈0.65eV) | R<20nm | 20nm<R<50nm | R>50 nm |

considering single energy surface trap levels with ionization energy close to mid-gap: $E_s = 0.7, 0.65, 0.55$ (eV). It is seen that the traps located at mid-gap are more effective, which is in accordance with existing literature [7]. For the given NW radius the ratio of electrons over the holes changes almost $10^3$ times by varying the ionization energy with 0.1 eV (see Fig.3). The dotted line corresponds to the case when the net number of electrons and holes are equal. Following up with $E_s = 0.7$eV curve we see that at given parameters holes are majority in NWs with radii less than 35nm, and at 20nm we already have a p-type conductivity. This is in a good agreement with experimental data [5], where p-type conductivity was observed for NWs with diameter less than 40nm. It is worth to note that in our calculations we chose the material and doping density in accordance with [5]. The comparison of the data from [5] and our calculations is presented in Table 1.

However, the impact of surface traps effect on NW conductivity depends also on NW material. In Fig. 4 we compare GaAs and Si NWs with the same doping concentration, density of surface states and assuming traps energy located close to mid-gap: $E_s = 0.55$ eV for the Si NW and $E_s = 0.7$eV for GaAs NW. It is seen that Si NW is less affected by surface roughness as it was expected.

In conclusion, in this work we discussed the mechanism of n-p- switching in NWs due to the existence of high density surface traps capturing electrons from the NW volume. The developed theory of n-p switching allows to perform hands-on calculations to estimate the dependence of conductivity type on NW parameters, particularly on NW radius.

## REFERENCES

[1] H. Y. Chen, R. S. Chen, F. C. Chang, L. C. Chen, et al., "Size-dependent photoconductivity and dark conductivity of m-axial GaN nanowires with small critical diameter," J. Appl. Phys. Lett., vol. 95, p.143123, 2009.

[2] S. Petrosyan, A. Yesayan, S. Nersesyan, "Photocurrent relaxations and gain in semiconductor nanowires," DOI: 10.1117/12.2180885 Proc. SPIE, vol. 9440, 2014.

[3] A.C. E. Chia and R. LaPierre, "Analytical model of surface depletion in GaAs nanowires," J. App. Phys., vol. 112, no. 6, p. 063705, 2012.

[4] Z. Chen, X. Zhou, G. Zhu, and S. Lin, "Interface-trap modeling for silicon-nanowire MOSFETs," in Reliability Physics Symposium (IRPS), May 2010, pp. 977-980.

[5] N. Han, F. Wang, et al. "Controllable p-n switching behaviors of GaAs nanowires via an interface effect," ACS Nano, vol. 6, no. 5, pp. 4428–4433, 2012.

[6] R.R. LaPierre, A.C.E. Chia, C.M. Haapamaki, N. Tajik, et al., "Passivation of III-V nanowires for optoelectronics," ECS Trans., vol. 45, no 5, pp. 51-60, 2012.

[7] S. M. Sze, K. K. Ng, "Metal-Insulator-Semiconductor Capacitors," in Physics of semiconductor devices, 3rd ed., J. Wiley & Sons, Inc., Hoboken: New Jersey, 2007, pp. 214-215.

[8] E. Gnani, A.Gnudi, S. Reggiani, G. Baccarani, "Theory of the Junctionless Nanowire FET," IEEE Trans. Electron Devices, vol.58, no. 9, pp. 2903-2910, 2011.

# Fabrication and Characterization of InGaAs-on-insulator Lateral N+/n/N+ Structures

L. Czornomaz, V. Djara, V. Deshpande, D. Caimi, L. Pirro[1], S. Cristoloveanu[1] and J. Fompeyrine
IBM Research – Zurich, Säumerstrasse 4, CH-8803 Rüschlikon, Switzerland
[1]IMEP-LAHC, Grenoble INP Minatec, France
*Email: luk@zurich.ibm.com*

**Abstract – Lateral N+/n/N+ InGaAs-on-insulator structures are successfully fabricated by direct wafer bonding and selective regrowth. Electrical characterizations are performed for varying n-layer thickness from fully-depleted films up to the limit of partial depletion. Measurements under externally applied uniaxial tensile strain show an improved drive current.**

## 1. Introduction

High-mobility channel materials such as Ge, SiGe and InGaAs are leading candidates to deliver the necessary power-performance benefits and added functionalities for future CMOS technologies and System-on-Chip applications (SoC). InGaAs-on-insulator layers are one possible approach [1] to integrate high-performance InGaAs FinFETs on Si [2] or realize hybrid InGaAs/SiGe CMOS circuits [3]. Nevertheless, those layers might suffer from additional carrier scattering compared to layers on bulk crystalline buffers such as InP [4] or InAlAs [5] owing to the presence of the back-side channel interface with the BOX. In this work, we fabricate and characterize lateral N+/n/N+ structures on InGaAs-on-insulator layers to mimic the channel transport of a MOSFET while minimizing the impact of process induced damages. The effect of InGaAs layer thickness and uniaxial tensile strain on transport characteristics are investigated.

## 2. Device fabrication

The lateral N+/n/N+ fabrication process mimics some of the key features of our InGaAs FinFETs process [3], such as obtained results are representative of what is expected in fully-processed devices. The n-layer is a non-intentionally doped InGaAs-on-insulator (InGaAs-OI) grown in a metalorganic vapor phase epitaxy reactor, with a background Hall carrier concentration of 2-3×$10^{16}$ $cm^{-3}$. InGaAs-OI layers on Si ($N_A$ = 2×$10^{17}$ cm-3) are prepared by direct wafer bonding of nominally-undoped $In_{0.53}Ga_{0.47}As$ films of varying thickness (25 nm, 50 nm, 100 nm and 200 nm) grown on InP wafers as described in [6]. The BOX consists of 25 nm thermal $SiO_2$, 10 nm $Al_2O_3$ and the high-k dielectric stack used in [2], for a resulting $C_{ox}$ of 0.11 µF/$cm^2$.

The fabrication of lateral N+/n/N+ structures starts with the deposition of a $SiO_2$ hardmask to define the length of the n-region (Fig. 1(a)). Sn-doped $In_{0.53}GaAs$ N+ regions ($N_D$ = 5x$10^{19}$ $cm^{-3}$) are selectively grown (Fig. 1(b)) at low temperature as in [7]. The hardmask is removed (Fig. 1(c)) and a mesa isolation is performed by wet etching (Fig. 1(d)). The top interface of the n-region is formed with same high-k dielectric as used for the bottom interface. The process is completed by the deposition of a $SiO_2$ layer (Fig. 1(e)), contact holes and W contacts (Fig. 1(f)).

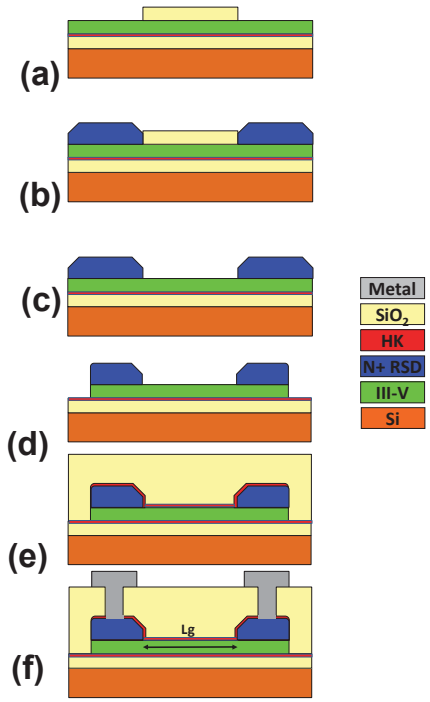



**Fig.1. Schematic of lateral N+/n/N+ test structure fabrication with (a) $SiO_2$ hardmask on InGaAs-OI layer with bottom passivation, (b) growth of N+ InGaAs, (c) hardmask removal, (d) mesa wet etching, (e) top passivation and interlayer dielectric deposition, (f) contact via and metallization.**

## 3. Electrical characterization and uniaxial strain

Back-channel measurements are carried out using the Si substrate as a back-gate. Transfer characteristics are reported in Fig. 2 for the three different InGaAs channel thickness. Although all structures present a modulation of the drain current with gate voltage, this modulation is reduced for thicker films. Indeed, the thinner channel thickness shows a clear behavior characteristic of a full-depletion of the channel with the steepest subthreshold swing, while the 200 nm thick InGaAs layers are at the limit of partial depletion since the drain current saturates for increasingly negative gate voltages. In addition, a dual $V_T$ (at $V_g$ = -3V and $V_g$ = 1 V) behavior can be observed for samples with an InGaAs thickness of 50 nm and above. By comparison, the 25 nm thick sample shows a regular single $V_T$ behavior.

ISBN 978-1-4673-8608-1  IEEE Catalog number CFP1649D-USB

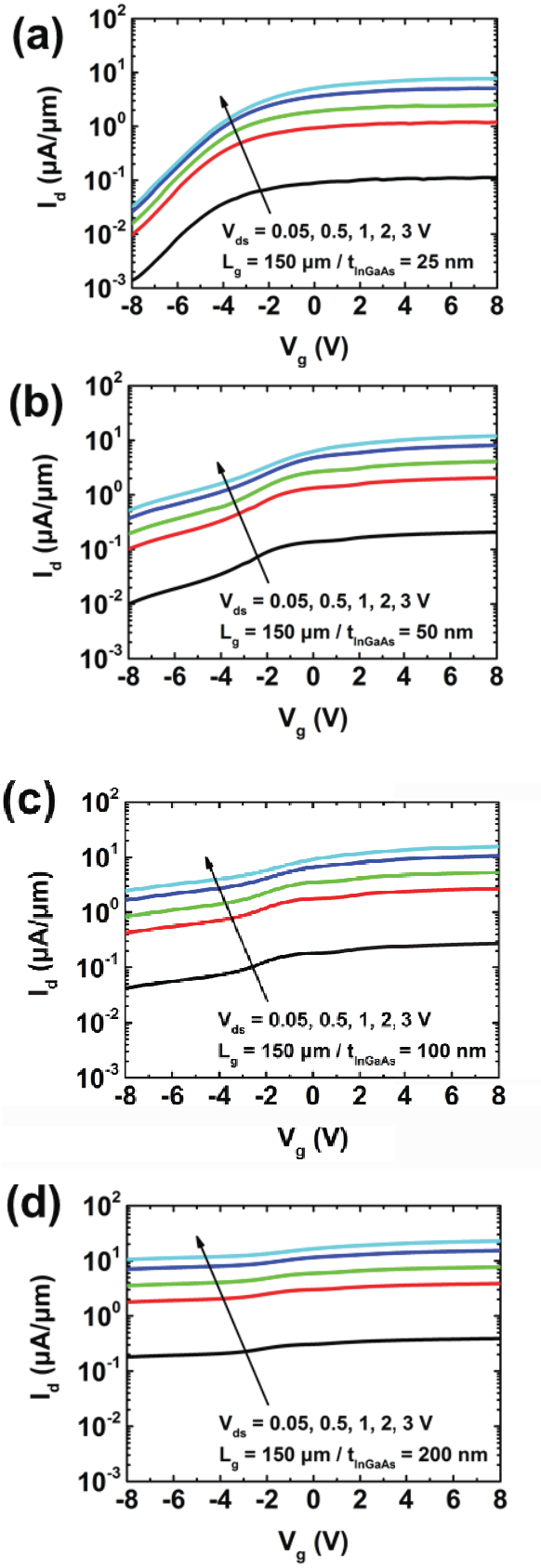



**Fig. 2. $I_d$-$V_g$ characteristics of lateral N+/n/N+ InGaAs-OI structures using the Si substrate as a back-gate, for (a) 25 nm, (b) 50 nm, (c) 100 nm and (d) 200 nm thick InGaAs.**

The improved full depletion of the channel for thinner InGaAs layers is further observed as a largely reduced subthreshold swing (SS) upon thickness scaling. SS is reported versus channel length for 4 different thicknesses in Fig. 3.

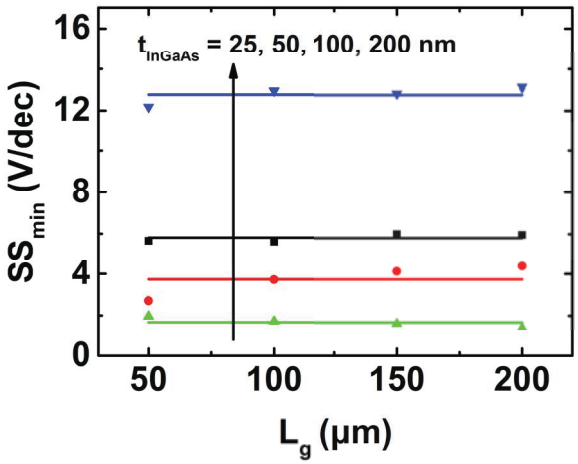



**Fig. 3. Subthreshold swing (SS) versus channel length ($L_g$) for devices with an InGaAs thickness of 25 nm, 50 nm, 100 nm and 200 nm.**

Fig. 4(a) shows the ON-resistance which varies linearly with the channel length. Extrapolation of this curve indicates that all samples have a similar contact resistance (about 5 kΩ.µm), which is low for an InGaAs-OI sample due to the optimized process of the source/drain terminals. The sheet resistance strongly depends on thickness as illustrated in Fig. 4(b). This dependence can be explained by the presence of two parallel conduction channels [8].

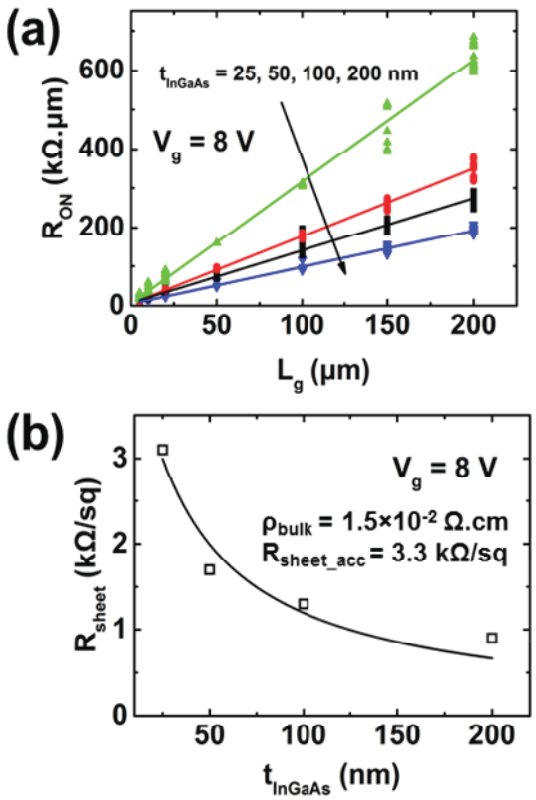



**Fig. 4. (a) $R_{ON}$ vs $L_g$ extracted at $V_g$ = 8 V and $V_{ds}$ = 50 mV for 4 different InGaAs-OI thickness. (b) $R_{sheet}$ from (a) vs InGaAs-OI thickness fitted by a two parallel conductance model.**

This dual-channel behavior also appears in the field effect mobility as two distinct mobility peaks located at two different $V_T$ for the thicker films, while the thinnest

InGaAs thickness only gives rise to a single mobility peak. The highest peak electron mobility reaches 1100-1200 cm$^2$/V.s for samples with a dual-channel behavior, while it is limited to about 500 cm$^2$/V.s for the 25 nm thick sample.

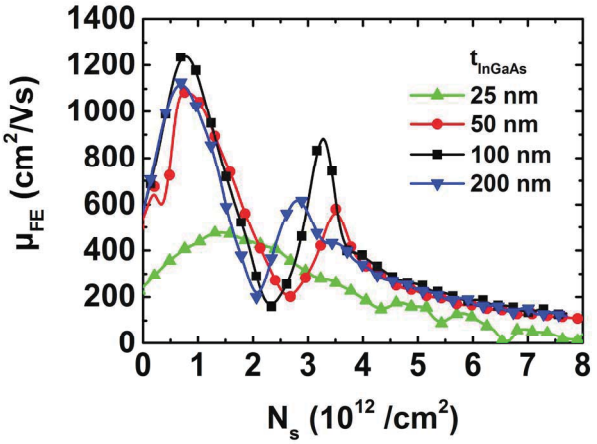



**Fig. 5. Field effect mobility versus estimated channel charge density calculated from the theoretical buried oxide capacitance and measured lowest $V_T$.**

Samples are diced in 2 cm x 3 mm pieces and mounted in a 3-point bending setup (Fig. 6) where uniaxial tensile strain can be applied up to 0.2 % (above, sample breaks). $I_{ON}$ is found to increase with increasing uniaxial tensile strain applied along the <110> transport direction, at a rate of 10-15% per percent of strain (Fig. 7).

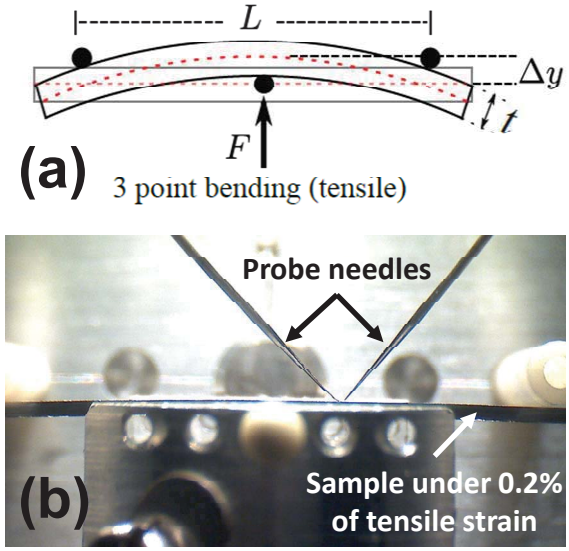



**Fig. 6. (a) Schematic of 3-point bending configuration to apply uniaxial tensile strain on the sample. (b) Picture from the side of the 3-point bending setup (as in (a)) showing the vended beam of Si under tensile strain and the contact probe needles.**

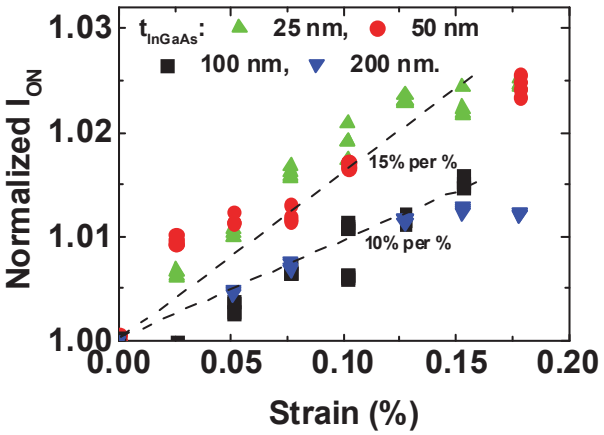



**Fig. 7. Relative change of $I_{ON}$ (at $V_g$ = 8 V) vs uniaxial tensile strain for 4 different InGaAs-OI thickness.**

## 4. Conclusion

Lateral N+/n/N+ InGaAs-on-insulator structures are successfully fabricated and show promising transport properties, with electron mobility above 1100 cm$^2$/V.s. Uniaxial tensile strain in the <110> transport direction increases on-current with a rate of 10-15% per percent of strain.

## 5. Acknowledgments

This work is supported by European projects COMPOSE$^3$ and III-V-MOS.

## 6. References

**[1]** L. Czornomaz, N. Daix, D. Caimi, M. Sousa, R. Erni, M. Rossell, M. El-Kazzi, C. Rossel, C. Marchiori, E. Uccelli, M. Richter, H. Siegwart, and J. Fompeyrine, "*An integration path for gate-first UTB III-V-on-insulator MOSFETs with silicon, using direct wafer bonding and donor wafer recycling*," Electron Devices Meeting (IEDM), 2012 IEEE International, p. 23.4.1, (2012), http://dx.doi.org/10.1109/IEDM.2012.6479088

**[2]** V. Djara, V. Deshpande, E. Uccelli, N. Daix, D. Caimi, C. Rossel, M. Sousa, H. Siegwart, C. Marchiori, J. Hartmann, K.-T. Shiu, C.-W. Weng, M. Krishnan, M. Lofaro, R. Steiner, D. Sadana, D. Lubyshev, A. Liu, L. Czornomaz, and J. Fompeyrine, "*An InGaAs on Si platform for CMOS with 200 mm InGaAs-OI substrate, gate-first, replacement gate planar and FinFETs down to 120 nm contact pitch*," VLSI Technology (VLSI Technology), 2015 Symposium on, pp. T176–T177 (2015),http://dx.doi.org/http://dx.doi.org/10.1109/VLSIT.2015.7223668

**[3]** L. Czornomaz, N. Daix, K. Cheng, D. Caimi, C. Rossel, K. Lister, M. Sousa, and J. Fompeyrine, "*Co-integration of InGaAs n- and SiGe p-MOSFETs into digital CMOS circuits using hybrid dual-channel ETXOI substrates*," Electron Devices Meeting (IEDM), 2013 IEEE International, pp. 2.8.1–2.8.4 (2013), http://dx.doi.org/10.1109/IEDM.2013.6724548

**[4]** N. Waldron, C. Merckling, W. Guo, P. Ong, L. Teugels, S. Ansar, D. Tsvetanova, F. Sebaai, D. van

Dorp, A. Milenin, D. Lin, L. Nyns, J. Mitard, A. Pourghaderi, B. Douhard, O. Richard, H. Bender, G. Boccardi, M. Caymax, M. Heyns, W. Vandervorst, K. Barla, N. Collaert, and A.-Y. Thean, "*An InGaAs/InP quantum well finfet using the replacement fin process integrated in an RMG flow on 300mm Si substrates*," VLSI Technology (VLSI-Technology): Digest of Technical Papers, pp. 1–2 (2014), http://dx.doi.org/10.1109/VLSIT.2014.6894349

**[5]** S. Lee, V. Chobpattana, C.-Y. Huang, B. J. Thibeault, W. Mitchell, S. Stemmer, A. C. Gossard, and M. Rodwell, "Record $I_{ON}$ (0.5 mA/μm at $V_{DD}$ = 0.5 V and $I_{off}$ = 100 nA/μm) 25 nm-Gate-Length $ZrO_2$/InAs/InAlAs MOSFETs," VLSI Technology (VLSI Technology), 2014 Symposium on, pp. 1–2 (2014), http://dx.doi.org/10.1109/VLSIT.2014.6894363

**[6]** L. Czornomaz, N. Daix, P. Kerber, K. Lister, D. Caimi, C. Rossel, M. Sousa, E. Uccelli, and J. Fompeyrine, "*Scalability of ultra-thin-body and BOX InGaAs MOSFETs on silicon*," Solid-State Device Research Conference (ESSDERC), 2013 Proceedings of the European, pp. 143–146 (2013), http://dx.doi.org/10.1109/ESSDERC.2013.6818839

**[7]** V. Deshpande, V. Djara, E. O'Connor, P. Hashemi, K. Balakrishnan, M. Sousa, D. Caimi, A. Olziersky, L. Czornomaz, and J. Fompeyrine, "*Advanced 3D Monolithic Hybrid CMOS with Sub-50 nm Gate Inverters Featuring Replacement Metal Gate (RMG)-InGaAs nFETs on SiGe-OI Fin pFETs*," Electron Devices Meeting (IEDM), 2015 IEEE International, pp. 8.8.1-8.8.4 (2015)

**[8]** L. Pirro, L. Czornomaz, H. J. Park, I. Ionica, M. Bawedin, V. Djara, V. Deshpande, and C. Cristoloveanu, "*Volume and interface conduction in InGaAs junctionless transistors*," Ultimate Integration on Silicon (EUROSOI-ULIS), 2016 Joint International EUROSOI Workshop and International Conference on, *accepted* (2016)

# Enhancing Electrical Performances of Metallic DG-SET based Circuits by Tunnel Junction Engineering

Khalil G. El Hajjam[a,b], Mohamed Amine Bounouar[a,b], Dominique Drouin[b], and Francis Calmon[a]
[a)] Institut des Nanotechnologies de Lyon, Université de Lyon, France
[b)] Laboratoire Nanotechnologies Nanosystèmes, Université de Sherbrooke, Québec, Canada
e-mail: khalil.el-hajjam@insa-lyon.fr

***Abstract*—The development of metallic Single Electron Transistor (SET) is extremely related to the downscaling and the electrical properties of its tunnel junctions. These tunnel junctions should insure high ON current, low OFF current and low capacitance. In this work, we propose an engineered tunnel junction based on multi-dielectric stacking to optimize the tunnel junction's characteristics. The optimized tunnel junction is demonstrated to increase $I_{ON}$ current and the $I_{ON}/I_{OFF}$ ratio in Double-Gate SET (DG-SET). DG-SET based elementary circuits are demonstrating enhanced electrical characteristics.**

***Keywords*—Single Electron Transistor, tunnel junction engineering, multi-layer dielectrics**

## I. Introduction

The operation of the Double-Gate Single Electron Transistor (DG-SET) is based on the quantification of the electric charge, the quantum transport and Coulomb repulsion. This new component exploits the phenomenon known as Coulomb blockade allowing the transit of electrons sequentially to precisely control the pumped flow. The granular nature of the electric charge in the transport of electrons by tunnel effect makes it possible to envisage the fabrication of low-power logic circuits in a high integration density. In addition to the miniaturization challenge, SETs have been known to have low driving current and low $I_{ON}/I_{OFF}$ ratio. In recent years, the emerging SET technology has been seen as a candidate to complement the ultimate CMOS. Moreover, the nano-damascene process is considered as a cool fabrication process that allows the co-integration of metallic SET in the BEOL with a low-power thermal budget (<450 °C) opening the way to the 3D integration [1]. In this paper, we propose to enhance the electrical performances of SET by means of its tunnel junction engineering. We demonstrate then the improved inverter's transfer function and the static noise margin (SNM) of DG-SET based SRAM cell.

## II. Simulation Methodology

### A. Crested barrier tunnel junctions

To demonstrate enhancing electric performances of DG-SET by its tunnel junctions' optimization, we chose to compare the two tunnel junctions described in Figure 1. The first tunnel junction is a composed of 4nm TiOx and the second one is composed of 3nm TiOx + 1nm $TiO_2$. The two materials have been chosen for their potential barrier height, in order to insure the conductance of tunnel current, but also for their dielectric constant difference. Figure 2 illustrates the comparison of simulated current trough a surface of $5nm^2$ for 4nm TiOx and 3nm TiOx + 1nm $TiO_2$ thick tunnel junctions. This junction is composed of 3nm plasma grown $TiO_x$ which has a low dielectric constant of 3.5 and a low barrier height of 0.32eV in addition to a 1nm ALD deposited $TiO_2$ with dielectric constant of 35 and a barrier height of 1eV (Figure2) [1-4].

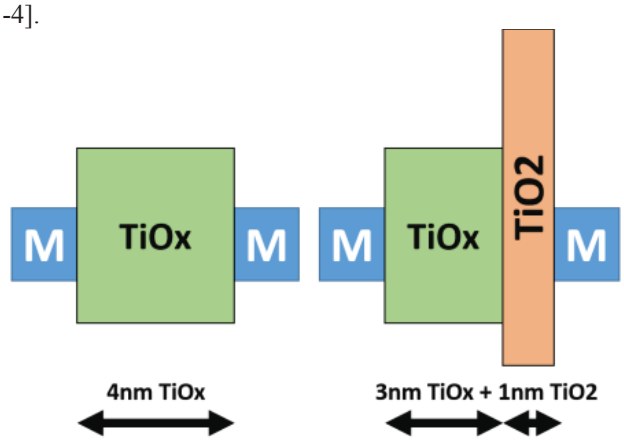



Fig.1: Energy Band Diagram schematic for the studied of 4nm TiOx and 3nm TiOx +1nm $TiO_2$ tunnel junctions.

Current-Voltage simulations were carried out using a Transfer Matrix Method based simulator [5]. The 4nm $TiO_x$ tunnel junction current characteristic allows high current at low applied potential ($I_{OFF}$), which is due to thermionic current surpassing the low potential barrier. On the other hand, the 3nm TiOx + 1nm $TiO_2$ tunnel junction however, improves the current level compared to the 4nm $TiO_x$ tunnel junction, at low and high applied potential. At low applied potential, the high potential barrier of $TiO_2$ allows blocking thermionic current and also decreasing the junction transparency reducing globally the $I_{OFF}$ current. By increasing the applied potential (starting from 0.5V), electric field, concentrated in the $TiO_x$ layer, lowers the $TiO_2$ potential barrier, and increases both tunnel and thermionic current (improved $I_{ON}$). Knowing that capacitance of this tunnel junction $C_j$=0.05aF, is close to the 4nm $TiO_x$ capacitance $C_j$=0.039aF, the crested tunnel junction composed of 3nm TiOx + 1nm $TiO_2$ is of great interest for SET based circuits.

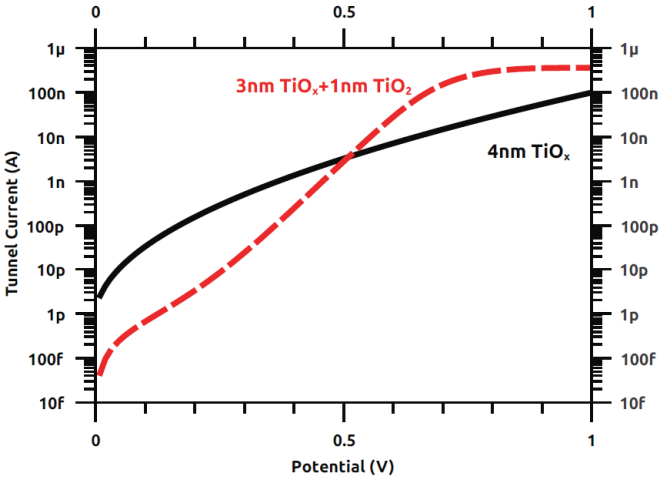



Fig.2: *Current-Potential simulation of 4nm TiOx and a 3nm TiOx + 1nm $TiO_2$ tunnel junctions having surface of 5nm².*

### B. Crested barrier DG-SET

Hereafter, we consider integrating crested barrier into a metallic DG-SET. This unipolar approach uses the second gate in order to operate in two logical states; '0' and '1' by setting $V_{G2}$ between [0, $V_{DD}$=$e$/4$C_G$]. In Figure 3, (a) P-type and (b) N-type DG-SET $I_D$–$V_{G1}$ characteristics were simulated for $V_{G2}$=GND (P-type) and $V_{G2}$=$V_{DD}$=0.7V (N-type). SET and junction parameters are $C_{G1}$=$C_{G2}$=0.057aF and $C_s$=$C_d$=0.039aF for a 4nm TiO*x* tunnel junction. It is conceivable to build CMOS-like standard digital or memory cells using P-SET and N-SET [6]. We will consider as the DG-SET to design elementary circuits such as DG-SET based inverter and SRAM bit-cell (Figure 8).

We thus compare the DG-SET based inverter and SRAM performances considering (i) single $TiO_x$ layer tunnel junction (ii) crested TiOx-$TiO_2$ barrier tunnel junction respectively (single and crested tunnel junctions are represented in Figure 1). The DG-SET current-voltage characteristics (Figure 3 and Figure 4) are simulated in accordance with the orthodox theory [7, 8]. Starting from drain to source and gate voltages; the change in free energy, the tunneling event rates and the island electron occupancy probabilities are calculated to obtain the current characteristics [9, 10]. Within this computation, the tunnel junction resistance was computed from the tunneling current using two approaches: (i) an analytical formulation [11, 12] which only allows considering single layer tunnel junction (ii) with the transfer matrix formalism for single layer or crested barriers [5].

Afterwards, the DG-SET-based inverter and SRAM simulations were obtained by using Verilog-A model in Cadence environment. To reduce computation time, we used Look-Up-Tables (LUT) in order to retrieve tunnel junction resistance of junction bias for each DG-SET.

## III. Results and Discussion

### A. DG-SET Device

In order to optimize tunnel current in DG-SET, increasing driving current and $I_{ON}/I_{OFF}$ ratio, we will consider the use of a crested barrier tunnel junction discussed previously. First, we consider a P-SET integrating a 4nm $TiO_x$ tunnel junction in Figure 4. The presented devices has a 5nm² surface tunnel junction which brings its capacitance value to $C_j$=0.039aF. The P-SET has been simulated for driving potentials $V_{DD}$ ranging from 0.4V to 0.8V and their corresponding gate capacitances (from 0.1aF to 0.05aF). As expected, ON current increases from less than 1nA to more than 10nA by increasing $V_{DD}$. A small increase is also measured in the $I_{ON}/I_{OFF}$ ratio, but the ratio doesn't surpass the value of 8.6 for $V_{DD}$=0.8V. In Figure 5, the P-SET integrating the 3nm $TiO_x$ + 1nm $TiO_2$ tunnel junction is simulated for driving potentials $V_{DD}$ ranging from 0.4V to 0.8V and compared to the 4nm $TiO_x$ P-SET. The ON current is also seen to increase this time from 10pA to reach 10nA while increasing $V_{DD}$. The $I_{ON}/I_{OFF}$ ratio in this case reaches a maximum of 414 for $V_{DD}$=0.7V. Thanks to tunnel junction engineering presented in this work, we are able to improve intrinsic characteristics of the nano-device as seen in Figure 4 and Figure 5. The $I_{ON}/I_{OFF}$ ratio increase is due to the reduction of the thermionic current contribution for an optimal tunneling current with different $V_{DD}$.

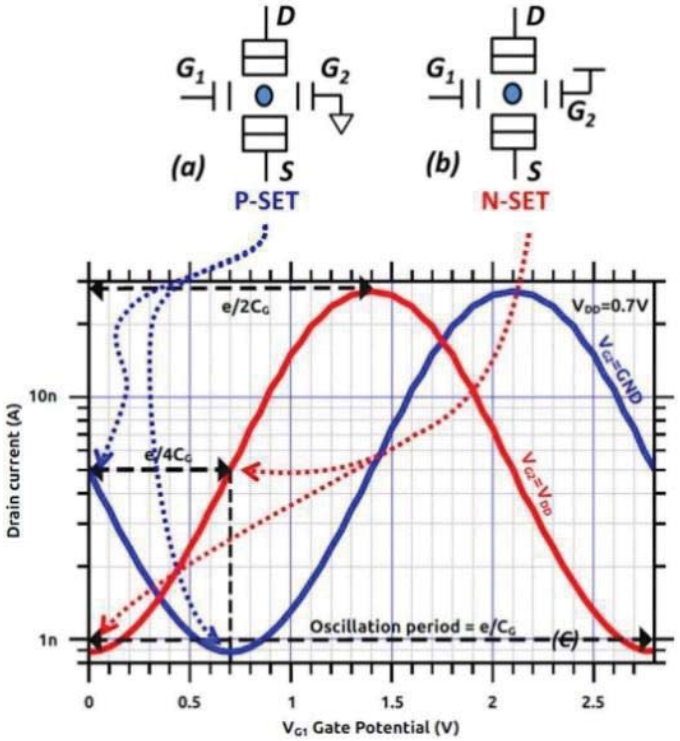



Fig.3: DG-SET configuration depending on the voltage applied to the second gate. (a) P-type. (b) N-type. (c) $I_D$–$V_{G1}$ simulated data (our model) for $V_{G2}$ = GND (P-type) and $V_{G2}$ = $V_{DD}$ =0.7V (N-type). SET and junction parameters are $C_{G1}$=$C_{G2}$=0.057aF and $C_s$=$C_d$=0.039aF for a 4nm TiOx tunnel junction [3].

*B. Application to Elementary Circuits*

Memory elements are amongst others the most attractive application for SETs. Herein, one bit Single Electron based static memory is presented. The design scheme of DG-SET-based SRAM cell is presented in Figure 6. The memory cell uses 6 DG-SETs to store and access one bit. It is composed of two coupled DG-SET inverters (S1-S2 and S3-S4 as presented in Figure 6) to store the data and two N-type SETs access transistors. We also used two tri-state DG-SETs buffers, which are designed to manage Read / Write cycles. Due to the feedback structure, a low input value on the first inverter will generate a high input value on the second inverter which feeds back the low value onto the first inverter and vice-versa. As long as the 'WL' is kept low, the cell is disconnected from the 'BL'. Thus, the cross coupled inverters will store their current logical value whatever their values.

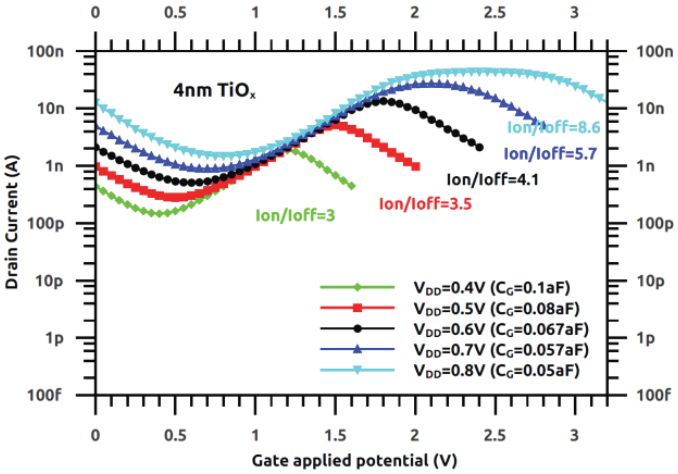



Fig.4: DG-SET $I_D$–$V_{G1}$ curve and $I_{ON}/I_{OFF}$ ratio for 4nm TiOx tunnel junction varying the gate capacitance $C_G$

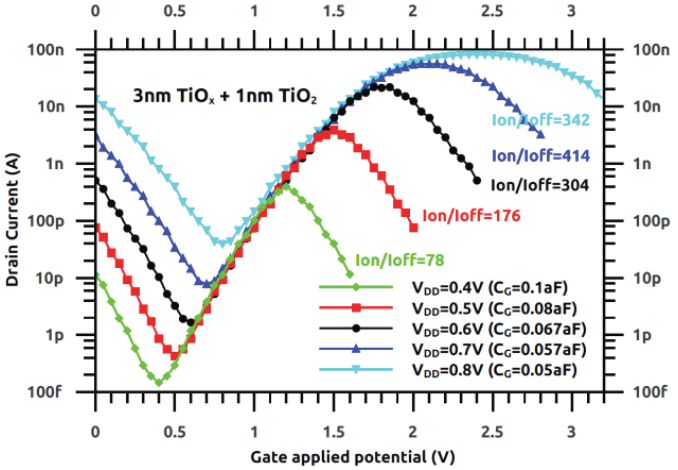



Fig.5: DG-SET $I_D$–$V_{G1}$ curve and $I_{ON}/I_{OFF}$ ratio for 3nm TiOx+1nm $TiO_2$ tunnel junction varying the gate capacitance $C_G$

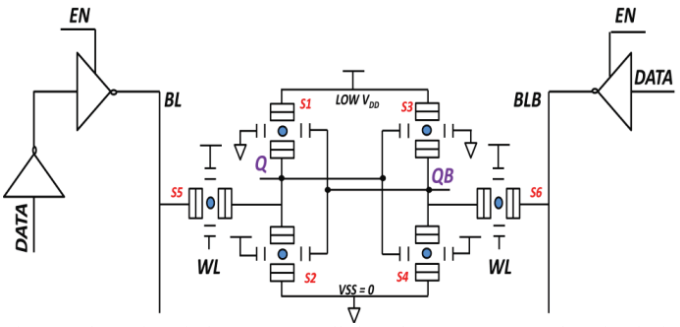



Fig.6: Schematic of the SRAM cell based on DG-SET. The circuit is composed by two N-SET access transistors, two inverters holding the stored data and tri-states buffers to manage the Read/Write cycles.

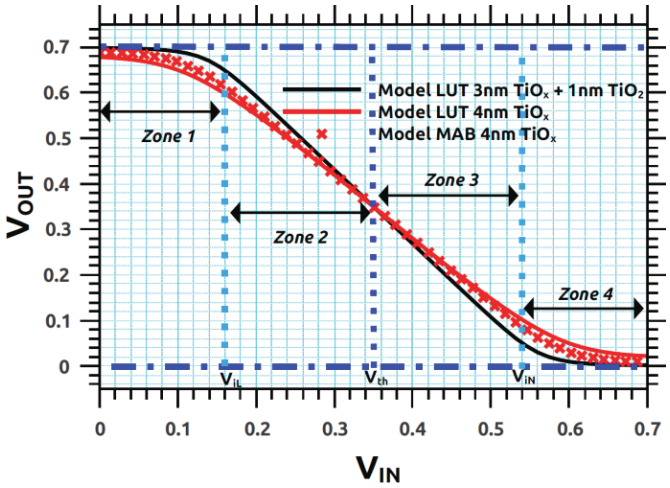



Fig.7: Transfer function of the DG-SET based inverter (MAB refers to the analytical formulation of the tunneling current [5], LUT indicates that the model reads the data in a stored table previously calculated with Transfer Matrix method

To hold the data properly into the cell, the cross-coupled inverters must maintain bi-stable operating points. A critical metric for SRAM bit-cell stability is the Static Noise Margin (SNM). SNM is the maximum amount of voltage noise that can be introduced at the outputs of the two inverters such that the cell retains its data. SNM quantifies the amount of voltage noise required at the internal nodes of a bit-cell to flip the cell's contents. Figure 8 illustrates the graphical representation of the SNM for a bit-cell holding data. The figure shows the voltage transfer characteristic (VTC) and its inverse from the two inverters which form the feedback loop. The length of the side of the largest square that can be embedded inside the lobes of the butterfly curve defines the SNM as illustrated in Figure 8. As we can see in Figure7, the slope of the transfer function of the inverter, based on crested $TiO_x/TiO_2$ tunnel junction, is higher leading to a superior static noise margin of the SRAM cell (Figure 6). It is then a real alternative to overcome power consumption issues mainly to the DG-SET low current flow nature while keeping a good performance metrics and transistor count involved in each bit-cell (6T architecture).

ISBN 978-1-4673-8608-1

IEEE Catalog number CFP1649D-USB

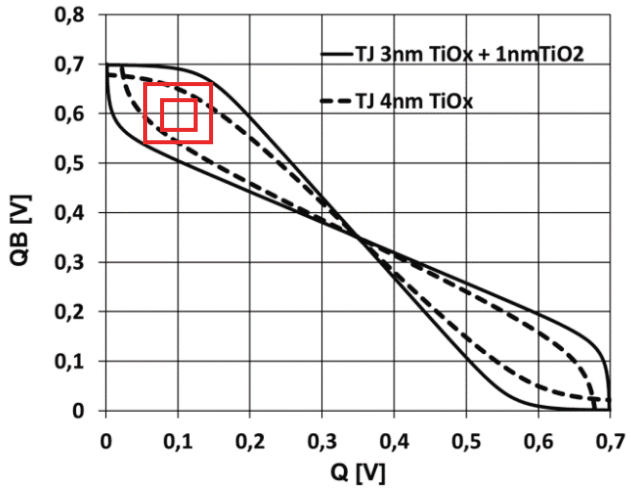



Fig.8: SRAM static noise margin butterfly curve during hold mode for TiOx single layer and TiOx/$TiO_2$ crested barrier. The TiOx/$TiO_2$ stack exhibits a better SNM window.

## IV. Conclusion & Perspectives

Tunnel junction engineering by means of optimal crested barriers allows enhancing the electrical Single Electron Transistor performances (e.g. $I_{ON}$ and $I_{ON}/I_{OFF}$ ratio) with benefit for SET-based circuits. Moreover, crested barriers do not only allow better performances at circuit level (e.g. SNM in this paper), but it could also contribute to consider SET technology, at least at the middle term, as a candidate to overcome power consumption and physical limitations facing CMOS technology. In term of perspectives, future works will focus on the device/circuit co-design. A thorough study with designers will be necessary to evaluate performance metrics (power consumption, delay, integration...) at large scale, and therefore bringing out the benefits of tunnel junction engineering and its impact at circuit level. The improvements shown on both device and circuits characteristics let us consider the hybrid integration of SET/CMOS logic and memory as an alternative for low-power applications such as IoT and embedded devices.

## Acknowledgments

This work was partly supported by the French RENATECH network, Region Rhone-Alpes, France and Wallonie-Bruxelles International. The authors would like to thank Nanoquebec/RQMP for funding support.

## References

[1] C. Dubuc, A. Beaumont, J. Beauvais, and D. Drouin, “Current conduction models in the high temperature single-electron transistor,” Solid-State Electron., vol. 53, no. 5, pp. 478–482, 2009.

[2] K. El Hajjam et al., “Highly transparent low capacitance plasma enhanced atomic layer deposition Al2O3-HfO2 tunnel junction engineering,” J. Vac. Sci. Technol. A, Vac., Surf., Films, vol. 32, no. 1, pp. 01A132-1–01A132-6, Jan. 2014.

[3] K. El Hajjam et al., “Tunnel Junction Engineering for Optimized Metallic Single-Electron Transistor” IEEE Transactions on Electron Devices, Vol. 62 no. 9, pp. 2298-3003, Sept. 2015

[4] B. Govoreanu, P. Blomme, M. Rosmeulen, J. Van Houdt, and K. De Meyer, “VARIOT: A novel multilayer tunnel barrier concept for low-voltage nonvolatile memory devices,” IEEE Electron Device Lett., vol. 24, no. 2, pp. 99–101, Feb. 2003

[5] B. Govoreanu, P. Blomme, M. Rosmeulen, J. Van Houdt, and K. De Meyer, “A model for tunneling current in multi-layer tunnel dielectrics,” Solid-State Electron., vol. 47, no. 6, pp. 1045–1053, 2003.

[6] M. A. Bounouar, A. Beaumont, K. E. Hajjam, F. Calmon, and D. Drouin, “Room temperature double gate single electron transistor based standard cell library,” in Proc. IEEE/ACM Int. Symp. Nanosc. Archit. (NANOARCH), Jul. 2012, pp. 146–151.

[7] D. V. Averin and K. K. Likharev, “Coulomb blockade of single-electron tunneling, and coherent oscillations in small tunnel junctions,” J. Low Temperature Phys., vol. 62, nos. 3–4, pp. 345–373, 1986.

[8] J. R. Tucker, “Complementary digital logic based on the ‘Coulomb blockade,’” J. Appl. Phys., vol. 72, no. 9, pp. 4399–4413, 1992.

[9] A. E. Hanna and M. Tinkham, “Variation of the Coulomb staircase in a two-junction system by fractional electron charge,” Phys. Rev. B, Condens. Matter, vol. 44, no. 11, pp. 5919–5922, Sep. 1991.

[10] K. K. Likharev, “Single-electron transistors: Electrostatic analogs of the DC SQUIDS,” IEEE Trans. Magn., vol. 23, no. 2, pp. 1142–1145, Mar. 1987.

[11] J. G. Simmons, “Generalized formula for the electric tunnel effect between similar electrodes separated by a thin insulating film,” J. Appl. Phys., vol. 34, no. 6, pp. 1793–1803, 1963.

[12] J. G. Simmons, “Potential barriers and emission-limited current flow between closely spaced parallel metal electrodes,” J. Appl. Phys., vol. 35, no. 8, pp. 2472–2481, Aug. 1964.

# Transient Second Harmonic Generation and correlation with Ψ-MOSFET in SOI wafers

D. Damianos, I. Ionica, A. Kaminski-Cachopo, G. Vitrant and S. Cristoloveanu
IMEP-LAHC,
MINATEC, Grenoble-INP, Univ. Grenoble Alpes
38016 Grenoble, France
dimitrios.damianos@minatec.grenoble-inp.fr

D. Blanc Pelissier
INSA de Lyon (INL)
69621 Villeurbanne, France

M. Kryger and J. Changala
Femtometrix Inc.
Santa Ana, CA 92705, USA

***Abstract*—Silicon-on-Insulator (SOI) wafers are characterized using a non-destructive second harmonic generation (SHG) method. Correlation between the electrical parameters extracted from pseudo-MOSFET characteristics and the SHG signal is demonstrated. A simple quantitative model allows reproduction of the SHG signal curves.**

***Keywords—Modeling; Optical characterization;Transient SHG; Silicon-on-Insulator; pseudo-MOSFET***

## I. Introduction

There is an industry need for non-destructive characterization of the surface and buried interface qualities in SOI wafers prior to device fabrication. The well-established Ψ-MOSFET method can characterize efficiently the SOI electrical properties [1], but it is an invasive method. Second Harmonic Generation (SHG) is a surface and buried interface-sensitive technique that could potentially lead to contactless, nondestructive characterization of SOI [2] and can currently be used as a complementary technique to Ψ-MOSFET in electrical parameter extraction.

Previous work has shown that SHG can be used to probe boron induced charge traps in $SiO_2$/Si (B-doped) stacks [3]. Doping type and concentration have been evaluated by measuring the magnitude of the initial SHG signal [4]. SHG also proves useful in tracing metallic contamination on SOI wafers [2]. This is of great importance for microelectronics since metallic contamination degrades device yield and reliability after migrating to the oxide interfaces during high temperature process steps. Furthermore SHG has demonstrated the ability to detect radiation induced charges in the buried oxide (BOX) and post-irradiation annealing effects on SOI wafers [5].

In a previous publication, we demonstrated an SHG testing station and its use for SOI characterization [6]. In this work, we study the transient SHG signals from SOI samples with different geometries and post-treatments. We then reproduce the measured curves using simple quantitative models of the SHG phenomenon. A comparison between interface trap ($D_{it}$) levels extracted from electrical measurements in pseudo-MOSFET configuration and SHG behavior is also reported.

## II. SHG and Ψ-MOSFET experiments

Three sets of samples with different Si thin film and BOX thicknesses were studied:

- Set 1: $t_{Si}$=18 nm and $t_{BOX}$=25 nm.
- Set 2: $t_{Si}$=24 nm and $t_{BOX}$=25 nm.
- Set 3: $t_{Si}$=12 nm and $t_{BOX}$=145 nm.

Both passivated (with thermal oxide) and non-passivated (with native oxide) samples were measured for the 1st and 3rd set. The samples from the 2nd set were also passivated with a thermal oxide on the top but one of them was annealed in a forming gas environment (Forming Gas Annealing - FGA).

The Ψ-MOSFET technique was used to monitor the electrical characteristics of the samples. For this purpose, the SOI samples were placed on a metal chuck. A back-gate bias was applied to the substrate while two metal probes placed on the top Si film were used as source and drain. The measured $I_D$-$V_G$ curves plotted in semilog scales are shown in Fig.1, Fig.2 and Fig.3 respectively for each set of samples. The subthreshold swing extracted from the experimental curves is related to $D_{it}$ through [1, 7]:

$$S = \frac{dlogI_D}{dV_G} = 2.3\frac{kT}{q}\left(1 + \frac{C_{Si} + qD_{it}}{C_{ox}}\right)$$

where $C_{Si}$ and $C_{ox}$ are the capacitances of the Si film and the BOX respectively.

TABLE 1: extracted interface trap densities

| SOI Sample | $D_{it}$ ($\times 10^{12}$ eV$^{-1}$cm$^{-2}$) |
|---|---|
| 1st set | |
| 18 nm/25 nm, non-passivated | 8.1 |
| 18 nm/25 nm, passivated | 3.5 |
| 2nd set | |
| 24 nm/25 nm, passivated (FGA) | 1.9 |
| 24 nm/25 nm, passivated | 1.4 |
| 3rd set | |
| 12 nm/145 nm, non-passivated | 3.3 |
| 12 nm/145 nm, passivated | 0.4 |

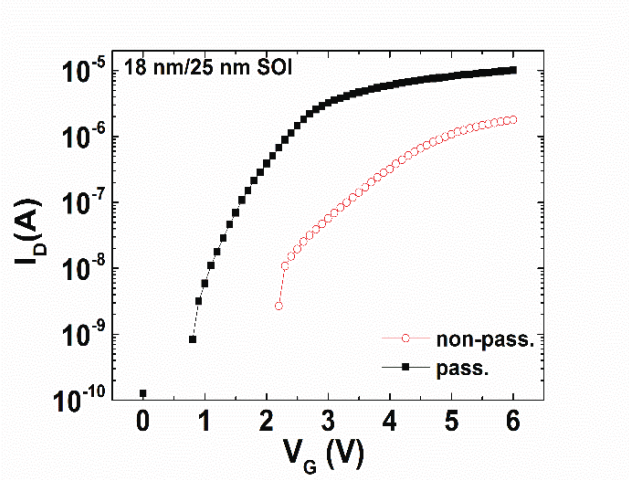



Fig. 1. $I_D$-$V_G$ curves obtained on 18 nm/25 nm SOI passivated (full symbols) and non-passivated (empty symbols) samples.

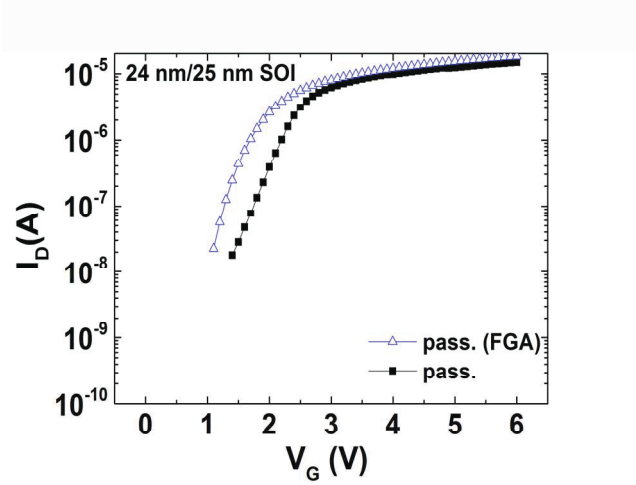



Fig. 2. $I_D$-$V_G$ curves obtained on 24 nm/25 nm SOI passivated with (empty symbols) and without forming gas annealing (full symbols).

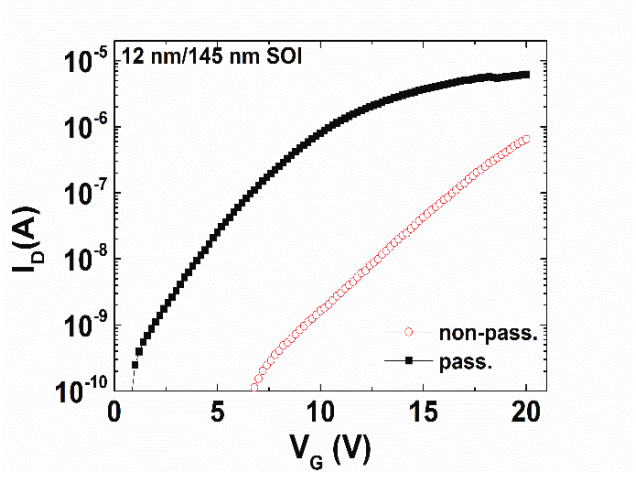



Fig. 3. $I_D$-$V_G$ curves obtained on 12 nm/145 nm SOI passivated (full symbols) and non-passivated (empty symbols) samples.

The results are shown in Table 1 above. $D_{it}$ is an effective value which includes the traps at Si film/BOX interface and at the top surface via a coupling mechanism, the latter being affected by the passivation step [10]. As observed previously [6], $D_{it}$ decreases with surface passivation.

The time dependent SHG measurements were performed using the Harmonic F1X metrology tool provided by Femtometrix [8]. A laser emitting femtosecond pulses at a fundamental wavelength of 780 nm was incident upon the samples. The minimum spot diameter was approximately 50 µm. The second harmonic generated (SHG) radiation at 390 nm was separated from the fundamental with an appropriate filter and was detected by a photomultiplier coupled with a photon counter. The angle of incidence was set at 45°, while the incident and second harmonic beam electric field polarizations were both parallel to the incidence plane (p-polarized). Time-dependent SHG signal was acquired with 10 ms gates.

Fig.4 shows the SHG signal of passivated and non-passivated 18 nm/25 nm SOI samples. The saturation signal (at 100s) is higher for the non-passivated sample. This can be attributed to the higher trap density $D_{it}$ reported in Table 1 (it reflects the lower surface quality [10] of the non-passivated sample). In this case, trapped photo-generated carriers will induce a higher quasistatic electric field, generating a greater SHG signal. The high SHG signal measured at t=0 on the passivated SOI sample may be due to fixed positive charges present at the thermal oxide/Si front surface that become compensated by photo-generated electrons.

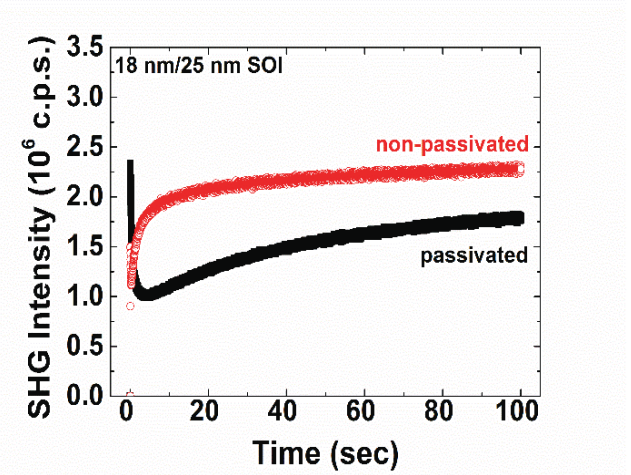



Fig. 4. SHG signals from the 18 nm/25 nm SOI with native oxide on top of the Si film (non-passivated) and with a thermal oxide (passivated).

For sample Set 2 with the same BOX thickness (25 nm) but different Si film thickness (24 nm) we observe a discharging-like behavior (Fig. 5). The time-dependent SHG decreases monotonically until it reaches a saturation value for both cases. A straightforward comparison between sets is not possible, since the geometry and the process technology is different. Again, for the sample with a higher $D_{it}$ value (passivated in FGA – Table 1) the saturation SHG signal is higher.

The transient behavior of the SHG in the case of the two 12 nm/145 nm SOI samples (Set 3, Fig.6) is dissimilar to the previous Sets 1 and 2. We can only observe a charging-like behavior, without any initial discharging as was observed in Set 1. The wafer with the inferior interfacial quality (non-

passivated) has a higher signal than the other (passivated). The corresponding $D_{it}$ values are shown in Table 1.

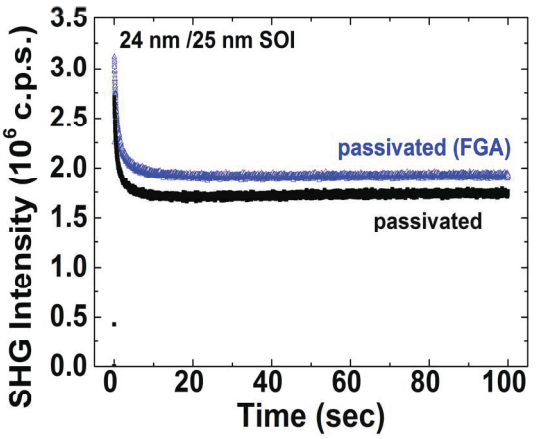



Fig. 5. SHG signals from the 24 nm/25 nm SOI with a thermal oxide on top of the Si film (passivated) and with a thermal oxide after forming gas annealing (passivated FGA).

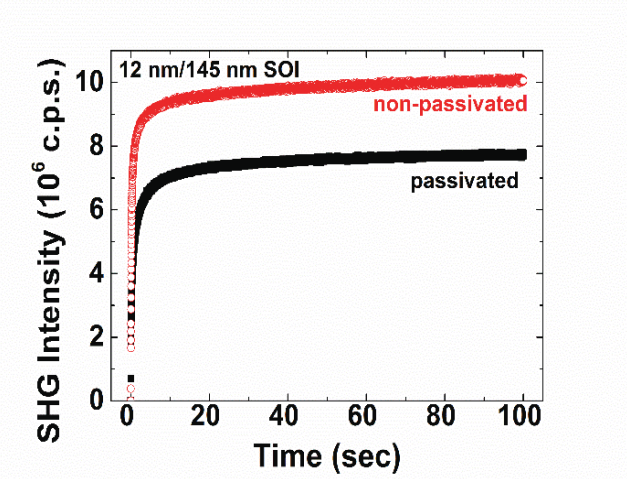



Fig. 6. SHG signals from passivated (thermal oxide) and non-passivated (native oxide) 12 nm/145 nm SOI.

All the SHG curves demonstrated a higher saturation signal for samples with higher $D_{it}$ (non-passivated). Nevertheless the transient SHG curves were different for each set of samples. In the next section we will focus on modelling the SHG in order to reproduce the experimental shapes.

## III. SHG Modeling

It has been shown [2, 3, 4, 5, 9] that the SHG signal can be expressed by an expression which includes terms that:

a) are relevant to the symmetry breaking at the interface of $Si/SiO_2$ and therefore are affected by the interface quality,

b) describe the Electric Field Induced Second Harmonic (EFISH) contribution arising from the interface dipole and bulk quadrupole polarization [9],

c) describe the static interfacial field.

For this reason we have used the following expression to model the experimental SHG signals [3]:

$$I^{2\omega}(t) = \left||\chi^{(2)}| + |\chi^{(3)}|e^{i\theta}E(t)\right|^2 (I^{\omega})^2 \qquad (1)$$

where $\chi^{(2)}$ and $\chi^{(3)}$ are the non-linear interface second-order and bulk third-order susceptibilities respectively, θ is a relative phase difference between the two susceptibilities (complex numbers), and $E(t)$ is a time-dependent electric field which includes both the initial DC field and its slowly varying component. $I^{\omega}$ is the intensity of the incident beam and $I^{2\omega}$ the intensity of the SHG beam. Bulk Si and $SiO_2$ are centrosymmetric materials and therefore do not contribute to the SHG signal ($\chi^{(2)}_{bulk} = 0$, but $\chi^{(2)}_{interface} \neq 0$).The time-dependent field in Eq.1 which gives rise to the EFISH contribution that was mentioned above can be described by the use of 2 exponential terms: one relevant to charging behavior and the other relevant to discharging behavior. According to [3], a general expression which includes the electric fields related to traps and the time constants related to trapping and detrapping can be used. Alternatively, one can think that the existence of the aforementioned trapping and detrapping mechanisms are relevant to a coupling effect between the 2 interfaces (surface oxide/Si film and Si film/BOX) which has been proposed both for electrical measurements [10] and for SHG [11].

The expression that we used for the modeling is [3]:

$$E(t) = Ae^{-t/t_1} - B(1 - e^{-t/t_2}) \qquad (2)$$

where we can see the different parameters described above; A and B are the electric fields, $t_1$ is the detrapping time constant and $t_2$ the trapping time constant. It should be noted that in this case the doping concentration is lower than the one used in [3].

For the previous experimental curves (Fig. 4, 5, 6) we can identify that at $t = 0$ there is a nonzero preexisting DC electric field connected to the initial value of the SHG signal. This can be also expressed in our model (Eq.1 with $E(t = 0) = E_0 = A$), where at $t = 0$ we have a nonzero SHG intensity $I^{2\omega} = \left||\chi^{(2)}| + |\chi^{(3)}|e^{i\theta}A\right|^2 (I^{\omega})^2$.

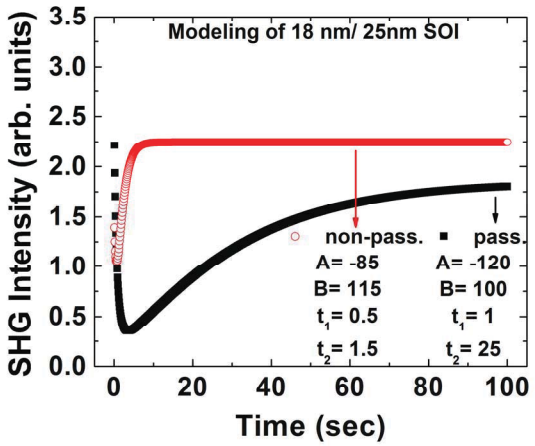



Fig. 7. Calculated time dependent SHG curves showing similar behavior as in Fig.4. The parameters used in equation (2) are also reported. The curves fitting the shape of passivated and nonpassivated SOI are identified.

The only parameters that were changed in the modeling were those in Eq. 2, since the ones in Eq. 1 are material dependent, thus were kept constant.

Fig. 7 shows the calculated curves and their associated parameters. The value of $B$ which describes the saturation regime in the model (Fig. 5) is higher for the non-passivated SOI, while the charging time is faster (smaller value of $t_2$).

The corresponding modeling for sample Set 2 (24 nm/25 nm SOI) with the appropriate parameters is shown in Fig. 8. The absolute value of $B$ is higher for the passivated FGA sample, which is connected to a higher SHG saturation value, as in the experiment.

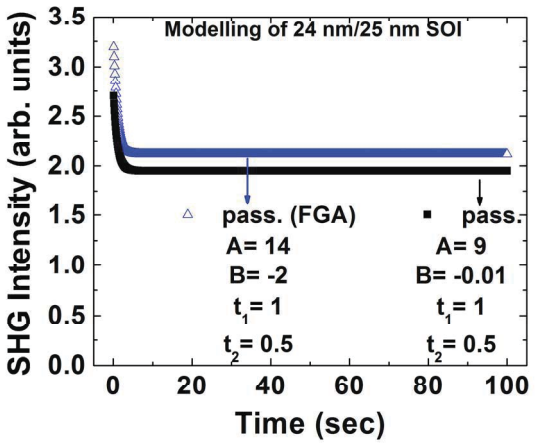



Fig. 8. Calculated time dependent SHG curves showing similar behavior as in Fig.5. The parameters used in equation (2) are also shown.

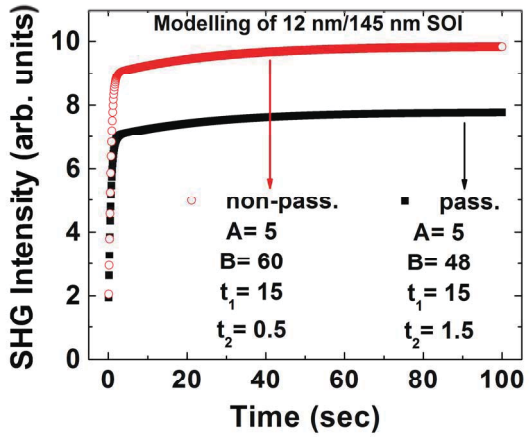



Fig. 9. Calculated time dependent SHG curves with their corresponding parameters, showing similar behavior as in Fig.6.

Fig. 9 depicts the calculated curves along with the fit parameters for sample Set 3 (12 nm/145 nm SOI). A difference is observed in the values of $B$ (difference between the saturation values – higher $B$ for the non-passivated sample) but the SHG time evolution is qualitatively the same. It is noteworthy that in this case $A \approx 0$ which means there is almost no initial or general discharging-like behavior, in contrast to Sets 1 and 2. This indicates the existence of other phenomena, probably related to the geometry and processing steps of SOI wafers.

## IV. Conclusion

A link between the effective extracted $D_{it}$ levels and the SHG signal was established. For samples included in the same set (with identical thicknesses of film and BOX), a correlation is evidenced: higher $D_{it}$ values are associated to a stronger saturation SHG signal. Differences in the time dependence of the signals were also observed between samples with different geometries. A simple quantitative model based on charging and discharging exponential terms was used to describe the transient behavior of the SHG signals. Our calculated curves effectively reproduce the transient SHG measurements obtained on different SOI geometries. Further work has the potential to produce more precise quantitative models relating the measured SHG signal and electrical parameters.

## Acknowledgements

This work is supported by Region Rhône Alpes (ARC6 program). We would also like to thank Vanderbilt University SHG team (Profs. M. Alles, R. Schrimpf, N. Tolk) and SOITEC (O. Kononchuk, F. Allibert) for cooperation.

## References

[1] S. Cristoloveanu and S. Williams, "Point-contact pseudo-MOSFET for in-situ characterization of as-grown Silicon-On-Insulator wafers", *IEEE Electron Device Letters vol. 13 (2),* p. 102, 1992

[2] M.L. Alles, R. Pasternak, X. Lu, N. H. Tolk, R. D. Schrimpf, D. M. Fleetwood et al, "Second harmonic generation for noninvasive metrology of Silicon-On-Insulator wafers", *IEEE Transactions on Semiconductor Manufacturing vol. 20(2)*, p. 107, 2007.

[3] H. Park, J. Qi, Y. Xu, K. Varga, S. M. Weiss, B. R. Rogers et al., "Boron induced charge traps near the interface of $Si/SiO_2$ probed by second harmonic generation", *Physica Status Solidi B vol. 247 (8)*, p. 1997, 2010.

[4] J. L. Fiore, V. V. Fomenko, D. Bodlaki, E. Borguet, "Second harmonic generation probing of dopant type and density at the $Si/SiO_2$ interface", *Applied Physics Letters vol. 98*, 041905, 2011

[5] B. Jun, R. D. Schrimpf, D. M. Fleetwood, Y. V. White, R. Pasternak, S. N. Rashkeev et al., "Charge trapping in irradiated SOI wafers measured by second harmonic generation", *IEEE Transactions on Nuclear Science 51 (6),* p. 3231, 2004

[6] D. Damianos, L. Pirro, G. Soylu, I. Ionica, V. Nguyen, G. Vitrant et al., "Second harmonic generation for contactless non-destructive characterization of silicon on insulator wafers", *Solid State Electronics,* 2015 (in press)

[7] S. M. Sze, *Physics of Semiconductor Devices,* 1981

[8] http://www.femtometrix.com

[9] J. H. Gielis, P. M. Gevers, I. M. P. Aarts, M. C. M. van de Sanden and W. M. M. Kessels, "Optical second-harmonic generation in thin fim systems", *Journal of Vaccum Science and Technology A vol. 26,* p. 1519, 2008

[10] G. Hamaide, F. Allibert, H. Hovel and S. Cristoloveanu, "Impact of free-surface passivation on silicon on insulator buried interface properties by pseudotransistor characterization", *Journal of Applied Physics vol. 101,* 114513, 2007.

[11] B. Jun, Y. V. White, R. D. Schrimpf, D. M. Fleetwood, F. Brunier, N. Bresson et al., "Characterization of multiple $Si/SiO_2$ interfaces in Silicon-On-Insulator materials via second-harmonic generation", *Applied Physics Letters vol. 85*, p. 3095, 2004.

# Direction Dependent Three-Dimensional Silicon Carbide Oxidation Growth Rate Calculations

Vito Šimonka*, Georg Nawratil‡, Andreas Hössinger§, Josef Weinbub*, and Siegfried Selberherr†
*Christian Doppler Laboratory for High Performance TCAD at the
†Institute for Microelectronics, TU Wien, Gußhausstraße 27-29/E360, 1040 Wien, Austria
‡Institute of Discrete Mathematics and Geometry, TU Wien, Wiedner Hauptstraße 8-10, 1040 Wien, Austria
§Silvaco Europe Ltd., Compass Point, St Ives, Cambridge, PE27 5JL, United Kingdom
Email: simonka@iue.tuwien.ac.at

***Abstract*—We propose a direction dependent interpolation method for silicon carbide oxidation growth rates and we compute these rates for three-dimensional simulations according to known growth rate values. Additionally, we analyze the temperature dependence of silicon carbide oxidation for different crystal directions. Our approach is an essential step towards highly accurate three-dimensional oxide growth simulations and helps to better understand the silicon carbide anisotropic nature and oxidation mechanism.**

## I. Introduction

Silicon carbide (SiC) is a wide bandgap semiconductor and has superior physical properties for power device applications, such as approximately three times wider band gap, ten times larger electrical break-down field, and three times higher thermal conductivity, compared to silicon (Si) [1], [2]. Taking advantages of these properties, the on-state resistance for unipolar devices such as metal-oxide-semiconductor field-effect-transistors (MOSFETs) can be reduced by a factor of a few hundreds when replacing Si with SiC [3], [4].

3C-SiC, 4H-SiC, 6H-SiC, and 15R-SiC are the most common polytypes presently being developed for device applications. These polytypes are characterized by the stacking sequence of the bi-atom layers of the SiC structure. Changing of the stacking sequence has a profound effect on the electrical properties. In this work we focus only on the 4H-SiC polytype as it has been recognized as the most promising material for electronic high power, high frequency, and high temperature applications [5].

Thermally grown silicon oxide ($SiO_2$) plays a unique role in device fabrication. Among the wide bandgap semiconductors, SiC is the only compound semiconductor which can be thermally oxidized in the form of $SiO_2$, similar to the Si substrate. The oxidation reaction of SiC is defined by [5]:

$$\mathrm{SiC} + \frac{3}{2}\mathrm{O_2} \leftrightarrow \mathrm{SiO_2} + \mathrm{CO}. \tag{1}$$

However, thermal oxidation of SiC is considerably more complicated compared to the oxidation of Si [2] and is about one order of magnitude slower under the same conditions [6], [7]. The oxidation of SiC additionally includes the out-diffusion of product gasses (e.g. CO) through the oxide film. Another unique phenomenon has been observed: The oxidation of SiC is a face-terminated oxidation, i.e., the top and the bottom face have different oxidation rates [8]–[10]. Fig. 1 shows popular faces of 4H-SiC.

In Section II we discuss thermal oxidation models of Si and SiC, in Section III we introduce the temperature dependence of oxidation growth rates with Arrhenius plots, and in Section IV we discuss geometrical aspects of SiC, proposed interpolation methods, and results.

## II. Thermal Oxidation Models

There are several one-dimensional Si and SiC oxidation models available [1], [2], [5], [11]–[17], of which the most popular one is the Deal-Grove model [5], [11], [14] and the more accurate Massoud empirical relation [1], [12]. The Deal-Grove model assumes that the oxidation occurs by diffusion of the oxidant to the $SiO_2$/Si interface, where it reacts with Si. This process is expressed by the following parabolic ordinary differential equation for the oxide thickness $X$ over time [11],

$$\frac{dX}{dt} = \frac{B}{A + 2X}, \tag{2}$$

where $B/A$ and $B$ denote the linear and parabolic rate constants of oxidation, respectively. The oxidation process cannot be characterized by the Deal-Grove model for the thin oxide region, hence Massoud *et al.* have proposed an empirical relation to describe the growth rate enhancement. This model includes an additional exponential term [12],

$$\frac{dX}{dt} = \frac{B}{A + 2X} + C\exp\left(-\frac{X}{L}\right), \tag{3}$$

where $C$ and $L$ are the exponential prefactor and the characteristic length, respectively. All of the above parameters ($B/A$, $B$, $C$ and $L$) are highly dependent on the crystal orientation of SiC [1], [5], i.e., the parameter values are different for the surface oxidation on different faces of the crystal.

The Deal-Grove and Massoud *et al.* models were originally proposed for Si oxidation, but can be applied in a modified form to SiC oxidation [2]. However, due to the one-dimensional nature those models cannot correctly predict oxidation growth for three-dimensional SiC structures. Our approach extends these models by incorporating the crystal direction dependence into the oxidation growth rates.

ISBN 978-1-4673-8608-1  IEEE Catalog number CFP1649D-USB

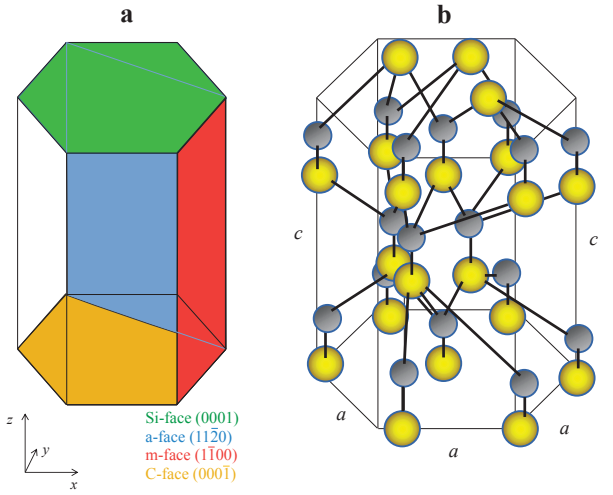



Fig. 1. A schematic illustration of **a)** common faces of a hexagonal structure and **b)** atomic view of a 4H-SiC polytype with sequence ABAC. Green, blue, red, and orange shapes show the Si-, a-, m-, and C-face, respectively. Yellow spheres show the Si atoms, gray spheres C atoms, $a$ is crystal dimension, and $c$ is the crystal height. The ratio between $c$ and $a$ for 4H-SiC is approximately three and for 6H-SiC approximately five.

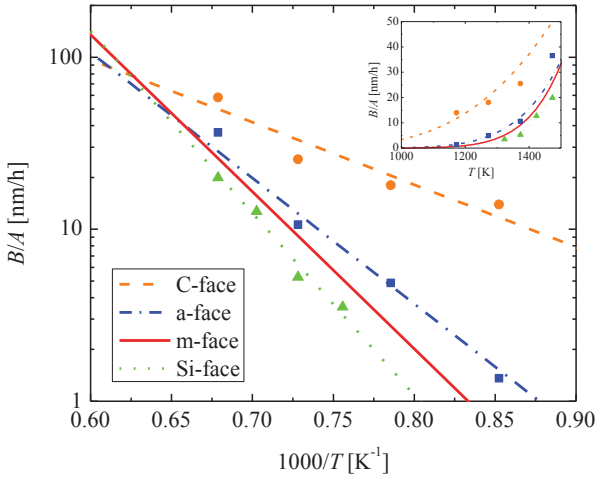



Fig. 2. Arrhenius plots of 4H-SiC oxidation, linear growth rates $B/A$ versus oxidation temperature for the Si- (green), m- (red), a- (blue), and C-face (orange). Experimental data for the Si-, a-, and C-face (symbols) were obtained from [1] and the data for the m-face (solid lines) were approximated from [19].

## III. Growth Rates of Oxidation

The rate of any chemical reaction depends on various physical quantities, e.g., temperature and pressure. As the temperature increases, the molecules move faster and collide more frequently with each other. The proportion of collisions influences the kinetic energy of the molecules and the activation energy of the chemical reaction. The relation between the temperature $T$ and the rate constant of the chemical reaction $k$ is defined by the Arrhenius equation [18]

$$k = Z \exp(-\frac{E_a}{RT}), \tag{4}$$

where $Z$ is the pre-exponential factor, $E_a$ is the activation energy of the chemical reaction, and $R$ is the ideal gas constant. The Arrhenius equation can be used to determine the activation energy [1] when applying the natural logarithm on both sides of the equation.

$$\ln(k) = -\frac{E_a}{R}\frac{1}{T} + \ln(Z) \tag{5}$$

The equation has the form of a linear function $y = mx + n$, with the slope $m = -Ea/R$ and the intercept $n = ln\,(Z)$.

As the oxidation of SiC strongly depends on the temperature, we use an Arrhenius plot to analyze the effect of temperature on the growth rates of oxidation. Fig. 2 and Fig. 3 show Arrhenius plots of the linear growth rates $B/A$ and initial growth rates $B/A + C$ for the four SiC faces, respectively. The data points are measured values, the dashed lines are fits using Massoud's empirical relation (Eq. 3), and the solid lines are approximated values. We have obtained the growth rates and activation energies of the Si-, a-, and C-face from experimentally measured data [1]. Additionally, we have approximated the growth rate and activation energy for the m-face, based on published oxide thicknesses [19], as there are

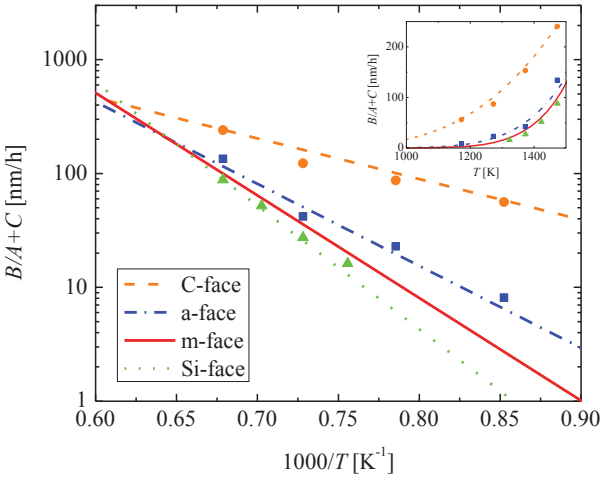



Fig. 3. Arrhenius plots of 4H-SiC oxidation, initial growth rates $B/A + C$ versus oxidation temperature for the Si- (green), m- (red), a- (blue), and C-face (orange). Experimental data for the Si-, a-, and C-face (symbols) were obtained from [1] and the data for the m-face (solid lines) were approximated from [19].

no experimental data available. These plots allow to directly obtain fixed growth rate values for different oxidation temperatures in order to perform growth rate surface calculations.

The linear growth rates are used when the oxide thickness $X$ is far below the characteristic thickness $A$, in which the rate-limiting step is the interface oxidation reaction. The initial growth rates are used for the thin oxide region when $X$ is approximated by zero. We do not show the Arrhnenius plot of the parabolic rate constant $B$, as its value and activation energy do not depend on the crystal orientation [1].

ISBN 978-1-4673-8608-1

IEEE Catalog number CFP1649D-USB

## IV. Geometry of SiC

Geometrical aspects of SiC must be described mathematically in order to calculate growth rate variations for different crystal directions. We propose a direction dependent interpolation method to convert an arbitrary crystal direction into a growth rate for oxidation, according to a set of known growth rate values [1]. For fixed points of oxidation growth rates we use the $(0001)$, $(10\bar{1}0)$, $(11\bar{2}0)$, and $(000\bar{1})$ directions, which have been examined experimentally [1], [5], [19] and correspond to the Si-, m-, a-, and C-face, respectively (see Fig. 1). Note, the hexagonal structure includes six m- and six a-faces, while it has only one Si- and one C-face.

The proposed interpolation is written as a parametric function, which consists of a symmetric star shape in the x-y plane and a tangent-continuous union of two half-ellipses in z direction. Fig. 4 shows the fixed points of the growth rates and the interpolation curves between them in the x-y and x-z planes. A linear star-shaped interpolation with sharp edges would fit the geometry of SiC well enough, but rather more accurate and realistic is a non-linear interpolation.

The parametric function of the three-dimensional interpolation method is

$$\begin{aligned} x &= \Big(k_y + (k_x - k_y)\cos^2(3t)\Big)\cos(t)\cos(u), \\ y &= \Big(k_y + (k_x - k_y)\cos^2(3t)\Big)\sin(t)\cos(u), \\ z &= k_z^+ \sin(u) \text{ for } u \geq 0, \\ z &= k_z^- \sin(u) \text{ for } u < 0, \end{aligned} \tag{6}$$

where $t \in [0, 2\pi]$ and $u \in [-\pi/2, \pi/2]$ are arbitrary parametric variables and $k_{x,y,z}$ are known oxidation growth rates in $x$, $y$, and $z$ direction, respectively.

The positive and negative z coordinates are calculated separately, as the oxide growth on top $k_z^+$ and bottom $k_z^-$ of the crystal is different. The growth rates $k_x$, $k_y$, $k_z^+$ and $k_z^-$ correspond to $k_m$, $k_a$, $k_{Si}$ and $k_C$, which are the growth rates in the directions of the m-, a-, Si- and C-face, respectively. The growth rate surface is given by a non-linear interpolation between these known growth rate values and follows the geometry of SiC, i.e., the planes tangent to the growth rate surface at $k_{Si}$, $k_m$, $k_a$, and $k_C$ are parallel to the corresponding faces.

The hexagonal structure of SiC gives geometrical symmetry in the x-y plane so that the crystal directions towards a- and m-faces repeat six times with an enclosed angle of $\pi/6$. Hence, the proposed interpolation method match with the three-dimensional behavior of SiC oxidation. The SiC oxidation growth rate surface is shown in Fig. 5, Fig. 6, and Fig. 7, respectively.

The distance from the origin $0 = (0, 0, 0)$ to any point on the growth rate surface gives the growth rate in direction to this point. The set of growth rate values together with the SiC oxidation models can be used for three-dimensional oxidation growth simulations.

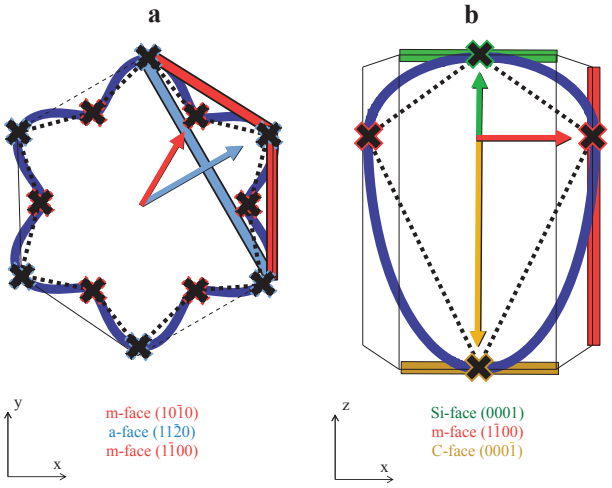



Fig. 4. Schematic representation of the two-dimensional interpolation in the **a)** x-y and **b)** x-z plane. A linear (black dotted) and a non-linear (dark blue line) interpolation is used according to known growth rate values (black crosses) of Si- (green), m- (red), a- (blue), and C-face (orange square). Colored arrows represent crystal directions towards the corresponding faces.

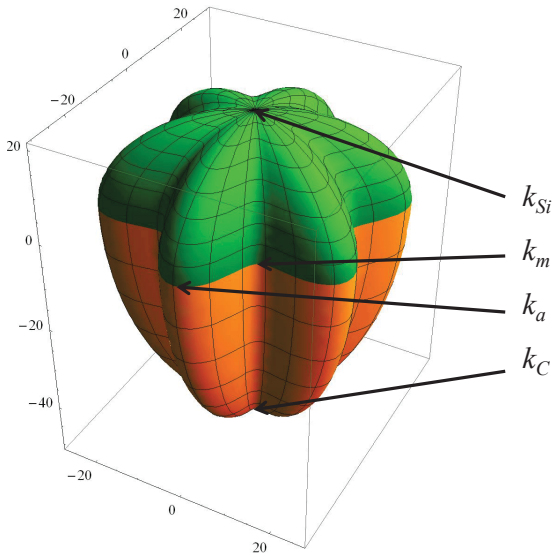



Fig. 5. Three-dimensional parametric plot of 4H-SiC oxidation growth rates. An arbitrary direction growth rate is calculated according to the four known growth rates ($k_{Si}$, $k_m$, $k_a$, and $k_C$) shown with black arrows. The surface color shows calculations for positive (green) and negative (orange) z direction.

## V. Summary

We have proposed an interpolation method for oxidation rates based on the SiC geometry, which converts an arbitrary crystal direction into a growth rate value. This allows to calculate SiC oxidation growth rates in three dimensions according to four known growth rate values. These vary with oxidation temperature and can be calculated with the provided Arrhenius plots.

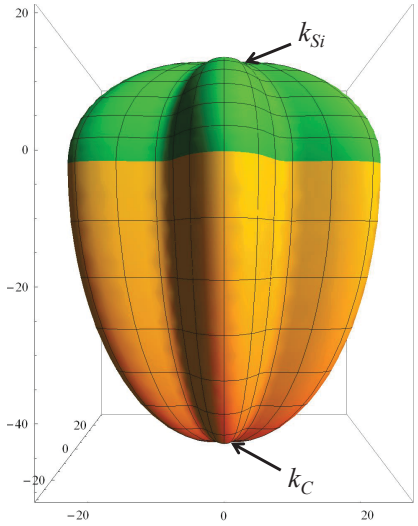



Fig. 6. Front view of the three-dimensional parametric plot of 4H-SiC oxidation growth rates. The two fixed points $k_{Si}$ and $k_C$ are shown with black arrows and correspond to Si- and C-face, respectively. The surface color shows calculations for positive (green) and negative (orange) z direction.

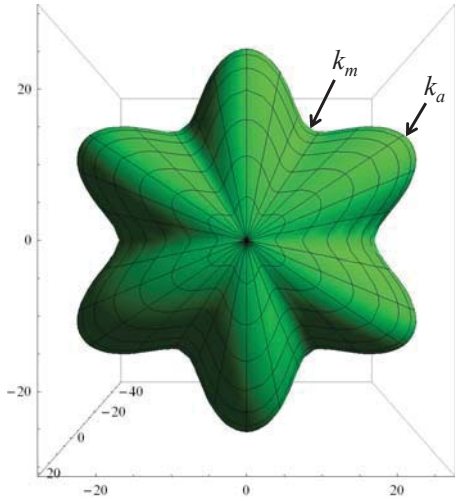



Fig. 7. Top view of the three-dimensional parametric plot of 4H-SiC oxidation growth rates. Black arrows show one of the six fixed points $k_m$ and $k_a$, which correspond to an m- and a-face, respectively.

## ACKNOWLEDGMENT

The authors wish to thank Y. Hijikata for providing experimental data. The financial support by the *Austrian Federal Ministry of Science, Research and Economy* and the *National Foundation for Research, Technology and Development* is gratefully acknowledged.

## REFERENCES

[1] D. Goto, Y. Hijikata, S. Yagi, and H. Yaguchi, "Differences in SiC Thermal Oxidation Process Between Crystalline Surface Orientations Observed by in-situ Spectroscopic Ellipsometry," *Journal of Applied Physics*, vol. 117, no. 9, p. 095306, 2015.

[2] Y. Hijikata, *Physics and Technology of Silicon Carbide Devices*. InTech Croatia, 2013.

[3] C. E. Weitzel, J. W. Palmour, C. H. Carter, K. Moore, K. J. Nordquist, S. Allen, C. Thero, and M. Bhatnagar, "Silicon Carbide High-Power Devices," *IEEE Transactions on Electron Devices*, vol. 43, no. 10, pp. 1732–1741, 1996.

[4] J. Casady and R. W. Johnson, "Status of Silicon Carbide (SiC) as a Wide-Bandgap Semiconductor for High-Temperature Applications: A Review," *Solid-State Electronics*, vol. 39, no. 10, pp. 1409–1422, 1996.

[5] Y. Song, S. Dhar, L. C. Feldman, G. Chung, and J. R. Williams, "Modified Deal Grove Model for the Thermal Oxidation of Silicon Carbide," *Journal of Applied Physics*, vol. 95, no. 9, pp. 4953–4957, 2004.

[6] I. C. Vickridge, J. J. Ganem, G. Battistig, and E. Szilagyi, "Oxygen Isotopic Tracing Study of the Dry Thermal Oxidation of 6H-SiC," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, vol. 161, pp. 462–466, 2000.

[7] J. M. Knaup, P. Deák, T. Frauenheim, A. Gali, Z. Hajnal, and W. J. Choyke, "Theoretical Study of the Mechanism of Dry Oxidation of 4H-SiC," *Physical Review B*, vol. 71, no. 23, p. 235321, 2005.

[8] M. Schürmann, S. Dreiner, U. Berges, and C. Westphal, "Structure of the Interface Between Ultrathin SiO 2 Films and 4H-SiC (0001)," *Physical Review B*, vol. 74, no. 3, p. 035309, 2006.

[9] P. Fiorenza and V. Raineri, "Reliability of Thermally Oxidized SiO2/4H-SiC by Conductive Atomic Force Microscopy," *Applied Physics Letters*, vol. 88, no. 21, p. 2112, 2006.

[10] T. Yamamoto, Y. Hijikata, H. Yaguchi, and S. Yoshida, "Oxygen-partial-pressure dependence of sic oxidation rate studied by in situ spectroscopic ellipsometry," in *Materials science forum*, vol. 600. Trans Tech Publ, 2009, pp. 667–670.

[11] B. E. Deal and A. Grove, "General Relationship for the Thermal Oxidation of Silicon," *Journal of Applied Physics*, vol. 36, no. 12, pp. 3770–3778, 1965.

[12] H. Z. Massoud, J. D. Plummer, and E. A. Irene, "Thermal Oxidation of Silicon in Dry Oxygen Accurate Determination of the Kinetic Rate Constants," *Journal of the Electrochemical Society*, vol. 132, no. 7, pp. 1745–1753, 1985.

[13] Y. Hijikata, H. Yaguchi, and S. Yoshida, "A Kinetic Model of Silicon Carbide Oxidation Based on the Interfacial Silicon and Carbon Emission Phenomenon," *Applied Physics Express*, vol. 2, no. 2, p. 021203, 2009.

[14] A. S. Grove, *Physics and Technology of Semiconductor Devices*. John Wiley & Sons Inc, 1967.

[15] H. Kageshima, K. Shiraishi, and M. Uematsu, "Universal Theory of Si Oxidation Rate and Importance of Interfacial Si Emission," *Japanese Journal of Applied Physics*, vol. 38, no. 9A, p. L971, 1999.

[16] S. Ogawa and Y. Takakuwa, "Rate-Limiting Reactions of Growth and Decomposition Kinetics of Very Thin Oxides on Si (001) Surfaces Studied by Reflection High-Energy Electron Diffraction Combined with Auger Electron Spectroscopy," *Japanese Journal of Applied Physics*, vol. 45, no. 9R, p. 7063, 2006.

[17] T. Watanabe, K. Tatsumura, and I. Ohdomari, "New Linear-Parabolic Rate Equation for Thermal Oxidation of Silicon," *Physical Review Letters*, vol. 96, no. 19, p. 196102, 2006.

[18] S. K. Gupta and J. Akhtar, *Thermal Oxidation of Silicon Carbide (SiC)-Experimentally Observed Facts*. INTECH Open Access Publisher, 2011.

[19] J. J. Ahn, Y. D. Jo, S. C. Kim, J. H. Lee, and S. M. Koo, "Crystallographic Plane-Orientation Dependent Atomic Force Microscopy-Based Local Oxidation of Silicon Carbide," *Nanoscale Research Letters*, vol. 6, no. 1, pp. 1–5, 2011.

# On the influence of the back-gate bias on InGaAs Trigate MOSFETs

Enrique G. Marin†, Francisco G. Ruiz*, Andrés Godoy, José M. Gonzalez-Medina, I. M. Tienda-Luna, Alejandro Toral and Francisco Gámiz

Departamento de Electrónica y Tecnología de los Computadores, Universidad de Granada
Av. Fuentenueva S/N, 18071 – Granada (Spain)
Email: †egmarin@ugr.es, * franruiz@ugr.es

***Abstract*— We analyze the behavior of InGaAs Trigate MOSFETs under the influence of a back-gate bias, $V_{bg}$. The charge distribution, the body-factor, the threshold voltage and the electron mobility dependences on $V_{bg}$ are discussed. The InGaAs devices are benchmarked against Si ones demonstrating a higher impact of the back-gate bias for the formers, causing larger body factors and stronger mobility variations.**

***Keywords—back gate bias, III-V materials, multigate devices, MOSFETs.***

## I. Introduction

Multiple gate (MuG) architectures and the dynamic control of the threshold voltage ($V_T$) stand out as two of the most efficient solutions to overcome the limitations associated to the Metal-Oxide-Semiconductor Field-Effect-Transistor down-scaling process. On the one hand, MuG architectures, such as trigate MOSFETs [1], provide a better gate electrostatic control of the channel, thus reducing the Short Channel Effects (SCEs). On the other hand, the dynamic control of $V_T$ would allow managing simultaneously power and performance. One potential way to modify $V_T$ is the back-gate biasing that makes use of the body effect [2,3].

Both alternatives have been studied separately, and a few works have dealt with the back-gate bias influence on MuG devices [2-6], focused mainly on their electrostatic behavior. Recently, we presented a study where the influence of the back-gate biasing on the electron mobility of Si trigates on ultrathin buried oxide [7] is thoroughly analyzed.

Moreover, III-V materials have attracted an increasing attention during the last years. Their potential to increase the ON current while reducing the dissipated power is promising [8]. Among all the III-V alloys, InGaAs is emerging as the most attractive one as it is pointed out to have a near optimum trade-off between the density of states and the electron mobility. So that, in this work we investigate the influence of the back-gate bias on the behavior of InGaAs trigates, taking into account both the electrostatic behavior and its influence on the electron mobility.

The outline of the work is the following. In Section II, we present the simulation tools employed. Next, Section III analyzes the main electrostatic features, including threshold voltage variation, body factor and charge redistribution of the carriers due to the back-gate bias. In Section IV the mobility of InGaAs and Si trigates is compared as a function of the back-gate bias, and the influence of each scattering mechanism is assessed. Finally, Section V presents the main conclusions of the work.

## II. Numerical Method

A 2D self-consistent Schrödinger-Poisson (SP2D) solver based on the effective mass approach has been used to evaluate the electrostatic behavior of long-channel trigate devices. Non-parabolic corrections have been included following the work by Jin et al. [9]. The charge corresponding to the Γ, L and X valleys has been calculated for $In_xGa_{1-x}As$ (x=0.53), while the three pairs of anisotropic Δ valleys have been considered for Silicon. The main parameters used in the electrostatic simulations are listed in Table I, including, among others, the effective masses of each valley, the energy separation between valleys and the non-parabolicity factor.

The electron mobility (μ) is calculated by solving the linearized Boltzmann Transport Equation (BTE). To do it, the implicit solution of the Momentum Relaxation Time (MRT) approximation is used [10]. The electron MRT of the *i*-th subband is calculated as:

$$\frac{1}{\tau_i(k)} = \sum_{i',k'} S_{i,i'}(k,k') \left( \frac{1-f(E')}{1-f(E)} \right) \left( 1 - \frac{\tau_{i'}(k') v_{i'}(k')}{\tau_i(k) v_i(k)} \right) \quad (1)$$

where $S_{i,i'}(k,k')$ is the scattering rate between the initial $(i,k)$ and final $(i',k')$ states, $v_i(k)$ ($v_i(k')$) is the initial (final) electron velocity, $E$ ($E'$) is the initial (final) electron energy, and $f$ is the Fermi occupation function.

Then, the mobility of each subband can be calculated using the Kubo-Greenwood expression:

$$\mu_i = \frac{g_i e}{n_i 2\pi k_B T} \int_{-\infty}^{\infty} dk v_i^2(k) \tau_i(k) f(E) \left(1 - f(E)\right) \quad (2)$$

where $n_i$ is the charge associated to subband $i$, $g_i$ is the valley degeneracy, and the rest of the terms keep their usual meaning.

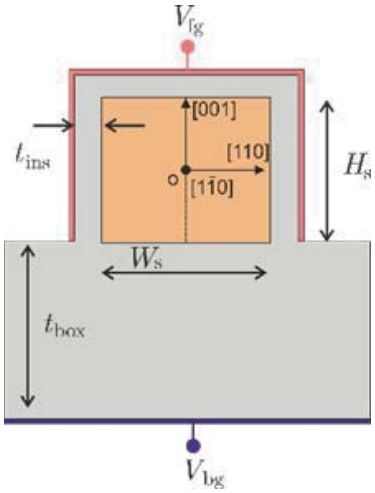



Fig. 1. Trigate cross-section with the main geometrical parameters. The device transport direction is [1-10].

The scattering rate in Eq. (1) is evaluated taking into account the main scattering mechanisms, namely: surface roughness (SR) [11,12], interfacial coulomb dispersion (CO), bulk acoustic and optical phonons (PH) [13] and, for InGaAs also polar optical phonons (POP) [14] and alloy disorder (AD) [15]. For SR, AD and CO, tensorial dielectric screening has been taken into account, following the approach derived in [9], which has been modified appropriately to take into account the non-cylindrical shape of the devices under consideration. The main parameters corresponding to the scattering mechanisms are listed in Table I.

The simulator has been validated against experimental data elsewhere, both for electrostatic analysis and for mobility calculations [16,17].

The device geometry considered in this work is shown in Fig. 1. The main parameters are the semiconductor width ($W_S$) and height ($H_S$), and the insulator and buried oxide thicknesses, $t_{ins}$ and $t_{box}$, respectively. The trigate geometry considered is rectangular and the insulator thickness has been considered constant for the top and lateral interfaces. The devices are oriented along the [011] direction and fabricated on a (100)-wafer. Therefore, different channel orientations are obtained for the top and lateral interfaces as depicted in Fig. 1. We have taken this fact into account in the modeling of SR by increasing the SR root mean square value from 0.4nm in the top interface to 0.5nm in the lateral sides.

## III. Electrostatic Results

The behavior of InGaAs Trigates with $H_S$=30nm and $W_S$ values ranging from 5nm to 20nm is analyzed as a function of the back-gate bias. For benchmarking purposes, Si devices are also considered. For InGaAs, $TaSiO_x$ was employed as front ($t_{ins}$=2.5nm) and buried insulator (with $t_{box}$ =20nm and 40nm). For Si, $SiO_2$ was used and the insulator thickness was calculated assuming the corresponding EOTs [19]. The buried oxide thickness was also scaled using the planar expression for the EOT.

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $m_{\Gamma}$ (InGaAs) | $0.046m_0$ | $E_g$ (InGaAs) | 0.81eV |
| $m_{l,L}$ (InGaAs) | $1.661m_0$ | $\Delta E_c$ (InGaAs-$TaSiO_x$) | 1.97eV |
| $m_{t,L}$ (InGaAs) | $0.115m_0$ | $m_{l,\Delta}$ (Si) | $0.91\ m_0$ |
| $\Delta E_{\Gamma\text{-}L}$ (InGaAs) | 0.75eV | $m_{t,\Delta}$ (Si) | $0.19\ m_0$ |
| $\alpha_{\Gamma}$ (InGaAs) | $1\ eV^{-1}$ | $\alpha_{\Delta}$ (Si) | $0.5eV^{-1}$ |
| $\alpha_L$ (InGaAs) | $0.5\ eV^{-1}$ | $E_g$ (Si) | 1.11eV |
| $\Delta E_c$ (Si-$SiO_2$) | 3.17eV | Top SR $\Delta_{sr}$ | 0.4nm |
| Alloy Dis. $V_0$ | 0.528eV | Lat. SR $\Delta_{sr}$ | 0.5nm |
| $N_{it}$ ($cm^{-2}$) | $5\times10^{11}$ | SR $L_{sr}$ | 1.5nm |

Table I. Relevant Si and InGaAs parameters: effective mass (m), non-parabolicity factor (α), valley gap ($\Delta E_{\Gamma\text{-}L}$), potential barrier with the insulator ($\Delta E_c$) and energy gap ($E_g$). Non-polar phonons and Coulomb parameters are taken from [13] (Si) and [18] (InGaAs). AD is implemented as proposed in [15].

Figure 2 (right) plots the threshold voltage ($V_T$) as a function of the back gate bias ($V_{bg}$). Figure 2 (left) depicts the body factor value ($\gamma = \Delta V_T/\Delta V_{BG}$) as a function of the device width. A lower body factor (γ) is observed in thinner devices due to the poorer control of the back-gate voltage on the device channel. However, the scenario changes when the device size is increased and γ values close to 40mV/V can be achieved for a $t_{box}$=20nm, $W_S$=20nm InGaAs trigate. These values are considerably higher than those achieved for Silicon structures with similar $t_{ins}/t_{box}$ ratio and device heights [7], as depicted in the figure.

This behavior is mainly due to the electron charge distribution, which is plotted in Fig. 3 for the $W_S$=20nm device, at two different back-gate biases (±2V). As can be observed, for the InGaAs device the charge is further from the front-gate interface and also from the lateral interfaces than in Silicon. This is due to the smaller confinement effective mass, as it has been already discussed that lower values of this parameter produce higher values of the charge centroid distribution [16]. As a consequence, there is a stronger influence of the back-gate bias and therefore an increased body factor.

## IV. Mobility Results

In this Section, we analyze the influence of the back gate bias on the electron mobility of InGaAs and Si trigate devices.

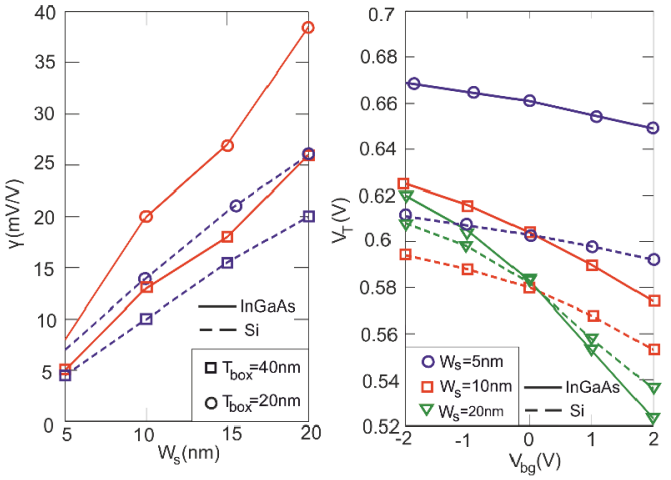



Fig. 2. Body factor as a function of $W_S$ (left) and $V_T$ vs. $V_{bg}$ (right) for InGaAs and Si trigates with $H_S$=30nm. $TaSiO_x$ (SiO2) is used as gate and buried insulator for InGaAs (Si) devices.

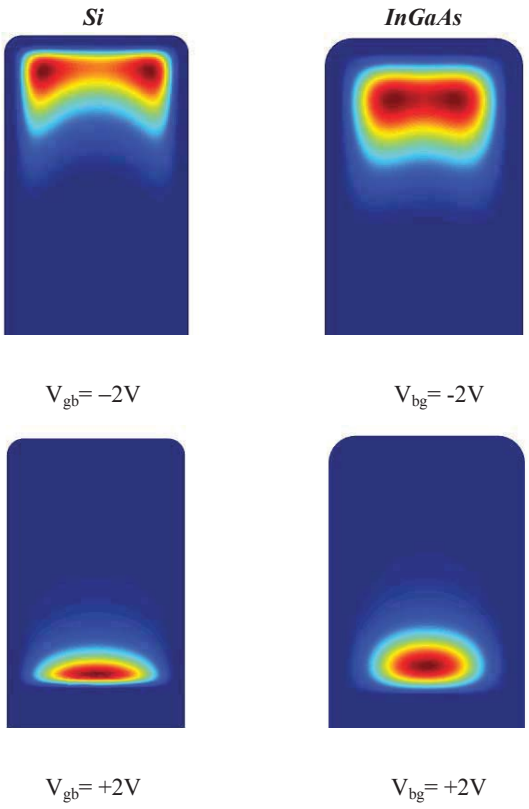



Fig. 3. Normalized charge distribution for Si and InGaAs devices with $V_{bg}$=±2V. $W_S$=20nm and $N_i$=1.25 x $10^{11}$ $cm^{-2}$.

Figure 4 shows the mobility as a function of the electron density ($N_i$) for InGaAs and Si devices. For the $W_S$=5nm devices, μ basically remains unchanged in both InGaAs and Si trigates. However, for $W_S$=20nm, it can be seen that positive $V_{bg}$ values help to improve μ for large $N_i$ values in both materials, but causes a strong degradation of the mobility at low $N_i$ values for InGaAs. In general, Si devices show a more moderate dependence on $V_{bg}$ than InGaAs ones (note the logarithmic scale and the different range of μ).

Analyzing the mobility associated to each of the scattering mechanisms (shown in Fig. 5), it can be concluded that SR scattering shows the strongest dependence on $V_{bg}$ among all the considered mechanisms, especially for the wider devices. Therefore, the changes on μ for the InGaAs devices can be explained according to the redistribution of the charge in the device and its proximity to the semiconductor-insulator interfaces as the back gate bias is modified.

## V. Conclusions

Dynamic control of the threshold voltage as a function of the back gate bias has been analyzed as a function of the geometry and the channel material, demonstrating a higher influence as the device width to height ratio is increased, and a stronger impact on InGaAs devices than in their Si counterparts. The role of the back gate bias on the mobility has also been analyzed: for wide devices, and in the whole range of Ni values, the influence of the back gate bias is higher in InGaAs than in Si trigates.

## Acknowledgment

This work is supported by the Spanish Government under the Project FIS2011-26005. J. M. Gonzalez-Medina, Alejandro Toral and E. G. Marin also acknowledge the University of Granada for the funding through the Plan Propio and CEI-BioTiC P7-2015 project.

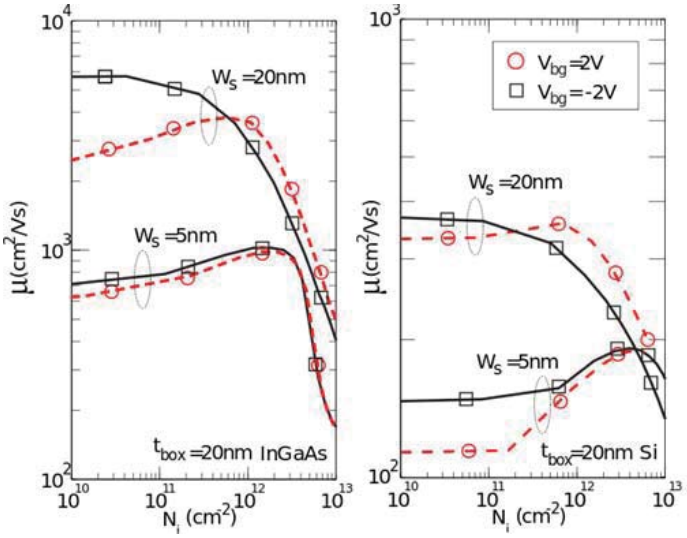



Fig. 4. Influence of the back-gate bias on μ for InGaAs (left) and Si (right) trigates, for $W_S$=5nm and 20nm, and $V_{bg}$=±2V as a function of the electron density.

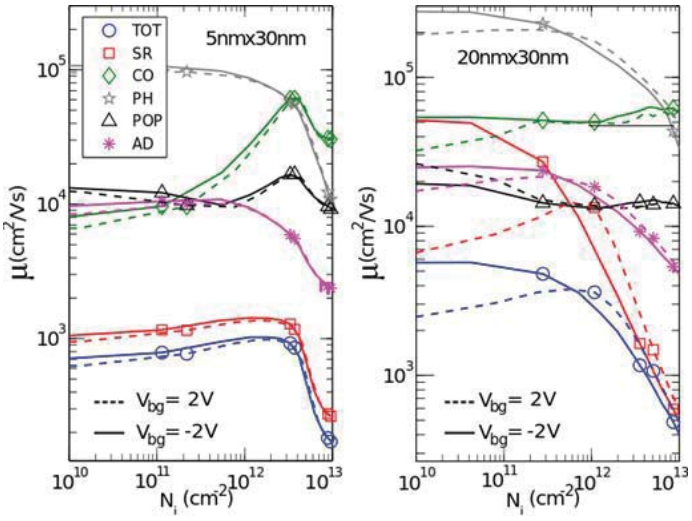



Fig. 5. Contribution of each scattering mechanism to the mobility of InGaAs trigates with $W_S$=5nm (left) and $W_S$=20nm (right).

## REFERENCES


[1] B. Doyle *et al.*, "Tri-gate fully-depleted CMOS transistors: Fabrication, design and layout," in *Symp. VLSI Technol. Dig. Tech. Papers*, Jun. 2003, pp. 133–134.

[2] T. Nagumo and T. Hiramoto, "Design guideline of multi-gate MOSFETs with substrate-bias control," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 3025–3031, Dec. 2006.

[3] C. Tanaka K. Uchida M. Saitoh, K. Ota, and T. Numata, "10 nmdiameter tri-gate silicon nanowire MOSFETs with enhanced high-field transport and *V*th tunability through thin BOX," in *Proc. Symp. VLSI Technol.*, Jun. 2012, pp. 11–12.

[4] K. Ota, M. Saitoh, C. Tanaka, and T. Numata, "Threshold voltage control by substrate bias in 10-nm-diameter tri-gate nanowire MOSFET on ultrathin BOX," *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 187–189, Feb. 2013.

[5] T. Ohtou, T. Saraya, and T. Hiramoto, "Variable-body-factor SOI MOSFET with ultrathin buried oxide for adaptive threshold voltage and leakage control," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 40–47, Jan. 2008.

[6] F. Daugé *et al.*, "Coupling effects and channels separation in FinFETs," *Solid-State Electron.*, vol. 48, no. 4, pp. 535–542, 2004.

[7] E. G. Marín, F. G. Ruiz, A. Godoy, I. M. Tienda-Luna, C. Martinez-Blanque, F. Gámiz, "Impact of the back-gate biasing on trigate MOSFET electron mobility", *IEEE Trans. Electron Devices*, vol. 62, no. 1, pp.224-227, 2015.

[8] J. A. del Álamo, "Nanometre-scale electronics with III–V compound semiconductors," *Nature*, vol. 479, pp. 317–323, Nov. 2011.

[9] S. Jin, M. V. Fischetti, and T.-W. Tang, "Modeling of electron mobility in gated silicon nanowires at room temperature: Surface roughness scattering, dielectric screening, and band nonparabolicity," *J. Appl. Phys.*, vol. 102, no. 8, p. 083715, Oct. 2006.

[10] E. G. Marín, F. G. Ruiz, A. Godoy, I. M. Tienda-Luna and F. Gámiz, "Implicit versus explicit momentum relaxation time solution for semiconductor nanowires", *J. App. Physics,* vol. 108, 024504, 2015.

[11] S. Jin, S.-M. Hong, W. Choi, K.-H. Lee, and Y. Park, "Coupled drift-diffusion (DD) and multi-subband Boltzmann transport equation (MSBTE) solver for 3D multi-gate transistors," in *Proc. Int. Conf. Simulation Semiconductor Process. Devices (SISPAD)*, Sep. 2013, pp. 348–351.

[12] Z. Stanojevic and H. Kosina, "Surface-roughness-scattering in nonplanar channels: The role of band anisotropy," in *Proc. Int. Conf. Simulation Semiconductor Process. Devices (SISPAD)*, Sep. 2013, pp. 352–355.

[13] M. V. Fischetti, "Monte Carlo simulation of transport in technologically significant semiconductors of the diamond and zinc-blende structures. I. Homogeneous transport," *IEEE Trans. Electron Devices*, vol. 38, no. 3, pp. 634–649, Mar. 1991.Marin, J. App. Phys. 118:024504, 2015.

[14] T. Wang, T. H. Hsieh, and T. W. Chen, "Quantum confinement effects on low-dimensional electron mobility," *J. Appl. Phys.*, vol. 74, no. 1, p. 426, 1993.

[15] A.-T. Pham, C. Jungemann, and B. Meinerzhagen, "Physics-based modeling of hole inversion layer mobility in strained-SiGe-on-insulator", *IEEE Trans. Electron Devices*, vol. 54, pp. 2174, 207.

[16] E. G. Marin, F. G. Ruiz, A. Godoy, I. M. Tienda-Luna, C. Martínez Blanque, F. Gámiz, "Theoretical interpretation of the electron mobility behavior in InAs nanowires", *J. App. Phys.*, 116:175405, 2014.

[17] E. G. Marin, F. G. Ruiz, A. Godoy, I. M. Tienda-Luna, F. Gámiz, "Mobility and capacitance comparison in scaled InGaAs vs. Si trigate MOSFETs", *IEEE Elec. Dev. Lett.* 36:114, 2015;

[18] J. Kim and M. V. Fischetti, "Electronic band structure calculations for biaxially strained Si, Ge, and III–V semiconductors," *J. Appl. Phys.*, vol. 108, no. 1, p. 013710, Jul. 2010.

[19] F. G. Ruiz, I. M. Tienda-Luna, L. Donetti, A. Godoy, F. Gámiz, "Equivalent Oxide Thickness of trigate SOI MOSFETs with high-k insulators", *IEEE Trans. Elec. Devices*, vol. 56, no. 11, pp. 2711-2719, 2009.

# Influence of quantum confinement effects and device electrostatic driven performance in ultra-scaled $Si_xGe_{1-x}$ nanowire transistors

Talib Al-Ameri, V. P. Georgiev, F. Adamu-Lema, X. Wang, and A. Asenov
Device Modeling Group, School of Engineering, University of Glasgow, G12 8LT, U.K.
*t.ali.1@research.gla.ac.uk*

***Abstract*— In this work we have investigated the impact of quantum mechanical effects on the device performance of n-type in ultra-scaled $Si_xGe_{1-x}$ nanowire transistors (NWT) for possible future applications. For the purpose of this paper $Si_xGe_{1-x}$ NWTs with different $Si_xGe_{1-x}$ molar fraction has been simulated. However, in all devices the cross-sectional area, dimensions and doping profiles are kept constant in order to provide fair comparison. The design of computational experiment in this work includes nanowire transistors with different gate length of 6nm, 8nm, 10nm, 12nm and 14nm. All wires are simulated with various $Si_xGe_{1-x}$ ratio. As a result we have established a correlation between the mobile charge distribution in the channel and gate capacitance, drain induced barrier lowering (DIBL) and the sub-threshold slope (SS). The mobile charge to gate capacitance ratio, which is an indicator of the intrinsic speed of the NWTs, is also have been investigated. More importantly all calculations are based on quantum mechanical description of the mobile charge distribution in the channel. This description is based on Schrödinger equation, which is indeed preferred approach for nanowires with such ultra-scale dimensions.**

***Keywords*— CMOS, $SixGe_{1-x}$, electrostatics, nanowire transistors, performance, quantum effects, TCAD**

## I. INTRODUCTION

The gate-all-around (GAA) silicon nanowire FET structure has the potential of keeping Moore's law applicable beyond sub-5nm CMOS technology. They are being investigated as an option near the end and beyond the current International Technology Roadmap for Semiconductors (ITRS) [1-4]. In such ultra-scaled dimensions the quantum mechanical nature of the charge carriers play an important role which dictates the device behaviour and performance. Some of the quantum mechanical effects are related to charge confinement in the direction perpendicular to the transport. As a result, threshold voltage shift is introduced which is directly correlated to reducing the gate-to-charge capacitance and the charge in the channel available for transport. Therefore, accurate description of quantum mechanical effects in such ultra-scaled devices is indeed mandatory [5-11].

Moreover, various combinations of device architecture and channel materials have been investigated in order to improve the transistor's performance [12]. One possibility is to replace the *Si* channel with Germanium-(*Ge*). *Ge* is of renewed interest as a semiconductor material to complement silicon due to its higher carrier mobility and the trend in gate dielectrics evolution [13]. *Ge* is also compatible to the existing CMOS technology which makes it easy to integrate. Moreover, using different ratio of *Si* and *Ge*, $Si_xGe_{1-x}$, can lead to improvement of the material properties and the performance of nanowire transistors (NWT) [13]. Our main aim in this paper is to establish a link between different molar ratio of *Si* and *Ge* channel and electrostatic performance on ultra-scaled NWTs, taking into account the quantum confinement effects.

## II. DEVICE STRUCTURE

In this paper we consider an n-type test structure of $Si_xGe_{1-x}$ NWT. All devices have a cylindrical cross-section with diameter of D = 4 nm which is similar to our recently published work [14], [16]. The channel has a low doping concentration in the gate region and it is warped with a high-k oxide material (Hafnium) while the source and drain region are relatively highly doped. The $Si_xGe_{1-x}$ molar fraction which is the amount of a constituent (expressed in moles), divided by the total amount of all constituents in a mixture are varied from 10% to 90% for booth *Si* and *Ge* in order to find the optimal electrostatic confinement and performance. The transport direction is along <110> crystallographic orientation. All NWTs have effective oxide thickness of $t_{ox}$= 0.8nm, gate length 6, 8, 10, 12 and 14 nm, spacer thickness of 5nm, source/drain doping peak of $2\times10^{20}$ $cm^{-3}$ and channel doping of $10^{15}$ $cm^{-3}$. 3D view and the design parameters for all simulated devices are presented in Fig. 1 and Table 1 respectively.

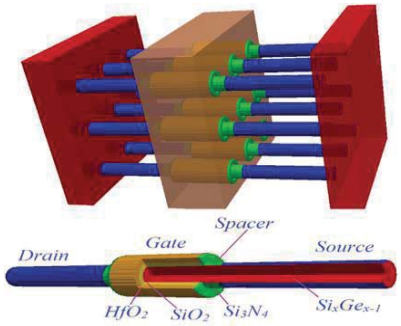



Fig. 1 3D schematic view of the circular NWT (down) and NWTs array (up).

## III. SIMULATION METHOD

Our simulations are based on a Poisson-Schrödinger (PS) quantum correction technology achieved in a drift-diffusion (DD) module of the GSS 'atomistic simulator' GARAND [15].

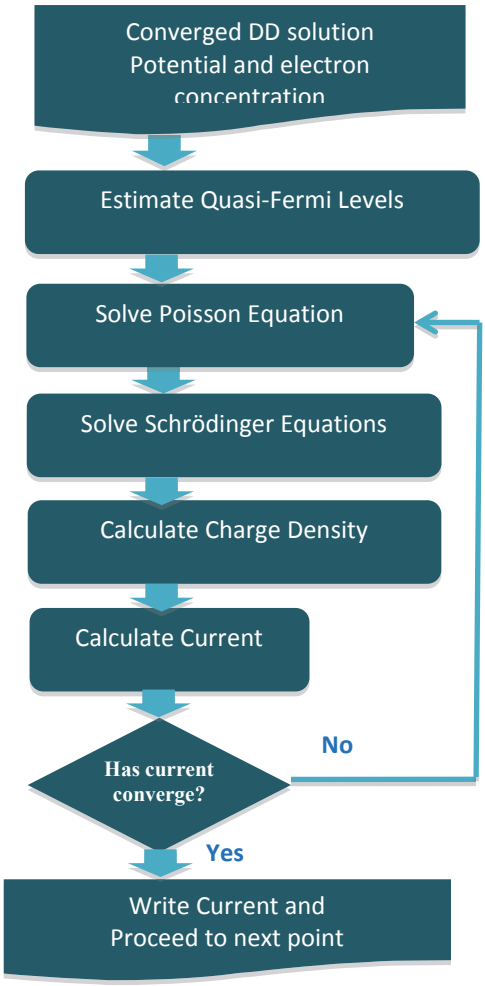



Fig. 2 Flow diagram of the Poisson-Schrödinger model in GARAND simulator.

The PS model is coupled with the GARAND drift-diffusion (DD) solution in stages to allow a computationally efficient manner of combining the impact of quantum confinement and carrier transport (as shown Fig .2). To achieve this, the DD simulation is carried out until convergence, then the quasi-Fermi level from the converged DD solution is used as a fixed reference within the PS model to transfer the current transport behavior. The PS model is then solved until convergence to obtain a QM solution of the charge density. After this the QM charge density is used to obtain a fixed 'quantum correction' term. Using the fixed 'quantum correction' the DD simulation is carried out again until convergence is obtained.

Quantum corrections is included within drift diffusion simulation through the solution of the density gradient equation. This is coupled with both the non-linear Poisson and current continuity solutions and applied to both majority and minority carrier distributions. The quantum corrections modify the carrier distribution in regions of high carrier density variation. The modified carrier density then set an effective quantum potential, applied in the solution of the current-continuity equation. In this way the charge distribution in the NWT's cross section identical to the charge distribution obtained from the Solution of the Schrodinger equation. The simulations are finished when the current converges.

| | |
|---|---|
| $T_{oxide}$ (nm) | 0.8 |
| Gate Diameter (nm) | 4 |
| Gate length (nm) | 14 |
| Spacer thickness (nm) | 5.0 |
| S/D peak doping ($cm^{-3}$) | $2\times10^{20}$ |
| Channel doping ($cm^{-3}$) | $10^{15}$ |
| Substrate orientation | 001 |
| Nanowire orientation | 110 |
| Channel material | $Si_xGe_{1-x}$ |
| Drain voltages (V) | 0.05V, 0.7V |

Table 1 Parameters of the simulated devices.

| | $Q_M$ ($\times10^6$/cm) | $C_G$ ($10^{-11}$F/cm) | $Q_M/C_G$ ($10^{17}$/F) |
|---|---|---|---|
| *Si* | 1.13008 | 3.864140 | 2.92453 |
| $Si_{90}Ge_{10}$ | 1.15170 | 3.897476 | 2.95499 |
| $Si_{80}Ge_{20}$ | 1.15990 | 3.927255 | 2.95346 |
| $Si_{70}Ge_{30}$ | 1.16580 | 3.953547 | 2.94874 |
| $Si_{60}Ge_{40}$ | 1.17150 | 3.976392 | 2.94614 |
| $Si_{50}Ge_{50}$ | 1.17870 | 3.999063 | 2.94744 |
| $Si_{40}Ge_{60}$ | 1.18690 | 4.014751 | 2.95635 |
| $Si_{30}Ge_{70}$ | 1.19790 | 4.026970 | 2.97469 |
| $Si_{20}Ge_{80}$ | 1.21280 | 4.03570 | 3.00517 |

Table 2 $Q_M(V_G=0.60V)$, $C_G$ ($V_G=0.60V$) and $Q_M/C_G$ ratio at identical $Q_M(G_V=0V)$ for NWTs at $L_G=14nm$.

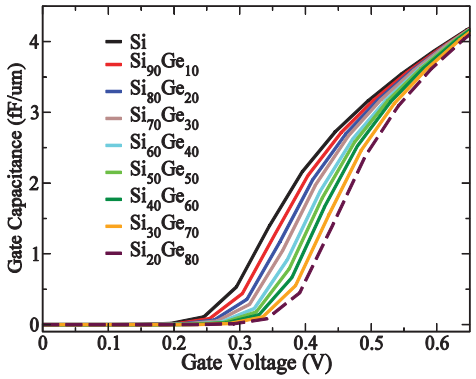



Fig. 3 Gate voltage dependence of the capacitance of all gate-all-around NWTs at $L_G$=14 nm channel length.

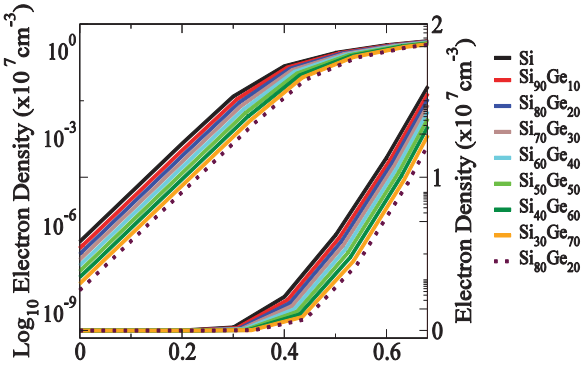



Fig. 4 Gate voltage dependence of the mobile charge of all gate-all-around NWTs at $L_G$=14 nm channel length.

## IV. Results and Discussion

Fig. 3 shows the capacitance-voltage (C-V) characteristics for all simulated NWTs. Fig. 4 presents the gate voltage dependence of the mobile charge in the channel. As expected the mobile charge ($Q_M$) and the gate capacitance ($C_G$) increases with increasing gate voltage. Moreover, both the $Q_M$ and $C_G$ reveal their dependence on the *Si/Ge* molar fraction. In order to evaluate objectively the impact of the *Si/Ge* concentrations on the NTW's performance, Table 2 compares $Q_M$ *and* $C_G$ ($V_G$=0.60V) for identical $Q_M$ ($V_G$=0.0V). To make this comparison fairer, the $Q_M$ ($V_G$) curves are aligned by modifying the gate work function.

From Table 2 the following important conclusions can be obtained. Firstly, $Si_{20}Ge_{80}$ has the highest $C_G$ and $Q_M/C_G$ ratio and consistently the lowest value is for pure Si wire. Secondly, increasing *Ge* concentration leads to almost linear increase of $Q_M/C_G$ ratio. $Q_M/C_G$ ratio is an indicator for the 'intrinsic' NWT's speed. Higher value of the ratio means better 'intrinsic' speed.

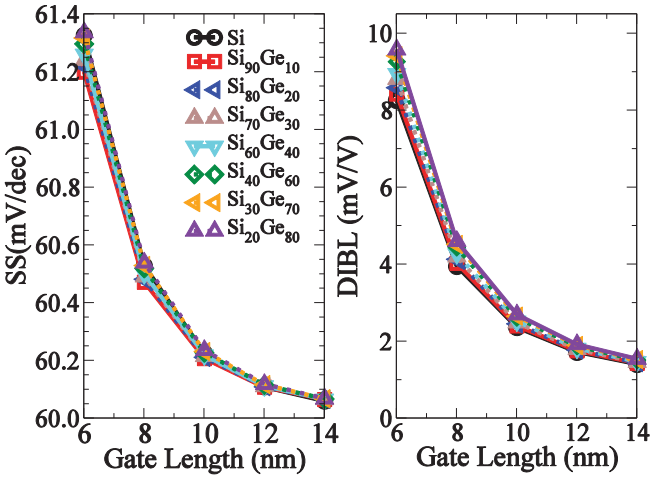



Fig. 5 Impact of the gate length on the SS (left) and DIBL (right) for all NWTs with different $SixGe1_{-x}$ molar fraction.

The impact of the gate length on the drain-induced barrier lowering (DIBL), defined as $\Delta V_T/\Delta V_D$, and sub-threshold slope (SS) is illustrated in Fig. 5. There is a relatively little difference in the electrostatic behavior between the NTWs with different *Si/Ge* fraction. Both DIBL and SS increase with decreasing the gate length of the devices. However, there is no significant difference between the values for both descriptors at each gate length. Also the difference in SS and DIBL values increases with decreasing of the gate length.

Fig. 6 presents the electron concentration and electrostatic potential for all devices along the transport direction. From the figure is clearly visible that the main difference between the devices is in the channel region. Also the charge in the channel and the potential increase with increasing *Si* concentration. Fig. 7 reveals the 2D charge distribution in the middle of the channel for all devices. The data show that the charge difference is not significant between various NWTs

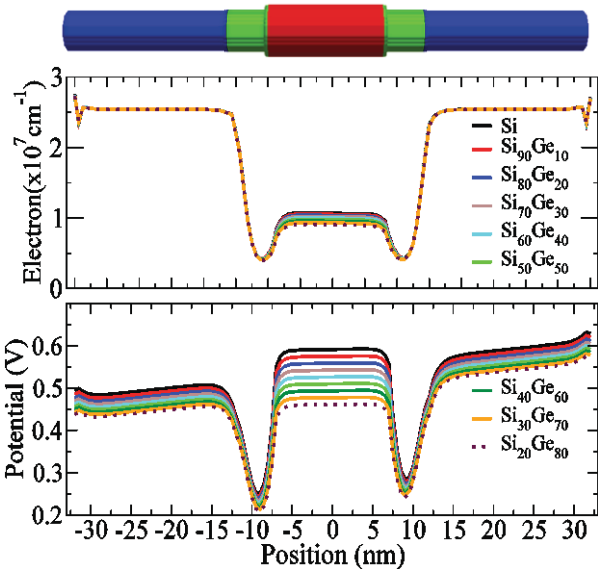



Fig. 6 Electron concentration (top) and electrostatic potential (down) along the transport direction of $Si_xGe_{1-x}$ NWTs at $V_D$=0.05 and $V_G$=0.6V. The concentration is obtained by integrating in the plane perpendicular to the transport direction.

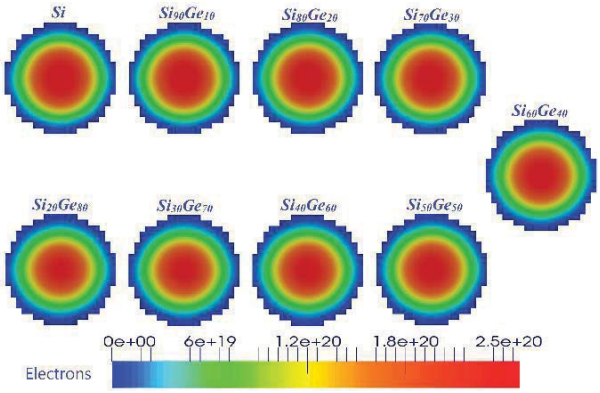



Fig. 7 2D charge distributions, in the middle of the channel, obtained for the $Si_xGe_{1-x}$ NWTs with deferent Si/Ge concentration.

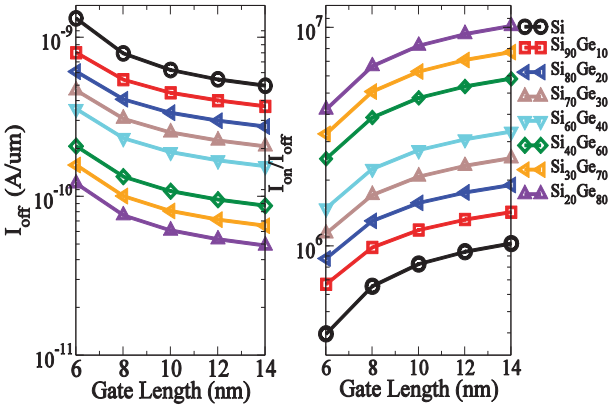



Fig. 8 The impact of different molar ratio of Si and Ge on $I_{on}/I_{off}$ (right) and on the leakage current $I_{off}$ (left).

and the quantum simulations capture the well-known volume inversion effects.

Fig 8 reveals the impact of channel length on $I_{off}$ at low drain voltage $V_D$=0.05V and gate voltage $V_G$=0.6V for the Silicon NWTs in addition to seven different $Si_xGe_{1-x}$ molar fraction. As it is expected reducing the channel length leads to decrease in the leakage current for all simulated devices. Additionally, increasing the *Ge* concentration in the channel reduces the leaked current as wll. For example, silicon channel with 14 nm gate length has the worst $I_{off}$ around $5x10^{-10}$ A/μm while $Si_{20}Ge_{80}$ shows the lowest (the best) leakage current about $5x10^{-11}$ A/μm for the same gate bias and and gate length. The right hand side of Fig. 8 shows the impact of channel length on $I_{on}/I_{off}$ which has a positive effect on the device performance.

Similarly, to the discussion in the above, the $Si_{20}Ge_{80}$ devices show the best Ion/Ioff performance in comparison to all other wires. For example at 14 nm gate length the Ion/Ioff ration for $Si_{20}Ge_{80}$ is around $10^7$ while for the silicon transistor is just bellow $10^6$. This ration decreases with decreasing of the channel length but more importantly the trend is consistent for all devices.

## V. Conculution

In this paper we have studied the impact of quantum mechanical effects on the electrostatic driven performance of $Si_xGe_{1-x}$ NWTs at the sub 5-nm CMOS technology. By varying the *Si/Ge* molar fraction in NWTs, we have established a link between the quantum confinement effects and the electrostatics properties in those devices. We also discuss properties such as DIBL and sub threshold slop SS. Based on our computational experiments we can conclude that the NTW with $Si_{20}Ge_{80}$ molecular share has the highest $Q_M/C_G$ ratio, the lowest DIBL and sub threshold slop (SS), which makes it the best choice from all investigated devices.

## VI. Referances


[1] K. J. Kuhn, "Considerations for Ultimate CMOS Scaling," *IEEE Transactions on Electron Devices*, vol. 59, pp. 1813 - 1828, 16 May 2012.

[2] N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, *et al.*, "High-performance fully depleted silicon nanowire (diameter < 5 nm) gate-all-around CMOS devices," *Electron Device Letters, IEEE,* vol. 27, pp. 383-386, 2006.

[3] W. Lu, P. Xie, and C. M. Lieber, "Nanowire Transistor Performance Limits and Applications," *IEEE Transactions on Electron Devices,* vol. 55, pp. 2859-2876, Nov. 2008.

[4] E. G. Marin, F. J. G. Ruiz, and I. M. Tienda-Luna, "Analytical Gate Capacitance Modeling of III–V Nanowire Transistors," *IEEE Transactions on Electron Devices,* vol. 60, pp. 1590 - 1599, 02 April 2013 2013.

[5] H. Takeda and N. Mori, "Three-dimensional quantum transport simulation of ultra-small FinFETs," in *Computational Electronics, 2004. IWCE-10 2004. Abstracts. 10th International Workshop on*, 2004, pp. 91-92.

[6] Y. Yamada, H. Tsuchiya, and M. Ogawa, "Quantum Transport Simulation of Silicon-Nanowire Transistors Based on Direct Solution Approach of the Wigner Transport Equation," *Electron Devices, IEEE Transactions on,* vol. 56, pp. 1396-1401, 2009.

[7] S. Sung Dae, L. Sung-Young, K. Sung-Min, Y. Eun-Jung, M.-S. Kim, L. Ming, *et al.*, "High performance 5nm radius Twin Silicon Nanowire MOSFET (TSNWFET) : fabrication on bulk si wafer, characteristics, and reliability," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, 2005, pp. 717-720.

[8] G. Chindalore, S. A. Hareland, S. A. Jallepalli, A. F. Tasch, C. M. Maziar, V. K. F. Chia, *et al.*, "Experimental determination of threshold voltage shifts due to quantum mechanical effects in MOS electron and hole inversion layers," *Electron Device Letters, IEEE,* vol. 18, pp. 206-208, 1997.

[9] V. P. Georgiev, E. A. Towie, and A. Asenov, "Impact of Precisely Positioned Dopants on the Performance of an Ultimate Silicon Nanowire Transistor: A Full Three-Dimensional NEGF Simulation Study," *IEEE Transactions on Electron Devices,* vol. 60, pp. 965-971, Mar 2013.

[10] S. U. Z. Khan and M. S. Hossain, "Impact of high-κ gate dielectric and other physical parameters on the electrostatics and threshold voltage of long channel gate-all-around nanowire transistor," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields,* vol. 28, pp. 389–403, 8 SEP 2014 2015.

[11] M. Bescond, "Quantum transport in semiconductor nanowires," in *Semiconductor Nanowires: Material, Synthesis, Characterization and Applications*, ed: Woodhead Publishing, 2015.

[12] J.-W. Lee and H.-M. Chou, "Silicon-Germanium Structure in Surrounding-Gate Strained Silicon Nanowire Field Effect Transistors," *Journal of Computational Electronics*, vol. 3, pp. 251-255, October 2004.

[13] D. Wang, Q. Wang, and A. Javey, "Germanium nanowire field-effect transistors with $SiO_2$ and high-k $HfO_2$ gate dielectrics," *Applied Physics Letters,* vol. 83, pp. 2432-2434, 22 September 2003.

[14] T. Al-Ameri, V. Georgiev, F. Adamu-Lema, X. Wang, and A. Asenov, "Correlation Between Gate Length, Geometry and Electrostatic Driven Performance in Ultra-Scaled Silicon Nanowire Transistors," in IEEE Nanotechnology Materials and Devices Conference (NMDC), 2015, pp. 23-27.

[15] "http://www.GoldStandardSimulations.com."

[16] Y. Wang and *et al.*, "Simulation Study of the Impact of Quantum Confinement on the Electrostatically Driven Performance of N-type Nanowire Transistors," *IEEE Transactions on Electron Devices*, vol. 62, pp. 3229 - 3236, 2015

# Scanning Microwave Microscopy for Non-Destructive Characterization of SOI Wafers

L. Michalas[1], I. Ionica[2], E. Brinciotti[3], L. Pirro[2], F. Kienberger[3], S. Cristoloveanu[2] and R. Marcelli[1]

[1] National Research Council, Institute for Microelectronics and Microsystems (CNR-IMM)
Via del Fosso del Cavaliere 100, 00133 Rome, Italy
loukas.michalas@artov.imm.cnr.it

[2] IMEP-LAHC, Minatec, Grenoble-INP, Univ. de Grenoble Alpes, CNRS-UMR 5130
3 Parvis Louis Néel - CS 50257, F-38016 Grenoble, France
irina.ionica@imep.grenoble-inp.fr

[3] Keysight Technologies Austria GmbH
Gruberstrasse 40, 4020, Linz, Austria
Enrico_Brinciotti@keysight.com

***Abstract*— The paper presents an experimental study aiming to highlight the potential of scanning microwave microscopy (SMM) as a non-destructive high precision characterization tool for SOI technology. Two identical SOI wafers having passivated and non-passivated top Si film surfaces have been assessed. Differential microwave measurements were found capable of detecting differences in the structures of the two samples. The results support the conclusion that, after appropriate calibration method, SMM may provide a powerful tool offering nm scale characterization for SOI technology.**

***Keywords—Scanning Microwave Microscopy (SMM);Silicon On Insulator (SOI); interface quality; nanoscale characterization.***

## I. Introduction

State of the art ultra-thin Silicon-On-Insulator (SOI) substrates require novel experimental techniques able to provide high sensitivity, non-destructive characterization, for evaluation of interfaces quality and of other parameters such as local thickness variation. This can be effectively achieved by the implementation of non-contact optical methods, as recently demonstrated [1,2]. Beyond the optical wavelengths, microwaves can also offer a useful tool to that final goal.

Scanning Microwave Microscopy (SMM) is a technique that provides high sensitivity non-destructive, subsurface, point-wise characterization with nanometer scale lateral resolution. This is achieved by applying a microwave signal through a sharp tip, to the material or the device under investigation and recording the response. For this, numerous microwave microscope configurations have been proposed [3-7]. In one of the late setups [5,7], the microwave signal, provided by a vector network analyzer (VNA), is applied to the device under test (DUT) through a modified atomic force microscope (AFM), using a specially designed tip. The tip may be placed in contact or in proximity to the surface of the DUT. The response of tip/sample system to the incident wave is determined in this case by the local properties of the studied material, but also by the properties beyond the top surface, since microwaves may penetrate inside. This way, the technique takes advantage of the high capabilities of both AFM and VNA and may provide high precision non-destructive characterization for the DUT. Operation can be performed in contact and in non–contact mode. A variation of the standard setup also allows transmission measurements, by involving two VNA channels and back illumination, which may provide complementary and in some cases higher sensitivity information [8].

The application of the proper calibration and de-embedding methodology on the measured microwave signals is a very critical step and can lead to the extraction of localized quantitative knowledge on the properties of the DUT. Regarding semiconductor characterization, there is an important interest over the last years for SMM studies on silicon samples having dopant profile structure [9-15]. Beyond semiconductors, SMM is already successfully implemented for the study of novel materials [16] and biological samples [17].

This paper presents the first experimental application of SMM for the characterization of SOI substrates and it mainly aims to highlight SMM potential as a non-destructive characterization tool for state-of-art SOI technology. This study is focused on reflection measurements with contact mode AFM, to monitor the differences between passivated and non-passivated top surface SOI wafers.

## II. Experimental Configuration

### A. Silicon On Insulator Samples

The study is performed on two SOI structures with 88 nm thick Si film on top of 145 nm thick buried oxide (BOX). The first sample is covered with native oxide (non-passivated), while second one has passivated surface with 4 nm dry thermal oxide. Thus the two samples have different density of states at the top surface [18]. The silicon film on top of the BOX is selectively etched in order to create SOI islands. This structure

Partial support from “Marie Curie” project NANOMICROWAVE, under GA:317116.

allows the simultaneous scan of both SOI structure and the BOX area, so that each contribution can be separately assessed.

### *B. Scanning Microwave Microscopy Setup and Measurements*

The Keysight's SMM experimental setup consists of an Atomic Force Microscope (AFM) interfaced with a Performance Network Analyzer (PNA). In our experimental procedure a Keysight´s N5230 PNA was matched with a Keysight´s LS5600 AFM with commercially available platinum tips especially designed for SMM measurements, i.e. Rocky Mountain Nanotechnology 12Pt400B, with a spring constant of 0.3N/m [19]. By choosing the appropriate AFM tip stiffness and setpoint (i.e. tip to sample force), the method can be non-destructive for the surface of the material under investigation, even in contact mode operation.

The device under test is connected to the setup as a properly terminated shunt capacitor, in order to achieve a match between the high tip/sample impedance and the VNA requirements and to take advantage of the very high sensitivity offered by the VNA, if properly connected. Therefore a 50 Ω shunt resistor and a resonator are also integrated in the SMM system (Fig.1).

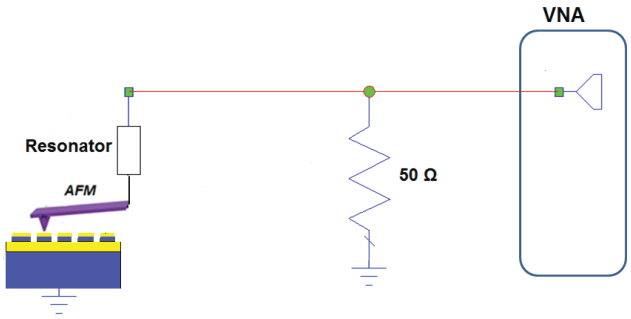



Fig.1 Simplified schematic of the experimental setup.

In our case the two samples were placed next to each other (Fig.2) and were characterized during the same experiment (using the same tip and frequency), to obtain a reliable comparative study by minimizing experimental variations.


Fig.2 Photo of the devices placed on the AFM chuck.

To eliminate topography related cross talk effects (i.e. non local capacitive coupling induced by the topography variation of the sample), the GHz microwave signal is coupled with an additional modulating small signal of frequency typically between 12-20 kHz also applied through the SMM tip. This allows performing differential measurements of the reflection coefficient amplitude $dS_{11}/dV$ and phase $dP_{11}/dV$, with no topographical artifacts superimposed to the signal of interest.

Both samples were characterized using the same setup. The scanned area was defined in a way to include both areas, without and with top silicon film; so that comparison can be performed. A schematic of the sample and of the scanned area is presented in the Fig.3.

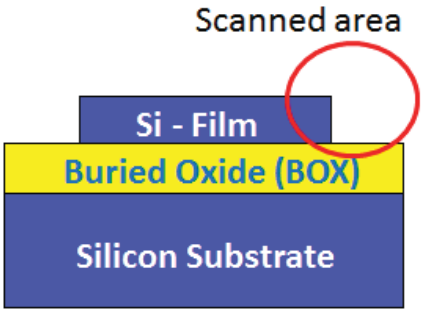



Fig.3 Schematic of the DUT showing the scanned area.

## III. Experimental Results And Discussions

Before scanning the sample, the AFM tip is placed in contact with a point of DUT, and a VNA frequency sweep is performed typically from 1 to 20 GHz (i.e. within the frequency interval which is the current state-of-art for the technology of the SMM probes). For this we have chosen a contact point at the BOX area so that it will not be affected by the differences in the two SOI islands. Multiple resonance frequencies are obtained because of the resonator integrated with the probe. In principle the method can be applied at any frequency close to a resonance notch, however typically higher frequencies offer higher sensitivity. The most appropriate one is chosen between those characterized by best imaging and impedance responses for the performed measurements. Fig. 4 presents the obtained sweep in the range of 18.5 GHz to 20 GHz and the selected notch. The selected fixed frequency for the experimental procedure was 19.05 GHz.

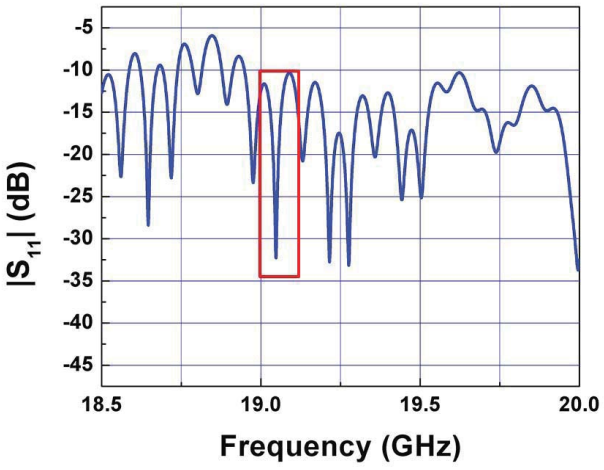



Fig.4 Frequency sweep – selected notch.

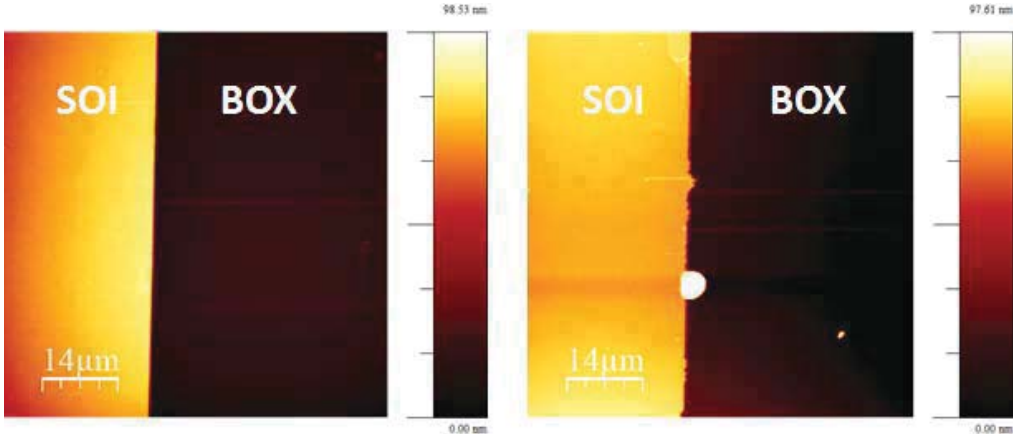



Fig.5 Topography image of (left) passivated and (right) non-passivated sample.

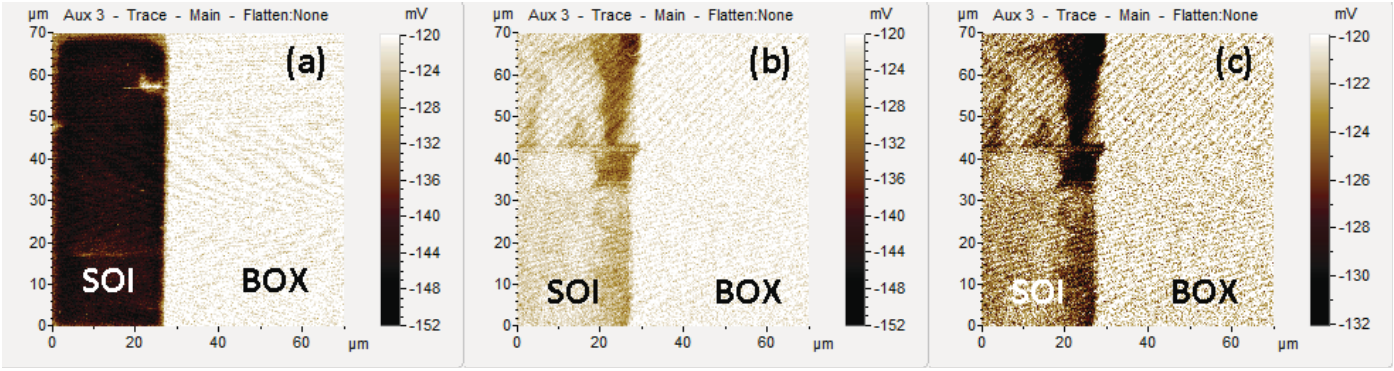



Fig.6 $dS_{11}/dV$ measurements on (a) passivated sample and (b) non-passivated sample using the same color scale levels and (c) non-passivated sample using more detailed scale, having the same "starting" and different "ending" levels. A clear difference between the levels of signals acquired on the SOI parts with respect to the corresponding BOX parts is observed.

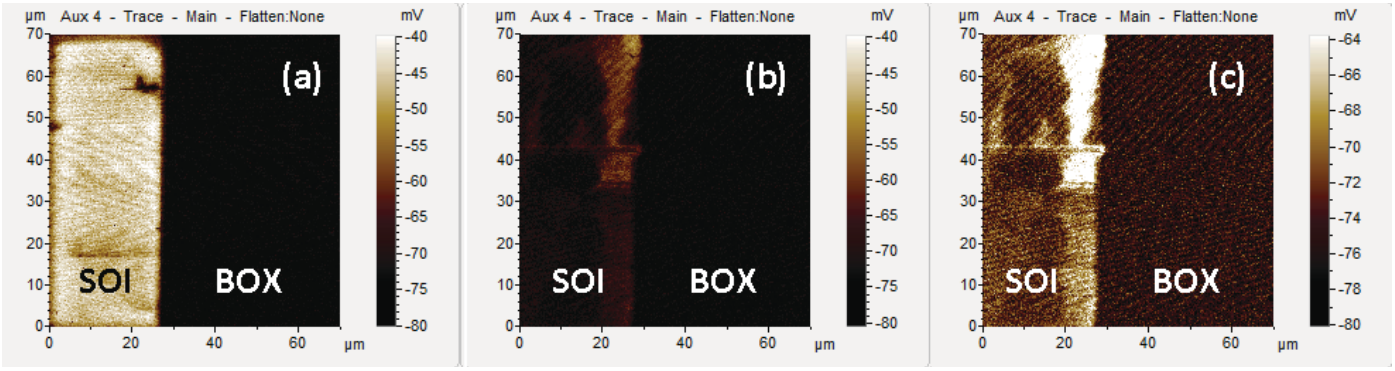



Fig.7 $dP_{11}/dV$ dV measurements on (a) passivated sample and (b) non-passivated sample using the same color scale levels and (c) non-passivated sample using more detailed scale, having the same "starting" and different "ending" levels. A clear difference between the levels of signals acquired on the SOI parts with respect to the corresponding BOX parts is observed.

The experimental obtained results (Fig.6 and Fig.7) clearly demonstrate the subsurface differences between the two SOI samples. The topography measurements (Fig.5) do not reveal any important differences on the two surfaces. To avoid any topographic induced crosstalk in the microwave images, we report the differential $dS_{11}/dV$ measurements, thus we can safely conclude that the differences recorded in microwave signals are not topography but rather material related. Results on passivated samples presented in Fig.6 (a) and Fig.7 (a). Non-passivated samples presented using the same color scale in Fig.6 (b) and Fig.7 (b) and in optimized color scale having the same reference level (BOX) in Fig.6 (c) and Fig.7 (c), for detailed comparison. The position of the Si film step is clearly identified. It is also worth noting that the same level of signal is obtained on the BOX part, in contrast to the levels of signals coming from the SOI island part. The microwave signals acquired on the SOI part of passivated samples (Fig.6 (a) and Fig.7(a)), are more uniform with respect to the non-passivated ones (Fig.6(b),(c) and Fig.7(b),(c)). It should be also noticed that SMM measurements are local, with respect to other characterization techniques and allow detailed mapping of the DUT properties with a lateral resolution in the nanometer scale. Moreover because of the implementation of purposely

fabricated samples with different top Si surfaces, the results present a straightforward experimental verification.

Regarding the interaction of SMM signals with the interface states it should be noted that although a preliminary discussion is already presented in particular for differential $dS_{11}/dV$ measurements, in [11], such interaction is not yet completely clarified. For reflection SMM measurements, the measured microwave coefficient, $S_{11}$ was found to be proportional to the reflective capacitance that interacts with the incident wave [5,9,14,15]. More precisely, in case of contact mode measurements with silicon samples, the metallic (Pt) AFM tip and the semiconductor with the native or purposely grown oxide on top, forms a MOS capacitor. In this case the $dS_{11}/dV$ is sensitive to the slope of the localized C-V in the vicinity of the tip [9,20]; thus includes in this way the corresponding local information.

Finally, although it is clear that additional effort is required for a full calibration study in order to obtain quantitative nanoscale SOI characterization by the SMM technique; this paper presents the first experimental evidence towards this direction and therefore should be considered as a quite promising starting point.

## IV. Conclusions

The paper presents an experimental study aiming to highlight the potential of scanning microwave microscopy (SMM), as a non-destructive characterization tool for silicon on insulator (SOI) technology. The study is focused on reflection and contact mode measurements. The differences between passivated and non-passivated $Si/SiO_2$ interfaces have been clearly monitored. The results constitute a promising starting point towards the conclusion that under the appropriate calibration, SMM may offer nm scale high sensitivity non-destructive characterization for state of the art SOI materials and devices.

## Acknowledgment

The authors wish to acknowledge the partial support from EC by means of “Marie Curie” fellowship in the framework of PEOPLE-2012-ITN project: Microwave Nanotechnology for Semiconductor and Life Science -NANOMICROWAVE, under GA:317116.

## References

[1] B. Jun, Y. V. White, R. D. Schrimpf, D. M. Fleetwood, F. Brunier, N. Bresson, S. Cristoloveanu, and N.H. Tolk., "Characterization of multiple $Si/SiO_2$ interfaces in silicon-on-insulator materials via second-harmonic generation" Appl. Phys. Lett., vol. 85, pp. 3095-3097, 2004.

[2] D. Damianos, L. Pirro, G. Soylu, I. Ionica, V. Nguyen, G. Vitrant, A Kaminski, D. Blanc-Pelissier, L. Onestas, J. Changala, M. Kryger, and S. Cristoloveanu “Second harmonic generation for contactless non-destructive characterization of silicon on insulator wafers” Solid State Electr., in press

[3] C.P. Vlahakos, R.C. Black, S.M. Anlage, A. Amar, and F.C. Wellstood “Near-field scanning microwave microscope with 100μm resolution” Appl. Phys. Lett. Vol. 69, pp. 3272-3274, 1996.

[4] A. Tselev, S.M. Anlage, Z. Ma, and J. Melngailis “Broadband dielectric microwave microscopy on micron length scales” Rev. Scient. Instr. vol.78, 044701, 2007.

[5] H.P. Huber, M. Moertelmeier, T.M. Wallis, C.J. Chiang, M. Hochleitner, A. Imtiaz, Y.J. Oh, K. Schilcher, M. Dieudonne, J. Smoliner, P. Hinterdorfer, S.J. Rosner, H. Tanbakuchi, P. Kabos, and F. Kienberger, “Calibrated nanoscale capacitance measurements using a scanning microwave microscope” Rev. Scient. Instr. vol.81, 113701, 2010.

[6] M. Farina, D. Mencarelli, A. Di Donato, G. Venanzoni, and A. Morini “Calibration protocol for broadband near-field microwave microscopy” IEEE Trans. Microw. Theor. And Techn. Vol. 59, pp. 2769 – 2776, 2011.

[7] T. Dargent, K. Haddadi, T. Larsi, N. Clèment, D. Ducatteau, B. Legrand, H. Tanbakuchi, and D. Theron “An interferometric scanning microwave microscope and calibration method for sub-fF microwave measurements” Rev. Scient. Instr. vol.84, 123705, 2013.

[8] A.O. Oladipo, A. Lucibello, M. Kasper, S. Lavdas, G.M. Sardi, E. Proietti, F. Kienberger, R. Marcelli, and N.C. Panoiu, “Analysis of a transmission mode scanning microwave microscope for subsurface imaging at the nanoscale” Appl. Phys. Lett. vol. 105, 133112, 2014.

[9] J. Smoliner, H.P. Huber, M. Hochleitner, M. Moertelmaier, and F. Kienberger, “Scanning microwave microscopy/spectroscopy on metal-oxide-semiconductor systems” J. Appl. Phys. vol. 108, 064315, 2010.

[10] I. Humer, H.P. Huber, F. Kienberger, J. Danzberger, and J. Smoliner, “Phase and amplitude sensitive scanning microwave microscopy/spectroscopy on metal-oxide-semiconductor systems” J. Appl. Phys. vol. 111, 074313, 2012.

[11] A. Imtiaz, T.M. Wallis, S.-H. Lim, H. Tanbakuchi, H.-P. Huber, A. Hornung, P. Hinterdorfer, J. Smoliner, F. Kienberger, and P. Kabos, “Frequency-selective contrast on variably doped p-type silicon with a scanning microwave microscope” J. Appl. Phys. vol. 111, 093727, 2012.

[12] G. Gramse, M. Kasper, L. Fumagalli, G. Gomila, P. Hinterdorfer and F. Kienberger, “Calibrated complex impendance and permittivity measurements with scanning microwave microscopy” Nanotechnol. vol.25, 145703, 2014.

[13] E. Brinciotti, G. Gramse, S. Hommel, T. Schweinboeck, A. Altes, M.A. Fenner, J. Smoliner, M. Kasper, G. Badino, S. S. Tuca, and F. Kienberger “Probing resistivity and doping concentration in semiconductors at the nanoscale using scanning microwave microscopy” Nanoscale vol. 7, pp. 14715 – 14722, 2015.

[14] L. Michalas, A. Lucibello, G. Badino, C.H. Joseph, E. Brinciotti, F. Kienberger, E. Proietti, and R. Marcelli “Scanning microwave microscopy for nanoscale characterization of semiconductors:De-embedding reflection conatct mode measurements” In Proceedings of 45th EuMW, European Microwave Conference, Paris, France 5-11 September 2015, Edited by IEEE-EuMA, pp. 159-162.,

[15] L. Michalas, F. Wang, C. Brillard, N. Chevalier, J.M. Hartmann, R. Marcelli, amd D. Theron “Modeling and de-embedding the interferometric scanning microwave microscopy by means of dopant profile calibration” Appl. Phys. Lett. vol. 107, 223102, 2015.

[16] A. Tselev, N.V. Lavrik, I. Vlassiouk, D. P. Briggs, M. Rutgers, R. Proksch, and S.V. Kalinin,“Near-field microwave scanning probe imaging of conductivity inhomogeneities in CVD graphene” Nanotechnol. vol. 23, 385706, 2012.

[17] Y.J. Oh, H.P. Huber, M. Hochleitner, M. Duman, B. Bozna, M. Kastner, F. Kienberger and P. Hinterdorfer, “High-frequency electromagnetic dynamics properties of THP1 cell using scanning microwave microscopy” Ultramicroscopy vol. 111, pp.1625-1629, 2011.

[18] G. Hamaide, F. Alibert, H. Hovel, and S. Cristoloveanu, “Impact of free surface passivation on silicon on insulator buried interface properties by pseudotransistor characterization” J. Appl. Phys. vol. 101, 114513, 2007.

[19] See http://Rmnano.com for information about SMM tips

[20] A. Imtiaz, T.M. Wallis, J.C. Weber, K. J. Coacley, M. D. Brubaker, P.T. Blanchard, K.A. Bertness, N.A. Sanford, and P. Kabos “Imaging the p-n junction in gallium nitride nanowire with a scanning microwave microscope” Appl. Phys. Lett. vol. 104, 263107, 2014.

# *Influence of the Ge amount at source on transistor efficiency of vertical gate all around TFET for different conduction regimes*

C. C. M. Bordallo, V. B. Sivieri, J. A. Martino and P. G. D. Agopian
LSI /PSI/USP, University of Sao Paulo
Sao Paulo, Brazil
caiobordallo@gmail.com

R. Rooyackers, A. Vandooren, E. Simoen, A. Thean and C. Claeys*
Imec, Leuven, Belgium
*also KU Leuven, Belgium

***Abstract*— In this work, the influence of the Ge amount at source on transistor efficiency and intrinsic voltage gain of vertical gate all around TFET is experimentally evaluated, comparing three different source compositions. The reference transistor has a source of 100% of Si, and the studied devices have 27% and 100% of Ge at the source. The increase of the Ge amount at source enhances the tunneling current, without degrading the off state current, improving the subthreshold region characteristics and reducing the onset voltage. At the same current level, devices with higher percentage of Ge present a higher Early voltage and improved efficiency, resulting in an increase of the intrinsic voltage gain. Comparing at the same gate bias, Ge source devices are also better due to their higher drain current value. At weak conduction regime, all devices show better analog characteristics due to their higher efficiency values. Considering the better performance of Ge source devices, two different $HfO_2$ thicknesses were also analyzed (3 nm and 2 nm). The device with thinner $HfO_2$ layer presents better transistor efficiency at both conduction regimes due to its better electrostatic coupling. However, when using high values of gate voltage, this device has a strong degradation on the intrinsic voltage gain.**

***Keywords—TFET, Analog Parameters, SiGe Source, Vertical Nanowire.***

## I. INTRODUCTION

Tunnel field effect transistors (TFETs) are new devices developed to overcome the conventional MOSFETs switching capability. The main conduction mechanism of TFETs is the band-to-band tunneling (BTBT) [1], which allows these devices to reach values of subthreshold swing (SS) lower than the conventional MOSFET theoretical limit (60 mV/dec) [2–4].

However, using only silicon, TFET devices present low on-state current ($I_{ON}$) values. Focusing on the improvement of $I_{ON}$, new source compositions have been studied, aiming the reduction of the material bandgap, decreasing the tunneling path and consequently improving BTBT [5- 8].

Although TFETs were developed to improve the switching performance, the analog characteristics analysis of TFETs have been recently studied and have shown promising results [9-13].

In this work, the impact of the conduction mechanism on the transistor efficiency and on the intrinsic voltage gain is evaluated for vertical gate all around TFET devices, with Si, $Si_{0.73}Ge_{0.27}$ and Ge source compositions. The studied parameters were analyzed in two conditions: weak and strong conductions.

## II. DEVICE CHARACTERISTICS

The analyzed devices are N-type vertical gate all around TFETs fabricated in imec/Belgium. These devices were measured using an Agilent B1500 Semiconductor Characterization System at the University of Sao Paulo.

The representation of the used devices structure is presented in figure 1.

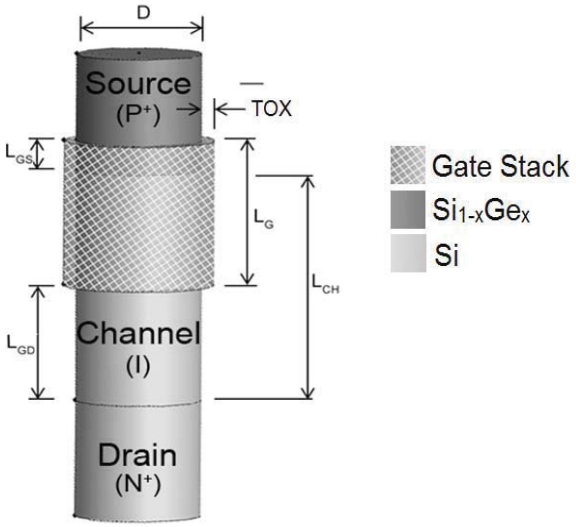



**Fig. 1 –** Representation of the studied devices structure.

These devices use a top down vertical process flow [14]. The devices have a physical gate length ($L_G$) of 150 nm, a total channel length ($L_{CH}$) of 220 nm, a gate/drain underlap ($L_{GD}$) of 100 nm, a gate/source overlap ($L_{GS}$) of 30 nm, a diameter of 140nm and have 2400 nanowires in parallel. Three different

source compositions were studied, one of $Si_{0.73}Ge_{0.27}$, one of pure Ge and the other of pure Si. The gate stack is composed by a dielectric of 3nm $HfO_2$ on top of 1nm interfacial $SiO_2$ and covered by a TiN and amorphous silicon layer. For the Ge source device, another device with 2nm of $HfO_2$ was measured. The drain region is doped with $2x10^{19}$ As/cm$^3$, the source is doped with $1x10^{20}$ B/cm$^3$ and the channel is doped with $1x10^{16}$ As/cm$^3$. More details regarding these structures can be found in [7].

## III. Analizes and Results

The experimental drain current ($I_{DS}$) as a function of the gate voltage ($V_{GS}$) for Si, $Si_{0.73}Ge_{0.27}$ and Ge sources TFET devices is presented on figure 2. From this figure it is possible to observe that the Ge device has the highest $I_{ON}$, due to its smaller bandgap (0.66 eV). The reduction of the bandgap decreases the tunneling path and increases the overlap between bands at source/channel junction, resulting in a higher BTBT current. This reduction of the bandgap also causes a decrease on the BTBT onset voltage, as can be observed for the Ge devices.

Although the Ge source devices present higher $I_{ON}$ current, their off state current ($I_{OFF}$) is slightly higher than the Si device, resulting also in an improvement of the $I_{ON}/I_{OFF}$ ratio.

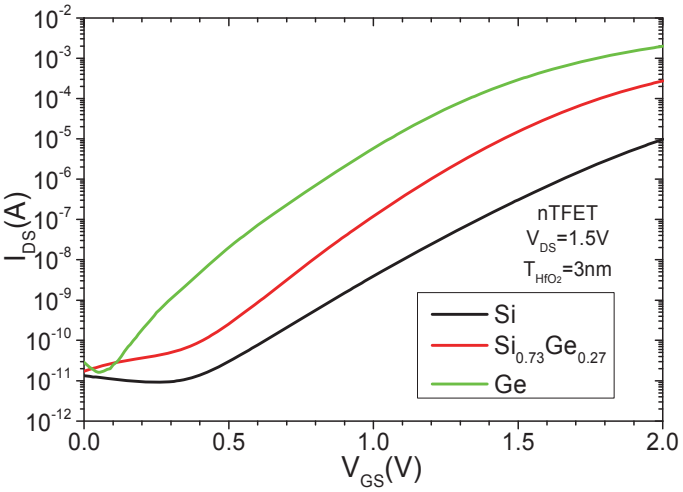



**Fig. 2 –** Experimental $I_{DS}$ vs $V_{GS}$ for TFETs with different source composition.

The transistor efficiency ($gm/I_{DS}$) is a very important figure of merit for analog application. From $gm/I_{DS}$ as a function of normalized $I_{DS}$ (figure 3), it is possible to study the efficiency behavior from weak to strong regime. From figure 3, it is noticeable that when the percentage amount of Ge in the source increases, the devices efficiency also increases for all $I_{DS}$ range due to the higher BTBT dominance that results in a better subthreshold swing (weak regime) and higher gm (strong regime).

Figure 4 shows the extracted values of $gm/I_{DS}$ for a fixed current at weak conduction, at strong conduction and also with the same gate bias of 1.9V, for all the different sources devices.

In weak conduction, as the reduction of the bandgap increases the $I_{ON}/I_{OFF}$ ratio, it improves the subthreshold region behavior, resulting in an improvement of the $gm/I_{DS}$ due to its dependence with subthreshold swing. In strong conduction, as the comparison is made using the same $I_{DS}$, and the transconductance is as higher as the percentage of Ge, the $gm/I_{DS}$ is also higher for the Ge devices.

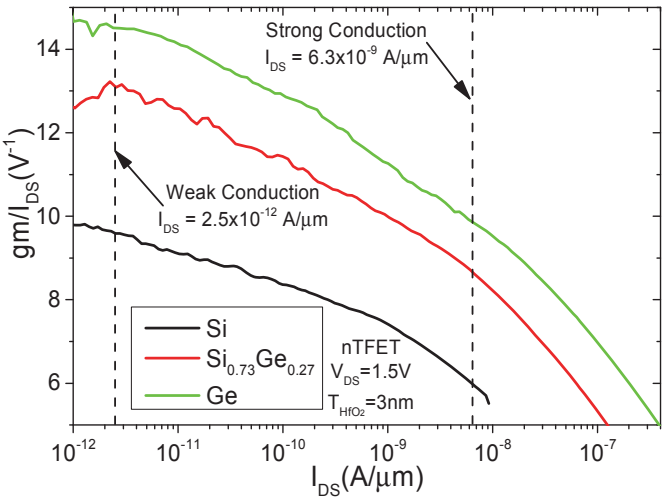



**Fig. 3 –** Experimental $gm/I_{DS}$ vs $I_{DS}$ for TFETs with different source.

When comparing with a fixed bias of $V_{GS}$=1.9 V, an opposite behavior can be noticed: the increase of the Ge percentage at the source degrades the $gm/I_{DS}$. This behavior can be explained by the high $I_{DS}$ values for Ge source devices, which becomes more pronounced than the gm improvement.

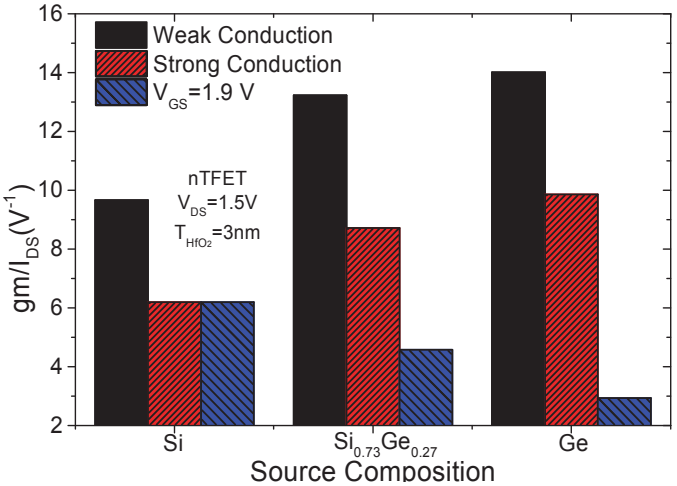



**Fig. 4 –** Values of $gm/I_{DS}$ for different conduction regime and source composition.

Figure 5 presents the Early voltage ($V_{EA}$) values for the different sources compositions. Focusing on the comparison that considers the same drain current level, in the weak and strong conduction, the Ge devices are less dominated by the BTBT mechanism [15], being less influenced by the drain voltage ($V_{DS}$), improving $V_{EA}$.

When the gate is biased at 1.9V, there is a competition between two factors: the conduction mechanism and the current level. As the BTBT onset voltage is lower for higher percentages of Ge at the source [10, 16], the Ge source devices have more BTBT influence, increasing the influence of $V_{DS}$, which tends to degrade $V_{EA}$. However, the increase of the current level in Ge source devices, caused by the bandgap reduction, tends to increase $V_{EA}$. Since the latter is more pronounced than the former, it results in a considerable improvement of the $V_{EA}$.

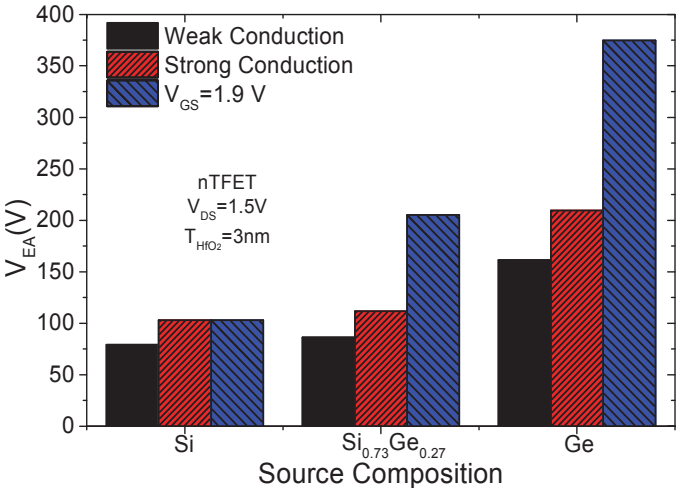



**Fig. 5** – Values of $V_{EA}$ for different conduction regime and source composition.

The intrinsic voltage gain analysis (Fig. 6) was also performed comparing the same $V_{GS}$ (1.9 V), and the same current level in weak and strong conduction. Among all the comparisons, the best results were obtained for the weak conduction. Although the trap assisted tunneling (TAT) has a strong influence in this regime and the obtained Early voltage is smaller than the one obtained for strong conduction, in weak conduction the $gm/I_{DS}$ values become the predominant factor on the intrinsic voltage gain.

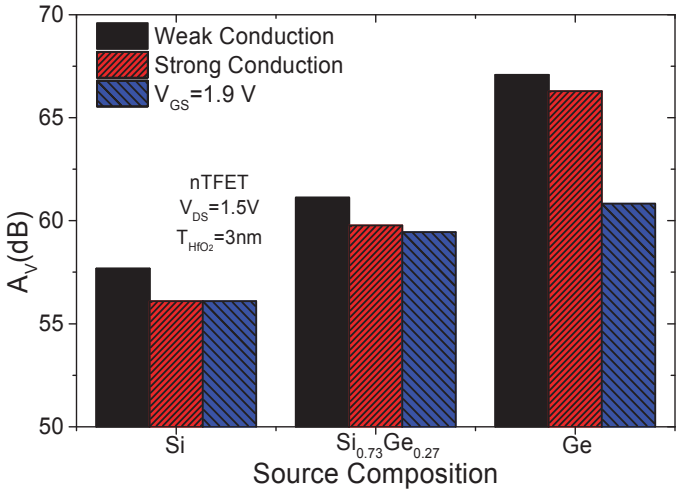



**Fig. 6** – Values of $A_V$ for different conduction regime and source composition.

However, independent on the proposed comparison, the Ge source TFET always presents a better $A_V$ behavior. In weak conduction due to better subthreshold swing (better $gm/I_{DS}$), in strong inversion due to the better gm (better $gm/I_{DS}$) and for $V_{GS}$=1.9V due to higher $V_{EA}$.

As the Ge source device showed to be the best among the analyzed devices, the comparison between the Ge source devices with 3nm of $HfO_2$ and 2nm of $HfO_2$ in the gate stack was also performed. Figure 7 presents the $I_{DS}$ as a function of the $V_{GS}$ for these devices. In this figure it is possible to observe that the 2 nm $HFO_2$ device although has more $I_{OFF}$ due to the increase of the gate current, it has better electric coupling, showing to have an improved subthreshold swing and $I_{ON}$. This improvement can also be observed in the $gm/I_{DS}$ as a function of the normalized $I_{DS}$ (Figure 8), where the 2 nm $HfO_2$ device curve has higher values of $gm/I_{DS}$ for all $I_{DS}$ range, even when comparing at same external bias ($V_{GS}$=1.9V).

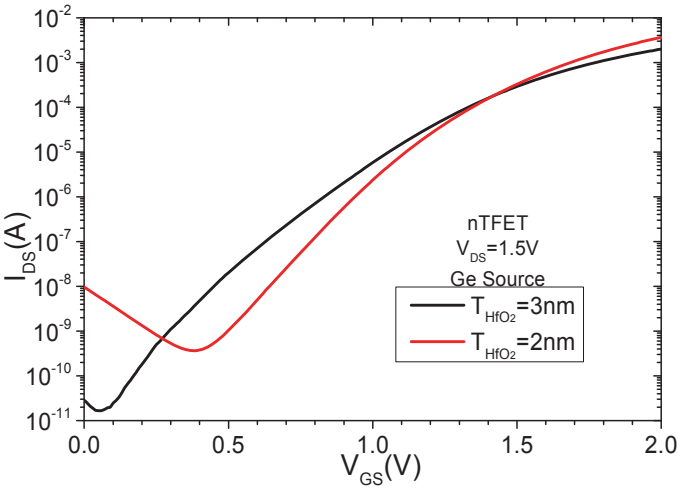



**Fig. 7** – Experimental $I_{DS}$ vs $V_{GS}$ for Ge source TFETs with different $HfO_2$ thickness.

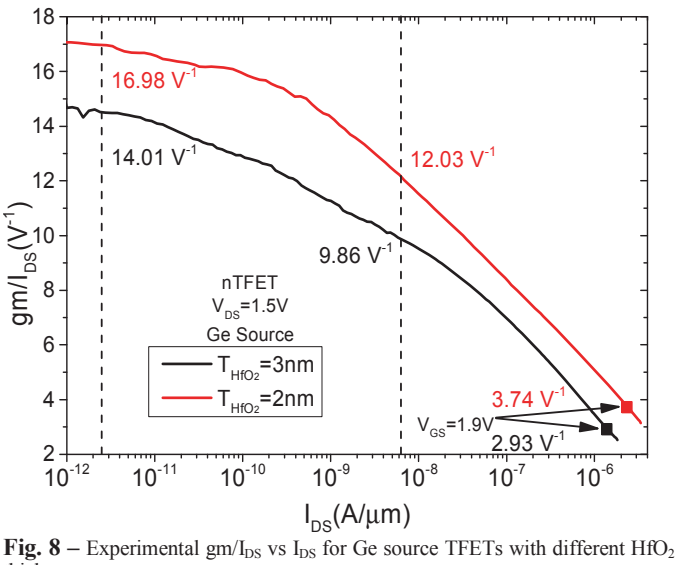



**Fig. 8** – Experimental $gm/I_{DS}$ vs $I_{DS}$ for Ge source TFETs with different $HfO_2$ thickness.

Table 1 presents the values of $V_{EA}$ and $A_V$ for both devices. The 2nm $HfO_2$ devices have higher $V_{EA}$ values for both weak and strong regimes, due to its higher electric coupling. However, for $V_{GS}$=1.9 V, the 2nm $HfO_2$ device have a degradation of $V_{EA}$, caused by the intense influence of BTBT mechanism.

**Table. 1** – Values of $V_{EA}$ and $A_V$ for the Ge source devices.

| $T_{HfO2}$ | $V_{EA}$ (V) | | | $A_V$ (dB) | | |
|---|---|---|---|---|---|---|
| | Weak | Strong | $V_{GS}$=1.9V | Weak | Strong | $V_{GS}$=1.9V |
| 3 nm | 161 | 209 | 375 | 67.1 | 66.3 | 60.8 |
| 2 nm | 388 | 504 | 116 | 76.4 | 75.6 | 52.7 |

Considering the $A_V$, in the weak and strong regimes the 2 nm $HfO_2$ device has higher $A_V$ because it has an improvement in the $gm/I_{DS}$ and in the $V_{EA}$, however, with $V_{GS}$=1.9 V it is degraded due to its $V_{EA}$ and $gm/I_{DS}$ degradation.

## IV. Conclusions

In this work a comparative study of the Ge amount at the source of gate all around TFET devices was performed, for three different conditions: fixed current at weak and strong conduction regimes and also for the same gate voltage (1.9 V). The increase of Ge amount at source reduces the bandgap, and consequently the tunneling path, that in turns increases the overlap between bands at source/channel junction and the BTBT current of TFETs.

For all comparisons, the devices with higher amount of Ge presented better analog characteristics than the others. Considering the conduction regime, although the Early voltage is smaller in weak conduction, the improvement of $gm/I_{DS}$ led to the best $A_V$ characteristics for all analyzed devices. It can be concluded that the Ge device in weak conduction regime is the most recommended device for analog applications, among all the studied devices.

The Ge device with the gate stack formed with 2 nm of $HfO_2$ proved itself to have even better analog characteristics than the 3 nm $HfO_2$ one, due to its better electrostatic coupling, being even better when it is working in weak conduction regime.

## Acknowledgment

The authors would like to thank CAPES, FAPESP and CNPq for the financial support. Part of the work has been performed under CNPq Brazil – FWO Flanders collaboration and was supported by the imec's Logic Device Program and its core partners.

## References

[1] W. M. Reddick, G. Amaratunga, "Silicon surface tunnel transistor," Applied Physics Letters, vol. 64, Issue 4, pp. 494-496, July 1995.

[2] M. Kim, Y. Wakabayashi, R. Nakane, M. Yokoyama, M. Takenaka, and S. Takagi, "High Ion/Ioff Ge-source ultrathin body strained-SOI Tunnel FETs," in IEEE IEDM Techn Digest, Dec. 2014, p. 331 – 334.

[3] T. Krishnamohan, D. Kim, S. Raghunathan, K. Saraswat, "Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) With Record High Drive Currents and <60mV/dec Subthreshold Slope", in IEEE IEDM Techn Digest, Dec 2008, p. 947 - 950.

[4] W. Y. Choi, B. G. Park, J. D. Lee, and T. J. K. Liu, "Tunneling Field-Effect Transistors (TFETs) with subthreshold swing (SS) less Than 60 mV/dec," IEEE Electron Device Lett., vol. 28, no. 8, pp. 743-745, August 2007.

[5] A. S. Verhulst, W. G. Vandenberghe, K. Maex, G. Groeseneken, "Boosting the on-current of a n-channel nanowire tunnel field-effect transistor by source material optimization" Journal of Applied Physics, vol. 104, Issue 6, September2008.

[6] D. Leonelli, A. Vandooren, R. Rooyackers, S. De Gendta, M. M. Heynsa, G. Groeseneken, "Drive current enhancement in p-tunnel FETs by optimization of the process conditions", Solid-State Electronics, Vol. 65–66, pp. 28-32, December 2011.

[7] A. Vandooren, D. Leonelli, R. Rooyackers, A. Hikavyy, K. Devriendt, M. Demand, R. Loo, G. Groeseneken, C. Huyghebaert, "Analysis of trap-assisted tunneling in vertical Si homo-junction and SiGe hetero-junction Tunnel-FETs", Solid-State Electronics, Vol. 83, pp. 50-55, May 2013.

[8] M. Schmidt, A. Schäfer, R. Minamisawa, D. Buca, S. Trellenkamp, J. M. Hartmann, Q. T. Zhao, and S. Mantl, "Line and point tunneling in scaled Si/SiGe heterostructure TFETs," IEEE Electron Device Lett., vol. 35, no. 7, pp, 699-701, July 2014.

[9] P. G. D. Agopian, M. D. V. Martino, S. D. dos Santos, F. S. Neves, J. A. Martino, A. Vandooren, R. Rooyackers, E. Simoen, A. Thean, and C. Claeys, "Influence of the source composition on the analog performance parameters of vertical nanowire-TFETs," IEEE Trans. Electron Devices, vol. 62, pp. 16-22, November 2014.

[10] M. D. V. Martino, F. S. Neves, P. G. D. Agopian, J. A. Martino, A. Vandooren, R. Rooyackers, E. Simoen, A. Thean, and C. Claeys, "Analog performance of vertical nanowire TFETs as a function of temperature and transport mechanism," Solid-State Electronics, - vol. 112, pp. 51-55, 2015.

[11] A. Mallik, A. Chattopadhyay, "Tunnel Field-Effect Transistors for Analog/Mixed-Signal System-on-Chip Applications" IEEE Transactions on Electron Devices, vol. 59, Issue 4, pp. 888-894, April 2012

[12] P. G. D. Agopian, S. D. dos Santos, F. S. Neves; J. A. Martino, A. Vandooren, R. Rooyackers, E. Simoen, C. Claeys, "NW-TFET analog performance for different Ge source compositions" IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), October 2013.

[13] P. G. D. Agopian; J. A. Martino, R. Rooyackers, A. Vandooren, E. Simoen, C. Claeys, "Experimental Comparison Between Trigate p-TFET and p-FinFET Analog Performance as a Function of Temperature" IEEE Transactions on Electron Devices, Vol. 60, Issue 8 , pp. 2493-2497, Julho 2013.

[14] R. Rooyackers, A. Vandooren, A. S. Verhulst, A. Walke, K. Devriendt, S. Locorotondo, M. Demand, G. Bryce, R. Loo, A. Hikavyy, T. Vandeweyer; C. Huyghebaert; N. Collaert; A. Thean, "A new complementary hetero-junction vertical Tunnel-FET integration scheme" Techn Digest, Dec 2013, p. 92 - 95.

[15] C. C. M. Bordallo, V. B. Sivieri, J. A. Martino, P. G. D. Agopian, R. Rooyackers, A. Vandooren, E. Simoen, A. Thean, and C. Claeys, "Impact of the diameter of vertical Nanowire-Tunnel FETs with Si and SiGe source composition on analog parameters," in Proc. EuroSOI-ULIS, January 2015.

[16] R. Rooyackers, A. Vandooren, A. S. Verhulst, A. M. Walke, E. Simoen, K. Devriendt, S. Lo-Corotondo, M. Demand, G. Bryce, R. Loo, A. Hikavyy, T. Vandeweyer, C. Huyghebaert, N. Collaert, and A. V. Y. Thean, "Ge-Source Vertical Tunnel FETs Using a Novel Replacement-Source Integration Scheme" IEEE Transactions on Electron Devices, Vol. 61, Issue 12 , pp. 4032-4039, December 2014.

# Analysis of TFET and FinFET Differential Pairs with Active Load from 300K to 450K

Márcio D. V. Martino[1], *Student Member, IEEE*, João A. Martino[1], *Senior Member, IEEE*, Paula G. D. Agopian[1], *Member, IEEE*

[1] LSI/PSI/USP, University of Sao Paulo, Sao Paulo, Brazil
mdvmartino@gmail.com

***Abstract* – The aim of this work is to compare differential pairs designed with TFETs or FinFETs and evaluate the impact of the working principle of each technology on differential ($A_d$) and common-mode ($A_{cm}$) voltage gains and on the susceptibility to the temperature. Circuits with TFETs present higher peak values of $A_d$ and common mode rejection rate (CMRR), but this performance is observed for a narrow input voltage range. When the temperatures raises, differential pair with TFET keeps its parameters almost unchanged, while FinFETs are clearly degraded, revealing a promising application of Tunnel-FET devices.**

***Keywords— TFET, FinFET, Differential Pair, Temperature impact.***

## I. INTRODUCTION

The continuous scale-down faced by MOSFET devices in the past few decades turned leakage currents and short-channel effects into major concerns. Considering that the supply voltage has not been reduced at the same proportion, it is clear that power dissipation becomes also a major roadblock [1, 2].

In order to overcome the subthreshold swing limit of 60mV/decade at room temperature, Tunnel Field Effect Transistors (TFETs) have been considered a promising alternative [3]. These devices are based on a gated p-i-n diode structure, in a way that band-to-band tunneling (BTBT) replaces drift-diffusion, reducing short-channel effects and subthreshold swing [4, 5].

This work studies the suitability of TFET technology in a basic circuit, namely a differential pair with active load. The results have been compared to FinFETs at room and high temperatures using numerical simulations.

## II. DEVICE CHARACTERISTICS

The devices used in this work represent the cross-section of a FinFET structure. The channel length and the distance between their 2 gate oxide interfaces are kept constant along the study, with values of 60 and 40nm respectively. The gate is self-aligned to both channel/drain and channel/source junctions.

Numerical simulations have been performed with low doped channel ($5x10^{15}$ $cm^{-3}$) and $10^{20}$ $cm^{-3}$ doped drain and source. TFET and FinFET devices are simulated with the same structure, but changing the source type. Figure 1 illustrates the case of pTFET and pFinFET.

The gate stack is composed of a midgap material with workfunction of 4.7eV and a gate oxide with thickness of 2nm.

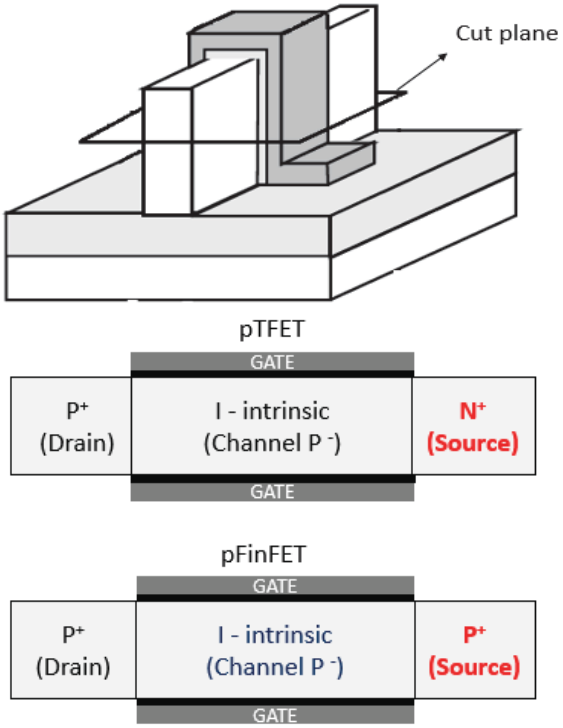



Fig. 1. P-type TFET and FinFET structure and the respective cut plane.

## III. METHODOLOGY

The circuit of the differential pair with active load is schematically represented in Figure 2. The power supply ($V_{DD}$) is 1.7V and $V_{SS}$ is -1.7V. Input voltages $v_{in1}$ and $v_{in2}$ refer to the gate of $Q_1$ and $Q_2$ transistors respectively and the output voltages $v_{out1}$ and $v_{out2}$ are their drains in the same order. The transistors currents $I_{d1}$ and $I_{d2}$ and the total I current are represented in Figure 2 as well. The circuit has been simulated with Atlas Mixed Mode.

The comparison has been performed based on parameters such as the differential voltage gain ($A_d$), the common-mode voltage gain ($A_{cm}$) and the common-mode rejection ratio (CMRR). The differential voltage gain is obtained when the differential input voltage ($v_{id}$) is defined as the difference

$v_{in1}$ - $v_{in2}$. The common-mode voltage gain is extracted when $v_{in1} = v_{in2} = v_{icm}$. Therefore, $A_d$, $A_{cm}$ and CMRR are calculated according to equations 1-3.

$$A_d = \frac{|v_{out2}|}{|v_{id}|} \quad (1)$$

$$A_{cm} = \frac{|v_{out2}|}{|v_{icm}|} \quad (2)$$

$$CMRR = \frac{|A_d|}{|A_{cm}|} \quad (3)$$

After the comparison of circuits with TFETs and FinFETs at room temperature, the same parameters are obtained for temperatures ranging from 300 to 450K.

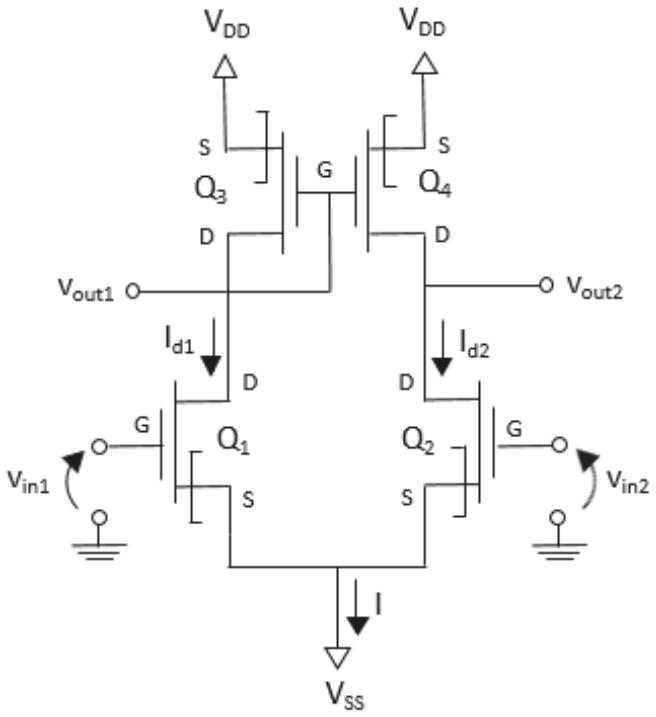



Fig. 2. Basic TFET circuit of a differential pair with active load.

## IV. Results and Analysis

The first part of this work focused on the comparison of TFET and FinFET differential pair at room temperature. Figures 3, 4 and 5 refer to the condition as a function of differential input ($v_{id}$).

Figure 3 reveals two main differences between these circuits, namely the output voltage for zero input and the non-linear curve of $v_{out2}$. For FinFETs, the mobility difference between carriers should be compensated by the bias condition for pFinFETs in the active load and nFinFETs in the differential pair. Therefore, the output voltage for $v_{id}$ = 0V is -0.55V for FinFETs and nearly zero for TFETs, since its current is basically due to BTBT, which occurs quite close to the channel/source junction and depends mainly on its bandgap.

Regarding the shape of $v_{out2}$ for TFET, it is important to notice the very high slope for low input voltages and the clear saturation for $|v_{id}| > 0.2$. The susceptibility to the input voltage leads to a higher values of differential gain, which may be justified by considering that this parameter is directly proportional to the transistor transconductance ($g_m$) and output resistance ($r_0$). As previously observed in [6], even with higher $g_m$ values for FinFETs, TFETs advantage in terms of $r_0$ prevails.

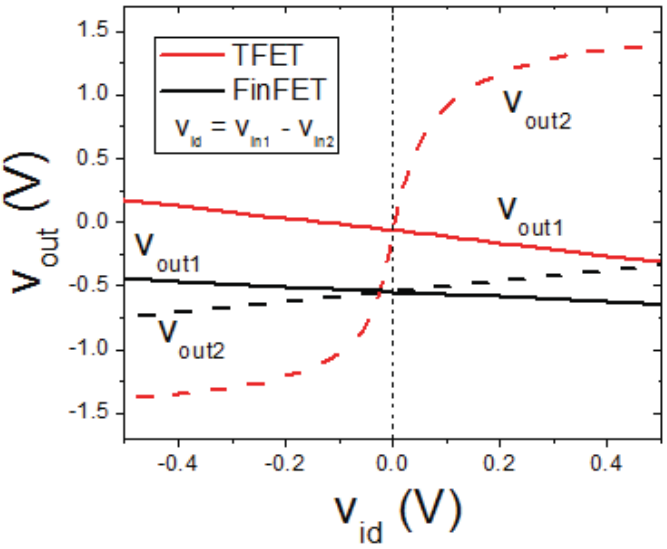



Fig. 3. Output voltages as a function of the differential input voltage.

Figure 4 illustrates this behavior in terms of drain current variation. At the same time, it shows the influence of the circuit asymmetry, due to the short circuit between $Q_3$ gate and drain, which keeps $Q_3$ in the saturation region for a wider range of input voltage than $Q_4$.

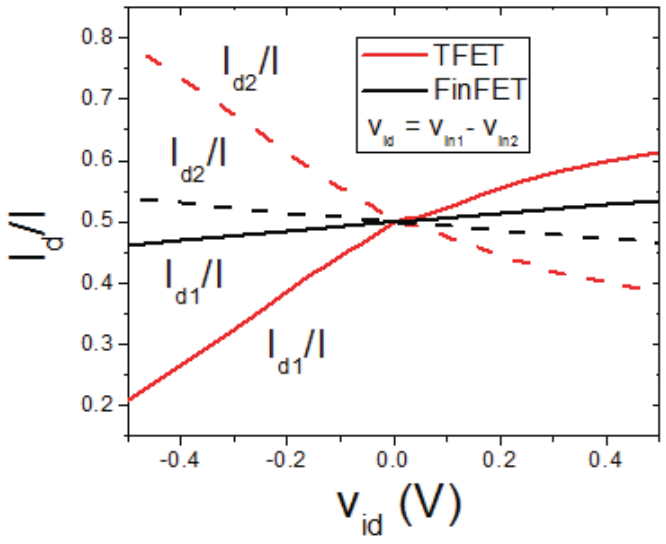



Fig. 4. $I_{d1}/I$ and $I_{d2}/I$ ratios as a function of the differential input voltage.

Figure 5 reveals the consequent differential gains for the circuits with TFETs and FinFETs. The results are normalized for a unitary gain for FinFETs at $v_{id}$ = 0V, so that it is clear that the peak value obtained for TFETs is more than 50 times higher. A similar behavior had been observed for differential pairs with passive load in [7], including highest $A_d$ and stricter linear regions for TFETs. On the other hand, without the mentioned $Q_3$ short circuit, $I_d$/I curves used to be symmetric to $v_{id}$.

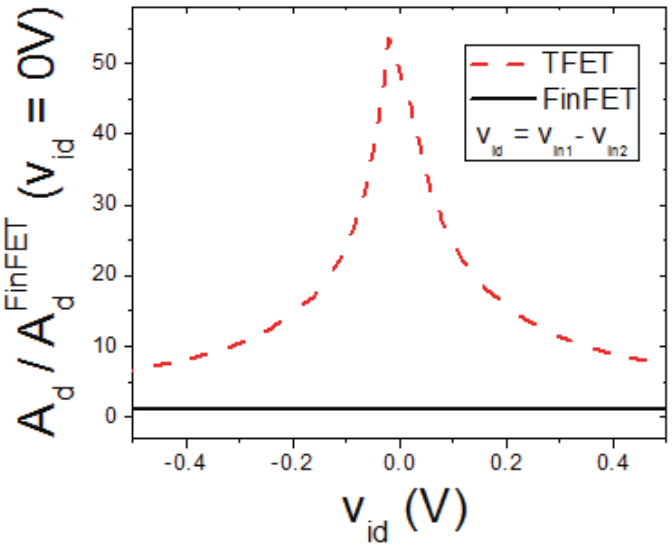



Fig. 5. Differential gain as a function of the differential input voltage.

Figure 6 exhibits the common-mode gain as a function of $v_{icm} = v_{in1} = v_{in2}$, following the same previously explained normalization criteria. In this case, the output voltages was closely linear for both circuits and the slope was relatively similar to each other. This way, there is no clear peak in any curve and the relative difference is much smaller than the one observed in Figure 5. A direct consequence may be noticed in the CMRR, which is related to the differential and common-mode gains ratio. Based on this parameter, the performance of differential pair with TFETs is more suitable than with FinFETs, since the former presented up to 22 times bigger CMRR than the latter.

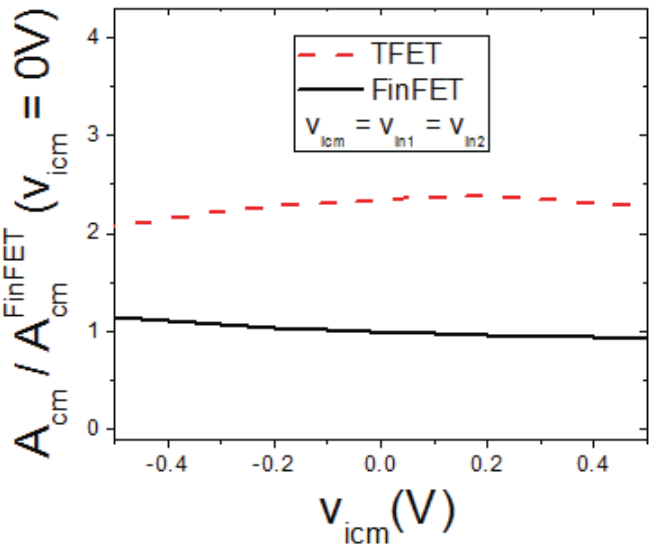



Fig. 6. Common-mode gain as a function of the input voltage.

In the second part of this work, these circuits have been analyzed in terms of susceptibility to the temperature. Once more, $A_d$, $A_{cm}$ and CMRR have been selected as relevant parameters and their relative variation for temperatures up to 450K have been plotted in Figure 7, 8 and 9 respectively.

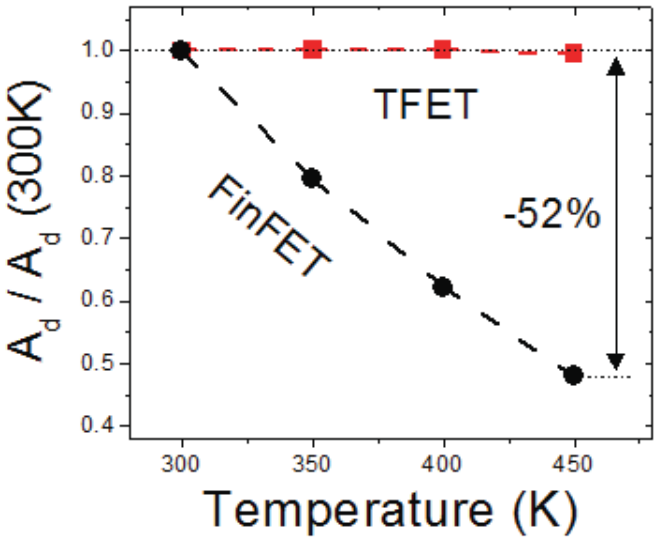



Fig. 7. Differential gain for temperatures from 300 to 450K.

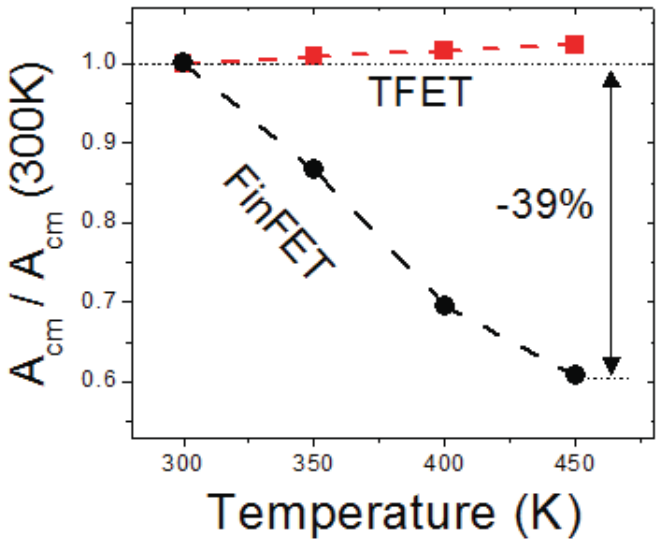



Fig. 8. Common-mode gain for temperatures from 300 to 450K.

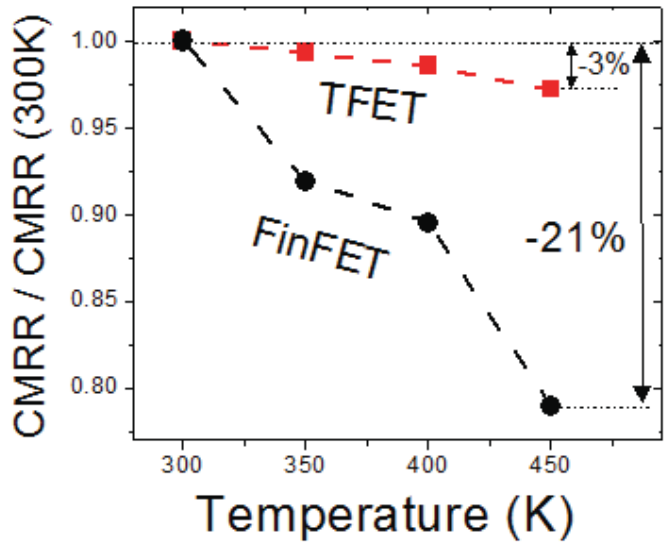



Fig. 9. Common-mode rejection ratio for temperatures from 300 to 450K.

Regarding the differential gain, values for FinFET clearly decreased by more than 50%, which may be explained by the mobility degradation for higher temperatures. Meanwhile, TFET was nearly constant, since the bandgap narrowing is closely compensated by the output conductance ($g_D$) increase. In terms of common-mode gain, TFET presents a slight increase, while FinFET reduction is relevant, but not as much as the one observed for $A_d$. As a consequence, CMRR for FinFETs reduces more than 20% and for TFETs decreases around 3%. Remembering that at room temperature the circuit with TFETs had already presented better CMRR values for low input voltages, it should be highlighted that this difference gets even more relevant as the temperatures goes up to 450K.

## V. Conclusion

This paper analyzed the suitability of differential pairs with active load designed with TFET or FinFET devices. A quantitative comparison has been performed based on the differential gain, the common-mode gain and the common-mode rejection ratio.

In the differential condition, TFETs presented a high susceptibility to the input voltage, leading to a more than 50 times higher value of $A_d$. On the other hand, there was a saturation for $|v_{id}| > 0.2V$, while FinFETs presented a linear behavior for the whole input range. The common-mode gain difference was much less significant, in a way that the CMRR was more than 20 times bigger for the circuit with TFETs.

For higher temperatures, differential pairs with FinFETs have been clearly affected by the mobility degradation, leading to a decrease in the 3 studied parameters. TFETs presented a less susceptible behavior, due to the compensation of bandgap narrowing and $g_D$ increment. CMRR decreased 21% for FinFETs, while there was a slight increase for TFETs.

To conclude, it was observed that the differential pair with TFETs presented better global results for low input voltages, but had a stricter range to work in the linear region.

## References

[1] W. M. Reddick and G. A. J. Amaratunga, "1-Silicon surface tunnel transistor", *Appl. Phys. Lett.s*, vol. 67, 1995, pp.494 -496.

[2] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, "Tunneling Field-Effect Transistors (TFETs) with Subthreshold Swing (SS) less than 60 mV/dec", *IEEE Electron Device Lett.*, vol. 28, no. 8, 2007, pp.743 -745.

[3] T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat, "Double-gate strained-Ge heterostructure Tunneling FET (TFET) with record high drive currents and <60mV/dec subthreshold slope", *IEEE International-Electron Devices Meeting* - IEDM 2008, 2008 , pp. 1- 3.

[4] A. Vandooren, D. Leonelli, R. Rooyackers, A. Hikavyy, K. Devriendt, M. Demand, R. Loo, G. Groeseneken and C. Huyghebaert, "Analysis of trap-assisted tunneling in vertical Si homo-junction and SiGe hetero-junction Tunnel-FETs", *Solid-State Electron.*, vol. 83, 2013, pp. 50–55.

[5] P. G. D. Agopian, J. A. Martino, R. Rooyackers, A. Vandooren, E. Simoen and C. Claeys, "Experimental comparison between trigate p-TFET and p-FinFET analog performance as a function of temperature," *IEEE Trans. Electron Devices*, vol. 60, no. 8, 2013, pp. 2493-2497.

[6] M. D. V. Martino, F. Neves, P. G. D. Agopian, J. A. Martino, A. Vandooren, R. Rooyackers, E. Simoen, A. Thean and C. Claeys, "Transport mechanism influence on Vertical Nanowire-TFET analog performance as a function of temperature", *Proceedings of 10th Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits,* vol. 1, 2014, pp. 1-2.

[7] M. D. V. Martino, J. A. Martino and P. G. D. Agopian, "Performance Comparison Between TFET and FinFET Differential Pair", *30th Symposium on Microelectronics Technology and Devices (SBMicro),* 2015, pp. 1-4.

# Numerical Simulation of Gunn Oscillation in AlGaAs/InGaAs High-Electron Mobility Transistor

Sung-Min Hong* and Jae-Hyung Jang
School of Information and Communications
Gwangju Institute of Science and Technology
Gwangju, Republic of Korea
* E-mail address: smhong@gist.ac.kr

***Abstract*—The Gunn oscillation in an AlGaAs/InGaAs high-electron mobility transistor is numerically simulated. Using the commercial drift-diffusion simulator with a mobility model considering the negative differential mobility effect, the autonomous on-set of the Gunn oscillation is directly observed. The Gunn oscillation can be observed only for a certain range of bias voltages. The electron density clearly shows that the recessed region between the gate and drain terminals plays an important role. The oscillation frequency and amplitude are shown as functions of the bias voltages.**

***Keywords—Gunn oscillation; high-electron mobility transistor; terahertz; simulation***

## I. INTRODUCTION

Since the electromagnetic waves in the frequency range between 0.1 terahertz (THz) to 10 THz have potential applications in various areas, it has gained great interest. In order to expedite wide spread deployment of THz technology, the development of more efficient THz devices are mandatory. [1] Especially, the development of efficient THz emitting devices is required.

Compared to other photoconductive antenna-based THz emitting devices [2], a transistor-type THz emitting device can reduce the form factor significantly, since it does not require the external laser source. Transistor-based THz emitting devices can be operable in the room temperature, in contrast to the quantum cascade laser [3]. The possibility of integration into a chip is also a big advantage. In this work, the high-electron mobility transistor (HEMT) is considered as a possible THz emitting device.

In the HEMT, two different mechanisms for generating the THz oscillation have been proposed. [4] The first one is the plasma instability in the HEMT channel. In the gated HEMT channel, there are plasma modes, whose dispersion relations are linear. However, due to the presence of the scattering, we need additional gain mechanisms for the plasma modes to support a stable oscillation. In [5], it is predicted that the unbalanced electrical boundary conditions together with a dc current flow can provide a gain mechanism for the plasma modes in the HEMT channel. There have been considerable efforts in the modeling and simulation of THz oscillation due to plasma instability. [6-10] With a reasonable set of device parameters, it is commonly believed that the plasma instability in the HEMT results in an oscillation well above 1 THz.

Another possible mechanism to generate a high-frequency oscillation is the Gunn oscillation. In the high electric field regime, due to the intervalley scattering, the electron effective mass is increased when the electric field is increased. As a result, the differential mobility becomes negative. This negative differential mobility (NDM) introduces the formation of a Gunn domain. Although the exact oscillation frequency depends on the specific device condition, it is expected that the oscillation frequency is in the sub-THz range, which is considerably lower than that of the plasma instability.

There have been some efforts to simulate the Gunn oscillation in transistors. [4, 11, 12] In [4], experimentally measured emission spectra are attributed to the Gunn oscillation. The 50 GHz drain current oscillation in AlGaAs/InGaAs HEMTs are shown by the Monte Carlo simulation in [11]. Recently, the results of Monte Carlo simulation of GaAs MOSFETs are reported in [12]. It is shown that the simulated transistor can generate a high frequency oscillation up to 325 GHz with the parameter optimization.

In this work, we present the simulation results of the Gunn oscillation in an AlGaAs/InGaAs HEMT. The structure of this extended abstract is as follows: The simulated device structure and the simulation methodology are introduced in Section II. The simulation results are shown in Section III. The oscillation frequency and amplitude are shown as functions of the bias voltages. Finally, the conclusion is made in Section IV.

## II. DEVICE STRUCTURE AND SIMULATION METHODOLOGY

The $Al_{0.25}Ga_{0.75}As/In_{0.25}Ga_{0.75}As$ HEMT structure is considered. Basically, the device-under-simulation is designed to have realistic parameters in order to enable future comparison with the measured results. The schematic of the simulated device is shown in Fig. 1. The thickness of the InGaAs channel layer is 10 nm. A delta-doping layer whose sheet density is $10^{[1]}$ $cm^{-2}$ is introduced to the AlGaAs barrier. The thickness of the barrier layer is 20 nm. The channel length is 150 nm and the length of each recessed region is 500 nm. The source and drain regions are heavily doped with $10^{20}$ $cm^{-3}$. The total channel width is 120 μm. A 0.8 μm–thick buffer layer is modeled as a perfect insulator for simplicity.

This work is supported by the Samsung Research Funding Center of Samsung Electronics under Grant SRFC-IT1401-08.

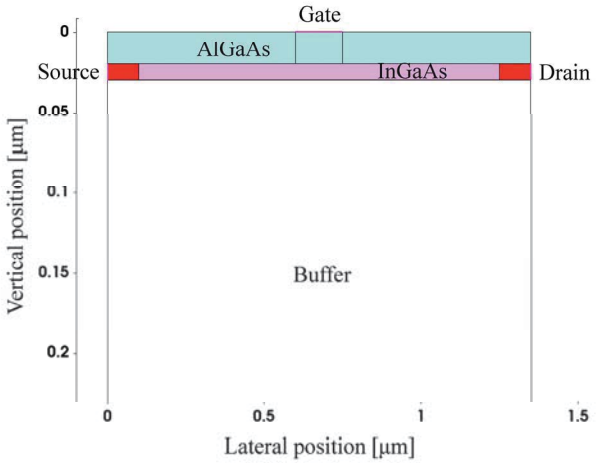



Fig. 1. Schematic of the simulated AlGaAs/InGaAs HEMT structure. The channel length is 150 nm and the length of each recessed region is 500 nm. The thickness of the buffer layer is 0.8 μm.

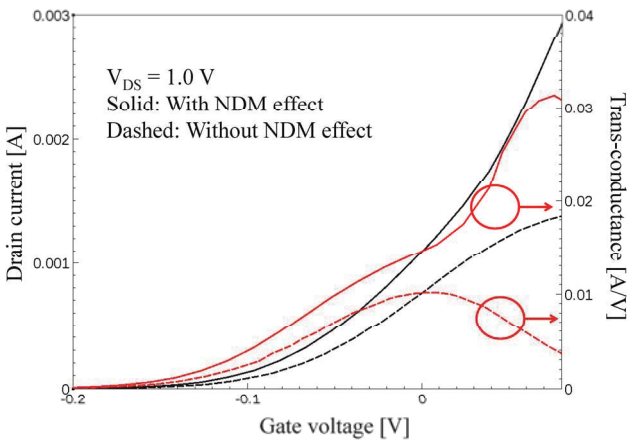



Fig. 2. Simulated dc Id-Vg relation at the drain-to-source bias voltage of 1.0 V. The trans-conductance is also shown. Solid lines are obtained with a mobility model considering the NDM effect. For dashed lines, the NDM effect is neglected in the velocity saturation model.

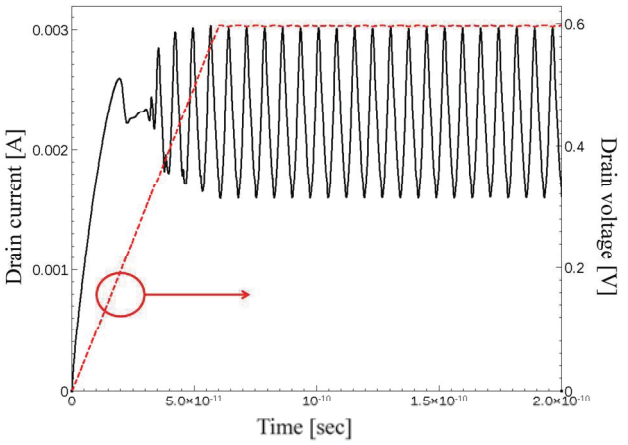



Fig. 3. Transient behavior of the drain terminal current. The gate voltage is 0.06 V and the supply voltage connected to the drain terminal is ramped up to 0.6 V with a ramping rate of 10 V nsec$^{-1}$.

A commercial device simulator [13] has been employed to solve the drift-diffusion equations. The mole-fraction dependent quantities are properly obtained by the interpolation scheme implemented in the simulator. The mobility model with the NDM effect [14] is considered for the electron mobility in the channel InGaAs layer.

It is revealed that selection of the driving force of the mobility model has a significant impact on the simulation results. The electric field parallel to the electron current is used as the driving force throughout this work. Other simulator options for the driving force, such as the absolute electric field or the gradient of the quasi-Fermi potential, do not give proper results. The hydrodynamic model suffers from some convergence problems. Since the Gunn oscillation without the impact ionization is of our primary interest in this study, the electron-hole pair generation due to the impact ionization is neglected. Moreover, the quantum confinement effect is not included in the simulation model.

It is our aim to calculate the maximum output capability of the simulated HEMT at an oscillation frequency, which is not affected by an external resonator. For this purpose, a transient simulation has been performed. A similar approach can be found in [15]. The supply voltage, which is connected to the drain terminal through a resistor of 1 Ω, is rapidly ramped up to the given target value. The typical value of the ramping rate is 10 V nsec$^{-1}$. Once after the target value is achieved, the supply voltage is kept for a sufficiently long time to yield a stable oscillatory waveform. Such a numerical experiment is repeated for various bias points. The oscillation frequency and amplitude are measured.

Note that the conventional device simulators typically adopt the implicit time differentiation scheme. In the case of the implicit scheme, the numerical dissipation due to a coarse time step reduces the instability. In order to prevent unwanted damping by the numerical dissipation, the maximum allowed time step is limited to 0.1 psec, which is sufficiently short.

## III. Simulation Results

Fig. 2 shows the dc drain current and trans-conductance as functions of the gate voltage. The drain-to-source bias voltage is 1.0 V. The NDM effect in the velocity saturation model yields large difference in the trans-conductance. It is noted that convergence problems have been observed with the NDM model for higher gate voltages.

A typical transient behavior of the drain terminal current is shown in Fig. 3. The gate voltage is 0.06 V. The ramping speed of the supply voltage is 10 V nsec$^{-1}$. During the ramping period, the oscillation of the drain current starts. Even after the ramping period is finished at 60 psec in this example, a stable oscillation can be clearly observed.

ISBN 978-1-4673-8608-1  IEEE Catalog number CFP1649D-USB

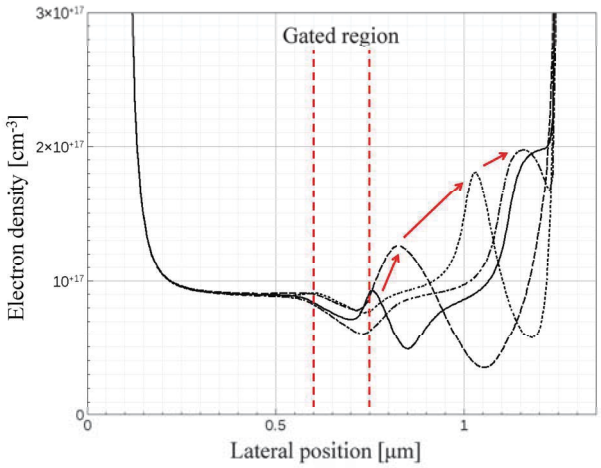



Fig. 4. Snap shot of the electron density in the InGaAs channel at various time instances with a 2 psec step. The values at the middle of the channel layer are taken. The gate voltage is 0.06 V and the supply voltage in the drain side is 0.6 V.

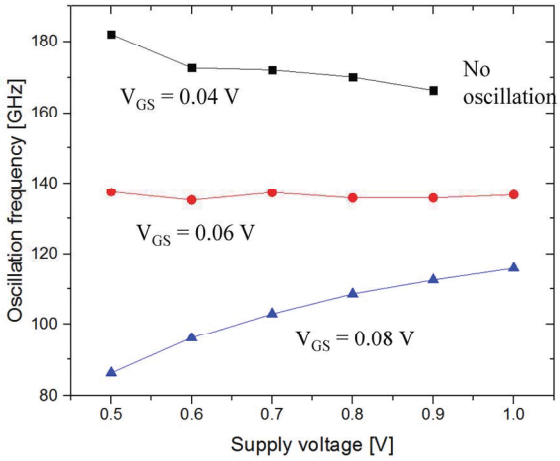



Fig. 5. Oscillation frequency as a function of the supply voltage. Three cases of the gate voltage (0.04 V, 0.06 V, and 0.08 V) are considered. For other gate voltages outside this range (such as 0.0 V or 0.1 V), no oscillation is observed.

Once after a stable oscillation is achieved, the internal quantities are inspected. The electron density is shown at various time instances in Fig. 4. The values at the middle of the channel layer (25 nm in the device coordinate) are taken. It is clear that the oscillation takes place in the recessed region between the gate and drain terminals. The overall travel length for the Gunn domain is mainly determined by the recess region, which is much longer than the gated region. On the other hand, the gated region acts as a launcher of the Gunn domain.

Note that the role of the gate-to-drain recess region is very different from the above observation in the case of the plasma instability. In this case, the overall travel length for the plasma wave is largely determined by the gated region while the gate-to-drain recess region contributes to the drain impedance.

In Fig. 5, the oscillation frequency is shown as a function of the supply voltage. The stable oscillation is observed only for a narrow range of the gate voltage. In this example, it is observed in the gate voltages between 0.04 V and 0.08 V. Interestingly, unusual behavior of the trans-conductance due to the NDM effect is observed in the same voltage range, as shown in Fig. 2.

The oscillation frequency shows a considerable dependence on the drain voltage. For example, when the gate voltage is 0.8 V, a 0.5 V difference in the drain voltage introduces about 35 % difference in the oscillation frequency. Since no external resonator is connected to the HEMT, the simulated oscillation frequency is solely determined by the device itself. Additional resonator may alter the oscillation frequency considerably.

Not only the oscillation frequency but also the oscillation amplitude exhibit dependency on the bias voltages. The peak-to-peak amplitude of the drain current fluctuation is shown in Fig. 6. When the drain resistor is 1 Ω, the peak-to-peak amplitude exhibits its maximum value of 1.44 mA at the gate voltage of 0.08 V. In this example, the amplitude is insensitive to the supply voltage, at least up to 1.0 V.

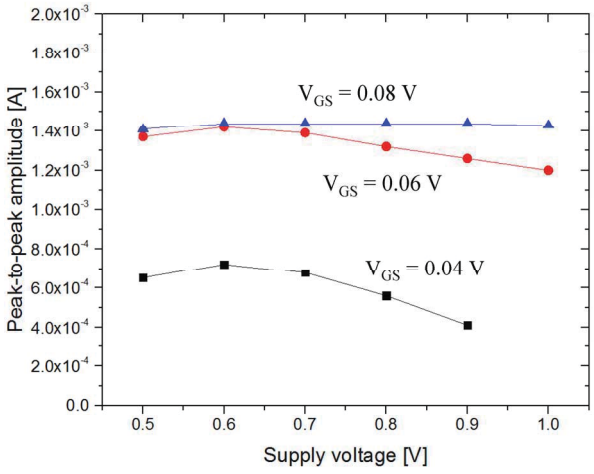



Fig. 6. Peak-to-peak amplitude as a function of the supply voltage.

As much as the emitting devices are concerned, the maximum power available from the given structure is of great interest. From the numeric values in the previous paragraph, the maximum power is roughly estimated to be a few tenths of a microwatt (μW). Impact of the drain resistor (or the external resonator) on the output power will be investigated later.

## IV. Conclusions

The Gunn oscillation in the AlGaAs/InGaAs HEMT has been simulated. It has been shown that the Gunn oscillation can be observed for a certain range of bias voltages. The electron density clearly shows that the recessed region between the gate and drain terminals plays an important role in the Gunn oscillation. The oscillation frequency and amplitude are shown as functions of the bias voltages.

## REFERENCES


[1] D. L. Woolard, E. R. Brown, M. Pepper, and M. Kemp, "Terahertz frequency sensing and imaging: A time of reckoning future applications?," *Proc. IEEE*, vol. 93, pp. 1722-1723, 2005.

[2] C. W. Berry, N. Wang, M. R. Hashemi, M. Unlu, and M. Jarrahi, "Significant performance enhancement in photoconductive terahertz optoelectronics by incorporating plasmonic contact electrodes," *Nature Commun*., vol. 4, Mar. 2013, Art. ID 1622.

[3] S. Kumar, C. W. I. Chan, Q. Hu, and J. L. Reno, "A 1.8-THz quantum cascade laser operating significantly above the temperature of $\omega/k_B$," *Nature Phys*., vol. 7, pp. 166-171, 2011.

[4] L. Varani *et al*., "Numerical modeling of terahertz electronic devices," *Journal of Computational Electronics*, vol. 5, pp. 71-77, 2006.

[5] M. Dyakonov and M. Shur, "Shallow water analogy for a ballistic field effect transistor: New mechanism of plasma wave generation by dc currnet," *Phys. Rev. Lett.*, vol. 71, pp. 2465-2468, 1993.

[6] M. V. Cheremision, M. I. Dyakonov, M. S. Shur, and G. Samsonidze, "Influence of electron scattering on current instability in field effect transistors," *Solid-State Electronics*, vol. 42, pp. 1737-1742, 1998.

[7] A. P. Dmitriev, A. S. Furman, V. Y. Kachorovskii, G. G. Samsonidze, and Ge. G. Samsonidze, "Numerical study of the current instability in a two-dimensional electron fluid," *Phys. Rev. B*, vol. 55, pp. 10319-10325, 1997.

[8] V. Ryzhii, A. Satou, W. Knap, M. S. Shur, "Plasma oscillations in high-electron-mobility transistors with recessed gate," *J. Appl. Phys*., vol. 99, pp. 084507-1-084507-5, 2006.

[9] E. Vostrikova, A. Ivanov, I. Semenikhin, and V. Ryzhii, "Electrical excitation of shock and solitionlike waves in two-dimensional electron channels," *Phys. Rev. B*., vol. 76, p. 035401, 2007.

[10] S.-M. Hong and J.-H. Jang, "Numerical simulation of plasma oscillation in two-dimensional electro gas by using a periodic steady-state solver," *IEEE Trans. Electron Devices*, vol. 62, pp. 4192-4198, 2015.

[11] G. M. Dunn, A. Phillips, and P. J. Topham, "Current instability in power HEMTs," *Semiconductor Science and Technology*, vol. 16, pp. 562-566. 2001.

[12] V. Gružinskis, E. Starikov, and P. Shiktorov, "Monte Carlo simulation of THz frequency Gunn effect in GaAs MOSFET with excess of electrons in channel at impact ionization conditions," Lithuanian Journal of Physics, vol. 54, pp. 7-10, 2014.

[13] *Sentaurus Device User Guide*, Synopsys Inc., Mountain View, CA, USA, 2014.

[14] J. J. Barnes, R. J. Lomax, and G. I. Haddad, "Finite-element simulation of GaAs MESFET's with lateral doping profiles and submicon gates," *IEEE Trans. Electron Devices*, vol. 23, pp. 1042-1048, 1976.

[15] Y. Wang, L.-A. Yang, W. Mao, S. Long, and Y. Hao, "Modulation of multidomain in AlGaN/GaN HEMT-like planar Gunn diode," *IEEE Trans. Electron Devices*, vol. 60, pp. 1600-1606, 2013.

# Metal-Graphene Contact Capacitance

A.M. Slobodyan
Dep. of General and Solid State Physics
National Technical University of Ukraine "KPI"
Kyiv, Ukraine

S.I. Tiagulskiy, Yu.V. Gomeniuk, *)A.N. Nazarov
Dep. of Functional Materials and Nanostructures (FMN)
Lashkaryov Institute of Semiconductor Physics NASU
Kyiv, Ukraine
*)nazarov@lab15.kiev.ua

***Abstract*—The paper considers a frequency dependence of Me-graphene contact capacitance. It is shown by theoretical analysis and experimental research that this frequency dependence of the capacitance can be described by a logarithmic function with a prefactor depending on the amplitude of a.c. signal. The dependence of the contact capacitance on defectiveness of the single layer graphene is discussed.**

***Keywords—graphene; contact capacitance; resistivity; method of tramsmission line***

## I. INTRODUCTION

Properties of the metal-graphene contact are crucial for efficient electrical operation of graphene devices. In spite of extensive research in this field the metal-graphene capacitance and its dependence on the frequency have not been studied up to now. Thus, in this work a theoretical analysis of the Me-graphene capacitance is carried out, and the experimental study of the frequency dependence of the capacitance of Ni-graphene contact fabricated on $SiO_2$/Si structure is performed.

## II. THEORY

The schematic view of the contact is shown in Fig.1. The contact capacitance can be determinated from the following expression [1]:

$$C = -\frac{e}{V_1}\int_0^\infty n_1(x)dx, \qquad (1)$$

where $n_1(x)$ is the nonequilibrium charge concentration induced in graphene by the alternating voltage $V_1 \sim exp(i\omega\tau)$, applied between the metal contact and the graphene layer. The $n_1(x)$ is found from the continuity equation

$$i\omega n_1 = \frac{\sigma}{e}\left(\frac{\pi\hbar^2}{2em_c}\frac{\partial^2 n_1}{\partial x^2} - \frac{\partial^2\varphi(x,0)}{\partial x^2}\right), \qquad (2)$$

where σ is the graphene conductivity. The graphene conductivity can be presented as $\sigma = e^2 D_n D$, where $D_n$ is the diffusion coefficient, and $D = 2m_c/\pi\hbar^2$ is the density of states, where $m_c = E_s/v_F^2$ is the cyclotron mass, $E_s$ is the carrier energy. The expression for the density of states takes into account that spin ($g_s$) and valley ($g_v$) degeneracy in graphene equal to 2.

The electrostatic potential $\varphi(x, z)$ can be obtained from Laplace equation with the following boundary conditions:

$$\varphi(0,z) = 0;\ \frac{\partial\varphi(x,0)}{\partial z} = \frac{2\pi e n_1(x)}{\varepsilon};\ \varphi(x\to\infty,0) = V_1,$$

where ε is the dielectric constant of the dielectric substrate. The solution of the Laplace equation is

$$\varphi(x,z) = -\frac{4e}{\varepsilon}\int_0^\infty \nu(\lambda)e^{-\lambda z}\sin(\lambda x)\frac{d\lambda}{\lambda}, \qquad (3)$$

where $\nu(\lambda) = \int_0^\infty n_1(x)\sin(\lambda x)\,dx$ is the Fourier component of $n_1(x)$. Thus, the equation for $n_1(x)$ can be obtained, which can be solved by using the Fourier sine transformation as follows:

$$n_1(x) = -\frac{4eV_1}{\pi^2\hbar^2 v_F^2}\left(E_s + \frac{eV_1}{2}\right)\int_0^\infty \frac{\lambda\sin(\lambda x)d\lambda}{\lambda^2 + \frac{2}{a}\lambda + \frac{i}{al}}. \qquad (4)$$

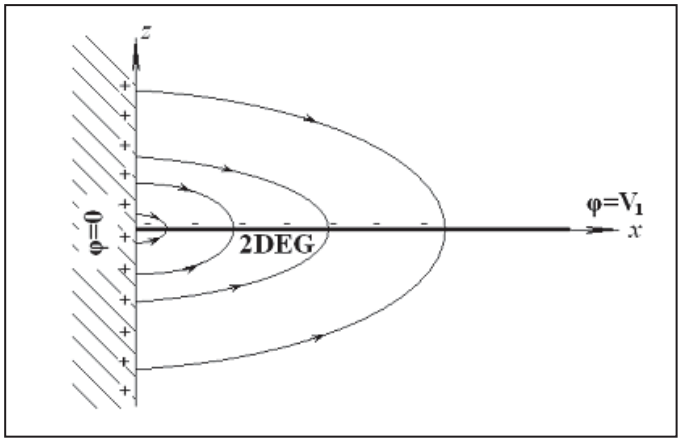



Fig. 1. Schematic view of the contact with a 2D graphene layer..

From equations (1) and (4) we get the metal-graphene contact capacitance per unit length

$$C = -\frac{e}{V_1}\int_0^\infty n_1(x)dx = \frac{\varepsilon}{\pi^2}\frac{1+\frac{eV_1}{2E_S}}{\sqrt{\left(1-\frac{ia}{l}\right)}}\ln\left(\frac{1+\sqrt{\left(1-\frac{ia}{l}\right)}}{1-\sqrt{\left(1-\frac{ia}{l}\right)}}\right), \qquad (5)$$

where $a = \varepsilon\hbar^2/2e^2m_c$ is the screening length, and $l = \pi\sigma/\omega\varepsilon$ is the relaxation length in graphene. For relatively low frequency ($a << l$) the contact capacitance has the following form

$$C \cong \frac{\varepsilon}{\pi^2}\left(1 + \frac{eV_1}{2E_S}\right)\left[\ln\left(\frac{8\pi e^2 m_c\sigma}{\varepsilon^2\hbar^2\omega}\right) - i\frac{\pi}{2}\right]. \qquad (6)$$

Thus, the real part of the contact capacitance decreases logarithmically with an increase of the measurement frequency.

In equation (6) the following simplifying conditions were taken into account: (a) the equilibrium carrier density of graphene was considered as homogeneous (band bending in the contact area ist taken into account); (b) the displacement current is not taken into account. Condition (b) imposes limitations on the both parameters of the problem: (1) $c/\sqrt{\varepsilon}\omega \gg a$ and (2) $c/\sqrt{\varepsilon}\omega \gg l$. The condition related to $a$ is always satisfied at the measurements of capacitance, whereas the second condition imposes the limitation on the graphene conductivity and can be written as $c \gg \pi\sigma/\sqrt{\varepsilon}$. In case of the graphene layer located on $SiO_2$ graphene mobility is small enough and can reach 4500 $cm^2/V\times s$ [2]; in this case the limitation (2) is met.

It should be noted that when the inverse boundary conditions for Laplace equation are applied the coefficient before square bracket in (6) reads as $(1 - eV_1/2E_s)$. Therefore the coefficient in the expression (6) for the equivalent measured capacitance is $[1 - (eV_1/2E_s)^2]$. Moreover, this coefficient depends on the alternating voltage amplitude, in contrast to the case of the contact capacitance between 3D metal and 2D electron gas [1].

## III. Experiment

Verification of the theory was performed by using of the Ni-graphene contact. The graphene layer was synthesized by CVD technique on Cu foil and transferred onto $SiO_2$/p-Si structure with the thickness of the $SiO_2$ layer about 300 nm. The quality of the graphene layer was checked by micro-Raman spectroscopy (RS, triple Raman spectrometer T-64000 Horiba Jobin-Yvon, equipped with electrically cooled CCD detector, and excitation by the 514 nm line of an Ar-Kr ion laser), and scanning Kelvin probe force microscopy techniques (SKPFM, NanoScope IIIa Dimension 3000) [3]. The micro-Raman measurements show that the graphene contains a single layer (Fig.2), and SKPFM technique demonstrates that the graphene film consists of single crystalline blocks with the sizes of about 5-10 μm (inset in Fig.2).

The Ni contacts were deposited on the graphene surface by dc magnetron sputtering to fabricate the transmission line (TL) with the same size of the contacts and different distances between them. The transmission lines were surrounded with defect areas formed by electron beam (the dose is more than $4\times10^3$ μC/cm$^2$, and energy is 3 keV) (see the inset in Fig.3). Resistance of the contacts determined from TL measurements equals to about 65 Ohm and the graphene resistivity is about 200 Ohm/□ (Fig.3). In order to change graphene defectiveness an electron beam irradiation with dose of $1\times10^2$ μC/cm$^2$ between 3rd and 4th contacts was used.

Measurements of graphene impedance vs. frequency were carried out using parallel equivalent circuits at zero bias between the two contacts. The used frequency range was $10^2$ - $10^6$ Hz, the amplitude of the input a.c. signal ranged from 30 mV to 1 V. Agilent 4284A Precision LRC Meter was used for the measurements.

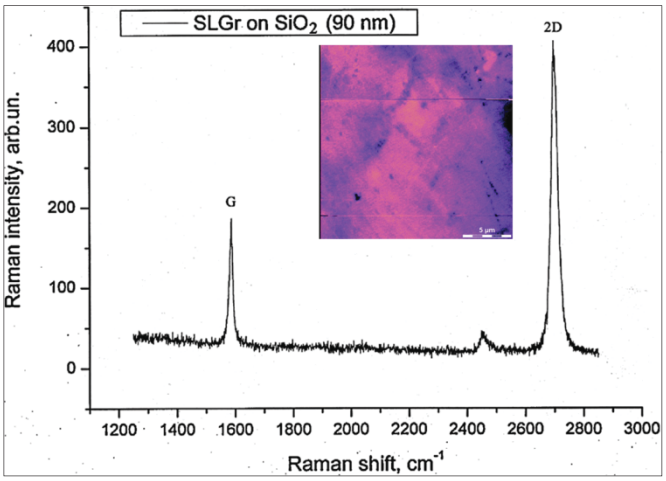



Fig. 2. Raman spectrum of the graphene film on the $SiO_2$/Si structure. Inset: Map of the graphene surface potential measured by scanning Kelvin probe force microscopy (SKPFM) technique.

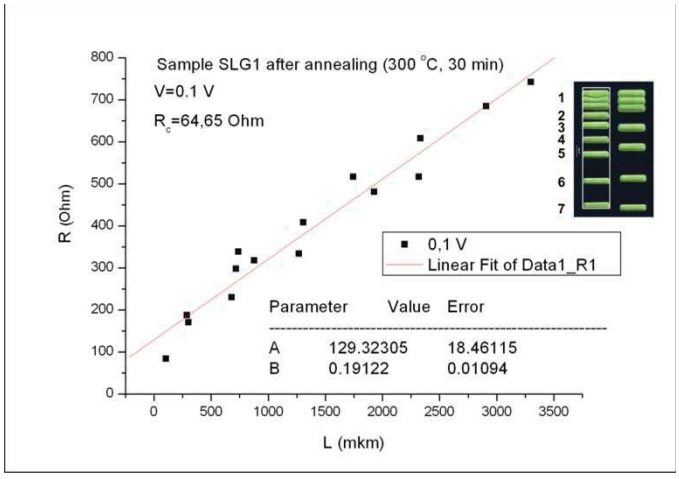



Fig. 3. Contact resistances of the Me contact-graphene and surface graphene resistivity obtained from the TL technique measurement.

## IV. Resuls and Discussion

The dependence of the capacitance on the measurement frequency at a fixed input a.c. signal can be described by the expression $C(\omega) = C_0 - C_S(V_1)\times ln(\omega+\omega_0)$ (Fig.4 (a)), and dependence of the capacitance vs. the amplitude of a.c. input signal can be written as $C_S(V_1) = A[1 - (eV_1/2E_s)^2]$ (Fig. 4 (b)).

Electron beam irradiation of the area between the contacts results in the decrease of the slope of the characteristic $C = C(ln(\omega))$ and increase of the magnitude of the measurement capacitance (Fig. 5 (a)). Additionally the "jumps" on the curve of $C = C(V_1)$ are appeared (Fig. 5 (b)). It should be noted that the electron beam treatment also leads to the decrease of low-frequency conductivity of the graphene region from $6.3\times10^{-3}$ S to $5.3\times10^{-3}$ S that has to result in an increase of the contact capacitance (see (6)). This effect we observe from experimental results (compare Fig. 4(a) and 5(a)).

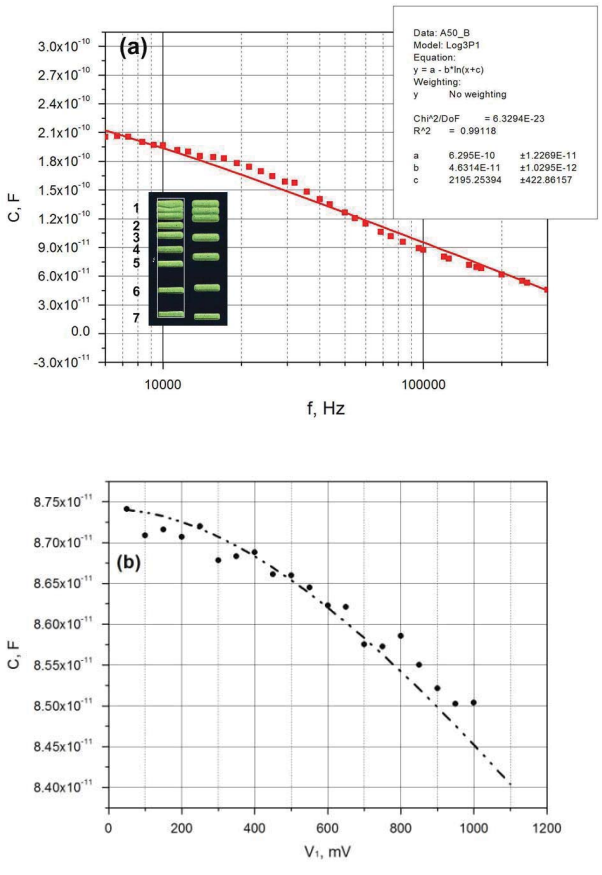



Fig. 4. Dependence of the capacitance between the contacts number 3 and 4 on the measurement frequency (distance between of the contacts is 288 μm, input a.c. signal is 30 mV) (a), and dependence of the capacitance on. the amplitude of a.c. input signal (f= 100 kHz) (b).

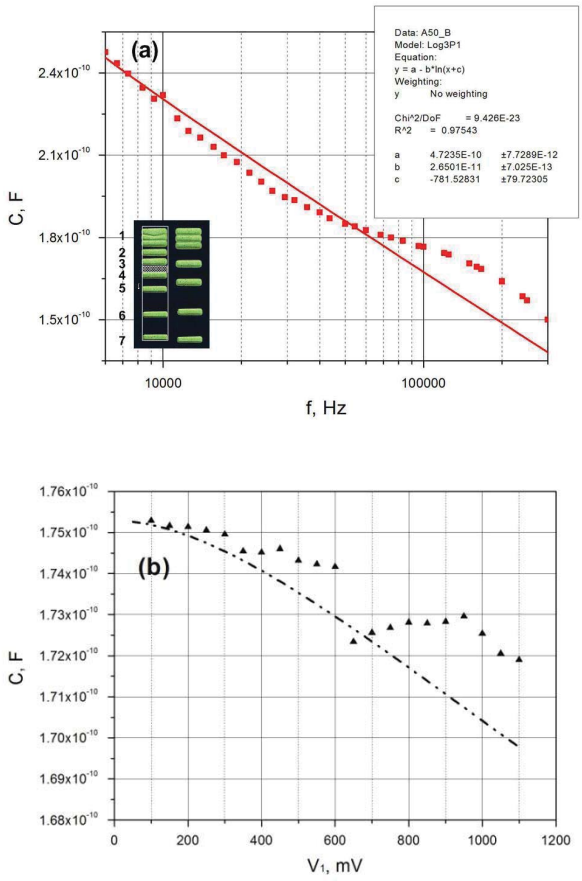



Fig. 5. Dependence of the capacitance between the contacts number 3 and 4 on measurement frequency after the treatment by electron beam with the dose of $1\times10^2$ μC/cm$^2$ (a), and dependence of the capacitance on the amplitude of a.c. input signal (f= 100 kHz) (b).

The dependence of capacitance on the amplitude of a.c. signal can be well described if $E_s$ is presented as $E_F+eV_1$ where $E_F$ is the electron energy in graphene layer. A good agreement can be obtained if $E_F$ ≈2eV that is larger than the electron energy on Fermi level [4].

Observed decreased slope of the dependence C vs. log(ω) after electron beam irradiation of the graphene is not explained in frames of the proposed theory. Probably there are also other phenomena effecting the dependence of graphene capacitance vs. measurement frequency. Charge trapping in the states located in the graphene/$SiO_2$ interface can be considered as an alternative effect.

## V. Conclusions

The observed effect of the dependence of graphene capacitance on measurement frequency is explained by manifestation of the contact capacitance between 3D metal layer and 2D graphene. The theory of this phenomenon for the case of low-mobility graphene on $SiO_2$ layer is presented.

## References

[1] A. Shik, "Contact capacitance in the two-dimentional electron gas," J.Phys.: Cond. Mat., vol. 4, pp. L335-L338, 1992.

[2] A. Venugopa, J. Chan, X. Li, C.W. Magnuson, W.P. Kirk, L. Colombo, R.S. Ruoff, and E.M. Vogel, "Effective mobility of single-layer graphene transistors as a function of channel dimensions", J. Appl. Phys., vol. 109, pp.104511-1 - 104511-5, April 2011.

[3] A.N. Nazarov, S.O. Gordienko, P.M. Lytvyn, V.V. Strelchuk, A.S. Nikolenko, A.V. Vasin, A.V. Rusavsky, V.S. Lysenko, and V.P.Popov, "Characterization of graphene layers by Kelvin probe force microscopy and micro-Raman spectroscopy", Phys. Stat. Sol. C., vol. 10, pp. 1172-1175, 2013.

[4] Kun Xu, Caifu Zeng, Qin Zhang, Rusen Yan, Peide Ye, Kang Wang, Alan C. Seabaugh, Huili Grace Xing, John S. Suehle, Curt A. Richter, David J. Gundlach, and N. V. Nguyen, "Direct Measurement of Dirac Point Energy at the Graphene/Oxide Interface", Nano Letters, vol. 13, pp. 131-136, December 2012.

# 2016 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon

## Author Index


### A

Adachi, K. ... 96
Adamu-Lema, F. ... 234
Agopian, P.G.D. ... 13, 162, 198, 242, 246
Al-Ameri, T. ... 234
Alarcon, E. ... 143
Aldegunde, M. ... 52
Alexander, C. ... 56
Ali, S.-Z. ... 155
Alper, C. ... 20
André, N. ... 155
Andrieu, F. ... 88, 174
Asenov, A. ... 56, 234
Athanasiou, S. ... 151
Aymerich, X. ... 84

### B

Baccarani, G. ... 16
Bae, Y. ... 44
Balakrishnan, K. ... 127
Baldauf, T. ... 1
Barraud, S. ... 5, 112, 124, 170
Baumgartner, O. ... 147
Bawedin, M. ... 104, 174
Baylac, E. ... 88
Beck, R.B. ... 190
Ber, K. ... 190
Berthelon, R. ... 88
Bittner, K. ... 48
Blanc Pelissie, D. ... 222
Bordallo, C.C.M. ... 242
Bounouar, M.A. ... 218
Bourdet, L. ... 112
Brachtendorf, H.G. ... 48
Brinciotti, E. ... 238
Brown, A.R. ... 56
Buca, D. ... 24
Bühler, R.-T. ... 186

### C

Caimi, D. ... 127, 214
Calmon, F. ... 166, 218
Campabadal, F. ... 84
Cassé, M. ... 112, 170
Chalker, P.R. ... 28
Changala, J. ... 222
Cheng, B. ... 56
Cho, I.-T. ... 44
Chowdhury, M.F. ... 178
Claeys, C. ... 13, 162, 198, 242
Claverie, A. ... 88
Collaert, N. ... 162
Corna, A. ... 124
Crespo-Yepes, A. ... 84
Cristoloveanu, S. 44, 104, 131, 151, 174, 214, 222, 238
Crupi, F. ... 139
Czornomaz, L. ... 104, 127, 214

### D

Damianos, D. ... 222
De Franceschi, S. ... 124
de Streel, G. ... 116
Demel, H. ... 147
Deshpande, V. ... 104, 127, 214
Dettmer, W. ... 52
Dimitriadis, C.A. ... 92
Djara, V. ... 104, 127, 214
Donetti, L. ... 100
Drouin, D. ... 218
Dubois, F. ... 166
Dutartre, D. ... 88


ISBN 978-1-4673-8608-1

IEEE Catalog number CFP1649D-USB

## E

El Dirani, H. ..... 131
El Hajjam, K.G. ..... 218
Elmessary, M.A. ..... 52
Esseni, D. ..... 139

## F

Farokhnejad, A. ..... 64
Faynot, O. ..... 170
Feng, X. ..... 36
Ferrari, P. ..... 131
Filipovic, L. ..... 120
Flandre, D. ..... 116, 155, 159
Fompeyrine, J. ..... 127, 214
Fonteneau, P. ..... 131
Francis, L.A. ..... 155
Funakubo, H. ..... 72

## G

Galy, Ph. ..... 151
Gámiz, F. ..... 20, 40, 68, 100, 230
García-Loureiro, A.J. ..... 52
Georgiev, V.P. ..... 234
Gérard, P. ..... 155
Ghibaudo, G. ..... 92, 135
Giacomini, R. ..... 116, 186
Glass, S. ..... 24
Głuszko, G. ..... 182
Gnani, E. ..... 16
Godoy, A. ..... 100, 230
Golanski, D. ..... 131
Gomeniuk, Y.V. ..... 254
Gonzalez, M.B. ..... 84
Gonzalez-Medina, J.M. ..... 230
Graef, M. ..... 64
Graziosi, T. ..... 166
Grillet, C. ..... 108
Grossi, A. ..... 80

## H

Haendler, S. ..... 92
Hain, F. ..... 64
Hall, S. ..... 28
Haond, M. ..... 88, 116, 135
Hartmann, J.M. ..... 24
Hashemi, P. ..... 127
Heinzig, A. ..... 1
Hofmann, E. ..... 24
Hokazono, A. ..... 96
Hong, S.-M. ..... 250
Horst, F. ..... 64
Hosenfeld, F. ..... 64
Hosey, G.P. ..... 206
Hössinger, A. ..... 120, 226
Hutin, L. ..... 124

## I

Iannazzo, M. ..... 143
Ikonic, Z. ..... 24
Im, K.-S. ..... 44
Indalecio, G. ..... 52
Iñíguez, B. ..... 64
Ionescu, A.M. ..... 20
Ionica, I. ..... 104, 222, 238
Iwai, H. ..... 36

## J

Jang, J.-H. ..... 250
Jasiński, J. ..... 194
Jaud, M.-A. ..... 5
Jehl, X. ..... 124
Jin, J.D. ..... 28
Josse, E. ..... 88
Jungemann, C. ..... 48

## K

Kakushima, K. ..... 36
Kalna, K. ..... 52
Kaminski-Cachopo, A. ..... 222
Karatsori, T.A. ..... 92
Karbasian, G. ..... 32
Karner, M. ..... 147
Kataria, S. ..... 143
Kazemi Esfeh, B. ..... 159
Kernstock, C. ..... 147
Kienberger, F. ..... 238
Kilchytska, V. ..... 116, 159
Kloes, A. ..... 64
Kotekar-Patil, D. ..... 124
Kryger, M. ..... 222
Kurosawa, M.K. ..... 72

## L

Lacord, M.-A. ..... 5
Langer, R. ..... 162
Lanuzza, M. ..... 139
Lavieville, R. ..... 124
Lee, J.-H. ..... 44
Lee, Ju.-H. ..... 44
Legrand, C.A. ..... 131, 151
Lemme, M.C. ..... 143

ISBN 978-1-4673-8608-1

IEEE Catalog number CFP1649D-USB

Leroux, C. ..... 135
Lesieur, P. ..... 166
Li, G. ..... 155
Li, J. ..... 112
Lindberg, J. ..... 52
Luong, G.V. ..... 178

## M

Maestro, M. ..... 84
Majkusiak, B. ..... 194
Malesińska, J. ..... 182
Manstetten, P. ..... 120
Mantl, S. ..... 24, 178
Marcelli, R. ..... 238
Marin, E.G. ..... 230
Marin-Cudraz, D. ..... 131
Marquez, C. ..... 40
Martin, M.D.V. ..... 246
Martinie, S. ..... 5, 112
Martin-Martinez, J. ..... 84
Martino, J.A. ..... 13, 162, 174, 198, 242, 246
Matsuzawa, K. ..... 96
Maurand, R. ..... 124
Mazurak, A. ..... 194
Medina-Bailon, C. ..... 100
Michalas, L. ..... 238
Mikolajick, T. ..... 1
Millar, C. ..... 56
Mitard, J. ..... 162
Mitrovic, I.Z. ..... 28
Mitterbauer, F. ..... 147
Miyata, T. ..... 96
Mohamad, B. ..... 135
Moselund, K. ..... 9
Mukasyan, A. ..... 32

## N

Nafria, M. ..... 84
Nagy, D. ..... 52
Nakagawa, S. ..... 72
Narimani, K. ..... 178
Navarro, C. ..... 5, 174
Nawratil, G. ..... 226
Nazarov, A.N. ..... 254
Nedjalkov, M. ..... 56
Nicolas, R. ..... 88
Niquet, Y.-M. ..... 112, 124
Novo, C.D. ..... 186

## O

O'Connor, E. ..... 127
Ohata, A. ..... 40
Oliveira, A.V. ..... 162
Olivo, P. ..... 80
Orlov, A. ..... 32
Ortolland, S. ..... 88

## P

Padilla, J.L. ..... 20
Pala, M. ..... 108
Palestri, P. ..... 139
Pandey, H. ..... 143
Park, H.J. ..... 104
Passi, V. ..... 143
Pavan, P. ..... 76
Pavanello, M.A. ..... 170
Paz, B.C. ..... 170
Pelloux-Prayer, J. ..... 112
Pereira, A.S.N. ..... 116
Perez, E. ..... 80
Perić, D. ..... 52
Petrosyan, S. ..... 210
Pirro, L. ..... 104, 214, 238
Planes, N. ..... 116
Poiroux, T. ..... 88
Poncelet, O. ..... 155
Prégaldiny, F. ..... 210
Puglisi, F.M. ..... 76

## R

Rama, I. ..... 84
Raskin, J.-P. ..... 159
Reggiani, S. ..... 16
Reimbold, G. ..... 135, 170
Rideau, D. ..... 112, 135
Riel, H. ..... 9
Rodriguez, N. ..... 40
Rodriguez, R. ..... 84
Rooyackers, R. ..... 13, 198, 242
Ruiz, F.G. ..... 230

## S

Sadi, T. ..... 56
Sampedro, C. ..... 100
Sano, N. ..... 60
Sanquer, M. ..... 124
Sant, S. ..... 9
Sasaki, K.R.A. ..... 174
Savoy-Navarro, A. ..... 166
Schenk, A ..... 9
Schulte-Braucks, C. ..... 24, 178
Selberherr, S. ..... 120, 202, 226
Selmi, L. ..... 139
Seoane, N. ..... 52

ISBN 978-1-4673-8608-1

IEEE Catalog number CFP1649D-USB

Shaw, A. ..... 28
Shuto, Y. ..... 72
Silveira, M.A.G. ..... 186
Simoen, E. ..... 13, 162, 198, 242
Šimonka, V. ..... 226
Sivieri, V.B. ..... 198, 242
Slobodyan, A.M. ..... 254
Snider, G. ..... 32
Solaro, Y. ..... 131
Sousa, M. ..... 127
Stange, D. ..... 24
Stanojevic, Z. ..... 147
Strangio, S. ..... 139
Sugahara, S. ..... 72
Sverdlov, V. ..... 202

## T

Takamura, Y. ..... 72
Tanaka, C. ..... 96
Thean, A. ..... 162, 198, 242
Theodorou, C.G. ..... 92
Tiagulskiy, S.I. ..... 254
Tienda-Luna, I.M. ..... 230
Tomaszewski, D. ..... 182
Toral, A. ..... 230
Trellenkamp, S. ..... 178

Triozon, F. ..... 112
Trommer, J. ..... 1

## U

Udrea, F. ..... 155

## V

Vandooren, A. ..... 13, 198, 242
Vignetti, M.M. ..... 166
Vinet, M. ..... 5, 124, 170
Visciarelli, M. ..... 16
Vitrant, G. ..... 222
Vodapally, S. ..... 44
von den Driesch, N. ..... 24

## W

Wang, L. ..... 56
Wang, X. ..... 234
Weber, W.M. ..... 1
Weinbub, J. ..... 120, 226
Wenger, C. ..... 80
Witters, L. ..... 162
Won, C.-H. ..... 44
Wong, H. ..... 36
Wrench, J.S. ..... 28

## Y

Yamamoto, S. ..... 72
Yesayan, A. ..... 210
Yu, D. ..... 36

## Z

Zambelli, C. ..... 80
Zeng, Y. ..... 155
Zhang, J. ..... 36
Zhao, Q.T. ..... 24, 178

ISBN 978-1-4673-8608-1 IEEE Catalog number CFP1649D-USB

ISBN 978-1-4673-8608-1