

Physical Modeling of the Hysteresis in MoS₂ Transistors

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Abstract—The hysteresis in the gate transfer characteristics of transistors made of two-dimensional materials is one of the most obvious problems of this novel technology. Here we attempt for the first time to develop a physical modeling approach for describing this hysteresis in devices based on two-dimensional materials. Our model is based on a drift-diffusion TCAD simulation coupled to a previously established non-radiative multiphonon model for describing charge capture and emission events in the surrounding dielectrics, which are considered the main cause for the observed hysteresis. We validate our model against measurement data on a back-gated single-layer MoS₂ transistor with SiO₂ as a gate dielectric. Our study provides new insights into the physical reasons for the observed hysteresis, thereby leading the way towards an alleviation of this problem in future devices.

I. INTRODUCTION

Molybdenum disulfide (MoS₂) is a two-dimensional (2D) material of the large group of transition metal dichalcogenides (TMDs), which has received a lot of attention over the past few years because of its inherent and comparatively large transport band gap ($E_G = 2.48$ eV [1]). This renders it an ideal candidate for applications in digital electronics [2–4], as it enables high current on/off ratios and a large transconductance [5].

However, up to now, MoS₂ based FETs have not met the high expectations for example when judging device performance in terms of mobilities. When accurately accounting for the non-negligible contact resistances [6], the mobility extracted for MoS₂ layers using multi-terminal measurements at room temperature does not exceed about 100 cm²/Vs [7]. Besides that, while this mobility value lies in a range comparable with standard silicon technology, the large variability observed in the device characteristics and performance issues like the frequently observed hysteresis in the gate transfer ($I_D(V_G)$) characteristics [8–12] and the typically large drifts of the threshold voltage (V_{th}) over time [13] are to the present day one of the most critical obstacles inhibiting any industrial applications of MoS₂ FETs.

Complementing our previous experimental works [13–15], here we present a detailed study on the main mechanisms governing the hysteresis phenomenon in the $I_D(V_G)$ characteristics of MoS₂ FETs. Our study is based on a drift-diffusion TCAD model [16] coupled to a four-state non-radiative multiphonon (NMP) model, which is necessary to accurately describe charge capture and emission events in the underlying gate dielectric [17]. Here we apply this simulation methodology which was originally developed and established for silicon (Si) technologies [18, 19], to devices based on 2D materials such as MoS₂. Our results confirm that the ubiquitous charge trapping at oxide traps is one of the main reasons for the hysteresis in MoS₂ FETs [13] and provide new insights into the details of these trapping and detrapping processes.

II. DEVICES AND MEASUREMENTS

A description of the device fabrication and measurement techniques we use here as a proof-of-concept for our modeling method have been reported in detail elsewhere [13]. For the sake of completeness, we give a short summary of all the details which will be important for understanding the simulation results later on. For demonstration purposes we study a back-gated MoS₂ FET using thermal silicon dioxide (SiO₂) as a back gate dielectric. The FET is based on a single layer (SL) flake of MoS₂ ($d \approx 6.5$ Å), obtained via mechanical exfoliation [20]. The titanium/gold (Ti/Au) electrodes for the source and drain contacts were fabricated using electron beam lithography and metal evaporation techniques [8]. As a final fabrication step, the device was annealed in vacuum ($< 5 \times 10^{-6}$ Torr, $T = 120$ °C) in order to reduce the contact resistances and to remove adsorbed impurities. The $I_D(V_G)$ characteristics of the MoS₂/SiO₂ FET were measured using a sweep range of $V_G \in [-20$ V, 20 V] at a temperature of $T = 25$ °C in vacuum ($< 1 \times 10^{-5}$ Torr). Several $I_D(V_G)$ s were recorded using a varying sweep rate $S = \Delta V/\Delta t$ (with ΔV as the voltage step and Δt as the time step), which corresponds to a sweep frequency of $f = 1/T$ with T being the total sweep time.

III. SIMULATION OF INITIAL DEVICES

Here, the general simulation methodology using drift-diffusion based TCAD [16] is validated against a measured $I_D(V_G)$ curve. The drift-diffusion equations [21] are computationally very efficient [22] and completely sufficient for describing the charge transport through the channel of these large-area MoS₂ FET prototypes. In several recent works [23–25] compact models describing devices based on 2D channel materials with drift-diffusion equations have been developed. The drift-diffusion equations can be used because the lateral dimensions of our devices are in the micrometer range ($W \times L \approx 7.0$ μm² for the device discussed here). As a consequence, the large number of scattering centers in the channel region result in scattering-dominated drift-diffusion charge transport.

We extend an existing drift-diffusion based device simulator [16] to this new device class and use the material parameters summarized in Table I. The list of parameters is divided into two sections. The first section contains material constants, extracted mainly from the thorough DFT study of Rasmussen *et al.* [1, 28] on TMDs. The second section contains material parameters which should be constant but which are strongly influenced either by the defects in the channel region or by the contacts [6, 27]. For these parameters we only give meaningful ranges according to literature, within which the values should be chosen. At the current stage of research these parameters have to be treated as fitting values and have to be adjusted to every device separately. The impact of the most important material

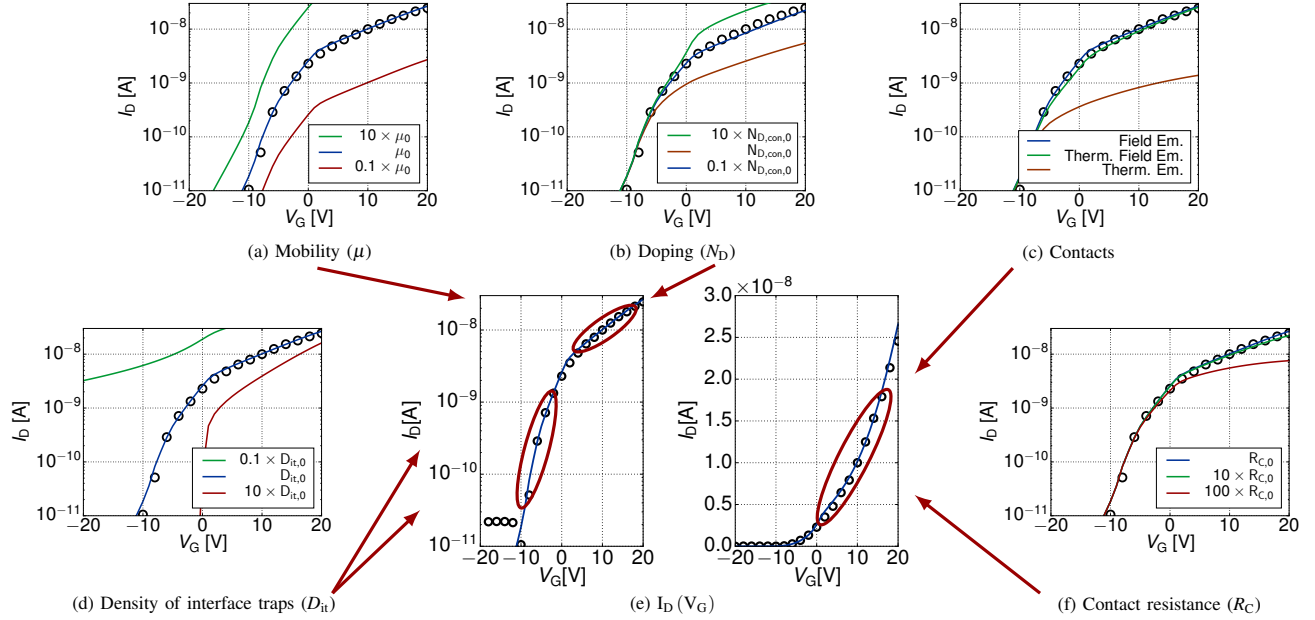


Fig. 1: $I_D(V_G)$ fit of the drift-diffusion based TCAD model to a measured curve (black circles) and illustration of the impact of the most important physical fit parameters on this characteristic (a)-(d),(f). The material properties on the left hand side (mobility (a), doping (b) and density of interface defects (d)) serve as fit parameters, because in this immature technology there is apparently a huge number of defects in the channel region ($D_{it} \approx 10^{13} \text{cm}^{-2} \text{eV}^{-1}$). The figures on the right hand side (contacts (c), contact resistance (f) and doping (b)) are used to demonstrate the impact of contact-related model parameters on the $I_D(V_G)$. These parameters are especially critical for MoS₂ FETs, as these devices are known to be Schottky barrier transistors [26].

parameters on the $I_D(V_G)$ is illustrated in Fig. 1. The central Fig. 1(e) demonstrates the quality of the fit, which can be established with the proposed simulation methodology. Our model is able to capture all aspects of the $I_D(V_G)$ visible on a logarithmic scale as well as on a linear scale.

The doping, the mobility, and the density of interface traps are quantities which are strongly related to the defects in the channel region. Therefore, they are fit parameters for the currently available MoS₂ FET prototypes. The mobility (μ) has an impact on the saturation current ($I_{D,sat}$) as well as on V_{th} (Fig. 1(a)). The doping level (N_D) affects only $I_{D,sat}$ (Fig. 1(b)). While these two parameters are inherent parameters of any drift-diffusion model, the impact of interface defects was considered by using the standard Shockley-Read-Hall (SRH) model [31], coupled to the drift-diffusion based TCAD simulator [16]. The density of interface traps (D_{it}) is a very

TABLE I: Simulation parameters used for drift-diffusion based TCAD simulations. The parameters in the first section are material constants, while the parameters in the second section are strongly influenced by defects and contacts [6, 27] and therefore, at the current stage of research, vary from device to device.

Parameter	Value/Range	Reference
Transport band gap (E_G)	2.48 eV	[1]
Electron affinity (χ)	-3.84 eV	[1]
Electron mass (m_n^*)	0.55	[1]
Hole mass (m_p^*)	0.56	[1]
Eff. rel. permittivity (ϵ_r^{eff})	≈ 4	[28]
Contact resistance (R_C)	$[10^4, 10^6] \Omega$	[27]
Work func.diff.(Ti/Au) (E_W)	$[0.05, 0.2] \text{eV}$	[27]
Mobility (μ)	$[0.1, 100] \text{cm}^2/\text{Vs}$	[6, 7, 29]
Doping (N_D)	$< 1 \times 10^{16} \text{cm}^{-3}$	[30]
Den. of interface traps (D_{it})	$[10^{12}, 10^{13}] \text{cm}^{-2} \text{eV}^{-1}$	[30]

important parameter, affecting at the same time the subthreshold slope and $I_{D,sat}$ through electrostatic doping [25, 32, 33] (Fig. 1(d)). This parameter has been studied in detail by Takenaka *et al.* [30], who associated the typical density of interface traps observed for MoS₂ FETs with sulfur vacancies in the MoS₂ layers.

As MoS₂ FETs are known to be Schottky barrier transistors [26], the work function differences between the contacts and the MoS₂ layer and the contact resistances R_C are very important parameters for an accurate description of the $I_D(V_G)$ s. In Fig. 1(c) the impact of different models for describing the current transport across Schottky barriers is shown. In general one distinguishes between thermionic emission, thermionic-field emission and field emission, depending on whether the thermionic current over the barrier or the tunneling current through the barrier dominates. In the approximation of pure field emission, one usually speaks of an Ohmic contact, while for pure thermionic emission one requires equations describing the transport over Schottky contacts [34, 35]. As stated previously [6, 32], the short tunneling distance in a 2D layer gives rise to large tunneling currents, thereby justifying the approximative modeling of MoS₂ FETs with a pure field emission model in the back-gated configuration.

This conclusion renders the work function difference unimportant in the case of back-gated devices [36] while the contact resistance remains an important fit parameter, the impact of which is demonstrated in Fig. 1(f). In relation to the contacts, it has been recently discussed in literature that only the reactions at the interface of the MoS₂ layer with the Ti adhesion layer enable a good contact to SL MoS₂ through covalent bonding [27, 37]. This coincides nicely with our observation that in our model the doping levels below the contacts ($N_{D,con}$) are by far more important than the intrinsic doping level of the SL MoS₂ ($N_{D,L}$) in the channel. Even for intrinsic doping levels of up to half of the effective doping in the contact region due to Ti atoms ($N_{D,L} < 0.5 \times N_{D,con}$) the device behavior remains dominated solely by $N_{D,con}$. From this we conclude that the impact of the Ti

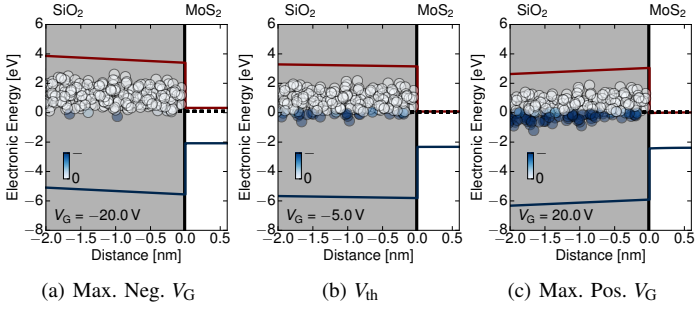


Fig. 2: Band diagrams of the MoS₂/SiO₂ FET at different gate voltages showing the electron trapping band [38, 39] responsible for the hysteresis.

adhesion layer does not lie solely in the establishment of covalent bonds for adequate contacts, but maybe even more importantly in the unintentional but essential introduction of defect states in certain regions of the band gap of SL MoS₂, corresponding to an effective doping of the layer, $N_{D,con}$. Therefore, only the impact of $N_{D,con}$ on the $I_D(V_G)$ is demonstrated in Fig. 1(b).

IV. DEFECT MODELING

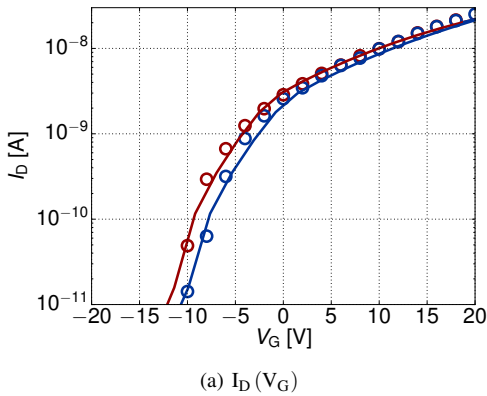
Having successfully established a good fit of the $I_D(V_G)$ characteristics, we now take the next step towards modeling the hysteresis. In order to see a shift in the threshold voltage between the up sweep and the down sweep of an $I_D(V_G)$, there has to be charge trapping in the vicinity of the channel. While several groups claim that the charge trapping takes place at the interface [11, 40, 41], we argue here in accordance with our previous works [13–15] that the fact that the largest hysteresis is observed for a total sweep time of $T = 200$ s is a strong argument in favor of oxide traps, as they usually have larger time constants than interface traps. What is more, oxide traps are located at a finite distance from the interface, the most important ones for the charge transfer processes lying typically within the first few nanometers. This leads to an increased bias dependence, which is especially important to explain the hysteresis in MoS₂ FETs. Interface traps provide trap levels inside the band gap, thus once the Fermi level reaches the conduction band edge (roughly at $V_G \approx V_{th}$) and remains pinned there due to the effective doping of the layer, $N_{D,con}$, there are

to a first approximation no more trapping and detrapping events at interface states. However, exactly these charge capture and emission events for gate voltages above the threshold voltage are the reason for the observed hysteresis.

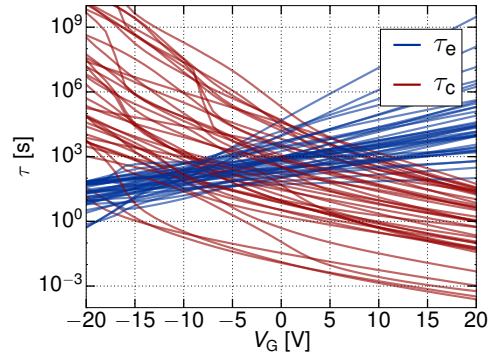
For the modeling of the hysteresis we use the four-state NMP model, which accurately describes charge transfer reactions in conventional Si/SiO₂ devices [17]. It does not only account for the energy balance of the transferred electrons, as it is usually done when using the SRH model [31], but it also considers the energetic relaxation of the structure around the defect, where the electron is captured or emitted [17]. Depending on the microscopic nature of the defect, which has been studied in great detail for SiO₂ based on Si/SiO₂ FETs [42, 43], one usually speaks either of hole or of electron trapping. As the charge transfer process is exactly the same in both cases, the two processes can only be distinguished by the charge change of the trapping defect in the oxide, which either goes from positive to neutral (hole trap) or from neutral to negative (electron trap).

Thus, in order to explain the hysteresis in MoS₂ FETs we use the two known defect bands of SiO₂ from silicon technologies [19, 38, 39], with the first being a donor-like hole trapping band located at $E_T^L = 4.6(3)$ eV below the conduction band edge of SiO₂ [19], and the second most likely being an acceptor-like electron trapping band at $E_T^U = 2.6(4)$ eV below the conduction band edge of SiO₂. The second defect band is less well known, but has already been observed for Si-based devices with dielectric gate stacks [38, 39]. Additionally, it has been used in our previous works for the modeling of the hysteresis and of bias-temperature instabilities in FETs based on MoS₂ [13, 15] and black phosphorus [14].

Fig. 2 illustrates how charges are trapped and detrapped in the oxide. At a positive gate voltage, the defect band is bent downwards, leading to more electron trapping, thereby causing a shift in the threshold voltage. However, if the same traps emit their electrons during the down sweep, no hysteresis can be observed. At this point the time constants of the responsible defects, as determined by the four-state NMP model, come into play. A trap can only contribute to the hysteresis if it captures an electron at a high gate voltage and emits this electron not before reaching again the low level of the gate voltage. This means that the electron capture time constant (τ_c) of the respective trap has to be smaller than the electron emission time constant (τ_e) at high gate voltages and vice-versa. For this criterion



(a) $I_D(V_G)$



(b) Bias dependence of time constants.

Fig. 3: Established hysteresis fit (red - up-sweep, blue - down-sweep), together with a time constant plot for an exemplary set of defects, selected to display the defects contributing to the hysteresis in our simulations.

the important voltage level is V_{th} , where the hysteresis is extracted, which lies for our devices at around $V_{th} \approx -5V$. If for $V_G < V_{th}$ it holds, that $\tau_e < \tau_c$ and for $V_G > V_{th}$ it holds that $\tau_e > \tau_c$, this trap can in principle contribute to the hysteresis.

The gate bias dependence of the time constants of some selected traps, contributing to the hysteresis in our simulations, are shown in Fig. 3 (b). In Fig. 3 (a) the established fit between the measured $I_D(V_G)$ and the simulated characteristics is presented. Our simulation results clearly corroborate the previously observed [13] PBTI-like hysteresis.

V. CONCLUSIONS

A drift-diffusion based simulation methodology was used to describe the charge capture and emission processes in gate oxide traps resulting in the hysteresis observed in the $I_D(V_G)$ characteristics of back-gated SL MoS₂ FETs. Our results emphasize that the voltage dependence of the time constants of the traps is an essential quantity, which has to be considered when identifying the traps responsible for the hysteresis phenomenon.

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