Benchmarking Time-Dependent Variability of Junctionless Nanowire FETs

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***Abstract*— Time-dependent variability of junctionless gate-all-around nanowire pFETs is studied through measurements and simulations. The variability, related to effects such as Random Telegraph Noise (RTN) and Bias Temperature Instability (BTI), is discussed in terms of the distribution of individual charged gate oxide trap threshold voltage shifts. This distribution is shown to be shaped by i) the electrostatics of the device, and ii) percolative source-drain conduction. It is concluded that the time dependent variability of our JL GAA NW pFETs is comparable to previously measured pFinFETs. However, provided that other sources of variability are suppressed, JL FETs time-zero and time-dependent variability may remain high due to the high body doping**.

Keywords—Time-Dependent Variability, Gate-All-Around Nanowires, Junctionless FETs, Single charged trap impact

I. Introduction

Nanowire (NW) FETs with gate all around (GAA) have superior channel control and are considered as a frontrunner device architecture for CMOS beyond the 5nm node [1,2]. With the industry's capability to fabricate narrow FET bodies, Junctionless (JL) devices become a viable alternative to the standard Inversion Mode (IM) devices (Fig. 1) [3]. JL FETs are simpler to manufacture, as complex junction engineering becomes unnecessary, making JL FETs an attractive option for e.g. 3D sequential integration. In IM FETs, high current and hence high carrier concentration is achieved by high doping of source and drain regions, with a lowly doped channel. However, by the nature of the JL device, its body is highly doped to maintain high carrier concentration in the source [3]. *This raises concerns about potentially high variability of JL FETs.*

The gate oxide electric field E_{ox} needed to switch a FET device is entirely used to create an inversion channel in IM FETs. In contrast, JL FETs operate in depletion or accumulation [3-5]. E_{ox} in JL FETs is more evenly distributed between the on and off states, resulting in lower absolute electric field applied to the gate oxide at operating conditions. Gate-oxide-related degradation mechanisms, such as BTI and HCI are therefore significantly suppressed in JL FETs [4,5].

To advance the assessment of JL FET reliability, here we study their *time-dependent* variability. As will become evident below, we trace the origins of time-dependent variability to device electrostatics, which are most conveniently understood in terms of threshold voltages V_{th} and their shifts ΔV_{th}. During device operation, time-dependent variability ($\sigma_{\Delta Vth}$), due to degradation effects such as Random Telegraph Noise (RTN), Bias Temperature Instability (BTI), and Hot Carrier Degradation (HCD) will add onto the as-fabricated, *time-zero* variability (σ_{Vth0}). The *relative* time-dependent variability ($\sigma_{\Delta Vth}/\sigma_{Vth0}$), benchmarked in Fig. 2 for multiple technologies, is therefore a simple indicator to circuit designers of how serious time-dependent effects are in their variability-aware designs.

Specifically, for the JL pFETs at hand, we *find that the time dependent variability $\sigma_{\Delta Vth}$ of our JL GAA NW pFETs is comparable to previously measured pFinFETs* [6]. The relative time-dependent variability ($\sigma_{\Delta Vth}/\sigma_{Vth0}$) of our *JL GAA NW pFETs* is found to be low when compared with other technologies (Fig. 2) [7]. This is, however, ascribed to the relatively high time-zero variability σ_{Vth0} of our JL devices.

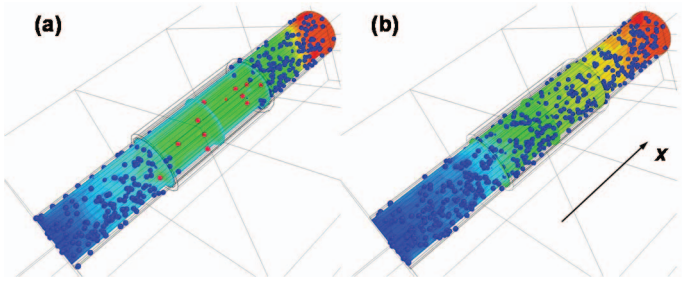

Fig. 1: Illustration of (a) Inversion Mode (IM), and (b) Junctionless (JL) GAA NW FET devices (spheres: dopants). High current and hence high carrier concertation are achieved by high doping of source and drain regions. By the nature of the JL device, this implies high doping of its body as well.

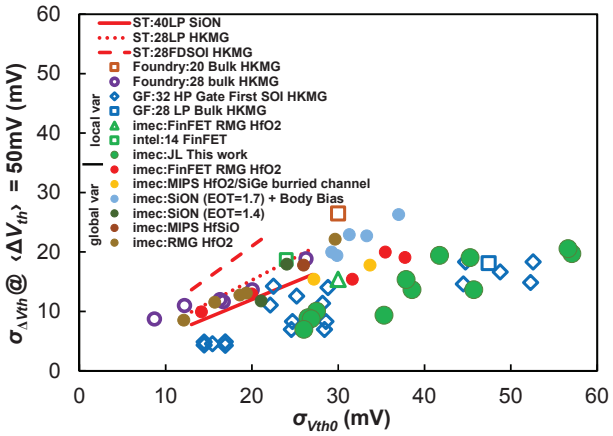

Fig. 2: Benchmark plot showing relative comparison of time-zero (σ_{Vth0}) and time-dependent ($\sigma_{\Delta Vth}$) variability of pFET devices for different technologies. Since $\sigma_{\Delta Vth}$ depends on degradation, the mean V_{th} shift of 50 mV must be specified. Data in "local var" group were corrected for across-wafer variability using matched pairs or local arrays, "global var" data were not. JL GAA NW pFETs discussed here (large green circles) show *relatively* low $\sigma_{\Delta Vth}$.

We have previously shown that ΔV_{th} variability can be well understood in terms of the mean impact of an individual charged gate oxide trap η. To gain more insight into JL GAA NW FET variability, we corroborate our electrical measurements with simplified, proof-of-concept atomistic TCAD simulations. The simulations confirm our previous conclusions—the intrinsic time-dependent variability is linked to the statistics of single-trap impacts [8], shaped by i) the electrostatics of the device, and ii) percolative source-drain conduction [9]. The former component depends on the device type (IM or JL), the latter on the amount of variability ("randomness") in the channel, due to e.g. random dopant fluctuations.

The implications are then extended toward multiple-trap statistics using the defect-centric model and the main features of the benchmark plot (Fig. 2) are reproduced. It is concluded that *the time dependent variability of our JL GAA NW pFETs is comparable to previously measured pFinFETs*. However, provided that other sources of variability are suppressed, JL FETs time-zero and time-dependent variability may remain high due to the high body doping.

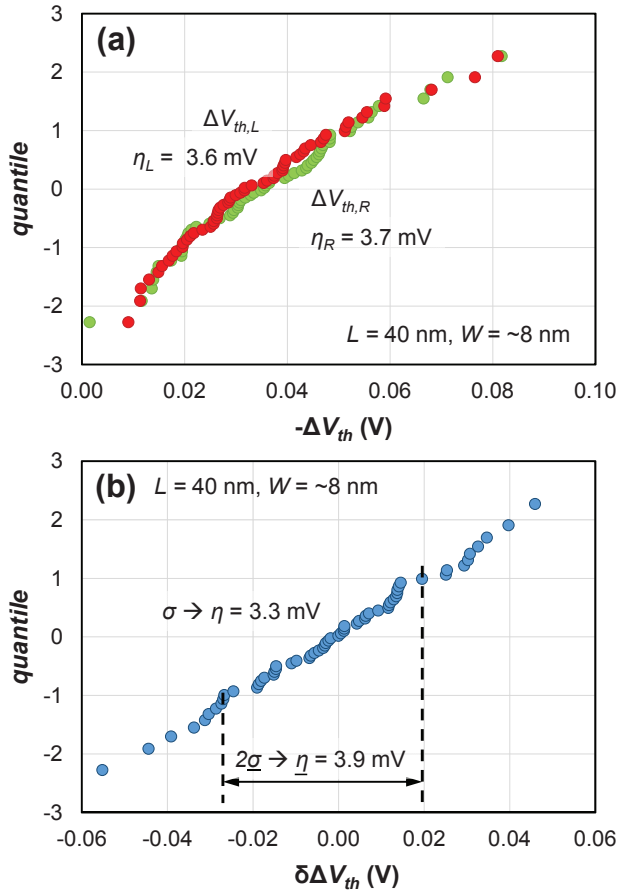

Fig. 3: (a) Well-behaving (i.e., without outliers) "defect-centric" distributions for "Left" and "Right" devices with the η values extracted using Eq. 3 indicated. (b) The distribution of $\delta\Delta V_{th}$ calculated from the corresponding values $\Delta V_{th,L}$ and $\Delta V_{th,R}$ of each matched pair taken from (a). The distribution is *approximately* Normal. The "robust" value (underlined) correctly reproduces the standardly-obtained value of η.

II. Electrical Measurements

The synopsis of the measured devices and the experimental methodology in the following subsection should elucidate the extracted time-zero and time-dependent variability data, discussed afterwards.

A. Experimental considerations

The fabrication and characteristics of the JL GAA NW pFET devices used here have been published previously [1]. JL pFETs with variable length L (40 – 1000 nm as drawn), approximately rectangular cross-section with two different widths W (20 and 40 nm as drawn → 8 and 28 nm as fabricated [1]), height H = 22 nm, and varying number of nanowires (1 and 5) were studied. The bodies were doped to ~2-3×10^{18} cm^{-3}. Note that the cross-section uniformity of longer devices (> ~80 nm) could not be maintained along the device length due to processing issues.

Closely-spaced *matched* NW FET device *pairs* were measured at room temperature to correct for across-wafer variability in order to extract the random component of both time-zero and time-dependent variability [10-12]. 30-60 pairs of each device size were used in each statistical sample. First, the initial threshold voltages V_{th0} of the "Left" and the "Right" devices were extracted and the differences

$$\delta V_{th0} = V_{th0,L} - V_{th0,R} \quad (1)$$

were calculated for each pair. The variance of the *random* component, representing the "intrinsic" *time-zero* variability, free of process-induced across-wafer effects is then calculated as

$$\sigma^2_{V_{th0}} = \sigma^2_{\delta V_{th0}}/2. \quad (2)$$

We have previously linked *time-dependent* variability with the *mean impact of a single charged trap* η [8]. All devices were therefore stressed one by one by applying negative gate voltages and stress times such as to obtain mean threshold voltage shifts $\langle\Delta V_{th}\rangle$ of tens of millivolts.

If we assume that the distribution ΔV_{th} due to multiple trapped charges is "defect-centric" (cf. Fig. 3a) [8], η can be extracted from the first two statistical moments of the distribution as

$$\eta = \frac{\sigma^2_{\Delta Vth}}{2\langle\Delta V_{th}\rangle}. \quad (3)$$

The value of thus-extracted η can be, however, affected by across-wafer variability, particularly if data are collected from the entire 12" wafer.

Following the same argument as for Eqs. 1 and 2, the "intrinsic" *random* component of the *time-dependent* variability can be extracted from the *differences* of threshold voltage *shifts* of the "Left" and the "Right" devices of each pair

$$\delta\Delta V_{th} = \Delta V_{th,L} - \Delta V_{th,R}. \quad (4)$$

The distribution of $\delta\Delta V_{th}$ for two "well-behaving" "Left" and "Right" devices of a given size is shown in Fig. 3b.

The variance of the random *time-dependent* variability component is then calculated as [8, 11]

$$\sigma^2_{\Delta V_{th}} = \sigma^2_{\delta\Delta V_{tho}}/2. \quad (5)$$

During the measurement of a large number (5000+) of devices, outlier ΔV_{th} values are inevitably generated and must be dealt with in scripted, automated data processing. Several criteria, such as $I_{source} \sim I_{drain}$, $I_{gate} << I_{drain}$, etc. are therefore built into the analysis to root out faulty devices. Still, remaining outliers can severely distort the standard deviation values extracted from the δV_{th0} and $\delta\Delta V_{th}$ distributions. We therefore use a simple "robust" estimator of σ, extracted from the values between -1st and 1st quantiles, as illustrated in Fig. 3b. Thus-designed robust estimator is not susceptible to outliers appearing at the tails of the δV_{th0} and $\delta\Delta V_{th}$ distributions. Fig. 3b also shows that for "well-behaving" distributions, the robust estimator, designated with an underline and used henceforth, correctly reproduces the standardly-obtained value.

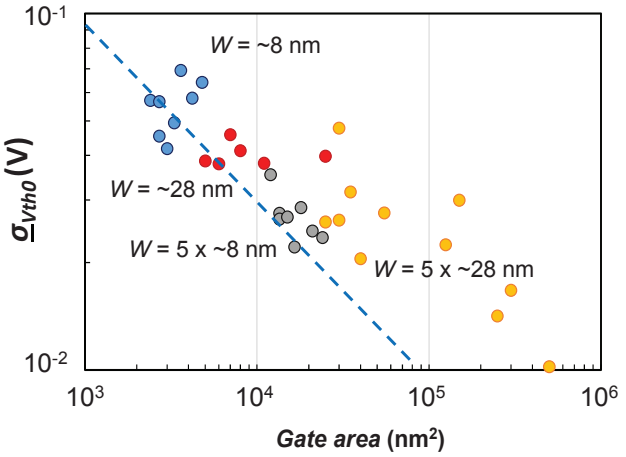

Fig. 4: *Time-zero* variability σ_{Vth0} of JL pFETs of varying dimensions, determined from matched pairs to compensate for across-wafer variability. The shortest devices of each *W* group follow approx. the expected square-root gate area dependence (dashed line) [10].

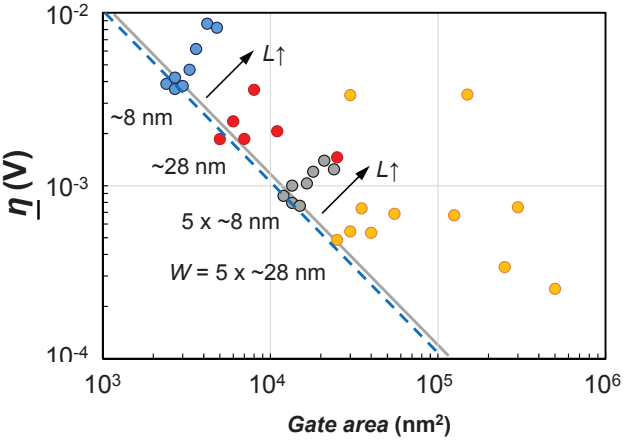

Fig. 5: Time-dependent variability of JL pFETs, extracted from matched pairs [12] and expressed via the mean impact of a single trap η. The shortest devices follow reciprocal area dependence (dashed line), similar to pFinFET devices (gray solid line) [6]. Longer devices in each group show increased variability (arrows), likely due to narrowing of wires caused by processing.

B. *Experimental results*

As-fabricated, i.e. time-zero variability of our JL devices, extracted using Eqs. 1-2 is shown in Fig. 4. The shortest devices follow approx. the expected square-root gate area dependence (dashed line). The Pelgrom coefficient $A_{Vth} \sim 3$ mV.µm is somewhat higher than for standard technologies [1, 13]. Longer devices show increased variability.

The mean impact of a single trap η of JL pFETs, extracted using Eqs. 3-5, is shown in Fig. 5. The shortest devices follow reciprocal area dependence. The magnitude of JL η is almost identical to pFinFET devices measured previously [6], i.e., *our JL pFETs do not appear to manifest increased time-dependent variability over their FinFET counterparts*. Longer devices in each group again show increased variability due to the abovementioned processing issues and are disregarded in the subsequent analysis.

Finally, the time-dependent variability $\sigma_{\Delta Vth}$ at $\langle\Delta V_{th}\rangle$ = 50 mV is calculated from the data in Fig. 5 using Eq. 3. The resulting values for well-behaving (i.e., close to the dashed lines in Figs. 4 and 5) devices are plotted vs. the corresponding time-zero variability σ_{Vth0} into the benchmark plot in Fig. 2, together with data from other technologies. Fig. 2 shows the time-dependent variability $\sigma_{\Delta Vth}$ of our JL GAA NW pFETs is *relatively* low. This could be, however, ascribed to the relatively high time-zero variability σ_{Vth0} of our devices, as discussed in Section IV.

III. Simulations

In order to better understand our measurements, we have performed *continuous-doping* and *atomistic* simulations of both IM and JL GAA NW pFETs. Idealized, "proof-of-concept" device geometries are simulated to extract and to understand the main underlying principles. The results are, nevertheless, in good *quantitative* agreement with our measurements as well. Although many sources of variability of the channel potential are likely present in our devices, only random dopant distribution (RDD) is introduced as a simple, yet representative means to randomize the channel potential.

We have previously linked the intrinsic time-dependent variability, extracted in the previous section, to the "exponential" statistics of single-trap impacts. The statistics is controlled by a single, physical parameter η, representing the average impact of a trapped gate oxide charge on the device threshold voltage shift Δv_{th} [8]. (Note that a small "*v*" is used for individual traps). Furthermore, we have recently argued that the single-trap impact Δv_{th}, approximately exponential distribution is shaped by i) the electrostatics of the device, and ii) percolative source-drain conduction [9]. This concept is discussed here again for both IM and JL GAA NW FETs and the similarities and differences are highlighted.

A. *Simulation setup*

The ~28 nm wide and ~22 nm tall NWs are simulated for the sake of simplicity as cylinders with diameter D = 25 nm. Devices of such relatively conservative dimensions are also not

strongly affected by quantum-mechanical effects, which are not considered here [14]. The junctions in the IM pFET devices are doped to 10^{21} cm^{-3}. Junction dopant diffusion, a potentially significant source of variability in IM devices, is not considered.

First, linear-regime I_d-V_g characteristics are calculated for devices with *continuous* (CONT) and *atomistic* (i.e., RDD) doping. V_{th0} extracted at a fixed I_d is used for σ_{Vth0} calculation. A positively charged trap is then introduced into a random position at the gate oxide/silicon interface, I_d-V_g characteristics are recalculated and Δv_{th} is extracted with respect to the respective V_{th0}. Some dependence of the Δv_{th} values on the chosen I_d has been observed [6,15]. The process is repeated 100× for both IM and JL devices for each doping level N_d, with re-instantiated dopant and trap locations, to generate statistics.

B. *Origins of single-trap Δv_{th} distribution*

We now examine the factors influencing the shape of the Δv_{th} distribution and confirm the explanation presented previously for planar FETs [9] is valid for both IM and JL GAA NW FETs.

The impact of individual trapped charges along the channel on GAA NW pFETs is shown in Fig. 6. As it is apparent from the *continuous-doping* simulation, the impact of a charged trap Δv_{th} is controlled by the device *electrostatics*. In IM FETs, $\Delta v_{th,CONT}$ decreases significantly when the trap is located close to the source and the drain junctions [9,16]. In contrast, the single-trap impact $\Delta v_{th,CONT}$ in JL FETs is more evenly distributed along the JL body. Finally, the maximum Δv_{th} is higher in IM devices because of their surface conduction is more strongly impacted by gate oxide traps. Around V_{th}, JL conduction proceeds through the bulk (center) of the device.

Fig. 7 then contains the $\Delta v_{th,CONT}$ profiles from Fig. 6 sorted into a standard CCDF plots. A clear saturation of both IM and JL $\Delta v_{th,CONT}$ distribution tails is due to the maximum impact of trapped charge in the middle of the FET (cf. Fig. 6, $\Delta v_{th,CONT}$).

From Fig. 6 it is also apparent that the values of Δv_{th} are further randomized around $\Delta v_{th,CONT}$ when RDD is activated. This results in a widening of the corresponding cumulative distributions in Fig. 7 and these distributions appear approximately exponential, as stipulated previously [8].

The additional impact of RDD on Δv_{th} is due to the percolative nature of source-drain conduction and can be easily deconvoluted by dividing $\Delta v_{th,RDD}$ by $\Delta v_{th,CONT}$ for each simulated FET instance. The distribution of this ratio appears to be *log-normal* (Fig. 8), as observed previously in meticulously calibrated simulations for planar FETs [9]. This indicates a fundamental underlying nature of this distribution [17].

The width of the $\Delta v_{th,RDD}$ / $\Delta v_{th,CONT}$ distribution increases with doping, in line with the picture of the randomly distributed dopants randomizing the channel potential. This trend is more formally expressed in the value of the log-normal scale parameter σ_{perc} (Fig. 8) increasing with doping as $N_d^{0.5}$ (Fig. 9).

As a side note, we remark that the values of σ_{perc} in Fig. 9 are generally higher for JL devices. We can only *speculate* at this

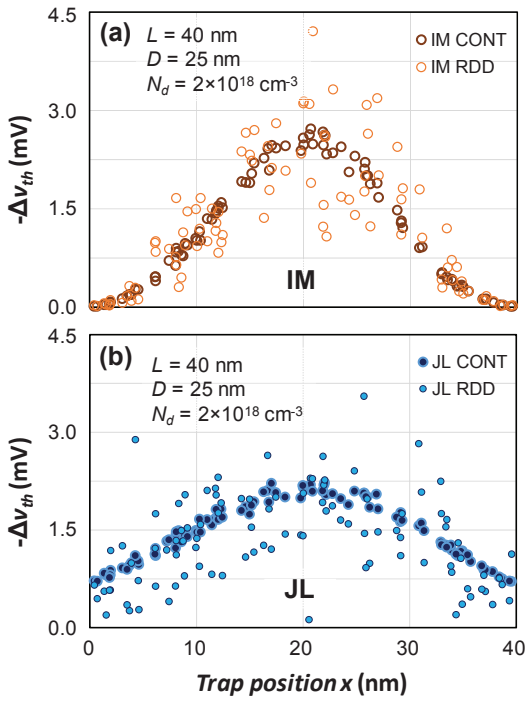

Fig. 6: The impact of single, positively-charged traps at position x along the device channel (cf. Fig. 1) on device threshold voltage shift $\Delta v_{th,}$ for (a) IM and (b) JL GAA NW pFETs, calculated with continuous (CONT) and atomistic (RDD) doping profiles. RDD is observed to further randomize the impact around the "mean" CONT profiles. In IM FETs, traps close to the source/drain junctions contribute little to Δv_{th} (a), while the single-trap impact in JL FETs is more evenly distributed along the JL body (b).

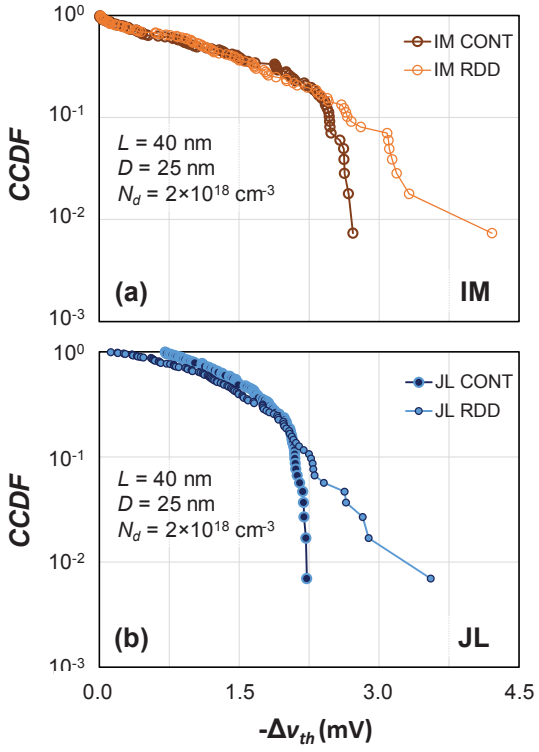

Fig. 7: Simulated Δv_{th} profiles from Fig. 6 are sorted into Complementary CDF (CCDF) plots for (a) IM and (b) JL GAA NW pFETs. RDD adds an approximately exponential tail to the CONT distributions.

point that this disparity may be related to the bulk vs. surface conduction in respectively JL and IM devices.

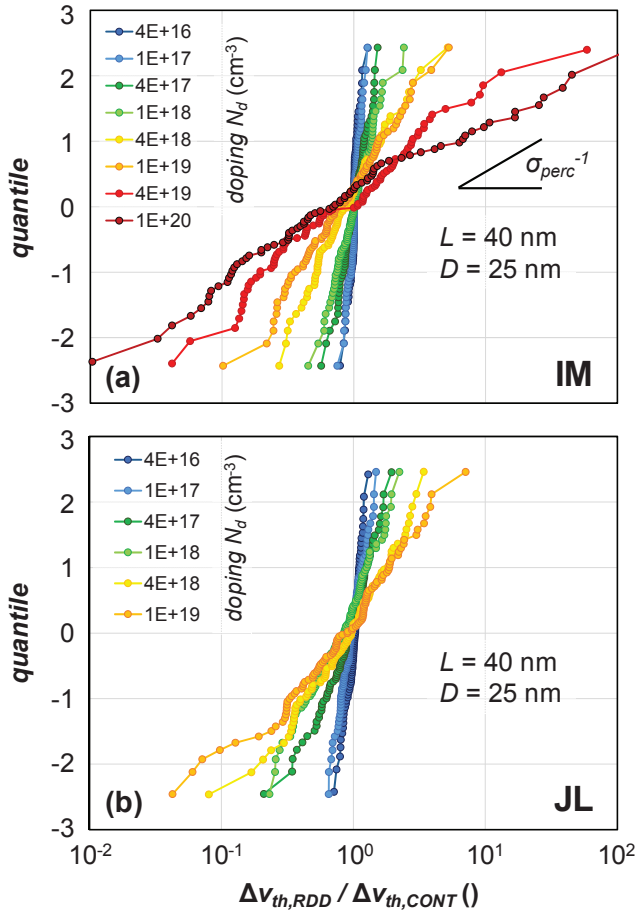

Fig. 8: The ratio of $\Delta v_{th,RDD}$ / $\Delta v_{th,CONT}$ constitutes the added impact of RDD to the device electrostatics (i.e., $\Delta v_{th,CONT}$, cf. Fig. 7). The distributions of this ratio can be acceptably described with a log-normal with parameter σ_{perc} for both (a) IM and (b) JL GAA NW pFETs, for a wide range of doping levels. Note: IM distributions are simulated to higher doping levels, resulting in wider distributions then those of the JL devices.

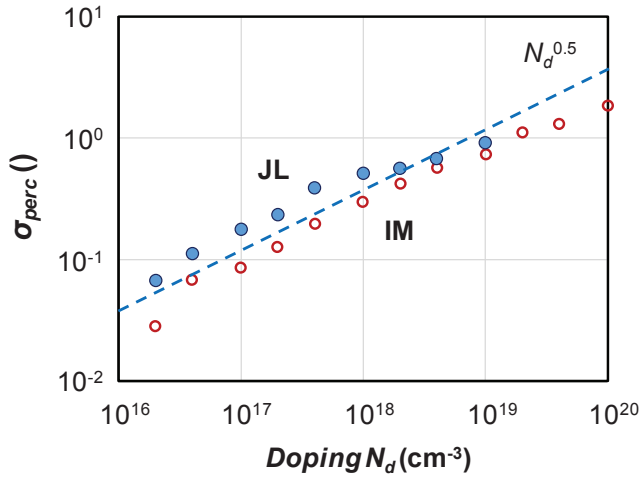

Fig. 9: The scale parameter σ_{perc}, controlling the width of the log-normal $\Delta v_{th,RDD}$ / $\Delta v_{th,CONT}$ distributions in Fig. 8, increases with $N_d^{0.5}$ for both IM and JL GAA NW pFETs.

We can now understand the GAA NW FET single-trap Δv_{th} distributions in Fig. 10 as a convolution of i) the electrostatics of the device ($\Delta v_{th,CONT}$), and ii) percolative source-drain conduction ($\Delta v_{th,RDD}$ / $\Delta v_{th,CONT}$) [9]. For *lowly-doped channels*, $\sigma_{perc} \rightarrow 0$ and the single-trap distributions Δv_{th} will take the concave shape of $\Delta v_{th,CONT}$ in Fig. 7. Note also that the single-trap impact on the JL devices is overall lower but more pronounced at high CCDF values (large circles in Fig. 10) than in the IM devices. This is related to the impact near the gate edges, cf. Fig. 6. For *higher-doped channels*, the source-drain percolative log-normal $\Delta v_{th,RDD}$ / $\Delta v_{th,CONT}$ component increases (σ_{perc} increases as per Fig. 9). As a result, the Δv_{th} distributions (Fig. 10a) widen and become more convex (log-normal) [9].

We remark that log-normal Δv_{th} distribution [18,19] would be more detrimental than an exponential distribution as a log-normal diverges from an exponential at high percentiles and reaches to higher Δv_{th} values (this trend is apparent in Fig. 10a). A log-normally distributed Δv_{th} would be therefore a significant concern for small-area devices with distributed degradation mechanisms (RTN, BTI, HCD).

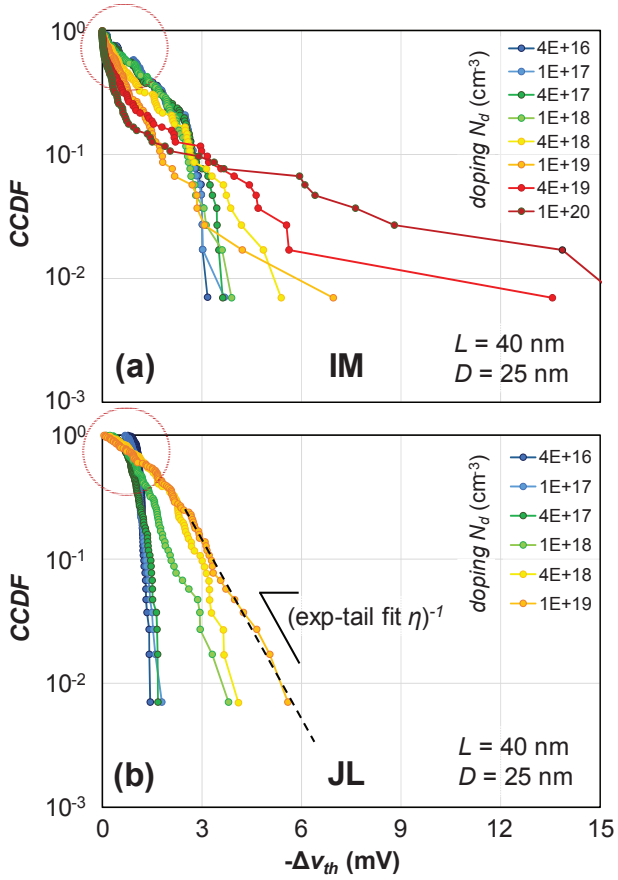

Fig. 10: Simulated distributions of single-trap impact on (a) IM and (b) JL GAA NW pFETs. The distributions are shaped by i) the electrostatics, including source and drain regions, and ii) percolative conduction, resulting in different shapes for IM and JL devices, esp. at high CCDF values (circles). Consequently, mean impact per charged trap $\eta \neq$ value of η extracted from the exponential-like tail of the distribution (example: dashed line in (b)). Note: IM distributions are simulated to higher doping levels, resulting in wider distributions then those of the JL devices.

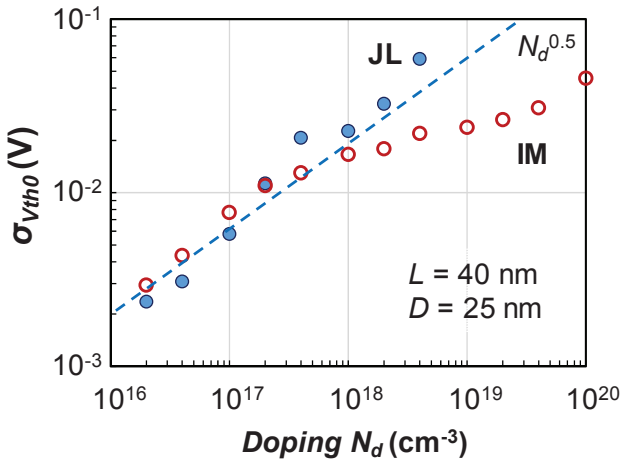

Fig. 11: Simulation of simplified IM and JL GAA NW pFETs shows the time-zero variability σ_{Vth0} of both types of devices is broadly identical and follows approx. square-root dependence (dashed line) at lower doping levels.

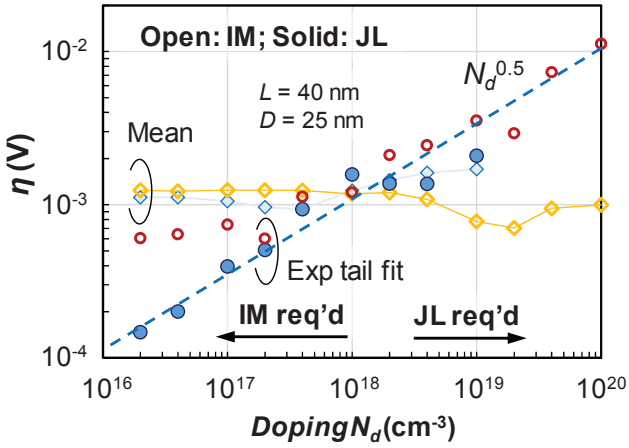

Fig. 12: Simulated impact per single trap η. Exp-tail-fit η, extracted as shown in Fig. 10, follows approx. $N_d^{0.5}$ dependence on doping (dashed line). Required doping *trends* for IM and JL devices are indicated by arrows.

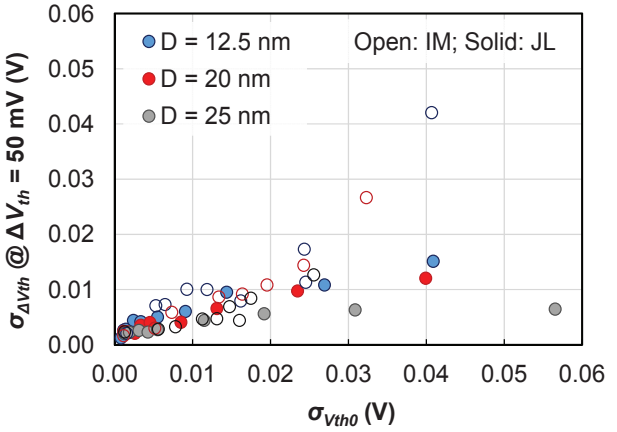

Fig. 13: IM and JL pFETs simulation results (time-zero: Fig. 5; time-dependent: Figs. 6-8) arranged into the benchmark plot (Fig. 2). The relatively low $\sigma_{\Delta Vth}$ of JL FETs observed experimentally (Fig. 2) is reproduced. (In this plot only, simulation results of different NW dimensions are shown.)

IV. Discussion

The simplified simulations show *time-zero* variability σ_{Vth0} follows approx. $N_d^{0.5}$ (Fig. 11), slightly higher than the $N_d^{0.4}$ trend reported elsewhere [20]. For $N_d > \sim 10^{18}$ cm^{-3}, we note that $\sigma_{Vth0,JL} > \sigma_{Vth0,IM}$.

The *time-dependent* variability caused by multiple traps is linked to the single-trap impact Δv_{th} distribution (Fig. 10) through the defect-centric model. As explained in the previous section, *the distribution of Δv_{th} is not inherently exponential*. Consequently, η is extracted from the distributions in Fig. 10 in two manners: i) "mean" η, obtained by simply averaging all values of the corresponding distribution, and ii) "exp-tail-fit" η, extracted from the distribution tail, as given in Fig. 10b. The latter "exp-tail-fit" η will be principal for Exp-Poisson distribution tails [21,22]. The result of the extraction for different simulated levels of doping is shown in Fig. 12.

For a strictly exponential distribution, the "mean" η should equal to the "exp-tail-fit" η. This is, within a factor of 2, the case for the IM devices below $N_d \sim 2\times10^{18}$ cm^{-3}. Note that for low doping, the "exp-tail-fit" η is still appreciable in our IM GAA NW FETs due the appreciable impact of the junctions on the relatively short device, cf. Figs. 6a and 7a. *The Δv_{th} distribution in IM devices can therefore be acceptably described as exponential.* The additional modulation by junctions is, however, missing in our simulated JL FETs and the exponential tail is virtually non-existent in the Δv_{th} distribution at low doping levels for these devices (cf. the low JL "exp-tail-fit" η values in Fig. 12).

We now note that our experimental observations are broadly consistent with our simulations at 2-3×10^{18} cm^{-3} doping levels. Specifically, the values of η for IM and JL GAA NW devices are similar in the simulations, as well as in the NW and FinFET measurements in Fig. 4 ($\eta \sim 2$ mV for $L \sim 40$ nm and $W \sim 28$ nm). While this is the intended doping level of our JL devices, IM FinFET devices have typically lower channel doping ($N_d <$ ~10^{17} cm^{-3}). We speculate that at this low doping, other sources of variability (surface roughness, metal work function variations, fixed oxide charge, interface states, etc.) may be taking over fin variability control, resulting in variability equivalent to 2-3×10^{18} cm^{-3} doping levels. This would be also consistent with the *time-zero* variability (Fig. 11), which is higher for JL devices at these doping levels. This trend is at last confirmed in the composite of our simulations in Fig. 13, which reproduces the JL variability measurements in the benchmark plot in Fig. 2.

We therefore conclude that the low *relative* $\sigma_{\Delta Vth}/\sigma_{Vth0}$ variability of our JL devices in Fig. 2 is primarily not due to the lower impact of charged traps but *more likely due to their increased time-zero variability*. Moreover, while we foresee that the variability of IM devices can be controlled if the presumed dominant sources of variability are suppressed, this is not the case for JL devices. By their nature, JL devices will require large doping levels, to the point that they may be controlled by the percolative *log-normal* component.

V. Conclusions

We have measured and extracted the time-dependent variability of JL GAA NW pFETs. The variability was discussed in terms of the distribution of impact of individual charged gate oxide traps and the factors influencing the shape of this distribution have been revealed. It was concluded that the time dependent variability of our JL GAA NW pFETs was comparable to previously measured pFinFETs. However, provided that other sources of variability are suppressed, JL FETs time-zero and time-dependent variability may remain high due to the high body doping.

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