Implications of Gate-Sided Hydrogen Release for Post-Stress Degradation Build-Up after BTI Stress

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***Abstract*— Contrary to irradiation damage, where the post-irradiation build-up of degradation is a commonly reported feature, degradation after BTI stress typically recovers monotonically. However, occasional reports on irregularities during recovery have been published. We will show here that – consistent with a gate-sided hydrogen release mechanism – additional degradation can apparently build-up during recovery also after BTI stress, which can under certain circumstances even exceed the post-stress degradation levels. This additional degradation may invalidate existing lifetime extrapolation methods and must therefore be carefully understood. Our results demonstrate that although post-stress degradation build-up is only visible under certain conditions, it is an essential feature of BTI and thus provides important clues on its microscopic origin.**

I. Introduction

Characterization of the bias temperature instability (BTI) is very challenging due to the extremely slow kinetics of the defects involved. In order to generate appreciable degradation, accelerated stress conditions are typically used to characterize BTI. While acceleration at increased temperatures ($< 250°C$) has previously been shown to give results consistent with non-accelerated conditions [1–4], voltage acceleration above use-voltages has long been suspected to charge additional defects which would otherwise not be able to contribute at use-voltages.

Typically, the recovery of the threshold voltage shift after BTI stress, ΔV_{th}, follows a monotonic logarithmic time dependence, with recovery starting outside even the fastest experimental resolution ($< 1\,\mu s$), and basically going on 'forever' ($>$ months) [5]. Occasionally, deviations from this logarithmic recovery have been observed: particularly using charge-pumping measurements, a post-stress degradation build-up of fast states has been seen [6], an effect particularly strong in H-rich wafers [7]. Also, for positive bias temperature instability (PBTI) a significant post-stress degradation has been reported [8]. Our data suggests that this peculiar behavior is a consequence of the migration of hydrogen from the gate- towards the channel-side of the oxide during stress and back during recovery, activating and deactivating defects along its path [4, 9–15]. We note that this behavior would be consistent with post-irradiation degradation build-up, which is also conventionally attributed to the release of hydrogen from the gate side during irradiation [16].

II. Experimental Setup

In order to systematically check for a possible post-stress degradation build-up following negative bias temperature stress (NBTS), we take our lead from literature and previous results, where this behavior was observed in charge pumping (CP) currents and after longer stress times [6, 7]. From this we conclude that post-stress degradation build-up could be a feature of the permanent component. To bring out the features of the slowly evolving permanent component more clearly, we use higher temperatures up to 200°C. Such high temperatures have been frequently used in NBTI characterization and have otherwise produced results consistent with degradation data recorded at lower temperatures[1, 2]. Voltage acceleration, on the other hand, which has been shown to dramatically enhance the recoverable component, is avoided (unless otherwise noted) by consistently using stress voltages lower than the operating voltage of each technology ($|V_G| \leq |V_{DD}|$) [4]. Furthermore, long stress and recovery times (days, weeks, and months) are used.

We systematically investigate post-stress degradation build-up using samples from 6 different technologies (5 SiON, 1 SiO_2/HfO_2), 4 of them commercial, from 3 different manufacturers to rule out artifacts related to peculiarities of a single product. Also, to rule out experimental errors, measurements were performed in 3 different laboratories, all leading to fully consistent results. We conduct eMSM measurements [5] where each relaxation transient was typically followed by 20 full I_D/V_G sweeps into accumulation (2 s for sweeping from -0.6 V to $+1$ V and 2 s for sweeping back, everything repeated 10 times). These I_D/V_G sweeps were conducted to remove trapped charges from the oxide [1, 4] which are considered a feature of the recoverable component. Note, however, that sweeps into the accumulation region of pMOS transistors results in the injection of electrons into the oxide, which in turn has been shown to lead to the release of atomic hydrogen from the gate side [12, 17–20].

III. Experimental Results

The basic observation in this experimental regime is shown in Fig. 1. As can be seen, already after 1 ks of stress at $V_G = V_{DD}$ and 200°C, following a regular recovery transient for about 1 ks, the recovery starts to turn around. This post-stress degradation build-up becomes stronger with increasing stress times, producing a hump of 13 mV after 1 Ms which only recovers very slowly (months), even at 200°C. This hump can result in degradation *larger* than what would be seen even with fast ($1\,\mu s$) measurements. Also interesting to note is that the I_D/V_G sweeps conducted after the first long 100 ks recovery trace and then on a daily basis only initially perturb the recovery but do not seem to impact the overall recovery trend.

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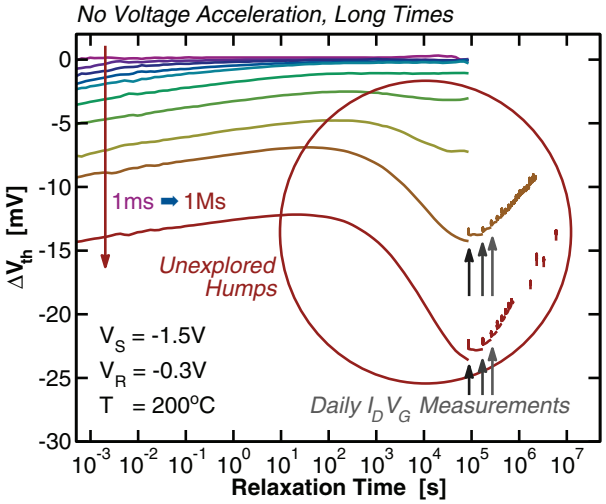

Fig. 1. NBTI recovery at use-voltages but elevated temperatures and for long stress *and* recovery times: Increasingly larger *degradation* is built up during recovery (humps) which recovers only very slowly.

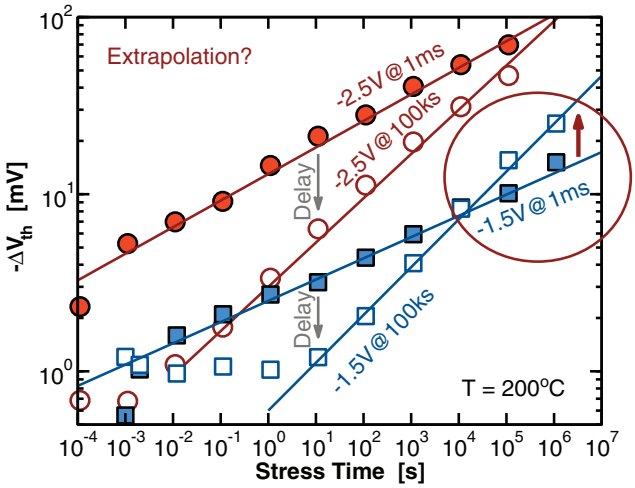

Fig. 3. Extrapolation from voltage accelerated data *misses* post-stress degradation build-up. At use-voltages, degradation measured with a 100 ks 'delay' is *higher* than what is measured using shorter delays.

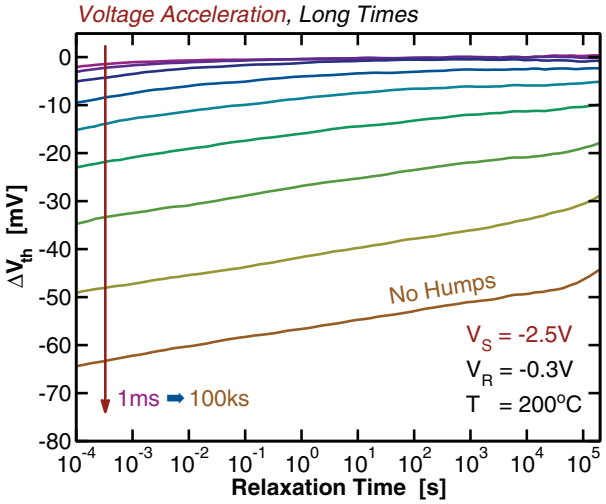

Fig. 2. Typically used voltage acceleration, here −2.5V, leads to charging of a large number of oxide traps which conceal the humps. Typically used stress voltages have been up to −3.5 V in this technology.

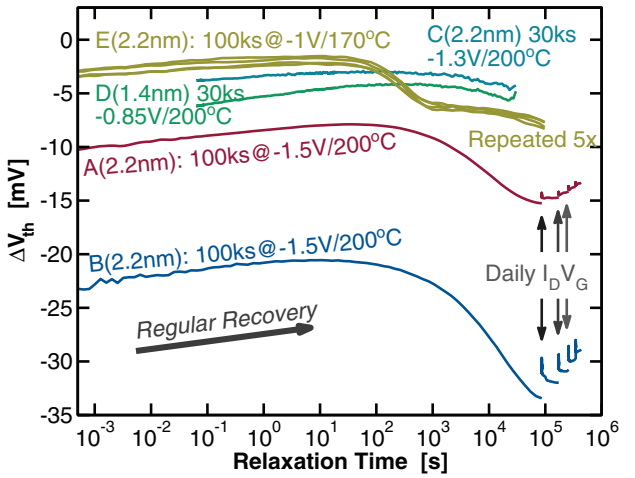

Fig. 4. While there is clearly a strong technology dependence, post-stress degradation build-up was found in *all* 5 investigated technologies. Measurements were taken in 3 different laboratories.

This indicates that the majority of the charges contributing to the hump are either fix positive traps with time constants too large to react to the I_D/V_G sweeps, or that they are due to interface states which only anneal slowly and independently of the gate bias. In any case, they are certainly not simply trapped holes which can be removed by the simple injection of electrons.

This post-stress degradation may result in serious issues for lifetime extrapolation. For example, if a device from the same technology is stressed at $V_G = -2.5$ V, which is an average voltage acceleration (2.2 nm SiON, sustains up to −3.5 V), the accumulated ΔV_{th} after $t_s = 100$ ks is already considerably higher than at −1.5 V, see Fig. 2. Most importantly, however, recovery follows its usual logarithmic dependence *without* any visible humps. If such voltage-accelerated data is extrapolated to V_{DD} using a simple power-law model, the impact of the hump is missed as shown in Fig. 3. For the first time we also observe that ΔV_{th} measured with a large delay (100 ks, about 28h), even exceeds the value recorded with a 1 ms delay, leading to a cross-over of the two fit lines.

To demonstrate that we are dealing with an intrinsic feature of NBTI rather than some strange peculiarity in a particular technology or even an experimental artifact, we investigated a number of samples of 3 different manufacturers in 3 different laboratories, see Fig. 4. While there is a strong process dependence, post-stress degradation clearly occurs in *all* technologies, provided the right stress conditions are used, namely no voltage-acceleration, but long stress and recovery times at higher T.

Furthermore, to rule out initial drifts of the device which are otherwise unrelated to NBTI, we repeatedly apply long stress/relax cycles to the same device using either different voltages (−1 V vs. −1.5 V) or different stress and recovery times (1/2 a day vs. a whole day). As can be seen in Fig. 5,

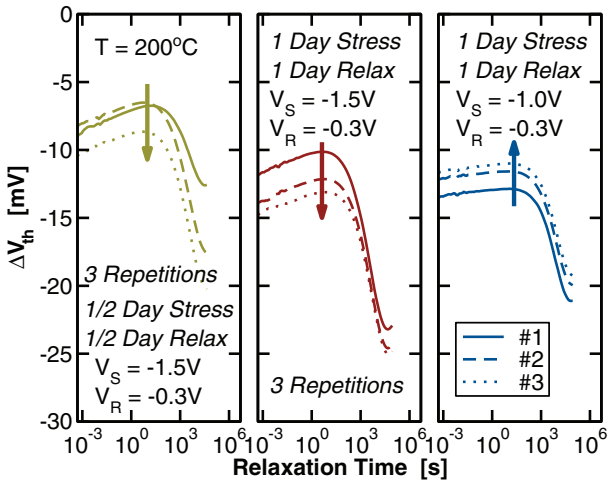

Fig. 5. While the humps recover only slowly around $V_G = V_{th}$ (see Fig. 1), they can be nearly perfectly cycled (shown for 3 times). This clearly shows that they are an intrinsic part of NBTI physics. In the left panel, the device was stressed and recovered for 1/2 day while on the other two a whole day was used. V_s was -1.5 V for the left two panels and -1 V for the right.

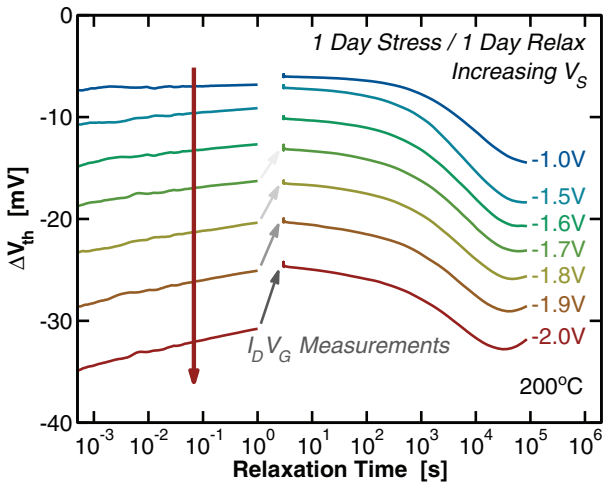

Fig. 6. Relaxation is interrupted after 1 s to remove trapped charges by 20 I_D/V_G measurements (between -0.6 and $+1$ V). All data taken in a single run with increasing V_s, which clearly reveals the humps. With increasing V_s, the height of the hump relative to the measurement at 1 ms decreases.

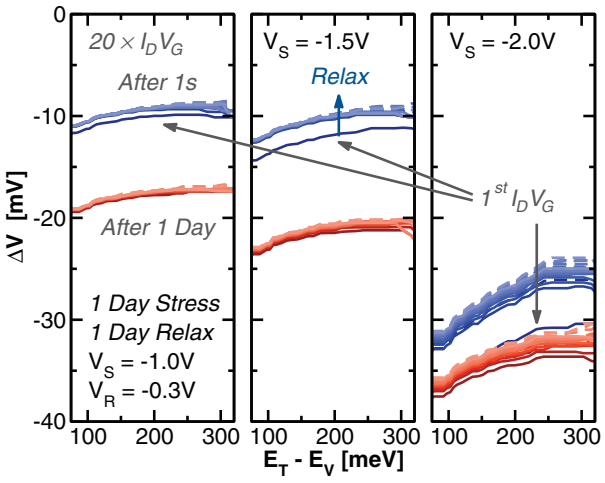

Fig. 7. The constant current voltage shift extracted from the 20 I_D/V_G measurements of Fig. 6 taken after 1 s and 1 day of recovery, plotted as a function of the Fermi-level in the Si bandgap. Post-stress degradation build-up is dominated by states outside the $100-300$ mV range and speculated to be due to states above midgap [10, 22, 23].

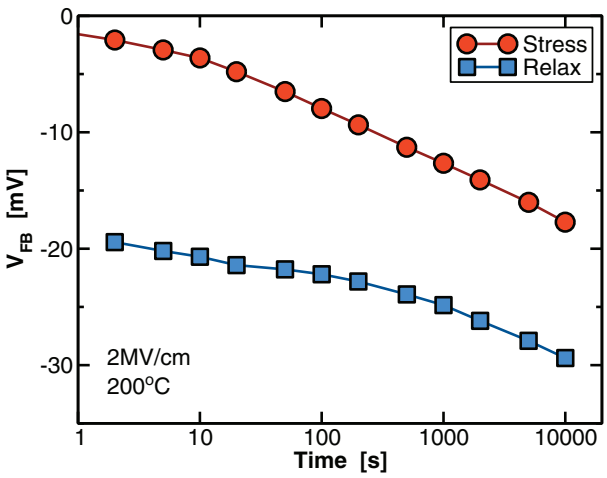

Fig. 8. Post-stress degradation is also observed in HK MOS capacitors at 200°C. Shown is V_{FB} extracted from CV measurements, which keeps degrading after the end of low-voltage stress ($t_s = t_r = 10$ ks).

the humps are removed by the subsequent stress and reappear during the next recovery cycle, clearly confirming that they are an integral part of NBTI degradation and recovery. A similar experiment is shown in Fig. 4 (Sample E), where the stress / recovery cycles are repeated five times in a row on the same device with virtually identical results. Another indication that the observed humps are not due to the drift or diffusion of mobile ions is the fact that the hump in the recovery traces always occurs after about the same recovery time independently of the stress duration in Fig. 1, while with increasing stress duration mainly its amplitude is increased. This would be consistent with a reaction-limited process but is inconsistent with a diffusion-limited process, for which one would expect a retarded occurrence of the hump with increasing stress time [21].

For a first identification of the relevant defects causing the degradation, recovery was interrupted after 1 s to record 20 I_D/V_G curves, then continued for 1 day to record another set of 20 I_D/V_G curves. As shown in Fig. 6, the I_D/V_G measurements immediately terminate the regular logarithmic recovery via the removal of trapped oxide charges to unveil the degradation build-up. It is likely that this build-up of degradation already starts at the beginning of recovery but is masked by the recovery of regular oxide traps. The recorded I_D/V_G curves are analyzed in Fig. 7, which show the horizontal (constant current) difference between the recorded I_D/V_G curves and the initial reference curve as a function of the Fermi-level relative to the Si valence band edge E_V. The DOS of the traps within this window corresponds to the slope of $\Delta V(E_F)$ and is relatively flat, implying that the traps responsible for

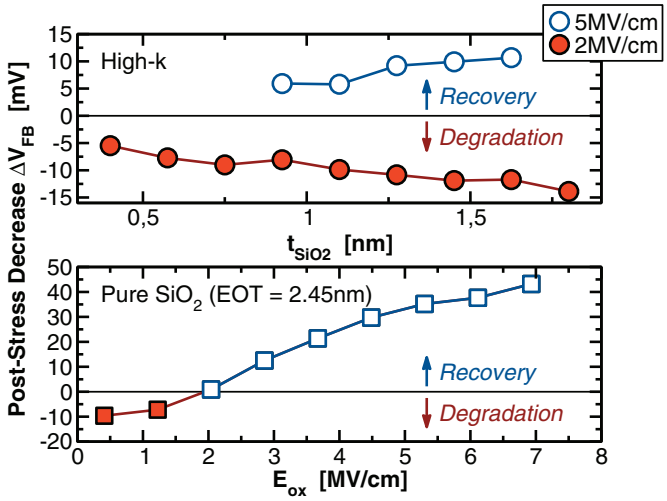

Fig. 9. V_{FB} keeps degrading after low-voltage stress, but relaxes in the expected way after high-voltage stress ($t_s = t_r = 10$ks, 200°C) as seen in Figs. 1 and 2. **Top**: HK with varying thickness of the SiO_2 layer. **Bottom**: Pure SiO_2 for varying E_{ox} during stress.

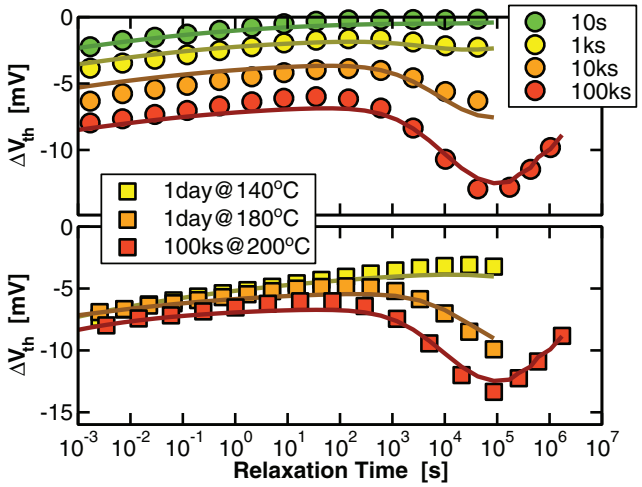

Fig. 10. Post-stress degradation build-up (symbols) can be consistently explained by the recently formulated gate-sided hydrogen release (HR) model (lines), including its time (**top**) and T dependence (**bottom**). Note that the long recovery has a strong impact on the subsequent stress phase.

the shift have their trap-level outside this window (likely around midgap [10, 22, 23]). After 1 day of recovery, this DOS remains basically unchanged but the whole curve is shifted to higher levels, implying that (net) charge has been built up in positively charged defects. Increase of the stress voltage mostly increases the regular recovery but does not change much about this observation.

Next, we investigated the effect using MOS capacitors with SiO_2/HfO_2 and SiO_2 gate stacks. Degradation is monitored using the V_{FB} shift from CV measurements [24]. As can be seen in Fig. 8, when low stress voltages are used, ΔV_{FB} keeps *increasing* during recovery. This is consistent with the I_D/V_G data and suggests that post-stress degradation is due to the temporary build-up of positive charge rather than due to changes of the interface state density. The data in Fig. 9 shows the relative increase/decrease of ΔV_{FB} for various thicknesses of the SiO_2 layer for both low and high voltage stress. While high voltage stress results in the expected behavior (regular recovery of ΔV_{FB}), low voltage stress reveals post-stress degradation.

IV. Discussion

Given the data at hand, a precise identification of the defects responsible for the hump is difficult. Regarding the boundary conditions, the following has to be kept in mind:

- With increasing duration, NBTS creates additional defects near the channel. These defects can be either interface states, e.g. P_b or K_N centers [25, 26] or slow oxide defects which either produce RTN noise [5, 27] or additional discrete recovery steps in small-area devices [4].
- It has been repeatedly shown that during NBTS atomic hydrogen is liberated at the gate-side of the oxide, which then moves towards the channel [11, 13–15, 28]. This highly reactive hydrogen is very likely the cause of the defects created during NBTS. For example, it could either create P_b centers from H passivated silicon dangling bonds via the reaction P_b–H + H → P_b + H_2, or attach itself to strained bridging oxygen centers [18], thereby creating a hydroxyl E' center via the reaction Si–O–Si + H → Si• HO–Si.
- While the barrier for releasing atomic hydrogen is relatively large (1.5 eV [4, 29]), the released atomic hydrogen is very reactive and both reactions suggested above will proceed with very small energetic barriers (0 − 0.2 eV [10, 29]). As a consequence, since the actual diffusion of the hydrogen from the gate towards the channel is very fast (10 ns at 200°C, using parameters from [30]), it is clearly the *release* of the atomic hydrogen which forms the rate-limiting step, consistent with previous assumptions [31, 32].

As such, we have to consider two options to explain the origin of the hump, namely a change in the post-stress oxide charge distribution or the creation of additional dangling bonds. Both options will be discussed in the framework of the recently formulated gate-sided H-release (HR) model [4]. In the current version of the HR model it is assumed that the permanent component is dominated by the redistribution of hydrogen inside the oxide which then becomes charged. The creation of dangling bonds is in principle consistent with the model but currently considered to be of minor importance and neglected for the sake of simplicity. However, this component may be large enough to explain the formation of the hump.

Scenario A: Post-Stress Change in Charge Distribution

By assuming a narrow hydrogen-related defect band close the valence band of Si, the development of a hump with both t_s and T can be explained, see Fig. 10. For such a defect band, humps result from the net difference in positively charged defects near the channel and the effective negative charge build-up near the gate due to an increase/decrease in the number of hydrogen-related defects, see Fig. 11. As the demarcation line between these two regions moves closer to the gate with decreasing T (as a consequence of the competing

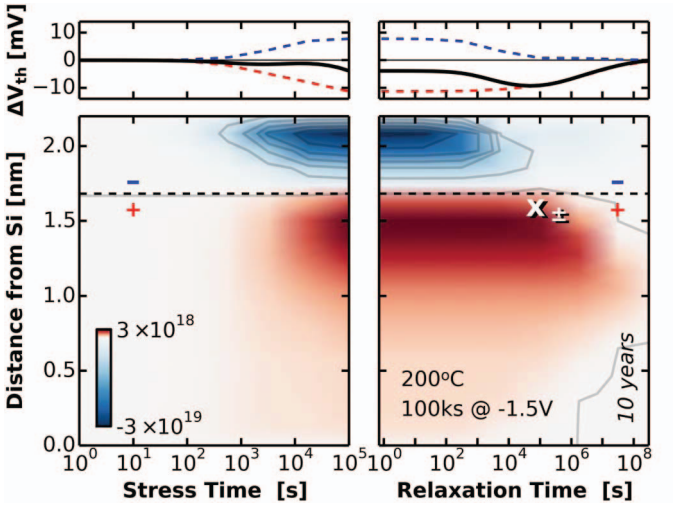

Fig. 11. Post-stress degradation build-up in the 2.2 nm SiO_2 is the net charge trapped near the gate (annihilated neutral defects, blue, above the demarcation line $x_{\pm}$) and the channel (created and positively charged defects, red, below $x_{\pm}$). The gate-sided defects are annealed first, resulting in the hump.

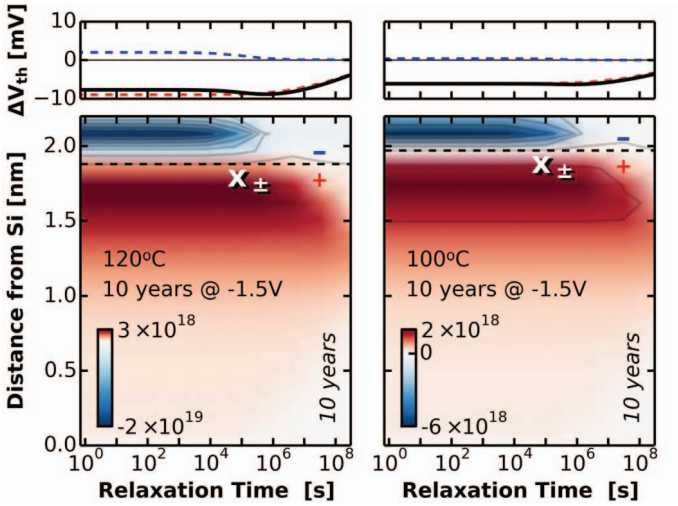

Fig. 12. As T is reduced below 120°C, the demarcation line between the positively and negatively charged regions ($x_{\pm}$) moves closer to the gate, shifting the occurrence of the humps to larger times, but virtually freezing out the humps for $t_s < 10$ years.

non-radiative multiphonon charge exchange between channel and gate [33–35]), the hump becomes smaller when T is decreased. In particular, at $T < 120$°C, the humps are shifted out of the 10 year window, see Fig. 12.

Scenario B: Post-Stress Creation of Interface States

As an alternative explanation, or a process happening in parallel, the following scenario can be envisaged: during stress, the creation of interface states is triggered by the slow release of hydrogen via neutralization of trapped protons at the gate-side of the oxide. Once released, however, hydrogen will quickly react with either passivated interface states or defects inside the oxide, so the post-stress creation of the hump is unlikely due to "lingering" hydrogen that had already been released before the stress was terminated. However, during stress, hydrogen becomes trapped near the channel in a protonic configuration, which is used in the HR model to explain the build-up of the "permanent" component. When the bias is now switched to a recovery condition, these protons become neutralized and are slowly released again. Once released, these hydrogens can either go back to the gate area where they originate from (slow recovery of the "permanent" component) or depassivate dangling bonds at the interface, thereby degrading the device and contributing to the hump. Again, this process would be *reaction-limited* via the slow release of the now neutralized protons. Indeed, the observed temperature dependence of the maximum of the hump, $E_A \approx 1.8$ eV, is close to the mean energy barrier estimated for the release of protons in SiO_2, $E_A \approx 1.7$ eV [19].

V. Conclusions

We have investigated post-stress degradation build-up following NBTS. We could show that this effect can be clearly revealed at higher temperatures and longer stress times, while the stress voltage has to be kept low in order to minimize regular charge trapping in the oxide. The recently formulated H-release model can consistently explain the experimentally observed humps as either the net difference between positively and negatively charged defects close to the channel and gate, the post-stress creation of interface states by neutralized protons trapped during stress, or a detailed experiments are required to determine the precise microscopic origin of these humps. However, extrapolation of the available data to lower T seems to suggest that the observed irregularities during recovery are unlikely to interfere with conventional lifetime extraction methods. Nonetheless, they provide an important clue towards the microscopic origin of NBTI and must therefore be studied more closely.

Acknowledgments

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