ECS Transactions, 80 (1) 203-217 (2017)
10.1149/08001.0203ecst ©The Electrochemical Society

Impact of Gate Dielectrics on the Threshold Voltage in MoS_2 Transistors

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The electrical characteristics of field-effect transistors based on 2D materials such as MoS_2 strongly depend on defects in various regions of the device. Thus, an accurate description of charge transfer reactions with defects is essential as they have a strong impact on several important performance parameters. In particular, they disturb the electrostatic control of the gate over the channel, which is one of the central advantages of 2D devices in the ultimate scaling limit. As a consequence of charge trapping in these defects, large threshold voltage shifts are possible on short (hysteresis) and long (drift) timescales, which prohibit stable device operation. Here we introduce a drift-diffusion based simulation methodology coupled to a non-radiative multiphonon model to describe charge transfer reactions. Our results shed light on the interaction of defects with the 2D channel, which is important to enable further progress in the area of 2D based transistors.

Introduction

The two-dimensional (2D) material molybdenum disulfide (MoS_2) is currently the most famous member of the large group of transition metal dichalcogenides (TMDs). Because of their inherent and comparatively large transport band gap (E_G) and their heavy effective masses (m_{eff}), TMDs have received a lot of attention over the past few years (1). These properties together with the prospect of exploiting its ultimate thinness for the channel of MOS transistors could lead to perfect electrostatic control, high current on-/off- ratios, reduced source-drain tunneling and respectable mobilities of around $100\,cm^2/Vs$ (2–4). This renders MoS_2 an attractive candidate for applications in next-generation digital electronics.

Nevertheless, up to the present day the available prototype MoS_2 transistors suffer from a broad variety of barely understood issues. For example, the mechanism required to establish a good top contact is not yet understood, but essential for high on-currents. Additionally, the contacts govern the switching mechanism in MoS_2 transistors, thereby rendering them contact-dominated devices (5, 6). In addition, all currently available prototypes show an enormous variability in their characteristics. While in conventional silicon technologies parameters such as the charge carrier mobility or the doping density are well known, this is no longer the case for this novel technology, as due to their atomic thinness they are highly sensitive to the contacts and the surrounding materials and dielectrics. From a historical perspective this is reminiscent of the evolution of the silicon MOS transistor, which could only be realized in practice once the defect density at the Si/ SiO_2 interface could be reduced to acceptable levels ($< 10^{10} cm^{-3}$) using a forming gas anneal to eventually

replace the bipolar junction transistor as the dominant technology. However, contrary to the novel 2D technologies today, these issues were due to the unavoidable dangling bonds at the Si/ SiO_2 interface, which should ideally be absent in 2D materials (7). Conversely, all currently available 2D prototype transistors seem to be suffering from charge trapping in defects in the dielectric materials. Led by this consideration, we strongly believe that only a thorough understanding of the interaction of charge carriers with the surrounding dielectrics can pave the way for this device concept to industrial maturity.

In our previous works, we have systematically evaluated the hysteresis in the $I_D\,(V_G)$-characteristics of MoS_2 MOSFETs and analyzed the typically large drifts of the threshold voltage over time (8–10). These measurements build the foundation for the development of our physical modeling approach for studying the charging and discharging of defects in the surrounding layers. Our modeling approach sheds light on the impact of defects on device variability as well as on the commonly observed hysteresis and long-term threshold voltage drifts. In addition, we aim at clarifying the difference between the impact of interface traps and the impact of defects in the dielectrics on the transistor performance.

Modeling Framework

Our simulation methodology uses a drift-diffusion (DD) based TCAD model (11) which is computationally very efficient and to first-order sufficient for describing the charge transport through the channel of large-area MoS_2 transistors (12–14). To account for quantum confinement effects in the 2D material (approximate channel thickness $d \approx 0.65\,\text{nm}$), the density gradient equations must be used (15). Recently, several groups have developed drift-diffusion based compact models for field-effect transistors using 2D materials as a channel (16, 17). The DD equations are applicable if the lateral device dimensions are in the micrometer range, as this assures that there is a sufficient number of dopants or defects along the channel to make transport scattering-dominated and as such diffusive rather than ballistic.

On the other hand, in the ultimate scaling limit below 10 nm, carrier transport might become ballistic. Ballistic charge transport can be described by a variety of methods, including the non-equilibrium Green's function (NEGF) formalism (18) or the top of the barrier (TOB) model (19, 20). However, in their basic form these methods do not account for scattering events. The importance of scattering and thus the importance of using an efficient formalism which inherently takes these events into account is demonstrated in the comparison of Figure 1. Here the measurement data from a back-gated SL-MoS_2 transistor with dimensions in the µm range are compared with simulation data obtained from a DD simulation (11) and from a ballistic simulation using the TOB model (21, 22). As can be clearly seen, the TOB model overestimates the current through the device by several orders of magnitude.

The DD equations as a semi-classical description are based on a number of approximations, which require a handful of parameters. While in conventional silicon technologies knowledge of the mobility is typically sufficient for the description of MOS transistors, the large number of traps requires careful modeling of the recombination terms. Furthermore, the dielectric function of the materials can be highly sensitive to the selection of surrounding materials. The values and dependencies (for example on the temperature or the doping) of these parameters have been thoroughly studied for silicon, gallium-arsenide and other conventional three-dimensional (3D) semiconductors over the last decades but are only poorly known for 2D material systems.

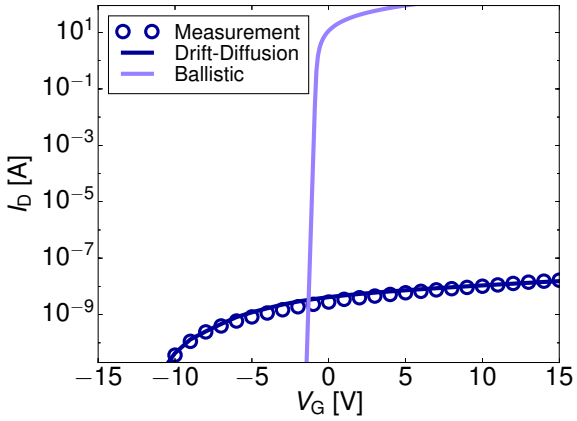


Figure 1: Comparison of drift-diffusion and ballistic simulations against experimental data for a prototype MoS_2 device.

Band Structure

One especially important material property from which several parameters are derived is the band structure. The band structure of SL-MoS_2 and other 2D materials has been studied in detail by the group of Thygesen (1, 23–27). They have shown that quantum confinement in the direction perpendicular to the plane leads to a weak and highly non-local dielectric function, which is responsible for many of the special properties found when studying the band structure of 2D materials (26). For 3D semiconductors the dielectric constant $\varepsilon(\omega)$ is defined as the limiting value of the dielectric function $\varepsilon(\mathbf{k},\omega)$ for vanishing momentum in $\mathbf{k}$-space. However, this definition cannot be extended in a straightforward manner to 2D semiconductors, as for an ideal 2D material it holds per definition that $\varepsilon(\mathbf{k}=0,\omega)=1$. Therefore, one has to use averaged values for DD simulations, which still vary strongly for in-plane and out-of-plane directions (28). This is one example for the high anisotropy which is observed in the material parameters of 2D materials.

In the DD model the highly complex band structure is typically approximated by two parabolas in the minimum and the maximum of the highest occupied band (the valence band) and the lowest unoccupied band (the conduction band). In SL-MoS_2 the minimum and the maximum are both located at the K-point, rendering this material a direct semiconductor, even though there is a transition to an indirect semiconductor if the number of layers is increased to two or more (29, 30). Particularly for the modeling of the recombination term, the band gap is of fundamental importance and is defined as the energetic distance between the conduction band edge and the valence band edge. However, over the past years there has been some confusion about the precise value of the band gap in SL-MoS_2, because several exotic effects have an impact on the band gap depending on the choice of experimental method. In particular, the obtained results for different methods vary quite substantially because in reality different properties are measured. As an example, the high free electron densities in the orbitals perpendicular to the 2D-plane which are not participating in any covalent bonds, lead to the existence of plasmons and strongly-bound excitons (31). The term plasmons refers to collective oscillations of the free electron gas, whereas excitons are quasi-particles consisting of an electron electrostatically bonded to a hole. For instance, conventional photoabsorption (PA) or photoluminescence (PL) measurements reveal only information about the so-called optical band gap ($E_{\text{opt.}}$) but not

Table 1: Comparison of literature values for the band gap of SL-MoS_2. In addition to the values for the electronic band gap, the values for the optical band gap ($E_{opt.}$) and the excitonic binding energy ($E_{exc.}$) are listed. The first section contains measured values and the second section DFT results. The measurement results are always smaller than the corresponding DFT results.

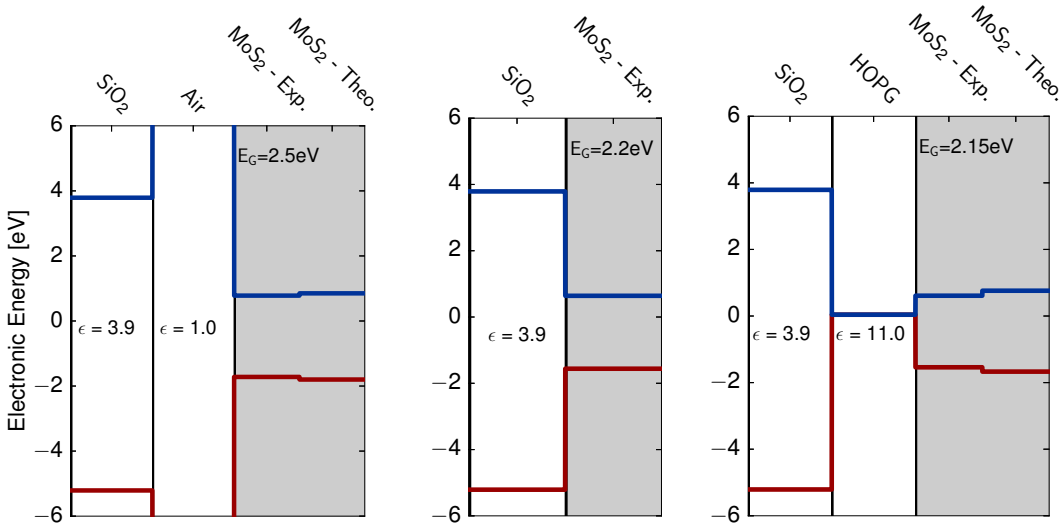
Substrate	Method	Band Gap	$E_{opt.}$	$E_{exc.}$	Reference
-	PS	2.5 eV	1.9 eV	0.6 eV	(35)
SiO_2	STS, PL, PA	2.1 ± 0.1 eV	1.85 ± 0.05 eV	0.2 ± 0.1 eV	(29, 32, 39, 40)
HOPG	STS, PL	2.15 ± 0.1 eV	1.93 eV	0.2 ± 0.1 eV	(33, 34)
-	PBE+GW_0	2.65 eV	-	-	(23)
-	LDA+G_1W_0	2.67 eV	2.04 eV	0.63 eV	(41)
-	LDA+G_0W_0	2.48 eV	2.01 eV	0.47 eV	(24)
Graphene	PBE+G_0W_0	2.43 eV	-	-	(25)

about the energy difference between the energy levels of free electrons and holes propagating across the 2D layer (29, 32). This energy difference, the electronic band gap, can be measured using for example scanning tunneling current spectroscopy (STS) or photocurrent spectroscopy (PS) (33–35). However, these experimental techniques suffer from the huge variability in the sample quality and from calibration problems. In any case, measurements can only provide a single value for the band gap at the K-point, whereas the full band structure can be calculated for instance using density functional theory (DFT). Within DFT an approximation for the exchange-correlation functional has to be adopted to approximately account for electron-electron interactions. As a well known problem, the simplest but still frequently used functionals (like LDA or PBE) massively underestimate the band gap for a broad range of semiconductors, including 2D semiconductors (36, 37). However, the single-particle DFT band structure is not supposed to be exact, even if it were calculated with the exact exchange-correlation functional. The so-called derivative discontinuity Δ_{xc} has to be calculated and added to the obtained single-particle band structure to obtain the correct band gap but most functionals incorrectly set this quantity to zero (1).

A different approach for calculating the band energies of a solid is the application of the Green's function theory to the self energy Σ instead of using an approximation for the exchange-correlation potential. The self energy is the local electrostatic potential, obtained by integrating over all electron coordinates and thus a very complex expression, which in a first-order approximation can be calculated as the product of the Coulomb interaction W and the single-particle Green's function G. These quantities are routinely calculated within the GW approximation (38). However, the quasi-particle energies calculated in this approximation strongly depend on the screened interaction and thus on the dielectric environment outside the 2D material. In consequence, the band gap of 2D materials depends on the choice of the substrate. This introduces a previously unknown tunability of the band gap via the choice of the gate dielectric. Also, large densities of charged defects in the channel's vicinity effectively change the band gap. It was shown that for 2D semiconductors with weaker intrinsic screening, like for example graphane (hydrogentated graphene), this effect is considerably stronger than for materials with a higher intrinsic electron density such as MoS_2 (27). As a result, the band gap of 2D dielectrics like hexagonal boron nitride (hBN) is the most adjustable compared to all other 2D materials.

In Table 1 the values reported in literature for the band gap of SL-MoS_2 are compared. In addition to the electronic band gap, also the values for the optical band gap and the excitonic binding energy are given. The measured electronic band gap, typically determined

via scanning-tunneling microscopy measurements, underestimates the value for the band gap in comparison to theoretical calculations. In Figure 2 the electronic band gaps, listed in Table 1, are displayed in a band diagram to further illustrate the impact of the substrate on the band gap of SL-MoS_2. The impact of the dielectric environment is the stronger, the higher the charge density in the vicinity of the 2D material is. Therefore, Figure 2(a) (a suspended MoS_2 sheet) and Figure 2(c) (MoS_2 on highly oriented pyrolytic graphite (HOPG), the bulk form of graphene) can be considered as limiting cases for the relevant case shown in Figure 2(b) (MoS_2 on SiO_2).



(a) (23, 24, 35, 41) (b) (39, 40) (c) (25, 33, 34)

Figure 2: Schematic drawing to demonstrate the impact of the dielectric environment on the band gap of SL-MoS_2. The band gap decreases if the dielectric screening in the environment is larger due to a higher density of free charges, therefore it is the largest in case 2(a) and smallest in case 2(c).

Another parameter which essentially determines the carrier mobility used in the DD model is the effective mass of the charge carriers, which is defined as the curvature in the energy minima of the band structure. For 2D materials the parabolic approximation of the band edges holds only under two conditions: Firstly, the dispersion at the band edges has to be quadratic, which is fulfilled for SL-MoS_2, but violated for graphene (13, 41). Secondly, this model neglects interband plasmons (bound states of electrons in different subbands of the conduction or valence band), which is justified as long as the focus lies on electric transport in the scattering regime and no optical interactions which could trigger interband transitions are considered (1).

Process-Related Material Parameters

Up to now, we have discussed material parameters which can be extracted from calculations of the band structure of SL-MoS_2. The remaining parameters, which are necessary for performing accurate DD-simulations (such as the mobility, the effective doping or the contact resistance), can be only measured. The main problem with these parameters is that they depend strongly on the details of the production process, like for example on the intrinsic defects in the MoS_2 monolayer resulting from the wet mechanical exfoliation process

or on the metals deposited on top of the 2D layer. This is why these parameters show enormous variations at the current level of technological maturity. As recent discoveries about a suitable establishment of good contacts or the benefits of encapsulation for SL-MoS_2 transistors have to be used as guidelines when it comes to choosing the correct values for these simulation parameters, we provide in the following a short literature review on the state of the art in the production process of SL-MoS_2 devices (42, 43).

In order to take advantage of the good transport properties of SL-MoS_2 by using it as the channel of a MOSFET, attention has to be paid to establishing good contacts to the channel as only good contacts can enable high saturation current levels. One criterion for a good contact is the choice of a suitable interface geometry. In the case of 2D materials one distinguishes in principle between top contacts, or more precisely laminar contacts, and edge contacts. In general it appears that the best contacts over which the highest possible current can flow are those with the largest area of covalent bonding of the metal to the 2D layer. In the case of SL-MoS_2, several metals have already been used to establish top contacts, however, their contact resistances are often enormous and the reported values vary considerably between different research groups (6).

For transistors based on SL-MoS_2, good contacts are not only important for achieving high current levels but also for the overall operation of the transistor itself, as these contacts typically act as Schottky barriers. As a consequence, the switching on of SL-MoS_2 FETs is not dominated by the accumulation of minority charge carriers in the ultimately thin channel below the gate in the inversion regime, as is the case for conventional MOSFETs based on 3D semiconductors. Rather, the large current on/off ratios of SL-MoS_2 transistors are caused by the electrostatic manipulation of the Fermi level in the channel and below the contacts where the Schottky barrier height is tuned (5). In the on-state of the device, the Schottky barriers become very thin and the short tunneling distance in monolayer MoS_2 channels gives rise to high tunneling currents (44, 45).

Apart from the contacts defining the saturation current levels and governing the switching process in MoS_2 transistors, they also determine the polarity of the devices. The contact deposition technique and the contact material determine whether the device behaves as an n- or pMOS. Mechanically exfoliated samples of SL-MoS_2 are usually intrinsically n-doped, presumably from adsorbed hydroxyl groups resulting from the wet transfer step of the MoS_2 sample to the oxidized silicon wafer serving as substrate and back-gate (46, 47). Thus for an n-doped layer, it is easier to turn the device on by applying a positive voltage, rather than by applying a negative voltage. Under these circumstances SL-MoS_2 transistors would behave as nMOS devices. In general it has to be noted, however, that in principle SL-MoS_2 FETs are ambipolar, only that the electric fields required to reach the p-conduction region can easily exceed the breakdown voltage of the gate dielectric. If, on the other hand, a different contact material is used, a SL-MoS_2 transistor could also operate in the pMOS regime (48). It has even been demonstrated by McDonnell *et al.* that the same flake of SL-MoS_2 can be operated in either the nMOS or the pMOS regime, depending on the contacts which are deposited on top (46).

During the last couple of years titanium (Ti) has been preferentially used as an adhesive layer for various contact metals as it apparently helps to establish high-quality covalently bonded top contacts to SL-MoS_2 (9, 10, 49). Even though it has been previously assumed that the titanium itself bonds covalently to SL-MoS_2 by changing the hybridization state of the sulphur atoms, it has only recently been shown by McDonnell *et al.* that the titanium rather serves as a getter material than as an adhesion layer (43). If the deposition of

Table 2: Simulation parameters used for DD based TCAD simulations of SL-MoS_2 transistors. The parameters in the first section are extracted from the band structure, the parameters in the second section depend strongly on the defects and thus on the processing conditions.

Parameter	Symbol	Value/Range	Reference
Dielectric constant	ε	5.5 ± 0.9	(26, 28)
Electronic band gap	E_G	$2.2 \pm 0.1\,\mathrm{eV}$	(1, 23–25, 39)
Electron affinity	χ	$-3.85 \pm 0.09\,\mathrm{eV}$	(1, 23–25, 53)
Electron mass	m_n^*	0.55 ± 0.05	(24, 54)
Hole mass	m_p^*	0.56 ± 0.05	(24, 54)
Contact resistance	R_C	$[10^3, 10^5]\,\Omega\,\mu\mathrm{m}$	(6, 50)
Work function diff. (Ti/TiO_2)/Au	E_W	$0.1 \pm 0.05\,\mathrm{eV}$	(6, 43)
Mobility	μ	$[0.1, 100]\,\mathrm{cm}^2/\mathrm{Vs}$	(4, 42, 45, 48, 49)
Effective Doping	N_D	$[10^{15}, 10^{17}]\,\mathrm{cm}^{-3}$	(47)
Interface trap density	D_{it}	$[10^{12}, 10^{13}]\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$	(47)

the contacts is conducted in high vacuum conditions (HV, $p \approx 1 \times 10^{-6}\,\mathrm{mbar}$) rather than in ultra-high vacuum (UHV, $p \approx 1 \times 10^{-9}\,\mathrm{mbar}$), the titanium forms a thin layer of TiO_2 on top of SL-MoS_2 by reacting with the hydroxyl molecules which had been previously adsorbed on the MoS_2 layer. If, on the other hand, the deposition is performed in UHV, the Ti forms Ti_xS_y which causes the contact resistance to rise (43). In general, the metals are deposited after annealing the sample at $T > 200\,^\circ\mathrm{C}$ for a few hours in vacuum, which causes the desorption of molecules from the crystalline surface (50). However, the electron affinity for Ti and TiO_2 is similar, leading to consistent values for the Schottky barrier heights measured, as long as one assumes Fermi level pinning due to the change in doping caused by the reaction at the contacts. English *et al.* reports record-low values for the contact resistances measured for pure gold (Au) contacts in UHV (50). Taking advantage of these improved contacts Smithe *et al.* fabricated MoS_2 MOSFETs with greatly improved properties, like for example saturation current levels on the order of 0.1 mA for widths in the µm range (42).

Even though it was previously reported that the Schottky barriers at the contacts mask the mobility in SL-MoS_2 transistors, the mobility can be extracted accurately by conducting four probe measurements (51). Also a reported dependency of the mobility on the gate dielectric turned out to originate from an incorrect treatment of the role of gate capacitances in the extraction of the mobility (52). In this way, the intrinsic mobility of encapsulated, high quality MoS_2 was measured to be around $100\,\mathrm{cm}^2/\mathrm{Vs}$, while the mobility of standard mechanically exfoliated MoS_2 is on the order of 1-50 $\mathrm{cm}^2/\mathrm{Vs}$ (4, 49). These values differ because of the varying number of scattering centers in the layer and the layer's vicinity.

Just like the mobility, the effective doping density also inherently depends on the defect concentration and is thus especially sensitive to the processing conditions. Even though in conventional silicon technologies the doping profile is well defined, at the current stage of research on 2D materials the samples are subjected to an effective doping via adsorbed molecules and impurities. Takenaka *et al.* extracted approximative values for the effective doping and the interface trap density by applying the Terman method to bulk MoS_2 samples on different gate dielectrics (47). In Table 2 the values of the most important material parameters for DD simulations of a SL-MoS_2 FET are summarized. The parameters are given for the special case of a back-gated transistor using SiO_2 as a gate dielectric and Ti/Au top contacts for source and drain electrodes.

Modeling Results

Modeling of Device Electrostatics

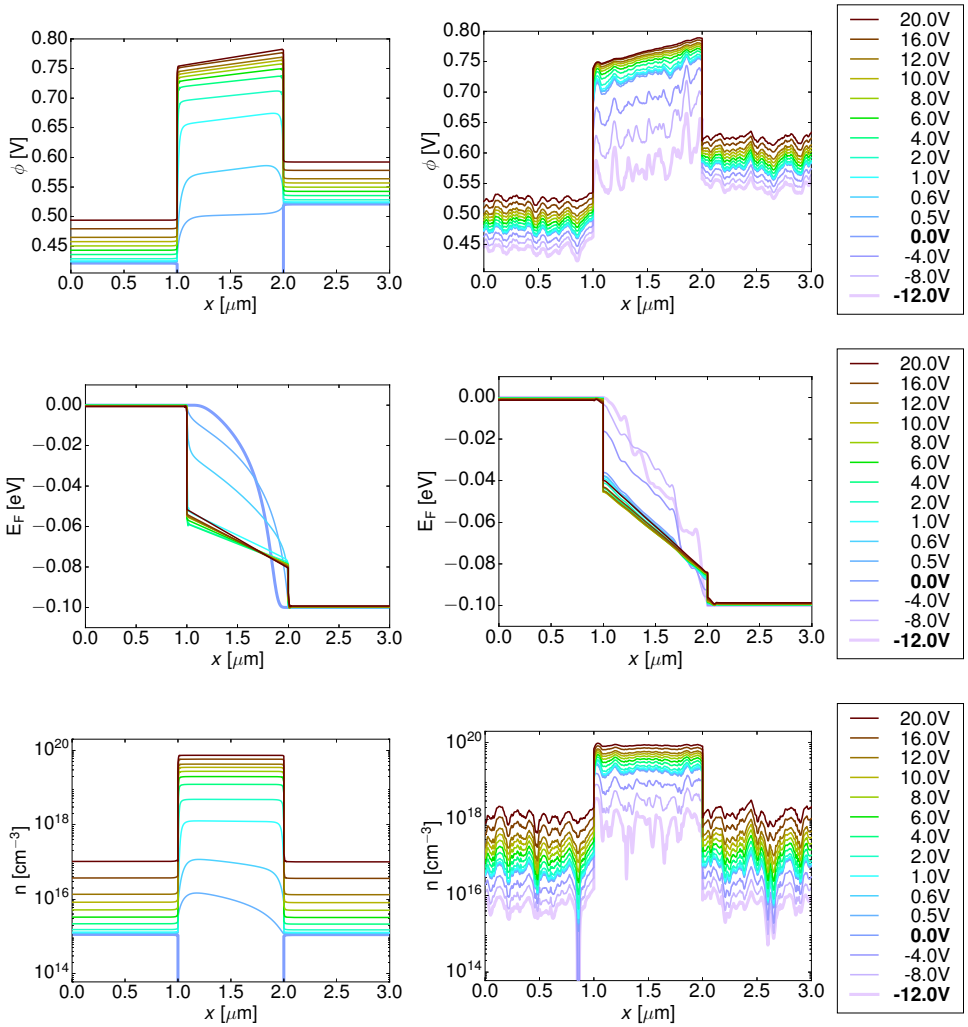
Due to the ultimate thinness of the channel in SL-MoS_2 transistors, the current flow through the channel is governed by the device electrostatics. From all the parameters discussed up to now, there are two parameters which are determined by the defects in the semiconductor, namely the mobility and the doping. In our simulations the mobility of the charge carriers is assumed to be controlled by the large number of defects and we suppose a weak unintentional *n*-doping of the layer. A device in which the impact of the defects beyond this level is neglected will be termed "ideal" in the following.

For the current flow through the channel of SL-MoS_2 transistors only the majority carriers, in this example electrons, are important. By way of analogy, the description of a pMOS device, realized by a different contact material or contact deposition method, would proceed along similar lines. The electrostatics of back-gated SL-MoS_2 transistors are illustrated in Figure 3. The variation of the potential (ϕ), the location of the quasi-Fermi level for electrons (E_F) and the electron concentration (n) in the channel is shown, with different back-gate voltages as a parameter. The left column (Figure 3(a)) displays these quantities for an ideal device. In this case the current suddenly drops at $V_G = 0\,V$, as the electron concentration reaches a minimum in between the source and drain contacts. At this voltage level the gate can no longer cause the injection of charges over the Schottky barriers at the contacts and the resulting lack of charges causes a feedback effect, which increases the barrier height for electrons in the channel even more. This feedback loop is commonly termed electrostatic doping. The sudden lack of this electrostatic doping turns the transistor at $V_G = 0\,V$ into a resistor with very high resistance.

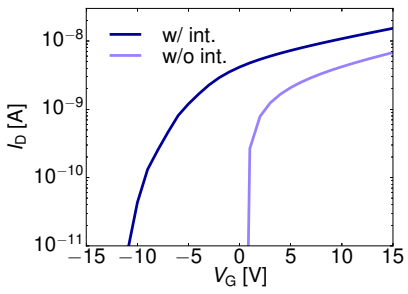
However, the large sensitivity of 2D devices to charged defects can be clearly seen from the comparison of the plots in the left column with the plots in the right column (Figure 3(b)). The electron concentration fluctuates over several orders of magnitude whenever a charged defect is located nearby. At the same time the charged defects shift the threshold voltage and the charge weakens the control of the gate and leads to an increased subthreshold slope. This is a first example of how important the correct description of defects in the surrounding dielectrics is for the accurate modeling of 2D devices and will be discussed in more detail in the next section.

Modeling of Defects

When describing defects in a FET, one usually distinguishes between interface defects, which are located directly at the boundary of the semiconductor to the gate dielectric, and oxide defects, which are inside the dielectric. The most relevant oxide defects lie within a distance of a few nanometers to the channel (55). Here, two models for describing the charging and discharging of these two defect classes are briefly introduced and then used to discuss the different impact of these defects on the threshold voltage of SL-MoS_2 transistors.



(a) ideal device (b) with interface defects



(c) $I_\mathrm{D}\,(V_\mathrm{G})$

Figure 3: Comparison of the simulated potential, Fermi level and electron concentration plotted along the channel with and without considering interface defects in the model. In addition, the $I_\mathrm{D}\,(V_\mathrm{G})$ characteristic is displayed for both cases. The channel of the simulated device is 1 µm long. It has the same length as the source and drain contacts. A constant voltage of $V_\mathrm{D} = -0.1\,\mathrm{V}$ is applied at the drain, the source contact is grounded and the gate voltage varies according to the color scheme given on the right. The gate voltages, where the gate loses control over the channel ($V_\mathrm{G} = 0\,\mathrm{V}/-12\,\mathrm{V}$ for left/ right column), are shown in bold style.

Interface Defects are usually described using the Shockley-Read-Hall (SRH) model, where the defects are modeled as trap levels in the band gap which serve as recombination centers for charge carriers (56). In addition, whenever charged, they disturb the electrostatics of the transistor. Due to the particularly high free electron densities which can be attained in 2D materials, recombination is less important than in silicon techonolgies. The electrostatic doping by the defects is essential, as the current flows right at the interface. If the defect is positively charged in the unoccupied state and neutral in the occupied state, it is termed a donor-like trap or a hole trap, while if it is negatively charged in the occupied state and neutral in the unoccupied state, it is an acceptor-like trap or an electron trap. In the case of an nMOS device, the donor-like traps at the interface become charged one after the other as the gate voltage decreases, thus leading to a smaller sub-threshold slope and at the same time to a shift of the threshold voltage towards more negative voltages. This is why the fluctuations in Figure 3(b) become more pronounced at negative gate voltages. The additional charges due to interface defects change the electrostatics of the device to such an extent that they even increase the saturation current level $I_{\mathrm{D,sat}}$.

Oxide Defects are in our work described using the more complex but from a physical point of view more accurate non-radiative multiphonon (NMP) model (57–61). The NMP model considers not only the energy balance of the transferred electron but also the energetic relaxation of the structure surrounding the defect (62). This makes it possible to explain the wide distribution of time constants which is observed in long-term stress measurements on Si/SiO_2 based devices (63). In this representation the charge transfer process is triggered by a change of the potential energy due to the applied gate voltage, which modifies the local potential around the defect in such a way that the electron can overcome the barriers and the microscopic bonding structure of the amorphous SiO_2 changes. However, for macroscopic devices with dimensions in the µm range, like the SL-MoS_2 transistors discussed here, the impact of these microscopic processes on the device characteristics becomes visible if there are many defects with similar properties distributed across the whole device area. In general, it is assumed that there are a few atomistic configurations, which are common to all industrially grown SiO_2, where electrons can easily be incorporated or emitted from the SiO_2 layer (64, 65). As these configurations are a material property of the gate oxide, the parameters extracted on Si/SiO_2 devices can be used as well in this context, as the change in the channel material used does not have any impact on the defect bands in the gate dielectrics.

To the present day, there are two known defect bands in SiO_2. The lower defect band is located at approximately $E_{\mathrm{T}}^{\mathrm{L}} = 4.6 \pm 0.3\,\mathrm{eV}$ below the conduction band edge of SiO_2 (66). Since this defect band is situated close to the valence band of Si, it causes the prominent negative bias-temperature instabilities (NBTI) in Si technologies (63) but its location in the middle of the band gap of SL-MoS_2 renders it unimportant for describing the degradation of devices based on MoS_2. The upper defect band, on the other hand, is located at approximately $E_{\mathrm{T}}^{\mathrm{U}} = 2.6 \pm 0.4\,\mathrm{eV}$ below the conduction band edge of SiO_2 (67, 68). Conventionally, the upper defect band is assumed to be acceptor-like and the lower defect band to be donor-like, leading to no threshold voltage shifts due to oxide charges, if the Fermi level is confined in between these two defect bands. Conversely, the upper defect band lies close to the conduction band edge of MoS_2 and also of monolayer black phosphorus, thus governing the degradation in many 2D based devices. (8–10).

Based on our previous results, it appears that the oxide defects in the dielectric layers surrounding the 2D material are at the same time responsible for the hysteresis and for the observed long-term degradation, commonly qualified via bias-temperature instability measurements (BTI). Both the hysteresis and the BTI shifts measured on 2D transistors are currently still several orders of magnitude larger than the typical shifts in standard Si technology. A systematic evaluation of the hysteresis, being in principle a threshold voltage shift in between the up-sweep and the down-sweep of an $I_D\,(V_G)$ measurement, and the BTI data offer two different views on the same phenomenon. While a hysteresis measurement reveals information on the bias dependency of the respective traps, a BTI measurement covers several orders of magnitude on the time scale, but stresses the device only with one discrete voltage level. The fact that oxide defects are situated a few nanometers away from the interface gives rise to two phenomena, both being strong arguments in favor of oxide defects causing the hysteresis and the BTI. First of all the bias dependency of oxide defects is larger than the bias dependency of interface defects, as the potential gradient in the oxide changes the potential energy surface in the defect's vicinity and at the same time shifts the defect level. Secondly, oxide defects show a much broader distribution of time constants in comparison to interface defects (62).

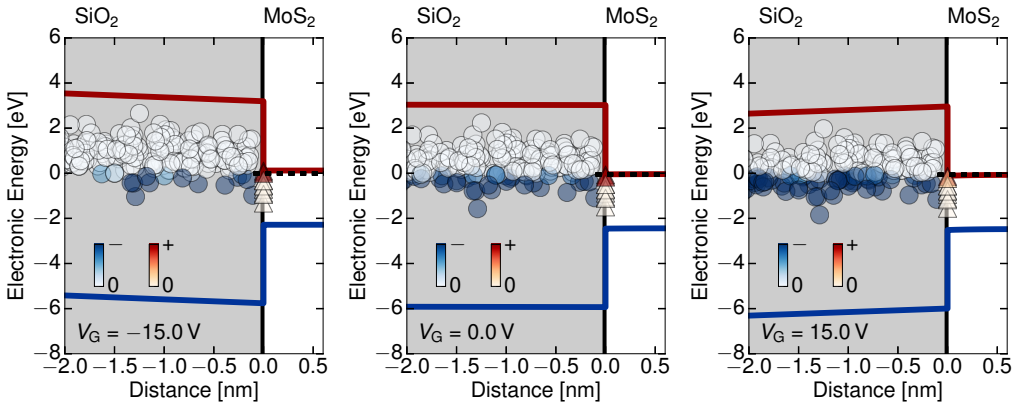
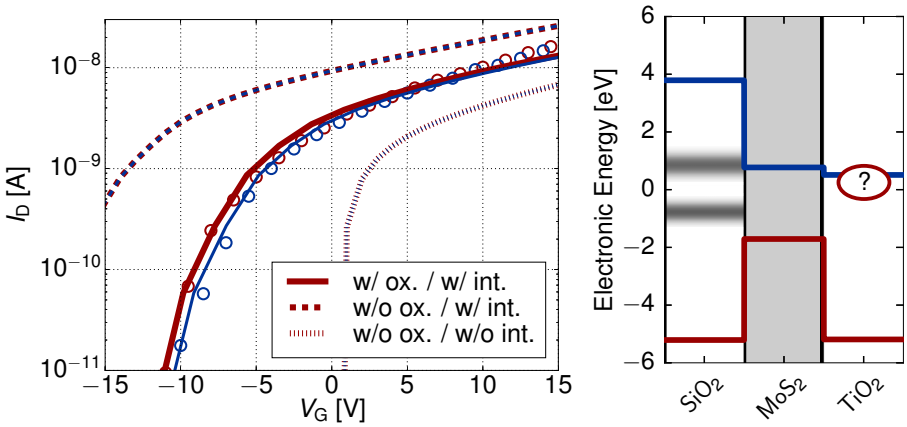


Figure 4: The charging and discharging of oxide defects (circles) and interface defects (triangles) is illustrated for a back-gated SL-MoS_2 FET.

Figure 4 illustrates the shifting of oxide traps due to the applied gate voltage and the charging and discharging of interface and oxide defects. In Figure 4 one can see that for negative gate voltages more interface defects become positively charged, while at the same time more oxide defects emit electrons, thus reducing the amount of negative oxide charges. At positive gate voltages the process is inverted. All defects which change their charge state in between the negative and the neutral gate voltage or the positive and the neutral gate voltage can in principle contribute to BTI. Whether a defect contributes in reality, depends on the measurement window and on the time constant of the defect itself. In the case of a hysteresis measurement only those defects contribute to the observed hysteresis width, which capture an electron at the high level of the gate voltage and emit this electron only after reaching the low level of the gate voltage. From these considerations one can conclude that a hysteresis measurement sums up the threshold voltage shifts of the traps over a small window in the time domain and a large window in the voltage domain, whereas a BTI measurement sums up the threshold voltage shifts over a large window in the time domain at one discrete stress voltage.

In Figure 5(a) the impact of oxide traps and interface defects on the $I_D(V_G)$- characteristic of a back-gated SL-MoS_2 FET is illustrated. The interface defects increase the sub-threshold slope and the saturation current level. The additional charges due to positively charged donorlike interface defects shift the threshold voltage to negative voltages. This shift is partially compensated by the negative charges originating from charged oxide defects in the acceptorlike upper defect band of SiO_2. As already stated, only the oxide defects can describe the large bias dependency and broad distribution of time constants observed in hysteresis or BTI measurements, while interface defects change the shape of the transfer characteristic. Regardless of that, every charged defect shifts the transfer characteristic.



(a) $I_D(V_G)$ (b) Defect bands

Figure 5: Comparison of simulated $I_D(V_G)$- characteristics with and without interface defects and with and without oxide defects. The circles represent measurement points, the red lines show the up-sweep ($V_G = -15\,V \rightarrow 15\,V$), the blue lines show the down-sweep ($V_G = 15\,V \rightarrow -15\,V$). The defect bands in the surrounding dielectrics are displayed on the right.

Figure 5(b) shows the defect bands in the dielectrics surrounding the SL-MoS_2 channel. The dark gray shaded areas are the two known defect bands of SiO_2, which have been used for the simulations of hysteresis and BTI on SL-MoS_2 devices up to now. Nevertheless, one has to be aware that it is likely that the TiO_2, which forms during the deposition of Ti/Au contacts under HV conditions, contains defects as well and thus defect bands. What is more, as the growth of this thin amorphous layer is not controlled, the defect density is assumed to be comparatively high. In this figure the band alignment for a crystalline monolayer of 1T-TiO_2 is shown, even though the specific band alignment together with the defect band of this amorphous TiO_2 is still unknown (24).

Conclusions

At the current stage of technology, the impact of defects on 2D based devices is more prominent and more important than for silicon technologies. Without a thorough understanding of the charge exchange processes with defects at the interface and in the surrounding dielectrics, the modeling of the most basic device characteristics is impossible. In this work we focus on MoS_2 transistors, whose switching mechanism is based on the

good electrostatic control over the channel due to the ultimate thinness of the layer. However, the electrostatics of 2D devices are strongly influenced by defects at the interface. Apart from that, stable device operation of 2D based transistors is currently inhibited by the observed large drifts of the threshold voltage. These drifts are caused by defects in the gate dielectric and in the dielectric layers used to establish good contacts to SL-MoS_2. In order to mitigate the problem of the drifts one should switch to a better suited process for contact deposition as well as focusing on reducing the defect densities in the defect bands of the gate dielectrics as much as possible, maybe by using 2D materials such as hBN.

Acknowledgements

The authors gratefully acknowledge financial support through FWF grant n° I2606-N30 (RELTMD). GTS (Global TCAD Solutions) is acknowledged for support and we gratefully acknowledge inspiring discussions with Gianluca Fiori (Universtiy of Pisa) and Mario Lanza (Suzhou University).

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