hardware synaptic resource to existing digital computing platforms. Like the transistor, multiple levels of computational abstraction can be defined on top of kT-RAM's synaptic primitive. To explore these levels of abstraction we have created the KnowmAPI, collection of Java code modules built on top of a kT-RAM emulator with interchangeable cores.

In this talk Alex will present a series of useful computational abstraction layers from low level synaptic hardware primitives to compositional (deep) supervised and unsupervised machine learning functions.

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B04: MTJs - Spin-Based Binary Memristors for Non-Volatile Memory and Logic Applications

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The use of memristive devices for new computational architectures enables the application of the same device as memory (latches) and logic (gates) [1]. Due to this unique combination of logic and memory within each element these architectures are called stateful [1]. The stateful logic is hence conceptually different from a conventional logic-in-memory architecture [2], where constituting elements are still clearly divided in logic and memory by their functionalities. Therefore, the memristive-based architectures, promising significant enhancements over existing computational resources, open at the same time new computational paradigms leading to increased energy efficient computations and reduced costs.

The realization of a material implication (IMP) gate based on two TiO_2 memristive switches and a conventional resistor [1] stimulated further development of memristive circuits by establishing a general methodology suitable for the design of integrated circuits based on a memristor-based crossbar architecture with a particular focus on an IMP-based eight-bit full adder [3].

A memristive device can also be based on a magnetic tunnel junction (MTJ) switched by spin transfer torque (STT) [4], which is operated in its binary mode, employing high/low resistance states as the bit storage in emerging non-volatile magnetoresistive random-access memory [5]. Since memristors are also employed in their binary mode in TiO_2-based IMP gates [1], it is attractive to replace them with MTJs [6] characterized by the two distinct and stable high/low resistance states [6]. However, a direct replacement of memristors by MTJs in the IMP gate [1] hampers the gate operation [6] due to the low high/low resistance ratio and thus weakens the state-dependent resistance modulation. A new IMP gate topology with an additional resistor in the source shoulder significantly reduces the gate operation errors and reduces the energy consumption per operation [7]. This so-called asymmetric IMP gate is conveniently realized in a 1Transistor(T)/1MTJ memory array by utilizing the access transistor as a nonlinear resistor [8]. By using only six of 1T/1MTJ cells a full adder is realized [9].

To extend the use of non-volatility for computations and to enable a higher integration density, it is desirable to omit circuitries needed for communication between the charge-based

CMOS and the spintronic parts and shift computations as much as possible from the CMOS domain to the spintronic domain [10]. To that end, we proposed a compact magnetic flip-flop employing two MTJs with a common recording layer [11]. The flip-flop performs the computations in the magnetic domain via the STT and the exchange coupling. By complementing the flip-flops with non-volatile magnetic shift registers [12] and majority gates [13], a very compact universal non-volatile processing environment is envisioned [14].

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B05: Resistive switching in planar metal/metal-oxide bilayer system with low voltage operation

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Development of nano-scale non-volatile memory device is an important milestone for next-generation nano-electronics. Although many devices with different operation principles have been demonstrated, each memory device have both advantage and disadvantage. Resistive switching and phase-change memories based on the phase transition are the promising candidates because of their simple device structures with the high compatibility of the present CMOS technology. Recently, we have developed a laterally configured resistive switching device based on a nanogap electrode[1]. This device configuration has greater advantage for the flexibility of the device geometry than the vertical device. However, the operation voltage is higher than the conventional vertical device. Here, we propose and demonstrate new memory device combining the PRAM and ReRAM technology.

Figure 1 shows a SEM image of our developed resistive-switching device based on an amorphous metal/metal oxide bi-layer together with its schematic illustration. As shown in Fig.2, the high resistive area, which is formed by passing the high-density current in a nano constriction of the amorphous metallic wire, enables to induce the resistive switching of NiO with the low operation voltage. This novel-style operation combining the resistive and phase-change memories will provide the great endurance and reliability with variety of material