Title: Spin-Based Non-Volatile Memory and Logic in Modern Nanoelectronics

Viktor Sverdlov[1], Josef Weinbub[2], and Dr. Siegfried Selberherr[1]*
Professor
1. Institute for Microelectronics, TU Wien, Austria
2. Christian Doppler Laboratory for High Performance TCAD, Institute for Microelectronics, TU Wien, Austria

Abstract

The current age of Big Data requires an unprecedented level of data storage capacity complemented by efficient processing capabilities. The major limitations of current datacenters arethe costly transfer of data between memoriesand processors as well as the increasing stand-by power. An efficient solution to this problem is to perform data processing close to the memory and to add non-volatility to the circuits.
Non-volatility can be added into the established complementary metal-oxide-semiconductor technology by introducing ferromagnetic source and drain electrodes, which allows employing another intrinsic characteristic of an electron, the spin, to enhance the functionality of electronic devices. However, in contrast to charge the injected excess spin is relaxing to its equilibrium zero value within a certain time, the spin lifetime, while diffusing along the channel. The general behavior of the spin lifetime in thin silicon films shows a two times lifetime enhancement for in-plane injection as compared to an orthogonalinjection. A further increase of the spin lifetime is predicted in tensely uniaxially stressed silicon films. Therefore, mechanical stress routinely applied to enhance the electron mobility can also be used to boost the electron spin lifetime. However, the weak spin-orbit interaction in the conduction band of silicon makes the realization of efficient silicon-based spin field-effect-transistors - a theoretically predicted attractive device - improbable in the near future. On the contrary, an efficient coupling between the electric and the magnetic degrees of freedom isachieved in magnetic tunnel junctions (MTJs) at the quantum-mechanical level. With the first magnetoresistiverandom-access memory (MRAM) arrays already commercially available for stand-alone applications, spin-transfer torque (STT)-MRAM becomes a viable candidate for future non-volatile applications in embedded dynamic RAM and last-level cache memories. Currently, the reduction of the switching current, while preserving the high thermal stability, as well as the MTJ tunnel dielectric reliability are the main challenges in the field. STT-MRAM enables also an intrinsic logic-in-memory architecture, where the same elements are employed to store and to process information. Another option is to design a non-volatile processing environment based on a STT majority gate used as a processing unit complimented by a non-volatile flip-flop (Novoflop), which is realized by three magnetic stacks sharing a common free magnetic layer. The information is stored in the magnetic orientation of the free layer. This extremely compact Novoflop is envisioned to serve as cache memory, i.e., to store the data from and for the processing unit.

Biography

Professor Dr. Siegfried Selberherr is the Chair Professor of the Institute for Microelectronics at the Technical University in Wien, Austria. He has been an IEEE Fellow and Distinguished Lecturer of the IEEE Electron Devices Society since 1993 and 1996, respectively. From 1998 to 2005 he served as Dean of the Faculty of Electrical Engineering and Information Technology. His current research topics are modeling and simulation of problems for microelectronics engineering.

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