

Modeling Electromigration in Nanoscaled Copper Interconnects

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Abstract—In this work we present an approach to modeling grain boundaries and material interfaces in nanoscaled copper interconnects. Using a sample structure with a $40\text{nm} \times 40\text{nm}$ cross section and an applied current density of $1\text{MA}/\text{cm}^2$, we perform a comparative analysis while ignoring or including grains, with an average grain size of 50nm . The novelty in our approach is the treatment of microstructure interfaces using a binary parameter, which is further used to define interface-specific material properties for copper resistivity and electromigration modeling. Our models show that the inclusion of microstructure effects results in an increased resistance, increased vacancy migration, and ultimately in a higher EM-induced stress.

I. INTRODUCTION

Electromigration (EM) is one of the major reliability concerns in modern integrated circuits. EM degradation results in chip failure due to the formation of voids under induced stresses, which grow to cause an increase in the line resistivity and ultimately in an open circuit failure [1].

One of the major challenges in continuing along the More Moore scaling path lies in the fabrication of reliable scaled interconnects. Ultrascaled nano-interconnects will have to include the use of novel materials, processes, tools, and designs, while copper-based metalization will continue to be relevant for nanotechnology nodes down to at least 7nm [2]. The copper (Cu) behavior at the nanoscale is very different from that observed in bulk material, especially, when it comes to its resistivity and reliability. Experiments have shown that the lifetime of Cu interconnects has decreased at every technology node by about one half, even at the same current density [3].

An increasing influence of grain boundaries (GBs) and material interfaces (MIs) has been shown to be the core reason for the increase in EM effects [4][5]. If one only considers these influences on the Cu resistivity, a drastic change in the interconnect behavior can be observed, as depicted in Fig. 1. There, we also show the technology nodes in terms of interconnect half-pitch from major industrial manufacturers [2].

Current state-of-the-art models and simulators of interconnect EM reliability cannot appropriately take into consideration the complex Cu microstructure and are therefore not able to address EM interconnect failure at advanced nodes. In addition to their influence on resistivity, GBs and MIs act as fast diffusivity pathways for vacancies as well as vacancy generation and annihilation sites. Previous attempts to include this microstructure in EM simulations relied on introducing GBs as a thin layer, requiring a very fine mesh, limiting the

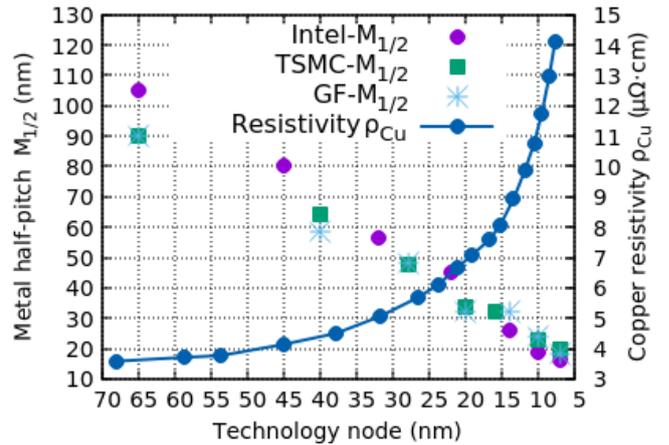


Fig. 1. Effective Cu interconnect resistivity and expected resistivity at future nodes as a function of the technology node obtained from [6]. The increasing resistivity from the bulk value of $2.5\mu\Omega \cdot \text{cm}$ is due to the increased influence of GB and MI scattering. In addition, the metal half-pitch for the technology nodes from Intel, TSMC, and Global Foundries (GF) are shown.

simulation to two dimensions, and restricting the geometry to simple grain structures [7]. In this work we present a novel EM modeling strategy which treats boundaries and interfaces as a material parameter, which further influences parameters of local resistivity, vacancy diffusivity, vacancy diffusion activation energy, and effective valence. This method allows to model the EM behavior for realistic three-dimensional nanoscaled interconnect Cu lines.

II. COPPER RESISTIVITY

When considering the resistivity of a metal line, three main components must be included:

- 1) Intrinsic resistivity of the bulk material, limited only by the electron mean-free-path (MFP),
- 2) the increase in resistivity due to surface scattering including MI, and
- 3) the increase in resistivity due to metal GB scattering.

The effects of the granular microstructure, surface scattering on MI, and cross-sectional area of a Cu interconnect on its resistivity ρ_f is modeled by [8]:

$$\frac{\rho_f}{\rho_i} = 1 + \frac{3\lambda}{4w} (1-p) + \frac{3\lambda}{2D} \left(\frac{R}{1-R} \right) \quad (1)$$

ρ_i is the bulk resistivity, λ is the electron MFP, w is the metal width, p is the probability of electron reflection from a MI, D is the average grain size, and R is the probability of electron reflection from a GB. Once we know the distance from the grain boundary from every point inside the individual metal grains, we can calculate the GB- and MI-dependent local resistivity ρ inside the Cu line. The added temperature influence on the resistivity is calculated by

$$\rho = \rho_f (1 + \alpha_{e0} (T - T_{ref})), \quad (2)$$

where T is the temperature, T_{ref} is the reference (room) temperature, and $\alpha_e = 0.0043K^{-1}$ is the temperature-dependence factor for Cu resistivity.

The stochastic polycrystalline structure of the metal line is modeled based on the following: A specified average grain diameter and average grain volume is calculated, assuming spherical grains. The volume to be filled by the grain pattern is divided by this average volume to give the expected number of grains. An actual number of grains is then picked randomly from a Poisson distribution with the mean equal to the expected number of grains. For each grain a seed point is placed randomly within the volume to be filled by the grain pattern. A three-dimensional Voronoi tessellation is generated based on the seed points by associating each node in the simulation mesh with the nearest seed point and thereby assigning it to the grain defined by that seed point. This technique is applied to a simple damascene structure with an average grain size of 50nm, resulting in the geometry shown in Fig. 2.

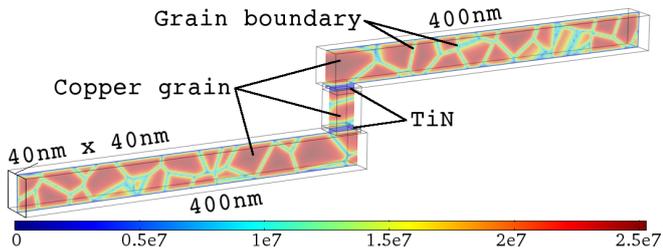


Fig. 2. Conductivity (S/m) inside the Cu interconnect layers.

It may be worth noting that a further reduction in the Cu dimensions may lead to a more columnar grain microstructure [9]. The model we present here can be inherently expanded to include these types of structures.

III. ELECTROMIGRATION

The model used to calculate the vacancy dynamics and EM-induced stress through the interconnect is described in [1]. The EM-induced failure proceeds in two stages. (1) The electric field causes the gradual movement of ions, which form a hillock on one end of the interconnect and a vacancy on the other. This vacancy generation results in a build-up of stress in the metal line. (2) The stress may cause a crack, resulting in immediate failure. Alternatively it may reach a critical stress level to nucleate a void, which continues to be affected by EM and grows slowly, eventually causing an open circuit failure.

A. Transport of vacancies

The total flux of vacancies is given by

$$\vec{J}_v = -D_v \left[\nabla C_v + C_v \left(\frac{eZ^*}{kT} \rho \vec{j} - \frac{Q^*}{kT^2} \nabla T + \frac{f\Omega}{kT} \nabla \sigma \right) \right], \quad (3)$$

with D_v the vacancy diffusivity, C_v the vacancy concentration, e the elementary charge, Z^* the effective charge, \vec{j} the current density, Q^* the heat of transport, f the vacancy relaxation ration, Ω the atomic volume, and σ the hydrostatic stress. The accumulation and depletion of vacancies is found according to the continuity equation

$$\frac{\partial C_v}{\partial t} = -\nabla \cdot \vec{J}_v + G, \quad (4)$$

where G is a surface function which models vacancy generation/annihilation, taking place only at GBs and MIs. Due to the difficulties in modeling G this term is frequently approximated and applied to the entire Cu line [10]. However, using the presented method the generation/annihilation term can easily be applied only at the GBs and MIs using

$$G = \frac{\partial C_{v,T}}{\partial t} = \frac{1}{\tau} \left[C_{v,eq} - C_{v,T} \left(1 + \frac{\omega_R}{\omega_T C_v} \right) \right], \quad (5)$$

where $C_{v,T}$ and $C_{v,eq}$ are the trapped and equilibrium vacancy concentrations, respectively, τ is the relaxation time, and ω_R and ω_T are the vacancy release and trapping rates, respectively. The strain caused by the moving atoms results in a tensile stress build-up at locations of high vacancy accumulation and a compressive stress at hillock accumulation.

B. Vacancy-induced strain

Due to the migration of vacancies and their generation/annihilation strain builds up in the bulk copper and at the GBs, respectively. The directional components (i, j) of the vacancy migration-induced strain rate ϵ_{ij}^m are given by

$$\frac{\partial \epsilon_{ij}^m}{\partial t} = \left[\frac{1}{3} (1 - f) \Omega \nabla \cdot \vec{J}_v \right], \quad (6)$$

while the directional components of the vacancy generation/annihilation-induced strain rate ϵ_{ij}^{ga} are described by

$$\frac{\partial \epsilon_{ij}^{ga}}{\partial t} = \left[\frac{1}{3} f \Omega G \right]. \quad (7)$$

The strain results in a stress build-up in the copper line, leading to void nucleation or cracking and eventual failure.

IV. MICROSTRUCTURE MODEL

The resistivity (or conductivity) of nanoscaled Cu interconnects cannot be treated as a bulk material property, but rather it must include the influence of the microstructure [6]. Since resistivity plays a significant role in vacancy migration, treating this material parameter properly is essential in EM modeling. In fact, since about the 65nm node, the GB has played an increasing role in determining the lifetime of copper interconnects, as shown in Fig. 3 [3]. For the structure we are

modeling, we note a lifetime reduction of about 5.72 times, when the GB effect is considered.

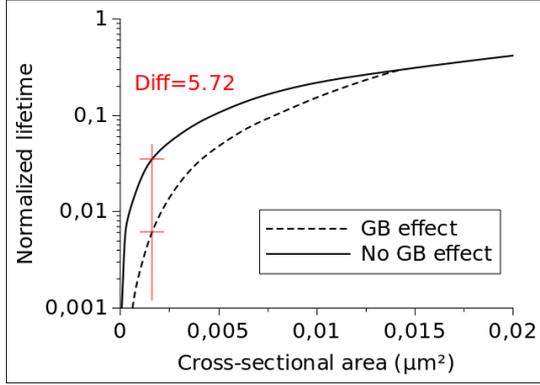


Fig. 3. Normalized EM median lifetime versus cross-sectional area of Cu interconnects showing the influence of GBs [3].

Although the microstructure has been included in previous EM studies, the principal novelty in our approach is how we define and treat it. Previous attempts have required a refined mesh at the GBs and MIs with additional refinement necessary for triple points, where two grains and a metal barrier layer intersect [11]. The use of this approach to model Cu interconnects showed the importance of treating GBs and MIs. However, due to the mesh refinement necessary it quickly becomes computationally and memory-wise expensive to perform these calculations on complex geometries.

Our EM model treats the GB and MI as a material parameter with the binary value **1** at these interfaces and a value of **0** inside the grain. This allows to further calculate the resistivity distribution in the Cu line locally in the entire structure, with the effects of GB and MI scattering as well as temperature included therein. The resistivity distribution is found by applying (1) and (2).

Our sample interconnect structure has cross-sectional dimensions of $40\text{nm} \times 40\text{nm}$ and an average grain size of 50nm . With this geometry we perform EM simulations, including the special treatment of GBs and MIs with different Z^* and D_v values, as shown in Fig. 4.

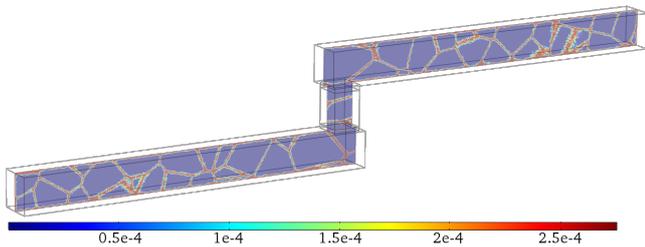


Fig. 4. Vacancy diffusion coefficient D_v (cm^2/s) in the Cu metal lines. The GBs and MIs influence on the vacancy diffusion is evident.

V. SIMULATIONS AND DISCUSSION

A current density of $1\text{MA}/\text{cm}^2$ is applied to the test structure at the bottom left end of the interconnect. The resulting current

density distribution through the bottom Cu line from Fig. 2 is shown in Fig. 5. When the microstructure is ignored, the maximum current density in the bottom Cu line away from the vertical via remains $1\text{MA}/\text{cm}^2$, while it increases to about $1.5\text{MA}/\text{cm}^2$ inside the grains, when GBs and MIs are properly included. The influence of the GB structure is immediately evident.

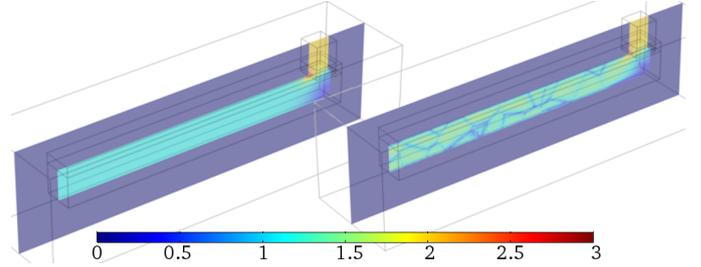


Fig. 5. The current density (MA/cm^2) through the bottom line of the Cu interconnect shown in Fig. 2 and calculated during the EM simulation.

A. Electromigration

At the onset of EM, the resistivity and current density terms from (3) have the highest influence, as can be seen in the result of the simulation for the normalized vacancy concentration after 0.1ms of operation, cf. Fig. 6. Here it is clear that, when GBs are present, the vacancies accumulate throughout the structure at a level 15 times higher than without GBs. When GBs are ignored, the accumulation is also noticeable at one end of the line, directly at the interface with the metal barrier layer.

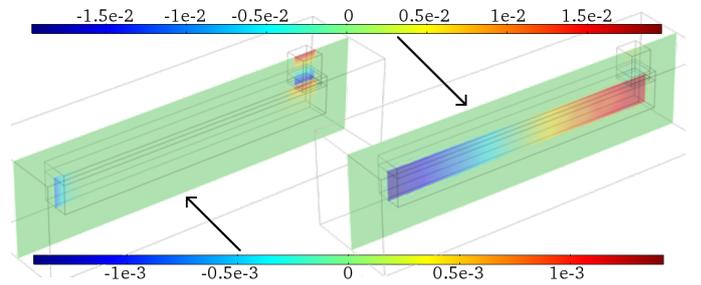


Fig. 6. The normalized vacancy concentration ($C_V/C_{V0} - 1$) is shown at the onset of EM, after 0.1ms at 300°C at a current density shown in Fig. 5 using a (left) bulk Cu material and (right) the grain structure from Fig. 2.

We note in Fig. 7 that the non-granular Cu line reaches a steady state, where the back flux evens out the EM term, after about 0.1s of operation. We can conclude that by ignoring the grain structure, the vacancy concentration change is significantly underestimated. In Fig. 8 we observe the vacancy concentration inside the Cu line after 0.01ms , where the effect of the GB and MI on the vacancy dynamics is highly pronounced. The GBs and MIs are clearly the principal vacancy diffusion pathways.

B. Stress

In Fig. 9 we observe the hydrostatic stress build-up as vacancy transport proceeds. It is clear that the GBs and MIs

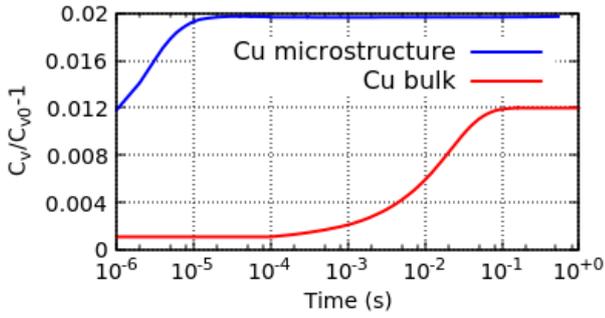


Fig. 7. The normalized vacancy concentration ($C_V/C_{V0} - 1$) after 1s of EM, where the conductivity term is dominant. We note that neglecting the grain boundaries significantly underestimates the vacancy concentration.

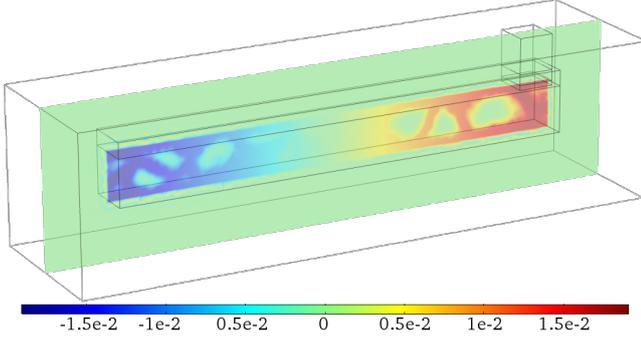


Fig. 8. The normalized vacancy concentration ($C_V/C_{V0} - 1$) after 0.01ms affects mainly the grain boundaries and material interfaces.

cause the stress to increase and we observe that the stress accumulates principally at the boundaries and interfaces. We note that from the onset of EM, the stress in the structure with GBs and MIs properly treated is higher. Furthermore, the rate at which stress increases with time is 2.6 times faster, when the microstructure is included.

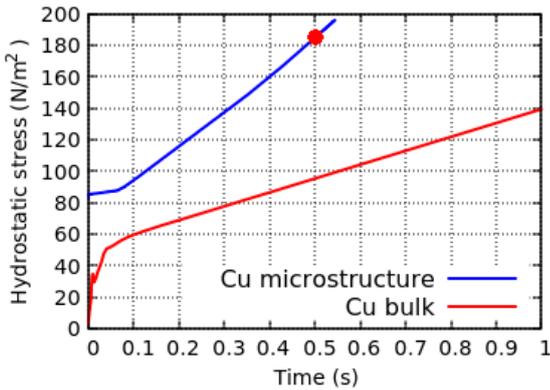


Fig. 9. Hydrostatic stress σ (N/m^2) through the Cu layer as EM proceeds. The red dot shows the time for the result in Fig 10.

In order to see where the stress build-up is highest, we plotted the hydrostatic stress distribution through the structure after 0.5s of operation in Fig. 10. It is clear that the maximum tensile and compressive stresses are found at the GBs and

MIs. This increase is mainly due to two main factors. The grain boundaries act as diffusivity pathways and the increased vacancy migration causes an increased stress according to (6). The vacancy generation/annihilation at the grain boundaries is an added source of strain according to (7).

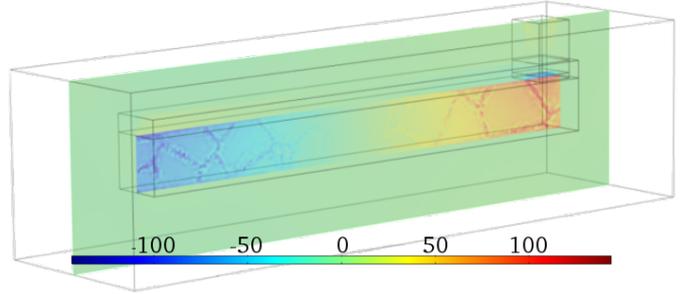


Fig. 10. Hydrostatic stress σ (N/m^2) through the Cu layer and in the Cu grain structure after 0.5s of operation.

VI. CONCLUSION

We show that the effect of the GBs and MIs cannot be ignored when performing EM simulations on nanoscale Cu interconnects. Therefore, we present a model which treats the presence of these microstructure interfaces as a binary material parameter, which is used to solve the spatial current density, the vacancy transport equations, and subsequently the EM-induced stress. The model allows to simulate complex and realistic interconnect geometries while including the effects of the GBs and MIs in a continuum simulation technique.

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