Hot-Carrier Degradation Modeling of Decananometer nMOSFETs Using the Drift-Diffusion Approach

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***Abstract*— We extend our previously suggested drift-diffusion (DD)-based hot-carrier degradation model to the case of decananometer transistors. Special attention is paid to the effect of electron–electron scattering, which populates the high energy tail of the carrier distribution function, by using a rate balance equation. We compare the results of the DD-based model with the results obtained from a spherical harmonics expansion of the Boltzmann transport equation as well as experimental data. We also study the accuracy and limits of the applicability of the DD-based model and conclude that this model is able to capture hot-carrier degradation in nMOSFETs over a range of gate lengths from 65 to 300 nm with excellent accuracy.**

***Index Terms*— Hot-carrier degradation, carrier transport, distribution functions, drift-diffusion, MOSFET.**

I. Introduction

HOT-CARRIER degradation (HCD) is a rather complex phenomenon and its physical modeling should be based on thorough carrier transport simulations [1]–[8]. However, solving the Boltzmann transport equation (BTE) is a challenging task which is often avoided during HCD modeling. As a result, a substantial fraction of HCD models are phenomenological, and even more dramatically, empirical [4]. A good trade-off between computational efficiency and accuracy can be achieved by using the drift-diffusion (DD) scheme. Although this scheme has a number of limitations, it has been shown to be effective for the description of carrier transport even in modern devices [9]. In one of our recent papers [10] we already demonstrated the applicability of the DD scheme for HCD modeling in high-voltages devices. In the case of decananometer MOSFETs, however, electron-electron scattering (EES) plays an important role [11]–[13] and results in a hump in the high-energy tail of the carrier energy distribution function (DF), see Fig. 1.

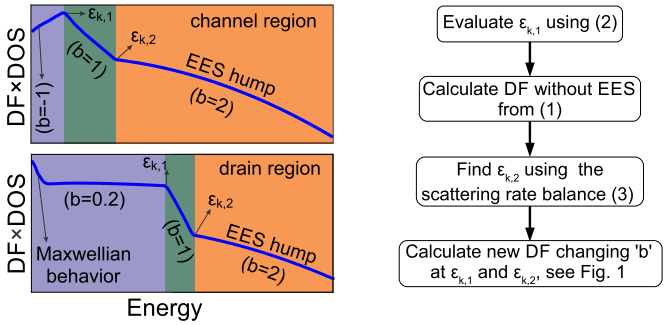

Fig. 1. Left panel: A schematic representation of the carrier DFs for the channel region (upper panel) and the drain region (lower panel) with the values of parameter *b*. Right panel: flowchart for the calculation of the carrier DF.

Here we extend our DD-based HCD model to decananometer devices and pay special attention to the effect of EES on the carrier DFs. This model allows to avoid the computationally expensive solution of the BTE but is expected to still provide excellent accuracy.

II. The Distribution Function

The reference electron DFs have been obtained with the deterministic BTE solver ViennaSHE for three different devices of the same architecture with SiON gate dielectric but with different gate lengths of $L_G = 65$, 150, and 300 nm and for $V_{gs} = V_{ds} = 1.8$ and 2.0 V (where V_{gs} and V_{ds} are the gate and drain voltages), see Fig. 2.

These complicated DFs can be approximated by the empirical expression [10] with a different value of b in each energy region (Fig. 1):

$$f(\varepsilon) = A \exp\left[-\left(\frac{\varepsilon}{\varepsilon_{\text{ref}}}\right)^b\right] + C \exp\left[-\frac{\varepsilon}{k_B T_n}\right], \qquad (1)$$

where ε is the carrier energy, and A, ε_{ref}, C are parameters [10]. The algorithm for the evaluation of the carrier DF is shown in Fig. 1. First, we calculate the first knee energy $\varepsilon_{k,1}$, which determines the end of the phonon

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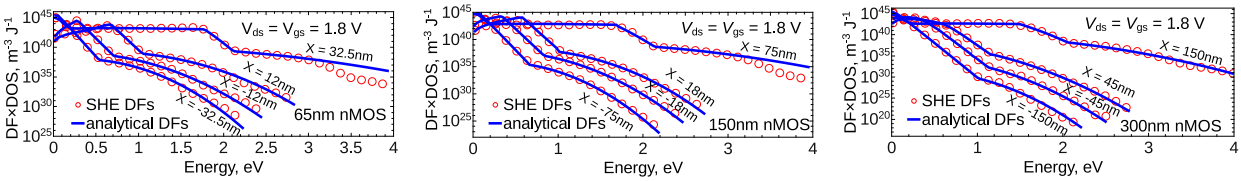

Fig. 2. The electron DFs simulated with ViennaSHE and with the DD-based model for three nMOSFETs with gate lengths of 65, 150, and 300 nm for $V_{gs} = V_{ds} = 1.8$ V plotted at different positions in the device. The source is at $x = -L_{G/2}$ and the drain is at $x = \mathcal{C} L_{G/2}$. The DFs are obtained for 25 °C.

cascade plateau visible at moderate energies for each lateral coordinate X, using the empirical formula:

$$\varepsilon_{k,1} = \alpha \exp[\beta - (\gamma - \delta F)^{\frac{1}{2}}], \tag{2}$$

with F being the electric field and α, β, γ, and δ the fitting parameters with values 0.4157 eV, 1.3, 11.04, 1.51×10^{-6} cmV^{-1}, respectively. Note that for all DFs calculated over the entire range of the lateral coordinate X and for various transistors stressed at different conditions we used this unique set of parameters.

Then, while neglecting EES for the moment, we evaluate the DF using (1). The parameters A, ε_{ref}, C in (1) are obtained from the moments of the BTE calculated from the DD simulations such as the carrier concentration, carrier temperature and DF normalization [10]. The full-band electron density-of-states in Si is taken from [14]. The parameter b in (1) varies with each knee energy as shown in Fig. 1. The DF slope is determined by b and ε_{ref}. There are two types of DFs, namely those typical for the channel and drain regions. For each of them we set the values of the parameter b according to the sketch shown in Fig. 1. This is performed without the effect of EES, i.e. at this stage we do not model the EES hump.

The second knee energy ($\varepsilon_{k,2}$) is obtained by balancing the in-scattering (EES) and out-scattering (interactions with phonons and ionized impurities) rates [15], [16]:

$$r_{ees} = r_{ii} + r_{op/abs} + r_{op/emi} + r_{ac}. \tag{3}$$

For $\varepsilon > \varepsilon_{k,2}$, the EES populates the high-energy tail of the DF (cf. Fig. 2) and therefore we set $b = 2$ at these energies. For the scattering rates in (3) we used the same standard expressions [17], [18] in both ViennaSHE and the DD-based model, namely:

$$r_{ac} = \frac{D_A^2 k_B T_L m^* p}{\pi c_l \hbar^4}, \tag{4}$$

where r_{ac} is the acoustic phonon scattering rate, D_A the acoustic deformation potential, k_B the Boltzmann constant, T_L the lattice temperature, m^* the electron effective mass, p the carrier momentum, c_l the elastic constant ($v_s = \sqrt{c_l/\rho}$, v_s the velocity of sound, and ρ the mass density);

$$r_{op/abs} = \frac{D_o^2 N_o m^* \sqrt{2m^* (\varepsilon + \hbar\omega_o)}}{2\pi\rho\omega_o\hbar^3}, \tag{5}$$

$$r_{op/emi} = \frac{D_o^2 (N_o + 1) m^* \sqrt{2m^* (\varepsilon - \hbar\omega_o)}}{2\pi\rho\omega_o\hbar^3}, \tag{6}$$

where $r_{op/abs}$ and $r_{op/emi}$ are the optical phonon scattering rates for absorption and emission of phonons, respectively, D_o is the optical deformation potential, $\hbar\omega_o$ the energy of optical phonons, while N_o is the density of optical phonons, $N_o = 1/(\exp[\hbar\omega_o/k_B T_L] - 1)$;

$$r_{ii} = \frac{N_A q^4}{16\sqrt{2m^*\pi}\,(\epsilon_{Si}\epsilon_0)^2}\Big[\ln\left(1 + {\gamma_D}^2\right) - \frac{{\gamma_D}^2}{1 + {\gamma_D}^2}\Big]\frac{1}{\varepsilon^{3/2}}, \tag{7}$$

with r_{ii} being the ionized impurity scattering rate, ϵ_{Si} the relative permittivity of silicon, ϵ_0 the absolute permittivity, ${\gamma_D}^2 = 8m^*\varepsilon L_D^2/\hbar^2$ with L_D being the Debye length given as $L_D = \sqrt{\epsilon_{Si}\epsilon_0 k_B T_n/q^2 n}$ and n the carrier concentration. Finally

$$r_{ees} = \frac{m^* q^4 n}{\epsilon_{Si}^2\epsilon_0^2\hbar^3}\sum_{\varepsilon}\frac{\sqrt{2m^*}/\hbar\,\left|\sqrt{\varepsilon} - \sqrt{\varepsilon_0}\right|}{{\beta_D}^2\left(\frac{2m^*}{\hbar^2}(\varepsilon - \varepsilon_0) + {\beta_D}^2\right)} f(\varepsilon) \tag{8}$$

where r_{ees} is the EES rate, and $\beta_D = 1/L_D$.

A pre-calculated DF is needed to calculate the EES rate. Thus, as a first step, DFs determined by (1) without taking EES into account are used to calculate $\varepsilon_{k,2}$. After the knee energies are evaluated, the new DFs can be calculated from (1) by changing the value of the parameter b correspondingly (see Fig. 1). To verify this DD-based approach, these DFs are then used in our physics-based HCD model [19]. It is important to emphasize that we use the same physical parameters in SHE- and DD-based simulations.

III. Results and Discussion

DFs simulated with the analytic approach and ViennaSHE for the 65, 150 and 300 nm devices at room temperature ($T = 25$ °C) are shown in Fig. 2 and very good agreement is achieved. Fig. 3 shows the knee energy profiles $\varepsilon_{k,2}(x)$ (x is the coordinate along the interface) obtained with the DD-based model and those extracted from the ViennaSHE DFs (Fig. 2). Good agreement between the results obtained with the two approaches suggests the validity of the rate balancing method.

Fig. 3 shows that the interface state density profiles $N_{it}(x)$ obtained using both versions of the model for stress times of 1 s and 4 ks are very similar. The changes in the linear drain current ($\Delta I_{d,lin}$) vs. stress time t simulated for two stress conditions $V_{gs} = V_{ds} = 1.8$ V and 2.0 V and stress times up to 10 ks at room temperature are shown in Fig. 4. As a reference we plot experimental $\Delta I_{d,lin}(t)$ curves for the 65 nm device which are properly captured by both versions of the model. In the 150 and 300 nm nMOSFETs, the DFs, N_{it} and $\Delta I_{d,lin}$ obtained with the two versions of the model match very well.

As can be understood from Fig. 1, the DF should change its shape at a certain position in the device X_{ch}. The value of X_{ch} is an important parameter of the model and therefore it is worth studying the model sensitivity to a change of X_{ch}. Fig. 4 (lower panels) summarizes the $\Delta I_{d,lin}(t)$ traces calculated with X_{ch} values artificially modified to $X_{ch} \pm 0.1 L_G$. In all three devices $\Delta I_{d,lin}(t)$ dependencies simulated for $X_{ch} + 0.1 L_G$ show that HCD is underestimated

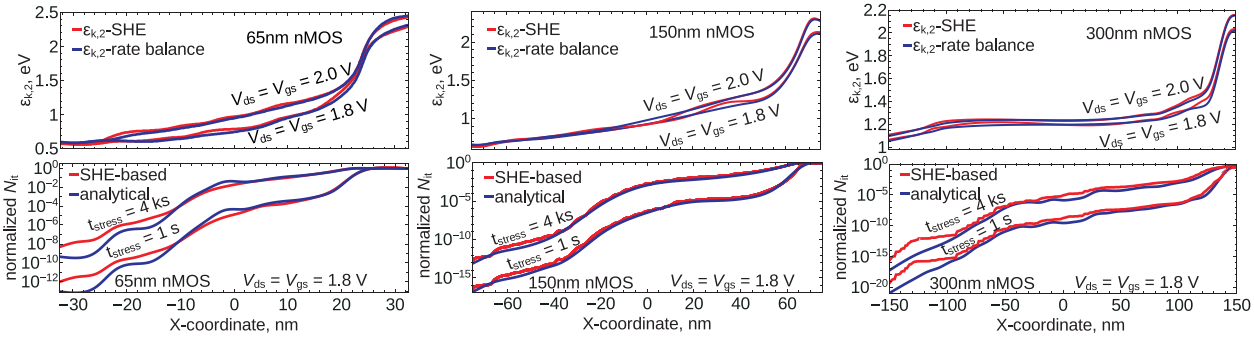

Fig. 3. Upper panels: The knee energy $\varepsilon_{k,2}$ (x) for all three devices obtained for the same stress conditions as in Fig. 2. Lower panels: The normalized (to the concentration of Si-H bonds) N_{it} (x) profiles, evaluated using DFs obtained with our analytic model and with ViennaSHE. Results are for $T = 25$ °C.

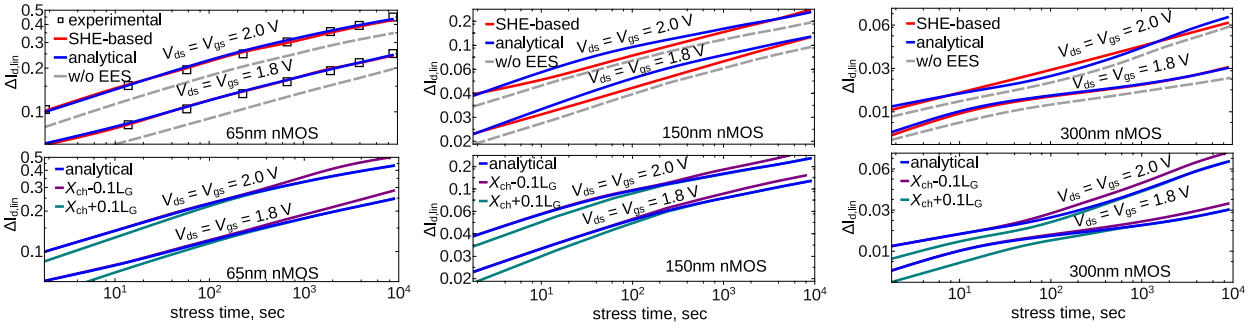

Fig. 4. Upper panels: Experimental vs. simulated changes in the linear drain current $\Delta I_{d,lin}$ for 65, 150, and 300 nm nMOSFETs as a function of stress time. The stress voltages are $V_{gs} = V_{ds} = 1.8$ V and 2.0 V. Dashed gray curves are the $\Delta I_{d,lin}$ traces obtained using (1), i.e. without the effect of EES. Lower panels: $\Delta I_{d,lin}$ traces simulated analytically with a regular X_{ch} and artificially shifted X_{ch} by 10% of the gate length L_G. All the data are for $T = 25$ °C.

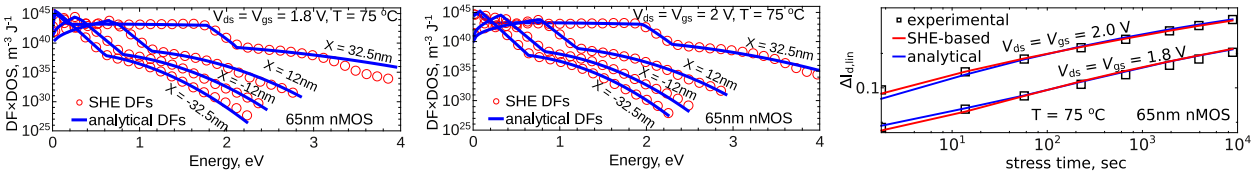

Fig. 5. The electron DFs calculated with ViennaSHE vs. those obtained with the DD-based version of the model for the 65 nm device at $T = 75$ °C (left and central panels) as well as experimental $\Delta I_{d,lin}$ (t) degradation traces compared with the results of two versions of the model (right panel).

at short times and is almost the same for longer stresses. HCD at short stress times is determined by the damage produced near the drain, i.e. by the drain DFs [10], [13]. If we artificially increase X_{ch}, the change of the DF shape occurs closer to the drain. Thus, DFs calculated for the segment of $[X_{ch}, X_{ch} + 0.1L_G]$ have lower populated high-energy tails and the damage near the drain is underestimated. The opposite trend is visible if the $\Delta I_{d,lin}(t)$ dependencies are calculated for $X_{ch} - 0.1L_G$.

To further check the predictive capabilities of the DD-based model we calculated eletron DFs and $\Delta I_{d,lin}(t)$ traces for the 65 nm transistor for the same combinations of stress voltages but for a higher temperature of $T = 75$ °C, Fig. 5. One can see that also in this case the model can properly represent the DFs and capture the drain current degradation. It is important to emphasize again that for all devices and all stress conditions we used a unique set of model parameters.

Note finally that in longer devices DFs have a less complex structure and are modeled by (1) [10], [20]. For the case of shorter devices, on the other hand, EES plays an important role and, thus, the comprehensive approach used in this work is required. To check this in more detail we also calculated $\Delta I_{d,lin}(t)$ traces using DFs obtained with (1). Fig. 4 shows that for both combinations of V_{ds}, V_{gs} HCD is underestimated in the entire stress time window. The difference in $\Delta I_{d,lin}$ values appears to be less significant when L_G increases. Therefore, we conclude that the presented model works properly over a wide range of gate lengths, i.e. for $L_G = 65 - 300$ nm.

IV. Conclusions

We have developed and validated an HCD model which is based on an analytical expression for the carrier distribution function with parameters computed using the drift-diffusion scheme. The effect of electron-electron scattering on the electron DF was captured by our approach by using a rate balance equation and a unique set of model parameters. It was shown that the model can properly represent DFs and HCD (including its temperature dependence) in nMOSFETs with gate lengths in a range of 65-300 nm, while for longer devices a similar model but omitting the EES is applicable. The main advantage of this model is that it uses the simple and fast DD scheme instead of a computationally intensive solution of the BTE.

REFERENCES

[1] W. McMahon, K. Matsuda, J. Lee, K. Hess, and J. Lyding, "The effects of a multiple carrier model of interface states generation of lifetime extraction for MOSFETs," in *Proc. Int. Conf. Modeling Simulation Microsyst.*, vol. 1. 2002, pp. 576–579.

[2] W. McMahon, A. Haggag, and K. Hess, "Reliability scaling issues for nanoscale devices," *IEEE Trans. Nanotechnol.*, vol. 2, no. 1, pp. 33–38, Mar. 2003.

[3] S. Tyaginov, I. Starkov, C. Jungemann, H. Enichlmair, J.-M. Park, and T. Grasser, "Impact of the carrier distribution function on hot-carrier degradation modeling," in *Proc. Eur. Solid-State Device Res. Conf. (ESSDERC)*, 2011, pp. 151–154.

[4] S. Tyaginov and T. Grasser, "Modeling of hot-carrier degradation: Physics and controversial issues," in *Proc. Int. Integr. Rel. Workshop (IIRW)*, 2012, pp. 206–215.

[5] Y. Randriamihaja, V. Huard, X. Federspiel, A. Zaka, P. Palestri, D. Rideau, and A. Bravaix, "Microscopic scale characterization and modeling of transistor degradation under HC stress," *Microelectron. Rel.*, vol. 52, no. 11, pp. 2513–2520, 2012.

[6] Y. Randriamihaja, X. Federspie, V. Huard, A. Bravaix, and P. Palestri, "New hot carrier degradation modeling reconsidering the role of EES in ultra short n-channel MOSFETs," in *Proc. Int. Rel. Phys. Symp. (IRPS)*, 2013, pp. 1–5.

[7] S. Reggiani, G. Barone, S. Poli, E. Gnani, A. Gnudi, G. Baccarani, M.-Y. Chuang, W. Tian, and R. Wise, "TCAD simulation of hot-carrier and thermal degradation in STI-LDMOS transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 691–698, Feb. 2013.

[8] S. Reggiani, G. Barone, E. Gnani, A. Gnudi, G. Baccarani, S. Poli, R. Wise, M.-Y. Chuang, W. Tian, S. Pendharkar, and M. Denison, "Characterization and modeling of electrical stress degradation in STI-based integrated power devices," *Solid-State Electron.*, vol. 102, no. 12, pp. 25–41, 2014.

[9] M. Lundstrom, "Drift-diffusion and computational electronics—Still going strong after 40 years!" in *Proc. Int. Conf. Simulation Semiconductor Process. Devices (SISPAD)*, Sep. 2015, pp. 1–3.

[10] P. Sharma, S. Tyaginov, Y. Wimmer, F. Rudolf, K. Rupp, M. Bina, H. Enichlmair, J.-M. Park, R. Minixhofer, H. Ceric, and T. Grasser, "Modeling of hot-carrier degradation in nLDMOS devices: Different approaches to the solution of the Boltzmann transport equation," *IEEE Trans. Electron Devices*, vol. 62, no. 6, pp. 1811–1818, Jun. 2015.

[11] S. E. Rauch, F. J. Guarin, and G. LaRosa, "Impact of E-E scattering to the hot carrier degradation of deep submicron NMOSFETs," *IEEE Electron Device Lett.*, vol. 19, no. 12, pp. 463–465, Dec. 1998.

[12] S. Tyaginov, M. Bina, J. Franco, Y. Wimmer, B. Kaczer, and T. Grasser, "On the importance of electron–electron scattering for hot-carrier degradation," *Jpn. J. Appl. Phys.*, vol. 54, no. 4S, pp. 04DC18-1–04DC18-6, 2015.

[13] M. Bina *et al.*, "Predictive hot-carrier modeling of n-channel MOSFETs," *IEEE Trans. Electron Devices*, vol. 61, no. 9, pp. 3103–3110, Sep. 2014.

[14] C. Jungemann and B. Meinerzhagen, *Hierarchical Device Simulation: The Monte-Carlo Perspective*. New York, NY, USA: Springer-Verlag, 2003.

[15] D. Ventura, A. Gnudi, and G. Baccarani, "An efficient method for evaluating the energy distribution of electrons in semiconductor s based on spherical harmonic expansion," *IEICE Trans. Electron.*, vol. E75-C, no. 2, pp. 194–199, 1992.

[16] P. A. Childs and C. C. C. Leung, "New mechanism of hot carrier generation in very short channel MOSFETs," *Electron. Lett.*, vol. 31, no. 2, pp. 139–141, Jan. 1995.

[17] M. Lundstrom, *Fundamentals of Carrier Transport*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2000.

[18] C. Jacoboni and P. Lugli, *The Monte Carlo Method for Semiconductor Device Simulation*. Wien: Springer-Verlag, 1989.

[19] S. Tyaginov, M. Jech, J. Franco, P. Sharma, B. Kaczer, and T. Grasser, "Understanding and modeling the temperature behavior of hot-carrier degradation in SiON nMOSFETs," *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 84–87, Jan. 2016.

[20] P. Sharma, S. Tyaginov, Y. Wimmer, F. Rudolf, K. Rupp, M. Bina, H. Enichlmair, J.-M. Park, H. Ceric, and T. Grasser, "Predictive and efficient modeling of hot-carrier degradation in nLDMOS devices," in *Proc. Int. Symp. Power Semiconductor Devices IC's (ISPSD)*, May 2015, pp. 389–392.