Characterization of Interface Defects With Distributed Activation Energies in GaN-Based MIS-HEMTs

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***Abstract*— Charge trapping is one of the main reliability issues for GaN-based MIS-high-electron-mobility-transistor technologies. In this paper, we focus on the defects located at or close to the interface with the dielectric, which are responsible for the threshold voltage instability at positive gate bias conditions. We present a methodology to analyze the experimental data based on the nonradiative multiphonon model for charge trapping. In particular, we show how to extract the density of interface traps as a function of their activation energy from stress and recovery experiments performed at various temperatures. Our approach is applied to two GaN/AlGaN/SiN samples with different trapping properties, at temperatures ranging from −190 °C to 200 °C. We evaluate their response to forward bias stress and finally, we extract the activation energy distribution for electron capture and emission over a continuous energy range.**

***Index Terms*— Gallium nitride, interface defects, MIS-high-electron-mobility-transistors (HEMTs), reliability.**

I. Introduction

WIDE bandgap materials have recently become the object of cutting-edge research in the field of power electronics. In particular, GaN-based devices are good candidates for high efficiency power switching applications because of their superior material parameters. However, device reliability is still a critical issue. In particular, charge trapping phenomena result in severe drift effects in high-electron-mobility-transistors (HEMTs) and MIS-HEMTs.

The cause of such drift phenomena is defects in the device structure. When a positive gate bias is applied, defects located in the gate stack act as charge trapping sites. This induces a shift of the device transfer characteristics toward more positive values. These defects are located at the interface between the III−N material and the dielectric. However, their origin is still under debate and their precise identity is still unknown [1]–[4]. In fact, the question whether the defects responsible for the device drift are the same as the donor states necessary to counterbalance the existence of the 2-D electron gas (2-DEG) has still to be satisfactorily answered.

In order to minimize the detrimental impact of defects on the device performance, a comprehensive understanding of their nature and behavior is necessary. In this paper, we focus on interface states and their dependence on temperature. We apply an experimental method we have discussed previously [5] and we present our experimental results on two samples with different III−N/dielectric interface properties. Assuming a physical model based on nonradiative multiphonon (NMP) carrier exchange, we evaluate the activation energy distribution associated with charge trapping and detrapping events, which is the fingerprint of the defects responsible for the device drift. In particular, the technique we use to analyze the data confirms that these do not just have a single-valued activation energy, but rather a broad distribution over a continuous range of energy, similar to what has been recently demonstrated for Si technologies [6].

II. Experimental Details

We use GaN/AlGaN/SiN MIS-HEMT structures processed in different ways in order to investigate the role of the AlGaN/dielectric interface defects in terms of device drift. The devices are grown on a silicon substrate by metal-organic chemical vapor deposition. The bulk consists of an unintentionally doped GaN buffer, above which the AlGaN barrier is deposited. An low pressure chemical vapor deposition grown SiN dielectric is realized on top of the AlGaN barrier, as shown in the cross sections in Fig. 1. We use two wafers with slight differences in layer thickness and epitaxial process, one of which has undergone an additional AlGaN surface treatment with a fluorination process by exposure to plasma containing NF_3, before the deposition of the SiN dielectric. We will refer to these test structures as standard and fluorinated devices. The former has a 25-nm-thick $Al_{0.25}Ga_{0.75}N$ barrier and a 50-nm-thick SiN dielectric, and the latter a 20-nm-thick $Al_{0.2}Ga_{0.8}N$ layer with 25-nm-thick SiN.

Manuscript received November 9, 2016; accepted January 13, 2017. Date of publication February 13, 2017; date of current version February 24, 2017. This work was supported in part by the Austrian Research Promotion Agency FFG under Project 854247 and in part by the Carinthian Economic Promotion Fund KWF under Contract KWF-1521|28101|40388. The review of this paper was arranged by Editor K. J. Chen. *(Corresponding author: Roberta Stradiotto.)*

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Digital Object Identifier 10.1109/TED.2017.2655367

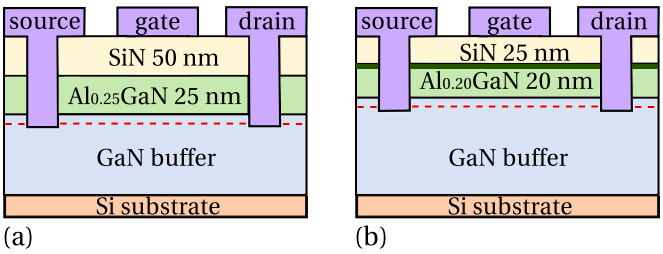

Fig. 1. Schematic cross section of (a) standard and (b) fluorinated GaN/AlGaN/SiN devices. The layer thicknesses are not to scale. Red dashed line: position of the 2-DEG. Dark green area: AlGaN surface cleaned with the fluorine plasma process.

The devices with a standard interface have been extensively investigated in our previous studies, and they usually show a broad distribution of time constants, ranging at least from 100 ns to 10 ks during both stress and recovery [5], [7], [8]. On the contrary, the fluorination process results in substantially different electrical properties of the MIS-HEMTs in terms of charge trapping, giving rise to a behavior never seen before in GaN/AlGaN MIS-HEMTs [9].

The goal of this paper is to investigate the two samples and further analyze the temperature dependence of their degradation, in order to understand the different trapping behavior and suggest an explanation based on a physical model.

We perform impedance and current measurements with a Zurich Instruments HF2LI lock-in amplifier. For impedance measurements, we use a frequency of 100 kHz and an oscillating amplitude of 500 mV. Variations of the amplitude down to 10 mV do not impact the results in terms of voltage shift, but increase the noise level. We optimized the measurement software for nearly logarithmic sampling after a gate bias switch [5].

All measurements have been run on a Lakeshore cryogenic probe station with liquid nitrogen cooling and cover a temperature range from −190 °C to 200 °C (83.15 to 473.15 K).

III. Methodology

We study the response of the MIS-HEMTs to the application of forward bias stress, over the temperature range accessible with our setup. With this experiment, we can investigate the properties of the gate stack, and in particular of the AlGaN/dielectric interface. In fact, at positive gate bias conditions, the 2-DEG effectively screens any contribution from defects in the GaN buffer.

A. Small-Signal Response of GaN/AlGaN MIS-HEMTs

We study the response of the MIS test structures to a superposition of large and small-signal excitation by measuring the impedance characteristics. By applying a small oscillating signal and varying the dc baseline to the gate, we distinguish the three regions of operation visible in Fig. 2: depletion, 2-DEG formation, and *spill over*, corresponding to the three capacitance plateaus. In particular, the spill-over region provides important information about the status of the gate stack, which is not directly accessible by drain current measurements. Above the threshold V_{so}, the spill-over voltage, the electrons from the 2-DEG start to flow through the AlGaN

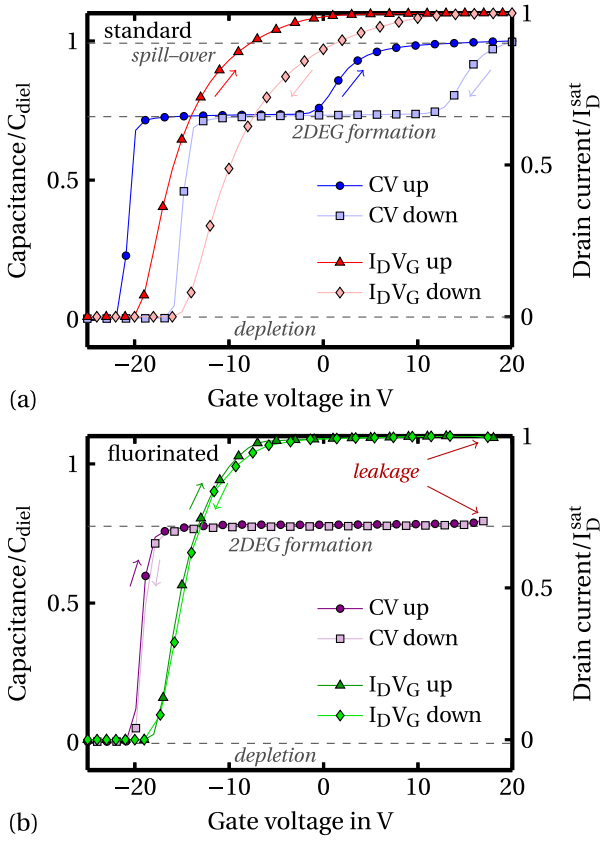

Fig. 2. Typical transfer characteristics of an MIS-HEMT and an MIS *CV* curve of (a) standard and (b) fluorinated devices. The hysteresis has a strong impact on standard devices, resulting in a horizontal shift of several volts. However, this effect is absent when the fluorination process is used.

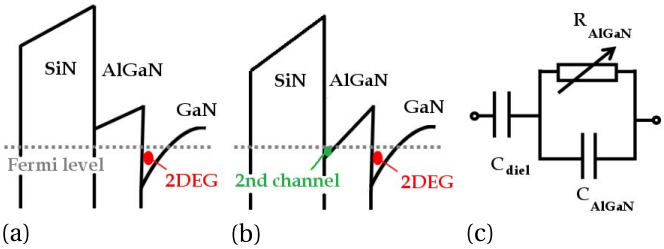

Fig. 3. Conduction band diagrams around zero gate bias, when (a) 2-DEG is formed and (b) above the spill-over voltage V_{so}. (c) Equivalent circuit model of a composite GaN/AlGaN MIS structure.

barrier to the AlGaN/SiN interface, forming a second channel [see the band diagrams in Fig. 3(a) and (b)]. As a consequence, the measured capacitance, which is $(C_{\mathrm{AlGaN}}^{-1} + C_{\mathrm{diel}}^{-1})^{-1}$ below V_{so} (capacitance of the barrier and that of the dielectric in series), gradually increases toward C_{diel}. The behavior of the AlGaN barrier changes from insulating to partially conductive, depending on the dc bias [7]. The standard equivalent model of C_{AlGaN} and C_{diel} in series is, therefore, not complete, as we must consider a certain bias-dependent resistance R_{AlGaN} in parallel with C_{AlGaN}, as shown in Fig. 3(c). This model can already explain the observed frequency dispersion of the *CV* curve, without introducing the contribution of interface traps [10].

Because of the dynamic response of composite GaN/AlGaN structures, methods to extract the density of interface defects

based on the frequency dispersion of capacitance or conductance characteristics [11] are inadequate in our case. In fact, such techniques usually assume an equivalent circuit model that neglects the role of the AlGaN layer. The frequency dispersion arising from the presence of the barrier conceals, or at least superimposes to the impedance response of the interface states. In addition, another limitation of many established methods is the assumption of the Shockley–Read–Hall model. Experimental evidence on silicon MOSFETs as well as on GaN/AlGaN MIS-HEMTs has proved that a more complete model for charge trapping is necessary instead [7], [12].

Furthermore, we must consider the impact of hysteresis when we characterize the devices with a standard interface. An example of two consecutive sweeps in different directions is shown in Fig. 2(a). We have shown that not only different sweep directions result in different characteristics, but also that the characteristics themselves depend on measurement parameters like sweep rate and sweep start and stop values [5]. This is a clear indication that the device does not reach thermal equilibrium during a *CV* measurement. In other words, the traps are not in resonance with the ac signal, capturing and emitting electrons by following the small-signal oscillations, because of the voltage drift caused by the dc bias. This ΔV does not saturate within the duration of the measurement at each gate voltage while sweeping, since the interface traps have such a broad range of characteristic time constants. This means that thermal equilibrium, one of the fundamental assumptions for methods based on the analysis of the impedance characteristics [11], is not reached. Therefore, we must conclude that the high-frequency analysis of the *CV* curve or the conductance method cannot be directly applied to our test structures.

The dependence of the impedance curves on the measurement parameters makes the characterization of the device quite challenging. Therefore, any measurement methodology must be carefully examined in order to avoid sources of systematic errors or artifacts.

B. Investigating the Standard Devices

An accurate way to measure the devices with the standard interface is the *capacitance-on the fly* (C-OTF) method, because it allows to evaluate the device degradation directly during the stress transient [5]. The fundamental concept is the same as that of the OTF method, already in use for the characterization of silicon MOSFETs [13], [14]. In practice, a positive excitation signal V_{stress} is applied to the gate contact of a fresh device to measure the time evolution of the impedance. We choose a dc bias value well above the spill-over voltage, in order to form the second electron channel at the AlGaN/dielectric interface, since the beginning of stress. In this way, any further decrease of capacitance is due to electron trapping at interface states, and it can be considered as a right shift of the whole *CV* curve. In addition, in this condition, the electron density at the AlGaN/SiN or at the AlGaN/GaN interface is always large enough to effectively screen any contribution from buffer defects.

After the stress transient, we measure the impedance characteristics with the same measurement parameters (oscillating amplitude and frequency), as shown in Fig. 4. This serves as a reference to calculate the amount of voltage shift (indicated as ΔV) from the transient data, as shown in Fig. 5. The final ΔV result does not depend on the frequency and on the oscillating amplitude, provided that the same values are used for the stress transient and for the *CV* curve. We have previously investigated in detail the impact of the sweep rate and the initial dc bias on the shape of the *CV* curve [5]. By using a relatively high sweep rate and gradually decreasing the dc bias from V_G' to zero, we minimize the impact of charge trapping during the measurement. As such, the resulting *CV* curve is the best representation of the device status at the end of the stress transient.

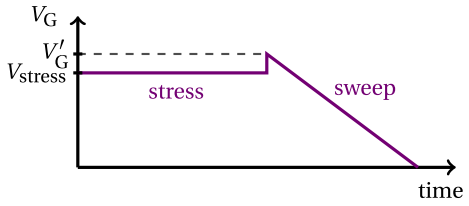

Fig. 4. Schematic of the C-OTF measurement method. We record an impedance transient at constant stress bias, followed by a sweep, the reference *CV* characteristic, which is used to calculate the voltage shift.

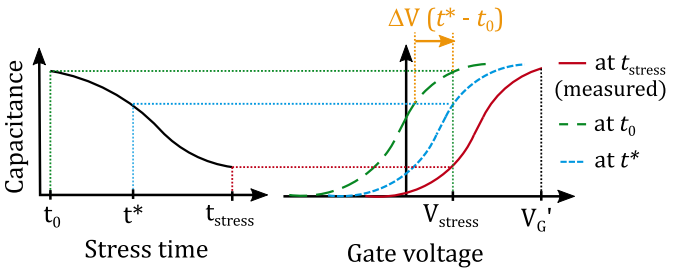

Fig. 5. Illustration of the C-OTF basic principle. After a stress transient (left), a *CV* curve is measured (right), which is used as a reference to extract the voltage shift ΔV for each point of the transient (from [5]).

The first limitation of this method is due to the fact that some additional stress must be applied when performing the *CV* sweep. In fact, in order to calculate the voltage shift during the whole period, we should choose $V_G' = V_{\text{stress}} + \Delta V$. Smaller values of V_G' do not allow the calculation of ΔV in the initial part of the transient. Some preliminary measurements allow to determine the most suitable V_G', to find a tradeoff between the amount of additional stress and the first achievable data point in time. We choose V_G' of 6 V after a stress at $V_{\text{stress}} = 5$ V, which allows the extraction of the voltage shift starting from 100 ms. Another drawback of the C-OTF approach is that the extracted ΔV should be corrected with an offset ΔV_0. In fact, we can determine the voltage shift between the first and last measurement point of the stress transient, but we do not know the amount of degradation present at the beginning. In other words, we miss a certain initial ΔV_0 because of the unavoidable experimental delay between the application of the stress bias and the first sampling point. Therefore, we arbitrarily set ΔV_0 to zero. This is an issue common to any characterization method. For example, in a stress-recovery experiment, the delay in the recovery transient

might severely underestimate the amount of degradation after stress [5], [7], [14].

C. Investigating the Fluorinated Devices

The spill-over voltage of the fluorinated devices is very close to the forward bias device breakdown, as shown in Fig. 2(b). However, even if it was possible to hold such a voltage without degrading the device, we would not see an increase of the capacitance as for the standard samples. In fact, the fluorinated structures exhibit a particular trapping behavior. Electron capture can be measured with our setup only at voltages close to the threshold voltage when the device is turned ON, i.e., when the gate bias is switched from a value in depletion to one slightly above V_{th}. Transients taken at gate biases well above the threshold voltage up to 20 V are very stable down to a few microseconds [9]. This means that electron trapping in these cases is too fast to be accessible with our setup, reaching an equilibrium condition before we can measure our first experimental point. As a result, the electrons in the second channel, which would cause the rise of capacitance to C_{diel}, are quickly trapped at interface states and the capacitance remains at the plateau value $(C_{\text{AlGaN}}^{-1} + C_{\text{diel}}^{-1})^{-1}$. For this reason, for the fluorinated devices, we focus on the electron emission mechanisms rather than on electron capture.

Most interestingly, once the traps have been filled, electron emission takes place at all values of gate voltage, with a strong dependence on temperature. This means that we can observe an increase of the drain current at all biases, from the spill-over voltage down to depletion, which corresponds to a parallel shift of the transfer characteristics to more negative values. In all cases, the negative drift comes to saturation at about 10 ms, and the final value of drain current is the same as before the application of the recovery bias [9]. This means that the Fermi level during recovery returns promptly to the position it had at a more positive gate voltage. For this reason, these devices appear very stable and the hysteresis is absent. Such behavior can be explained with the presence of a very high density of trap states close to the Fermi level. In equilibrium conditions, they are filled with electrons, which are then readily emitted during recovery, thus bringing the Fermi level back to the same position. In order to further investigate the mechanism of charge detrapping as a function of time and temperature, we perform the following experiment: we hold the gate bias at 10 V until all traps are filled (variation of the duration from 1 to 100 s does not change the result), and then we switch it to −10 V and record the increase of drain current. We use an OTF procedure based on the measurement of drain current transients, which allows the extraction of the drift ΔV as a function of time [9]. In this case, we obtain a decrease of ΔV, which is due to electron emission. On the contrary, the C-OTF experiment on standard devices results in an increase of the voltage shift as a function of stress time because of electron capture. However, in both cases, the device is in equilibrium before the beginning of the experiment.

Finally, from the voltage drift extracted from the measurement and assuming the defects to be located at the AlGaN/dielectric interface, we can directly calculate the effective density of interface states activated during stress as

$$\Delta N_{\text{it}} = \frac{C_{\text{diel}}}{qA}\Delta V \tag{1}$$

where C_{diel} is the dielectric capacitance, q is the elementary charge, and A is the device area. The measurements on the standard and fluorinated devices allow us to study the behavior of the test structures under forward bias stress and recovery, and extract the activation energy for the capture and emission of electrons from the interface states.

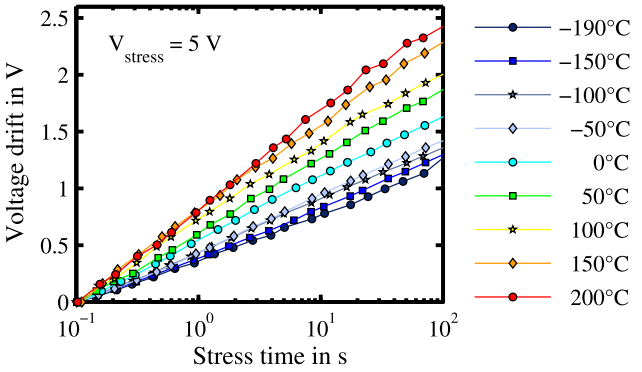

Fig. 6. Isothermal forward gate bias stress experiments on the standard structures from cryogenic (−190 °C) to high (200 °C) temperature, for the GaN/AlGaN/SiN. Interestingly, the temporal behavior of the degradation does not change much in a range of almost 400 °C.

IV. Experimental Results

The results of forward gate bias stress experiments on the standard GaN/AlGaN/SiN structures are shown in Fig. 6. We observe a logarithmic behavior over time, consistent with previous observations [5], [7]. We estimate the density of electrically active interface states at the interface to be on the order of 10^{13} cm^{-2}.

We investigate the influence of temperature by performing C-OTF experiments for 100 s at 5 V, placing the wafer in a cryogenic probe station. We span a range of nearly 400 °C, from liquid nitrogen temperature (−190 °C) to the highest chuck temperature (200 °C). From the coldest to the hottest conditions, we always observe a logarithmic behavior over time. The only difference with increasing temperature is an increase of the slope of ΔV.

The fluorinated devices instead exhibit significantly different trapping properties. In fact, they recover completely from a 10 V forward bias stress in a short time, namely, 10 ms at room temperature [9]. Varying the duration of stress from 1 s to longer intervals up to 100 s does not change the recovery transients, neither in terms of their temporal evolution nor with respect to the threshold voltage shift value after stress. This means that all available trapping sites capture an electron in a period smaller than one second and remain stable until the gate bias is changed to a more negative value. Then, all traps emit their electron with a temperature-dependent time constant, as can be seen in Fig. 7 for a recovery bias of −10 V.

In Section V, we discuss the different results of our measurements and offer a physical interpretation to help

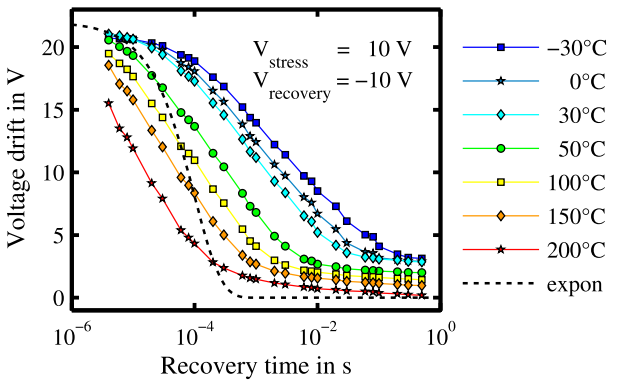

Fig. 7. Isothermal forward gate bias stress experiments on the fluorinated structures. Only the recovery transient is shown. An exponential recovery line with a single time constant of 100 μs is also shown for comparison (labeled "expon").

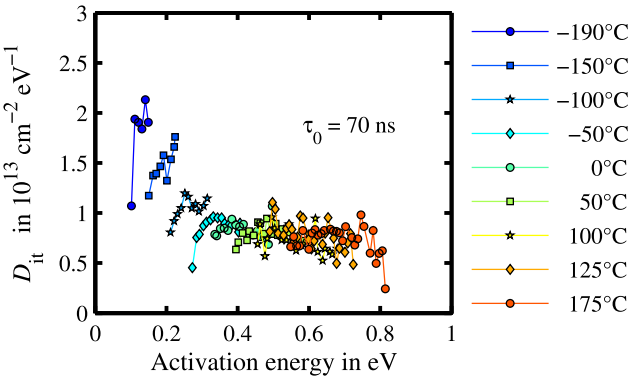

Fig. 8. Distribution of interface traps per unit energy D_{it} over activation energy for the standard AlGaN/SiN samples is distributed over the whole accessible energy range, from 0.1 to 0.8 eV.

understand the trapping properties of standard and fluorinated III−N/dielectric interfaces.

V. Discussion

In order to correctly interpret the experimental data, we must adopt a model that can explain the dependence of the device shift on time, on bias as well as on temperature. In the past years, research on silicon and silicon carbide bias temperature instability confirmed the validity of the NMP theory for charge exchange between defects and their surroundings [12], [15]. The basic idea of this approach is to consider the changes in the structural configuration of the defect site caused by charge exchange. In other words, when a trapping (or detrapping) event takes place, the microscopic structure of the defect and its surroundings evolves toward a different equilibrium configuration. The equilibrium configuration is determined as the minimum of the total potential energy of the system. In this way, the capture (or emission) of an electron corresponds to a transition between different potential energy surfaces, followed by a relaxation toward the final equilibrium configuration. In order to accomplish a certain transition, typically there is an energy barrier to overcome the activation energy E_A. In the absence of electromagnetic radiation (nonradiative process), the transition is mediated by phonons. This means that the excess energy E_A is provided to the system as thermal energy through phonon scattering. In the classical high-temperature limit, the characteristic time constant for an NMP transition can be, therefore, expressed by an Arrhenius equation

$$\tau = \tau_0 \, e^{E_A/k_B T}. \tag{2}$$

Equation (2) describes a single charge trapping event, taking place at a specific defect site. This reaction contributes to the total voltage shift of the device under test. The measurable time constant associated with the time evolution of ΔV is, therefore, the average over all defects present in the macroscopic structure. However, there can be different types of defects, each with its own E_A. Furthermore, the chemical composition of the material may present a certain variability. For example, the trap state could be located in an amorphous material, or at nonideal interfaces, where structural defects give rise to a highly disordered interlayer. As a consequence, slightly different equilibrium configurations are also possible for the same defect type, thus allowing a continuous interval of activation energies. In addition, in general, we could expect each trap to have a different characteristic coefficient τ_0 as well. However, in the following, we will approximate τ_0 as an effective average value, which is usually accurate enough for our purposes [6].

We can extract the distribution of activation energies with a method previously suggested for the analysis of chemical reactions with distributed energy barriers [16]. A similar approach has also been used more recently for the extraction of broadly distributed time constants in Si MOSFETS [6]. In fact, the charge trapping events responsible for the device drift involve a chemical modification to certain bonds at the AlGaN/SiN interface. We assume for simplicity the reaction to be the first order, thus following a rate equation given by:

$$-\frac{dg}{dt} = kg \tag{3}$$

where g (t) is the reactant concentration and $k = 1/\tau$ is a temperature-activated rate constant, for which (2) holds. In our case, the reactants are the active trap states. We simplify the solution by assuming the trap concentration to be distributed smoothly over activation energy, which means that this approach will not be sensitive to sharp features but will capture the overall general behavior of the distribution. We can calculate the initial concentration of defects per unit energy, D_{it}, from the experimental data during recovery as [16]

$$D_{it}(k_B T \ln(k_0 t)) = -\frac{t}{k_B T}\frac{d\Delta N_{it}}{dt} \tag{4}$$

where ΔN_{it} is calculated from (1) and k_0 is the inverse of the coefficient τ_0.

This method enables us to directly visualize the energy spectrum of the defect concentration. The prefactor τ_0 is the parameter, which allows to connect the measurements at various temperatures. We optimize it in order to obtain one single peak in the spectrum, minimizing the difference between the parts at different temperatures.

The result on standard samples is shown in Fig. 8. These devices exhibit a broad distribution of activation energies from 0.1 to 0.8 eV with an approximate energy density

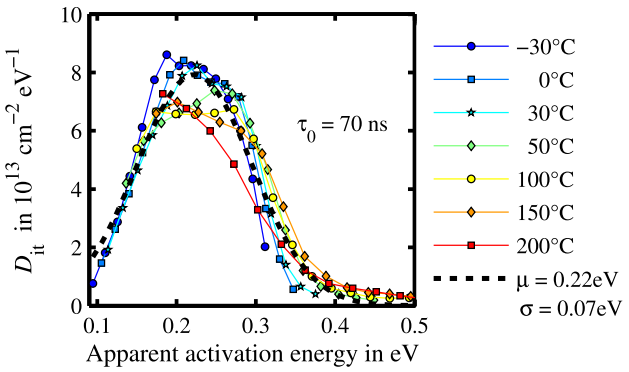

Fig. 9. Distribution of interface defects per unit energy D_{it} over the activation energy for the fluorinated devices. The trap level is distributed around 0.22 eV, and it is fitted with a normal distribution with mean $\mu = 0.22$ eV and standard deviation $\sigma = 0.07$ eV.

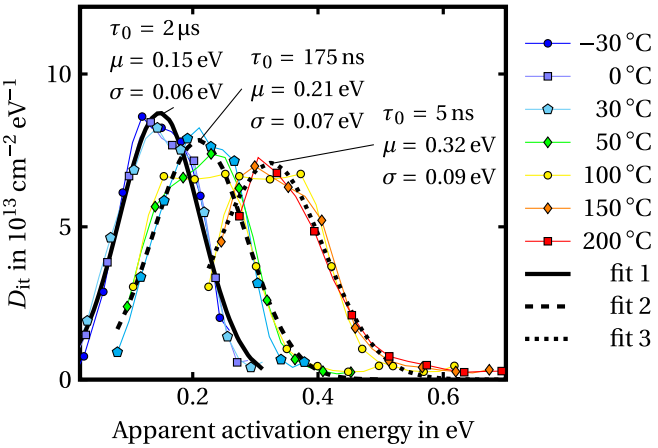

Fig. 10. Distribution of the interface defects per unit energy D_{it} over activation energy, calculated in three separate groups of temperatures. Group 1: −30 °C, 0 °C, and 30 °C. Group 2: 30 °C, 50 °C, and 100 °C. Group 3: 100 °C, 150 °C, and 200 °C. The optimized τ_0 values as well as the parameters of the normal fit are reported in the figure.

of 10^{13} cm^{-2}eV^{-1}, giving rise to an almost uniform distribution of time constants, which leads to the logarithmic time dependence observed in such structures. This is consistent with the observed amorphous nature of the AlGaN/SiN interface. In fact, the chemical variability results in a broad distribution of bond length and angles, thus allowing a very large range of possible activation energies [17].

The fluorinated devices, on the other hand, show a narrower distribution of activation energies, as shown in Fig. 9. Using the optimized value of $\tau_0 = 70$ ns, we obtain an activation energy distributed around the mean value of 0.22 eV, ranging from 0.1 to 0.3 eV. We fit the spectra with a normal distribution with mean value $\mu = 0.22$ eV and $\sigma = 0.07$ eV.

However, at closer inspection of Fig. 9, we note that the approximation of τ_0 to a constant value does not hold completely true. In fact, we can see that a single τ_0 value does not allow a perfect alignment of the curves at all different temperatures. This becomes more evident if we try to apply the analysis to smaller groups of temperatures separately. Fig. 10 shows that the τ_0 value optimized by the numerical algorithm decreases from the coldest to the hottest temperature group.

The prefactor τ_0 includes the contribution of tunneling from the trap states to the electron reservoir in the conduction band. This coefficient can be calculated with the Wentzel–Kramers–Brillouin approximation, which can be further simplified to be field independent for defects very close to the interface [12]. The discrepancy between results at different temperatures indicates that this simplification cannot be applied in our case. Therefore, similar to what has been concluded in a previous study on fluorinated devices[1] [9], we must consider an additional field and temperature-dependent charge transport mechanism, for instance, phonon-assisted tunneling. This phenomenon would cause a deviation from the Arrhenius behavior, which is visible in the nonlinearity of the Arrhenius plot. As a consequence, the activation energy obtained with our analysis would contain an error, because our method assumes that only NMP transitions take place. However, since phonon-assisted tunneling has a weaker temperature dependence than NMP transitions, its contribution becomes smaller the higher the temperature. For this reason, the most accurate estimation of E_A with the method presented in this paper is the one at high temperature, the fit 3 in Fig. 10. Using only the three highest temperature data sets, the optimized time constant is $\tau_0 = 5$ ns and the apparent activation energy is fitted by a normal distribution with mean value $\mu = 0.32$ eV and standard deviation $\sigma = 0.09$ eV. This must be considered only as a lower limit for the real E_A value, which could be better estimated with further measurements at higher temperatures, or by modeling the τ_0 dependence as a function of bias.

The different trapping behavior compared with standard devices can be explained by assuming that the fluorinated AlGaN/SiN interface is more ordered and stable. In fact, it has been suggested that the fluorine radical F^- competes with the hydrolytic group OH^- for the AlGaN surface bonds [17]. In this way, it could substitute a portion of the surface bonds, which is large enough to influence the properties of the 2-DEG [9], thereby changing the dominant defect type at the interface and thus modifying the electrical and trapping properties of the device.

VI. Conclusion

In this paper, we have investigated the behavior of GaN/AlGaN MIS-HEMTs under forward gate bias stress. Our experimental approach consists of recording capacitance or current transients of the devices at a constant bias and for various values of temperature. From this measurement, it is possible to calculate the temporal evolution of the threshold voltage shift, which is proportional to the amount of charge trapped at the interface. By using a physical model for charge trapping based on NMP transitions, we can extract the distribution of the activation energy of the dominant defects.

We have applied this method to two samples with different AlGaN/SiN interface properties. Forward gate bias stress experiments on devices with a standard interface have revealed the presence of trap states with a broad distribution of activation energies over a range from 0.1 to 0.8 eV,

[1]Our previous calculation contained an error which lead to an apparent activation energy of 0.6 eV, rather than the correct apparent activation energy value of 0.4 eV.

with an average density of 10^{13} cm^{-2}. This gives rise to a broad time response behavior, leading to a logarithmic time evolution of the voltage drift for temperatures ranging from −190 °C to 200 °C. On the contrary, the activation energy spectrum of the test structures with a fluorinated AlGaN/SiN interface is compatible with a normal distribution with mean 0.32 eV, standard deviation 0.09 eV, and maximum density of 8×10^{13} cm^{-2}eV^{-1}. The narrow distribution results in a faster response to gate bias stress and the higher density to a larger overall threshold voltage shift.

The results shown in this paper demonstrate the applicability of the experimental approach for devices with a very different trapping behavior. The extraction of the density of states as a function of the activation energy allows for a physically accurate interpretation of the data, which does not require any further assumption or any prior knowledge about the distribution of the defects.

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