# On the Impact of the Gate Metal Work-Function on the Charge Trapping Component of BTI

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***Abstract*— We investigate BTI charge trapping trends in high-k metal gate (HKMG) stacks with a variety of work function metals. Most BTI models suggest charge trapping in oxide defects is modulated by the applied oxide electric field, which controls the energy barrier for the capture process, irrespective of the metal work function. However, experimental data show enhanced or reduced charge trapping at constant oxide electric field for different work function metal stacks. We ascribe this to a different chemical interaction of the metal stack with the dielectric, yielding different defect profiles depending on the process thermal budget. Furthermore, by employing the imec/T.U. Wien physics-based BTI simulation framework "Comphy", we also show that different metal work functions within a typical range of relevance (4.35-4.75eV) can yield a different charge state of the deep high-k defects, and can therefore have an impact on charge trapping kinetics during BTI stress, particularly in nMOSFETs.**

***Keywords—NBTI, PBTI, Multi-$V_{th}$, Replacement Gate, CMOS, BTI Models, Aging Simulations.***

## I. INTRODUCTION

System on Chip (SoC) application designs require the fabrication of MOSFETs with different threshold voltages ($V_{th}$) on the same wafer to best fulfill a range of system functions (e.g., high performance vs. low power). In recent Replacement Gate CMOS technologies, multiple device $V_{th}$ flavors (up to six different ones [1]) are realized, typically by depositing different work function metal stacks. It is hence of interest to investigate whether a different metal work function can affect the reliability of a given dielectric stack.

Most Bias Temperature Instability (BTI) models consider this aging mechanism to be primarily accelerated by the applied oxide electric field [2]. One would therefore expect a similar degradation to be observed in devices with different work function metals (WFM), if the gate stress test voltage is adjusted to maintain a given gate overdrive ($V_{ov}$=$V_G$-$V_{th0}$). While this expectation is confirmed in some literature reports [3,4], others have reported unexpected BTI trends: e.g., [5] reported that high-$V_{th}$ pMOS and nMOS, with metal work function close to Si mid-gap, can withstand larger operating overdrive voltages.

The recently proposed "hydrogen-release" model for the permanent component of NBTI [6] predicts an inherent impact of the metal work function on the pMOS degradation: interstitial hydrogen can be trapped in dielectric defect sites in different configurations, e.g., protons can bind to bridging oxygens in $SiO_2$ with a wide distribution of energy levels; a fraction of such defect levels, particularly in the vicinity of the gate, might move below the gate Fermi level—which therefore plays a crucial role—due to the application of an electric field; in this case the proton can be neutralized by a gate electron, and the hydrogen can be released as a neutral

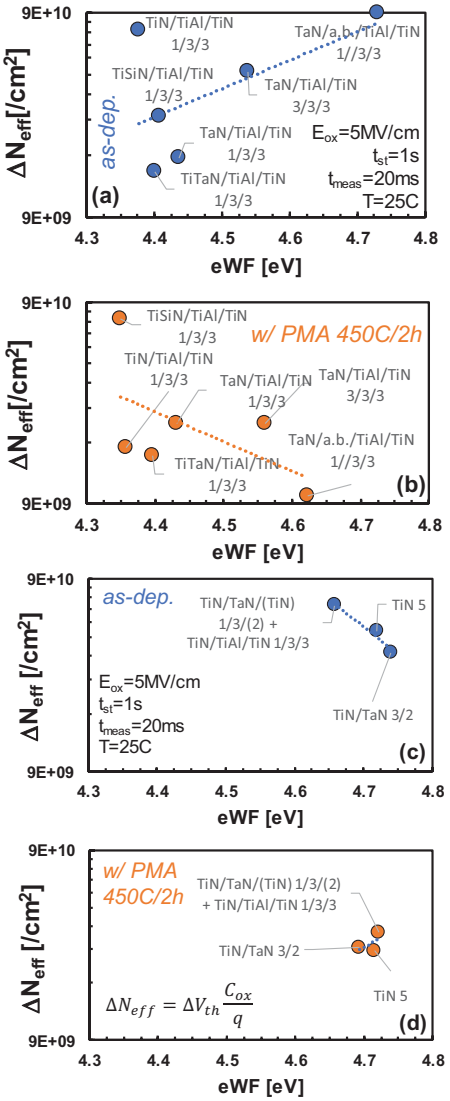


**Figure 1:** Charged oxide defect density estimated from BTI trapping measurements ($\Delta N_{eff}$ defined as $\Delta V_{fb}$*$C_{ox}$/$q$, where $\Delta V_{fb}$ is the flatband voltage shift measured after 1s stress at equivalent oxide field $E_{ox}$=$V_{ov}$/CET=5MV/cm, at room temperature) in **(a,b)** $n$-channel and **(c,d)** $p$-channel $Si/SiO_2/HfO_2$ MOS capacitors with various metal stacks (indicated by the data labels, which also report the thickness of each metal layer in nm), as-deposited (a,c), and after 450°C-2h PMA (b,d). At low thermal budget, the stacks with lower WF (i.e., nMOS low $V_{th}$, pMOS high $V_{th}$) show reduced $\Delta N_{eff}$ in PBTI stress condition and increased $\Delta N_{eff}$ in NBTI stress condition. In contrast, after a 450°C-2h PMA the stacks with lower WF show increased $\Delta N_{eff}$ in PBTI stress condition and slightly decreased $\Delta N_{eff}$ in NBTI stress condition. These contrasting trends suggest that the oxide reliability is controlled by the chemical interaction of a given metal stack with the underlying dielectric stack, as a function of the process thermal budget, instead of the metal work function per se (note: the latter is supposed to have a negligible impact when benchmarking at constant oxide electric field).

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specie; the released hydrogen quickly migrates due to diffusion (an extremely fast process; note the mechanism is assumed to be *reaction*-limited, and controlled by the activation energy of the hydrogen neutralization step) and gets trapped at the channel side where it either forms a new defect site or passivates a pre-existing defect, or induces the depassivation of a Si-H bond at the channel/oxide interface through a hydrogen dimerization process, Si-H+H → Si°+$H_2$, where Si° denotes a dangling bond at the interface. Note that dimerization is the only reasonable mechanism to explain how the strong Si-H bond could break during normal pMOS operation, as a direct H-removal would require an excessive energy of ~2.5eV [7-9].

While this model foresees a direct impact of the metal work function, at least on NBTI, this mechanism concerns mostly the permanent component of the degradation, which has been suggested to be smaller than the charge trapping component (i.e., the so-called 'recoverable' component) across the entire device lifetime [6]. In this work, we compare the BTI-induced $V_{th}$ shifts ($\Delta V_{th}$) measured after a short stress (i.e., focusing only on the 'recoverable' component of BTI) at fixed oxide electric field in HKMG stacks with a variety of metal stacks, covering a work function range of ~0.4eV. Contradicting trends are observed depending on the thermal budget applied after gate stack fabrication: e.g., for the as-deposited gate stacks, improved reliability is observed in low-$V_{th}$ devices; in contrast, if a post metal anneal (PMA) is performed, high-$V_{th}$ devices show best reliability. We ascribe this to *different chemical interaction of the considered metal stack with the dielectric, yielding different defect profiles depending on the process thermal budget*.

Furthermore, to isolate the pure impact of a different metal work function on charge trapping, we perform simulations with the imec/T.U. Wien BTI modeling framework Comphy ("Compact Physical" [10]). We observe that *a different metal work function can induce a different charge state of the deep high-k defects, and therefore affect charge trapping during stress, particularly in nMOSFETs.*

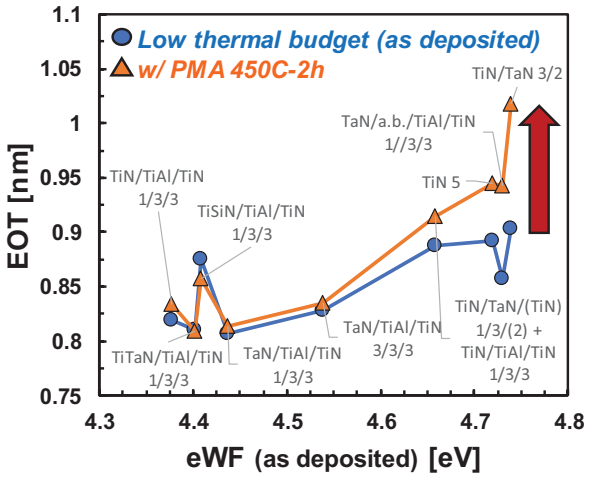


**Figure 2:** EOT and effective work function estimated from C-V measurements of Si/$SiO_2$/$HfO_2$ MOS capacitors with various metal stacks, as deposited and after 450ºC-2h PMA. While the low WF (TiAl-based) stacks show similar EOT before and after the PMA, the high WF (TiN-based stacks) show an EOT increase after PMA, possibly due to $SiO_2$ regrowth induced by oxygen movement within the gate stack favored by metals with higher electron affinities. These different trends suggest that different metals may interact differently with the dielectric stack during the fabrication steps following gate stack deposition, inducing different dielectric defect properties.

## II. Experimental Results

We fabricated *n*- and *p*-type MOS capacitors comprising a ~0.6nm $SiO_2$ interfacial layer, ~1.8nm $HfO_2$ high-k dielectric, and various TiN- and TiAl-based WFM stacks. A variety of work functions within a ~0.4eV range were obtained by employing different metal thicknesses and different bottom adhesion layers (TiN, TaN, TiSiN, TiTaN; stack composition and layer thicknesses in nm are noted in the data labels in Figs. 1-2, note "a.b." stands for "air-break"). For each gate stack, two set of capacitors were fabricated: one received only a 400ºC-5' hydrogen anneal after metal deposition ('as-deposited'), while the other received also a 450ºC-2h Post Metal Anneal (PMA) in nitrogen.

BTI charge trapping measurements were performed for increasing stress voltages at room temperature. To compare the various gate stacks, we evaluated the BTI-induced flatband voltage shift ($\Delta V_{fb}$) after 1s of stress at an equivalent oxide field of 5MV/cm. To account for slight EOT differences across the gate stacks, the $\Delta V_{fb}$ values were converted into an equivalent charge sheet $\Delta N_{eff}$ (=$\Delta V_{fb}$*$C_{ox}$/$q$).

Experimental data in **Fig. 1** show contradictory trends: in the 'as-deposited' capacitors, a low metal work function (i.e., nMOS low-$V_{th}$, pMOS high-$V_{th}$) is associated with a reduced PBTI trapping, and an enhanced NBTI trapping. In contrast, on the capacitors subject to a PMA, a low metal work function is generally associated with an enhanced PBTI trapping and a slightly reduced NBTI trapping. These results suggest that *the impact of a different WFM on charge trapping might be controlled by the chemical interaction of the metal stack with the underlying dielectric stack* [e.g., i) oxygen dynamics affected by the different metal electron affinities; ii) diffusion of metal species as Al in the dielectrics which might modify the defect properties], *yielding different oxide defect distributions as a function of the process thermal budget*, instead of by the work function itself. This hypothesis is qualitatively supported also by the different EOT increases measured after PMA in the stacks with different metals (**Fig. 2**; note that the high work function metal stacks seems to systematically induce larger EOT increase, possibly by favoring oxygen atoms movement within the gate stack due to their high electron affinity).

**Table I**

| | | Foundry 28 nm |
|---|---|---|
| Shallow $SiO_2$ | $N_t$ [/cm³] | 1.5 x10¹⁹ |
| | $\langle E_t \rangle \pm \sigma_{Et}$ [eV] | 1.13 ± 0.15 |
| | $\langle S \rangle \pm \sigma_S$ [eV] | 3.82 ± 1.36 |
| | R [1] | 0.407 |
| Shallow $HfO_2$ | $N_t$ [/cm³] | 5.52 x10²⁰ |
| | $\langle E_t \rangle \pm \sigma_{Et}$ [eV] | 1.2 ± 0.156 |
| | $\langle S \rangle \pm \sigma_S$ [eV] | 3.19 ± 0.77 |
| | R [1] | 0.587 |
| Deep $SiO_2$ | $N_t$ [/cm³] | 1.42 x10²⁰ |
| | $\langle E_t \rangle \pm \sigma_{Et}$ [eV] | -1.26 ± 0.25 |
| | $\langle S \rangle \pm \sigma_S$ [eV] | 5.63 ± 2.67 |
| | R [1] | 1.8 |
| Deep $HfO_2$ | $N_t$ [/cm³] | 2.95 x10²⁰ |
| | $\langle E_t \rangle \pm \sigma_{Et}$ [eV] | -0.17 ± 0.14 |
| | $\langle S \rangle \pm \sigma_S$ [eV] | 6.5 ± 1.99 |
| | R [1] | 0.514 |

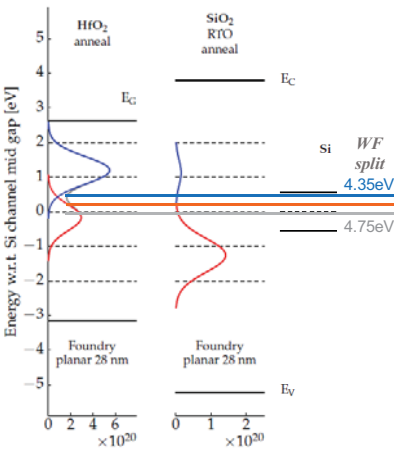


**Figure 3:** Sketch of the $SiO_2$ and $HfO_2$ shallow and deep defect bands as calibrated in [10] to model the PBTI and NBTI kinetics of a commercial 28 nm HKMG technology. The defect parameters are reported in the table. This defect model is used here to explore the intrinsic impact of a different metal work function on BTI kinetics by using the imec/T.U. Wien BTI simulation framework Comphy.

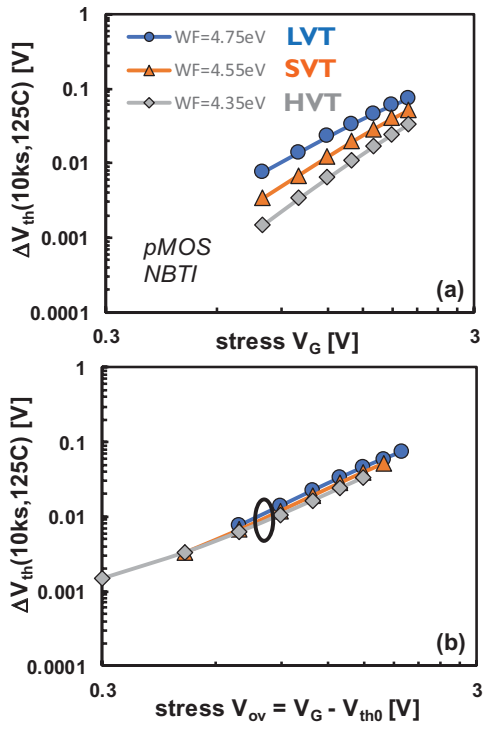


**Figure 4:** NBTI-induced $\Delta V_{th}$ after 10ks stress at 125ºC simulated in Comphy using the defect model calibrated on a commercial 28nm technology (cf. Fig. 3), for three different metal work functions [4.75, 4.55, 4.35eV, corresponding to pMOS Low $V_{th}$ (LVT), standard $V_{th}$ (SVT), and high $V_{th}$ (HVT) flavors, respectively], (a) for increasing stress $V_G$, or (b) replotted vs. the overdrive stress voltage ($V_{ov}$=$V_G$-$V_{th0}$) instead.

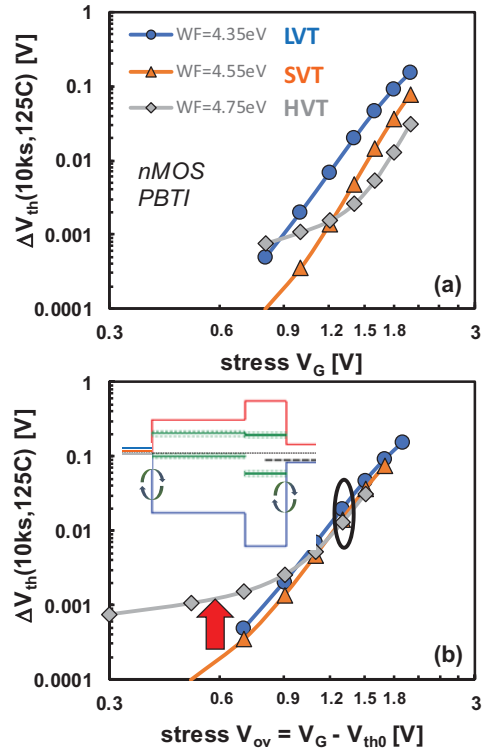


**Figure 5:** PBTI-induced $\Delta V_{th}$ after 10ks stress at 125ºC simulated in Comphy using the defect model calibrated on a commercial 28nm HKMG technology (cf. Fig. 3), for three different metal work functions [4.35, 4.55, 4.75eV, corresponding to nMOS Low $V_{th}$ (LVT), standard $V_{th}$ (SVT), and high $V_{th}$ (HVT) flavors, respectively], **(a)** for increasing stress $V_G$, or **(b)** replotted vs. the overdrive stress voltage ($V_{ov}$=$V_G$-$V_{th0}$) instead.

## III. COMPHY SIMULATIONS

To investigate the issue from a theoretical standpoint, we performed BTI simulations with Comphy [10]. We considered the oxide defect band model calibrated on a commercial 28nm HKMG technology (**Fig. 3**), and calculated the expected $V_{th}$ shifts ($t_{stress}$=10ks, T=125ºC) for increasing stress $V_G$, for three different WFM values commonly adopted in real technologies (4.75, 4.55, 4.35eV). For pMOS NBTI, while a larger $\Delta V_{th}$ is obviously observed at a given stress $V_g$ for low $V_{th}$ devices, the same $\Delta V_{th}$ is obtained when comparing at same stress $V_{ov}$ (i.e., compensating for the different initial $V_{th}$, **Fig. 4**), as expected from an electric field-driven charge trapping mechanism. In contrast, for nMOS PBTI a constant $\Delta V_{th}$ at same $V_{ov}$ is obtained only for high stress voltages (**Fig. 5**): at low $V_{ov}$ of relevance for logic operation (~0.6V, Fig. 5b), a larger $\Delta V_{th}$ is calculated when assuming a high WFM (nMOS high-$V_{th}$).

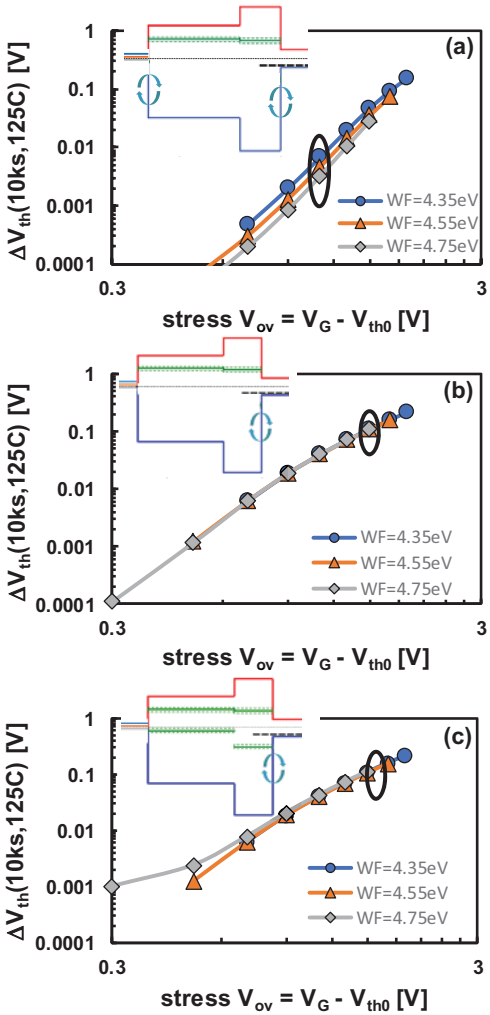


**Figure 6:** PBTI-induced $\Delta V_{th}$ after 10ks stress at 125ºC simulated in Comphy using the defect model calibrated on a commercial 28nm technology (cf. Fig. 3), for three different metal work functions [4.35, 4.55, 4.75eV, corresponding to nMOS Low $V_{th}$ (LVT), standard $V_{th}$ (SVT), and high $V_{th}$ (HVT) flavors, respectively], plotted vs. the overdrive stress voltage ($V_{ov}$=$V_G$-$V_{th0}$). The various interactions between oxide defects bands and charge reservoirs are selectively considered: **(a)** only shallow defect bands in $SiO_2$/$HfO_2$ interacting with both the channel and gate reservoirs; **(b)** only shallow defect bands interacting only with the channel; **(c)** shallow and deep defect bands interacting only with the channel.

We ascribe this unexpected behavior to the deep defect band in $HfO_2$, which is located only ~0.17eV below Si midgap (cf. Fig. 3; i.e., aligned to the Fermi level of a metal with work function 4.52eV). For a low or midgap WFM, this deep defect band is filled with electrons already at $V_{fb}$. However, when using a high WFM, some of these deep states can release their electron to the gate at equilibrium condition, and therefore become available to trap a channel electron during PBTI stress, contributing additional $\Delta V_{th}$. In agreement with this interpretation, the same $\Delta V_{th}$ at same $V_{ov}$ can be almost re-established in the simulations (**Fig. 6a**) by removing the deep oxide defect bands from the model (cf. Table I in Fig. 3), suggesting that the gate work function has almost a negligible impact on the occupancy of the shallow defect bands. If instead the gate interaction with the oxide defects is deactivated in the simulations, the same $\Delta V_{th}$ at same $V_{ov}$ is perfectly re-established, irrespective of the presence of the deep oxide defect bands (**Fig. 6 b-c**), confirming that the root cause of the different $\Delta V_{th}$ at same (low) $V_{ov}$ shown in Fig. 5b originates mainly from the impact of the gate Fermi level on the deep defect band occupancy.

## IV. Conclusions

We investigated BTI charge trapping trends in high-k metal gate (HKMG) stacks with a variety of work function metals. Most BTI models suggest charge trapping in oxide defects is modulated by the applied oxide electric field, which controls the energy barrier for the capture process, irrespective of the metal work function. However, experimental data showed enhanced or reduced charge trapping at constant oxide electric field for different work function metal stacks. We ascribed this to a different chemical interaction of the metal stack with the dielectric, yielding different defect profiles depending on the process thermal budget. Furthermore, by employing the imec/T.U. Wien physics-based BTI simulation framework "Comphy", we have also shown that a different metal work function can yield a different occupancy of the deep high-k defects, and can therefore have an impact on the charge trapping kinetics during BTI stress, particularly in nMOSFETs at low operating voltage of relevance for logic applications.

## References


[1] B. Sell, B. Bigwood, S. Cha, Z. Chen, P. Dhage *et al.*, "22FFL: A High Performance and Ultra Low Power FinFET Technology for Mobile and RF Applications", in IEEE *Proc.* IEDM, pp. 685-688, 2017;

[2] T. Grasser, "Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities", in Microelectronics Reliability, Vol. 52, pp. 39-70, 2012;

[3] C.-Y. Su, M. Armstrong, L. Jiang, S. A. Kumar, C. D. Landon *et al.*, "Transistor Reliability Characterization and Modeling of the 22FFL FinFET Technology", in IEEE *Proc.* IRPS, 6F8.1-7, 2018;

[4] W. Liu, Andreas Kerber, Fernando Guarin, Claude Ortolland, "Cap Layer and Multi-Work-Function Tuning Impact on TDDB / BTI in SOI FinFET Devices", in IEEE *Proc.* IRPS, pp. 2A4.1-5, 2018;

[5] B. Linder, A. Dasgupta, T. Ando, E. Cartier, U. Kwon *et al.*, "Process Optimizations for NBTI/PBTI for Future Replacement Metal Gate Technologies", in IEEE *Proc.* IRPS, pp. 4B1.1-5, 2016;

[6] T. Grasser, M. Waltl, Y. Wimmer, W. Goes, R. Kosik, *et al.*, "Gate-Sided Hydrogen Release as the Origin of "Permanent" NBTI Degradation: From Single Defects to Lifetimes", in IEEE *Proc.* IEDM, pp. 535-538, 2015;

[7] E. Cartier and J.H. Stathis, "Atomic hydrogen-induced degradation of the $SiSiO_2$ structure", in Microelectronic Engineering, Vol. 28, No. 3, pp. 1-4, 1995;

[8] A. Stesmans, "Dissociation kinetics of hydrogen-passivated Pb defects at the (111) $Si/SiO_2$ interface", in Physical Review B, Vol. 61, No. 12, pp. 8393-8403, 2000;

[9] J.H. Stathis, S. Mahapatra, and T. Grasser, "Controversial issues in Negative Bias Temperature Instability", in Microelectronics Reliability, Vol. 81, pp. 244-251, 2018;

[10] G. Rzepa, J. Franco, B. O'Sullivan, A. Subirats, M. Simicic *et al.*, "Comphy — A compact-physics framework for unified modeling of BTI", in Microelectronics Reliability, Vol. 85, pp. 49-65, 2018; http://www.comphy.eu