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Ultra-Fast Switching of a Free Magnetic Layer with out-of-Plane Magnetization in Spin-Orbit Torque Mram Cells

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Abstract

Continuous miniaturization of complementary metal-oxide semiconductor (CMOS) devices is one of the driving forces for the unprecedented increase of speed and performance delivered by modern integrated circuits However, a rapid increase of the stand-by power due to transistor leakages and the need to refresh the data in dynamic random access memory (DRAM) is becoming a pressing issue. The microelectronics industry is facing major challenges related to power dissipation and energy consumption, and the microprocessors' scaling will hit a power wall soon. An attractive path to mitigate the unfavorable trend of increasing power at stand-by is to introduce non-volatility in the circuits. The development of an electrically addressable non-volatile memory which combines fast operation, simple structure, and high endurance is essential to mitigate the increase of the stand-by power and to introduce instant-on architectures without the need of data initialization when going from a stand-by to an operation regime. Oxide-based resistive RAM (RRAM) possesses filamentary switching between on/off states and is thus intrinsically prone to significant resistance fluctuations in both on and off states. In addition, the endurance reported is only slightly higher than that in flash memory. For this reason, it is premature to consider RRAM at its current stage of development for digital applications. Since continuous conductance modulation is suitable for implementing analog synaptic weights, both filamentary and non-filamentary switching RRAM types are currently intensively investigated, particularly also for neuromorphic applications [1].

Spin-transfer torque magnetic RAM (STT-MRAM) is fast (10ns), possesses high endurance (10^{12}), and a simple structure. It is compatible with CMOS and can be straightforwardly embedded in circuits, e.g. [2]. High-density STT-MRAM arrays with 4Gbit capacities have been already demonstrated [3]. The availability of high-capacity non-volatile memory positioned close to high-performance CMOS circuits opens a new horizon in exploring conceptually new logic-in-memory [4] and computing-in-memory architectures for future artificial intelligence and cognitive computing.

Although it might be possible to introduce STT-MRAM in L3 caches, the memory is too slow for entering L1 and L2 caches currently mastered by static RAM (SRAM). In addition, rapidly increasing critical currents for switching STT-MRAM at 5ns and faster reduce the endurance to

that of the flash memory. The development of an electrically addressable non-volatile memory combining high speed (sub-ns operation) and high endurance is essential for replacing SRAM) in high-level caches of hierarchical multi-level processor memory structures with a non-volatile memory [4]. The spin-orbit torque MRAM (SOT-MRAM) with perpendicular magnetization combines non-volatility, high speed, and high endurance, which makes it suitable for applications in caches [5]. However, its development is still hindered by the need of an external magnetic field to guarantee deterministic switching [6].

We apply the two-pulse scheme previously proposed for switching of an in-plane structure [7]. The SOT due to the first 100ps pulse tilts the magnetization of the free layer in-plane perpendicular to the direction of the "Write pulse 1" (Fig.1). The SOT of the second consecutive pulse results in an additional precession of the magnetization in the part of the free layer under it, which is transferred to the remaining part of the free layer through the exchange interaction. Depending on the spin of this precession, the magnetization of the remaining part tilts up or down with respect to the in-plane orientation. The part under the wire of "Write pulse 2" follows the precession after the current is turned off, thus completing the switching. Results of the switching time calculations for several pulse durations as a function of the width of the second pulse wire are shown in Fig.2. We conclude that the fastest, sub-300ps switching, is achieved at around 30% overlap of the second pulse wire with the free layer.

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Footnotes

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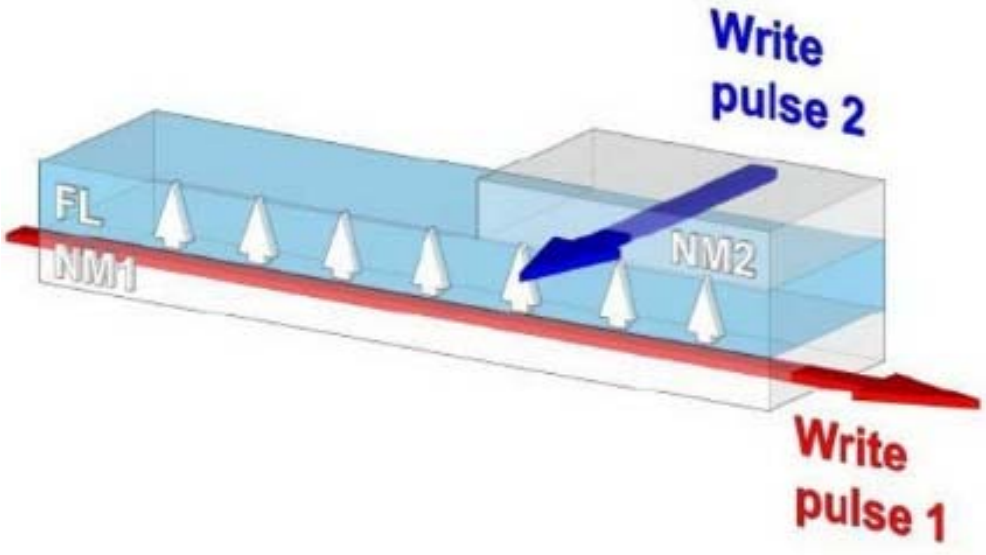

Fig.1: Perpendicular SOT-MRAM memory cell with a 52.5nmx12.5nmx2nm free layer

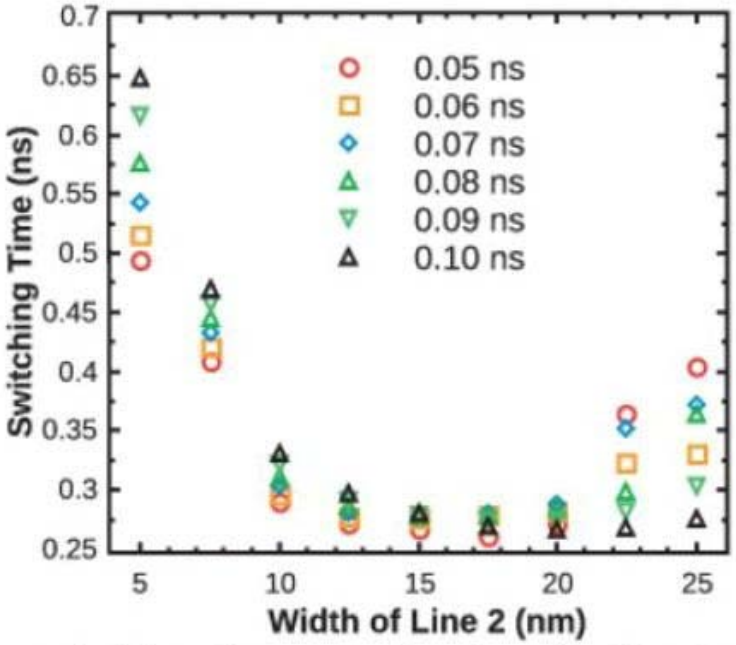

Fig.2: Switching time as a function the line 2 width, for several durations of the pulse 2, $I_1=I_2=100\mu A$