Actual Problems in the Field of Spintronics

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The dramatic increase of dynamic and stand-by power due to transistor scaling prompts for an introduction of non-volatility in charge based modern microelectronics. The electron spin as the other intrinsic degree of freedom of an electron is an apparent choice for emerging electronic switches and memories. Thanks to resolving several important fundamental problems including nonequilibrium spin injection, spin propagation, and purely electrical spin manipulation several spin-based transistors built with Si, InGaAs, and graphene/two-dimensional materials were recently demonstrated. However, these demonstrations are still far from being implemented as commercial devices, and basic research is continuing in this field.

Non-volatile magnetoresistive memory (MRAM) is currently introduced into a production phase by all major foundries. MRAM is based on a tunnel junction with ferromagnetic contacts, a magnetic tunnel junction (MTJ), with the MTJ resistance depending on the relative magnetization orientation. The essential quantum mechanical effects, such as the tunneling magnetoresistance (TMR) and the electrical current generated spin-transfer torques (STT) acting on the magnetization, ensure a strong coupling of the magnetization with the electric field and provide spin-to-charge and charge-to-spin conversion, respectively. MRAM based on MTJs with a high quality crystalline MgO tunnel barrier and the CoFeB/MgO interface-induced perpendicular magnetic anisotropy possesses a sufficiently large TMR, good retention, fast (down to 10ns) switching, and high endurance. MRAM technology is compatible with CMOS technology. Although MRAM is currently positioned as a replacement of flash memory, it offers faster operation and potentially can be used as an embedded main computer memory. Its simple structure, high endurance, compatibility with CMOS processing and non-volatility makes MRAM perfectly suited for monolithic three-dimensional integration in circuits, where high-performance CMOS logic layers are separated by non-volatile memories with low or no power consumption. As high-density STT-MRAM arrays with 4Gbit capacities have been already demonstrated, a combination of high-capacity embedded MRAM together with high-performance semiconductor logic leads to conceptually new logic-in-memory and in-memory computing architectures, which are highly attractive for artificial intelligence and cognitive computing.

To operate STT-MRAM at access time shorter than 5ns, high current densities through the tunneling oxide are needed, which reduces the endurance severely. For sub-ns switching required in first and second level processor's caches spin-orbit torque MRAM with perpendicular magnetization employing the spin Hall effect and/or spin-orbit torques (SOT) is a solution. SOT MRAM combines non-volatility, high speed, excellent retention, and long endurance. Although an integration of SOT MRAM on a 300mm CMOS wafer was recently reported, its large-scale application is still hindered by the need of an external magnetic field to guarantee deterministic switching. Nevertheless, recent developments to achieve deterministic switching without a magnetic field and to utilize new unconventional materials like topological insulators are excitingly promising.

In this talk, recent advances and remaining problems in the field of spintronics will be complemented by mathematical modeling approaches to physical phenomena driving the operation of modern spintronic devices.