Study of (correlated) trap sites in SILC, BTI and RTN in SiON and HKMG devices

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ABSTRACT

Recently, several experimental groups have found correlations in gate and drain current fluctuations. In this paper, by studying single trap activated leakage paths, both evidence and a refined 4-state defect model are provided, ascribing additional gate tunneling current in nm-FETs to thermally activated defect states. The model is capable of explaining both positive and negative correlations in gate and drain current RTN, but also the mostly uncorrelated nature of these drain and gate RTN signals.

I. INTRODUCTION

Enormous CMOS device improvements have been achieved over the last few decades, both by scaling device dimensions as by reducing the equivalent gate oxide thickness. As a consequence of this, degradation and fluctuations in drain and gate leakage currents become more pronounced, even in a way that they could seriously affect device performance. Phenomena such as bias temperature instabilities and RTN have been extensively studied over the last years [1].

Studying these phenomena in nm-sized FETs can give insight in the underlying physical principles—it is well established that in small devices, charge trapping and de-trapping of single defects can significantly alter the channel current, as shown in Franco et al.'s "*ultimate*" BTI experiment [2]. Also single leakage paths from the substrate to the gate electrode can be identified and extracted [3], as illustrated in Fig. 1. Finally, it has been shown [4-6] that correlated gate and drain current RTN exists in nFETs. Recently it was shown that even *in one single device*, both positive as negative correlations can be found [7].

A possible explanation for this latter phenomenon is the electrostatic screening in a direct tunneling model, affected by a discontinuous oxide band banding. Conversely, it has been shown by [8] that electrostatic screening alone cannot alter the gate leakage current more than a few percent. Another theory based on trap-assisted tunneling (TAT) was proposed in [9] and [10], where a trap in the oxide acts as a (thermally activated) stepping stone for tunneling towards the gate electrode, as illustrated in Fig. 2.

This paper shows that the full I_GV_G characteristics of individual trap site-induced leakage paths can be extracted and provides indications that *trap-assisted tunneling can described with a refined 4-state defect model,* in which the *transition rates are crucial* for describing all correlated gate leakage currents in nm-size FETs. Moreover, indications are given that most defects responsible for (de-)activating the SILC, also in HKMG devices, should be located in the SiO_2 interfacial layer.

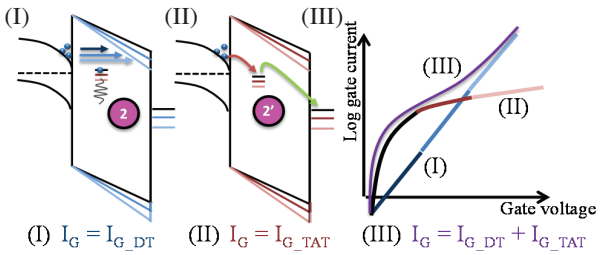


Fig 1. The schematic representation of the components of the gate leakage current. (I) A pre-existing or generated TAT-defect is charged and subsequently relaxed through multi-phonon emission. The trap cannot contribute to the gate leakage current and therefore only a direct tunneling current is measured. (II) The defect can actively contribute by trap-assisted tunneling (TAT). (III) This gate leakage path is superimposed on the direct tunneling gate leakage [9].

II. MEASUREMENT APPROACH

The measurements in this work were conducted on nanoscale nFETs (dimensions as indicated below) with SiON and HKMG gate stacks respectively. The stacks were specifically selected to have a comparable *physical* thickness. While the lateral dimensions of these devices are chosen small enough to increase the impact of single-defects on the drain current [2], the gate leakage current density has to be sufficiently high to be within measurement resolution at gate biases around the device's threshold voltage. The FET currents were simultaneously measured with a pair of Keithley 2636 units, either with a voltage sweep or with a constant voltage at a rate of 10 samples/s. All the measurements reported here were performed at 25°C unless noted otherwise. The experimental procedures are depicted in Fig. 3. Experiment A reveals the properties of trapped-charge induced BTI-shifts, the voltage dependence of a single leakage path, and the effect of stress on the generation/activation of these gate leakage paths, whereas experiment B reveals the time-dependent characteristics and

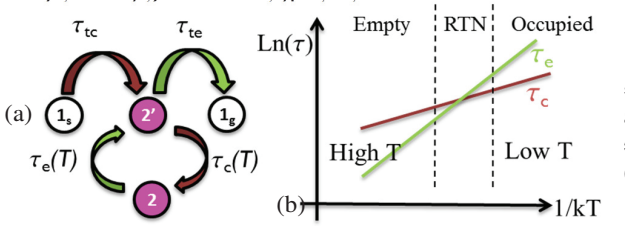


Fig 2. (a) The trap-assisted tunneling model as proposed by [9] and [10], and (b) typical temperature dependence of the time constants characterizing the transition between metastable states 2' and 2.

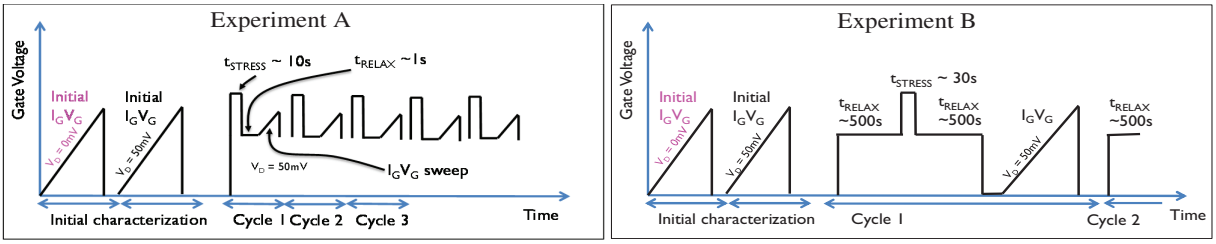


Fig 3. Schematic illustration of the experiments performed. Experiment A provides learning about the *stress dependent evolution* of the SILC as it is focused on measuring I_GV_Gs after intermittent stress cycles. The cycles are repeated 100 times. Experiment B focusses on the *time evolution and correlation* of both the gate and drain current after one short stress phase. During t_{RELAX} correlations between RTN in I_G and I_D are measured, as well as I_B.

only [Fig. 1(a)]. The latter can be found after scanning multiple devices. Note that the TAT-current is *not necessarily stress-induced*, but it can also be process-induced as shown for the initial I_GV_Gs in Fig. 4. An inflected gate leakage current (thus with a TAT component) can be observed in both SiON as HKMG devices, but remarkably, *it's not observed substantially more in the latter*, even though it's known that the high-k and SiO2/high-k interface defect density is at least one order of magnitude higher. This is an indication that the enabling trap for the TAT is located in the SiO_2 rather than in the high-k material, a conclusion similar to [11] and [12].

The voltage shift of the I_G curves in the linear regime of the MOSFET when increasing V_D from 0 to 0.05V reflects *the lateral position of the TAT path,* as explained in Fig. 5. The linear drop of the channel potential influences the local field in the gate oxide, and thus the leakage current through the TAT-path, as shown in Fig. 1. Therefore, the ratio of voltage shift of this single TAT-path (ΔV_{IG_TAT}) with the applied V_D thus determines the relative position of the trap in the channel:

$$x_{trap} = L_{channel} \frac{\Delta V_{IG\_TAT}}{V_D} \qquad (1)$$

This technique is a suitable alternative for the 's-ratio' technique in inversion [13], which relies on the channel resistance differences between the leakage path and drain/source junction, which become unmeasurable in nanoscale and thus ultra-short FETs.

IV. Link with Bias Temperature Instabilities

The introduction of HKMG devices also leads to positive BTI, visible as a positive shift of the I_D-V_G characteristic. The *TAT-paths after subsequent stresses are also influenced by the electrostatic charge accumulated in the oxide* due to this BTI-induced charge trapping [Fig. 6(a)]. It is therefore necessary to compensate for this shift. This can be done trace by trace, as the channel current is measured simultaneously.

Our experiments cannot conclusively determine a correlation between the impact of the defects on the drain current (i.e. the position w.r.t. the percolation path) and the screening of the gate current: the trapped BTI-charges will have an electrostatic impact on the TAT-path, but *not* according to their impact on the I_D, i.e. a trap close to a channel percolation path will not necessarily induce a large voltage shift on the TAT-path and vice versa.

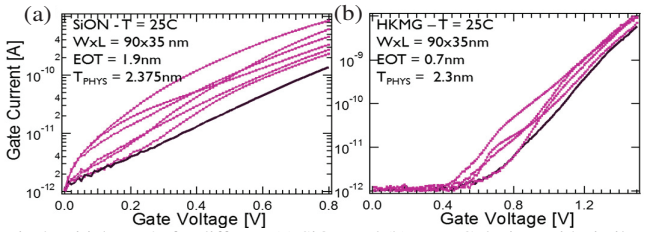


Fig 4. Initial I_DV_G's for different (a) SiON and (b) HKMG devices with similar physical thickness. In both cases, only a few devices show a near-perfect exponential leakage current (black lines). Other devices show a inflected I_DV_G, indicating the presence of at least one TAT-leakage path.

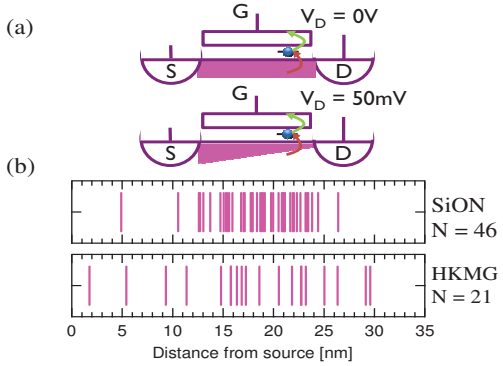


Fig 5. (a) The linear drop over the channel potential allows to extract the lateral position of the TAT-paths, using the V_D dependence of the I_{G_TAT} curves. (b) The SiON traces show a more centered distribution of TAT-paths than the HKMG devices.

However, based on BTI relaxation traces and simple charge sheet approximation (Fig. 6 [a]), we can conclude that our HKMG devices (90x28nm) can easily contain a few tens of trapped charges after stress, and *the 'average' BTI shift and I_G shift are nearly equal*, as shown in Fig. 6 (b). Therefore, in these devices, correcting the I_GV_G traces with a 'BTI' shift measured on the drain, as shown in Fig. 7, is a crude yet useful fix, as it helps to reveal the smaller ΔI_G TAT paths over the shifted background current.

Fig. 7(b) shows that the TAT-paths can both be induced or activated by stress, but *also de-activated* [Fig. 8(a)]. In some cases [Fig 8(d)], the TAT-paths *are activated and de-activated dynamically* during the I_GV_G sweep. It is well known that the generation of defects and thus potential TAT-paths is gate bias dependent (a high stress voltage will induce new defects), but also the activation and de-activation of such a path can show a *gate bias dependence during the sweep*. For the case of Fig. 8

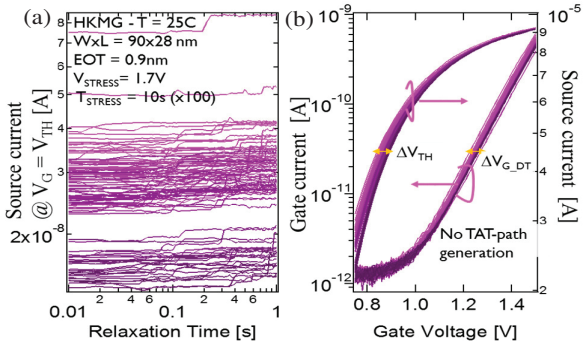


Fig. 6 (a) Experiment A performed on a HKMG device (WxL: 90x28nm, EOT = 0.9nm) for one stress voltage. Relaxation traces of the device after subsequent stresses shows tens of charges being trapped. (b) The I_DV_G and I_GV_G traces after the short relaxation show a comparable total V_{TH} shift for both drain and gate currents, but no TAT-paths have been created.

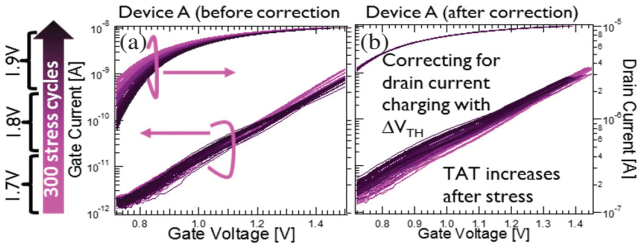


Fig 7. Experiment A performed on a HKMG device (WxL: 90x28nm, EOT = 0.9nm). The V_{TH} is quasi-*continuously* shifting with increasing stress voltage and stress cycles, visible in the I_D, due to the large number of trapped charges. The I_G shows mostly discontinuous steps which are not distinguishable in I_D. In (a) the trapped-charge screening effect on the TAT is apparent, while in (b) correcting for this V_{TH} shift, also illustrated in I_D, makes the TAT paths visible.

(b), the extracted probability for the TAT-path being disabled *increases* with gate bias (Fig 8 [c]).

Switching TAT-paths show RTN-like behavior if the gate leakage current is measured at constant bias, thereby proving that *one trap can activate or de-activate these leakage paths*. As the single path ΔI_G can be $\approx 2.5x10^{-11}$A [Fig. 8(b)], about $1.5x10^8$ charges/s should be captured and emitted to the gate by the oxide trap. The *slowest* time constant in the inelastic TAT process (thus either τ_{tc} and τ_{te}) is thus is the order of ns. The (in)elasticity of this tunneling current has no impact on the considerations in the proposed model.

At elevated temperature, the I_G traces become unstable and vary between every sweep. This RTN-like I_G is mostly not visible in I_D. Fig. 8(d) shows experiment A (Fig. 1) performed at a temperature typical for BTI experiments (125°C). More charge trapping—observed as V_{TH} shift in I_D—is apparent. Shifts up to 300mV are observed (not shown here), although the device remains fully functional.

Meanwhile, the gate leakage current is strongly increased to the point where the *individual TAT-paths become indistinguishable*. Their *activation and de-activation time constants are strongly temperature dependent* and decrease below measurement integration time, as predicted in the phonon relaxation model, and illustrated in Fig. 2 (b).

The results of experiment A and B show that PBTI of SiON is much lower than HKMG FETs. Typically, PBTI is attributed to defects in the high-k. In the latter, charge trapping occurs at much lower stress. Due to the defective nature of the high-k layer, phenomena as BTI and I_D RTN are abundantly visible, thereby inhibiting individual characterization, but the TAT-paths remain similar.

V. Gate and Drain Current Correlation

I_D and I_G are measured simultaneously and $\Delta I_G/\Delta I_D$ correlations are well within the measurement window. For the devices tested, *most discharging events in the drain show no*

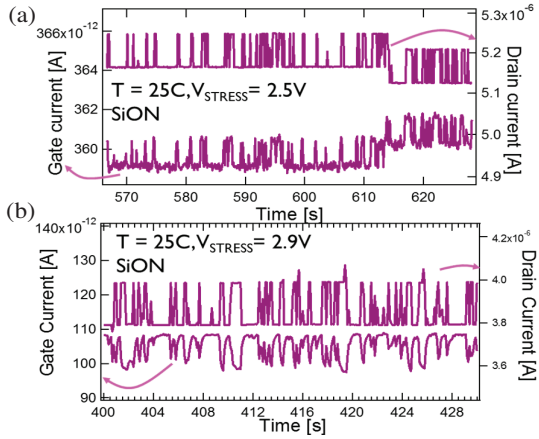


Fig 9 Both (a) positive and (b) negative I_D/I_G correlations are measured on separate SiON nFETs after stress. The negative correlation in (b) also shows signs of a second RTN path in the drain current, and is superimposed both on the low and the high state of the signal, but not visible in the gate current.

effect on the gate current and vice versa. This is remarkable as it is generally assumed that PBTI is primarily caused by traps in the high-k and the SiO_2/high-k interface, far from the channel, so also charging these 'far' traps should have an impact on the drain current.

Apart from the discharging, single and multi-level RTN signals are visible, mostly in I_D. These signals are ideal for studying correlations in TAT-paths and BTI traps. The multi-level RTN traps can be distinguished and treated as separate traps, as long as the ΔI are deviating enough. In some cases, a correlated gate and drain RTN could be found, and remarkably both positively and negatively, as shown in Fig. 9.

Our model, explained schematically in Fig 10, can describe no, positive and negative I_G/I_D correlations for nFET devices, is consistent with the 4-state defect model as proposed by [14]. The no-correlation, which is mostly seen, is explained with an active TAT-path located near the channel. Even in its meta-stable position, the trap will have a net charge, as the time constant for inelastic tunneling from the channel towards the trap (1s →2') is smaller than the time constant to tunnel from the trap towards the gate (2'→1g). The net charge is then defined by the product of the occupancy probability and the defect charge state. The trap's de-activated complement state 2 is by definition also a charged defect state [Fig. 10(a)]. Therefore, *no net charging in the oxide occurred whilst activating or de-activating the TAT-path*.

Only the cases where the capture time is dominant (i.e. state 1s →2' is slowest, thus the trap located far from the interface) could show a *positive correlation between I_D and I_G*, [Fig. 10

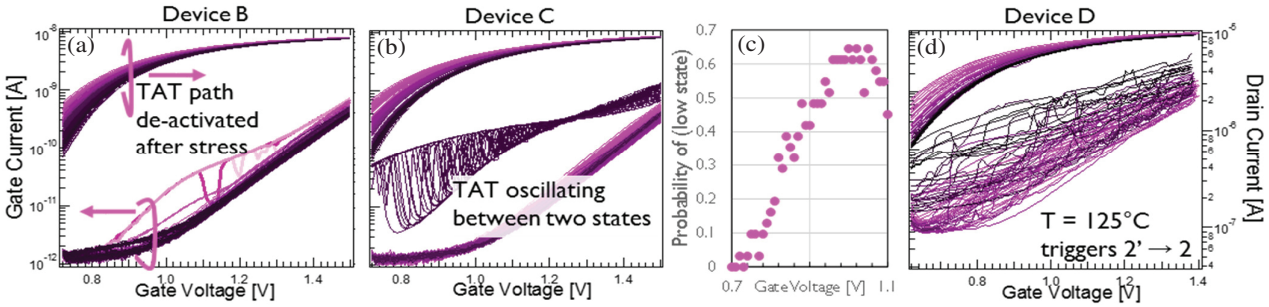
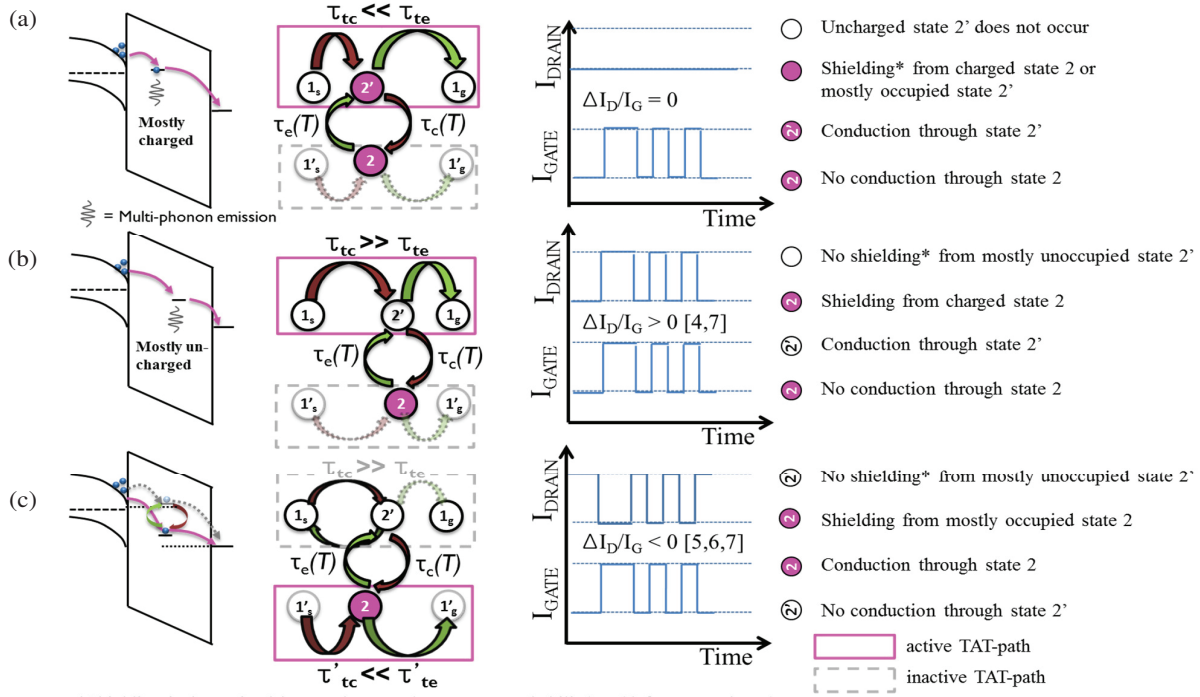


Fig 8. Experiment A performed on other HKMG devices (WxL: 90x28nm, EOT = 0.9nm). The V_{TH} is continuously shifting with stress voltage and cycles for all cases. The I_G shows mostly discontinuous steps which are not distinguishable in I_D. (a) TAT paths are oscillating and then de-activated after stress and (b) vice versa. (c) The gate voltage dependence of occupation probability of the two states in (b). (d) At high temperatures, the 2'↔2 transitions are occurring promptly and faster than the measurement integration time.



*Shielding is determined by net charge = (occupancy probability) x (defect state charge)

Fig 10. Model for TAT explaining no, positive and negative I_D/I_G correlations for nFET devices. The open symbol indicates the net charge of the defect state, the closed symbol vice versa. (a) The TAT needs an intermediate charged state 2', of which the occupancy probability can vary depending on the time constants τ_{tc} and τ_{te}. When the transition 2'→2 occurs, the TAT path (due to exchange between states 1 and 2') switches off. If $\tau_{tc}<<\tau_{te}$, state 2' is quasi continuously charged, making the 2' → 2 transition invisible for the channel current (= $\Delta I_D/\Delta I_G$ =0). (b) If $\tau_{tc} >> \tau_{te}$ (for states far away from the interface), state 2' is mostly unoccupied. In this case, the phonon relaxation of the TAT defect towards state 2 *will result* in a net charge difference observable in I_D. We therefore find a *positive* RTN correlation ($\Delta I_D/\Delta I_G$ >0). (c) Negative correlations are explained by favorable transitions between the *defect states* $1'_g/1'_s$ and 2. State 2 (the defect state after reconfiguration after electron capturing) *also has to be a net charged state*. Thus, for inverse correlation, the transition rates $\tau'_{tc} << \tau'_{te}$ between the secondary states are 1) much shorter and 2) opposite in their magnitudes: $\tau_{tc} >> \tau_{te}$.

(b)]. These correlations were already experimentally shown by [4] and [7] and are confirmed in these measurements.

Also the negative correlation observed earlier in [5-7] and now seen here, cannot just be explained with a TAT scheme and neither with direct electrostatic interaction. A plausible explanation for these correlations is by favorable transitions between the secondary defect states $1'_g/1'_s$ and 2. The transition rates $\tau'_{tc} << \tau'_{te}$ between the secondary states are 1) much shorter and 2) opposite in their magnitudes: $\tau_{tc} >> \tau_{te}$. The transition rate τ_c *towards the secondary defect state* has to be short as state 2' is quasi unoccupied.

In both correlated cases, an indirect gate voltage dependence is expected ascribed to a change in occupancy probability of state 2' influencing the 2'→2 transition, due to typical voltage dependency of BTI parameters τ_c. This gate bias dependence can be further investigated with noise or RTN measurements.

VI. Conclusions

Extended analysis of currents on all terminals of nanoscaled devices yields large insight in TAT/SILC, RTN and BTI mechanisms we propose a model capable of explaining the measurement observations, and in particular the positive and negative I_D and I_G correlations.

VII. References

[1] W. Goes, M. Toledano-Luque, O. Baumgartner, M. Bina, F. Schanovsky, B. Kaczer and T. Grasser, "Understanding correlated drain and gate current fluctuations", in Proc. of IPFA, pp. 51-56, July 2013.

[2] J. Franco, B. Kaczer, B,, M. Toledano-Luque, P.J. Roussel et al., "Impact of Single Charged Gate Oxide Defects on the Performance and Scaling of Nanoscaled FETs", in Proc. IRPS, pp. 5A.4.1 - 5A.4.6, April 2012.

[3] R. Degraeve, B. Govoreanu, B. Kaczer, J. Van Houdt and G. Groeseneken, "Measurement and statistical analysis of single trap current-voltage characteristics in ultrathin SiON", in Proc. IRPS, pp. 360-365, 2005.

[4] M. Toledano-Luque, B. Kaczer, E. Simoen, R. Degraeve, J. Franco et al., "Correlation of single trapping and detrapping effects in drain and gate currents of nanoscaled nFETs and pFETs", in Proc. IRPS, pp. XT. 5.1 – XT. 5.6, April 2012.

[5] C-Y. Chen, Q. Ran, H. Cho, A. Kerber, Y. Liu et al., "Correlation of Id- and Ig-Random Telegraph Noise to Positive Bias Temperature Instability in Scaled High-κ/Metal Gate n-type MOSFETs" in Proc. IRPS, pp. 190 – 195, 2011.

[6] X. Ji, Y. Liao, C. Zhu, J. Chang, F.Yan, Y. Shi, and Q. Guo, "The Physical Mechanisms of Ig Random Telegraph Noise in Deeply Scaled pMOSFETs," in Proc. IRPS, pp. XT.7.1–XT.7.5, 2013.

[7] W . Liu et al, "Analysis of Correlated Gate and Drain Random Telegraph Noise in Post-Soft Breakdown TiN/HfLaO/SiOx nMOSFETs", in Electron Devices Letters, Vol. 35, No. 2, pp. 157-159, 2014.

[8] O. Baumgartner, M. Bina, W. Goes, F. Schanovsky, M. Toledano-Luque, B. Kaczer, H. Kosina and T. Grasser, "Direct Tunneling and Gate Current Fluctuations", in Proc. SISPAD, pp. 17-20, September 2013.

[9] M. O. Andersson, Z. Xiao, S. Norrman, and O. Engstrom, "Model based on trap-assisted tunneling for two-level current fluctuations in submicrometer metal—silicon-dioxide—silicon diodes", Phys. Rev. B., Vol 41, pp. 9836-9842, 1990.

[10] B. Kaczer, M. Toledano-Luque, W. Goes, T. Grasser and G. Groeseneken, "Gate Current Random Telegraph Noise and Single Defect Conduction", in Microelectronic Engineering Volume 109, pp. 123–125, September 2013.

[11] T. Kauerauf, Robin Degraeve, Lars-Åke Ragnarsson, Philippe Roussel, Sahar Sahhaf, Guido Groeseneken, "Methodologies for sub-1nm EOT TDDB evaluation" in Proc. IRPS, pp. 7-16, 2011.

[12] G. Bersuker, D. Heh, C. D. Young, L. Morassi, A. Padovani, L. Larcher and K. S. Yew, "Mechanism of high-k dielectric-induced breakdown of the interfacial SiO2 layer", in Proc. IRPS, pp. 373-378, 2011.

[13] F. Crupi, B. Kaczer, R. Degraeve, A. De Keersgieter and G. Groeseneken, "Location and Hardness of the Oxide Breakdown in Short Channel n- and p- MOSFETs", in Proc. IRPS, pp. 55-59, 2002.

[14] T. Grasser, H. Reisinger, P.-J. Wagner, F. Schanovsky, W. Goes, and B. Kaczer, "The Time Dependent Defect Spectroscopy (TDDS) for the Characterization of the Bias Temperature Instability", in Proc. IRPS, pp. 16-25, 2010.