Hot-Carrier Degradation in FinFETs: Modeling, Peculiarities, and Impact of Device Topology

A. Makarov[1], S.E. Tyaginov[1–3], B. Kaczer[2], M. Jech[1], A. Chasin[2],
A. Grill[1], G. Hellings[2], M.I. Vexler[3], D. Linten[2], and T. Grasser[1]

[1]TU Wien, Vienna, Austria; [2]imec, Leuven, Belgium; [3]A.F. Ioffe Inst., St.-Petersburg, Russia

Abstract: We perform a comprehensive analysis of hot-carrier degradation (HCD) in FinFETs. To accomplish this goal we employ our physics-based HCD model and validate it against experimental data acquired in n-FinFETs with a channel length of 28 nm. We use this verified model to study the distribution of the trap density across the fin/stack interface. The methodology is applied to analyze the effect of transistor architectural parameters, namely fin length, width, and height, on HCD. Our results show that at the same conditions HCD becomes more severe in shorter devices and in transistors with wider fins, while the impact of the fin height on the damage is weak. Finally we demonstrate that a proper HCD description can be achieved only with a physics-based model.

Introduction

Properly tackling reliability issues is highly required for introduction and optimization of novel transistor nodes. Although the problem of device reliability includes a number of concomitant phenomena, for the most recent transistor topology, the FinFET architecture, hot-carrier degradation (HCD) was reported to be the most detrimental one [1]. Thus, proper understanding and modeling of HCD in FinFETs becomes a crucial task.

Whilst during recent years HCD in FinFETs was a subject of extensive experimental [2–4] and modeling studies [5, 6], a detailed understanding of HCD in these devices is still missing. For instance, substantial experimental efforts have been devoted to the problem of device geometry optimization needed to suppress HCD. In this context, consensus on the optimal fin width needed to alleviate HCD has not been reached. Indeed, some groups suggest that HCD becomes more severe in devices with wider fins [3, 7], while other researchers show the opposite trend [2, 8]. As for the simulation aspect, some models for HCD in FinFETs use the impact ionization rate as a metric for hot-carrier damage [5]. This approach seems doubtful because HCD is driven by Si-H bond dissociation, the rate of which has a substantially different functional form than that for impact ionization [9]. In modern devices the operating voltage is scaled below 1.0 V and under these conditions impact ionization is negligible and corresponding models cannot predict HCD. Up to now, many simulation approaches have been empirical or at best phenomenological [6, 10]. As a consequence, they fail to capture HCD at operating conditions when the physical mechanisms behind this detrimental effect are completely different as compared to stress conditions [9].

We apply our detailed physical HCD model [11, 12] to thoroughly analyze HCD in FinFETs. To validate this model vs. measurement data we employ the actual transistor geometry and dimensions (Figs. 1-5), while for studying the effect of the device architecture on HCD we use three series of virtually fabricated (simplified) FinFETs with varying gate lengths (L_G), fin widths (W_{fin}), and fin heights (H_{fin}), Figs. 6-11. We pay special attention to the localization of hot-carrier damage and to studying the interface state density (N_{it}) throughout the fin/dielectric interface.

Experimental

To acquire HCD data we used n-channel FinFETs with a gate length of $L_G = 40$ nm (channel length ~28 nm), Fig. 1, with operating and threshold voltages of $V_{dd} = 0.9$ V and $V_{th} \sim 0.4$ V. The high-k gate stack consists of an interfacial SiO_2 layer and a HfO_2 film and has an EOT of 1.2 nm.

These FinFETs were subjected to hot-carrier stress close to the worst case conditions typical for scaled transistors, i.e. at $V_{gs} \sim V_{ds}$. Note, however, that we chose V_{ds} values of 1.6, 1.7, 1.8 V, while V_{gs} was adjusted to ensure that the transistor overdrive voltage $V_{gs} - V_{th}$ is equal to V_{ds}. Thus, three combinations of stress voltages were used: $V_{ds} = 1.6$ V, $V_{gs} = 1.7$ V; $V_{ds} = 1.7$ V, $V_{gs} = 1.8$ V; and $V_{ds} = 1.8$ V, $V_{gs} = 1.9$ V. To assess HCD we monitored the change in the linear drain current ($I_{d,lin}$, measured at $V_{ds} = 0.05$ V and $V_{gs} = 0.9$ V) vs. stress time t up to ~2 ks, see Fig. 5 which shows normalized $\Delta I_{d,lin}(t) = |I_{d,lin}(t) - I_{d,lin}(0)|/I_{d,lin}(0)$ values. Let us also note that in our recent work [13] we checked whether positive BTI contributes to the damage in FinFETs fabricated by the same process which were stressed at high V_{ds}, V_{gs}. We concluded that at high V_{ds} the recoverable component of degradation is negligible and the PBTI contribution can be ignored (cf. [1]).

The Modeling Framework

Our HCD model [11, 12] considers the cumulative contribution of all carriers in the ensemble toward Si-H bond dissociation. Carriers characterized by low energies (cold carriers) can trigger multiple vibrational excitation of the bond which eventually results in its rupture (the multiple-carrier mechanism) [14]. In contrast, hot carriers have energy high enough to dissociate the bond in a single strike, i.e. induce the single-carrier mechanism. Thus, proper modeling of the rates of these mechanisms (and their superpositions [11, 15]) should be based on the carrier energy distribution function (DF) [9, 16, 17]. Therefore, the carrier DF is the core ingredient controlling HCD. It is important to emphasize that many HCD models use the electric field, the average carrier energy or the impact ionization rate as a metric of HCD [9]. However, by comparing N_{it} profiles extracted from charge pumping data with those simulated by our model we unequivocally showed previously that only the bond-breakage rates calculated using the carrier DFs can properly describe HCD [18].

To compute these DFs, our HCD model uses the deterministic Boltzmann transport equation solver ViennaSHE based on the spherical harmonics expansion method, which captures full-band effects, different energy exchange mechanisms including scattering at ionized impurities, impact ionization, as well as carrier-phonon and carrier-carrier interactions [19]. ViennaSHE also includes an approximation similar to the density gradient method used to describe carrier confinement in nanoscale devices [20]. For calculation of DFs it is necessary to have an accurate device structure available. Thus, the architecture of the FinFET used for HCD experiments was generated by the Sentaurus Process simulator coupled with the device simulator MINIMOS-NT in the GTS framework [21] and used to mimic measured current-voltage characteristics.

In addition, we virtually generated three series of simplified n-FinFETs with varying parameters L_G, W_{fin}, and H_{fin}: **(1)** $L_G = 23$, 29, 32, 35 nm and $W_{fin} = 8$ nm, $H_{fin} = 30$ nm; **(2)** $W_{fin} = 8$, 10, 15 nm and $L_G = 29$ nm, $H_{fin} = 30$ nm; and **(3)** $H_{fin} = 25$, 30, 35 nm and $L_G = 29$ nm, $W_{fin} = 8$ nm. These devices have geometries very similar to the real device, albeit simplified in order to reduce the computational expense required

for HCD simulations. E.g. instead of using a trapezoidal shape of the fin (as in the real FinFET, Fig. 1) these simplified devices have rectangular fins (Fig. 6). Thus, the simulation mesh contains a dramatically smaller number of mesh points.

After the DFs are calculated at all mesh points we use them to model the trap generation rates. The Si-H bond dissociation reaction is assumed to occur via the stretching mode with the corresponding activation energy, which is considered as a normally distributed quantity with the mean value of $\sim$2.6 eV [12] and the standard deviation being a fitting parameter in the model (0.22 eV is used in this work). Another process-dependent parameter is the concentration of passive Si-H bonds in a pristine device. Other parameters, such as the reaction cross sections for the multiple- and single-carrier bond-breakage processes and other quantities related to the bond energetics are assumed to be fixed in the model [12].

Ultimately, the bond-breakage rates allow us to evaluate the density $N_{\rm it}$ at each mesh point of the Si/SiO_2 interface and at an arbitrary stress time step. These $N_{\rm it}$ distributions are then used to model the degradation traces of device characteristics such as $\Delta I_{\rm d,lin}$. Note that although self-heating is important for FinFET reliability [1] our HCD simulations were performed at constant temperature. This can be the reason of very small discrepancy between experimental and simulated $\Delta I_{\rm d,lin}(t)$ traces visible in Fig. 5.

Results and Discussion

Electron DFs calculated for the real device stressed at $V_{\rm ds}$ = 1.6 V, $V_{\rm gs}$ = 1.7 V and $V_{\rm ds}$ = 1.8 V, $V_{\rm gs}$ = 1.9 V are given in Fig. 2. These DFs are plotted for three different positions along the channel: near the source, in the middle of the fin, and at the drain (Fig. 1). The behavior of DFs is typical: they are non-equilibrium and have a plateau visible at medium and high energies followed by high-energy tails (cf. [11, 12]).

Interestingly, the density $N_{\rm it}$ becomes higher close to the top of the fin, Fig. 3. Such a trend is related to the strong vertical component of the electric field which heats the carriers not only in the x (source-drain) direction but also along the y (vertical) axis, as already suggested in [3]. This important result allows one to analyze the location of the most degraded spot in the device. Fig. 4 shows the evolution of $N_{\rm it}(x)$ profiles with stress time and applied bias along the top/sidewall edge (as in Fig. 2) where HCD is strongest. One can see that the $N_{\rm it}$ front propagates with time inside the channel while short-term HCD is determined by the drain peak, as discussed in [11].

Fig. 5 shows that our model represents experimental traces with very good agreement using an almost identical set of model parameters as for HCD modeling in planar short-channel transistors [12] and in high-voltage devices [22]. The two only parameters to be optimized are the concentration of virgin Si-H bonds and the technology-dependent bond-breakage energy dispersion.

The DFs of simplified devices calculated for the series with varying $L_{\rm G}$ near the drain at the top/sidewall fin edge are very similar to those of the real FinFET (cf. Fig. 2). At a first glance, one can conclude that HCD should be more severe in longer devices because in this case the high-energy tails of DFs are more populated. However, the main contribution to HCD is made by carriers which form the plateau visible at moderate/high energies [12] and in this range DFs have larger values for shorter $L_{\rm G}$. The $N_{\rm it}$ distribution (Fig. 8) computed with these DFs for $V_{\rm ds} = V_{\rm gs}$ = 1.9 V, $t \sim$ 200 s and using the parameter set of the calibrated model is qualitatively similar to the $N_{\rm it}$ concentration of the real device, as discussed next.

The $\Delta I_{\rm d,lin}(t)$ traces obtained for devices with different gate lengths $L_{\rm G}$ stressed at $V_{\rm ds} = V_{\rm gs}$ = 1.9 V are summarized in Fig. 9 (left) and are consistent with the change of the DFs due to $L_{\rm G}$ variations. The trend that HCD becomes less pronounced in longer transistors corresponds to previously reported results, see e.g. [23]. Concerning the effect of $W_{\rm fin}$ on HCD, the $\Delta I_{\rm d,lin}$ values become higher in devices with wider fins. As we already discussed, there is no agreement in the literature on this issue. Our trend corresponds to results reported in [2, 8] and contradicts findings of [3, 7]. We suppose that this problem is rather complex and the HCD behavior due to $W_{\rm fin}$ variations strongly depends on the device geometry, as it was recently shown for the temperature behavior of HCD [12]. Finally, the impact of $H_{\rm fin}$ variations on the $I_{\rm d,lin}$ degradation is weak but still discernible, i.e. HCD becomes slightly stronger in FinFETs with higher fins.

All trends visible in Fig. 9 are supported by the corresponding $N_{\rm it}(x)$ dependences computed for $t \sim$ 1.8 and 2 ks (Fig. 10). Additionally, $\Delta I_{\rm d,lin}$ changes modeled for $V_{\rm ds} = V_{\rm gs}$ = 2.2 V (Fig. 11) reveal the same behavior as those presented in Fig. 9. One can see that $\Delta I_{\rm d,lin}(t)$ curves for 2.2 V are less steep than those for 1.9 V, especially for longer stress times. This is because at high voltages all available Si-H bonds near the drain are already broken and HCD is close to saturation (see [11]).

The discussed change of the time exponent is visible in long-term HCD traces obtained for real and simplified FinFETs stressed at $V_{\rm ds} = V_{\rm gs}$ = 1.0 V (close to the operating regime), see Fig. 12. This clearly demonstrates the need for a complex physics-based HCD model. Indeed, experimental HCD data are usually available in a stress time window limited by 10^5-10^6 s. Approximately at these times $\Delta I_{\rm d,lin}(t)$ starts to saturate and significantly changes its slope (Fig. 12). Therefore, if the device lifetime τ is extracted in the experimentally available time slot, such a procedure leads to spurious (underestimated) values of τ. Even more dramatic, the slope of HCD traces varies also with the applied bias (Fig. 12, left panel; cf. [24, 25]) and device geometry Figs. 9, 11, thereby making extrapolation of the τ from stress conditions to the operating regime questionable.

Fig. 13 summarizes the values of device lifetime extracted using our HCD model for two series of simplified devices. One can see that variations in device geometry result in a spread of τ values. FinFETs with wider fins have improved τ values, while device lifetimes aggravate with reduction of the gate length.

Conclusions

Using our physical model for hot-carrier degradation we performed a thorough analysis of this detrimental phenomenon in FinFETs. The model was validated against experimental HCD data acquired in an n-FinFET with a channel length of 28 nm. It is important to emphasize that for modeling HCD in FinFETs we used a very similar set of model parameters as for HCD modeling in planar MOSFETs and high-voltage devices. For the first time we calculated the distribution of the trap density over the fin/dielectric interface and showed the location of the most damaged spot. In addition to real devices we used three series of virtually fabricated FinFETs of an identical architecture but with varying gate lengths, fin widths, and fin heights. The validated model was applied to investigate the effect of these geometrical parameters on HCD. Quite naturally, HCD becomes more severe in shorter transistors. Device characteristics change less in FinFETs with narrower fins, while the fin height influences the HCD behavior insignificantly. Finally we showed that thorough device lifetime extraction is possible only by using a physical model for HCD and simplified empirical approaches have very limited applicability.

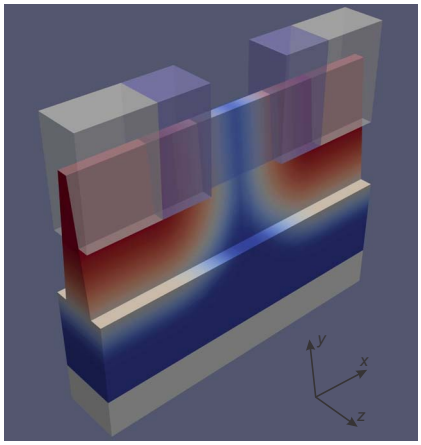


Figure 1: Schematic representation of the real FinFET used for HCD measurements and model verification.

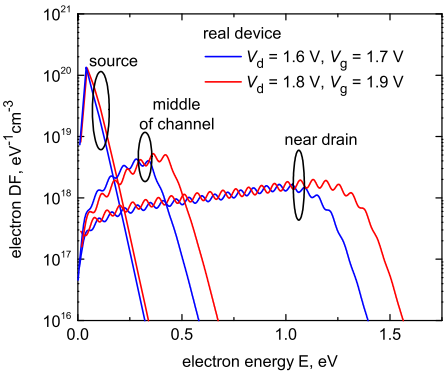


Figure 2: Electron DFs calculated for two combinations of V_{gs}, V_{ds}, at the edge between the sidewall and the top of the fin for three different positions: at the source, in the middle of the channel, and at the drain.

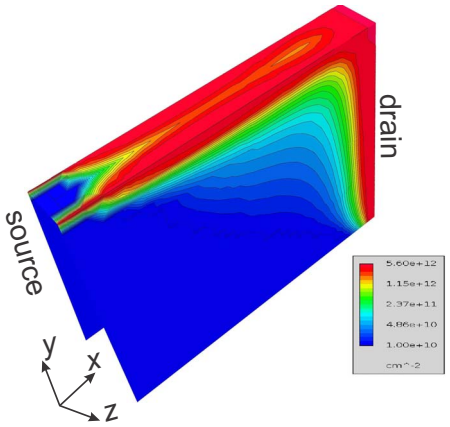
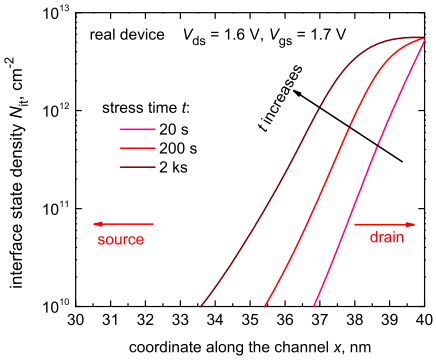


Figure 3: The N_{it} density throughout the fin/dielectric interface of the real device for $V_{ds} = 1.7$ V, $V_{gs} = 1.8$ V and $t \sim 200$ s.



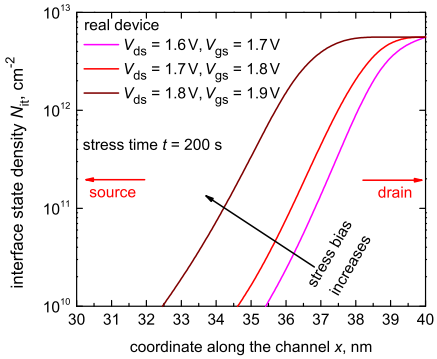


Figure 4: The evolution of the N_{it} density with stress time (left) and stress bias (right) for the real device. The N_{it} profile is shown for the same cut as DFs in Fig. 2. For the sake of visibility we show only the drain peak of N_{it} (the drain is at x =40 nm, source is at $x = 0$).

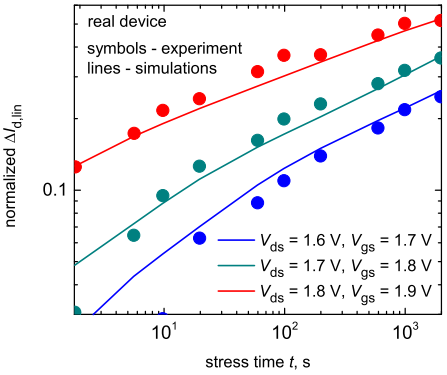


Figure 5: Measured and simulated $\Delta I_{d,lin}(t)$ traces for three stress conditions show very good agreement.

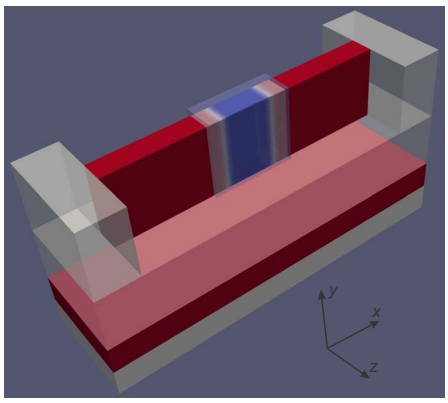


Figure 6: A sketch of the simplified FinFET.

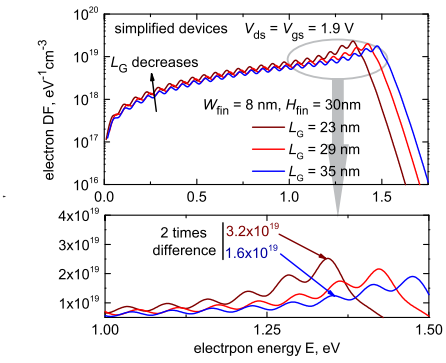


Figure 7: Electron DFs calculated for the series of simplified devices with varying L_G.

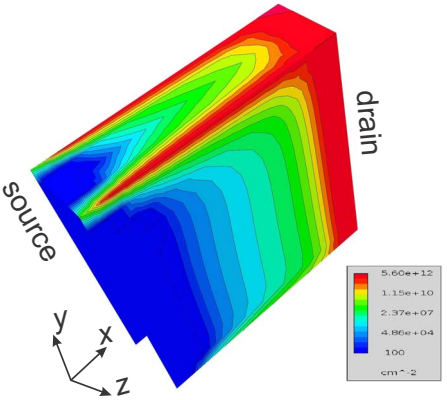
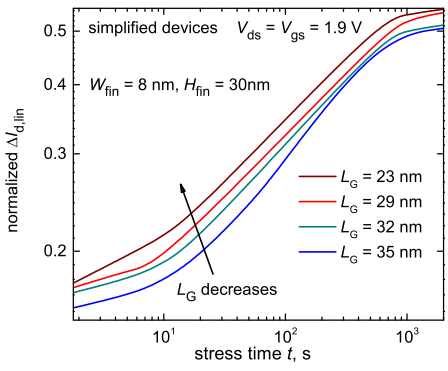
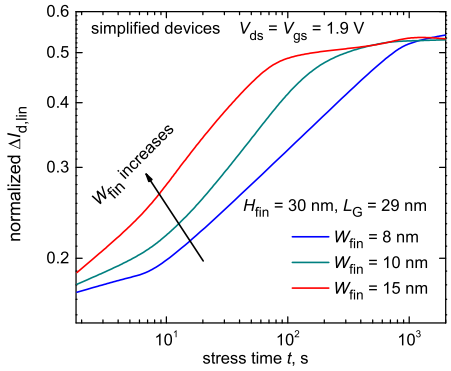


Figure 8: The N_{it} density throughout the fin/dielectric interface of the simplified device.





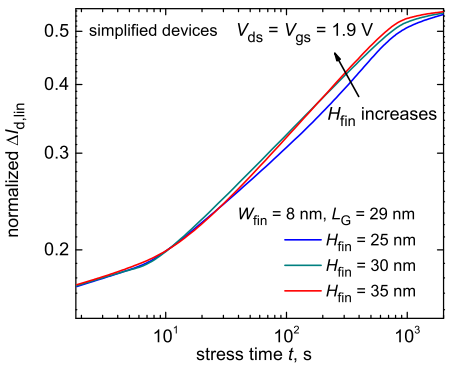


Figure 9: $\Delta I_{d,lin}(t)$ traces simulated for three different series of devices: with varying L_G, W_{fin}, and H_{fin} for $V_{ds} = V_{gs} = 1.9$ V.

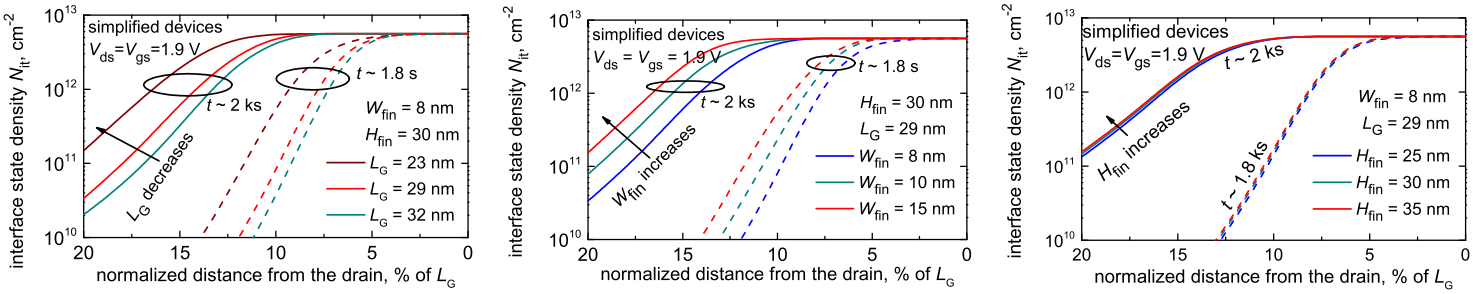


Figure 10: The $N_{it}(x)$ profiles simulated for three series of simplified devices with varying L_G, W_{fin}, and H_{fin} stressed under $V_{ds} = V_{gs} = 1.9$ V; stress times are ~1.8 s and ~2 ks. They are shown along the top/sidewall edge of the fin and x axis represents the distance from the drain (in % of L_G). One can see that the N_{it} front propagates deeper inside the fin at longer stress times and as the stress bias grows.

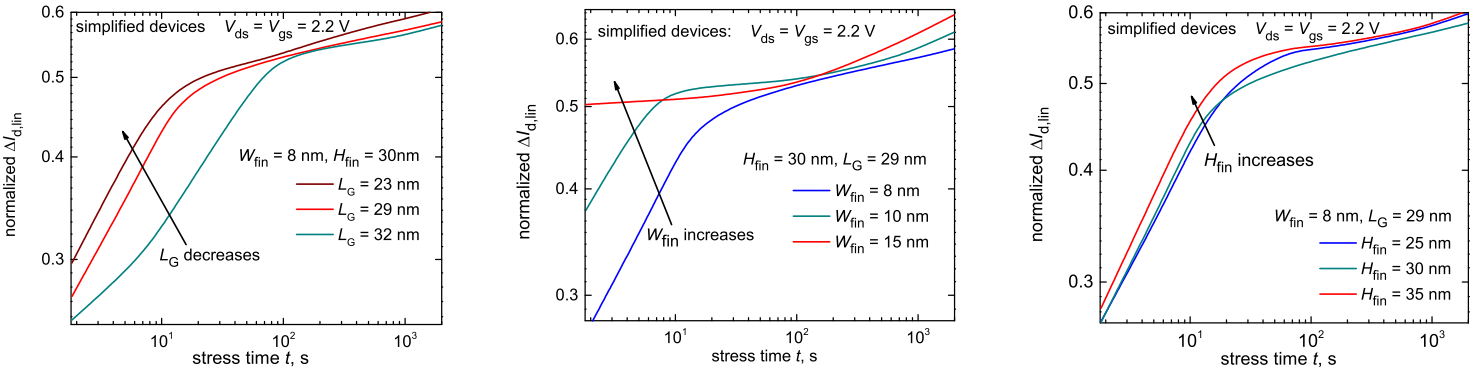


Figure 11: $\Delta I_{d,lin}(t)$ traces simulated for three different series of devices (with varying L_G, W_{fin}, and H_{fin}) for $V_{ds} = V_{gs} = 2.2$ V.

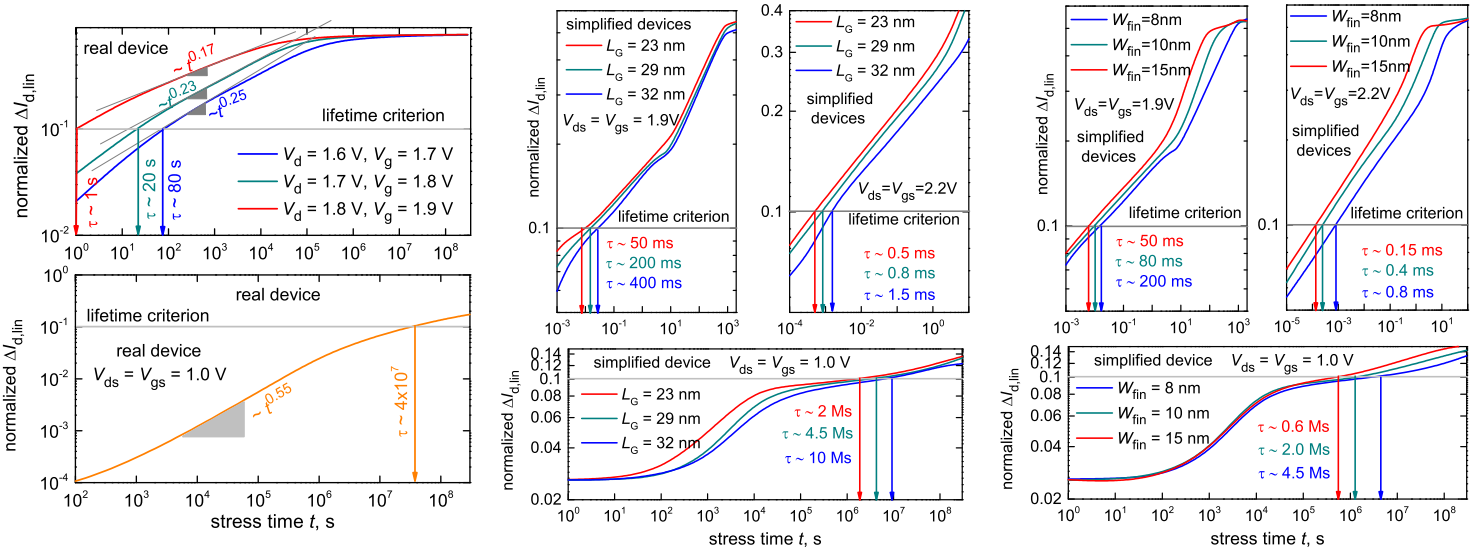


Figure 12: $\Delta I_{d,lin}(t)$ dependences calculated for the real device and two series (with varying L_G and W_{fin}; H_{fin} effects HCD insignificantly and corresponding data are not shown here) of simplified FinFETs. Data for stress conditions and for bias close to the operating voltage ($V_{ds} = V_{gs} = 1.0$ V) are plotted. In order to enable extraction of the device lifetime, these traces are obtained also for shorter stress times as compared to Figs. 9, 11.

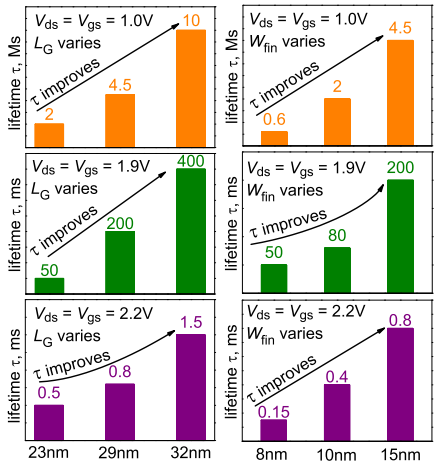


Figure 13: Summary of device lifetime values extracted for simplified FinFETs.

References:

[1] S. Novak *et al.*, IRPS 2015, p. 2F.2.1. [2] D. H. Lee *et al.*, IEEE EDL **32**, 1176 (2011). [3] S. Ramey *et al.*, IRPS 2013, 4C.5.1. [4] M. Cho *et al.*, IEEE TED **60**, 4002 (2013). [5] C. D. Young *et al.*, JVST-B **27**, 468 (2009). [6] I. Messaris *et al.*, Microel. Reliab. **56**, 10 (2016). [7] W. T. Chang *et al.*, IEEE TDMR **15**, 86 (2015). [8] D. W. Kim *et al.*, Microel. Reliab. **50**, 1316 (2010). [9] S. Tyaginov *et al.*, ECS Tran. **35**, 321 (2011). [10] Y. Wang *et al.*, IEEE/ACM Int. Symp. Nan. Arch. (2011), p. 175. [11] M. Bina *et al.*, IEEE TED **61**, 3103 (2014). [12] S. Tyaginov *et al.*, IEEE EDL **37**, 84 (2016). [13] A. Chasin *et al.*, IRPS 2016, p. 4B.4. [14] A. Bravaix *et al.*, IRPS 2009, p. 531. [15] Y. Randriamihaja *et al.*, IRPS 2013, p. 1. [16] A. Zaka *et al.*, SSE. **54**, 1669 (2010). [17] S. Reggiani *et al.*, IEEE TED **60**, 691 (2013). [18] I. Starkov *et al.*, JVST-B **29**, 01AB09 (2011). [19] K. Rupp *et al.*, IEDM 2011, p. 789. [20] K. Rupp *et al.*, J. Comp. El. **15**, 939 (2016). [21] http://www.globaltcad.com/en/products/minimos-nt.html. [22] P. Sharma *et al.*, IEEE TED **62**, 1811 (2015). [23] B. Kaczer *et al.*, IRPS 2015, 3B.5.1. [24] T. Grasser, Hot Carrier Degradation in Semiconductor Devices, Springer 2015. [25] D. Varghese *et al.*, IRPS 2010, p. 1091.