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PHYSICS OF SEMICONDUCTOR DEVICES

Impact of the Device Geometric Parameters on Hot-Carrier Degradation in FinFETs

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Abstract—The effect of the geometric parameters of Fin field-effect transistors (FinFETs) on hot-carrier degradation (HCD) in these devices is theoretically studied. To this end, a model is used, in which three subproblems constituting the physical phenomenon of HCD are considered: carrier transport in semiconductor structures, description of microscopic defect formation mechanisms, and simulation of degraded device characteristics. An analysis is performed by varying the gate length, fin width and height. It is shown that HCD becomes stronger under fixed stress conditions in transistors with shorter channels or wider fins, while the channel height does not substantially affect HCD. This information can be important for optimizing the architecture of transistors with the fin-shaped channel to suppress degradation effects.

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1. INTRODUCTION

The advent of transistors of three-dimensional architecture such as field-effect transistors (FETs) with a fin-shaped channel (FinFET), multigate FETs (MGFETs), and nanowire FETs (NWFETs) made it possible to overcome a number of undesirable effects preventing further miniaturization of the microelectronics components [1–3]. In particular, better channel control from the gate side and larger subthreshold slopes were achieved, hence, the ratio of ON/OFF currents was improved and power consumption was significantly lowered. Although very promising, these devices—as any novel transistor nodes—demonstrate a bunch of reliability issues. It includes a large variety of parasitic phenomena; however, as shown by various teams [4–6], degradation called hot-carrier degradation (HCD) is most destructive. This is first of all due to the fact that electric fields in the channel reach high values in nanoscale transistors even at operating voltages of 0.8–1.0 V, resulting in strong carrier acceleration to energies sufficient to break bonds at the silicon–insulator interface. Another important aspect typical of three-dimensional topologies is self-heating [7, 8]. This parasitic effect occurs because the FET channel is surrounded on all sides by an insulating layer with a low thermal conductivity, which results in a significant increase in the local lattice temperature under operating conditions, especially under high stress voltages.

The situation becomes even more complicated because the problem of reliability of the next FET generation should be solved at the same time as architecture optimization. In other words, both microscopic (doping profiles, insulator stoichiometric-composition variations, deformation stress at the interface, and others) and macroscopic (insulating-film thickness, gate length L_G, channel width and height, W_{fin}, H_{fin}, etc.) transistor parameters can and should be optimized to improve the device operating characteristics and suppress degradation effects, first and foremost HCD.

As for the latter aspect, numerous attempts have been undertaken (mostly in experimental studies) to analyze the effect of the parameter W_{fin} on HCD behavior in devices with a fin channel. However, consensus with respect to optimal W_{fin} has not been achieved. Indeed, it is suggested in some papers devoted to this problem that HCD becomes stronger in transistors with a wider channel [9–11], whereas other teams show the opposite tendency [7, 12, 13]. Attempts to simulate the effect of nanoscale width of the transistor channel were based on the use of the impact-ionization rate as a HCD metric [9, 14]. This approach seems doubtful, since the impact-ionization rate in those publications was calculated as a local function of the electric field. However, as we showed recently, the peak of the interface state generation rate during HCD and the electric field maximum are

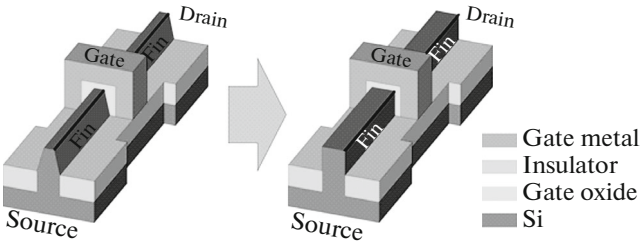

Fig. 1. Schematic diagram of FinFETs previously used for testing the model (left) and the effect of channel-geometry parameters under study on HCD (right).

shifted with respect to each other along the lateral coordinate [15]. Furthermore, impact ionization and silicon–hydrogen (Si–H) bond rupture (which is the mechanism driving HCD) are different processes and have thereby different dependences of their rates on the electric field and carrier energy.

In this paper, we perform numerical analysis of the effect of such geometric parameters of a FinFET as L_G, W_{fin}, and H_{fin}, on HCD in these devices. To achieve this goal, we use our physics-based model for hot-carrier degradation. This model was shown to describe with good accuracy $\Delta I_{d,\,\text{lin}}(t)$ degradation traces (here $I_{d,\,\text{lin}}$ is the linear drain current, while t is stress time) [16, 17].

2. CALCULATION PROCEDURE

Our HCD model [18–21] considers and describes three main aspects associated with the degradation caused by hot carriers: carrier transport in semiconductor structures, simulation of the kinetics of defect generation, and modeling of the characteristics of damaged devices.

To tackle the first task, the deterministic Boltzmann transport equation solver ViennaSHE is used. ViennaSHE employs the spherical harmonics expansion method to obtain the carrier distribucion function (DF) [22, 23]. The simulator incorporates the actual silicon band structure up to high energies, which is especially important to describe phenomena associated with hot carriers. Also, various scattering processes are taken into account, including impact ionization, scattering at a charged impurity and at the interface, as well as electron-photon and electron-electron interactions. We note that electron-electron scattering is one of the main mechanisms responsible for HCD in short-channel FETs [24, 25].

The description of HCD at the microscopic level is based on the concept that defects are generated by the breakage of initially neutral Si–H bonds under their bombardment with carriers. We consider the contributions of both hot and cold particles [26–31]. The former case corresponds to the "classical" HCD where the bond can be broken by the impact of one high-energy particle (single-particle mechanism). The contribution of cold carriers during defect formation consists in the excitation of the vibrational modes of the bond followed by its breaking (many-particle mechanism). For both mechanisms, defect generation rates were calculated based on the DFs obtained using ViennaSHE. These DFs are required to "distinguish" cold and hot carriers and determine their contributions to bond breaking. Our model considers all superpositions of the two mechanisms constituting the entire bond-breakage process, i.e., scenarios where the bond is initially excited by successive bombardment with cold particles (accordingly, the breaking energy efficiently decreases [20, 21]), and then is broken by a single particle with a high (but lower than in the single-particle process) energy.

The Si–H bond has two vibrational modes, i.e., stretching and bending ones. We believe that the bond is broken via the stretching mode with the breaking energy of $E_a = 2.6$ eV [21]. The concept is consistent to experimental results [32]. We also take into account statistical fluctuations of the parameter E_a, inevitable because of the amorphous nature of the insulator and the fact that the silicon-insulator interface is a disordered system.

Defect generation results in local distortions of device electrostatics (which can manifest themselves in a shift of the transistor threshold voltage). Charged states also play the role of scattering centers, which causes carrier-mobility degradation, hence, the drain-source current decreases. These effects are modeled using the device and circuit simulator MiniMOS-NT, which allows one to calculate changes of the device characteristics at each stress time step.

3. DEVICE ARCHITECTURE

The HCD model used in the present study was previously tested for several transistor types including also FinFET devices with the trapezoidal cross section of the channel [16, 17] (Fig. 1, left). Such a configuration corresponds to an actual FET; however, to quantitatively study the effect of geometric parameters, it is reasonable to simplify the shape of the fin cross section to a rectangle.

To analyze the effect of variations in the FinFET architecture, we consider three series of FinFETs with a fin channel shaped as a rectangular parallelepiped. In the first series, the gate length is varied, $L_G = 29$, 32, 35 nm (other parameters are fixed, $W_{\text{fin}} = 8$ nm, $H_{\text{fin}} = 30$ nm); in the second series, the channel width is varied, $W_{\text{fin}} = 8$, 10, 15 nm ($H_{\text{fin}} = 30$ nm, $L_G = 29$ nm); and in the last series, the fin height is varied, $H_{\text{fin}} = 25$, 30, 35 nm ($W_{\text{fin}} = 8$ nm, $L_G = 29$ nm).

The architecture of these transistors is almost identical to that of the devices in [17, 25], with the exception that the fin cross section is rectangular, rather than trapezoidal, as it was in the real FinFETs (see Fig. 1). This simplification is made to decrease the number of simulation grid elements and hence significantly reduce the time required to calculate the carrier energy distribution functions. With the same purpose, consideration is performed for shorter gate lengths (in actual devices, the gate length $L_G = 40$ nm). The gate dielectric consists of two films: an intermediate sublayer SiO_2 and then HfO_2. The equivalent oxide thickness (EOT) of the entire layer is 1.2 nm.

4. RESULTS AND DISCUSSION

Figure 2 shows the interface state density profiles N_{it}, generated during HCD, calculated for the stress voltages $V_{ds} = V_{gs} = 1.9$ V (V_{ds} and V_{gs} are the drain-source and gate-source voltages, respectively), room temperature, and two stress times, $t \approx 1.8$ s and 2 ks. The density of passive silicon–hydrogen bonds N_0 is set to be 5.6×10^{12} cm^{-2}; this value gives the maximum possible N_{it}. The profiles in Fig. 2 were constructed for the edge between the channel upper face and side wall (see Fig. 1). The argument is the normalized lateral coordinate x/L_G (measured in the drain-source direction, zero corresponds to the drain) for two series of devices with varied geometric parameters.

We can see that a highly degraded device region in transistors with shorter gates occupies a major portion of its length, i.e., the HCD appears more intense in shorter-channel FinFETs (under the same stress conditions). This is consistent with the results we published previously [33], and is explained by the fact that electrons in longer devices, moving from the source to drain, experience more scattering events, which result in depopulation of the high-energy ensemble portion, hence, HCD weakening with increasing L_G. As for the effect of the parameter W_{fin} on HCD, we can see that the trap density is higher in transistors with wider channels for both stress times t.

Figure 3 shows the relative changes in the linear drain current $\Delta I_{d,\,lin}(t) = [I_{d,\,lin}(t) - I_{d,\,lin}(0)]/I_{d,\,lin}(0)$ ($I_{d,\,lin}(0)$ is the drain current of the undamaged FET at $V_{ds} = 0.05$ V and $V_{gs} = 0.9$ V) with time for two transistor series. We can see in Fig. 3 that all tendencies appearing in Fig. 2 are also typical of the current $I_{d,\,lin}$ behavior. For example, it is clearly seen that HCD becomes stronger in FETs with shorter channels. We also conclude from the dependences $\Delta I_{d,\,lin}(t)$ that degradation is stronger pronounced in transistors with wider channels, which is consistent with the results of [9–11] and contradicts to the data of [7, 12, 13]. The latter situation suggests that the effect of W_{fin} on HCD is probably controlled by the totality of the geometrical

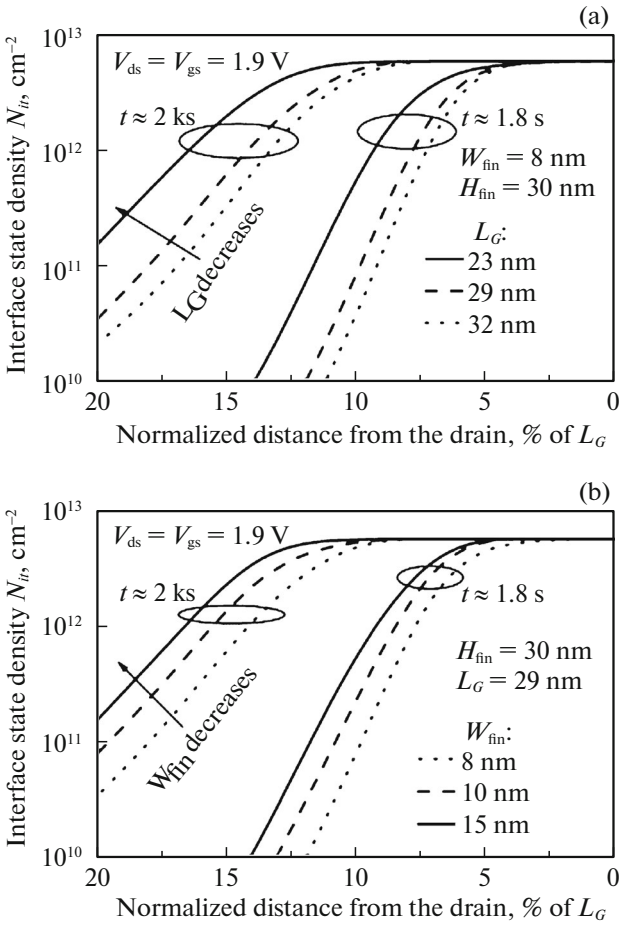

Fig. 2. Concentration of interface states as a function of the normalized lateral coordinate for two transistor series: with (a) varied length L_G and (b) varied width W_{fin}.

parameters of the device (as we showed in the case of the temperature dependence of HCD [21]) and can be different for various technologies.

As for the effect of the transistor channel-fin height H_{fin} (the effect of H_{fin} is not presented in Figs. 2 and 3), an insignificant HCD enhancement in FETs with higher channels was indicated.

We note one more important feature of the behavior of HCD, i.e., a change in the slope of curves $\Delta I_{d,\,lin}(t)$ and degradation "saturation" with time. For example, for the series with a varied width W_{fin} and stress voltages $V_{ds} = V_{gs} = 1.9$ V (Fig. 3b), this saturation is observed at times of ~50, 300 s, and 2 ks for $W_{fin} = 15$, 10, and 8 nm, respectively. Such a behavior is caused by the fact that the FinFET region near the drain at rather high voltages can reach the degradation limit (saturation: $N_{it} \sim N_0$, compare with Fig. 2) when available Si–H bonds are mostly broken. As a result, further HCD evolution can be associated only with N_{it} front propagation to the source (details are given in [16, 20]).

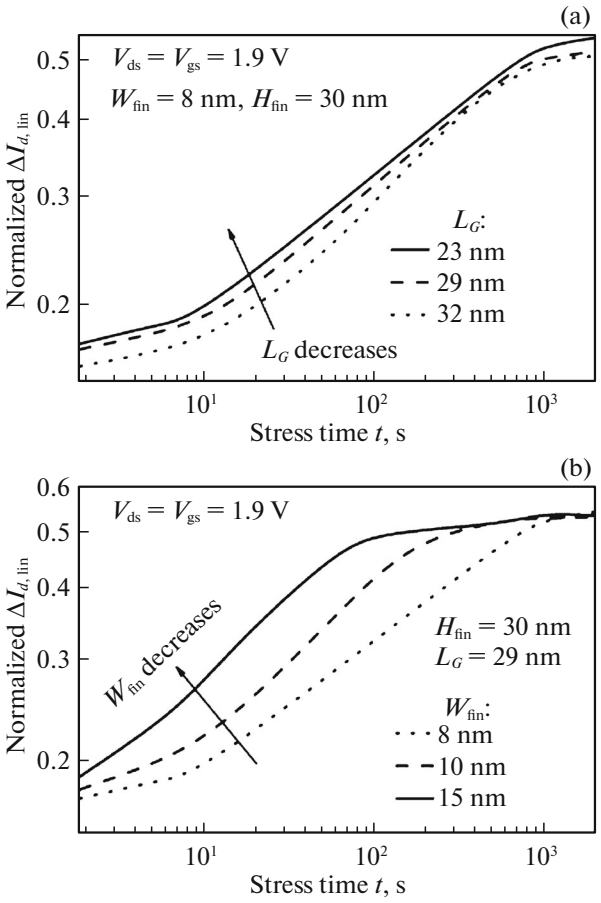

Fig. 3. Relative change in the linear drain current with the stress time for three transistor series with varied parameters (a) L_G and (b) W_{fin}. The voltages are $V_{ds} = V_{gs} = 1.9$ V.

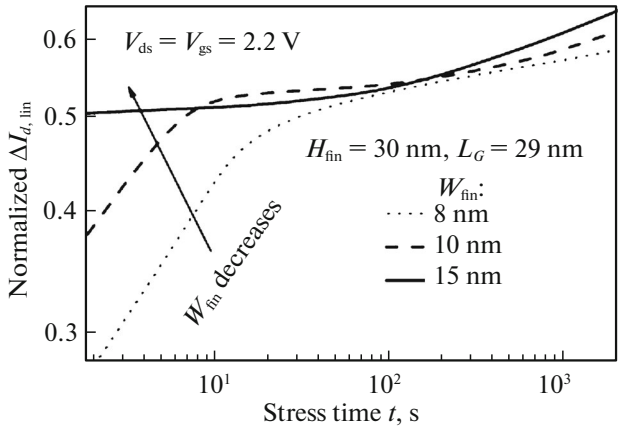

Fig. 4. The same as Fig. 3b, but for $V_{ds} = V_{gs} = 2.2$ V.

Figure 4 in combination with Fig. 3b illustrates the role of voltage variations. As the voltage is increased to $V_{ds} = V_{gs} = 2.2$ V (Fig. 4), saturation occurs earlier, and the times corresponding to the inflection of the $\Delta I_{d, lin}(t)$ characteristics shift to lower values, as expected.

5. CONCLUSIONS

The effect of the geometric parameters of a FinFET on the hot-carrier degradation behavior was studied. The analysis was performed by varying the gate length, and the channel width and length. Our HCD model was used, which consolidates three important aspects of the physical phenomenon of insulator–silicon interface fracture in the device: the carrier transport description, the defect incorporation kinetics, and the calculation of transistor characteristics during stress. We previously showed that the used model describes HCD in FinFETs with very good accuracy.

The results show that HCD under fixed stress conditions becomes stronger in devices with shorter channels. The effect of the fin height is insignificant, but distinguishable: the change in the FET characteristics is stronger in transistors with a higher channel segment. As for the effect of the channel width, our calculations showed that devices with wider channels degrade to a much greater extent. For now, there is no common consensus in the literature with respect to the nature of the effect of this parameter on the behavior of HCD. We believe that, to answer this question, the entire set of FET architecture parameters should be considered, not only W_{fin}.

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