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A Physical Model for the Hysteresis in MoS_2 Transistors

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ABSTRACT Even though the hysteresis in the gate transfer characteristics of two-dimensional (2D) transistors is a frequently encountered phenomenon, the physics behind it are up to now only barely understood, let alone modeled. Here, we demonstrate that the hysteresis phenomenon can be captured accurately by a previously established non-radiative multiphonon model describing charge capture and emission events in the surrounding dielectrics. The charge transfer model is embedded into a drift-diffusion based TCAD simulation environment, which was adapted to 2D devices. Our modeling setup was validated against measurement data on a back-gated single-layer MoS_2 transistor with SiO_2 as a gate dielectric. We use the modeling approach to gain a thorough understanding of the hysteresis, which will help to control this problem in future devices.

INDEX TERMS MOSFET, nanomaterials, semiconductor device modeling, hysteresis, semiconductor device reliability, two-dimensional materials, TCAD modeling.

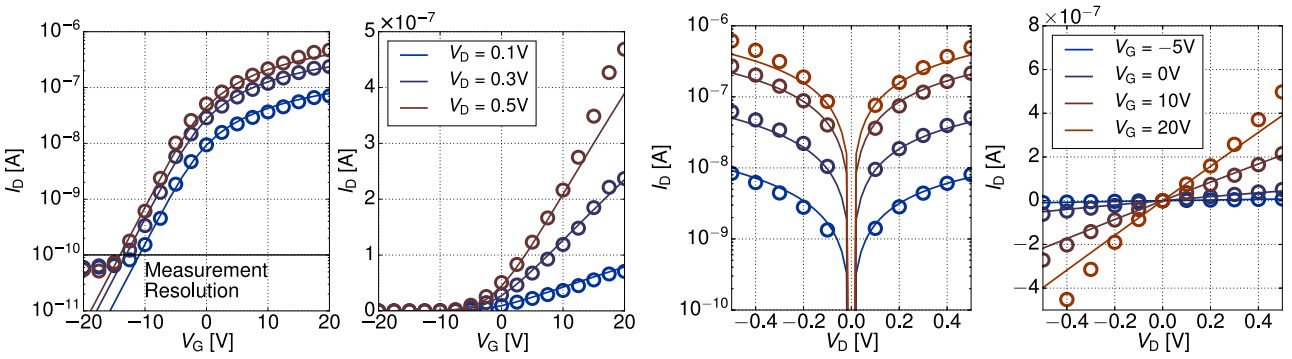
I. INTRODUCTION

Molybdenum disulfide (MoS_2) is a 2D material of the large group of transition metal dichalcogenides (TMDs), which has received a lot of attention over the past few years. It combines a superior electrostatic control over the channel due to its ultimate thinness, leading to a sufficient suppression of short-channel effects [1], with an inherent, comparatively large transport band gap [2]. This renders it an ideal candidate for applications in digital electronics [3]–[5], as it enables high current on/off ratios and a large transconductance [6].

However, up to now, MoS_2 based field effect transistors (FETs) have not met the high expectations for example when judging device performance in terms of mobilities. When accurately accounting for the non-negligible contact resistances [7], the mobility extracted for MoS_2 layers using multi-terminal measurements at room temperature does not exceed about 100 cm^2/Vs [8]. Besides that, while this mobility value lies in a range comparable with standard silicon technology, the large variability observed in the device characteristics and performance issues like the frequently observed hysteresis in the gate transfer ($I_D(V_G)$) characteristics [9]–[13] and the typically large drifts of the threshold voltage (V_{th}) over time [14] remain critical obstacles inhibiting industrial applications of MoS_2 FETs.

Complementing our previous experimental works on the hysteresis and drift of 2D FETs [14]–[16], here we present a detailed study on the main mechanisms governing the hysteresis phenomenon in the $I_D(V_G)$ characteristics of MoS_2 FETs. Our study is based on a drift-diffusion TCAD model [17], which is adapted to 2D devices in the first part of this paper using experimental results to test our model.

In the second part the degradation of the devices due to charge trapping in the underlying gate dielectric is discussed by coupling the model to a four-state non-radiative multiphonon (NMP) model [18]. This model was originally developed and established for charge transfer reactions in silicon (Si) technologies [19], [20] and is applied here to



(a) $I_D(V_G)$ (b) $I_D(V_D)$

FIGURE 1. Comparison of measured transfer characteristics (a) and output characteristics (b) (circles) to the simulated curves (solid lines). Excellent agreement between model and data is obtained.

devices based on 2D materials such as MoS_2. Our results confirm that the ubiquitous charge trapping at oxide traps is the main reason for the hysteresis in MoS_2 FETs [14] and provide new insights into the details on the occurrence of a hysteresis. We demonstrate that the hysteresis is caused by the same defect bands in silicon dioxide (SiO_2) that also govern the degradation in silicon devices. However, the degradation in MoS_2-based devices is more pronounced due to the unfavorable band alignment of the SiO_2 defect bands to the band edges of MoS_2.

II. DEVICES AND MEASUREMENTS

A description of the device fabrication and measurement techniques we use here to calibrate our model have been reported in detail elsewhere [14]. For the sake of completeness, we give a short summary of the details which will be important for understanding the simulation results later on. We study a back-gated MoS_2 FET on a 90 nm thick thermal SiO_2 serving as a back gate dielectric. The FET consists of a single layer (SL) flake of MoS_2 (around 6.5 Å), obtained via mechanical exfoliation and selection in an optical microscope [21]. The titanium/gold (Ti/Au) electrodes for the source and drain contacts were deposited using electron beam lithography and metal evaporation [9], forming a device with the dimensions $W = 6.8\,\mu m$ and $L = 1\,\mu m$. As a final fabrication step, the device was annealed in vacuum for 12 hours ($< 5 \times 10^{-6}$ Torr, $T = 120\,°C$) in order to reduce the contact resistances and to remove adsorbed impurities. For a basic electrical characterization the $I_D(V_G)$ characteristics as well as the $I_D(V_D)$ characteristics of the MoS_2/SiO_2 FET were measured using a gate voltage range of $V_G \in [-20\,V,\ 20\,V]$ and a drain voltage range of $V_D \in [0.1\,V,\ 0.5\,V]$ at a temperature of 25 °C in vacuum ($< 1 \times 10^{-5}$ Torr). To thoroughly analyze the hysteresis in the transfer characteristics, several $I_D(V_G)$s were recorded using a varying sweep rate $S = \Delta V/\Delta t$ (with ΔV as the voltage step and Δt as the time step), which corresponds to a sweep frequency of $f = 1/2t_{sw}$ with t_{sw} being the sweep time for one up- or down-sweep. The sweep time was varied in the range of $t_{sw} \in [8\,s,\ 200\,s]$. While the sweep time t_{sw} is an important parameter since it determines the time scale on which the hysteresis occurs, the primary property of the voltage step size ΔV is that it limits the measurement resolution of the hysteresis widths.

III. SIMULATION OF INITIAL DEVICES

In this section the general simulation methodology using drift-diffusion based TCAD [17] is verified against measured characteristics. The drift-diffusion equations [22] can be used because the lateral dimensions of our devices are in the micrometer range ($W \times L \approx 7.0\,\mu m^2$ for the device discussed here). As a consequence, there is a large number of scattering centers in the channel region resulting in scattering-dominated drift-diffusion charge transport. In several recent works [23]–[25] compact models describing devices based on 2D channel materials with drift-diffusion equations have been developed. The usage of drift-diffusion based TCAD has many advantages, among them a high computational efficiency [26] and a good adaptability to variations in device design.

The agreement between measurement and simulation obtained with our method is presented in Fig. 1. Our model is able to capture all aspects of the $I_D(V_G)$ and the $I_D(V_D)$ characteristics on a logarithmic scale as well as on a linear scale.

Critical for this good agreement is the correct choice of material parameters which are given in Table 1. The list of parameters is divided into two sections. The first section contains material constants which are extracted from the band structure calculated with density functional theory. The band structure of TMDs in the single-layer form has been studied in detail by the group of Thygesen [2], [27], [28], [30], [33], [39]. The shape of the band structure and thus also the parameters of this section depend on the dielectric surroundings and the layer number [39], thus the data in Table 1 refers only to the case of SL- MoS_2 on SiO_2.

The second section contains material parameters which are strongly influenced by defects in the channel region and are therefore processing dependent or which are determined by

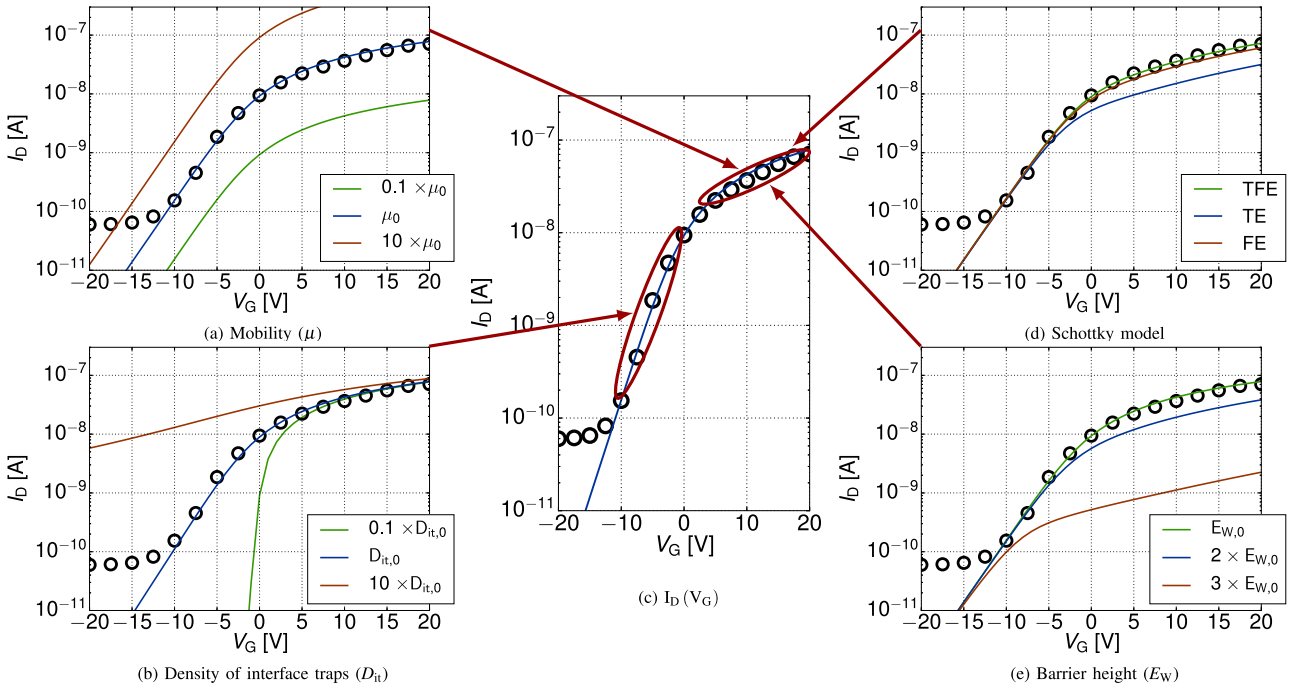


FIGURE 2. **The impact of the most important simulation parameters on the $I_D(V_G)$ characteristic. In the center (c) the fit of the drift-diffusion based TCAD model (solid curve) to the measured data (black circles) is shown. The material properties which are varied on the left hand side (mobility (a) and density of interface traps (b)) are related to the defects in the channel. On the right hand side (Schottky model (d) and barrier height (e)) the impact of contact-related parameters is illustrated.**

TABLE 1. **Material parameters of SL-MoS_2 on SiO_2 serving as input parameters for drift-diffusion based TCAD simulations. The parameters in the first section are extracted from band structures calculated with density functional theory, the parameters in the second section depend strongly on the defects in the semiconductor and thus on the processing conditions.**

Parameter	Value/Range	Reference
Transport band gap (E_G)	2.2 ± 0.1 eV	[2, 27–30]
Electron affinity (χ)	-3.85 ± 0.09 eV	[2, 27, 28, 30, 31]
Electron mass (m_n^*)	0.55 ± 0.05	[2, 32]
Hole mass (m_p^*)	0.56 ± 0.05	[2, 32]
Eff. rel. permittivity (ε_r^{eff})	5.5 ± 0.9	[33, 34]
Work func.diff.(Ti/Au) (E_W)	$[0.05, 0.2]$ eV	[35, 36]
Mobility (μ)	$[0.1, 100]$ cm^2/Vs	[7, 8, 37]
Den. of interface traps (D_{it})	$[10^{12}, 10^{13}]$ cm^{-2}eV^{-1}	[38]

the choice and the processing conditions of the metal contacts [7], [35]. For these parameters we only give meaningful ranges according to literature, within which the values should be chosen. At the current stage of research, where there are no generally acknowledged and standardized processing conditions, these parameters have to be treated as fitting values and have to be adjusted to each device separately.

The impact of the most important material parameters on the $I_D(V_G)$ characteristics is illustrated in Fig. 2. The central Fig. 2(c) demonstrates the quality of the established fit and Fig. 2(a) shows the effects of the mobility. The mobility (μ) is degraded by impurities in the channel, which act as scattering centers and determine the overall current level (Fig. 2(a)). While the mobility is the most important parameter of the drift-diffusion model, the impact of interface defects was considered by using the standard Shockley-Read-Hall (SRH) model [40], coupled to the drift-diffusion based TCAD simulator [17]. The density of interface traps (D_{it}) strongly affects the subthreshold slope (Fig. 2(b)). This parameter has been studied in detail by Takenaka *et al.* [38], who associated the typical density of interface traps observed for MoS_2 FETs with sulfur vacancies in the MoS_2 layers.

Contrary to standard CMOS devices, MoS_2 FETs are accumulation devices and the switching process is governed by the modulation of the Schottky barriers at source and drain [41], [42]. The work function difference between the metal contacts and the MoS_2 layer is an important parameter as it defines the Schottky barrier height. The impact of the work function difference is illustrated in Fig. 2(e), demonstrating that already small variations of this parameter can decrease the saturation current level ($I_{D,sat}$) by several orders of magnitude.

In Fig. 2(d) the impact of different models for describing the current transport across Schottky barriers is shown. In general one distinguishes between thermionic emission (TE), thermionic-field emission (TFE) and field emission (FE), depending on whether the thermionic current over the barrier or the tunneling current through the barrier dominates [43], [44]. The TFE model, where the total current over the Schottky barrier is given by the sum of the thermionic component and the tunneling component is the most accurate model and was used in our work. It was

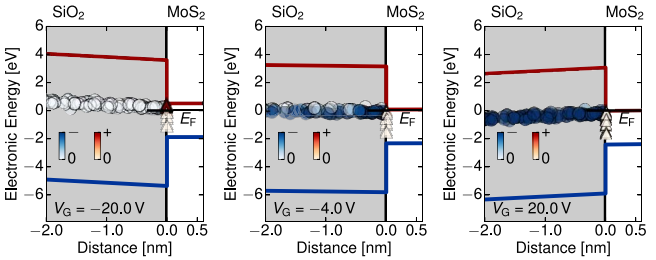
stated previously [7], [45] that the reduced Schottky barrier width in a 2D layer gives rise to large tunneling currents, which is confirmed by Fig. 2(d), where the tunneling component dominates.

In summary, our modeling approach for the characteristics of 2D based devices combines the drift-diffusion equations, which describe the scattering dominated transport through the channel, with a model for the current modulation by the Schottky barriers at source and drain, similar to the one outlined by Appenzeller *et al.* [42] and Penumatcha *et al.* [46]. With this approach a versatile model is obtained, which can serve as a first step towards enabling TCAD-aided device design.

IV. DEFECT MODELING

Having successfully developed a model to describe the current through a fresh device we now take the next step towards modeling the hysteresis. In order to see a shift in the threshold voltage between the up sweep and the down sweep of an $I_D(V_G)$ curve, there has to be charge trapping in the vicinity of the channel. While several groups claim that charge trapping takes place at the interface [12], [47], [48], we argue here in accordance with our previous works [14]–[16] that the fact that the largest hysteresis is observed for the largest sweep time is a strong argument in favor of oxide traps, as they usually have larger time constants than interface traps. For example, according to the SRH model with a band gap of 2.2 eV SL-MoS_2 provides a maximum time constant of 1 µs for a typical capture cross section of 1×10^{-15} cm^2.

Moreover, oxide traps are located at a finite distance from the interface, the most important ones for the charge transfer processes lying typically within the first few nanometers [49]. This leads to an increased bias dependence, as observed in the hysteresis in MoS_2 FETs. The enhanced bias dependence of charge trapping in the oxide in comparison to charge trapping at the interface is illustrated in Fig. 3. Interface traps provide trap levels inside the band gap, thus as the Fermi level sweeps across the band gap for increasing gate voltages, the interface traps become discharged. This charging process is five orders of magnitude faster than the sweep time, thereby effectively reducing the subthreshold slope. Once the Fermi level reaches the conduction band edge (roughly at $V_G \approx V_{th}$), it remains pinned there due to the high concentrations of injected electrons. To a first approximation there are no trapping and detrapping events at interface states above threshold voltage, which is confirmed by comparing the charge state of the interface traps in Fig. 3(b) and 3(c). However, for increasingly positive gate voltages, the oxide defect band is bent downwards, leading to more trapping events in the oxide, consistent with the experimentally observed increase in the hysteresis for increased high levels of the gate voltage $V_{G,H}$ [16]. The charge capture and emission events for gate voltages above the threshold voltage cause an effective shift of the whole $I_D(V_G)$, which produces the observed hysteresis.



(a) $V_G = V_{G,L}$ (b) $V_G = V_{th}$ (c) $V_G = V_{G,H}$

FIGURE 3. Band diagram of the MoS_2/SiO_2 FET showing the location of donor-like interface traps (red triangles) and of the acceptor-like oxide defect band (blue circles) [50], [51] responsible for the hysteresis. For gate voltages below the threshold voltage, the Fermi level moves through the band gap and interface states become discharged. Above the threshold voltage, the charge state of the interface states remains unchanged and the charging of oxide traps dominates.

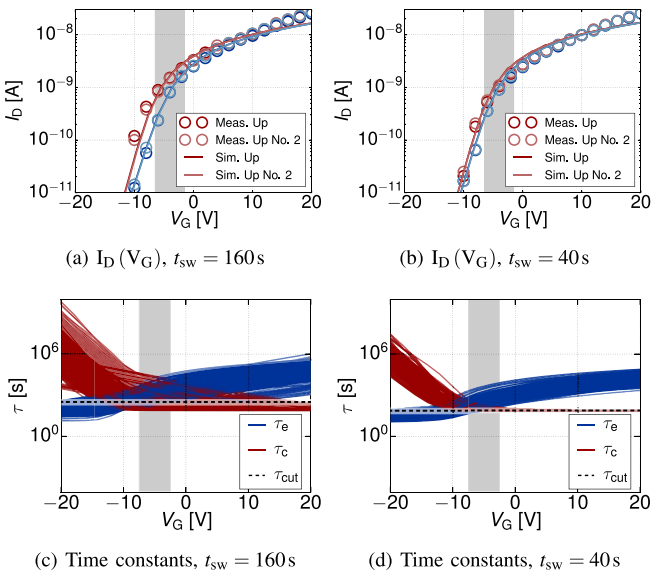
For the modeling of the hysteresis we use the four-state non-radiative multiphonon (NMP) model, which accurately describes charge transfer reactions in conventional Si/SiO_2 devices [18]. It does not only account for the energy of the transferred electrons, as it is usually done when using the SRH model [40], but it also considers the energetic relaxation of the structure around the defect, where the electron is captured or emitted [18], [52]. Depending on the microscopic nature of the defect, which has been studied in great detail for SiO_2 based on Si/SiO_2 FETs [53], [54], one usually speaks either of hole or of electron trapping. As the charge transfer process is exactly the same in both cases, the two processes can only be distinguished by the charge change of the trapping defect in the oxide, which either goes from positive to neutral (hole/ donor-like trap) or from neutral to negative (electron/ acceptor-like trap). Therefore, the difference between electron traps and hole traps is only visible in an offset of the transfer characteristic, as it only changes the balance of fixed charges.

Thus, in order to explain the hysteresis in MoS_2 FETs we use the two defect bands of SiO_2 known from silicon technologies [20], [50], [51], with the first being a donor-like hole trapping band located at $\langle E_T^L \rangle \pm \sigma_{E_T^L} = 4.6 \pm 0.3$ eV below the conduction band edge of SiO_2 [20], and the second being an acceptor-like electron trapping band at $\langle E_T^U \rangle \pm \sigma_{E_T^U} = 3.0 \pm 0.2$ eV below the conduction band edge of SiO_2. The second defect band has already been observed for Si-based devices with dielectric gate stacks [50], [51] and has been used in our previous works for the modeling of the hysteresis and of bias-temperature instabilities in FETs based on MoS_2 [14], [16] and black phosphorus [15]. The first defect band is located in the lower half of the band gap of SL-MoS_2 and does not contribute to the degradation in nMOS devices, where the Fermi level only scans across the upper half of the band gap. Therefore, only the second defect band has to be taken into account and is shown in Fig. 3.

Besides the bias dependence of the charge trapping process the second important aspect is the temporal behavior of the responsible defects, as determined by the four-state

NMP model. A trap can only contribute to the hysteresis if it captures an electron at a high gate voltage and emits this electron not before reaching again the low level of the gate voltage. This means that the electron capture time constant (τ_c) of the respective trap has to be smaller than the electron emission time constant (τ_e) at high gate voltages and vice-versa. For this criterion the important voltage level is $V_{th} \approx -4\,V$, where the hysteresis is extracted. If for $V_G < V_{th}$ it holds that $\tau_e < \tau_c$ and for $V_G > V_{th}$ it holds that $\tau_e > \tau_c$, this trap can in principle contribute to the hysteresis.

In Fig. 4(a) and (b) the simulated hysteresis for two different frequencies is shown and compared to measurement data. There were two subsequent measurement rounds to demonstrate that the hysteresis is a reproducible phenomenon and there is no general drift of the characteristics interfering with the hysteresis. Our simulation results clearly corroborate the previously observed [14] PBTI-like hysteresis. PBTI stands for positive bias temperature instability and PBTI-like hysteresis means that the down sweep is shifted to higher threshold voltages just as the threshold voltage is increased under positive stress bias.



(a) $I_D(V_G)$, $t_{sw} = 160\,s$ (b) $I_D(V_G)$, $t_{sw} = 40\,s$

(c) Time constants, $t_{sw} = 160\,s$ (d) Time constants, $t_{sw} = 40\,s$

FIGURE 4. Hysteresis fit at two different frequencies (red: up-sweep, blue: down-sweep), together with the voltage dependence of the time constants for a selected set of defects. The sweep time t_{sw} determines the cut-off time via $\tau_{cut} = 2t_{sw}$. At the shorter sweep time, there are fewer defects with time constants in the appropriate range causing a smaller hysteresis width.

When comparing Fig. 4(a) and (b) there is an apparent dependence of the hysteresis width on the sweep frequency. In fact, the traps contributing to the hysteresis at different frequencies are not the same. The time for one up-sweep or one down-sweep ($2t_{sw} = 1/f$) sets to a first approximation an upper limit (τ_{cut}) for the time constants of the contributing traps. If either $\tau_e < \tau_{cut}$ at the maximum negative V_G or $\tau_c < \tau_{cut}$ at maximum positive V_G, this trap can change its charge state for the first time towards the end of the up sweep and for the second time towards the end of the down sweep. If this condition is not fulfilled, it is very unlikely that this trap changes its charge state at all during the sweeping process. In addition, the trap also must not change its charge state too quickly. To be precise, it cannot contribute to the hysteresis if it captures a charge before the hysteresis width is measured at $V_G = V_{th}$. This corresponds to meeting the condition $\tau_c > t(V_{th})$ at threshold voltage, with $t(V_{th})$ being the sweep time until threshold voltage is reached.

In Fig. 4(c) and (d) the bias dependence of the time constants of all traps fulfilling all of the above mentioned criteria and thus causing the hysteresis are displayed. The electron capture time shows a larger bias dependence than the emission time. At shorter sweep times, less defects meet the criteria, reducing the hysteresis width.

To quantify the hysteresis phenomenon, we extracted the hysteresis width at the threshold voltage for all measured sweep frequencies. In Fig. 5 the hysteresis width is shown as a function of the sweep frequency for the measurements and for the simulations. The error bars denote the minimal measurement errors given by the voltage stepping used in the measurements. Additionally, the offset between subsequent measurement rounds is displayed to make sure that no permanent shift of the characteristics interferes with the hysteresis. Good agreement between measured and simulated data is obtained, clearly demonstrating that our simulation methodology captures the time behavior of the hysteresis phenomenon correctly.

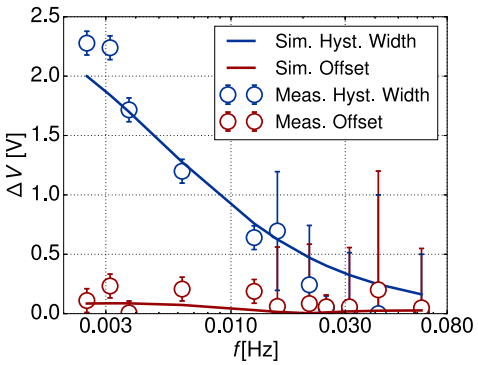


FIGURE 5. Hysteresis width (extracted between up- and down-sweep (blue)) and the offset (extracted between two up- or two down-sweeps for different measurement rounds (red)) as a function of the sweep frequency. The error bars report the minimum error of the measurement process given by the voltage step ΔV used to record the $I_D(V_G)$ curve. The hysteresis width decreases quickly for fast sweeps and there is only a small overall offset, ruling out a dominant general drift.

V. CONCLUSION

A general drift-diffusion based TCAD simulation methodology for devices based on 2D materials such as MoS_2 was established. By coupling a non-radiative multiphonon model to this simulation framework, charge capture events at oxide traps can be described. As oxide traps show a larger bias dependence and larger time constants than interface traps,

we concluded that oxide traps are responsible for the hysteresis observed in the $I_D(V_G)$ characteristics of back-gated SL-MoS_2 FETs. The NMP model correctly captures the sweep time dependence of the hysteresis width, confirming the suitability of our approach.

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