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CONFERENCE PROGRAM

MONDAY 19

9:00 - 9:30 **CONFERENCE PRESENTATION AND WELCOME**

INVITED TALK

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9:30 - 10:00 **MBE growth of ordered InGaN/GaN nano/microrods: basics and applications** **p. 1**

Enrique Calleja

Polytechnical University of Madrid, Spain

SESSION 1: Fabrication and Process Characterization

Chair: *Viktor Sverdlov, TUWien, Austria*

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Seung Min Lee[1,2], Jung Hwan Yum[3,4], Eric S. Larsen[3,4], Christopher W. Bielawski[3,4] and Jungwoo Oh[1,2]

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10:20 - 10:40 **Dopant Activation in Ultra-thin SiGeOI and SOI layers characterised by Differential Hall Effect** **p. 5**

R. Daubriac[1], E. Scheid[1], S. Joblot[2], R. Beneyton[2], P. Acosta Alba[3], S. Kerdilès[3], F. Cristiano[1]

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[3]*CEA-LETI and Univ. of Grenoble, 17 rue des Martyrs, 38054 Grenoble, France*

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F. Tcheme Wakam[1,2], J. Lacord[1], M. Bawedin[2], S. Martinie[1], S. Cristoloveanu[2], J.-Ch. Barbe [1].

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INVITED TALK

Chair: *Luca Donetti, UGR, Spain*

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Byungil Kwak

SK Hynix, Republic of Korea

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M. Duan[1], F. Adamu-Lema[1], C. Navarro[2], F. Gamiz[2], A. Asenov[1]

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[2]University of Granada, Spain

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SESSION 3: Simulation

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[3]*University of Nottingham Ningbo China, 199 Taikang Road, Ningbo, 315100, China*

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[2]*CRANN and AMBER Research Centres, Trinity College Dublin, Ireland*
[3]*Universität der Bundeswehr, München, Germany*

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INVITED TALK
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SESSION 5: Memories II
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INVITED TALK

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Tyndall National Institute, University College Cork, Cork, Ireland

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[2]*Institute of Physics and Technology RAS, Moscow, Russia*

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Device Modeling Group, University of Glasgow,Glasgow G128LT, Scotland, UK

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Peter Grünberg Institute (PGI-9) and JARA-FIT, Forschungszentrum Juelich, 52428 Juelich, Germany

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Chair: *Paul Hurley, Tyndall, Ireland*

WEDNESDAY 21

INVITED TALK

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[1]Integrated Circuits Laboratory (ICLAB), Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland
[2]CEA-Leti, Grenoble, France

12:40 - 13:00 **Adaption of Triple Gate Junctionless MOSFETs Analytical Compact Model for Accurate Circuit Design in a Wide Temperature Range** **p. 143**
Antonio Cerdeira[1], Fernando Ávila-Herrera[1], Magali Estrada[1], Rodrigo T. Doria[2] and Marcelo A. Pavanello[2]

[1]SEES, CINVESTAV, Mexico City, Mexico
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SESSION 10: III-V Devices

Chair: *Edward Y. Chang, National Chiao Tung University, Taiwan*

MBE growth of ordered III-Nitride nano/microrods: basics and applications

Enrique Calleja

ISOM-ETSIT, Polytechnical University, Av. Complutense 30, 28040 Madrid. Spain

Self- assembled (SA) growth of nanostructures by Molecular Beam Epitaxy (MBE) is a rather straightforward process providing defect and strain-free material with a very high structural and optical quality. However, nanostructures grown by SA have an inherent size and density dispersion detrimental to device applications[1]. Selective Area Growth (SAG) was then used to develop a variety of nanostructures arrays on different substrates.

Some basic aspects of SAG will be first addressed, referring to the initial stages of nano/microrod nucleation within the mask nano/microholes leading to a final stable hexagonal structure (figure 1), the control of the nano/microrod diameter in axial heterostructures, and the dislocation filtering efficiency as a function of the nano/microrod geometry.

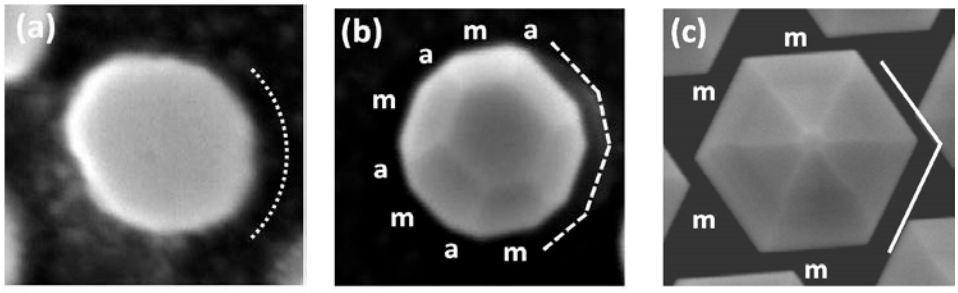

Fig.1. Evolution of NW nucleation/growth. From ref (2).

Axial InGaN/GaN nanostructures have been grown aiming at nanoLED fabrication where emission wavelength can be easily controlled. Furthermore, mixing fundamental colors (RGB) provide white light emission without the need of phosphors (figure 2)[3,4]. On the other hand, core-shell InGaN/GaN microstructures have been successfully grown by MBE for microLED purposes[5] where the advantages are a much higher active emission area and the absence of internal electric fields that strongly reduce emission efficiency (figure 3).

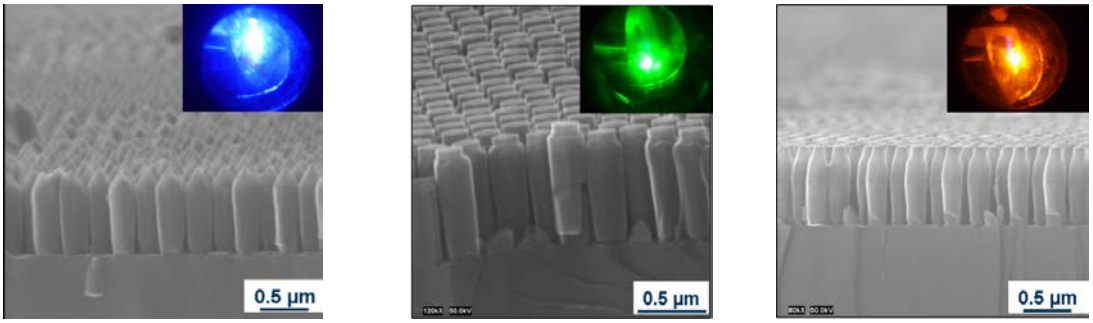

Fig. 2. SAG Axial nanowires emitting at different wavelengths

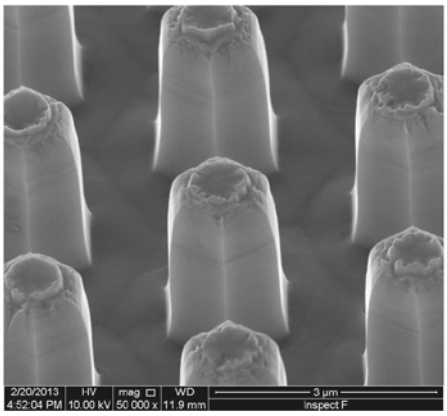

Fig. 3. SAG Core-shell microstructures

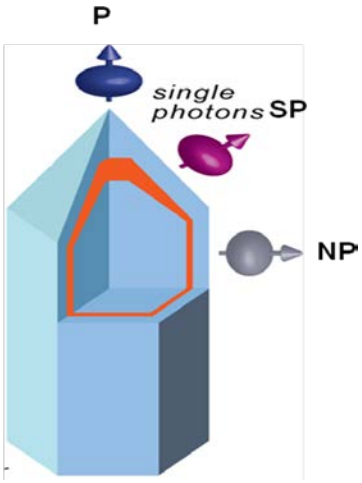

Fig. 4. Dot-in-a- Wire structure

A relevant finding is the evidence that the In incorporation efficiency depends very much on the crystal plane considered, being the highest on polar *c*-planes and minimum for non-polar ones. Thus, different In-related emissions are observed in the microstructures. Taking advantage of this effect, Dot-in-a-Wire InGaN structures[6] were grown embedded in ordered GaN nanorods. The InGaN region grows along the polar, semi-polar and non-polar planes, thus incorporating different amounts of In (figure 4).

Finally, SAG was also used to grow III-Nitride ordered nanostructures on semi-polar and non-polar oriented GaN/sapphire templates aiming at the fabrication of pseudo-substrates by nanocrystal coalescence with tailored lattice constant and high crystal quality[7].

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Epitaxial Growth of BeO-on-GaN using Atomic Layer Deposition

Seung Min Lee[1,2], Jung Hwan Yum[3,4], Eric S. Larsen[3,4], Christopher W. Bielawski[3,4] and Jungwoo Oh[1,2,*]
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***Abstract*— BeO film has excellent insulator properties of bandgap (10.6 eV) and dielectric constant (6.9). In addition, a high thermal conductivity (330 W/m-K) can effectively reduce a self-heating problem. We demonstrated an epitaxial growth of BeO film on GaN using atomic layer deposition (ALD) for the first time. The HR-TEM and XRD indicated wurtzite (002) crystal structure of BeO-on-GaN. The Raman shift and soft phonon modes verified characteristics of thin film BeO were close to those of bulk BeO. Capacitance-voltage curves confirmed a low interface defect density. The results enable the application of epitaxial BeO to high-k gate dielectrics and heat dissipation layers for future transistors.**

Keywords-beryllium oxide; gallium nitride; atomic layer deposition; epitaxy

I. INTRODUCTION

Beryllium oxide (BeO) can be structurally matched with gallium nitride (GaN) thanks to the same crystalline structure (wurtzite) and symmetry ($P6_3mc$). It also exhibits unique physicochemical properties such as high electrical resistivity (>10^{14} Ω.cm), high band gap (10.6 eV), high melting point (2532±10 °C), and dielectric constant (6.9). One of the most important property of BeO is high thermal conductivity (330 W/m-K) [1]. Thus, BeO is regarded as the best candidate for a heat sink layer and/or an electrical insulator for high power electronics [2]. By utilizing atomic layer deposition (ALD) as the epitaxial growth, excellent thermal-electrical properties of BeO can be applied to the front-end process of GaN based power devices.

In this study, we demonstrated the single-crystalline BeO films epitaxially grown on GaN at low temperature (250 °C) via ALD process. Using Grignard metathesis, the precursor ($Be(CH_3)_2$) was synthesized for ALD precursor [3]. The high resolution-transmission electron microscope (HR-TEM) and x-ray diffraction (XRD) analysis were used to identify the crystallinity of BeO film. The high thermal conductivity of BeO was verified by Raman spectroscopy. From the capacitance-voltage (*C-V*) results, we confirmed dielectric constant and interface trap density (D_{it}) of epitaxial BeO film.

II. RESULTS AND DISCUSSION

Figure 1 shows cross-sectional and plane-view TEM images of BeO-on-GaN. The BeO films clearly exhibited high crystallinity, featuring sharp interfaces. From selective-area electron diffraction (SAED) patterns, we confirmed that the BeO films were epitaxially grown on GaN as a hexagon-on-hexagon without any tilt.

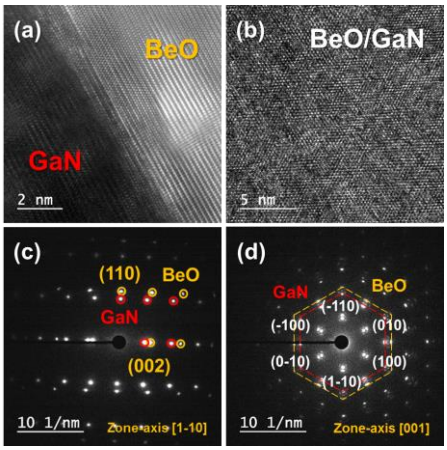

Figure 1. (a-b) Cross-sectional and plane-view TEM images of ALD BeO-on-GaN and (c-d) corresponding SAED patterns.

The θ-2θ profiles of BeO-on-GaN are shown in Figure 2(a). Only (002) peak and no other peaks were observed and the BeO (002) reflection was almost identical to XRD database (41.21°). The θ-2θ analysis indicated that single-crystalline BeO (001) films were epitaxially grown on GaN. The φ-scan profile across the off-normal plane was plotted in Figure 2(b). The coincidence in angular positions of BeO {102} and GaN {102} reflections and six separate peaks of BeO repeated at every 60° revealed that the grains of BeO films were well aligned along in-plane axis of wurtzite structure without any tilt.

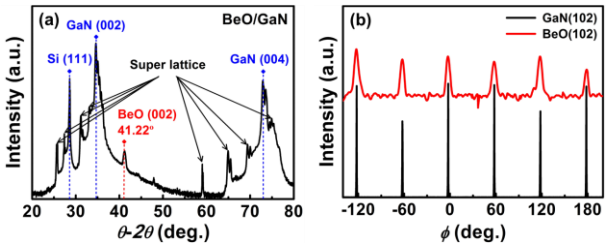

Figure 2. (a) θ-2θ XRD profiles of BeO grown on GaN and (b) φ-scans across the off-normal {102} plane.

The thermal conductivity of the epitaxial BeO film was indirectly investigated by Raman spectroscopy (Figure 3) as non-destructive optical method to measure the thermal conductivity of thin-film and bulk materials [4]. The Raman-active E_1(TO) mode of the ALD BeO film (753 cm^{-1}) were similar to molecular-beam epitaxial (MBE) BeO film (762.6 cm^{-1}) [5] and *ab initio* calculation data (753.4 cm^{-1}) [6]. Results suggested that the material properties of ALD BeO films were close to those of bulk BeO. Small wavenumbers were associated with soft phonon modes, and soft phonon modes reflected the thermal conductivity [7]. Raman shifts for the epitaxial BeO were greater than reported for typical high-k dielectrics such as Al_2O_3, HfO_2, and ZrO_2, indicating that BeO has a higher thermal conductivity than these oxides [8].

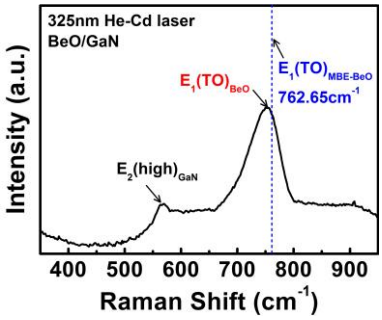

Figure 3. (a) θ-2θ XRD profiles of BeO grown on GaN and (b) φ-scans across the off-normal {102} plane.

Figure 4 shows (a) schematic diagram of BeO/GaN metal-oxide-semiconductor (MOS) capacitor and (b) *C-V* measurements. Small frequency dispersion and hysteresis (in-set) implied reasonably low interface trap density, resulting from the good inter-atomic matching of BeO-on-GaN. The dielectric constant of 7.3 was large due to series connection of 20 nm AlGaN capacitor (k = 9.5). In addition, BeO gate insulator potentially reduce channel mobility degradation due to relatively low electro-magnetic interactions between the electrical carriers and atoms in the gate dielectric [9].

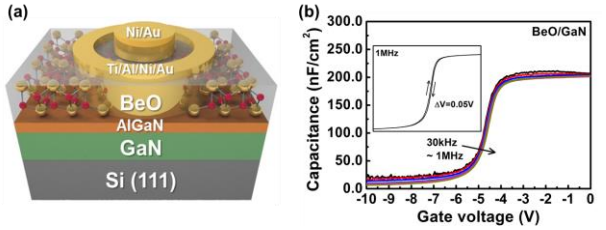

Figure 4. (a) Schematic diagram BeO-on-GaN MOS capacitors and (b) frequency dispersion and hysteresis curves.

III. Conclusion

For the first time, we epitaxially deposited single-crystalline BeO (001) on GaN using ALD. The precursor (DMBe) was synthesized by Grignard metathesis. The crystallographic relationship of BeO-on-GaN was characterized using HR-TEM and XRD. The thermal conductivity of BeO were verified by Raman spectroscopy. In addition, *C-V* revealed reasonably high dielectric constant of ~ 7.3 and low hysteresis of 0.05V. Epitaxially grown BeO using ALD exhibited excellent gate dielectrics and thermal conductivity for future power and CMOS transistors.

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Dopant Activation in Ultra-thin SiGeOI and SOI layers characterised by Differential Hall Effect

R. Daubriac[1], E. Scheid[1], S. Joblot[2], R. Beneyton[2], P. Acosta Alba[3], S. Kerdilès[3], F. Cristiano[1]
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***Abstract*— The reduction of the contact resistance R_C is one of the most challenging issues related to the miniaturisation of advanced MOSFET architectures, including FDSOI technology (Fully Depleted Silicon-On-Insulator). R_C strongly depends on the active dopant concentration at the semiconductor/salicide interface. It is therefore essential that electrical activation at different depths within a doped layer is reliably determined to optimise the fabrication processes. In this paper, we firstly present a Differential Hall Effect (DHE) method which allows measuring the active dopant concentration profile close to the surface with nm resolution for ultra-shallow doped $Si_{1-x}Ge_x$ and Si layers. Then, we present DHE measurements made on junctions processed with advanced techniques, including nsec LTA and msec DSA anneals.**

Keywords– FDSOI, contact resistance, shallow junctions, Differential Hall Effect

I. Introduction

The research efforts made throughout the last decades have made it possible to keep the momentum for a continuous miniaturization of electronics devices. For instance, the bulk planar transistor limitations have been overcome thanks to the diversification of the device architecture, with the actual spectrum going from enhanced planar architectures like FDSOI **[1]** to 3D transistors like TriGate FinFETs or gate-all-around NWFETs. Despite their differences, some technological issues, such as the reduction of the access resistance, still represent a common challenge for all of them. According to theory, the increase of the active dopant concentration at the semiconductor/silicide interface is a strong lever for access resistance reduction (eq. (1)):

$$\rho_{Sal,SC} = \rho_{Sal,SC_0}.exp\left(\frac{2\phi_B}{\hbar}\sqrt{\frac{\varepsilon_S m^*}{N}}\right) \propto \frac{\phi_B}{\sqrt{N}} \qquad (1)$$

Several techniques including dopant segregation and pre-amorphisation have been proposed to this purpose. Further optimisation of the doping processes (or improvement of the TCAD models calibration), make it therefore necessary to reliably characterize dopant activation at the surface of the doped layers.

Hall effect has been used for years to characterize semiconductors providing the active dose N, the sheet resistance R_S and the carrier mobility μ. However, due to current flowing in the whole layer, only average values are measured. Differential Hall Effect (DHE) has therefore been proposed in order to extract depth depending values of these parameters. This method is based on the iteration of oxidation/etch cycles based either on anodic or native oxidation processes, with the etch rate determining the depth resolution. DHE has been successfully demonstrated for pure Si and Ge; however its application to SiGe is far more challenging due to the different oxidation rates of these two species.

In this paper, we present a DHE method allowing to precisely evaluate these parameters for both Si and SiGe materials. The method is presented in section II and then applied to test structures fabricated using advanced processes (section III).

II. Differential Hall effect method

A. *Ecthing processes*

For SiGe, we use a one-step chemistry based on the SC1 solution that simultaneously oxidizes and etches both Si and Ge **[3] [4].** For Si, a two-step process consisting in controlled ambient air oxidation followed by HF oxide stripping and ethanol rinsing is used **[5]**. Both processes allow reaching sub-1nm etching resolution with negligible surface roughness and, for SiGe, stoichiometry conservation. All these characteristics have been determined by AFM, XRD, TEM and ellipsometry and are summarized in **Tab. 1**.

B. *Electrical measurements*

Electrical measurements are performed on optimized greek-cross Van der Pauw structures (1.8 x 1.8 cm^2). A dedicated o-ring cell has been designed to protect the metallic peripheral contacts during etch. After a sequence of oxidation/etch and measurements cycles, it

Characteristics	Si	$Si_{1-x}Ge_x$
Chemistry	HF(5%) + Ethanol	$NH_4OH:H_2O_2:H_2O$ (1:1:5)
Mechanism	Oxidation then stripping **(2 steps)**	Oxidation and dissolution **(1 step)**
Surface	Low roughness (~0,2nm)	Low roughness (~0,1nm)
Etchrate	~ 1 nm / cycle	~ 0,5 – 1 nm / cycle
Stoechiometry	-	Preserved

Tab. 1: Summary of main features of Si and SiGe etching chemistries.

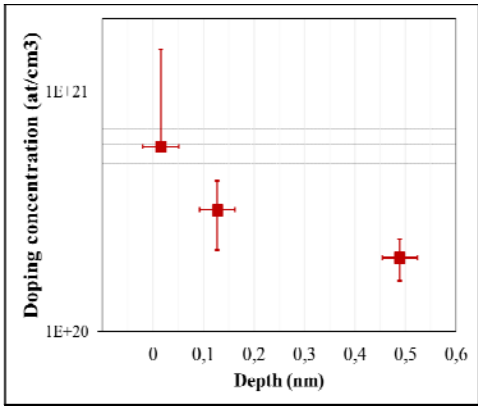

Fig. 1: Depth distribution of the active dopant concentration as determined by Differential Hall effect measurements from the SiGeOI sample implanted with Boron and laser annealed at an energy density of 0.68 J/cm^2.

is finally possible to extract the dopant concentration profile as a function of depth, taking into account the predetermined Hall scattering factor (~0.75 for Si and ~0.4 for SiGe **[5] [6]** for *p-type* doping).

III. Application of DHE procedure to samples fabricated with advanced techniques

A. 6nm SiGeOI layers doped by Ion Implantation and nanosecond LTA (Laser Thermal Annealing)

In the designed process, *n-type* and *p-type* dopants were implanted in a pre-amorphised SiGe layer obtained by Ge^+ implant. LTA was achieved using a SCREEN-LASSE XeCl excimer laser (λ = 308 nm) with energy densities ranging from 0.65 to 0.79 J/cm^2. Although the investigated doping process is at a preliminary stage, and considering the difficulty in controlling the sharp transition between a "no melt" and a "full melt" condition for such ultrathin layers, our DHE investigations allow to conclude that a doping process based on nanosecond laser annealing can be successfully applied to ultrathin SiGeOI layers of ~6 nm thickness, with achieved active dopant concentrations at the surface well above 1x10^{20} cm^{-3} for annealing conditions below the threshold energy (0.68 J/cm², **Fig. 1**). This is a promising result in view of improving contact resistivity in source/drain regions of advanced devices.

B. 11nm SOI layers doped by Ion Implantation and annealed by spike-RTA or msec DSA methods

We also characterised 11nm-thick arsenic doped SOI layers processed either with RTA annealing (Rapid Thermal Annealing) or with msec DSA laser annealing (Dynamic Surface Annealing). For the same implanted dose, conventional Hall effect measurements indicate that a higher active dopant fraction is achieved by DSA compared to RTA. Our DHE analysis reinforced this result by showing that a higher active dopant concentration is achieved at the surface by DSA (cf. **Fig. 2**), confirming the interest for DSA as an efficient solution for contact resistance reduction.

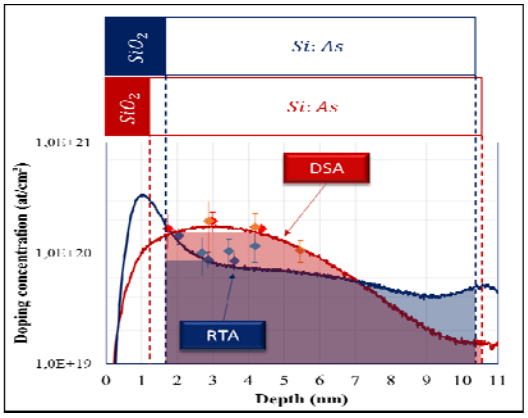

Fig. 2: Depth distribution of active dopant concentration for DSA and RTA processes measured by DHE **(colored dots)** compared to their respective SIMS **(colored lines)** from the 11 nm SOI samples implanted with arsenic at the same dose (10^{14}at/cm²). Colored areas in the graph correspond to the active dose. Diagrams above graph zone represent the layers dimensions measured by ellipsometry.

IV. Conclusion

We presented a DHE method for the investigation of dopant activation in ultra-thin Si and SiGe layers. We demonstrated the reliability of our process in terms of depth resolution, surface roughness and stoichiometry. The DHE method is applied to samples fabricated by advanced doping techniques. Fast anneals as LTA and DSA are confirmed as very efficient activation processes to achieve the high surface dopant concentrations that are required for contact resistance optimisation.

Acknowledgments

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Doping profile extraction in thin SOI films: application to A2RAM

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***Abstract*—We propose for the first time a method based on C-V measurement to extract the bridge doping profile which governs the A2RAM performances. Assessed with TCAD simulation and simple extraction model adapted from bulk devices, this technique is validated with experimental data.**

Keywords - A2RAM; C-V characteristic; SOI; electrical characterization.

I. INTRODUCTION

The A2RAM (Fig.1) is a 1T-DRAM [1] with an N doped layer (nMOS case) called 'the bridge' located at the bottom of the low-doped p-type body. The bridge allows short-circuiting the source and drain. The concept of A2RAM has been presented in [2] and its experimental performance in [3]. Recently, the scalability issues of the A2RAM have been studied by TCAD simulations [4]. We noticed some inconsistencies with measurements, presumably related to the mismatch of the bridge doping profile between TCAD simulations and experiments. As the A2RAM behavior is strongly related to these parameters, we need an accurate solution to evaluate them. The use of a physical characterization such as Secondary-Ion Mass Spectroscopy (SIMS) is not reliable here because (i) the silicon film is too thin and (ii) the target doping is too low (around 10^{18}cm^{-3}). For this purpose, the C-V electrical characterization is emulated through TCAD simulations and validated with the electrical measurements.

II. A2RAM: TCAD SIMULATION METHODOLOGY AND C-V CHARACTERISTIC

We simulate the A2RAM structure (Fig. 1) as fabricated in [3] with Synopsys TCAD tools [5] using the same models as in [4].

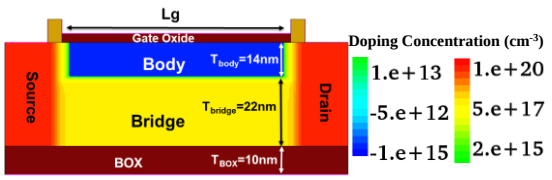

Figure 1. Simulated A2RAM cell with parameters defined by the process flow in [3].

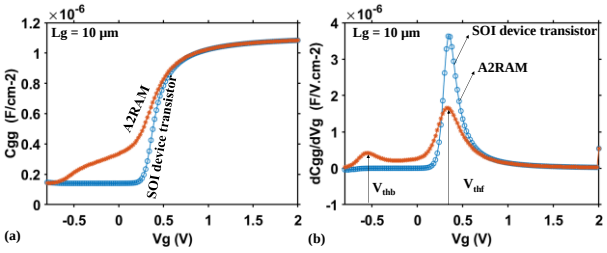

Figure 2. (a) C(Vg) characteristic of the A2RAM and the standard SOI transistor with same silicon thickness as A2RAM but with no doped bridge, (b) first derivative of the C-V curves.

The main technological parameters are: abrupt Gaussian doping profiles, body thickness T_{body} = 14 nm, bridge thickness T_{bridge} = 22 nm, bridge doping $N_{bridge} = 1.10^{18}$ cm^{-3}, Equivalent Oxide Thickness EOT = 3.1 nm and Buried Oxide thickness T_{BOX} = 10 nm. We performed small signal simulation and report on Fig.2-(a) the gate capacitance C_{gg} versus the gate voltage V_g for both the A2RAM and a standard SOI device transistor. Similarly, to a back biased FD SOI devices with an inverted back channel, the A2RAM C-V characteristic shows a double hump. When the front-gate bias increases, the first hump is related to the 'conduction of the bridge' at V_{thb} and the second one to the onset of the front channel at V_{thf} (Fig.2-(b)).

III. BRIDGE DOPING PROFILE EXTRACTION METHOLOGY WITH TCAD

To extract the bridge doping profile, we use the method describes in [6-8]. The depletion depth is dependent on the gate voltage: a small signal variation on the metal leads to the variation of the depletion depth, thus the variation of the majority charge density in the semiconductor.

A. Extraction of the 'doping profile of the bridge'

Having C_{gg}, and considering depletion regime in the body and all dopants ionized, we need to compute the so called 'doping function' N_{net} (1) defined as an apparent density of charge in the silicon film:

$$N_{net} = 2\left(qA^2\varepsilon_{SI}\frac{dC_{gg}^{-2}}{dV_g}\right)^{-1} \quad (1)$$

with q the elementary charge, ε_s the silicon permittivity and A the gate area. Fig.3-(a) shows $|N_{net}|$ versus V_g derived from the C-V characteristic of the A2RAM (Fig.2-(a)).

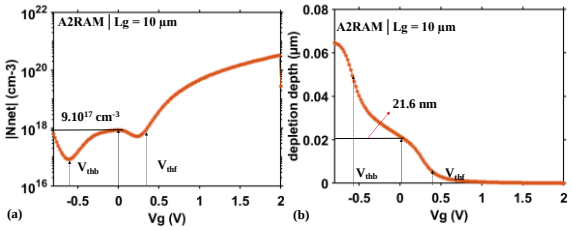

Figure 3. (a) Doping function and (b)-depletion depth in A2RAM by TCAD simulations.

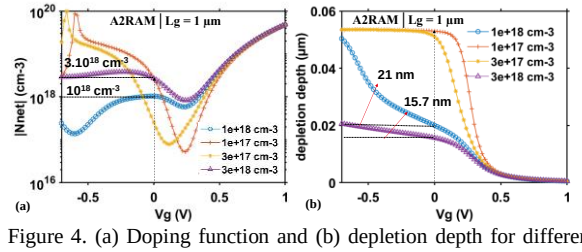

Figure 4. (a) Doping function and (b) depletion depth for different N_{bridge} obtained by A2RAM TCAD simulations.

In the gate bias range between V_{thb} and V_{thf}, the 'doping function' presents a broad peak with the maximum value $10^{18}cm^{-3}$ corresponding to the doping value set in TCAD (Fig.1). In fig.4-(a), similar simulations are performed for various N_{bridge}. If the N_{bridge} is low ($<3.10^{17}$ cm^{-3}), the extracted value has no sense because the bridge is fully depleted. But higher values of N_{bridge} (3.10^{18} cm^{-3}) can be accurately evaluated because less and less portion of the bridge is depleted by the field effect.

B. Extraction of the 'Body' thickness

We aim to extract N_{bridge} and T_{body}. At a gate voltage between V_{thb} and V_{thf}, the bridge is formed and the body is depleted: this means that the gate capacitance C_{gg} corresponds to C_{ox} and C_{si} in series, with C_{ox} and C_{si} the gate oxide capacitance and the depletion layer capacitance respectively. In this particular case, the depletion layer is the body layer, so we have:

$$\text{Depletion depth} = T_{body} = \varepsilon_{SI}\left(C_{gg}^{-1} - C_{ox}^{-1}\right) \quad (2)$$

As we precisely know the value of the silicon thickness T_{Si}, thus, we can easily deduce T_{bridge} ($T_{bridge} = T_{Si} - T_{body}$). Fig.3-(b) shows the depletion depth versus gate bias V_g. The depletion depth corresponding to the electrical thickness of the 'body' must be determined at same gate voltage as the one used for the bridge doping extraction (here V_g=0). The value extracted, T_{body} = 21.6 nm, is 8 nm higher than the 14 nm of T_{body} defined in TCAD (Fig.1). This difference is related to the relatively low value of the bridge doping. To confirm this hypothesis, we have extracted T_{body} for different N_{bridge}, and the results are shown in Fig.4-(b. Similarly as N_{bridge} extraction, T_{body} extraction is more accurate for higher N_{bridge}: for N_{bridge} = 3.18 cm^{-3}, T_{body}= 15.7 nm, so just 2 nm higher than the expected 14 nm.). If N_{bridge} is too low ($<3.10^{17}$ cm^{-3}), the silicon film is fully depleted, including the bridge. So this means that C_{gg} capacitance depends on BOX capacitance and equation (2) can't be used (this explains why $T_{body}>T_{si}$ for low N_{bridge}). Previous simulations consider a metal electrode directly below the BOX with a mid-gap work-function. However, in real A2RAM device [3] a silicon ground plane GP acts as the back gate. To determine if the presence of GP could have an impact on our extraction methodology, we performed simulation of A2RAM including a p-type GP (doping 10^{18} cm^{-3}). Because of back gate work-function shift, C-V are not aligned (Fig.5-a): we need to apply 500 mV on the GP to superpose the C-V with the metal and the silicon back gate as in Fig.5-(a,b). In this condition, the bridge doping extracted is the same as the one without the GP (Fig.5-c). Note also that T_{body} extraction is not impacted by the GP (Fig.5-d).

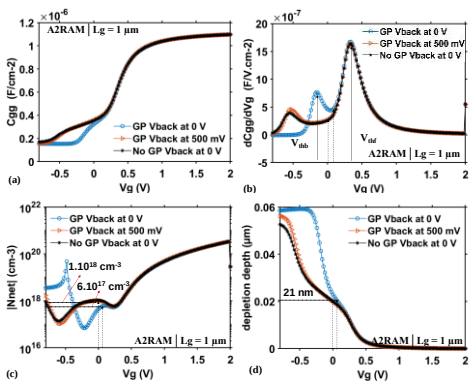

Figure 5. (a) C-V characteristic, (b) first derivative of the C-V, (c) doping function, and (d) depletion depth of the A2RAM with mid-gap back metal and with a p-type GP (TCAD simulations).

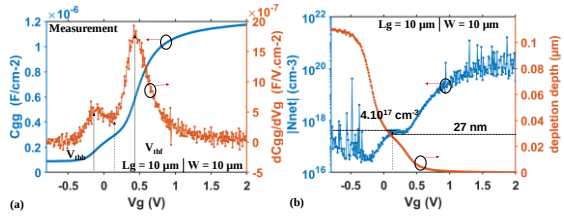

Figure 6. A2RAM experimental measurement performed on one die (a) C-V (b) first derivative of the C-V, (c)-doping function, (d)-depletion depth.

IV. EXPERIMENTAL RESULTS AND CONCLUSION

We extract the doping profile of the bridge on the samples fabricated at LETI with process flow described in [2]. The experimental C-V characteristic in Fig. 6(a) is comparable to C-V from TCAD (Fig.2-(a)). The shift of the V_{thb} that can be evidenced on Fig.6-(a) compared to Fig.2-(b) is mainly due to the presence of the GP (like in Fig.5-(b)). In consequence, the bridge doping value of $4.10^{17}cm^{-3}$ read on Fig.6-(b) is lower than the real value but the accuracy can be improved by biasing the back gate as evidenced by simulation. The T_{body} extracted (Fig.6-d) is 27nm and should be overestimated because value of doping extracted on Fig.6-c is low (Fig.4-b). We will discuss the limitations of this technique (minimum values of N_{bridge} and T_{body} which can be detected).

ACKNOWLEDGMENT

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Simulation Study on Z2FET Scalability, Process Optimization and Their Impact on Performance

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Introduction

Memory technology requires high density, large volume memory arrays in the limited chip real estate. Z2FET memory architecture has demonstrated advantages for CMOS technology implementation including compatibility and scalability, novel capacitor-less memory action, area reduction, and sharp switching characteristics. As a candidate of e-DRAM applications [1-4], minimizing cell dimensions is one of the key targets in order to deliver Z2FET competitive advantage in memory technology design and applications. The cell area is mainly determined by the Z2FET length and width. Therefore, the scaling study the Z2FET length is crucial in achieving high-density storage solutions.

In this work, we first evaluate the scalability of Z2FET concentrating mainly on real time operation, with the rest of the basic process parameters fixed at their nominal values. This is followed by long range process variability [5-6] analysis focusing on critical geometric process parameters such as Effective Oxide Thickness (EOT), channel Si thickness (Si), Length of Intrinsic Si region (Lin) and Length of Gated Si region (Lg) considered as process variability sources. The important device performance figures of merit (FoM), such as Memory Window (MW), Retention time, OFF current during hold '0' operation and ON current during read '1' operation will be characterized. The 2D TCAD structure of Z2FET was modelled using Synopsys Sentaurus [7]. Process simulator in which the TCAD model fully comply with 28 nm FDSOI technology [3-4, 8].

Memory Operation

The waveform shown in Fig. 1a is carefully designed to monitor the Z2FET functionality during the scaling down study. Previous publications [1] suggest that lower anode voltage (VA) can deliver longer retention time. So front gate voltage of VFG=1.2V and VA=1.0V are always used in this work. Since Z2FET is a timing sensitive device, to satisfy the speed requirement, a fast access speed of 6.7ns is used to perform the DRAM operation. A normal operations sequence including Program '0' (P0), Hold (H0), Read (R0), Program '1' (P1), Hold (H1), and Read (R1) are performed in this simulation pattern. The IA-Time dependence in Fig. 1b shows a typical output result for successful operation. If the output logic level of IA does not match the levels in Fig. 1b, a functionality failure is detected.

Using the current ST Microelectronics 28 nm FDSOI process as a base line technology, Lin and Lg are scaled down in our simulations. During the scaling down, it's found that all operations remain successful except for R0 operation, where '0' should be read out but the stored '0' flips and actually '1' is read out, as shown in Fig.1c. It's also found that scaling down of Lin is more critical than the scaling of Lg. Z2FET can still be working with a minimum Lg size length of 28 nm, but only if Lin remains larger than ~80 nm. The device structures simulated before and after downscaling are shown in Fig. 2a & b.

Failure Analysis

The reasons for failure can be illustrated using Fig. 3. For Lg scaling, both potential barriers in ungated Lin region and gated Lg region remains almost constant. However, this is not the case for Lin scaling as shown in Fig. 3b. The potential barrier in ungated Lin region reduces gradually with the reduction of Lin. When reaching a critical level, the shallower barrier in Lin region will not be able to stop electrons injection from the cathode, and finally pulls down the potential in Lg. This is confirmed by the simulation results presented in Fig. 3c & d.

Process Optimization

These results clearly suggest that Lin is the most critical dimension which limits the scaling-down of Z2FET. In the following discussion, we will focus on the Lin scaling only. According to the failure analysis, the optimization solution should be focusing on enhancement of electrostatics control in the ungated region. Fig. 4 compares the dimensions scaling and optimization. 1) Thinner BOX can lower down the potential in the ungated region and increase potential barrier for electrons injection. With an optimum BOX, the Z2FET can be scaled down to 64 nm. 2) Channel Si doping (Nin) profile can be adjusted in the FDSOI process. Nominally, the default channel doping is 1E16 cm^{-3}. Fig. 4 shows that the increase in the doping density can significantly improve the scalability. When the doping of Si is increased to 5E17 cm^{-3}, Z2FET can be scaled down to 52 nm. Higher doping density reduces the short channel effects, which can lower down the potential in the ungated Lin region and prevents the electrons injection from the cathode. 3) Trapped charge density (Nit) located at the interface between the Si channel and the BOX can be adjusted in the process technology. It changes the local potential and have the similar effect as the increase of back gate voltage, abs(VBG). By increasing Nit, the Lin length can be scaled down to 64 nm. 4) Thinner epitaxy can enhance the controllability of back gate bias in the ungated Lin region. Thinner epitaxy only affects the potential barrier in Lin region and has little effect on the gated Lg region. By optimizing the epitaxy thickness the Lin length can scale down to 40 nm as shown in Fig. 4, and is the most effective approach to improve the scalability.

To tolerate more margin, minimum dimension with Lin=50nm, Lg=50nm are chosen in the following FoMs vs process variability simulation. The process optimization adopts method 4), removal of Epitaxy layer (Fig. 2c).

Figures of Merits

Several important Figures of Merit are used to characterize Z2FET performance. Memory window (MW) determines the suitable VA voltage applied in the memory read operation, and is one the most important FoM for Z2FET. The second FoM that we have examined is the retention time, which determines data storage stability and memory cell refresh frequency. Since state '1' is a stable state for Z2FET we focus on the state '0' condition. In order to evaluate the power consumption, we have examined OFF current under Hold '0', and ON current under Read '1'.

In Fig. 5a-d we can observe that MW becomes ~0V and the retention time is in the range of several microseconds when Lin is scaling down to 50nm. However, the optimized 50nm DUT (the bottom layer) can restore MW to ~0.5V and retention to tens of milliseconds respectively. Fig. 5e & 5f show that the Z2FET with Lin=50nm has the largest OFF current. Although optimized 50nm DUT can bring the device back to normal working condition, it's at the price of lowered driving current (Fig. 5g & 5h). In addition, the relation between each FoM and process parameters Lg, Lin, EOT and t_{Si} can be observed in Fig. 5. The detailed description will be provided in the full paper.

Conclusion

In this paper, the Z2FET memory operation failure caused by Lin and Lg scaling has been extensively studied. Several process optimizations scenarios were proposed. Simulation results show that the reduction in the epitaxy is the most effective way to facilitate the Z2FET downscaling. Without optimization, DUTs with Lin=50nm totally lose memory action in terms of MW and retention time. The optimum DUTs can restore the operation to an acceptable level, although it is at the price of lowered driving current. The findings in this paper lay the foundation for further process optimization and matrix cell design of Z2FET based memory product.

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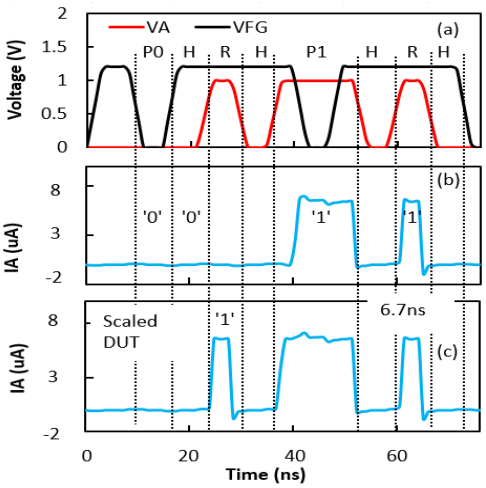

Fig. 1 a) Waveform for Z2FET used as DRAM device. Operation speed is 6.7ns to reach a 133MHz access speed. b) Both '1' and '0' can be successfully programmed and read out on nominal device. c) Same memory operation but on deeply scaled device. There is failure during read '0' operation.

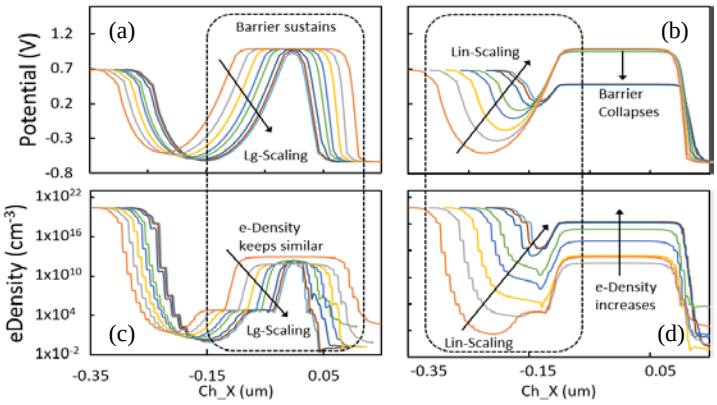

Fig. 3 Potential and electron density profile along Si channel. (a) is potential over Lg-scaling and (b) is potential over Lin-scaling. (c) and (d) are electron density over Lg-scaling and Lin-scaling respectively. All scaling ranges from 200nm to 28 nm.

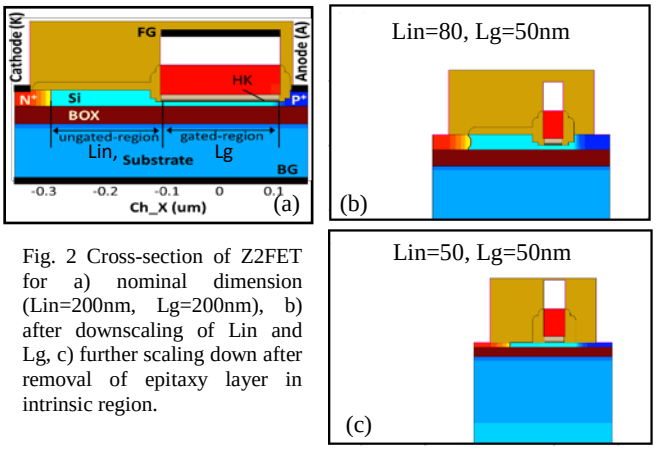

Fig. 2 Cross-section of Z2FET for a) nominal dimension (Lin=200nm, Lg=200nm), b) after downscaling of Lin and Lg, c) further scaling down after removal of epitaxy layer in intrinsic region.

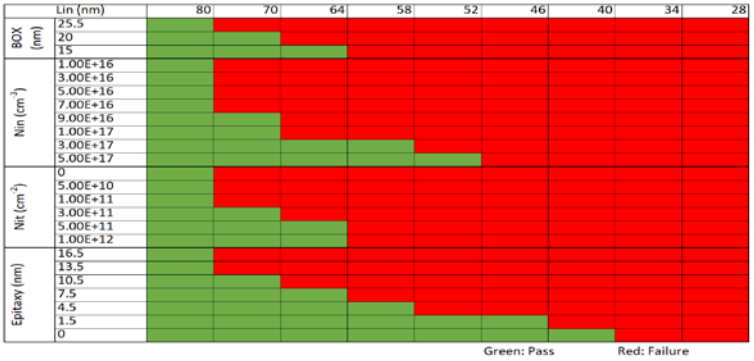

Fig. 4 Process optimization for further dimension scaling, including 1) BOX thickness reduction; 2) increase of channel Si doping (Nin); 3) Introduction of electron charges (Nit) in the surface of BOX and body-Si; 4) reduction of epitaxy layer on the ungated region. All the effects are intended to enhance the electrostatic controllability in ungated-region.

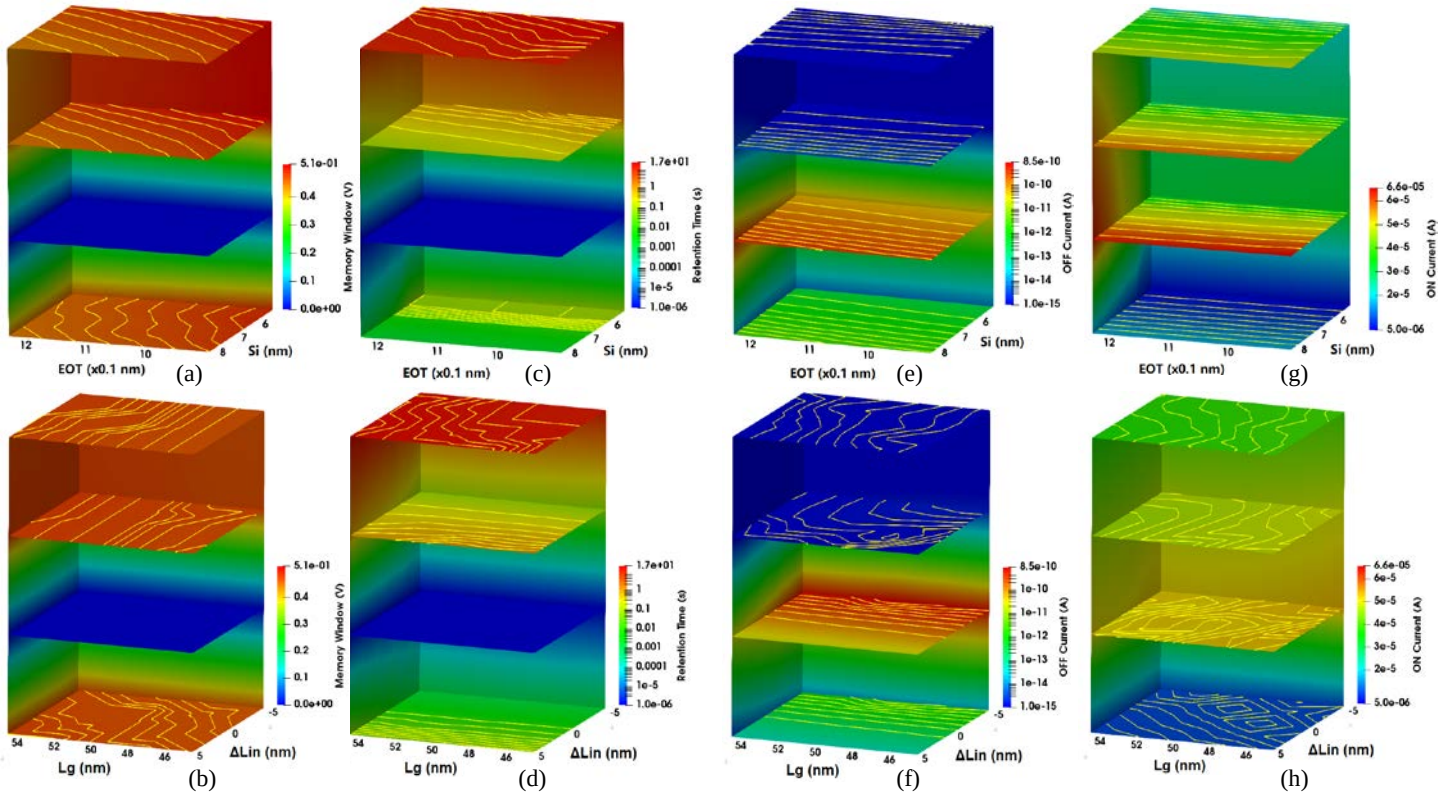

Fig. 5 Z2FET FoMs against different process variation. Four process parameters, front gate EOT, intrinsic length (Lin), front gate length (Lg) and channel Si thickness (Si), are selected as they are considered to have the most significant impact on Z2FET performance. Four FoMs are used to characterize Z2FET characteristics. (a) and (b) are memory window; (c) and (d) are retention time extracted; (e) and (f) are OFF current (during Hold '0' operation), and (g) and (h) are ON current (during Read '1' operation). The four layers in each figure indicates different Lin length: 200nm, 100nm, 50nm, and optimized 50nm respectively, since Lin length is limiting the further downscaling.

Z^2-FET Memory Matrix in 28 nm Technology

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***Abstract*—The article puts forth the comparison between the two available options of Z^2-FET in 28 nm technological node, i.e. thin and thick gate oxide. Ideally, the performance of Z^2-FET with thinner oxide would overcome the one with thicker, if the gate leakage in not taken into account. TCAD mixed mode simulations show that both thin and thick oxide can be implemented successfully in the DRAM array formation.**

Keywords-Z²-FET; capacitorless; 1T-DRAM; memory matrix; retention time

I. INTRODUCTION

Z^2-FET capacitorless 1T- DRAM (Z^2-RAM) has emerged as a possible candidate for designing low power, low cost and efficient embedded DRAM for IoT [1-2]. In this paper, we compare the performance of the Z^2-RAM designed with thin and thick front gate oxide with by TCAD simulations calibrated on experimental data in the 28 nm SOI technology node.

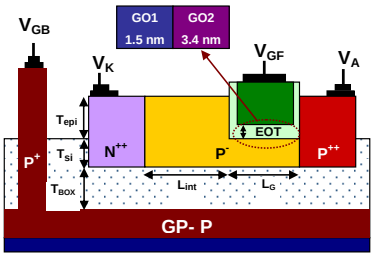

Figure 1. Schematic of Z^2-FET with two different EOTs.

II. DEVICE DISCRIPTION

The schematic of Z^2-FET device fabricated and simulated [3] in the 28 nm technology node is shown in Fig. 1. Z^2-FET is a partially gated PIN diode based on FDSOI technology. Film thickness (T_{si}) is 7 nm, epitaxial layer thickness (T_{epi}) is 15 nm and buried oxide thickness (T_{BOX}) is 25 nm. The effective oxide thickness (EOT) for GO1 is 1.5 nm and for GO2 is 3.4 nm. P-type ground plane (GP-P) is used for back biasing the device. L_g and L_{int} are the lengths of gated and ungated regions, respectively.

III. MEMORY PERFORMANCE

To program state '1' and state '0' different combinations of anode voltage (V_A) and front gate voltage (V_{GF}) are used [2]. Cathode is grounded and the back-gate voltage (V_{GB}) is kept at -1 V. Fig. 2 exhibits the performance of Z^2-RAM memory cell in terms of the ratio of read '1' current (I_1) and read '0' current (I_0) for both thin GO1 and thick GO2 gate oxide.

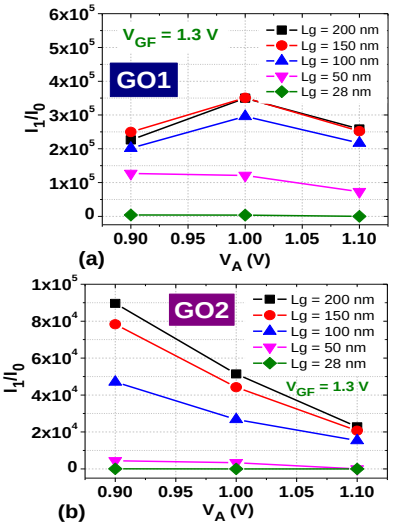

Figure 2. Read Margin (I_1/I_0) of (a) GO1 and (b) GO2 Z2-RAM for various gate legnths (Lg = 200 nm to 50 nm).

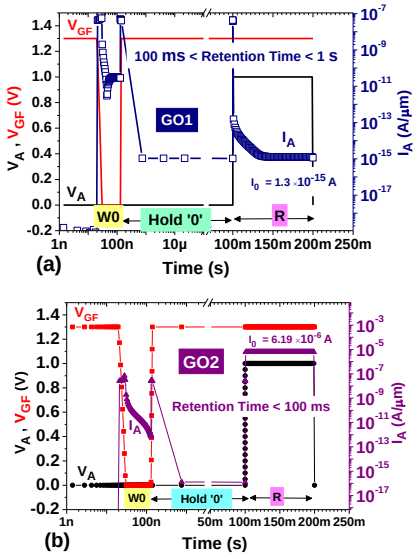

Figure 3. Retention-time for (a) GO1 and, (b) GO2 Z^2-RAM.

Both GO1 and GO2 devices (L_g = 200 nm, L_{int} = 200 nm) deliver high current margin ($I_1/I_0 > 10^4$) at a read voltage (V_A) of about 1 V. I_1/I_0 for GO1 is almost one order of magnitude higher compared to GO2 due to better electrostatics control with thinner EOT. Fig. 3 presents the retention of state '0', which is meta-stable, whereas state '1' is stable [2]. To write '0', a 100 ns writing pulse is applied at V_{GF}, followed by a hold time of 100 ms. Thereafter, a 100 ms long read pulse is applied to evaluate the state of the programmed cell. In case of GO1 (Fig. 3a) read current is low (10^{-15} µA/µm) confirming the retention of state '0', whereas for GO2 (Fig. 3b), the reading current is high and the state '0' is lost after a hold of 100 ms. Note that in these simulations, the gate leakage current was not included. If activated, the gate leakage may affect the stable state 1 and degrades the retention time from ideal behavior for thin oxide (GO1) technology.

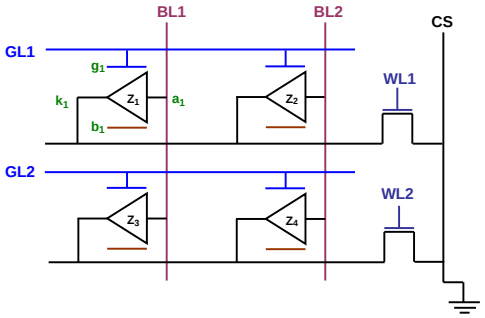

Figure 4. Layout of Z²-RAM 2×2 matrix (L_g = L_{int} = 200 nm).

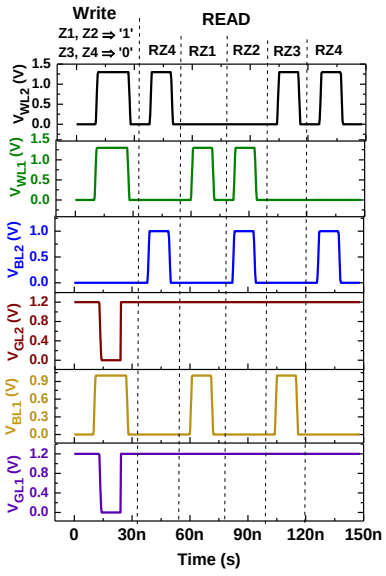

Figure 5. Applied signals to program cells Z_1 and Z_3 with state '1' and, Z_2 and Z_4 with state '0' followed by read operation.

IV. Z²-RAM IN MATRIX DESIGN

The design of Z²-RAM (Z_1, Z_2, Z_3 and Z_4) in 2x2 matrix array is shown in Fig. 4. A single nMOSFET selector is connected to the common cathode of each row. The front gates of each row are connected together through the gate line (GL) and, anodes of each columns are tied together to form the bit line (BL). WL1 and WL2 are the biases applied to the gate of the MOS selectors to select/deselect individual row.

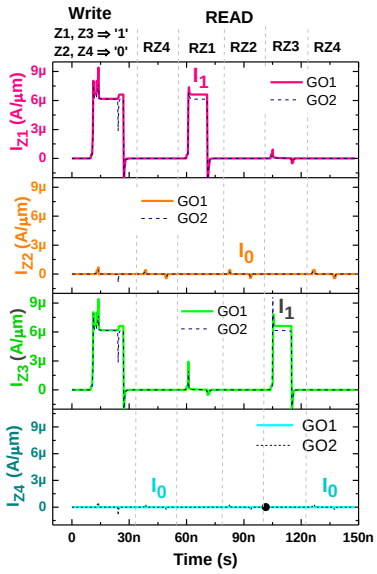

Figure 6. Response of the applied signals shown in Fig. 5.

A set of signals (Fig. 5) is applied to the six terminals of the Z²-RAM matrix to program the cells Z_1 and Z_3 with state '1' and cells Z_2 and Z_4 with state '0', followed by read signals to read each cell individually. The response (Fig. 6) shows that all the cells are being read correctly without any error, e.g. during operation RZ1, the current through Z_1 cell (I_{Z1}) is high (I_1) and remaining all currents are low. Both GO1 and GO2 are successfully implemented in the DRAM matrix configuration.

Simulations in GO1 technology has shown better read margin, retention and higher scalability due to strong electrostatics compared to GO2. Note that in experiments, preliminary results showed that thinning of gate oxide might result in the degradation of (i) retention due the gate leakage increase, and (ii) the surface properties leading to higher variability. In practice either of GO1 or GO2 options can be optimized by tuning the biases to design the low-cost and efficient DRAM.

ACKNOWLEDGMENT

This work was supported by the European project REMINDER.

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Evaluation of thin-oxide Z^2-FET DRAM cell

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***Abstract*— Advanced 28 nm node FDSOI Z^2-FETs with thin top-gate insulator are characterized as capacitor-less DRAM cells. Results demonstrate effective Z^2-FET memory behavior for narrow devices (below 1 µm). As compared with thicker gate oxide Z^2-FETs, thinning the insulator yields lower performance in terms of retention, variability and stability of the logic states during holding.**

Keywords- 1T; capacitor-less; FDSOI; DRAM; feedback; memory; PIN; Sharp switch; Z^2-FET.

I. INTRODUCTION

The traditional 1 transistor – 1 capacitor (1T-1C) DRAM memory cell is approaching its scaling limit [1]. Novel capacitor-less cells have been proposed [2-5] in order to further increase the DRAM integration density and limit the fabrication costs, key aspects for embedded applications.

A promising solution is the Z^2-FET DRAM cell whose basic structure is depicted in Fig. 1. Z^2-FET is similar to a conventional PIN diode in which the intrinsic region is partially covered by a front gate (FG); below the whole device, a highly-doped ground-plane (GP) acting as back gate is implemented. As opposed to conventional diodes, a complementary gate biasing scheme (V_{FG}>0V and V_{BG}<0V) is employed to induce high vertical energy barriers and block the current flow. Only when the anode voltage (V_A) is high, carriers start to diffuse and, at $V_A = V_{ON}$, the Z^2-FET abruptly recovers the diode behavior, Fig. 2a. The energy barrier control, defining the current level and thus the DRAM logic states, is achieved by altering the inner body carrier concentration: '0'-state corresponds to a very low electron concentration whereas the '1'-state reflects high population. The stored charge is programmed (W) by: forward biasing the diode (V_{FG} = 0V and V_A > 0V), which introduces carriers (W_1), or by capacitive coupling (V_{FG} = 0V and V_A = 0V) which evacuates them (W_0). State reading, R, is accomplished by simply pulsing the anode terminal (V_A>0V). During holding operations, available body carriers are retained thanks to the gate-induced potential wells (V_{FG}>0V and V_{BG}<0V). Exhaustive information regarding the Z^2-FET as 1T-DRAM can be found in [7].

In this work, characterization results of narrow 1T-DRAM Z^2-FET cell on 28 nm FDSOI [6] with ultrathin gate oxides are reported.

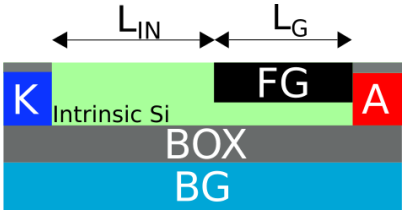

Fig. 1. Parameters of Z^2-FET DRAM cell : $L_G = L_{IN}$ = 200 nm (gated/ungated region length), W = 100 nm, EOT ≈ 1.5 nm, t_{Si} ≈ 7 nm, t_{Epi} ≈ 15 nm (ungated epitaxy thickness) and t_{BOX} ≈ 25 nm. $N_{body} \approx 10^{16}$ cm^{-3}, $N_{BG} > 10^{18}$ cm^{-3} and $N_{A/K} > 10^{21}$ cm^{-3}.

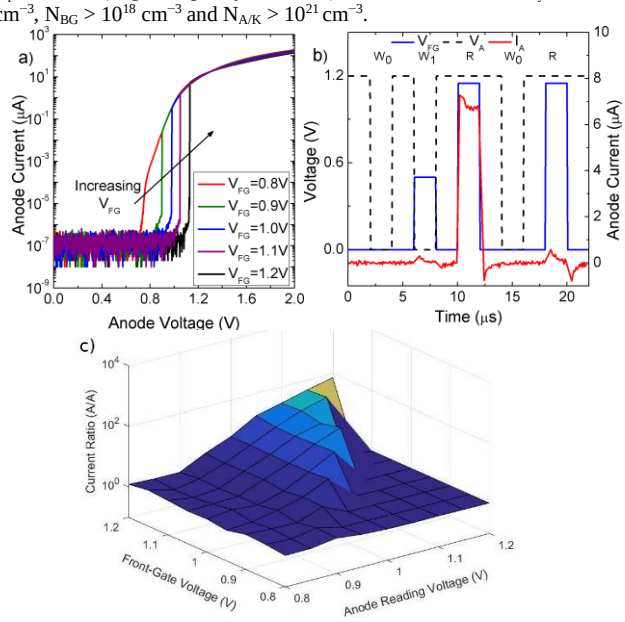

Fig. 2. a) DC $I_A(V_A)$ sweeps for various V_{FG}. b) Transient anode readout current for a W_0-W_1-R-W_0-R sequence demonstrating valid DRAM operation. t_{RISE} = t_{FALL} = 50 ns and t_{WIDTH} = 2 µs. c) Current ratio between logic states as a function of V_{FG} and V_A. V_K = 0 V and V_{BG} = -1 V. Fabrication parameters are shown in Fig. 1.

II. SHARP SWITCH AND DRAM VALIDATION

DC $I_A(V_A)$ curves, probing the typical Z^2-FET abrupt switch, are obtained by applying a sufficiently slow anode ramp signal, Fig. 2a. As also happens for thick insulators [5,7], V_{ON} shifts to larger voltages as the

front-gate bias is increased since the required potential to overcome the anode-body barrier is higher. To verify the Z^2-FET DRAM operation a W_0-W_1-R-W_0-R pattern is applied to the cell. The sequence timing was optimized to reduce the leakage current and RC parasitics discharges in the setup. Fig. 2b illustrates the anode current readout. The current ratio is high (with $I_1/I_0 \approx 44$, Fig. 2c) and the memory behavior is correct: two distinct readout current levels are achieved according to the last programmed state. It is also worth noting that the V_A bias can be smaller for writing than for reading, allowing more tenability and power saving.

III. Memory Window and Retention Time

The memory window (defined as the V_{ON} shift between logic states) is extracted by monitoring the current level for different anode reading pulse heights. **¡Error! No se encuentra el origen de la referencia.**Fig. 3a shows the experimental DRAM Z^2-FET memory window with the dashed line being the reading anode voltage used in Fig. 2b.

The retention time is characterized with several $W_{1/0}$-H-R bias patterns. The holding (H) time is gradually increased, from 20 µs to 70 ms, to monitor if the previously programmed state ($W_{1/0}$) is still available (R) afterward. Fig. 3b illustrates that the Z^2-FET correctly holds the logic state for around 200 µs. Wide Z^2-FET cells with thicker top dielectrics yield longer retention times above tens of ms [8]. Notice also that, unexpectedly [5,7], the stable state during holding seems to be the '0'-state (logic '1' falls toward the '0'). However, for continuous reading, the Z^2-FET cell always ends up driving the high-current '1'-state (not shown). This surprising result, not observed in Z^2-FET with thicker gate dielectrics, is thought to be a consequence of the thinner oxide: the increased vertical electric field reinforces the energy barriers preventing the current flow ('0'-state). Additional recombination and/or evacuation mechanism, e.g. direct tunneling, might also affect the memory operation. Nonetheless, during reading, the carrier injection can easily counteract any carrier gate leakage or recombination finally leading to the '1'-state.

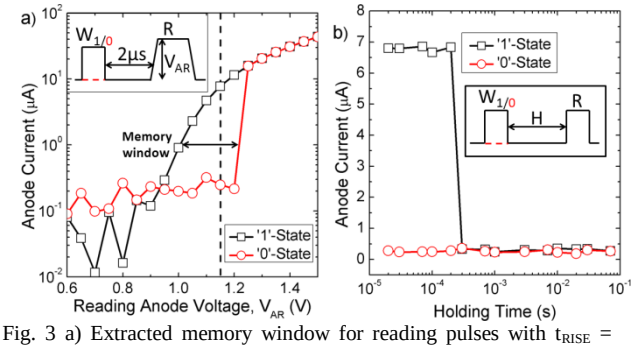

Fig. 3 a) Extracted memory window for reading pulses with t_{RISE} = t_{FALL} = 50 ns and t_{WIDTH} = 2 µs. Dashed line corresponds to anode reading bias in Fig. 2b. b) Retention time for V_{AR} = 1.15 V. V_{FG}=1.2V, V_K = 0V and V_{BG} = -1V.

IV. DC Variability

Fig. 4 shows the spreading of Z^2-FET parameters in DC: a) ON voltage, b) OFF voltage, c) turn-on current, and d) turn-off current. A set of 56 devices were studied for the wafer-level variability at V_{FG} = 1.2 V. Notice that the switching V_{ON} voltages range from 0.95 V to 1.3 V and turn off voltages V_{OFF} range from 0.75 V to 0.9 V. Similarly, the turn-on currents vary from 1 to 20 µA although the turn-off currents remain low. This variability makes difficult the optimization of the biasing conditions in transient mode for the memory performance.

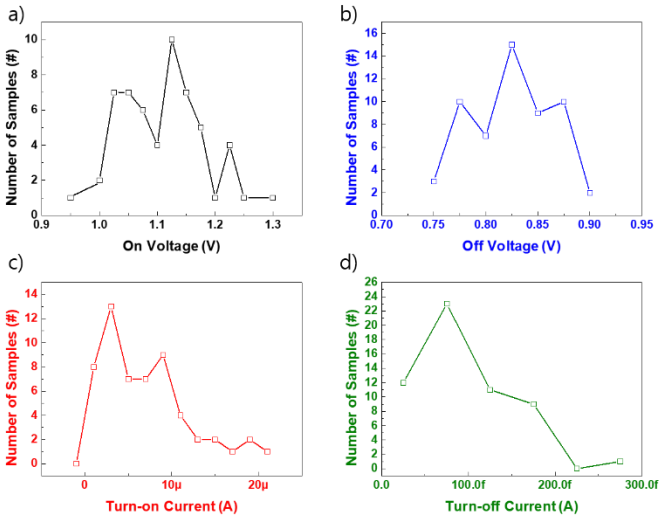

Fig. 4 Statistical distributions of a) ON voltage, b) OFF voltage, c) turn-on current, and d) turn-off current for 56 Z^2-FETs. L_{IN} = L_G = 200 nm and W = 100 nm. V_{BG} = -1 V, V_{FG} = 1.2 V and V_K = 0 V.

Conclusions

Advanced narrow Z^2-FET memory cells with ultrathin gate oxide have been experimentally characterized. The memory operation is successfully demonstrated despite a performance drop with respect to previous results, due to increased variability and vertical electric field.

Acknowledgment

H2020 REMINDER European project (No. 687931) is thanked for financial support.

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Study of the 1D Scattering Mechanisms' Impact on the Mobility in Si Nanowire Transistors

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***Abstract*— The most extensive research of aggressively scaled nanoelectronic devices involves the inclusion of quantum confinement effects and their impact on the performance of new architectures. This work implements a set of multisubband phonon and impurity scattering mechanisms and the Kubo-Greenwood theory in order to study the mobility in Si nanowire structures.**

Keywords-Phonon Scattering; Impurity Scattering; Kubo-Greenwood Formalism; Matthiessen rule; Nanowire FETs

I. INTRODUCTION

Nanowire transistors (NWTs) are being considered as an alternative to replace standard CMOS technology due to their better charge transport control in the channel. In the simulation framework, it has been mandatory to develop different schemes in order to reduce the computational effort of the quantum transport theories. One of the most popular trends is to incorporate into semi-classical simulators models with refined macroscopic quantities and physical analysis accounting for important quantum effects. The approach considered herein combines quantum effects with the semi-classical Boltzmann transport equation (BTE) using the relaxation time approximation and the Kubo-Greenwood formalism [1]-[3]. This strategy provides reliable mobility values at low-field near-equilibrium conditions, based on the rates of the relevant scattering mechanisms governing multisubband transistors in quantum wires [4]. In this work, we study the effect of quantum confinement on the electron mobility in NWTs including phonon and impurity scattering. In addition, we analyze the impact of the nanowire size and geometry on the transport properties.

II. METHODOLOGY

Long-channel simulation is a convenient framework for assessing low-field electron mobilities in devices which incorporate a confining structure, such as gate-all-around. It directly studies the effect of charge confinement on transport as a function of out-of-plane (lateral) applied electric field. The channel is assumed to be infinitely long and the electric field in the transport direction is fixed to a low value. First, multiple cross sections of the device are simulated using the coupled 3D Poisson and 2D Schrödinger solver (Fig. 1) integrated in the TCAD simulator GARAND from Synopsys. Second, the potential and the corresponding eigenfunctions of the subbands are included in the particular scattering rates, whose expressions have been directly developed from Fermi's Golden Rule accounting for the multi-subband quantization in the normal to the wire plane of confinement. In this work, we have included: *(i)* acoustic phonons which are considered within the elastic equipartition approximation in the short wave vector limit; *(ii)* optical phonons including fixed parameters for the different branches; and *(iii)* ionized impurity scattering which is relevant for all types of doped nanostructures due to the short range Coulomb interaction with the carriers. The mobilities are calculated by applying the Kubo-Greenwood formula to the relaxation times corresponding to the linearized BTE. Finally, Matthiessen's rule [5] is used to combine the scattering probabilities, and so both the individual and the total mobilities of the simulated device are analyzed separately.

III. RESULTS

Fig.1 shows the device parameters for the NWTs herein analyzed. Both square and circular shapes are studied. Despite NWTs start to have a bulk-like behavior only at diameters higher than 8nm, we use bulk effective mass values. Fig.2 presents the scattering rates as a function of the total energy for electrons calculated for impurity, acoustic phonon, and optical phonon (including f-, g-type and total) scatterings for a square NWT with 3nm (top) and 8nm (bottom) widths for a [100] orientation and 20 subbands. The multisubband effects in the scattering rates are generally more pronounced for smaller wire width. This is associated with the higher energy difference between the lower and upper subbands (Fig.3), which minimizes the possible electron transitions between subbands. This fact results in the reduction of the mobility (both the individual and the total) for higher confined devices (Fig.4). Moreover, for these particular devices, the mobility is limited by acoustic phonon scattering due to its high scattering

rates, especially at low energy (Fig.4). Finally, Fig.5 shows the total mobility of square and circular NWTs as a function of the cross section area: the latter affects directly the subband energy levels and eigenfunctions. Consequently, the change in these parameters may enhance or degrade the mobility substantially. The results presented in Fig. 5 are in good agreement with our previous work [6] where we observed higher mobile charge in circular NW in comparison to the square device.

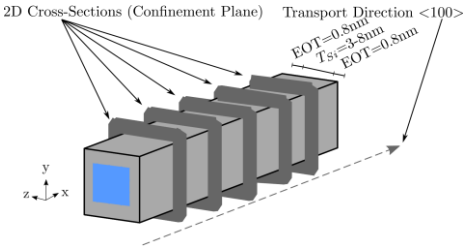

Figure 1. NWT structures analyzed in this work with widths ranging from 3nm to 8nm. The coupled 2D Schrödinger and 3D Poisson equation are solved for each cross-section (confinament plane) and then the scattering rates are calculated accounting for the potential and the eigenfunctions for each subband.

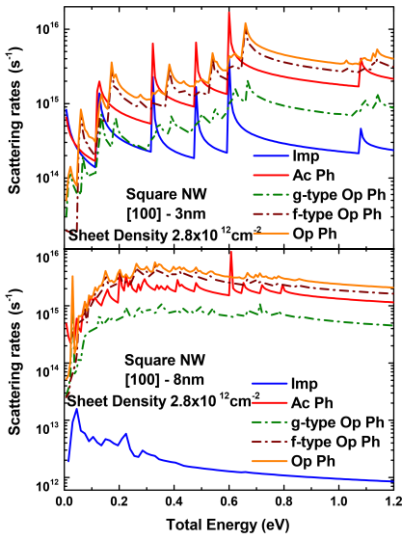

Figure 2. Impurity scattering rate (Imp) as well as acoustic (Ac Ph), optical (including g-type, f-type and total (Op Ph)) phonon scattering rates as a function of the total energy for a square NW with 3nm (top) and 8nm (bottom) width for [100] orientation and sheet density of $2.8x10^{12}cm^{-2}$.

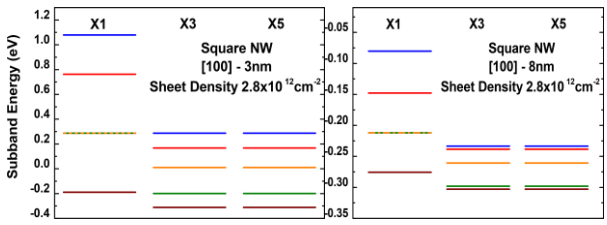

Figure 3. Energy levels for a square NW with 3nm (top) and 8nm (bottom) width for [100] orientation and sheet density of $2.8x10^{12}cm^{-2}$, showing band splitting for the set of valleys X1, X3 and X5.

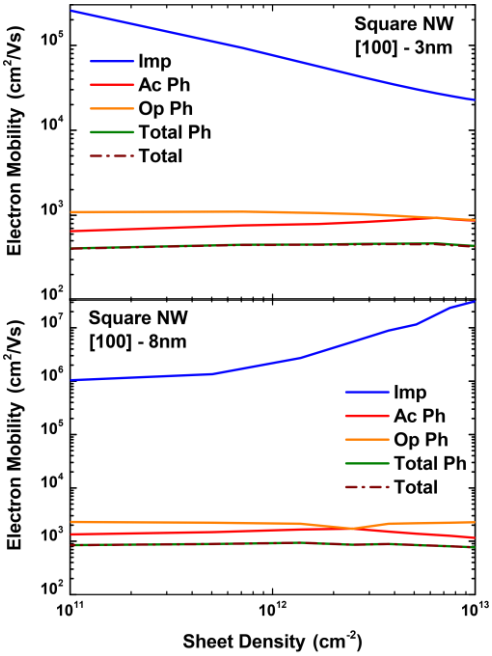

Figure 4. Electron mobility as a function of the sheet density considering the impurity (Imp) as well as the acoustic (Ac Ph), optical (Op Ph), and total (Total Ph) phonon scattering separately as well as combined for a square NW with 3nm (top) and 8nm (bottom) width for [100] orientation.

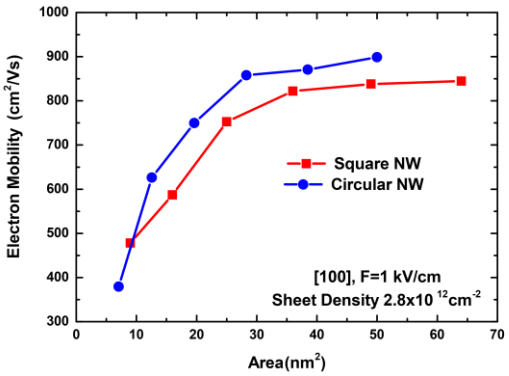

Figure 5. Electron Mobility as a function of the area for a square and circular NW with sheet density of $2.8x10^{12}cm^{-2}$.

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3D Multi-Subband Ensemble Monte Carlo simulation of ‹100› and ‹110› Si nanowire FETs

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***Abstract*— This work presents a comprehensive study of MOS transistors based on Si nanowires with ‹100› and ‹110› channel orientations employing our 3D Multi-Subband Ensemble Monte Carlo simulator. The results show that ‹100› oriented devices provide larger current and mobility than their ‹110› counterparts. The differences in the spatial charge distribution are analyzed and explained in terms of the population of the different valleys.**

Keywords-component; Monte Carlo simulation; multi-subband; Si nanowire; channel orientation.

I. INTRODUCTION

Gate-All-Around (GAA) transistors based on cylindrical nanowires provide the best possible electrostatic control of the channel charge and, as a consequence, can allow the ultimate scaling of device gate length. In this paper, we compare the performance of transistors based on Si nanowires with ‹110› (traditional for Si MOSFETs) and ‹100› channel orientations, employing a 3D Multi-Subband Ensemble Monte Carlo simulator.

II. SIMULATION SETUP

The 3D simulation tool employed in this work is based on the space-mode approach: it solves in a self-consistent way the 3D Poisson equation, the 2D Schrödinger equation in several device cross sections along the channel and the 1D Boltzmann equation through the Monte Carlo method [1, 2]. Electron band structure is described employing the effective mass model with non-parabolic corrections [3]. The 1D Monte Carlo simulation includes carrier scattering by acoustic and optical phonons [4]. The same simulator also allow the calculation of carrier mobility by restricting the simulation to the channel region (assuming infinite length) and applying a constant drift electric field. The simulated devices are GAA FETs based on cylindrical Si nanowires with channel along the ‹100› or ‹110› directions. The nanowire diameters considered for this study are D=4 nm, 6 nm and 8 nm with channel length L_G=14 nm. The gate oxide (SiO_2) thickness is T_{ox}=1 nm, the channel is considered undoped and a midgap metal is employed as gate material. The doping density in the source and drain regions is $N_{SD}=1\times10^{20}$ cm^{-3}.

III. RESULTS

The computed drain current (Fig. 1) is larger for wider devices, as expected given the larger area available. Moreover, the channel orientation has a noticeable effect, with ‹100› devices always providing more current than the corresponding ‹110› devices, especially for the narrower ones. To check a possible cause for this behavior, we computed the electron mobility μ_n for the different structures (Fig. 2). The results show that μ_n decreases for larger values of the inversion charge density and for the devices with smaller diameter. Moreover, consistently with [5], the mobility of ‹100› channels is always larger than ‹110› channels. On the contrary, the linear inversion charge density below the center of the gate is larger for the latter, as shown in Fig. 3. In any case, Fig. 1 makes it clear that the transport advantage of ‹100› orientation (here represented by larger mobility) is more relevant than the lower charge density and gives rise to a better DC

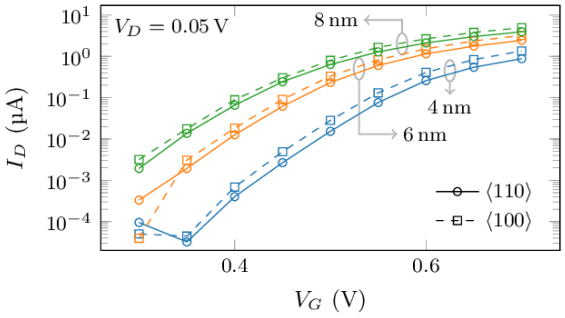

Figure 1. Output characteristics of ‹100› and ‹110› devices with different diameters.

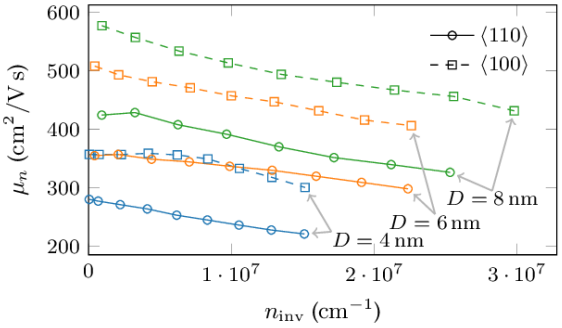

Figure 2. Computed electron mobility for the different devices, as a function of the inversion charge density.

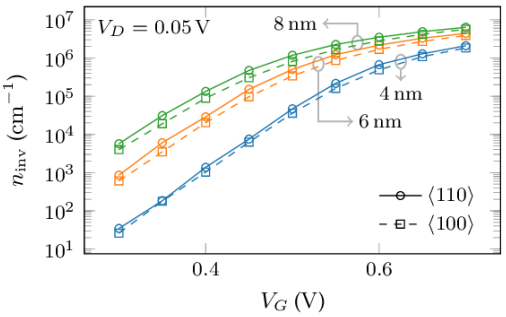

Figure 3. Inversion charge density as a function of gate bias.

performance. Next, we considered the cross sectional charge distribution in the middle of the channel. To perform a fair comparison of the different devices, we applied the same gate voltage overdrive V_G-V_{th}=0.2 V, where the threshold voltage V_{th} has been extracted for a fixed current. The results (Fig. 4), show that in ‹100› devices the inversion charge is distributed symmetrically in the cross section and the peak of the distribution corresponds to the geometrical center of the channel (Fig. 4 b, d, f). Only for larger values of the V_G and the largest diameter, the charge moves towards the gate and several peaks appear [1]. On the contrary, ‹110› devices present a visible in-plane asymmetry that can be quantified by the ratio $\langle y^2\rangle/\langle x^2\rangle$ of the variance of the distribution in

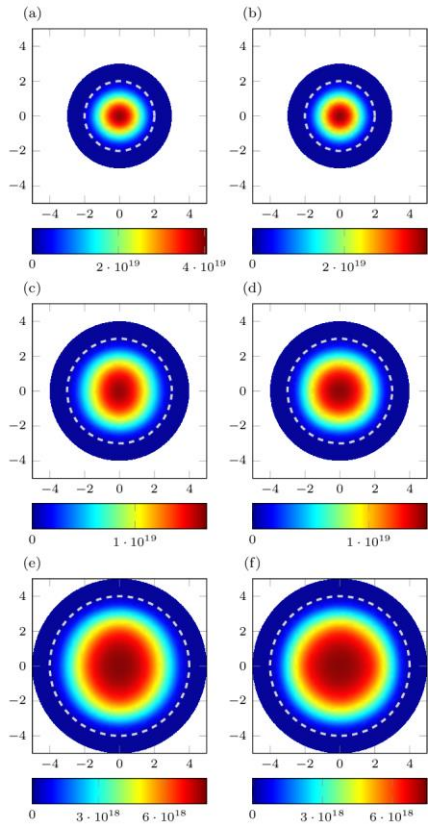

Figure 4. Inversion charge distribution for D=4 nm (a) (b), D=6 nm (c) (d), D=8 nm (e) (f); for ‹110› orientation (a) (c) (e) and ‹100› orientation (b) (d) (f), for V_G=V_{th}+0.2 V.

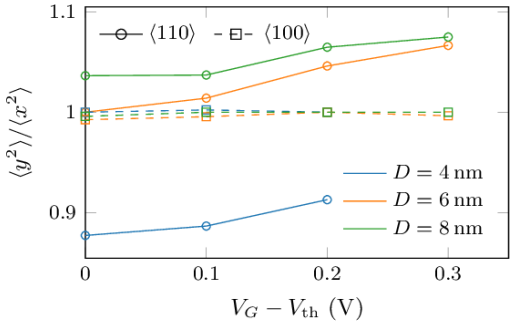

Figure 5. Ratio of y and x spreading of charge distribution.

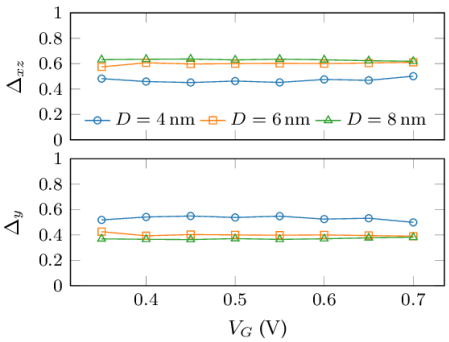

Figure 6. Fraction of inversion charge in each set of valleys for different ‹110› devices.

the vertical (y) direction and the horizontal (x) direction (Fig. 5). Such ratio is 1 (up to the numerical accuracy) for ‹100› devices while in ‹110› devices it is >1 for D=6 nm and 8 nm and <1 for D=4 nm. This can be explained by the different valley occupation (Fig. 6): for D=4 nm, the doubly degenerate Δ_y valleys are the most populated ones, and their effective mass is larger in the y than in the x direction. On the contrary, for D=6 nm and 8 nm, the fourfold degenerate Δ_{xz} valleys represent the bigger contribution to the total inversion charge, and their effective mass is larger in the y than in the x direction.

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Innovative Tunnel FETs architectures

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1. Abstract

We propose three innovative SOI Tunnel FET architectures. They are evaluated and compared with a standard TFET structure using Sentaurus TCAD. The extension of the source (anode) at the bottom of the body generates vertical band-to-band tunneling with a very steep slope and higher I_{ON} than lateral tunneling, but only for gate lengths longer than 100 nm. Using a heavily doped boron thin layer at the bottom increases I_{ON} even for aggressive gate lengths. Implementation of a tip in the source provides performance similar to the reference TFET.

Keywords: Tunnel FET, TFET, SOI, TCAD, tunneling, BTBT, Extended-Source, Pure Boron, Sharp Tip.

2. Introduction

Diminution of energy consumption is one of the major challenges to be faced by beyond CMOS devices. The most effective path for power reduction in ICs is through V_{DD} reduction [1]. Low Subthreshold Swing (SS), low I_{OFF} current and high I_{ON}/I_{OFF} are crucial for ultra-low power applications. Unfortunately in CMOS technology SS cannot be reduced below the 2.3 kT/q limit and I_{OFF} increases at low V_{TH}. Besides, MOSFET scaling is reaching its limits, creating the need for developing new device concepts such as steep slope devices [2]. Standard tunnel FETs (TFETs) are p-i-n gated diodes [3] based on a different carrier injection mechanism compared to CMOS devices. TFETs rely on band-to-band tunneling (BTBT) [4] enabling very low OFF current and have the theoretical capability of achieving a SS lower than 60 mV/dec (at 300K). These characteristics make TFETs promising candidates for ultra-low power applications. In practice it has been proven extraordinarily difficult to get a steeper slope, regardless of materials, architectures or specific fabrication steps considered to increase the tunneling probability [5]. Best cases show that SS below 60 mV/dec is only feasible for a narrow range of current values and have low current drive.

3. Proposed TFET architectures

We focus on TCAD simulation of planar TFET architectures with different optimizations at the source junction to increase the performance, specifically: i) **Extended-Source TFET** (**ES**-TFET) with extension of the source in the intrinsic region, ii) **Pure Boron TFET** (**PB**-TFET) with a higher dopant concentration in a thin bottom layer and iii) **Sharp tip TFET** (**Tip**-TFET) with enhance electric field at the source junction. 2D TCAD simulations of TFETs with silicon homo-junctions were performed using the Nonlocal Path Band-to-Band model couple to classical Drift-Diffusion equation with constant mobility [6]. Fig. 1a shows the standard TFET which serves as reference. The parameters common to all devices are: L_G from 500 nm down to 15 nm, T_{BOX} = 145 nm, EOT = 1.18 nm, intrinsic region L_{IN} = 20 nm, Φ_{gate} = 4.0 eV and dopant concentration in S/D of $N_D = N_A = 10^{20}$ cm^{-3}. ES-TFET (Fig. 1b) presents the extension of the source at the bottom of the body with $N_{ext} = N_A$, which creates a large contribution of the vertical BTBT to drain current. The PB-TFET (Fig. 1c) has a heavily doped 1 nm pure boron layer (simulated using $N_A = 10^{21}$ cm^{-3}) at the bottom [7], enabling the simultaneously presence in the channel of electrons and holes for very thin T_{Si} to increase the ON current. The Tip-TFET (Fig. 1d) includes a sharp tip in the source to enhance the source electric field and tunneling current.

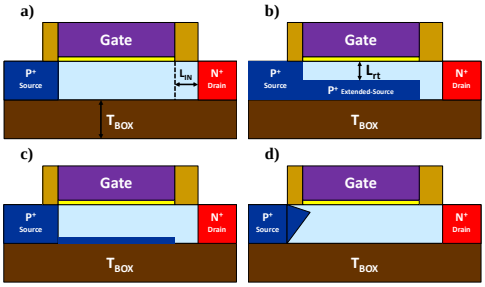

Fig. 1: TFETs structures: *a)* Standard reference TFET; *b)* Extended-Source TFET; *c)* Pure Boron TFET and *d)* Sharp tip TFET.

4. Extended-Source TFET

The ES-TFET shows a higher ON current and steeper slope (Fig. 2) for the small distances between the extension and the gate oxide (L_{rt} = 3 nm). The gate terminal starts to lose the electrostatic control of the vertical BTBT when increasing L_{rt} and there is a severe degradation of the slope and the I_{ON}. Fig. 3a clearly establishes how the ES-TFET architecture outperforms the standard structure for a long channel length because of vertical BTBT occurs in the whole source extension.

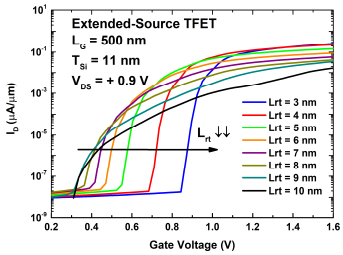

Fig. 2: $I_D(V_{GS})$ curves of Extended-Source TFET for a given T_{Si} = 11 nm and different depths of extension with regard to the gate (L_{rt}).

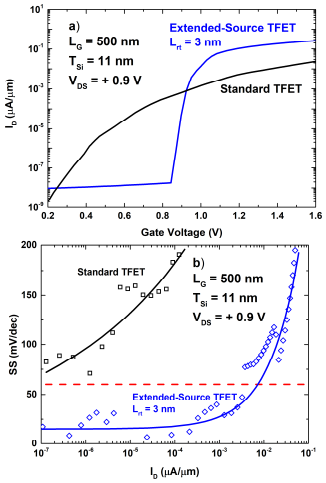

Fig. 3: Comparison of: *a)* $I_D(V_G)$ curves and *b)* Figure of merit $SS(I_D)$ for standard and Extended-Source TFET.

The SS extractions in Fig. 3b confirm the extension of SS below 60 mV/dec (over ~ 4 decades) for the ES-TFET. In the standard TFET the current is generated by BTBT carrier injection at the source/channel junction and is independent of L_G (Fig. 4). However, for ES-TFET I_{ON} magnitude depends on the length of the extension of the source into the channel, which means that for advanced nodes (L_G < 100 nm) the current will be degraded as shown in Fig. 4.

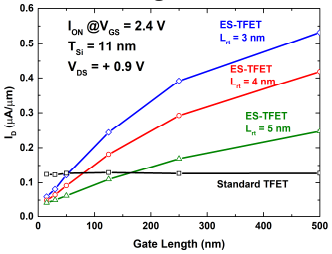

Fig. 4: $I_{ON}(L_G)$ for standard and Extended-Source TFET. Short gate lengths (< 100 nm) provide better I_{ON} for standard TFET.

5. Pure Boron TFET

PB-TFET shows an improved electrostatic control with narrow channels and a 10X I_{ON} increase (Fig. 5a) respecting the ES-TFET. SS reaches values below 60 mV/dec for 3 decades (Fig. 5b). Heavily doped boron layer increases the vertical BTBT, and even for short gate lengths (L_G < 100 nm) PB-TFET has better performance than the reference device (Fig. 6).

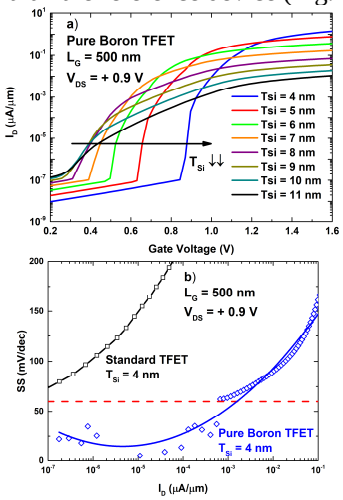

Fig. 5: *a)* $I_D(V_G)$ curves of PB-TFET for different T_{Si}; *b)* Figure of merit $SS(I_D)$ for standard and PB-TFET.

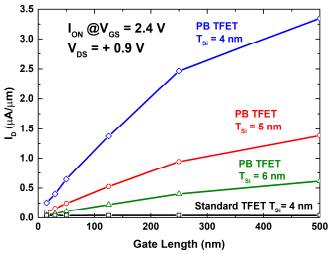

Fig. 6: $I_{ON}(L_G)$ for standard and Pure Boron TFET for different T_{Si}.

6. Sharp Tip TFET

The designing of a sharp tip in the source junction has not significant impact in the I_{ON} and the SS with respect to the standard TFET (Fig. 7). Besides, the Tip-TFET produces only lateral BTBT and the current is independent on L_G. The tip generates a shift in the position of maximum electric field and the BTBT is improved where the overlap of this field and the P^+ region takes place (Fig. 8).

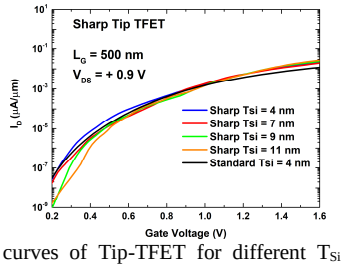

Fig. 7: $I_D(V_G)$ curves of Tip-TFET for different T_{Si} and Standard TFET for T_{Si} = 4 nm.

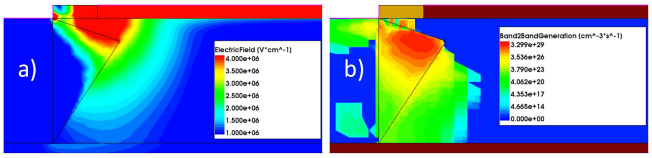

Fig. 8: Sharp Tip-TFET: *a)* Emax and *b)* BTBT generation.

7. Conclusion

Among the three innovative TFET architectures studied, the ES-TFET exhibits a SS below 60 mV/dec (over ~ 4 dec.) and higher I_{ON} current for small L_{rt}. For L_G smaller than 100 nm the doped extension length mitigates this I_{ON} enhancement. The use of a thin layer of boron heavily doped in PB-TFETs for small T_{Si} solves the I_{ON} degradation at small gate lengths. Implementation of a sharp tip in the source (Tip-TFET) does not show significant difference in relation to the standard TFET. The most promising architecture for further studies is the Pure Boron TFET.

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TFET-based Inverter Performance in the Presence of Traps and Localized Strain

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***Abstract*—This paper investigates the circuit-level performance of an inverter made by n- and p-type tunnel field-effect transistors (TFETs), integrated on the same InAs/AlGaSb technology platform, in the presence of interface traps and localized strain. Interface traps are found to induce a significant degradation of the voltage gain, noise margin and transient performance. The effect of localized strain at the source/channel heterojunction caused by lattice mismatch, while being beneficial at the device level, is unable to recover the circuit-level performance of the ideal case.**

Keywords: Tunnel Field-Effect Transistors, III-V materials, strain, interface traps, quantum transport, TFET inverter

I. INTRODUCTION

In the last decade TFET has been widely investigated as one of the most promising devices for low-power applications [1]. TFET-based technology has to face some challenges, especially regarding relatively low ON-state currents, ambipolar effects, and superlinear onset and high saturation voltage of the output characteristics [2,3]. Furthermore, it has been shown that interface traps pose a significant threat to the performances of these kind of devices [4]–[6]. Interface traps are thus a key factor that must be taken into account for a realistic investigation of the TFET circuits performance.

In [7] it has been demonstrated that a localized strain at the source/channel junction, arising from lattice mismatch in heterojunction devices, is able to mitigate the effect of traps. Specifically, for n-type InAs/AlGaSb TFETs, the on-state current degradation can be fully recovered, with an improvement of subthreshold swing. For p-type TFETS, instead, a current degradation with respect to the ideal device is observed. For digital applications, subthreshold slope and on-state current are not the only relevant parameters that must be considered. Voltage transfer characteristics (VTC), voltage gain and switching current, as well as rise and fall times, significantly contribute to the circuit-level performance.

In this paper we extend the full-band quantum simulation of a TFET inverter based on the technology platform presented in [7], to include the effect of interface traps and strain.

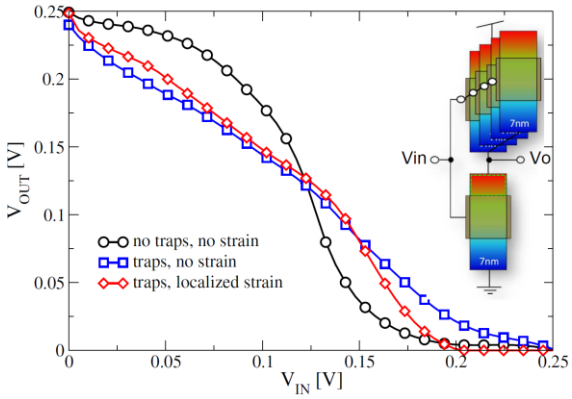

Figure 1. Inverter VTC. Black dots: unstrained without traps; blue squares: unstrained with interface traps; red diamonds: with localized strain and interface traps. All curves are calculated by exploiting nonlinear interpolation between $I_D - V_{DS}$ families.

More specifically, the combined effect of traps and localized strain at the source/channel junction is here investigated.

II. SIMULATION DETAILS

The investigation is carried out on a TFET inverter realized with the $Al_{0.05}Ga_{0.95}Sb$/InAs technology platform examined in [7]. All calculations are performed at V_{DD} = 0.25V, at which the TFET-based inverter has shown to outperform the FinFET-based CMOS one for equal levels of static power dissipation. Numerical simulations are based on a four-band k*p Hamiltonian for the device, coupled with non-equilibrium Green's function (NEGF) formalism for transport. The trap model has been described in detail in [7], and represents an extension of the standard Shockley-Read-Hall theory consistent with the ballistic NEGF approach and carrier degeneracy. Only the electrostatic effect of traps is considered via Poisson's equation, while transport remains fully ballistic. The trap energy distribution is taken from experimental data presented in [8]. Finally, in the absence of experimental and simulation data on strain maps in AlGaSb/InAs nanowire TFETs, we took advantage of process simulation data carried out in [9]. The details of the physical model and device structures can be found in [7].

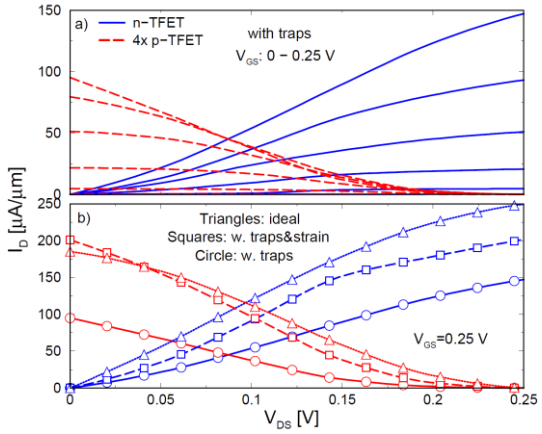

Figure 2. Top: $I_D - V_{DS}$ curves for the PDN and PUN in the presence of interface traps. Additional curves are obtained via nonlinear interpolation, using the same procedure described in [10]. Bottom: $I_D - V_{DS}$ @ V_{GS} = 0.25V in the ideal case (tringles), with traps (circles), and with traps and localized strain (squares).

III. RESULTS

Figure 1 shows the VTC for the ideal inverter (black circles) and the corresponding VTC where interface traps are accounted for (blue squares). The inverter design, as well as the procedure for the calculation of the I_D–V_{DS} families for pull-up and pulldown networks (PUN and PDN, respectively), are the same used in [10]: four p-type TFETs are in the PUN, in order to compensate the lower on-state current delivered by p-TFETs, with respect to n-TFETs (see Fig. 2). I_{OFF} is fixed for both devices to 100 nA/μm. In the presence of interface traps, the VTC is dramatically degraded. This degradation severely lowers noise-immunity margins, strongly affects voltage gain, and alters the switching current behavior. The voltage gain at the inverter logic threshold is ~ 4.5 for the ideal case, but it drops down to ~ 1.75 in the presence of traps (not shown).

The transient performance is estimated by computing the rise and fall times $t_{r,f}$ required for a transition from 10% to 90% of the supply voltage, and back, in response to an instantaneous voltage step. t_r and t_f are computed by integrating the output current of the switching device at V_{GS} = 0 V or $|V_{GS}| = V_{DD}$ (Fig. 2 bottom), with a fixed load capacitance C_L. While rise and fall times are fairly balanced for the ideal inverter (25 ps vs. 10 ps for t_r and t_f, respectively), t_f is greater than its ideal counterpart by a factor of ~ 2,3, if interface traps are taken into account (23 ps). The difference is even larger for t_r, with a factor of ~ 12 (300 ps). The reason for this degradation is twofold. First, the I_D–V_{DS} curves at V_{DS} = 0.25V with interface traps are not completely saturated (see Fig. 2 top). Moreover, the "S" shape of the output curves, responsible of the small drain conductance at low V_{DS}, is enhanced by the trapped charge (see Fig. 2 bottom).

Lattice mismatch at the source/channel heterojunction causes a significant strain across the S/CH junction (~ 3%). Surprisingly, this unavoidable effect can be quite beneficial in some cases, with an overall increase of I_{ON}, together with a reduction of SS [7].

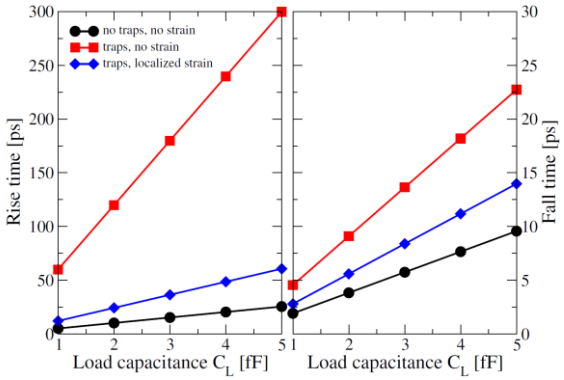

Figure 3. Computed rise and fall times in constant-loading case, for ideal tunnel-FETs (black circles), with interface traps included (red squares) and with localized strain at the source/channel junction (blue diamonds).

From our investigation it appears to improve the circuit-level performance as well. Localized strain also improves the transient performance as shown in Fig. 3 (blue diamonds). Thanks to the n-TFET enhancement t_f is almost equal to that of the ideal case, whereas t_r is still 2× higher (53 ps).

IV. CONCLUSIONS

The circuit-level performance of a TFET-based inverter, realised with co-optimized p- and n-type TFETs on the same InAs/AlGaSb technology platform, has been investigated via 3D full-quantum ballistic simulations in the presence of interface traps and localized strain. Realistic trap energy distribution and strain conditions have been taken from literature. It turns out that interface traps induce a significant degradation of the voltage gain, noise margin and transient performance. Unfortunately, the effect of localized strain at the source/channel heterojunction, caused by lattice mismatch, while being beneficial at the device level, is unable to recover the circuit-level performance of the ideal case.

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Near field scanning microwave microscope based on a coaxial cavity resonator for the characterization of semiconductor structures

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***Abstract*— In this work, we have designed and fabricated a near-field scanning microwave microscope based on a coaxial cavity resonator. The coaxial cavity resonator is fed by a Keysight N5242A PNA-X Network Analyzer. The inner conductor of the coaxial resonator is connected to a sharpened tungsten tip home-made in our Lab following an electrochemical process. The transmission coefficient S_{21}, the resonance frequency f_r and the quality factor Q are measured as the sharp tip is scanned over the device under test at a fixed sample-tip distance in the near field region. The variations of these parameters are related to the topographical and dielectric properties of a very small region of the material under the tip.**

Keywords- Near-Field Scanning Microwave Microscopy (NSMM), coaxial cavity resonator, non-destructive semiconductor characterization.

I. INTRODUCTION

Near Field Scanning microwave microscopy (NSMM) is a technique used for the characterization of materials at microwave frequencies. A NSMM system consists of a sharpened metal tip, mounted at the edge of the center conductor of a high quality coaxial resonator connected to a Vector Network Analyzer (VNA). The VNA, which feeds the resonator, continuously measures the transmission, S_{21} and reflection, S_{11} coefficients of the cavity. When the tungsten tip is placed close enough (in the near field region) above the device under study (DUT) a shift in the resonant frequency f_r and the quality factor Q of the cavity is produced. This shift of the resonant frequency depends on the distance between the tip and the sample and the electromagnetic properties of the sample under test, such as the conductivity, sheet resistance, or dielectric constant [1]–[3]. If the distance between the tip and the surface of the sample is kept constant, the shift in f_r only depends on the electromagnetic properties of a very small area of the DUT near the tip. The sample is then scanned by the tip of the cavity while the distance between tip-sample is kept constant and the resonant frequency of the cavity is continuously measured by the VNA. The 2D representation of the resonant frequency, quality factor, and magnitude of the transmission coefficient of the cavity provides a map of the electromagnetic properties of the sample at the nanoscale. Therefore this technique could be used to non-destructively characterize materials especially semiconductor structures at microwave frequencies [4], [5] and with nanoscale resolution without damaging it. Figure 1 shows an scheme of a near field scanning microwave microscope (NSMM) structure, which is composed by a network analyzer (PNA) that continuously feeds a coaxial cavity resonator with a conductive tip connected at the end of its inner conductor.

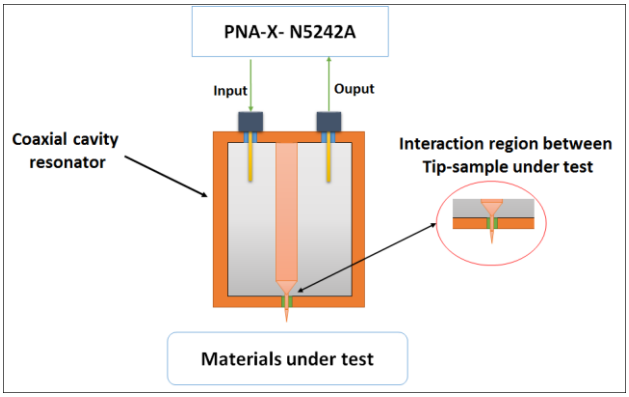

Fig. 1. Near field microwave microscopy structure [4], [6].

This type of resonator makes possible to obtain very high-quality factor and its potential to characterize metallic materials has been well demonstrated by several groups of research [6], [7]. In this work, the design and set up of a coaxial cavity resonator NSMM platform has been carried out. The transmission coefficient of the resonant cavity S_{21} is continuously measured and monitored by a vector network analyzer, while a sharpened tungsten tip placed at the edge of the central conductor of the coaxial cavity is scanned over the device under test at a very short distance (near field regime). We show that the spatial variations of the resonant frequency f_r, or the maximum of S_{21} are then related to the spatial variations of the electromagnetic properties, and therefore of the composition, of the studied sample in an area whose size is of the order of magnitude of the tip thickness. This technique could then be used to non-

destructively characterize semiconductor structures with micrometric or even nanometric spatial resolution [8].

II. RESULTS

The device under test in this work consists in a silicon sample covered with 300nm of SiO_2. Different patterns of gold and aluminum with different sizes and shapes are deposited on top of the oxide by thermal evaporation. The thickness of the gold metallization is around 30-50nm. These structures are used to calibrate the system. Once the DUT is placed in the sample holder the tip is approached to the sample until the distance sample-tip is around 2µm. Then the sample is slowly approached to the tip and the transmission coefficient is recorded as a function of the Z position. Figure 2 shows the evolution of f_r as the sample is approaching the tip. Two cases are considered: the tip is approaching a gold pattern (solid line) and when the tip is moving towards the SiO_2 surface (dashed line). In the first part of the curve (right side of the figure) f_r is almost constant and very similar for both SiO_2 and gold samples (Far field regime). However, as the tip is approaching the surface of the sample, f_r decreases sharply although faster in the case of gold, and reaching lower values, thus demonstrating that the behavior of the cavity depends on the material over the one the cavity is scanned. In the approaching procedure, the Z stepper motor is stopped before the physical contact between the tip and the sample is produced, what could damage the tip and/or the sample.

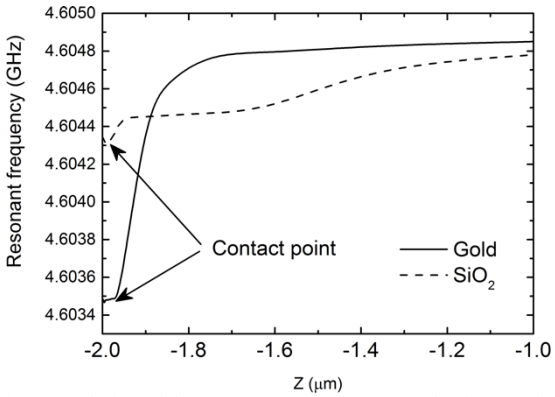

Fig. 2. Evolution of the resonant frequency versus the distance tip-sample, Z

III. CONCLUSION

A Near-Field Scanning Microwave Microscope (NSMM) has been designed, simulated and fabricated, using a coaxial cavity resonator. A very sharp tungsten tip, electrochemically sharpened, is attached at the edge of the inner conductor of the coaxial resonator and through the wall of the lower face of the cavity. The resonator is feed with a Vector Network Analyzer, and the transmission coefficient S_{21} is continuously measured, while the tip is approached to the surface of the material under study. We have demonstrated that when the tip is placed is in the near field region, the resonant frequency of the cavity depends on the electromagnetic properties of a small region of the material under it, whose dimensions are similar to the size of the tip.

ACKNOWLEDGMENT

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Energy Harvesting Power Management Circuit Design in 22nm FDSOI Technology

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***Abstract*—Today, users of existing commercial products expect longer battery hours from the electronic products that they use in their daily activities. In addition to this, emerging technologies, especially in the Internet-of-Things domain require very long battery life time to be regarded as useful by their potential users. Energy harvesting methods which are used for extending the battery life or battery-free operation have been long studied by researchers. With the utilization of FD-SOI technology which can significantly reduce the leakage current in the stand-by mode of the electronic devices, more efficient energy harvesting power management integrated circuits can be designed. In this work, we present the design of an energy harvesting circuit which is optimized to benefit from the low leakage current characteristics of FD-SOI transistor.**

Keywords- FD-SOI, energy harvesting, energy scavenging, 22nm, CMOS design

I. INTRODUCTION

According to a recent market report [1], the number of connected Internet-of-Things objects will reach 20.8 billion by 2020. Types of these connected objects cover sensor nodes, smart home units, wearables, electronic civil infrastructure components and many other devices. Some of these devices are supplied by a power line and power management can be regarded as a minor issue for them. On the other hand, a large set of applications requires batteries as their electrical energy source. Effective usage of the battery is one of the major factors which determine the performance level of IOT applications.

Objective of this work is to design an efficient energy harvesting circuit which charges a large external storage capacitor to support the main battery of the application circuit. By implementing a generic PMIC solution which can be used for both AC energy sources, such as piezoelectric generators and DC energy sources like thermo-electric generators. We also aim this circuit to be efficient in terms of power and physical space.

The application circuit in which the designed circuit will be utilized is shown in Fig. 1. Since the circuit will accommodate a battery, in some situations where the harvested energy is not enough, the battery can be used for the operation of the application circuit.

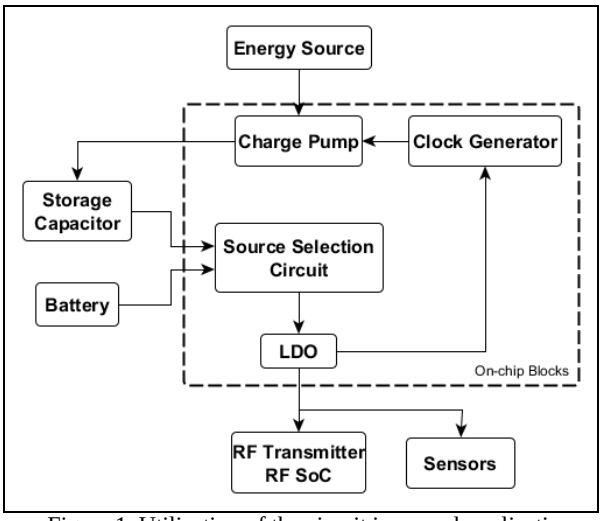

Figure 1. Utilization of the circuit in an end-application.

II. CHARACTERISTICS OF THE ENERGY SOURCE

In Fig.1 blue colored blocks represent the parts of the PMIC, where the other blocks are the parts of the application PCB. As it can be seen from the Figure 1, designed power management circuit includes a charge-pump stage to increase the voltage supplied by the energy source to a higher value, so the charge on the capacitor can be sufficient for periodic sensor read-out and RF transmissions.

The conversion ratio of the charge pump is determined according to the open circuit output voltages of the thermoelectric generators (TEGs) found in literature [2][3]. The voltage output generated by a thermocouple is calculated by the following formula [2]:

$$V=(S_p-S_n)\Delta T/2 \quad (1)$$

Where S_p and S_n are Seebeck coefficients of p- and n-type legs and ΔT is the temperature difference between the hot and cold thermocouples junctions. For 1°C of temperature difference and ±0.2mV/°C Seebeck coefficient which implies the utilization of bismuth telluride thermocouples, one can calculate that the output voltage per thermocouple will be 0.2mV. Therefore, there will be a need of 5000 thermocouples in the

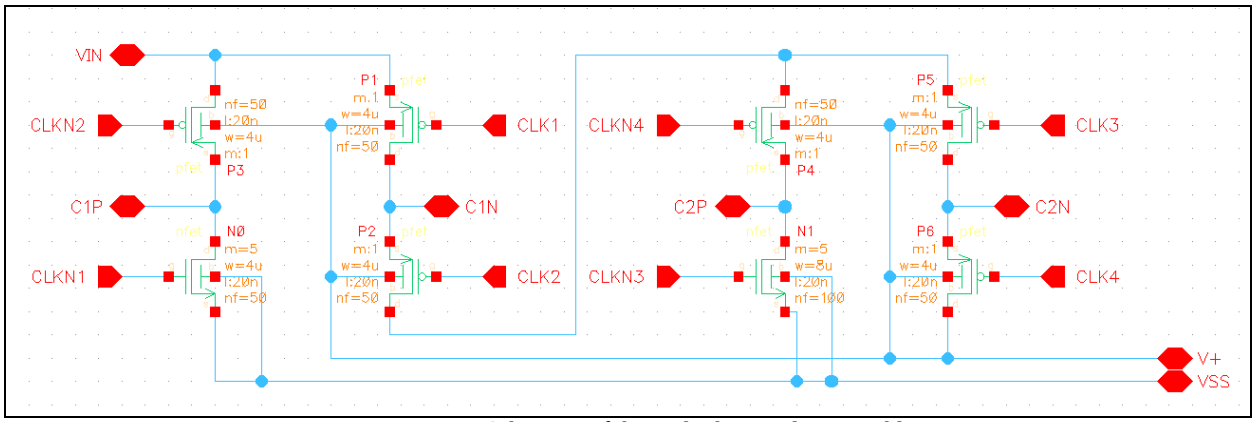

Figure 2. Schematic of the Multiphase Voltage Doubler.

TEG for a 1V output. It can be inferred from [2] that 0.25V output voltage can be obtained by a thermopile with 2.5cm x 2.5cm size. This size can be suitable for most of the wearable systems.

Output voltage of 0.25V should be converted to a more meaningful level before storing into the storage capacitor. By converting to a higher level, the energy stored in the capacitor will be sufficient for the applications at the expense of longer charging time.

III. Charge Pump Design

Multiphase voltage doubler (MPVD) [4] is selected to convert the input voltage to a higher level because of its transistor number advantage when compared to other charge pump designs. Two-stage MPVD charge pump conversion ratio is determined by the number of stages. Intermediate capacitors on the charge pump are kept internal. Therefore, a more compact solution can be obtained with many recurring stages. The schematic of the MPVD is shown in Figure 2.

Two-stage MPVD type charge pump requires four non-overlapping clock signals. Non-overlapping clock generator can generate 4 pairs of non-overlapping clock signals using one clock input. As the required single clock source an astable multivibrator circuit is used. Frequency of astable multivibrator is determined by RC constant formed by the resistor and the capacitor on the feedback loop. The capacitor and the resistor of the astable multivibrator are kept off-chip for flexible operation.

A two-stage op-amp is used in astable multivibrator for simplicity. Op-amp is used in a single supply scheme. Source selection part is used for selecting between battery and capacitor, depending on the charge status of the storage capacitor. If storage capacitor is at a level which can be used by the RF transceiver and sensor circuitry, source selector circuit connects capacitor to the loads. This part is implemented using a DPST switch using FD-SOI transistors.

The design has been implemented using GLOBALFOUNDRIES 22FDX process. RVT type transistors have been used for the clock generator and the charging circuit. Figure 3 depicts the simulation result of charging voltage of a 3.3µF storage capacitor.

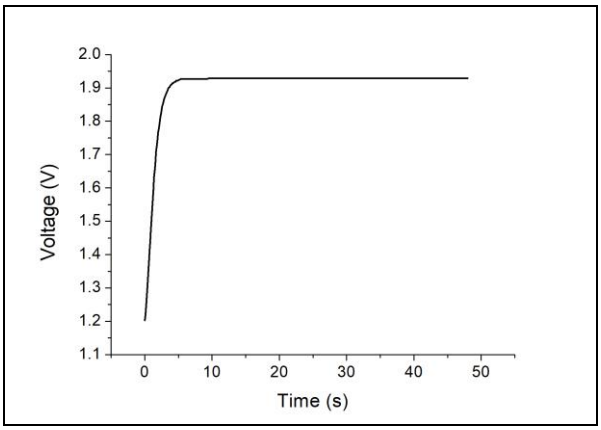

Figure 3. Charger Output.

IV. Conclusion

FD-SOI technology lets designers to optimize their design by selecting a back-biasing scheme. Using back-biasing, the designer can choose between higher clock frequency and lower leakage current. Energy harvesting applications are typically doesn't require high frequency clocks. However, this type of applications may benefit from low leakage current which can be obtained by increasing the threshold voltage level.

As it can be seen from Figure 3, the designed circuit is able to charge the storage capacitor to a level that can be used for supplying an RF transceiver with a supply voltage of 1.8V. Using the circuit in conjunction with main battery, lifetime of an IOT node can be extended.

Ferroelectric FET as a Low Power Device with reduced SCE and RDF Effect

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***Abstract*— It is known that for a classical Field-Effect Transistor (FET), the Subthreshold Swing (SS) cannot be reduced below the Boltzmann limit of 60mV/dec. Recently, it has been proposed that by instilling a ferroelectric material in the gate stack the SS can be reduced below 60mV/dec limit, which also defines the minimum limit of power dissipation. Simulations were carried out using Sentaurus TCAD for the Ferroelectric FET having Si doped HfO_2 as a ferroelectric material and SiO_2 as a linear dielectric in the gate stack and results show that SS is brought down below 60mV/dec, with high I_{ON}/I_{OFF} ratio and low threshold voltage. Short Channel Effect (SCE) and Random Dopant Fluctuation (RDF) is also investigated for various channel length and channel doping concentration.**

Keywords- ***Negative capacitance, Subthreshold swing (SS), Short Channel Effect (SCE), Surface potential and Ferroelectric.***

I. INTRODUCTION

The scaling in microelectronics has been impelled by the quest for higher density integration, since the switching energy and the switching delay of MOSFET is directly proportional to channel length, the aim of having faster and more energy efficient devices also leads to aggressive scaling. With miniaturization of MOSFET, the device geometry such as channel length, junction depth and oxide thickness have been reduced but for maintaining a low power density, the applied voltage V_{DD} should also be scaled down. As, the V_{DD} decreases the gate overdrive voltage also decreases which negatively affects device performance by decreasing I_{ON} (On-current),I_{ON}/I_{OFF} ratio and dynamic speed. To meet the I_{ON} requirement V_{th} (Threshold Voltage) should be brought down, but with threshold voltage reduction the I_{OFF} (Off-current) increases exponentially. So, to meet a sufficiently high I_{ON} with respect to I_{OFF}, Subthreshold Swing (SS) should be small. However, for conventional MOSFET the SS cannot be less than 60mV/dec because of Boltzmann tyranny. In order to evade this limitation, a number of devices have been proposed such as Impact Ionization MOSFET[1], Feedback-FET[2], Suspended Gate MOSFET [3], Tunneling FET [4], Fe-FET [5,6]. Salahuddin et al. [7] theoretically demonstrated that by embracing a ferroelectric material in the top of silicon dioxide in Metal–Oxide–Semiconductor structure, the surface potential can be highly boosted leading to a steep transition. Ferroelectric materials during polarization switching show the transient phenomenon of negative capacitance. By the virtue of this property, ferroelectric materials can act as an inner voltage amplifier to enhance the surface potential and thus opening a new way for the apprehension of transistors with steeper subthreshold characteristics (SS < 60 mV/decade) without changing the essential physics of the FET.

II. THEORY

At a given V_{DD}, in order to achieve energy efficient switches I_{ON}/I_{OFF} ratio has to be as high as possible and to increase the ratio, the subthreshold swing needs to be small. The Subthreshold swing (SS) is defined as-

$$SS = \frac{\partial V_g}{\partial (log I_d)} = 2.3 \frac{K_B T}{q} \left(1 + \frac{C_s}{C_{ox}}\right) \quad (1)$$

Where K_B is the Boltzmann constant, T is the absolute temperature and q is the unit charge. C_s and C_{ox} denotes the depletion capacitance and oxide capacitance respectively. The first term $2.3 \frac{K_B T}{q}$ denotes that the transport in subthreshold region is dominated by diffusion transport of excess minority carriers and is defined by the Boltzmann statistics of electrons/holes, which limits the SS to 60mV/dec.

Recently, it has been found that the ferroelectric thin films show the phenomenon of negative capacitance due to the negative slope of polarization-electric field (P-E) curve. Thus, if ferroelectric material is used as a gate insulator, the factor $\left(1 + \frac{C_s}{C_{ox}}\right)$ can be made less than one and thus the Subthreshold Swing (SS) can be further brought down below 60mv/dec.

III. PROPOSED DESIGN

In this paper, an n-type Silicon On Insulator (SOI) ferroelectric FET is proposed. The device is shown

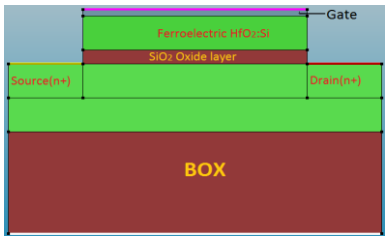

Figure 1.The Proposed structure of Ferroelectric FET

schematically in Fig.1. The length of the channel varies from 40nm to 60 nm. The doping concentration of the channel is varied from 8 x 10^{17} to 4 x 10^{18} , the highly doped n^+ source concentration is 10^{20} cm^{-3} and n^+ drain concentration is 10^{19} cm^{-3}. In the gate stack SiO_2 is used as an oxide layer and silicon-doped HfO_2 is utilized as ferroelectric layer due to its unique property of exhibiting the ferroelectricity even in a 5 nm thin film [8, 9]. Thickness of oxide layer is varied from 0.8nm to 2nm and thickness of ferroelectric layer is varied from 5nm to 15nm.

IV. RESULTS

Simulation of the proposed device was done using Sentaurus TCAD. The results shows that Threshold Voltage is reduced to very low values in Fe-FET and it also demonstrates the dependence of $V_{th,}$ on gate voltage $V_{g,}$ oxide layer thickness and ferroelectric layer thickness. Also, by the virtue of negative capacitance, surface potential is highly boosted which lead to a higher On-current (I_{ON}) and thereby better I_{ON} /I_{OFF} ratio and SS below 60mV/dec. It also reveals that Fe-FET greatly suppresses the effect of RDF. Further, the Drain Induced Barrier Lowering (DIBL) effect is also measured and is found to be smaller in Fe-FET as compared to any state of art design and also MOSFET. The outcome of the simulation are shown in Fig. 2-Fig.5.

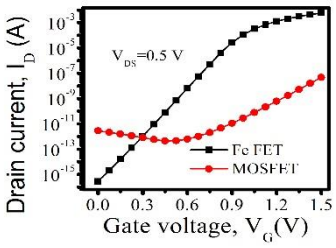

Figure 2. Log I_d/V_g curve for FeFET and MOSFET

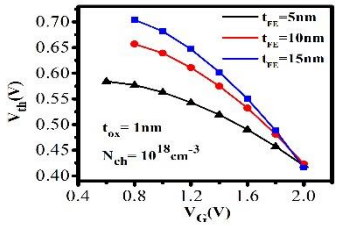

Figure 3.V_{th}/V_g curve for different t_{FE}

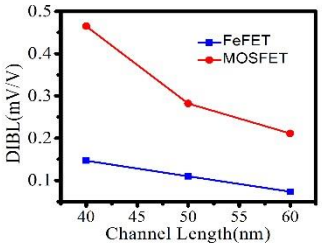

Figure 4. DIBL effect on varying channel lengths

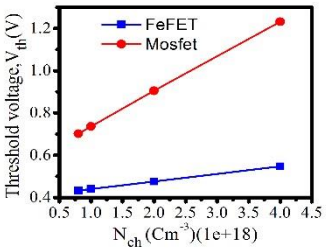

Figure 5. Dependence of V_{th} on different channel doping concentration.

V. CONCLUSION

A comparative examination of MOSFET and Fe-FET has been done using Sentaurus TCAD simulation tool. It is found that with thicker ferroelectric layer and thinner oxide layer, Fe-FET shows steeper and better sub-threshold transition, having a higher I_{ON}/I_{OFF} ratio of 10^{15} and SS of 52mV/dec. It also revealed that the RDF effect is greatly reduced in Fe-FET and SCE like DIBL is also smaller compared to MOSFET.

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Indium oxide nanostructures for RRAM integration in CMOS-BEOL

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***Abstract* — this work report on the integration of indium oxide (In_2O_3) nanoparticles (NPs) for Resistive Random Access Memory (RRAM) applications. The RRAM integration based on MOCVD and ALD depositions is fully compatible fabrication process with CMOS of back-end-off-line. The objective is to evaluate the effect of In_2O_3 nanoparticles on the RRAM memory device performances. A bipolar switching behavior with very good HRS/LRS ratio between 10^7 and 10^4 obtained from 25°C to 100°C. Cycling measurements confirm a good control of device parameters with increasing temperatures up to 100°C. 64 SET/RESET cycles have been obtained at 100°C with a HRS/LRS ratio of 10^4. The results provide insights for further integration of In_2O_3 nanoparticles-based NVM applications.**

Keywords: RRAM; NVM; nanoparticles; indium oxide.

I. INTRODUCTION

Among emerging memory device technologies, Resistive Random Access Memory (RRAM) appears as a suitable candidate for the next generations of non-volatile memories (NVM) based on two terminal devices [1]-[4].

To improve the switching stability, several methods have been proposed such as inserting NPs in the insulating layer and design RRAM devices [5]-[10].

In this work, we show In_2O_3 nanoparticle (NPs)-based RRAM devices for CMOS back-end-off-line integration. The work function of In_2O_3 is about 5 eV [11] and could be increased using appropriate surface treatments [12]. A simulation work shows that the work function could be larger than 6 eV depending on surface oxidation process [13]. In2O3 is thus expected to act as a quite efficient electron trap with SiO2 barriers since it could offer potential barriers larger than 5 eV. The charge trapping in NCs allows a good control of the electric field. A recent work on nickel nanostructure-based OxRAMs shows a large reduction of SET/RESET voltage dispersion [14]. The electric field focused in NCs gives indeed a better control of the forming process.

The proposed NP-RRAM stack Au/Cr/Al_2O_3/In_2O_3-NPs/SiO_2/Si-n+ is illustrated in Fig.1.

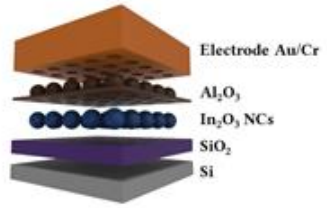

Figure 1. Schematic structure of the fabricated devices

II. DEVICE FABRICATION

The above-mentioned-two-terminal-device architecture was fabricated using n+-type silicon substrates (001). The first step is a thermal oxidation of the substrate, leading to the formation of a 2-nm-thick tunnel oxide. Indium nano-dots are thus deposited at low-temperature (< 450 °C) by metal-organic-chemical-vapor-deposition using a 300 mm-MOCVD reactor from Applied Materials. The system is cooled down to room temperature and exposed to ambient atmosphere, leading to the formation of In_2O_3 NPs on the SiO_2 surface. Atomic force microscopy (AFM) measurements have been performed to determine an average NP diameter Φ_{moy} =12 nm. The estimated density NPs is $3x10^8$ NPs/cm^2. Subsequently, a Al_2O_3 control oxide is deposited by atomic layer deposition (ALD) at 200 °C with an Ultratech/CNT Fiji series reactor, using trimethylaluminum and H_2O reactors in thermal mode. 25 cycles of ALD-process give a 2 nm-thick Al_2O_3 layer. NPs are in a crystalline phase as shown in Fig.2.

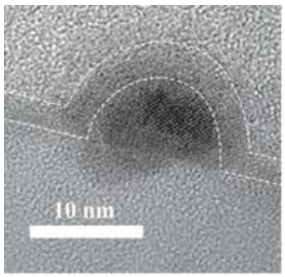

Figure 2. HR-TEM image of In_2O_3 NPs on a 100 nm-thick SiO_2 layer

For electrical characterizations, 200 nm-thick gold circular top electrodes were deposited with an Edwards thermal evaporator using a shadow mask. The electrodes nominal-diameters were comprised between 100 µm and 30 µm. Finally, a rapid thermal annealing stage (RTA, ADDAX) of 10 minutes at 400 °C, under N_2 atmosphere, was used to passivate the electrical contacts.

III. ELECTRICAL CHARACTERIZATION

Current-voltage measurements were recorded using a Keithley 4200 semi-conductor parameter analyzer from 25°C to 100°C. Measurements were done with a power-gradual increase frame, i.e. for an applied bias sweep range and a fixed current compliance (I_c), if no resistive switch-behavior appeared, then the amplitude of the applied bias was first increased. Bipolar switching behavior was observed for all the devices without initial forming. Fig.3 (a) illustrates the I-V characteristics for a 100 µm-diameter device. Devices with a 100 µm diameter with I_{ON}/I_{OFF} ratio around 10^4 for V_{read} = 0.5 V. A large variability of V_{RESET} is however observed.

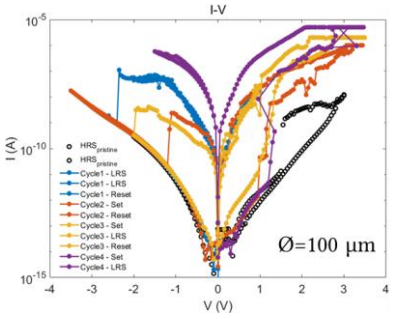

Figure 3. I-V characteristics at 25°C of a 100 µm-device (4 cycles)

I-V measurements have been performed at 25°C, 75°C and 100°C. The cumulative distribution as function of the temperature of LRS and HRS is illustrated in Fig. 4. The HRS/LRS ratio varies from 10^7 to 10^4 from 25°C to 100°C.

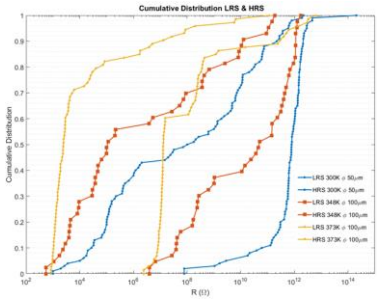

Figure 4. Cumulative distribution of LRS and HRS at 25°C, 75°C and 100°C.

Cycling measurements have been also performed at 25°C, 75°C and 100°C. Fig. 5 shows a first interesting result with 64 cycles at 100°C. This demonstrates a good thermal behavior of RRAM devices. We have noticed one HRS level but two LRS levels in our samples.

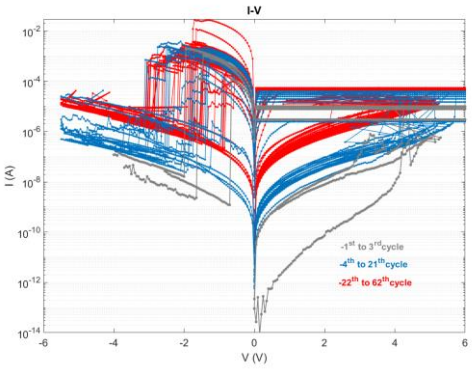

Figure 5. Cycling measurements at 100°C of a 100 µm-device.

IV. CONCLUSIONS

In_2O_3 nanoparticles were integrated in functional two-terminal devices that exhibited memory properties suitable for non-volatile applications. The fabrication process was fully-compatible with CMOS back-end-off-line integration, with low temperature processes, and with industrial process manufacturing.

The study confirmed the results of first demonstrators over a temperature range from ambient to 100 ° C. The bipolar behavior of the realized OxRAM is confirmed up to 100 ° C with HRS / LRS ratios up to 10^4 even at high temperature.

A more in-depth statistical analysis should allow a better understanding of the switch mechanisms. For this new study, we optimized the technique of nanostructure deposition in order to obtain samples with good uniformity over 300 mm, a small size dispersion and a higher density (2.10^{10} cm $^{-1}$).

ACKNOWLEDGMENT

This work has been partially funded by the "Nano 2017" program; by the French government program "Investissements d'avenir" managed by the National Research Agency (ANR) under the contract number ANR-10-EQPX-33; by the French "Recherches Technologiques de Base" (Basis Technological Research) and RENATECH programs. The authors also would like to thank the Nanolyon Technological Platform and the CLYM for their support and David Albertini for the AFM characterizations. Nicholas Blanchard from Institut Lumière Matière-UMR CNRS 5306 is acknowledged for TEM characterizations.

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Investigation of Memory Effect with Voltage or Current Charging Pulse Bias in MIS Structures based on codoped Si-NCs

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***Abstract* – Co-doped Si-NCs have been introduced into MIS structures with HfO_x gate dielectric layers. The fabricated MIS structures were characterized by means of stress-and-sense measurements in terms of device capacitance, flat-band voltage shift, and retention time. Presented results are promising for applications of Si-NCs in memory structures.**

Keywords – silicon nanocrystal; memory; metal-insulator semiconductor structure; electrical characterization; high-k dielectric

I. Introduction

Silicon nanocrystals (Si-NCs) are commonly investigated for future applications in modern optoelectronics and photonics [1]. The most frequently utilized method for Si-NCs formation is Plasma-Enhanced Chemical Vapor Deposition (PECVD) of amorphous silicon (a-Si) with following high-temperature recrystallization/annealing processes [2]. However, Si-NCs can be also obtained by a physical method based on a co-sputtering process of Si, silicon dioxide (SiO_2), boron trioxide (B_2O_3) and phosphorus pentoxide (P_2O_5) followed by etching in a hydrofluoric (HF) acid solution (46 wt%), yielding free-standing hydrogen (H)-terminated nanocrystals [3]. In this work, we investigate the memory effects in Metal-Insulator-Semiconductor (MIS) structures based on colloidal co-doped Si-NCs embedded in the gate insulator layer. The test structures were analyzed by means of stress-and-sense measurements with different type of stress (voltage, current) and measured response (capacitance, voltage). The effect of stress parameters (voltage, current, time) on memory effect is presented.

II. Electrical Measurements

The measurement procedure used to investigate the fabricated devices consists of charging pulses and measurements performed in a staggered manner (Fig. 1a). At the very beginning the fresh device is measured. Then charging bias pulses (electrical stress) followed by measurements (capacitance or current) are applied. The charging bias pulse may be implied by a voltage (Fig. 1b) or a current source (Fig. 1c). In the program-erase voltage analysis (Fig. 1d) voltage pulses of opposite values are subsequently applied. The measurement may be taken in a sweep (Fig. 2a) or sampling mode (Fig. 2b). In the sweep mode a single or a dual sweep may be performed. The dual sweep is depicted as (1) followed by (2) in Fig. 2a. In the sampling mode one or more probes may be taken.

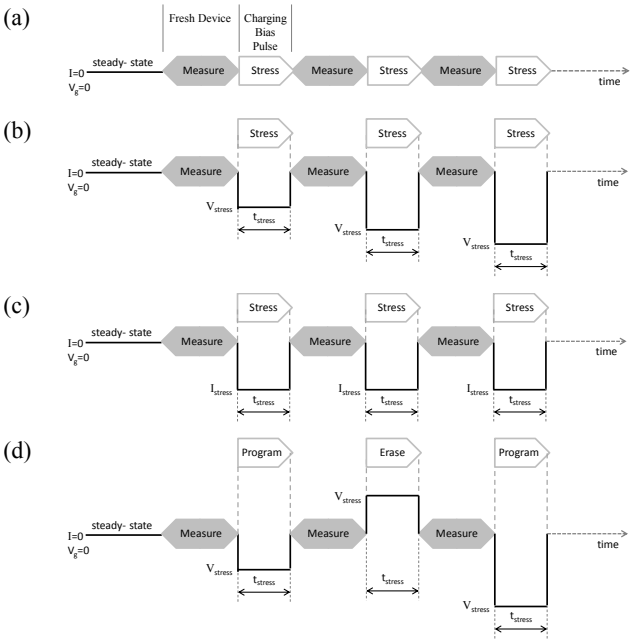

Figure 1. The measurement procedure: general scheme (a), voltage excitation (b), current excitation (c), program-erase voltage ($V_{p/e}$) analysis (d).

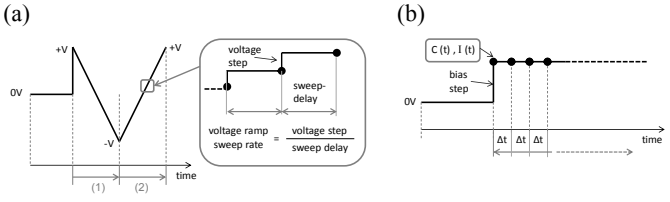

Figure 2. Measurements: sweep (a) and sampling (b) mode.

III. FABRICATION OF SAMPLE DEVICES

In this study silicon (Si) substrates with the resistivity of 1÷10 Ωcm were used. The processing sequence of Si-NCs MIS structures was as follows: Si substrates were cleaned by means of modified RCA method (Piranha + SC1 + SC2 + HF dipping). In the first step, 3 nm thick silicon dioxide (SiO_2) layer was grown. In the next step the bottom 3 nm hafnium oxide film was deposited, followed by the Si-NCs spinning off on top of the hafnia surface. Then, 10 nm top HfO_x thin layer was deposited. After the formation of Si-NCs embedded in dielectric layer ensembles the aluminum contact pads were formed by means of the standard UV photolithography process and wet etching. Hafnium oxide and aluminum layers were deposited in RF reactive magnetron sputtering process. In the last step, the post-metallization annealing at 300°C in vacuum atmosphere was performed. For the sake of comparison reference MIS structures (without the Si-NCs introduction) were also fabricated.

IV. RESULTS

The sample structures were stressed with current bias pulses and the shortcut current characteristics were measured according to the procedure depicted in Fig. 1c. The clear difference between the characteristics of reference structures (i.e., without nanocrystals embedded in the gate stack) and NC-MIS structures proves that the memory effect is caused by nanocrystals (Fig. 3).

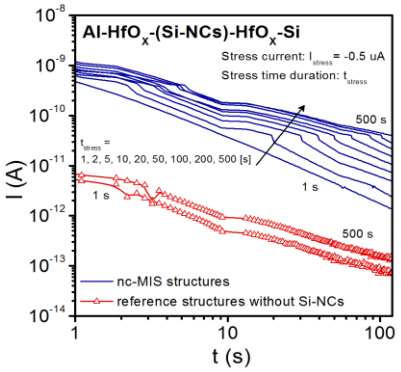

Figure 3. Comparison of the shortcut current characteristics with stress time duration as a parameter.

Fig. 4 presents the the measurements of capacitance of the MIS stack that were taken at the flat-band voltage value (V_{fb}) of fresh device according to procedure depicted in Fig. 1c. The charging effect due to the nanocrystals presence is visible, but the magnitude is lower compared to reference structure. Moreover, the longer stress current pulse, the smaller difference of capacitance value near the V_{fb}.

A clearly less wide memory window has been obtained for MIS structures with Si-NCs (i.e., ~2 V), however, the V_{fb} value after consecutive voltage stress seems to be more stable in the examined range of $V_{p/e}$ as it is presented in Fig. 5.

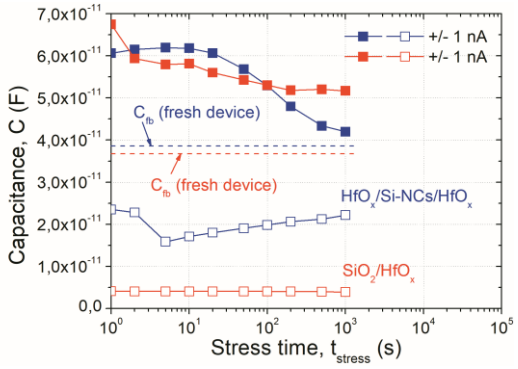

Figure 4. Comparison of capacitance values near the flat-band V_{fb} of MIS structures after consecutive stress-and-sense measurements with current stress pulses and different stress-time.

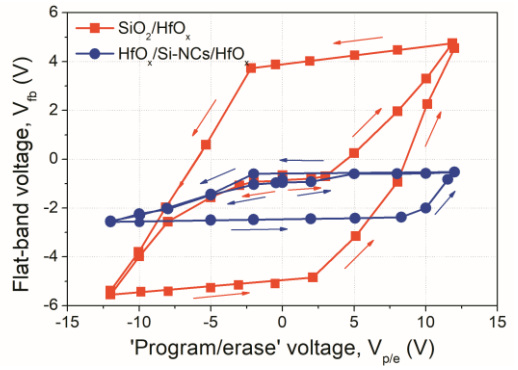

Figure 5. Memory windows of investigated in this work MIS structures expressed as flat-band voltage vs. program/erase voltage.

V. CONCLUSIONS

In this work, the electrical characteristics of MIS structures based on co-doped Si-NCs, are analyzed and discussed in terms of possible applications of colloidal nanocrystals in memory structures.

ACKNOWLEDGMENT

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Reliability of Z^2-FET

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***Abstract*—Reliability of Z^2-FET has been investigated with various gated channel length, back gate voltage and temperature. Current margin of 50nm gated length is larger than that of 200nm gated length. Even at -0.1V of back gate the current margin maintains the same trend. However, memory window and current level are seriously degraded at 125C°.**

Keywords-component; Z^2-FET; L_G scaling; Back gate bias; high temperature; potential barrier

I. Introduction

Zero impact ionization zero subthreshold swing field effect transistor (Z^2-FET) has been suggested as a 1T DRAM cell device since it shows interesting performance: very low subthreshold swing, high on/off current ratio, low power consumption and fast access speed [1,2]. However, reliability of Z^2-FET is still not explored in detail [3-5]. In this work, we have studied the current margin (I_1-I_0) between '0' and '1' state with gate length and at low back gate voltages (V_{Gb}). The relations between AC/DC electrical characteristics and operating temperature have been also thoroughly investigated since temperature reliability causes variation of threshold voltage, reduction of mobility, high leakage current, and eventually relates with failure of memory array performance.

II. Experiment

Electrical characteristics of the Z^2-FET have been studied under the various anode voltages (V_A), back gate voltages (V_{Gb}) and temperatures. Z^2-FET device has a p+ type anode with an n+ type cathode and an intrinsic channel. The channel is partially covered by a gate electrode (L_G) on the anode side and a back gate electrode under the buried oxide layer (BOX). L_G is varied from 200nm to 50nm, the ungated channel (L_{IN}) is fixed at 200nm, and the channel width is fixed at 1μm. To write and read '0' and '1' states, voltage pulses of front gate voltage (V_{Gf}) and V_A were given with 1.0-1.2V and 0.95-1.15V, respectively at 200ns rise/fall time and 1μs pulse width. The V_{Gb} was fixed at 0V to -1V. The temperature was increased by 25C° from 25C° to 125C°.

III. Results and Discussions

A. Scaling L_G length

Devices were operated with Write '0'-Read-Write'1'-Read bias pattern and the current margin was investigated with scaling of L_G. Figure 1 shows current margin with various L_G length while increasing V_A. The shorter L_G, the larger current margin, which means that ratio of L_G/L_{IN} decreases, the both potential barriers on anode and cathode sides are dominantly controlled by V_A. When L_{IN} is less than 150nm, the device does not turn on even at high V_A. We need to investigate the reason with further measurements and simulation of potential barrier distribution with various ratio of L_G/L_{IN}.

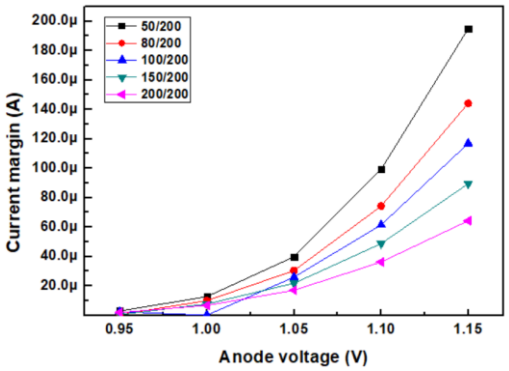

Figure 1. Current margin with various ratio of L_G/L_{IN}

B. Lowered back gate voltage

From the scaling of L_G, we selected the L_G=50nm device to investigate the effect of V_{Gb} while changing V_{Gb} from -1V to 0V. Fig. 2 shows that current margin keeps nearly constant even at -0.1V. However, when V_{Gb} is zero, the '0' state cannot be maintained due to no electron injection in the channel. Thus, the current of '0' and '1' state both show high current which leads to almost 0 current margin. This means that for memory operation the minimum V_{Gb} is -0.1V and V_{Gb} does not affect on the anode current.

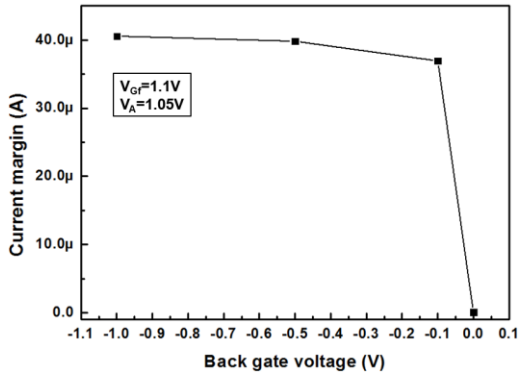

Figure 2. Current margin with lowered V_{Gb} from -1V to 0V.

C. Elevated temperatures

A W0-R-W1-R bias pattern was employed to test the Z^2-FET memory capabilities. Figure 3 show the anode and front gate bias to write and read the states, and the current at each temperature is represented with different colors. The current of '0' state is very low until 100C°. However, at 125C° (red line) the '0' state current rises to higher level, which means the degradation of '0' state.

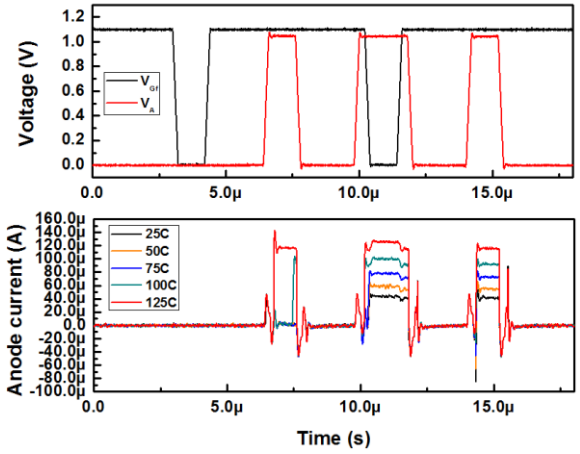

Figure 3. W0-R-W1-R bias pattern and the anode current at elevated temperatures.

Simulation results in Figure 4 explain the reason of degradation of '0' state at high temperature. The potential barrier at both sides of the channel gets lowered as the temperature increases but it is still high enough to block the injection of carriers and the current flow to the other side until 375K. However, from 400K the potential barrier is collapsed and the carriers move through the channel, and high current flows at '0' state. Simulated carrier density indicates that at high temperature, energy barriers at the cathode and anode junctions become to be lowered owing to high temperature. The electron and hole carriers are injected into the intrinsic channel owing to the lowered barriers, and these injected carriers might be recombined with thermally generated carriers till dominating over the thermally generated carriers. Finally, the current level of '0' state increases owing to high density of electron and hole carriers, resulting in the failure of memory.

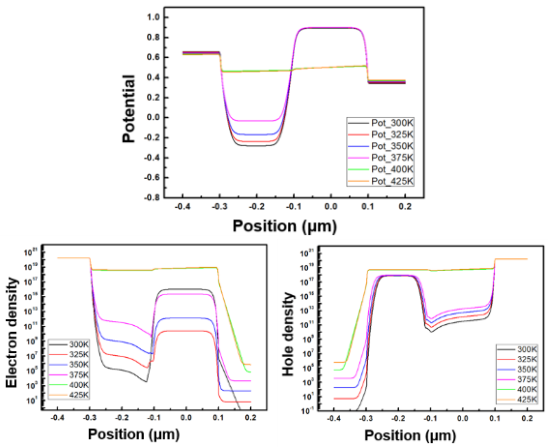

Figure 4. Simulation result of potential and carrier density at elevated temperatures during read '0'.

IV. Conclusion

Reliability of Z^2-FET devices have been studied. Experimental results of the current margin show that the L_G region can be scaled down to 50nm with reliable results and the back gate bias can be reduced down to -0.1V with almost the same current margin. The device memory operation fails at 125C° due to the degradation of '0' state. The potential barrier of both carrier rapidly collapse due to the lowered barrier and thermally generated electron-hole pairs at 125C°, which leads to memory failure.

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Towards a magnetoresistance characterization methodology for 1D nanostructured transistors

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***Abstract*— A novel approach to magnetoresistance characterization of 1D-like nanoscaled transistor structures will be presented. The proposed approach, which is based on the physical magnetoresistance effect (PMR), exploits the reality that carriers have non-discrete velocity distributions even when a single carrier species is present.**

Keywords- mobility, magnetoresistance

I. INTRODUCTION

Emerging nanoelectronic devices based on one-dimensional (1D) nanostructures, such as nanowires, nanotubes and quantum wires, promise disruptive and revolutionizing advances in electronic and optoelectronic technologies, as well as in novel chemical/biological/gas sensing technologies. Research efforts have already achieved exciting and exceptional progress in the synthesis, characterization, and fabrication of increasingly complex 1D nanoelectronic device structures, which have resulted in the demonstration of novel nanosensors, and nanoscaled electronic and optoelectronic devices. Noteworthy is the relentless effort that has driven the silicon-based "micro" electronics industry from planar to 1D-like "Fin" field-effect transistors (FinFETs) in microprocessor designs, with 1D nanostructured field effect transistor arrays now effecively regarded as the next evolutionary step away from conventional scaling-based miniaturization. Innovation in this area faces the challenge of finding new methods and approaches to characterize fundamental properties at the nanoscale. One such challenge is the need to accurately quantify carrier concentrations and mobilities in 1D nanoelectronics.

For many decades, conventional Hall-effect analysis has been the workhorse of electronic transport characterization. However, and not surprisingly, geometry and technology considerations have limited the utility of this analysis technique in the study of electronic transport in 1D nanostructures. Nevertheless, effective electronic transport parameters have been extracted from 1D nanostructures using the charge control afforded by gated field effect transistor (FET) test structures, as well as from nano-patterned Hall structures, and transient terahertz conductivity measurements of nanowire ensembles [1-9]. These characterization and analysis approaches rely on the assumption that only one single carrier species exists within the sample, and that all carriers within the sample move at exactly the same velocity. Although these electronic transport characterization approaches undoubtedly yield necessary information that has enabled optimization of materials and devices, such techniques provide limited insight into the fundamental physical mechanisms that may enable exploitation of transport phenomena unique at the nanoscale.

II. A NOVEL APPROACH

In this work, a novel approach to magnetoresistance characterization of 1D-like nanoscaled transistor structures will be presented. The proposed approach, which is based on the physical magnetoresistance effect (PMR), exploits the reality that carriers have non-discrete velocity distributions even when a single carrier is present. Conventionally, the resistance of a nanowire-like structure (length > width) with a single carrier species and a delta-like velocity distribution is expected to be independent of magnetic-field applied perpendicular to current flow, However, FinFETs and nanowire-like structures are known to exhibit significant magnetoresistance effects [10]. While the analysis of such magnetoresistance effects in 1D-like nanoscaled transistors is expected to yield additional insights into the electronic transport properties of 1D nanoelectronic structures, the feasibility of such an approach depends on whether the following can be resolved:

- What is the measurement resolution needed for such analysis to be practically realizable?
- How broad do mobility distributions need to be at practical measurement temperatures?,
- Since the Hall voltage generated cannot be measured, can a quantitative analysis method be developed?

Regarding measurement resolution, initial modeling suggests that the measurements will require high signal to noise ratio (SNR) conditions, as illustrated by the results shown in Fig. 1 in which, for convenience, carrier mobility distributions were assumed to be Gaussian. The calculations indicate that noise levels below 0.1% will be required to accurately characterize a single carrier

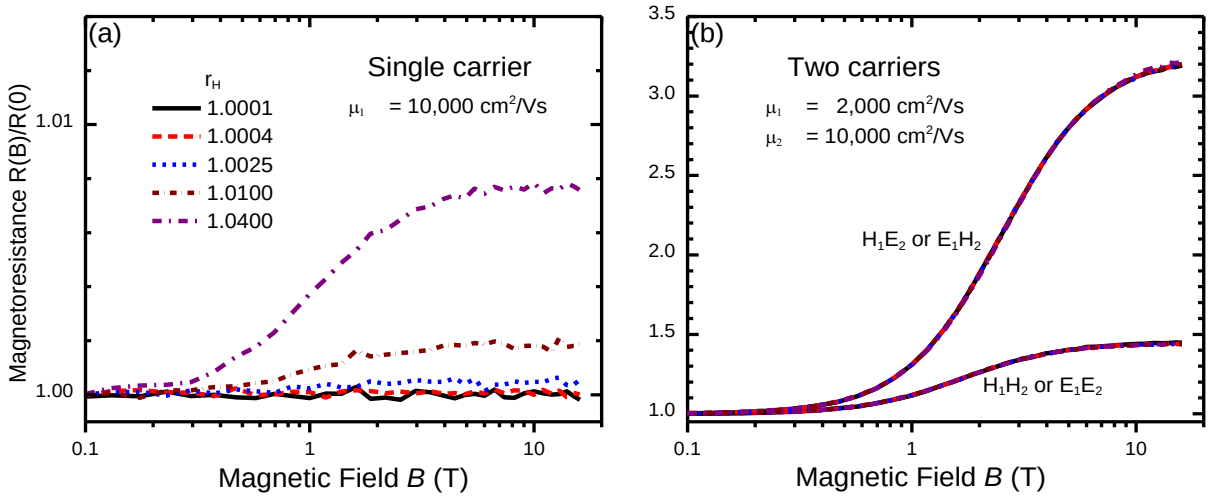

Figure 1 Normalised magnetoresistance calculated using a Gaussian carrier mobility distributions corresponding to Hall scattering factors near unity. The synthetic data has a simulated measurement noise level of 0.01%, for the case of (a) a single carrier species, and (b) two carrier species. Electrons and holes are denoted by E and H, respectively. It is important to note that although carrier type cannot be determined, ambipolar transport can easily be discriminated since it yields the highest SNR.

mobility distribution with a minimum full-width-at-half-maximum to average mobility ratio (dμ/μ) of 0.1. This is approximately equivalent to a Hall scattering factor r_H = 1.01. By reducing noise levels below 0.01%, a single carrier with a mobility distributions with dμ/μ=0.05 (rH = 1.0025) can realistically be measured employing phase-sensitive techniques (e.g., lock-in amplifier based). It is important to note that such high SNR must be achieved while minimizing self-heating effects [11]. On the other hand, regarding mobility distributions, published results suggest that mobility distributions are sufficiently broad and/or complex to be resolvable in bulk and 2D semiconductors structures via magnetic-field dependent magnetotransport measurements and mobility spectrum analysis techniques [12-14]. These reports, together with the observation of multiple carrier effects associated with sub-band modulation effects in quantum confined structures [15], suggests that PMR is a feasible electronic transport characterization approach for nanoscaled devices.

Analysis methodology considerations regarding parameter extraction employing an iterative multiple carrier fitting (MCF) and mobility spectrum analysis approaches will be presented, together with examples of its application in practical 1D-like nanostructures. The impact of contact and access series resistances on extracted parameters will also be discussed.

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Design of Dickson Rectifier for RF Energy Harvesting in 28 nm FD-SOI technology

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***Abstract*— In the context of the radio frequency energy harvesting, RF-DC converter based on a one stage Dickson voltage rectifier has been studied and realized in 28 nm FD-SOI technology. After the analysis of the operating constraints of the circuit, a choice was made on the N-low threshold voltage transistor (NLVT). Moreover, the back gate polarization (BGP) effect, on circuit performance, has been analyzed and a dynamic BGP is proposed which improve rectifier performance.**

Keywords: Dickson rectifier, RF energy harvesting, FD-SOI 28 nm, Dynamic Back Gate Polarization

I. INTRODUCTION

A promising growing market of IoT like wireless autonomous sensors lead to a question of "How to manage batteries replacement and recylcing?". In the same time numerous wireless objects spread ambiant RF energy.. For example, measured RF power density on GSM Communications and WLAN frequency bands could reach 10 nW/cm^2, as shown in [1-2]. Furthermore, recent innovation in microelectronics reduce the sleep power of microcontroller down to 50 nW [3]. So today, it becomes possible to supply these sleep mode power with RF energy harvesting.

To convert the RF signal into a DC signal RF-DC a nonlinear element (usually diode) is required.. Some studies, e.g. [2], indicates that a sensitivity of up to -40 dBm at 2.45 GHz can be achieved by using tunnel diodes. Furthermore, Voltage doubler designed in 0.18 µm CMOS technology with 1 V output voltage at -27 dBm input power as been demonstrated [4]. However, in CMOS technology, there are undesirable parasitic effects, which degrade the performance. To limit these parasitic effect, a new technology FD-SOI (described as more appropriated for design of low power circuit) has been investigated. In this paper, design and measurements of a voltage doubler using 28 nm FD-SOI technology is proposed.

II. RF VOLTAGE MULPLIER PRINCIPLE AND TECHNOLGY

A. Dickson rectifier structure

Different topologies of voltage multipliers can be used in the field of energy harvesting, Dickson voltage multiplier is widely used thanks to a good trade off between simplicity and performance. N-stages of Dickson voltage rectifier is described in fig. 1. The non-linear components (diodes) will be replaced by FD-SOI 28 nm transistors configured as a diode. Consider a one stage rectifier (represented by D1, D2, C1, and C2 in Fig. 1). When the input voltage is negative, the capacitor C_1 is charged through the diode D_1.

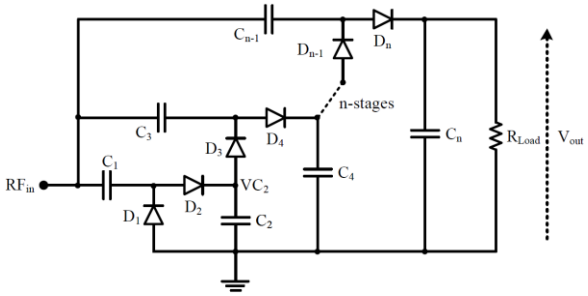

Figure 1. N-stages Dickson voltage rectifier.

On the other hand, when the input voltage becomes positive, capacitance C_2 stores the charges resulting from the sum of the input voltage and the voltage across C_1 via D_2. In the case of ideal diodes, the final voltage thus transferred to C_2 (VC_2) without load is equal to $2.(\sqrt{2}V_{RF,in}-V_{th,})$ with V_{th} represent the threshold voltage of the diode. It is obvious that the average output voltage (VC_n) of such *n*-stage multiplier with diodes with the conduction threshold V_{th} is given by the equation Eq.(1):

$$VC_n = 2.n(\sqrt{2}.V_{RF,in} - V_{th}) \quad (1)$$

B. 28 nm FD-SOI technology

FD-SOI technology offers advantages in terms of leaks and parasitic compared to bulk technology. Thanks to the "BOX" (Burried Oxide) insulation placed between the substrate and the active part of the transistors, this technology reduces the different types of leaks and losses in the substrate. Moreover, the substrate can be seen as another grid, called a back gate (BG), and its polarization makes it possible to modify the parameters of the transistor.

In the FD-SOI 28 nm, four types of transistors are available: N and P LVT for "Low Voltage Transistor", and, N and P RVT for "Regular Voltage Transistor".

The measurements of *I-V* characteristics of both N and P types for LVT and RVT transistors reveal that NLVT has the lowest threshold voltage, but, has the largest leakage current. Nonetheless, compared to NLVT, NRVT transistor has a marginally larger threshold voltage with a smaller leakage current.

For N-type transistor in FD-SOI technology, the threshold voltage decrease if the BG is positively biased. But on the other hand, the leakage current will increase and vice versa. This variation is measured for NLVT transistor (Fig. 2).

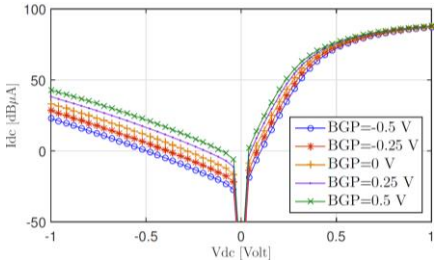

Figure 2. NLVT *I-V* characteristic Vs. back gate polarization (BGP).

III. BACK GATE POLARIZATION

Fig. 3 illustrates the variation of the output voltage of one stage Dickson voltage rectifier as a function of the input power for different BGP. For same RF input powers, the output voltage obtained for a positive BGP is greater compared to when the BGP is negative (for both diodes D_1 and D_2). Moreover, when the BG is connected directly to the ground, the output voltage is even larger than the voltage obtained for a positive BGP. As the diodes D_1 and D_2 operate in reverse mode (when D_1 is on, D_2 is off and vice versa), with a static BGP, it is impossible to insure a small threshold voltage and a low leakage current at the same time.

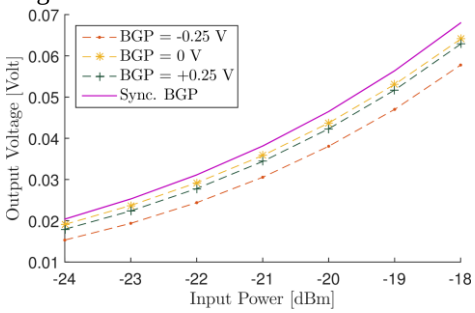

Figure 3. Output voltage for different BGP.

Furthermore, an improved polarization solution is proposed, in which the BGP voltage is varied as a function of the operating mode of D_2. This dynamic BGP allows the control of leakage current and threshold voltage as a function of the operating mode of the diode D_2.

To realize this synchronization of the BG (Sync. BGP), the BG of the transistor D_2 is connected directly to the input of the rectifier. Whereas, the BG of D_1 will always be connected to ground. In this way, a dynamic BGP is proposed in this article to improve circuit efficiency.

IV. RECTFIER MEASUREMENTS RESULT

In this section, we present the measurement results obtained from designed Dickson voltage doubler. The measurements are made using a manual station probe SUSS MICROTEC PSM6RF and Infinity probes with 50 µm pitch. The power conversion efficiency (*PCE*) is calculated as a function of load resistance (R_{Load}) for different input powers.

The *PCE* is calculated as the ratio between the output power and the power presented at the input of the rectifier, and its presented in Figure 4. At -15 dBm, the maximum of *PCE* obtained is 38 % with a R_{Load} of 5 kΩ (figure 4-a). Figure 4-b shows the maximum *PCE* obtained in function of input power. Furthermore, the maximum obtained is 82% for an input power of -4 dBm.

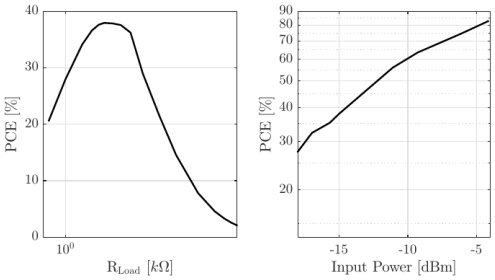

Figure 4. *PCE* Vs. Rload at -15 dBm (a), Maximum of *PCE* Vs. input power (b).

CONCLUSION

In this article, the design of a voltage doubler optimized using 28nm FD-SOI technology. NLVT is the most suitable transistor due to its low threshold voltage. At -15 dBm, the *PCE* max achieved is 38 % with a R_{load} = 5 kΩ. Furthermore, the maximum *PCE* reachs 82% for an input power of -4 dBm. Finally, when a dynamic BGP is applied, a higher output voltage than with a fixed polarization (positive, negative or zero).

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A Low Noise Wideband VCO with 4 bit Switched Capacitor Array

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***Abstract*— In this work, firstly, a narrowband Voltage Controlled Oscillator is designed which uses Cross-Coupled Differential Topology and a capacitor-inductor based tail filtering circuit. The proposed VCO also uses PMOS inversion mode MOS Varactor for frequency tuning and a combination of fixed MIM and variable MOS capacitance as tank capacitor. The LC tail filtering circuit is used to supress those noise-frequencies which are more influenced by the tank current when the VCO operates in current limited region. Simulations were done in cadence Virtuoso using UMC 180nm technology which indicated that the proposed narrowband VCO demonstrated a phase noise characteristics of -128.7 dBc/Hz, which is lower in comparison to most other VCO structures proposed in literature. Secondly, the proposed VCO design was extended to include a 4 bit Switched Capacitor array, thereby designing a wideband VCO capable of working in the frequency range 2.18 GHz to 4.18 GHz. The single ended switched capacitor array was used for coarse tuning and overcome noise sensitivity due to varactor gain. Simulation results showed that at high frequencies, the phase noise performance of the proposed VCO degraded due to large amplitude variations from current limited to voltage limited region. Finally, an automated amplitude control (AAC) System was added in the design of wideband VCO so as to limit the amplitude variations. Simulation results showed that the proposed VCO with AAC was successful in preventing the oscillator from entering the voltage limited region and a phase noise reduction of 3dBc/Hz was observed.**

Keywords- ***Cross Coupled Differential pair, VCO, Tank Oscillator, In-Phase Noise, Tail Filtering Technique, Automatic Amplitude Control, Switched Capacitor Array.***

I. INTRODUCTION

Over the last few decades, there has been a significant growth in Radio frequency integrated circuits (RFIC's) design and combining RF as well as digital ICs on a single chip for realizing complex System On Chip designs (SoC) has become a general trend [1,2]. Low-power, low noise design is an important prerequisite of such designs. A Voltage controlled oscillator (VCO) is a special class of oscillator used in many RF Transceivers wherein the frequency can be varied to a particular extent by varying the control voltage.

Among the important performance metrics, phase noise and power consumption (Van der Pol) are of utmost importance and has been a burning topic of research over the years.

The earliest works on Oscillators includes that by Elihu Thomson, called the Thomson Oscillators. Other noted works includes [3]. To explain the phase noise spectra of Oscillators, many models were proposed, among which the LESSON'S model which explains the 1/f2 region very well is widely followed. The LTV Model is also a widely followed model for explaining noise spectra of oscillators. The Phase Noise issue has attracted many researchers over the years and various proposals have been put forward by researchers to overcome them. The tail current source was found out to be one of the major sources of Phase Noise. The high-frequency tail current noise at twice the oscillation frequency is found out to be down-converted into phase noise by the hard switching oscillator. Two different techniques as such as inductive degeneration and capacitive filtering were also reported, which suppress the low-frequency tail current noise as well. Since both high-frequency and low-frequency tail current noise are now prevented from flowing into the oscillator core, the nonlinearities in the LC tank are no longer critical. Another technique proposed by [4] indicates that the high-frequency tail current noise is removed by an on-chip lowpass LC filter and low frequency noise is reduced by minimizing size of CMOS varactor.

This work focuses on the reduction of thermal noise by using an auto-zero configuration, or amplifier chopping. First of all, a narrowband LC-VCO design for improved phase noise performance has been presented. The narrowband VCO design is extended to design a wideband VCO Circuit.

II. PROPOSED DESIGN

In the proposed work, initially, a 3 GHz narrowband VCO is designed. A LC based tail filtering circuit is used for improving the phase noise performance of the proposed circuit Fig. 1 & Fig. 2. Then, the design is extended to include a 4 bit switched capacitor array, thereby extended the VCO to work for a wideband range of 2 GHz with frequency ranging from 2.18-4.18 GHz. Then, an automated amplitude control system is

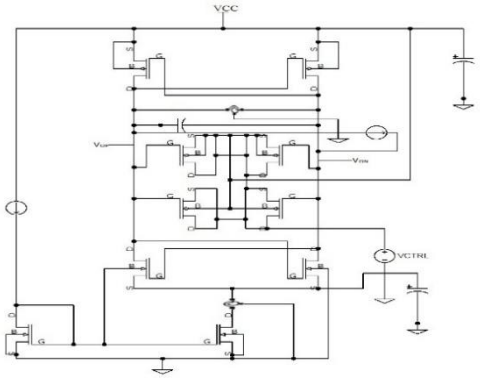

Figure 1. Proposed 3 GHz Cross Coupled VCO Design

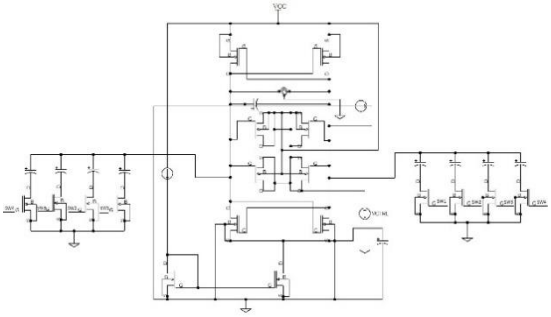

Figure 2. Wideband VCO with Switched Capacitor Array

added to further improve the phase noise performance for the proposed wideband VCO.

III. RESULTS

For analyzing the performance of the proposed narrowband VCO, different simulations were performed in Cadence Virtuoso using UMC 180nm technology parameters. For calculating the phase noise, the LTV Model is used. The Phase noise variation at 1MHz with tuning voltage shown in Fig. 3. The simulations were done for wideband VCO with switched capacitor array in Cadence Virtuoso using UMC 180nm technology. The results are shown in Fig. 4 & Fig. 5.

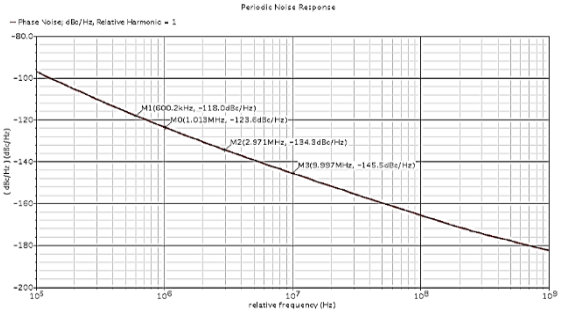

Figure 3. Phase noise analysis for tank current at 2.5 GHz

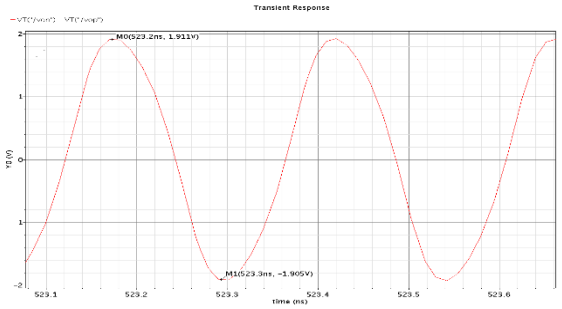

Figure 4. Transient response of VCO

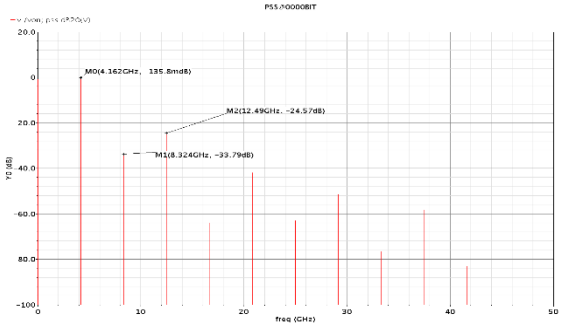

Figure 5. PSS analysis

IV. CONCLUSION

A Wideband VCO with Switched capacitor Array operating at a frequency of 2.18 GHz-4.18 GHz has been designed. For this, first of all, a narrowband LC Voltage Controlled Oscillator operating at 3 GHz using Cross Coupled Differential Pair has been designed and simulated. A phase noise reduction of around –4dBc/Hz was observed while employing the noise filtering technique. Then, the VCO design was extended to include a 4 bit switched capacitor array. Simulations were performed and a bandwidth of 2GHz ranging from 2.18 to 4.18 GHz was obtained with a minimum phase noise of -117dBc/Hz at 4.18 GHz. Finally, an automatic amplitude control system was added to circuitry to prevent the Oscillator from entering Voltage limited region at high frequency side of multiband.

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FoMPy: A figure of merit extraction tool for semiconductor device simulations

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Abstract—**The aim of this work is to present an effective tool that extracts the main figures of merit (FoM) of a semiconductor's IV curve and provides useful statistical parameters for variability studies. It includes several methods to extract the threshold voltage. Two state-of-the-art devices have been used as benchmarks in order to show its capabilities.**

Keywords; python tool; threshold voltage; figure of merits; FinFETs, nanowires, FoMPy.

I. Introduction

In this paper we present a python tool [FoMPy] developed for automatic extraction of the main figures of merit that characterize the IV curve of a semiconductor device. When working with variability studies, where hundreds or thousands of simulations need to be examined, FoMPy not only automatically extracts all the FoMs but also performs a thorough statistical analysis. A first approach of the problem was to obtain the threshold voltage (V_T) as it is the most commonly used estimator of a device's behaviour and resilience towards variability. V_T can either be obtained from the drain current or capacitance characteristics [1]. Different extraction methods can be found in the literature [1] but it is unclear which one is the best candidate for the future technology nodes. In this tool we have implemented several of the most widely used V_T extraction methods which allow for a comparison between different threshold voltage dependent results. FoMPy will soon be available for the scientific community to use on various online sites.

II. Benchmark devices

The threshold voltage study has been performed for both a 10.7 nm gate length Si FinFET and a 10 nm gate length Si GAA nanowire (see schematics in Figure 1).

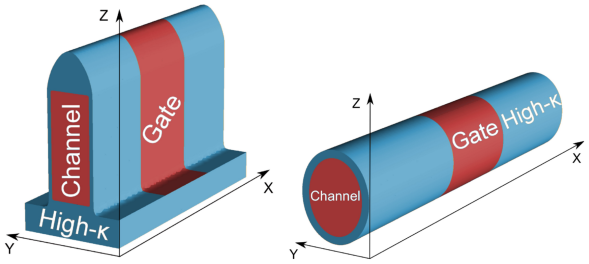

Figure 1: Schematics of the Si FinFET [3] and GAA nanowire [2].

These are two state-of-the-art devices modeled from scaled experimental transistors following the ITRS guidelines [4]. A complete summary of the devices dimensions for the scaled devices can be found in [2][3]. Note that this tool can be used for any other semiconductor devices, as it is only necessary to have an IV curve as an input parameter.

III. Extraction Methods

Initially in FoMPy we have implemented several V_T methods that are widely used in industry [1][5]. Moreover, further implementations of the code can be easily incorporated in the future to meet specific needed criteria. The V_T extraction methods implemented are shown below and explained in detail in [1].

A. Second Derivative (SD)

This method sets V_T at the gate voltage (V_G) at which the derivative of the transconductance (g_m) is maximum (i.e $dg_m/dV_G = d^2I_D/dV^2_G$). Note that in the saturation region we use instead $d^2I_D^{0.5}/dV^2_G$ [1].

B. Constant Current (CC)

The user defines a fixed arbitrary current of the IV curve at which $V_G = V_T$ (see an example of this methodology in [5]).

C. Third Derivative (TD)

Similar to the SD method, but the V_T criteria is the maximum of the second derivative ($d^3I_D/dV^3_G = 0$).

D. Linear Extrapolation (LE)

V_T is extracted as an extrapolation of the maximum slope in the linear region on the x axis intercept ($I_D = 0$).

E. Cross Extrapolation (CE)

V_T is set to the value where the extrapolations of both the linear and the saturation regime on logarithmic scale cross.

IV. Extraction Results and Discussion

The V_T values extracted by FoMPy are presented in Table I for the several methods implemented. Note that in all cases the tool extracts V_T through a formula, but in the CC method the criteria has to be user defined [5]. A visual description on the implemented V_T extraction methods is presented in Figure 2.

TABLE I. THRESHOLD VOLTAGE METHODS RESULTS FOR THE SIMULATED SI FINFET AND SI GAA NW IN THE LINEAR AND SATURATION REGION

Method	*Si FinFET (V_D = 50 mV)*	*Si FinFET (V_D = 0.7 V)*	*Si GAA NW (V_D = 50 mV)*	*Si GAA NW (V_D = 0.7 V)*
SD	0.272	0.182	0.373	0.330
CC	0.246	0.193	0.425	0.377
TD	0.230	FE*	0.378	0.293
LE	0.240	0.154	0.328	0.290
CE	0.342	0.358	0.417	0.460

* Failed to extract

All methods, except CE, produce smaller values in the saturation region than in the linear region. Note that the third derivate is not able to properly extract the V_T at high drain bias, as also seen before in [1].

As we can see FoMPy managed to extract in several ways the threshold voltage for these benchmark devices. As the effectiveness of the tool has been proven, it presents itself as a way to easily compare V_T-dependent results unconstrained by the methodology used to extract them. As we mentioned before, on top of the threshold voltage, FoMPy includes several other functions that allows us not only to extract other important FoMs (such as subthreshold slope, OFF-current, drain-induced-barrier-lowering and ON-current), but also it can perform statistical analysis for variability simulations.

ACKNOWLEDGMENT

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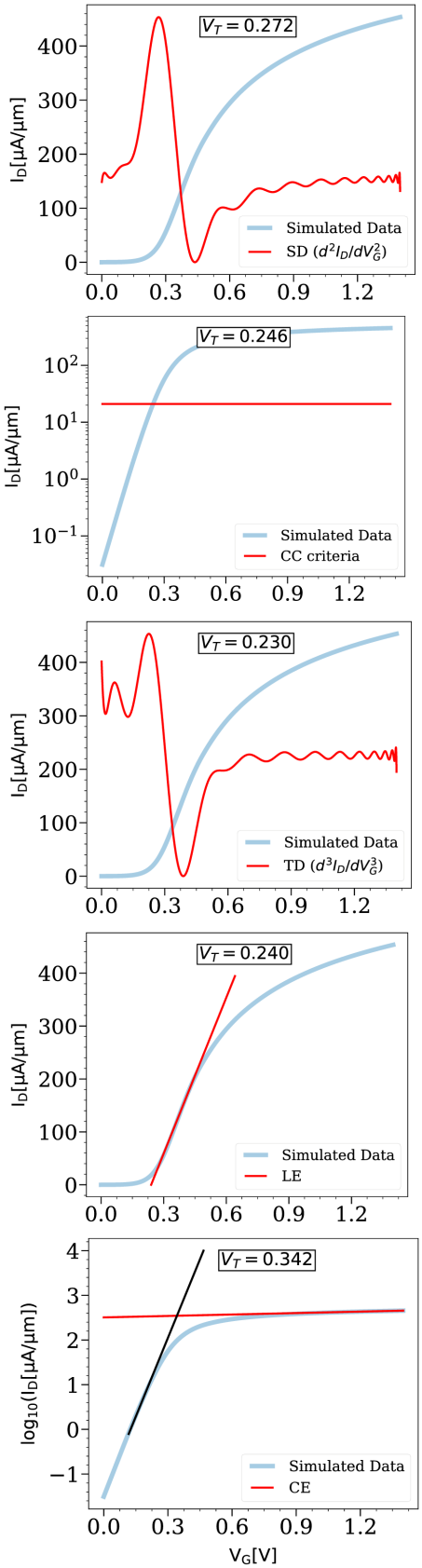

Figure 2: SD, CC, TD, LE and CE methods of V_T extraction applied to the 10.7 nm gate length FinFET at $V_D = 50$ mV.

Impact of TFET Reverse Currents Into Circuit Operation: A Case Study

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***Abstract*— Tunnel FET transistors (TFETs) are one of the most promising candidates to replace CMOS transistors for future integrated circuits. However TFET-based circuit design can exhibit significant limitations due to their reverse conduction currents caused by the direct bias of the intrinsic diode of these transistors. In this paper we analyze in depth this issue through the design of charge pump (DC-DC step up converters) circuits for energy harvesting applications. The proposed solution mitigates the impact of reverse conduction currents and, thus, improves power conversion efficiencies (*PCE*) compared to previous designs.**

***Keywords*- Tunnel transistors, Steep subthreshold slope, Charge pump, Reverse conduction, Energy harvesting.**

I. MOTIVATION OF THIS WORK

Internet of Things (IoT) applications, in which ultra-low power devices and systems are combined with energy harvesting, has led to the irruption of new applications that previously were not possible. Emerging technologies, including emerging transistor devices, circuits, and architectures, allow aggressive scaling of supply voltages to achieve ultra-low power operation and, thus, overcome power density and energy efficiency challenges exhibited by CMOS technologies [1]. Tunnel field-effect transistors (TFETs) are one of the most attractive steep subthreshold slope (*SS*) devices currently being investigated as a means of overcoming such limitations of CMOS [2]. A smaller *SS* makes it possible to lower threshold voltage while keeping leakage current under control, facilitating low voltage operation.

Circuits for logic applications have been thoroughly evaluated using TFETs and benefits in higher performance domains in power or thermal limited applications could be achieved [3]. More recently, other applications domains in addition to logic ones have been identified. In particular, and relevant to the IoT application field, it has been shown that front-end circuits for energy harvesting can benefit from the superior performance of TFETs at low voltages [4], [5]. These TFET-based circuits take advantage of the reduced turn-on voltage of these transistors with respect to Si FinFET to very much improve performance with weaker input signals. In addition, the higher I_{ON} current exhibited by TFETs at low supply voltages translates into a reduced on-state resistance which contributes to decrease resistive power losses improving *PCE*. Finally, according also to [4], [5] unidirectional conduction of TFETs has a positive impact on *PCE* through reduced reverse losses. Reverse losses are associated to the symmetric conduction of conventional transistors which conduct under both positive and negative drain to source voltages. However, although *P* (*N*) TFETs do not conduct under low positive (negative) drain to source voltages, enough high reversed drain to source voltages produce the forward biasing of their intrinsic *p-i-n* diode which translates in large losses currents. That is, the advantage associated to unidirectional conduction is limited to enough low amplitude input signals (or enough low input power).

In this paper, we analyze in depth the operation limits of TFET-based switched capacitor charge pumps (*SCCP*) with respect to voltage levels of input signals and input power, and propose tuning the *SCCP* topology to the specific TFET characteristic to better control reverse currents and thus, extend the voltage/power operation range of TFET-based charge pumps.

II. DESIGN CHALLENGES OF TFET-BASED SCCPS

Fig. 1a shows the schematic of the selected series-parallel *SCCP* [6]. Although most efficient topologies could be selected, its simplicity will clearly illustrate the inherent problem of the design of charge pumps using TFETs. The design of these circuits using TFETs is not straightforward because it must take into account the particular characteristics of these transistors in terms of their unidirectionality. As discussed in the previous section, the TFET could exhibit significant reverse currents for very negative (positive) values of the drain-source voltage of *N* (*P*) transistor. When the clock signal is high (*PAR* phase), transistors M_1, M_3 and M_4 are on, charging both capacitors to the input voltage. In this phase transistor M_5 could discharge capacitor C_L in the *PAR* phase since $V_{DS,M5}=V_{IN}$ and, therefore, being $I_{M5}\neq 0$. On the other hand, when the clock signal is low (*SER* phase), only the transistors M_2 and M_5 are switched on. Then, M_4 could have reverse conduction currents for high values of the input voltage since $V_{DS,M4} = -V_{IN}$. Thus, part of the current flowing through the series connection of capacitors C_1 and C_2 would go through M_4 instead of charging the output impedance via M_5.

Reverse currents can be reduced if transistors M_4 and M_5 are not operated with reversed drain to source bias above the diode´s on voltage. To achieve this, a new topology is

proposed in which transistors M_4 and M_5 are implemented by the series connection of two transistors. Fig. 1b shows the currents through the transistors M_4 and M_5 of the original and the proposed topologies (implemented using 20nm GaN/InN single gate TFETs [7]) for V_{IN}=1V. Note that the modified topology allows a significant reduction of reverse currents due to the distribution of the drain to source voltages between the series connected transistors.

III. Simulation results

The proposed modification of the original topology is evaluated using TFET models reported in [7]. Simulation results are compared with those obtained for the original topology (hereafter "*1PH*"). In addition, a modification of *1PH* employing two non-overlapping clock phases ($V_{CLK,1}$ and $V_{CLK,2}$) is considered to avoid current leakage from M_2 to M_3 at transitions when the clock switches low. This topology ("*2PH*") applies $V_{CLK,1}$ to the gate of all transistors except in M_2, which is replaced by an *N* type transistor. When $V_{CLK,1}$ is at high level the *PAR* phase is activated and the *SER* phase when $V_{CLK,2}$ is. The M_5 transistor is not switched to *N* type to ensure that the increase in the output voltage does not affect its gate-source voltage. Moreover, being *P* type, it is activated when lowering $V_{CLK,1}$, guaranteeing a suitable V_{GS} voltage to operate properly. Both *1PH* and *2PH* topologies are evaluated using the proposed configuration ("*1PH-PROP*" and "*2PH-PROP*"). In addition, the *2PH* topology is designed using predictive 20nm FinFET transistors for high-performance (HP) obtained from the PTM web page [8] and is denoted as *"2PH-FinFET*". Fig. 2a illustrates *PCE* versus the range of input voltages analyzed for the five topologies studied. These results show that the TFET-based designs are more efficient than the one that uses FinFET transistors. On the other hand it is observed that, unlike conventional topologies, for the larger values of the input voltage efficiency hardly degrade due to reverse conduction currents. For example, for V_{IN}=1V *PCE* improves by approximately 25% with respect to the original (*1PH* and *2PH*) and FinFET topologies. Note the improvements achieved in the proposed topology in *2PH-PROP* (10% for V_{IN}=1V).

The modification of the proposed topology can be easily extended to more complex (and efficient) charge pumps designs in which reverse currents are obtained. In the TFET-based cross coupled implementation of a charge pump [5], this problem occurs again for high values of V_{IN}. Similarly to the *SCCP* topology, the proposed modification based on the series connection of transistors reduces the impact of these reverse currents, improving their power conversion efficiency. Fig. 2b shows *PCE* vs. V_{IN} for the original and the proposed topologies, verifying that, from V_{IN}=0.2V, $PCE_{PROP}(2 \cdot V_{IN}) \simeq PCE_{ORIG}(V_{IN})$.

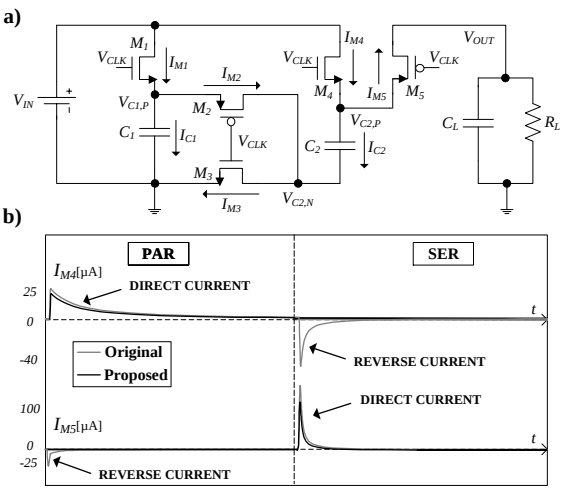

Fig. 1 (a) Schematic of the original *SCCP*. (b) Transistor-based implementation of the *SCCP*. (b) Currents flowing through transistors M_4 and M_5 (V_{IN}=1V) for the original and the modified *SCCP* circuits.

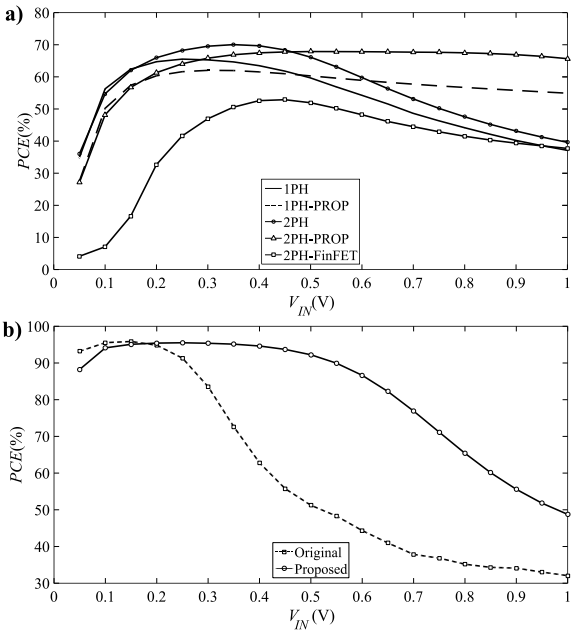

Fig. 2 Evaluation of the *PCE* (%) versus V_{IN} performance of the original and proposed implementations of *SCCP* designs. (a) *SCCP* of Fig. 1a and (b) cross coupled.

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Nanoindentation effects on the electrical caracterization in Ψ-MOSFET configuration

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Abstract – The effect of nanoindentation on the electrical transport in the Ψ-MOSFET configuration is presented. Systematic measurements were performed in order to evaluate the dependence of the drain current on the probe pressure in different operating regimes. This enabled to investigate the existence of the metallic β-Sn crystallographic form of silicon, which emerges at high pressures and shows a significant impact in the accumulation regime.

Keywords – SOI, Ψ-MOSFET, nanoindentation, metal-semiconductor contact, field-effect

I. Introduction

The Ψ-MOSFET configuration was successfully used for SOI substrate electrical characterization since 1992 [1]. Besides its simplicity of use, the physics of the contacts is still misunderstood. In this setup, the drain current (I_D) is measured between two metallic probes placed on the SOI wafer with controlled pressure (Figure 1). Even though the metallic (tungsten carbide) probes on a low-doped (10^{15} cm^{-3}) silicon film should act as a Schottky contact theoretically, the behaviour of I_D-V_D curves is ohmic (see for example Figure 2 obtained on a SOI with 88nm film thickness). The explanation given so far is that the ohmic behaviour originates from the "defects" created by the pressure applied on the probes [1], [2]. TEM images (not shown here) performed on a probe trace (crater) within an 88nm film with a pressure of 90g show no defects or crystalline dislocations in the silicon film. In this paper, we explore another point of view of the ohmic behaviour: the formation of the β-Sn form of silicon under nanoindentation [3].

II. Results

The SOI substrates have a BOX thickness of 145nm and a silicon film thickness of either 88nm or 12nm. A passivation layer of thermal SiO_2 (of about 2nm) is grown on the SOI surface. Islands of 5x5mm² were patterned using photo-lithography and reactive ion etching.

For each pressure on the probes, we traced the static characteristics (I_D-V_D and I_D-V_G), extracting the threshold (V_T) and the flat band (V_{FB}) voltages. The gate voltage was fixed to values corresponding to strong inversion and accumulation. The drain current was obtained by making an average over a 40 seconds sampling interval. This I_D value is represented versus the pressure applied on both probes (Figures 3-6). In all cases the I_D increases with the pressure during the loading phase and decreases during unload. This is consistent with previous results of nanoindentation with diamond probes on p-type doped bulk silicon substrates [4], [5]. Experiments and simulations [6] confirmed that the ohmic nature of the contacts was related to the formation of a metallic β-Sn phase of silicon which appears for high pressures. Additionally, the literature showed a dissymmetry between the load/unload phases for different polarization setups [7]. Indeed, the drain current is significantly lower in the unloading phase in the accumulation regime (Figure 4) compared to the inversion regime (Figure 3). This shows the effects of nanoindentation on hole conduction.

In the case of a thin film (Figure 5 and 6), the electrical measurements show an increase of the drain current which begins only from a threshold pressure. This suggests that the formation of the metallic β-Sn phase of silicon appears for higher pressures in thin silicon film SOI. Considering that the depth of the craters is larger than the silicon film thickness in this case [8], the allotropic transformation may take place laterally, explaining the difference. This effect is further emphasised in the I_D-V_D characteristics traced in the accumulation regime (Figure 7). Between 20g and 40g, the shape of the drain current completely modifies, turning into an ohmic contact. This transformation does not take place in the case of a thick film (Figure 8).

III. Conclusion

The present work investigates the presence of the β-Sn phase of silicon during indentation in the Ψ-MOSFET configuration and its contribution to the conduction at the source/drain metal-semiconductor contacts. Work in progress is aimed at describing in detail the transport mechanisms involved.

Acknowledgment

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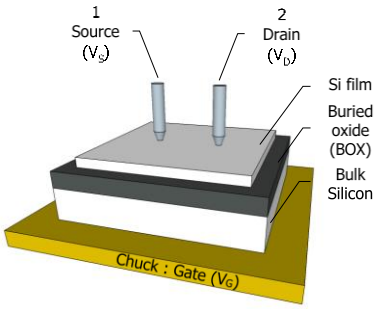

Figure 1. Experimental setup of the Ψ-MOSFET configuration.

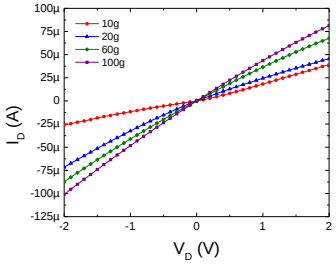

Figure 2. Drain current vs. drain voltage for different probe pressures in accumulation conditions (V_G= -6V, V_D = 0.1V). Thin film (88nm) and BOX (145nm).

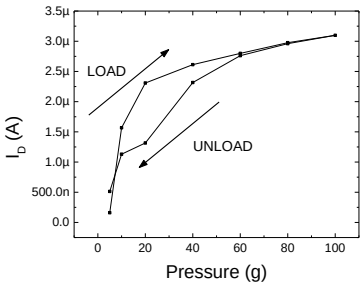

Figure 3. Drain current vs. probe pressure. Thick film (88nm) and BOX (145nm). Measurements realized in inversion conditions (V_G = 8V, V_D = 0.1V, V_T = 2.1V).

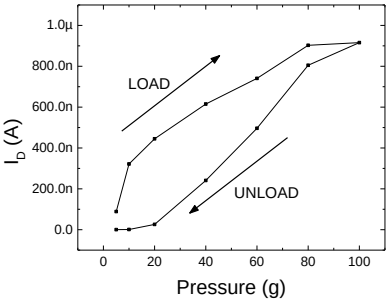

Figure 4. Drain current vs. probe pressure. Thick film (88nm) and BOX (145nm). Measurements realized in accumulation conditions (V_G = -6V, V_D = 0.1V, V_{FB} = -1.1V).

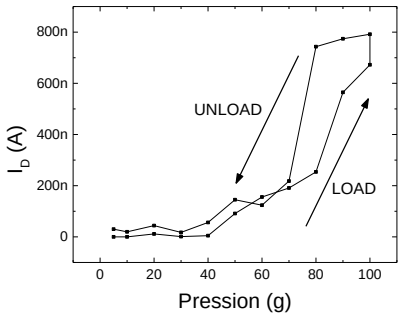

Figure 5. Drain current vs. probe pressure. Thin film (12nm) and BOX (145nm). Measurements realized in inversion conditions (V_G=16V, V_D = 0.1V, V_T = 11.2V).

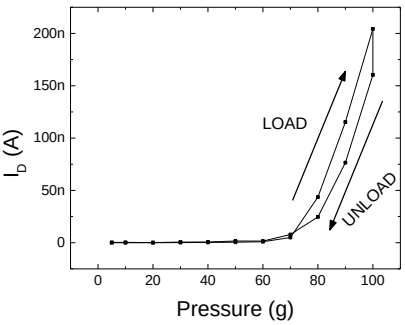

Figure 6. Drain current vs. probe pressure. Thin film (12nm) and BOX (145nm). Measurements realized in accumulation conditions (V_G= -12V, V_D = 0.1V, V_{FB} = -7.1V).

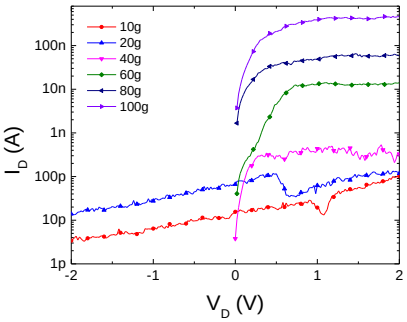

Figure 7. Drain current vs. drain voltage for different probe pressures in accumulation conditions (V_G= -12V, V_D = 0.1V). Thin film (12nm) and BOX (145nm).

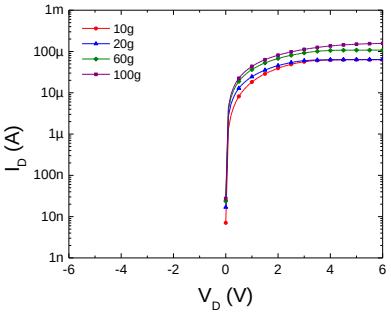

Figure 8. Drain current vs. drain voltage for different probe pressures in accumulation conditions (V_G= -6V, V_D = 0.1V). Thin film (88nm) and BOX (145nm).

Impact of Electron Effective Mass Variation on the Performance of InAs/GaSb Electron-Hole Bilayer Tunneling Field-Effect Transistor

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***Abstract*—In the roadmap for the optimization of Electron-Hole Bilayer Tunneling Field-Effect Transistors (EHBTFETs), the employment of III-V compounds is regarded as an appealing solution due to their direct band-to-band tunneling injection. In order to achieve both n and p acceptable operation channels, the combination of As- and Sb-based III-V materials leads to the proposal of a heterosturcture InAs/GaSb-EHBTFET. In this paper, we analyze the impact that the required ultrathin InAs layers have on the electron effective mass and, subsequently, on the device performance.**

Electron-Hole Bilayer Tunneling Field-Effect Transistors, band-to-band tunneling, III-V compounds, quantum confinement effects.

I. Introduction

Tunneling field-effect transistors (TFETs) have remained throughout the last decade as non-disposable candidates to replace conventional MOSFETs in spite of their well-known ON-current level limitation. One of the most recent proposals is the design of an electron-hole bilayer TFET (EHBTFET) based on an InAs/GaSb heterojunction in which the quantum confinement across the body thickness direction allows to close the broken gap between the InAs and the GaSb and, therefore, makes the structure become suitable to behave as a steep slope switch. However, due to the effect that the utilization of very thin InAs slabs entails on the electron effective mass compared to bulk reference values, it is important to assess the influence of this phenomenon on the performance of the InAs/GaSb-EHBTFET.

II. Device Description and Simulation Approach

The device under consideration is depicted in Fig. 1 and features p+ GaSb source, intrinsic top/bottom InAs/GaSb channel, and n+ InAs drain. Top and bottom gate insulators are 3nm HfO_2 layers. Additional HfO_2 spacers have been included at the top-left and bottom-right of the channel for suppressing parasitic leakage tunneling contributions. Our simulation approach makes use of Synopsys Sentaurus with an additional customization inside it which allows to incorporate subband discretization in a self-consistent way by modifying the so-called *Apparent Band-Edge Shift Model*. By doing so, the so far semiclassical edges of the conduction and valence bands are readjusted to make them coincident with their first subbands. Band-to-band tunneling (BTBT) generation rates are calculated by means of the dynamic nonlocal BTBT model of Sentaurus.

III. Results

Assuming the hypothesis that the isotropy of the InAs Γ-valley is still preserved when dealing with reduced values of t_{InAs} [1], we will use the modified values of the electron effective mass for solving Schrödinger-Poisson along the vertical direction inside the channel to determine the position of the first electron subband for a given InAs slab thickness. Considering this, we need to make an adequate t_{InAs} choice so as to make the OFF-state attainable when V_{TG}=0V.

Table I contains the electron effective masses extracted from $k{\cdot}p$ calculations [2] taking into account nonparabolicity effects through the inclusion of the α parameter. In our study, we will consider bulk hole effective masses for GaSb (m_{hh}=0.4m_0) which yields weaker confinement effects at the bottom of the channel compared to the upper slab. Yet, it was demonstrated that in III-V compounds, the top of the valence band is connected with the conduction band through an imaginary branch with lower mass [3] (approximately equal to that of light holes, m_{lh} [2]) even in the presence of strong quantization effects.

TABLE I. Electron effective mass variation for the Γ-valley as a function of the InAs thickness

InAs thickness	$m_e(\Gamma)$	α(eV^{-1})	Bulk $m_e(\Gamma)$
5nm	0.037	3.6	0.023
10nm	0.026		
15nm	0.025		

Fig. 2 shows the top gate voltage at which first subbands, E_{e1} and E_{hh1}, align, $V_{TG,align}$, for different combinations of t_{InAs} and t_{GaSb}. Observe how, for a chosen value of $V_{TG,align}$, the effective mass increase entails a certain relaxation of the size-induced confinement strength and this, in turn, allows to design structures with thinner InAs layers inside the channel. Once that we make an appropriate slab choice ensuring that the broken gap is closed at V_{TG}=0V, we start playing with the bias-induced contribution to confinement by applying increasing values of V_{TG} —within the targeted voltage range ($0<V_{TG}<V_{DD}$=0.2V)— that lower E_{e1} till the moment when alignment with E_{hh1} is attained.

Once the modified effective masses are taken into account, we depict in Fig. 3 the band profile along a vertical cut taken at the center of the channel for t_{InAs}=5nm and t_{GaSb}=4nm for V_{TG}=0 and V_{DS}=0.2V demonstrating the OFF state of the device thanks to the effective staggered gap induced by confinement. We have displayed in both cases the semiclassical edges of the conduction and valence bands to illustrate that in the absence of subband discretization, the switching ability of the device would be suppressed since BTBT would always be enabled due to the existing energy overlap between bands.

The resulting transfer characteristics shown in Fig. 4 feature very reduced SS values ranging between 6-8mV/dec over more than 6 decades of current.

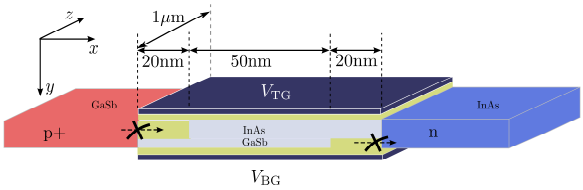

Figure 1. Schematic representation (not to scale) of the InAs/GaSb-EHBTFET. HfO_2 spacers inside the channel prevent the appearance of parasitic leakage tunneling.

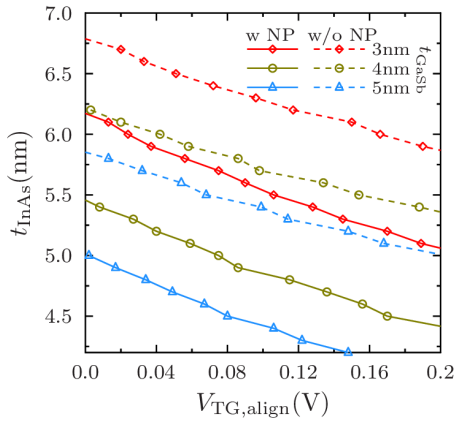

Figure 2. Impact of electron effective mass variation in the InAs layer (solid lines) on the top gate voltage at which first subbands align, $V_{TG,align}$, compared to the scenario with bulk masses (dashed lines).

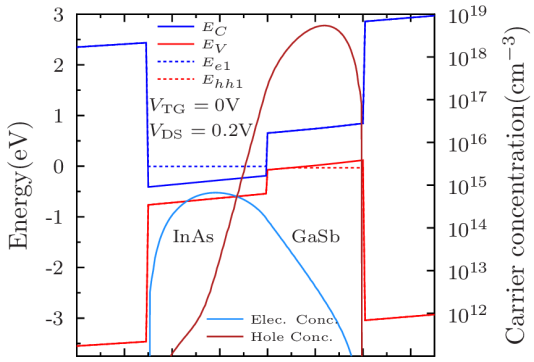

Figure 3. OFF-state band profile across a vertical cut at the center of the channel along with the corresponding quantized carrier concentrations.

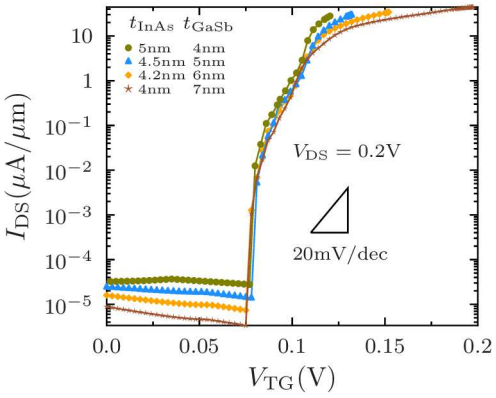

Figure 4. Transfer characteristics for the InAs/GaSb-EHBTFET with t_{GaSb}=4,5,6,7nm along with the adjusted InAs thickness so that $V_{TG,align}$≈0.08V.

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Hole mobility of cylindrical GaSb nanowires

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***Abstract*—The hole mobility of GaSb field-effect transistor nanowires is analyzed as a function of the device orientation and gate bias. To this purpose, a self-consistent Poisson-Schrödinger solver with an 8×8 k·p Hamiltonian is employed to study the electrostatics, and the hole mobility is calculated under the momentum relaxation time solution of the Boltzmann transport equation including the main high-field scattering mechanisms.**

Keywords- III-antimonides, GaSb, Hole mobility, k·p simulation, charge screening, phonons, surface roughness, III-V materials

I. INTRODUCTION

III-V materials constitute an interesting alternative to substitute or augment silicon CMOS technology in future high-speed and low-power logic applications. Indeed, nFETs with InGaAs channels outperforming silicon has already been successfully demonstrated and more recently, fully operative III-V CMOS devices have been experimentally proven. In spite of that, the investigation of the best III-V p-type complement to n-type InGaAs is still open. III-antimonides are revealing as promising contenders. Particularly, GaSb has exhibited high bulk hole mobility, and the fabrication of both, planar devices and nanowires has been recently achieved [1]. Previous works have focused on ultra-thin semiconductor-on-insulator GaSb devices, and analyzed theoretically their mobility as a function of orientation, size and/or strain conditions [2]. Nevertheless, despite their interest in the devices community, there is not a systematic work studying the hole mobility of GaSb nanowires (NWs), which is the main objective of this paper.

II. NUMERICAL METHOD

First, we calculate the electrostatics of long-channel GaSb nanowires solving an 8×8 k·p Hamiltonian self-consistently with the Poisson equation, as described in [3]. Arbitrary orientation is included in the simulations through the rotation of the corresponding Hamiltonian matrix. To evaluate the mobility, we solve the Boltzmann Transport Equation under the Momentum Relaxation Time approximation and make use of the Kubo-Greenwood approach, taking the most relevant scattering mechanisms into account: non-polar acoustic and optical phonons (ACPH, OPPH), polar optical phonons (POP) and surface roughness (SR) scattering. For ACPH and OPPH, the calculation of the scattering matrix is performed as described in Martínez-Blanque et al. [4], including the dependence of the wavefunction with the wavevector k. On the contrary, for POP and SR scattering mechanisms, the calculations are simplified considering the wavefunctions at $k=0$, in order to save computational burden. The evaluation of the SR scattering elements is performed as in [5], with Δ_{sr}=0.25nm and L_{sr}=1.5nm, whereas the numerical determination of the spatial integrals is performed employing the Fast-Fourier Transform as proposed by Stanojevic et al. [6]. Moreover, dielectric screening is included in the calculation of the SR scattering. So, we follow the approach by Jin et al. [7], considering only intra-subband interactions in the screening matrix. In this calculation, the wavefunctions at $k=0$ are taken into account.

III. RESULTS

We study the hole mobility in GaSb cylindrical nanowires oriented along [001], [011] and [111] crystallographic axis. As long-channel devices are considered, only the semiconductor radius (R_s=5nm) and the insulator thickness (T_{ins}) are needed to fully define the structure. Al_2O_3 is used as gate insulator, with T_{ins}=1.5nm. Figure 1 shows the mobility as a function of the carrier density P_i. The three channel orientations considered are included, and the total, SR-limited, and ACPH-limited mobilities specified. The behavior of POP and OPPH-limited mobilities follow that of ACPH but are less limiting and have therefore not been depicted. As can be observed, there is a considerable impact of the channel orientation on the mobility and, more importantly, quite different trends on the surface-roughness and the phonon-limited mobilities.

i) The [001]-oriented device attains the lowest phonon mobility. This behavior is related to the fact that [011] and [111]-oriented devices show a sharper band profile close to the valence band limit (see Fig. 2, where the band structure at V_G=-1V is represented).

ii) On the other hand, SR-limited mobility is much larger for the [001]-oriented nanowire than for [011] and [111] devices, in particular for high P_i values. To explain this trend, we have studied the charge distribution, which is critical to determine SR behavior. Figure 3 depicts the charge density for the three devices under consideration at V_G=-1V, which turns out to be strongly anisotropic. Thus, it is not easy to analyze the position of the charge, so we have depicted three slices of the charge distribution taken at different angles (Fig. 4), which reveal that the charge distribution is furthest from the semiconductor/insulator interface in the [001]-oriented device, diminishing the SR influence and therefore explaining the presented results.

iii) The effects of SR and phonons tend to balance at low carrier densities, and the three orientations result in mobilites close to $2x10^3$ $cm^2/eV{\cdot}s$. For higher bias (and carrier densities), SR becomes the dominant mechanism because of the charge redistribution in the nanowire, and large differences are observed amongst crystal orientations, with the [001] device mobility at least doubling those of [011] and [111] devices.

ACKNOWLEDGMENT

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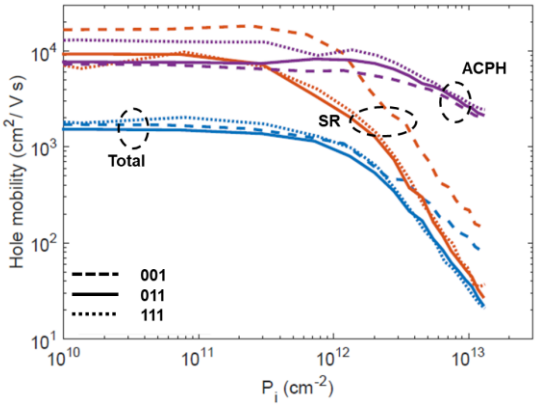

Figure 1. Total, ACPH and SR-limited mobility vs. P_i for [001], [011] and [111]-oriented GaSb NWs.

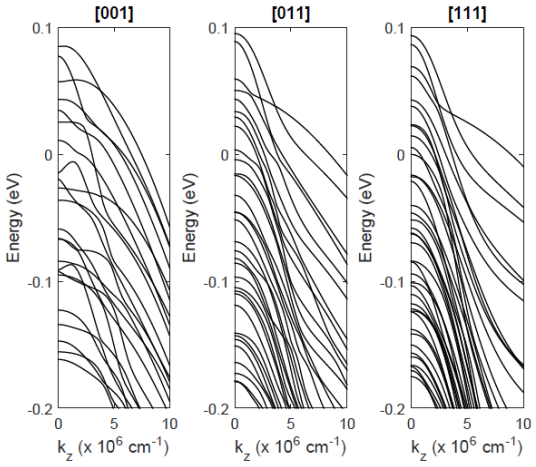

Figure 2. Band structure of R_S=5nm GaSb NWs with three different transport orientations at V_G = -1V.

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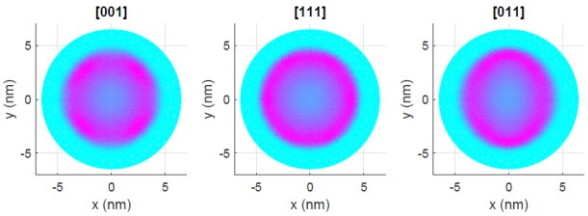

Figure 3. Hole density for the three orientations under consideration at V_G=-1V.

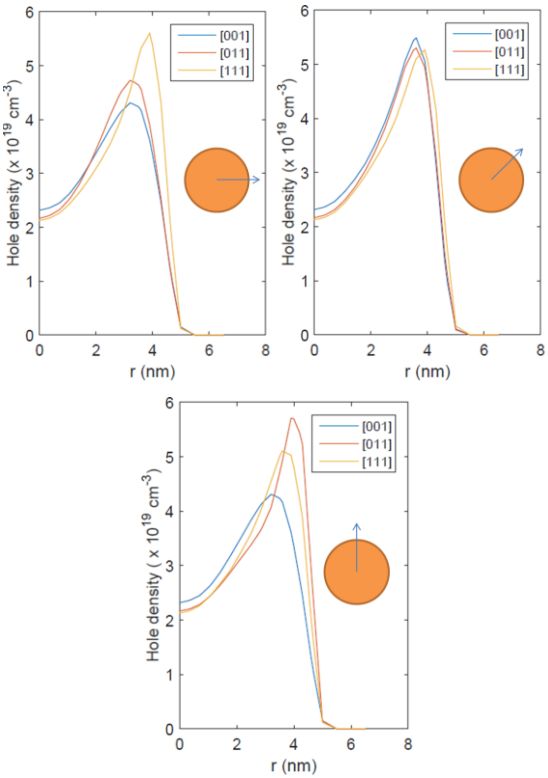

Figure 4. Hole density for different-oriented GaSb NWs at V_G = -1V (the directions for each slice are depicted in the insets, to account for anisotropic charge).

New method for self-heating estimation using only DC measurements

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***Abstract*—This paper reports a new method for estimating the thermal resistance of a device using the inverse of the transistor efficiency as a function of the power applied to the transistor's channel. The advantages of this new method are the use of DC measurements only and errors smaller than 4% in the estimation of the channel temperature increase due to the SHE when compared to a pulsed method for the UTBB SOI studied in this work.**

Keywords-Self-heating effect, Silicon-On-Insulator, UTBB

I. INTRODUCTION

Since the introduction of VLSI MOSFETs, the self-heating effect (SHE) has become significant to the characterization of devices at room temperature [1]-[2]. The area available for the heat to be dissipated is smaller due to the constant scaling, while the use of SOI technology adds a thermal barrier below the channel, resulting in a more significant heat accumulation in the devices, leading to ever-increasing temperatures. Currently, both Ultra-thin body and buried oxide (UTBB) and FinFET technologies suffer significantly with the effect, affecting their performance [3]-[4] and reliability [5]. However, currently no electrical techniques allow the extraction of the thermal resistance (R_{th}) without using dedicated structures or very specific test setups (e.g. the gate resistance requires a four-terminal gate, the pulsed I-V needs ultra-short pulses for scaled nodes, and the small signal RF relies on specialized RF test setups) [6]. Thus, in this paper it is proposed for the first time a new method that relies only on DC measurements for the evaluation of the SHE.

II. PROPOSED METHOD

Assuming the drain current (I_D) in saturation is given by

$$I_D = \mu_{eff}.C_{ox}.(W/L).(V_{GS}-V_t)^2/(2.n), \quad (1)$$

where μ_{eff} is the effective mobility, C_{ox} the gate oxide capacitance, W the channel width, L the channel length, V_{GS} the gate voltage, V_t the threshold voltage, and n the body factor; and the dependence of the mobility with temperature and vertical electric field is given by

$$\mu_{eff} = \mu_0.(T_0/T)^c/(1+\theta.V_{GT}), \quad (2)$$

where μ_0 is the low field, reference temperature mobility, T_0 is the reference temperature, T is the temperature of operation, c is the coefficient of the mobility degradation with temperature, θ is the mobility reduction factor due to the vertical electric field, and $V_{GT} = V_{GS} - V_t$ is the overdrive voltage.

From (1) and (2), one can demonstrate that the inverse of the transistor efficiency in saturation may be written as

$$I_D/g_m\,(P) = K.[1 + c.R_{th}.P/(R_{th}.P + T_0)], \quad (3)$$

where $g_m = \partial I_D/\partial V_{GS}$, $K = 1/V_{GT} + 1/[V_{GT}.(1+\theta.V_{GT})]$, $P = I_D.V_{DS}$, and V_{DS} is the drain voltage. Approximating (3) by a first order Taylor polynomial in P (around $P = P_0$ chosen to minimize the quadratic error) results in

$$I_D/g_m\,(P) \approx K.[1 + c.R_{th}.T_0.P/(R_{th}.P_0 + T_0)^2], \quad (4)$$

which allows R_{th} to be extracted from I_D/g_m if K and c are known. K may be directly estimated as being the independent term of the linear regression from I_D/g_m (P). Using (2) and assuming that $g_m \propto \mu$, the c-factor may be extracted in the saturation regime:

$$c = \log(g_m/g_{m0})/\log(T_0/T), \quad (5)$$

where g_{m0} and g_m are the transconductances measured for the same V_{GT}, at high V_{DS}, and at temperatures T_0 and T, respectively. However, T_0 and T are also affected by the SHE when such polarizations are employed, which makes an estimate of the c-factor using only the application of an external temperature unreliable. To solve this, an iterative approach is suggested to estimate both c and R_{th} simultaneously, as presented in Fig. 1.

III. DEVICES CHARACTERISTICS

An UTBB structure was employed, with equivalent oxide thickness of 1.2 nm, source and drain doping of 10^{20} cm^{-3}, lightly doped drain extension of 10 nm and concentration of 10^{17} cm^{-3}, buried oxide thickness (t_{BOX}) of 30 nm, silicon film thickness of 10 nm, channel width of 140 nm and lengths of 150 nm, 300 nm, and 500 nm. The devices were simulated using Sentaurus Device from Synopsys, and are presented in Fig. 2.

IV. RESULTS

To test the proposed method, the R_{th} values obtained for each L using the pulsed method described in [7] are used as a reference for comparison. Fig. 3, Fig. 4, and Fig. 5 show the estimation of the temperature in the channel of the self-heated devices at each power level by comparing I_D suffering with SHE at 300 K versus I_D without SHE at multiple temperatures. This estimation is summarized in Fig. 6, from which the thermal resistance for each L is

obtained as being the slope of the lines. I_D/g_m (P) is calculated using the I_D (V_{DS}) data with SHE from Fig. 3, Fig.4, and Fig. 5, and adding similar curves with 1.4 V < V_{GS} < 1.6 V. I_D (V_{GS}) was measured for temperatures between 300 K and 400 K to estimate the c-factor. Applying the proposed method, the R_{th} points presented in Fig. 7 were obtained. Finally, comparing the estimated temperatures obtained for each L when using both methods in Fig. 8, it becomes clear that the proposed method provides a good approximation even at the worst case, resulting in an error of 3.3%. Given such a low error, and considering that it requires only DC measurements while the pulsed method requires ultra-short pulses for scaled nodes (< 5 ns), this new method becomes a more applicable option.

V. CONCLUSIONS

A new method for obtaining R_{th} using I_D/g_m at room temperature and I_D (V_{GS}) at multiple temperatures was proposed. Using this method, it is possible to obtain an estimative of the channel temperature increase due to the SHE very similar to that obtained by the pulsed method, but using only DC measurements. When applied to the UTBB SOI, an increase of the channel temperature when L decreases is observed as expected, and comparing to the pulsed method an error lower than 4% was obtained in the worst case for the ranges studied.

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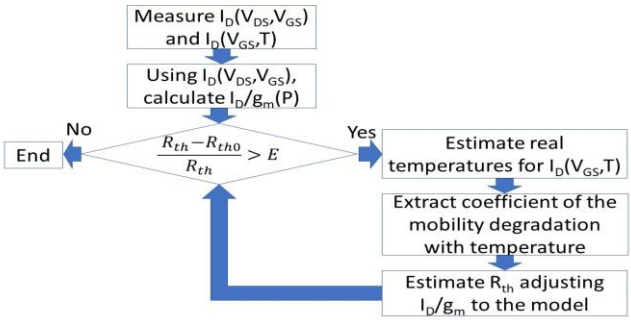

Figure 1 – Flowchart for the estimation of the thermal resistance using the proposed method

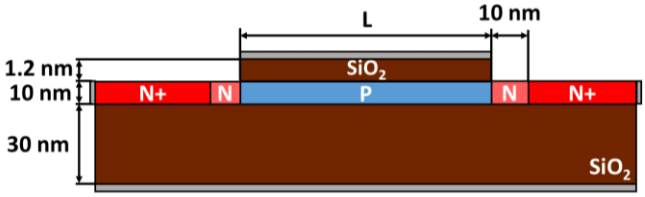

Figure 2 – Schematic view of the UTBB SOI MOSFET

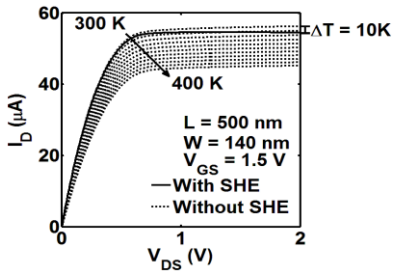

Figure 3 – Estimation of the channel temperature using pulsed measurements for L = 500 nm

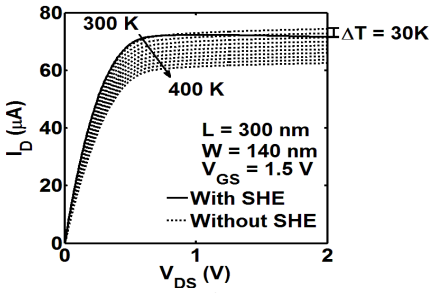

Figure 4 – Estimation of the channel temperature using pulsed measurements for L = 300 nm

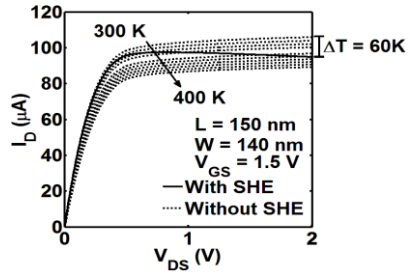

Figure 5 – Estimation of the channel temperature using pulsed measurements for L = 150 nm

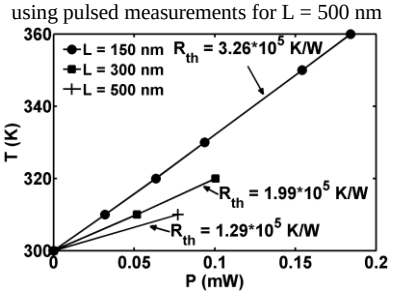

Figure 6 – Estimated temperature versus applied power to obtain the thermal resistance for each L

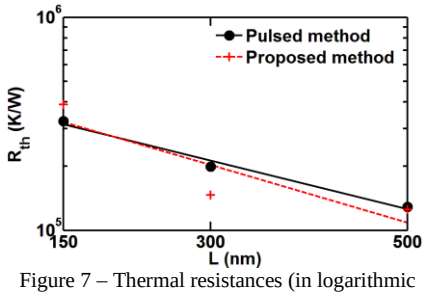

Figure 7 – Thermal resistances (in logarithmic scale) obtained through pulsed and proposed methods versus channel length

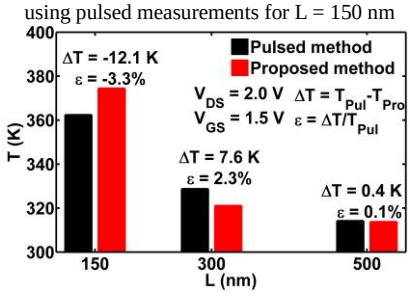

Figure 8 – Comparison of pulsed and proposed methods to estimate channel temperature

Profiling Border-Traps by TCAD analysis of Multifrequency CV-curves in Al_2O_3/InGaAs stacks

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***Abstract*— This paper reports physics based TCAD simulations of the multi-frequency C-V curves of InGaAs MOSCAPs including the AC response of border traps. The simulations reproduce the experimental inversion and accumulation capacitance vs frequency, and provide a way to profiling defect state density and energy at the high-k/III-V interface.**

Keywords—III-V compounds, TCAD simulation, border traps, parameter extraction, C-V

I. Introduction

Compared to the Si/SiO_2 material system, high-k dielectrics deposited on III-V semiconductors exhibit large interface and border trap (BT) values, which induce mobility degradation [1,2], Fermi-level-pinning [3,4] and 1/f noise [5]. Multi-frequency C-V measurements are highly sensitive to such traps and can be used to extract trap concentration profiles in energy and space [6,7,8]. This requires accurate models, most of which are already implemented in commercial TCAD tools (e.g. Sentaurus [9]), which include Fermi-Dirac statistics, a multi-valley band structure with non-parabolicity and quantum corrections via the modified local density approximation MLDA, [10]. Elastic and inelastic band to trap tunneling models can be used for the so called border traps [11,12].

In this paper we will show how with a suitable calibration, the model can reproduce the frequency dispersion of state-of-the-art Al_2O_3/InGaAs MOSCAPs.

II. Device and Model Calibration

The n-type InGaAs MOSCAP fabrication starts with a InP(100) substrate. A 2 µm n-$In_{0.53}Ga_{0.47}As$ layer was grown by MOVPE using a nominal Si doping concentration of 4×10^{17} cm^{-3}. The value measured by Electrochemical Capacitance-Voltage (ECV) varies between 4 and 6×10^{17} cm^{-3} across the layer. The Al_2O_3 dielectric (nominal thickness 8 nm) was grown by atomic layer deposition (ALD). TEM measurements indicate an actual thickness of 6 ± 0.3 nm. Ni(70 nm)/Au(90 nm) was used as the metal gate and was formed by electron beam evaporation and a lift-off process. MOS capacitors were treated by post-metal FGA using the optimum temperature of 450 °C.

Capacitance vs voltage curves have been measured between 1 kHz and 1 MHz using a E4980 LCR meter. The device area is large enough to allow neglecting gate edge effects.

For the simulations, ε_{ox} has been extracted using TCAD simulations; namely: assuming $N_D=4\times10^{17}$ cm^{-3} and varying ε_{ox} and T_{ox}. Under the assumption that traps do not respond to high-frequency C-V signal, we found a set of parameters (T_{ox}=6.3 nm and ε_{ox}=7) that matches the experimental minimum capacitance in inversion (C_{min}), see **Fig. 1**.

Carrier lifetime was calibrated to match the frequency position of the peaks in the G/ω and $-\omega\cdot dC/d\omega$ curves [13] in **Fig. 2**. This calibration also captures the experimental inversion capacitance vs frequency (**Fig. 3**, proving that the sample is genuinely inverted).

III. Results

Reproducing the frequency dispersion in accumulation requires determining the distribution of the BT (D_{BT}). To simplify the problem, some assumptions are made: 1) the energy distribution has a Gaussian shape, also reported in [1,2,6,]; 2) the spatial energy distribution has a Gaussian shape with its maximum at the high-k/III-V interface [14], 3) the tunneling mechanism of capture and emission is elastic.

Good agreement between experiments and simulations was achieved, see **Figs. 4** and **5**. The BT distribution is reported in **Fig. 6** and composed by: a Gaussian energy profile with its peak value of $5x10^{21}$ cm^{-3} eV^{-1}, centered at ~ 1.13 eV above the InGaAs conduction band and with a standard deviation of 0.33 eV with a Gaussian spatial profile with a standard deviation of 0.57 nm. It is worth saying that the position of the Fermi level in the experimental voltage range suggests that the distribution in energy is explored only up to ~ 0.4 eV above the InGaAs conduction band. Similar concentrations of border traps have been found with alternatives techniques [1,6,7,13].

Here we notice that AC simulations including interface traps are not reliable when one employs the MLDA model: the electrons are set back from the high-k/III-V interface so that the concentration at the interface vanishes. Because the calculation of interface traps emission rate is local and relies on the carrier concentration at the interface, the emission rates become unphysically small. We plan to use BTs with inelastic tunneling to improve the matching in this region.

IV. Conclusions

In this paper, we used extensive TCAD simulations to analyze the frequency dispersion of C-V curves for advanced InGaAs/Al_2O_3 MOSCAP. Through the simulations, we understood and demonstrated the inversion of the device and we were able to characterize the distribution and the volume of the border traps.

ACKNOWLEDGMENTS

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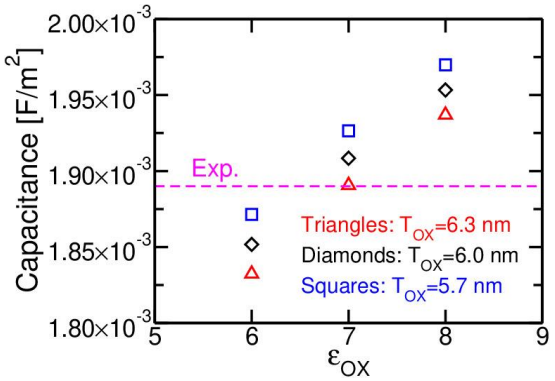

Fig. 1. Simulated Cmin values (at 1 MHz and V_G=-3 V) using N_D=4·10^{17} cm^{-3} and changing T_{ox} and ε_{ox}. T_{ox} is varied inside the confidence interval find by TEM (6 ± 0.3 nm). The experimental value of Cmin is reported with the dashed line.

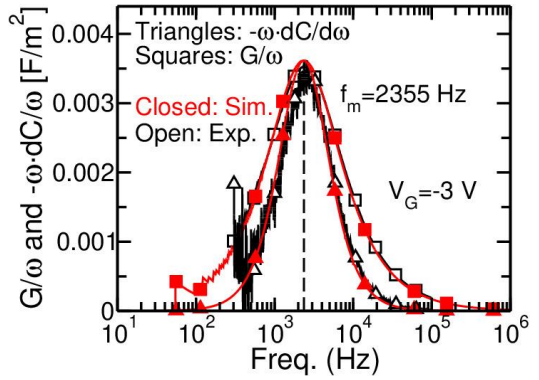

Fig. 2. Experimental (open symbols) and simulated (closed symbols) curves of G/ω and -ω·dC/dω plotted as a function of frequency (ω is the angular frequency). The transition frequency is reproduced using a carrier life time of ~ 92 ps.

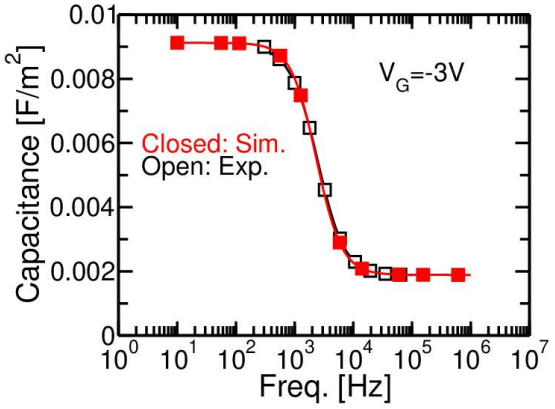

Fig. 3. Experimental (open symbols) and simulated (closed symbols) curves of the inversion capacitance (extracted at V_G=-3 V) as a function of frequency.

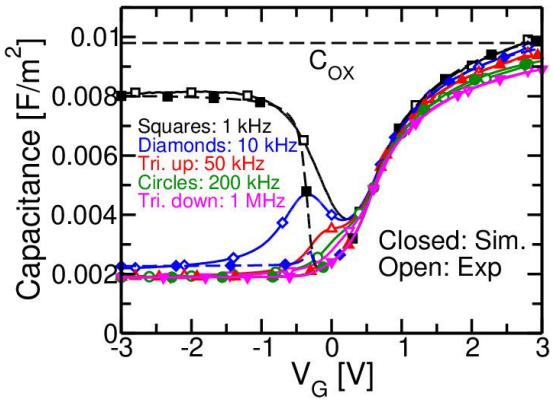

Fig. 4. CV characteristics measured (open symbols) and simulated (closed symbols) including border traps at 300K. Negligible leakage current is observed during the measurements.

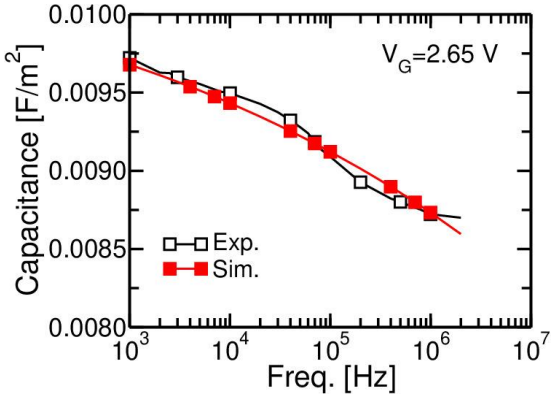

Fig. 5. Experimental (open symbols) and simulated (closed symbols) curves of the accumulation capacitance (extracted at V_G=-2.65 V) as a function of frequency.

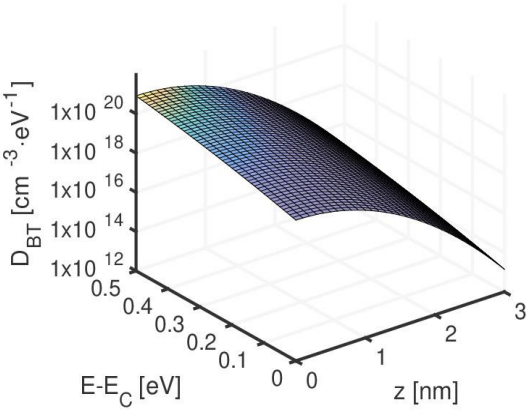

Fig. 6. Border traps distribution in energy and space. The energy axis is referred to the InGaAs conduction band and is limited within the range explored in experiments. z is the distance of BT from the high-k/III-V interface.

MS-EMC *vs*. NEGF: A Comparative Study Accounting for Transport Quantum Corrections

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***Abstract*—As electronic devices approach the nanometer scale, quantum transport theories have been recognized as the best option to reproduce their performance. Other possible trend, mainly focused on reducing the computational effort, is the inclusion of quantum effects in semi-classical simulators. This work presents a comparison between a NEGF simulator and a MS-EMC tool including S/D tunneling both applied on a DGSOI transistor.**

Keywords-Multi-Subband Ensemble Monte Carlo; Non-Equilibrium Green Function; direct Source-to-Drain tunneling; quantum effects; DGSOI

I. INTRODUCTION

Short-channel effects (SCEs) degrade the performance of conventional devices as the dimensions are scaled down. From a modeling point of view, it is mandatory to include of quantum transport phenomena not relevant in previous technological nodes [1] in order to explain the electrical behavior of aggressively scaled nanodevices. In particular, Source-to-Drain tunneling (S/D tunneling) allows electrons to tunnel from the source to the drain through the narrow potential barrier, eroding the gate control. However, this phenomenon cannot be straightforward included in semiclassical transport models. Multi-Subband Ensemble Monte Carlo (MS-EMC) simulators provide a detailed description of quantum effects in confinement directions and their impact on scattering but, due to the semi-classical MC transport framework, the tunneling phenomena have to be included in a separate way. In this work, S/D tunneling has been implemented in a MS-EMC simulator and compared to ballistic Non-Equilibrium Green's Function results which consider implicitly tunneling in order to assess the MS-EMC implementation.

II. METHODOLOGY

The simulation framework is based on a MS-EMC code with already demonstrated capabilities in different scenarios [2-3]. The tool, based on the mode-space approach of quantum transport, solves the Schrödinger equation in the confinement direction, and the Boltzmann Transport Equation (BTE) in the transport plane (Fig. 1). The system is coupled by solving Poisson equation in the whole simulation domain. The additional modules needed for taking into account the tunneling are included as separated transport mechanisms and can be activated or not depending on the simulation scenario. S/D tunneling [4] and gate tunneling [5] are implemented as stochastic mechanisms evaluated for each superparticle at the end of Monte Carlo free flight. The transmission coefficients are calculated using the WKB approximation. Band-to-Band tunneling can be also considered as described in [6]. In order to assess the accuracy of including quantum transport in this way, the simulation results will be compared to those obtained with NanoMOS [7], a NEGF simulator that considers ballistic transport in an effective mass approximation. In this way, our simulation frame will only consider ballistic transport and S/D tunneling with two approaches: instantaneous tunneling (IT) which does not consider charge under the barrier and ballistic tunneling (BT) where particles drift in the barrier region as described in [4].

III. RESULTS

Fig. 1 shows the double gate structure and device parameters herein analyzed. The Si thickness is 5nm, and abrupt doping profiles in the S/D-channel junctions have been considered. The I_D-V_G characteristics for a 10nm channel length transistor are shown in Fig. 2. A perfect agreement is observed in the ON region whereas the subthreshold region presents some differences. It is interesting to highlight the importance of the tunneling model. When IT is considered, there is a small difference with the simulations that do not take tunneling into account. However, the inclusion of BT degrades the subthreshold characteristics approaching closely the NEGF results. In the BT the electrons inside the barrier change the subband profile, approaching its value to those obtained in NEGF simulations as shown in Fig. 3. In the IT, there is no extra charge in the channel region; therefore, the subband profile stays unaltered. Despite the higher barrier, which prevents thermionic emission in the case of NEGF and BT, the high electron concentration near the tunneling region (X=-4nm in Fig. 4) enhances the S/D tunneling with the aforementioned degradation of the subthreshold behavior. Therefore, further device optimization is demanded reduce these phenomena for sub-10nm nodes.

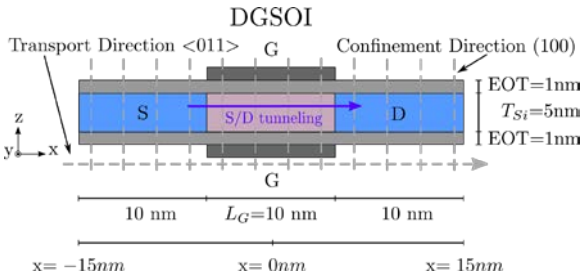

Figure 1. DGSOI structure analyzed in this work with L_G=10nm and T_{Si}=5nm. 1D Schrödinger equation is solved for each grid point in the transport direction and BTE is solved by the MC method in the transport plane.

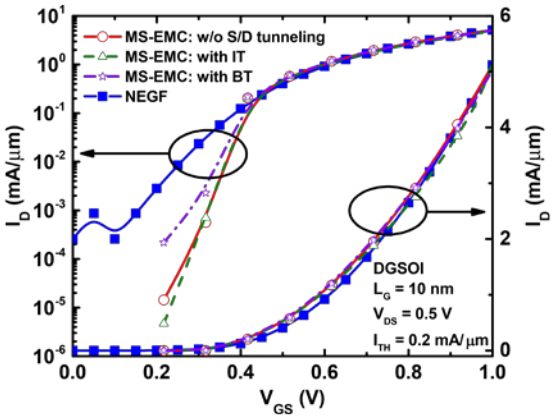

Figure 2. I_D vs. V_{GS} in the 10nm DGSOI device at V_{DS}=0.5V for the NEGF tool as well as the MS-EMC considering a simulation w/o S/D tunneling and both the instantaneous and the ballistic S/D tunneling models.

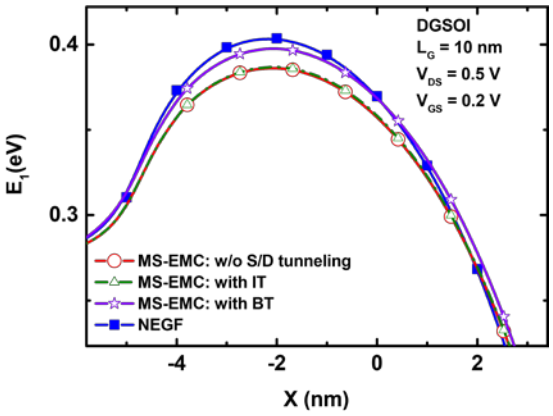

Figure 3. Energy profile of the lowest energy subband in the 10nm DGSOI device at V_{DS}=0.5V for the NEGF tool as well as the MS-EMC considering a simulation w/o S/D tunneling and both the instantaneous and the ballistic S/D tunneling models. V_{GS} = 0.2V and V_{DS} = 0.5V.

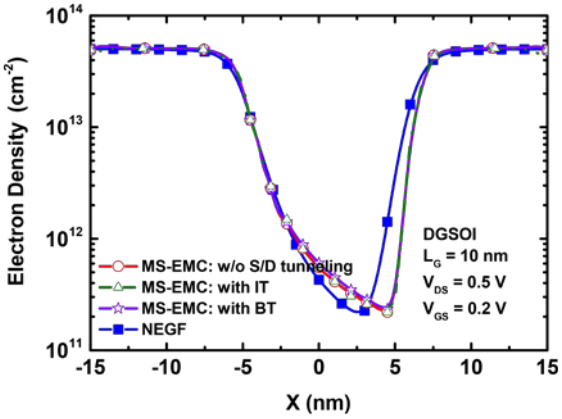

Figure 4. Electron distribution in the 10nm DGSOI device at V_{DS}=0.5V for the NEGF tool as well as the MS-EMC considering a simulation w/o S/D tunneling and both the instantaneous and the ballistic S/D tunneling models. V_{GS} = 0.2V and V_{DS} = 0.5V.

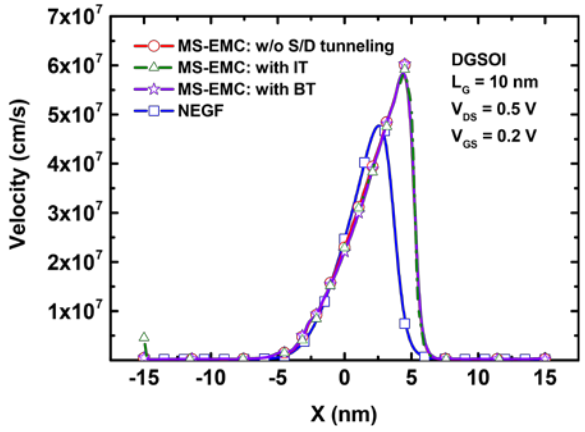

Figure 5. Average velocity in the direction normal to the interfac (v_x) in the 10nm DGSOI device at V_{DS}=0.5V for the NEGF tool as well as the MS-EMC considering a simulation w/o S/D tunneling and both the instantaneous and the ballistic S/D tunneling models. V_{GS} = 0.2V and V_{DS} = 0.5V.

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Switching Current Reduction in Advanced Spin-Orbit Torque MRAM

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***Abstract*—Several paths to reduce the switching current by spin-orbit torques in an in-plane MRAM structure are analyzed. The switching by two orthogonal current pulses complemented with an interface-induced perpendicular magnetic anisotropy allows reducing the switching current and to achieve sub-500ps switching.**

Keywords-Spin-orbit torque; MRAM; switching; perpendicural magnetic anisotropy

I. INTRODUCTION

Magnetoresistive random access memory (MRAM) based on spin-transfer torque (STT) switching possesses several important advantages: non-volatility, purely electric operation, long retention time, infinite endurance, and the capability to operate in harsh environments. It is also fast compared to other types of non-volatile memories: flash and phase change memory cannot operate at 10ns speed. This speed is sufficient to replace the main computer memory – DRAM. However, to compete with SRAM in the caches of hierarchical multi-level processor memory the switching must be further accelerated down to the sub-ns regime [1]. Spin-orbit torque (SOT) based MRAM is an electrically addressable non-volatile memory combining high speed and high endurance and is thus suitable for applications in caches [2]. Although the high switching current is not flowing through a magnetic tunnel junction but rather through a heavy metal line under it, the currents are still high, and their reduction is the pressing issue in the field of SOT MRAM development.

II. METHOD AND RESULTS

The investigated memory cell is shown in Fig.1. It consists of an in-plane magnetized MTJ with its free layer lying on top of the heavy metal Line 1 of 3nm thickness. The dimensions of the free layer are $52.5\times12.5\times2\text{nm}^3$. Another heavy metal Line 2 with an overlap NM2 from the right side less or equal to the total free layer width 52.5nm serves to apply the second perpendicular current pulse and the spin-orbit torque associated with it. In this case only the current pulse through Line 2 with the complete overlap NM2=52.5nm is applied, the magnetization can be switched deterministically without an external magnetic field [3], provided the pulse is sufficiently long and the current is high enough. Switching by the current through Line 1 alone is not possible unless an external magnetic field is applied to break the mirror symmetry [4]. The torque due to the pulse through Line 2 switches the magnetization deterministically; however, the current is large. The reduction of the current by simply reducing the overlap NM2<52.5nm results in a smaller area where the torque is active and a longer switching time (Fig.2). This can be compensated by a larger current running through Line 2, as seen in Fig.3; however, this results in an unwanted current density increase. Next, we apply the current pulse through Line 1 just before the second pulse through Line 2 [5]. We assume equivalent pulses of 200ps duration. The first pulse through Line 1 creates an initial deviation of the magnetization from its equilibrium direction along the OX axis. This makes the torque from the second pulse efficient from the beginning thus removing the incubation period. The two-pulse scheme allows reducing the switching current by a factor of 3 as compared to single pulse switching of a similar duration. Fig.4 demonstrates that the optimal width NM2 of Line 2 is around 12.5 nm as its further reduction results in a high current density.

To further decrease the switching current, a perpendicular magnetic field typically developed at the MgO/CoFeB interface is introduced [6]. The perpendicular anisotropy compensates the large demagnetizing contribution when the magnetization is out of plane. However, the perpendicular anisotropy may compromise the temperature stability of the in-plane structure, when its value K_1 is too large. Fig.5 shows the time evolution of the magnetization projection on the direction OZ perpendicular to the structure, for several K_1, while Fig.6 displays a typical dependence of the in-plane magnetization along the easy axis.

In conclusion, the introduction of the perpendicular anisotropy K_1 into the two-pulse switching scheme allows reducing the switching current from 180μA to 30μA, while achieving fast sub-0.5ns writing suitable for cache applications.

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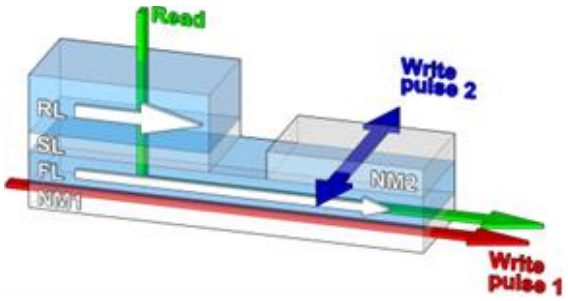

Figure 1. Schematic of the in-plane SOT MRAM cell. The free layer of an MTJ is grown above the heavy metal Line 1, through which the current pulse is applied. Line 2 serves to conduct the perpendicular current Write pulse 2.

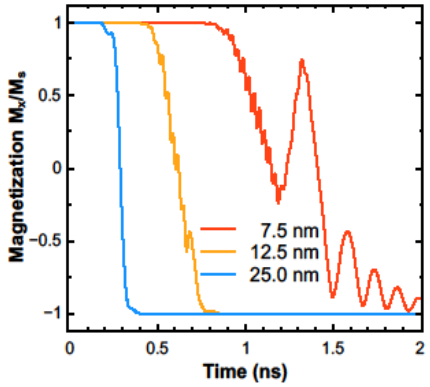

Figure 2. Time dependent magnetization evolution for several values of the second wire NM2 overlap. The current is scaled with NM2 and is equal to 180μA for NM2=25nm, 90μA for NM2=12.5nm, and 54μA for NM2=7.5nm.

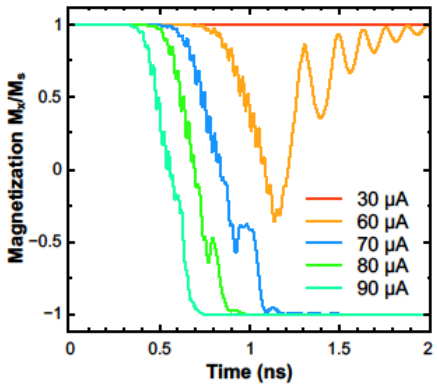

Figure 3. Time evolution of the magnetization for several values of the current through Line 2 with NM2=12.5nm. The current through Line 1 is zero.

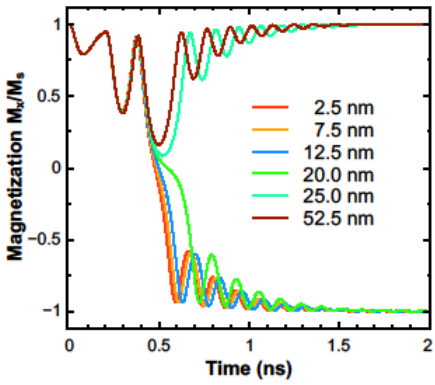

Figure 4. The magnetization dynamics for several overlap lengths NM2. Two consecutive perpendicular pulses with 30μA current and 200ps duration are applied.

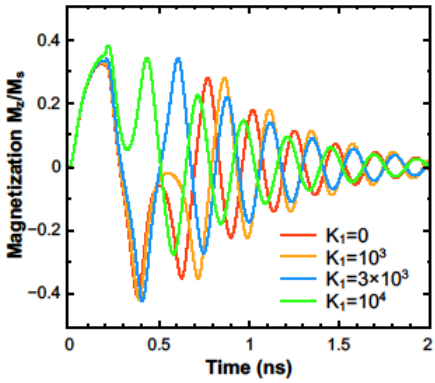

Figure 5. Time dependence of the magnetization projection on the perpendicular OZ axis, for several values of the interface-induced perpendicular anisotropy.

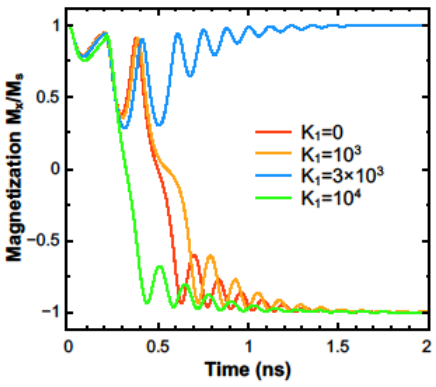

Figure 6. Adding perpendicular magnetization if a two-pulse scheme allows to reduce the current by a factor of 6 for sub-0.5ns switching.

Finite Element Simulation of 2D Percolating Silicon-Nanonet Field-Effect Transistor

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***Abstract*—Percolating networks of silicon nanowires, also called nanonets, have been proposed as a possible material for the channel of Field-Effect Transistors. Experimental results have shown that the dependence of current-voltage characteristics with parameters such as device dimension and nanowire density might be influenced by the statistical dispersion of individual nanowires threshold voltage. In order to further analyse this effect, this paper provides a finite element simulation of such nanonet-based field-effect transistor. We studied the influence on transistor characteristics of above-mentioned parameters. Simulation results were compared with experimental ones using the same parameter extraction methodology as in experiments.**

Nanonet; Finite Element Simulation; Random network; Lambert Function; Threshold Voltage Dispersion

I. INTRODUCTION

A silicon nanonet (Si NN) is a random network of Si nanowires (NWs). It can be obtained with low cost fabrication techniques [1] and can be transferred on any kind of substrates [2]. It is thus a good candidate for potential 3D integration above a CMOS wafer. Moreover, being made of NWs, NNs are expected to be highly sensitive to changes in their surface charge [3]. Because of these different properties, Si-NNs are a promising building block for the integration of low cost, sensitive, label free sensors. However, the randomness of the networks introduces some complications in the analysis of such devices. Several simulation studies have been published. Although they use different approaches, the NN-FET simulations that have been proposed so far are usually making simplifying assumptions. Many of them, especially those based on percolation theory, do not account for gate control.[4,5] Due to the complexity of the network, the calculation is often reduced to that of the most effective conduction paths, for instance with the use of Dijkstra algorithm.[6] Moreover, to the best of our knowledge, threshold voltage dispersion in the nanowire population used in the nanonet has never been accounted for, while experiments show that this dispersion can be very large.[7] In this paper, we simulated Si-NN FETs with a 2D finite element algorithm which takes into account threshold voltage dispersion of individual nanowires, and we analysed the impact on electrical properties of channel length and density of nanowires. For simplicity, individual NWs were assumed to have fixed physical length L_{NW}, although this is not necessarily the case for real experiments, and NW-NW junction resistance was not yet taken into account.

II. FINITE ELEMENT SIMULATION

In this simulation, 2D Si-NNs (with a finite size defined by channel length L and channel width W) were realized by randomly generating a number N_{NW} of nanowires defined by the position of their centre (2D coordinates x_{0i} and y_{0i}) and their angle (θ_i) to horizontal axis (along source-drain direction). The threshold voltage V_{ti} of individual nanowires was randomly generated, following a normal distribution with mean value V_{t0} and standard deviation σ_{Vt} (Fig.1). Drain voltage was assumed to be small, so that individual nanowires were operating in the linear regime, each with a uniform charge Q_i which depends on gate voltage V_g. To describe this dependence, we used the Lambert $\mathcal{W}$-function (Eq. 1), which has the advantage of providing a continuous description from below threshold to strong inversion and has been proved to provide good fit to experiments with a reduced number of parameters [7]:

$$Q_i(V_g)=C_{ox}\, n_i \frac{kT}{q}\, \mathcal{LW}\left(\exp\left(q\frac{V_g-V_{ti}}{n_i kT}\right)\right) \qquad \text{(Eq. 1)}$$

where C_{ox} is the gate capacitance, T is the temperature, k the Boltzmann constant, q the electron charge, V_{ti} the threshold voltage and n_i the subthreshold slope ideality factor for an individual NW. Source and drain contact regions of width W and length 0.5×L were positioned on each side of the nanonet. In these regions, we assumed a very large conductivity compared to that of silicon. Electric potential was fixed at 0V on the source (left-hand side) and equal to drain voltage V_d, (here equal to 50 mV) on the drain (right-hand side). In order to prevent computation errors in the case where random generation results in no connecting paths between source and drain, a highly resistive domain was added between the two contacts. For each value of gate voltage, the Finite Element Method (FEM) was used to solve Poisson's equation with Eq. 1 above, from which we deduce the distribution of current density in the considered 2D system (Fig.2), and, finally, drain current I_d. As an example, Fig. 3 plots the gate characteristic I_d-V_g obtained for the system of Fig. 1. Because of the random aspect of the problem, a large number of NWs arrangements must be generated for each set of parameters (density of NW and channel length), in order to get an order of magnitude of statistical variability.

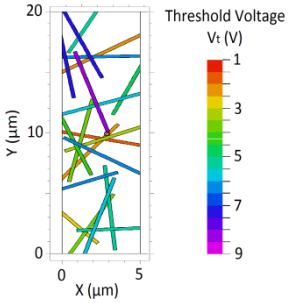

Figure 1. Threshold Voltage as a function of position for a Nanonet generated with W = 20µm, L = 5µm, L_{NW} = 7µm, N_{NW} = 20, V_{t0} = 5V, σ_{Vt} = 2V, n_i = 10.

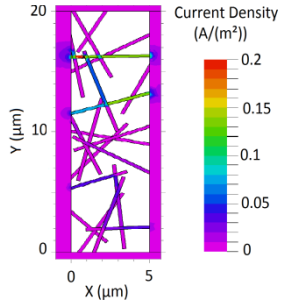

Figure 2. Current Density as a function of position for the configuration of Fig.1. Due to V_t dispersion, percolating paths are not necessarily shortest paths.

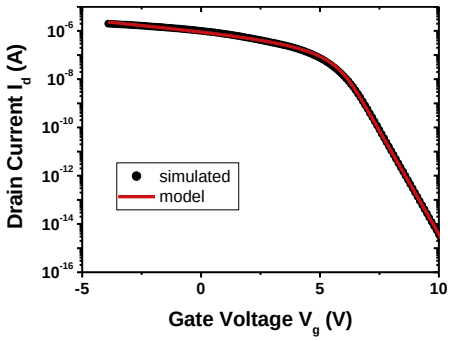

Figure 3. Gate Characteristic for the configuration shown in Fig.1 (black points). This characteristic can be fitted with a Lambert $\mathcal{W}$–function based model (red) to extract main electrical parameters (μ_0 = 26.6 $cm^2.V^{-1}.s^{-1}$, V_t = 5.8 V, n = 10)

III. Discussion

Like in experiments, the main electrical parameters such as low field mobility μ_0, subthreshold slope ideality factor n, threshold voltage V_t and first order mobility attenuation factor θ_1, were extracted by fitting the simulated Id-Vg curves with a (now global) Lambert $\mathcal{W}$-function.[7] W and L were used in place of the physical, but unknown, channel width and length. This method thus provides *effective* values, however suitable for compact modelling. Figs. 4-5 are plotting n and V_t versus σ_{Vt}, for 4 different values of nanowire density, and a short channel (channel length L smaller than L_{NW}). Simulation shows that the ideality factor increases with NW density, if $\sigma_{Vt} \neq 0V$, which is the trend observed experimentally for short L.[7] An increase of Vt was found with increasing σ_{Vt}. This result can be explained by the fact that, in the short channel case, conduction is driven by the NW of highest threshold voltage that links source and drain (in the case of p-type NW). Additional simulation results, showing for instance the influence of channel length, will be included in the 4 pages abstract.

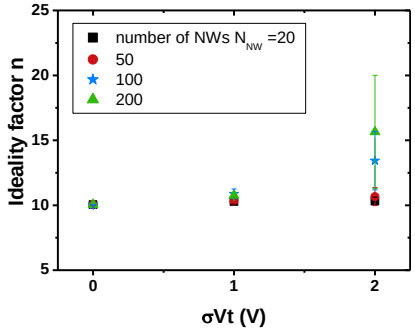

Figure 4. Extracted ideality factor n as a function of individual nanowires threshold voltage standard deviation σ_{Vt} for 4 values of NW densities (W = 200µm, L = 5µm, L_{NW} = 7µm, V_{t0} = 5V, n_i = 10)

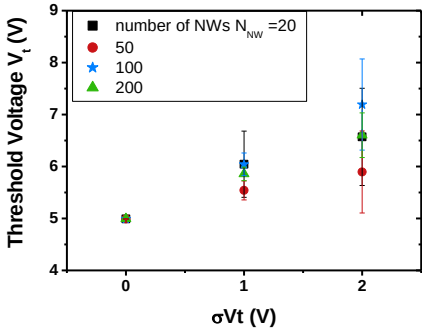

Figure 5. Extracted threshold voltage V_t as a function of individual nanowires threshold voltage standard deviation σ_{Vt} for 4 values of NW densities (W = 200µm, L = 5µm, L_{NW} = 7µm, V_{t0} = 5V, n_i = 10)

I. Conclusions

We developed a Finite Element model of NN-based Field-Effect transistor which accounts for nanowire dispersion in the calculation of the current-voltage characteristics. Simulation results are consistent with experimental trends. This model can be further used to analyse NN-FET biosensors operation.

Acknowledgment

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Investigation on built-in BJT in FD-SOI BIMOS

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***Abstract*— The built-in BJT of a BIMOS fabricated in 28nm UTBB FD-SOI high-k metal technology is investigated in common-emitter mode and in MOSFET off-state. In the weak V_{BE} regime, field-effects dominate, generating a negative base current and making the current gain β_0 meaningless. For V_{BE} high enough, the BJT works normally but with and very low gain.**

Keywords: BIMOS, body-contacted, MOSFET, FD-SOI

I. Introduction

BIMOS has previously been studied in bulk technology [1] and proposed as an ESD protection device [2]. Afterwards, it has been investigated in Hybrid-bulk [3], [4] and, recently in FD-SOI [5], [6]. In [7], the latter has been characterized in Hybrid common-base mode featuring a tremendous "apparent gain" of 10^7. However, this gain is ambiguous as the voltage set-up prevented the MOSFET and the BJT contributions to be distinguished. In order to clear this ambiguity, we assessed the real common-emitter current gain β_0 in built-in MOSFET off-state mode. It relies on Gummel plot measurements with the collector-emitter potential V_{CE} and the gate-emitter potential V_{FGE} as parameters at room temperature. Different current contributions are analyzed and identified.

II. Device Structure and Fabrication

The FD-SOI BIMOS is a body-contacted FD-SOI N-MOSFET featuring 5 terminals: front gate (FG), back gate (BG) and emitter-base-collector (E-B-C) or source-body-drain (S-B-D) depending on whether BJT or MOSFET point of view is adopted (Fig. 1). In our device, the body/base contact is achieved using a T-shape gate that separates the P^+-doped and the two N^+-doped areas. It is fabricated in 28nm UTBB FD-SOI STMicroelectronics technology featuring an ultra-thin silicon film of 7 nm, an ultra-thin BOX of 25 nm and a high-k metal gate stack. Selected options were extended gate (EG) with an EOT of 3.4 nm and p-type well (ground plane) under the BOX. Dimensions are given in table I.

TABLE I. Device dmensions

L	W	L_D	W_D
135 nm	270 nm	144 nm	351 nm

III. Measurements and Results

DC measurements of collector current I_C, emitter current I_E and base current I_B versus the base-emitter potential $V_{BE} \geq 0$ are performed, in common-emitter mode ($V_E = 0$), using an HP 4156C prober. In a first experiment, V_{CE} is taken as parameter, and front and back gates are grounded. Two regimes are observed in Fig. 2. Firstly, for V_{BE} high enough, the BJT behaves normally – defining the *normal* regime (NR). The current-voltage characteristic is split in an exponential and a linear region. It is worth noticing that $I_B > I_C$. Secondly, for weak V_{BE} the BJT behaves abnormally – defining the *abnormal* regime (AR). A current independent of V_{BE} flows from the collector to the base and increases V_{CE}. I_E remains constant regardless of collector or base potential. The corresponding common-emitter current gain β_0 (Fig. 3) is defined as:

$$\beta_0 = (I_C - I_{CEO}) / I_B \quad (1)$$

with $I_{CEO} \equiv I_C$ when the base is short (inset in Fig. 3). In a second experiment, V_{FGE} is taken as a parameter, the back-gate is grounded and V_{CE} is set to 1.8V (Fig 4). The same two regimes are observed. In the NR, decreasing V_{FGE} solely affects the linear region by slightly increasing I_C and I_B. In the AR, it increases the collector-to-base current and decreases I_C

IV. Discussion

In the AR, β_0 is meaningless as I_B is negative and not modulated by V_{BE}. Its positive sign is due to $I_C < I_{CEO}$ and its high amplitude, reaching up to 400, relies on I_B sign change. Hence both are mathematical artefacts. Furthermore, currents are driven by field-effects mechanism. The gate-induced drain leakage mechanism is identified as the collector-to-base current driver. Indeed, it increases with the collector-gate potential V_{CFG} in both experiments and it is compliant with the current path [8]. At the emitter side, I_E is identified as a current of electrons. Their injection into the channel is modulated by V_{FGE} as in classical off-state N-MOSFET. In the NR, β_0 is positive and meaningful but smaller than unity. This poor performance can be explained by non-optimized doping-profiles and absence of neutral region in the FD-SOI channel. The hole injection at the base side is modulated by the gate-base potential V_{FGB} and V_{BE} as in classical on-state P-MOSFET.

V. Conclusion

The built-in BJT of the studied FD-SOI BIMOS has been characterized in common-emitter mode. It features a weak $\beta_0 < 1$ in its exponential and linear regimes. An abnormal regime has been identified where $I_B < 0$ and β_0 is meaningless. In this regime, field effects dominate and the base acts as an attractor for holes generated in the devices. This analysis paves the way to relevant compact

modeling of the device for further application as analog neuromorphic circuit.

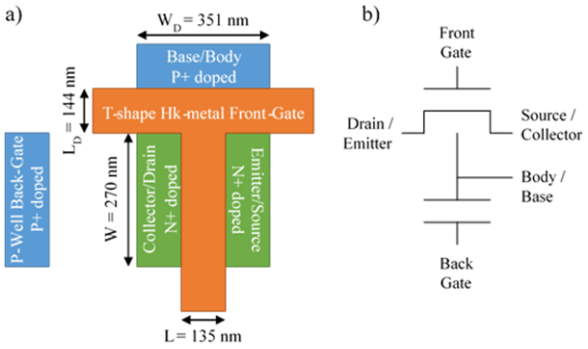

Figure 1. FD-SOI BIMOS layout (a) and schematic (b)

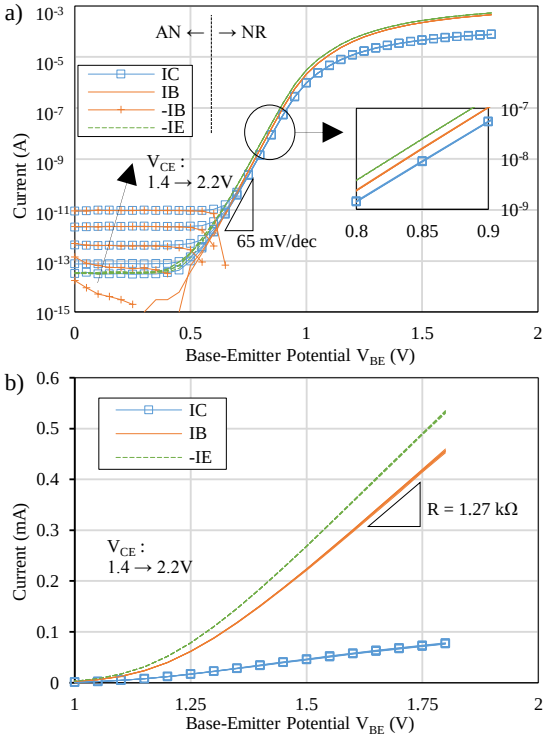

Figure 2. Emitter, base and collector currents versus base potential in semilogarithmic (a) and linear (b) scales, for V_{FGE} =V_{BGE} = 0 V and V_{CE} from 1.4 to 2.2 V.

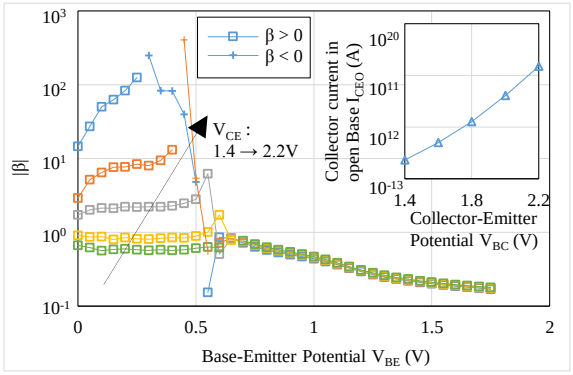

Figure 3. Common Emitter Gain β_0.

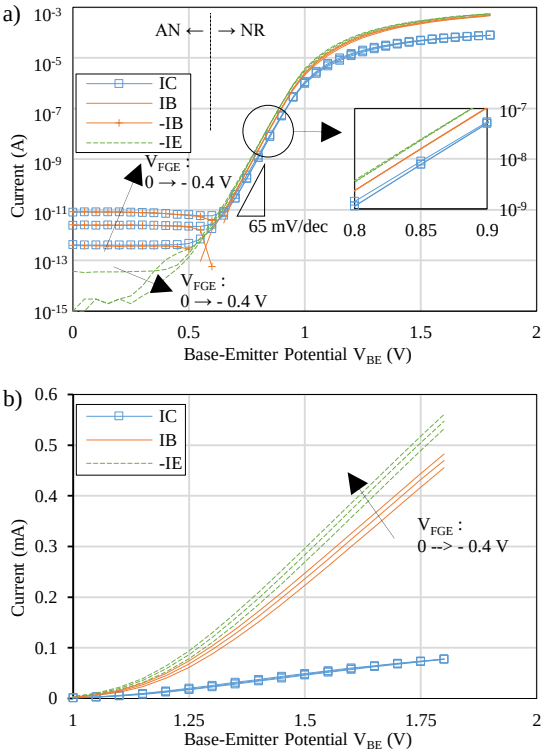

Figure 4. Emitter, base and collector currents versus base potential in semilogarithmic (a) and linear (b) scales, for V_{CE} = 1.8V, V_{BGE} = 0 V and V_{FGE} from 0 to -0.4 V.

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Simulation and Automated Characterisation of Optimal Load for Flexible Composite Generators Based on Piezoelectric ZnO Nanowires

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***Abstract*— This paper reports the experimental and numerical study of flexible piezoelectric transducers made of a thin active composite material (~3 µm thick) over a thin flexible metallic foil (~25 µm of stainless steel). The active piezo-layer consists of vertical ZnO nanowires (NWs) embedded into dielectric fillers of different composition. The voltage over a known resistance was measured with an automatic bending setup, and the corresponding power was computed and compared to numerical simulations as a function of load resistance and dielectric matrix in the composite structure. FEM simulations show that the output power can be higher than conventional thin-film devices. These results confirm previous findings and provide important guidelines to optimize flexible piezoelectric transducers for applications as sensors and generators for the Internet of Things. Comparison with a commercial thick-film piezoelectric energy harvester was also made experimentally.**

Keywords-ZnO nanowires; piezoelectricity; mechanical energy transducer; FEM simulation

I. INTRODUCTION

Thin lightweight flexible mechanical energy harvesters can find multiple applications in autonomous devices for the Internet of Things (IoT) scenario. In particular, since the first demonstration of energy generated by deflecting a single ZnO nanowire (NW) [1], piezoelectric energy transducers and nanogenerators (NGs) have attracted increasing attention [2,5]. In this context, we compare one such transducer to a commercial thick-film (100 µm) device in order to estimate the potential of NW-based NGs. We also report a numerical study on such energy harvesters [4] integrating vertical semiconducting nanowires into a dielectric matrix on a flexible substrate (Fig. 1). *Three innovative aspects of this paper are: 1) simulations that couple the piezoelectric NGs to a resistive load and allow us to assess numerically the power generation capabilities of the technology; 2) a dedicated test bench for the automatic characterization of real devices; 3) the benchmarking of NW-based NGs against a commercial flexible device.*

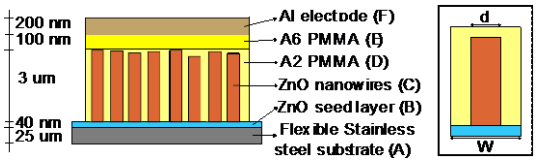

Figure 1. Schematic (out of scale) diagram of the flexible energy transducer of this work, integrating piezoelectric ZnO NWs in a dielectric matrix. The inset shows the section of a single-NW cell.

II. NUMERICAL SIMULATIONS

The simulations are based on 2D and 3D FEM models reported in [4]. The 2D model of the bending plate (substrate and active layer) is used to calculate the strain in the active layer of the transducer upon bending. With respect to previous works [4], we take into account more realistic non-linear mechanics. The calculated strain is then input to a more elaborate 3D model of a unit cell containing only one NW immersed in the dielectric with seed layer and top electrode, inset of Fig.1. The NW length and diameter are consistent with measurements (see Section III). The cell width is adjusted to obtain a NW diameter over cell width ratio, r = d/W [4], ranging from 0.1 to 0.9, as to represent various densities of NWs on the NG when d = 300 nm is fixed. Previous results only

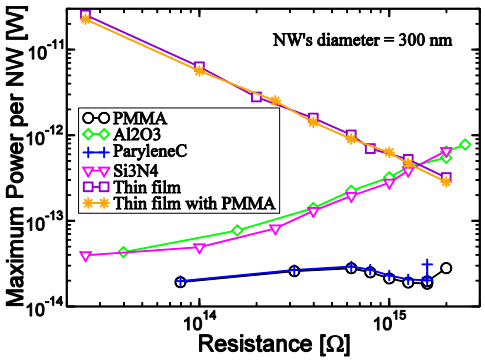

Figure 2. FEM results: maximum generated power versus resistance plots for single-NW cells (d=300 nm) with various matrix materials and thin-film reference cells, all located in the middle of the NG. Each point corresponds to a ratio r ranging, from left to right, from 0.1 to 0.9.

provided the voltage generated by single-NW cells in the middle of the device as an approximation for the behaviour of the full NG. In this work, simulations of individual cells are run at different locations of the NG, which are subjected to different strains. Each cell is individually connected to a variable resistive load and the corresponding power is calculated as $P = V^2/R$ (results from cells in the middle of the NG are shown in Fig. 2). Single-NW cells results can then be extended to the whole NG by considering the effect of the top electrode and the number of such cells that would fit for maximum packing in an area equal to that of a NG (2.25 cm^2). The numerical results of Fig. 2 confirm that the stiffer the dielectric, the higher the strain which is transferred to the NWs, thus increasing their piezoelectric output [4]. Full-NG simulations (partially shown in Fig. 4) indicate that NW-based NGs can outperform thin-film devices (thickness equal to NWs length) if their density corresponds to $r \geq 0.7$ (more than $1.2 \cdot 10^9$ NWs of 300 nm diameter on the whole NG) and the matrix material is sufficiently stiff (i.e. Si_3N_4, Al_2O_3).

III. Device Preparation

Device fabrication follows the same process flow as in [4]. Piezoelectric ZnO NWs (C in Fig. 1, approximately 3 µm long and 300 nm in diameter [6]) were grown using a hydrothermal method [4] on flexible stainless steel substrate (A) from a ZnO seed layer (B) deposited through Atomic Layer Deposition (ALD). This was followed by the deposition of a dielectric as matrix material (PMMA). The matrix layer was deposited by spin coating and consists of a double coating of PMMA (D and E). Aluminium (200 nm thick) was deposited as top electrode (F) by evaporation.

IV. Experimental Results and Discussion

The characterization focused on a NW-based NG fabricated following the procedure presented in Section III and on a commercial thick-film energy harvester (Piceramic P876-A11), with active layer volume of $6.75 \cdot 10^{-4}$ cm^3 and 0.213 cm^3, respectively. Thanks to its higher flexibility, the NG bends with much less force than A11 (1.3 N instead of 8.2 N). Measurements were taken by automatically bending the devices using a dedicated test bench based on an Arduino-controlled servomotor (Fig. 3). The samples were connected to various resistors and in parallel to the differential input of an instrumentation amplifier, whose output was acquired through an oscilloscope. The maximum voltage of the generated peaks was measured and averaged to calculate the maximum power as $P_{max}=V_{max}^2/R$, and normalised by the active material's volume. The results are reported in Fig. 4, which shows the higher power density generated by the commercial device with respect to the NG. The same Figure shows that simulated ideal NGs could outperform these results. Optimal load resistances were found to be 470 kΩ (~0.3 µW/cm^3) and 330 kΩ (~27 µW/cm^3) for NG and A11, respectively. Open-circuit voltages were ~18 mV and ~1.9 V for NG and A11.

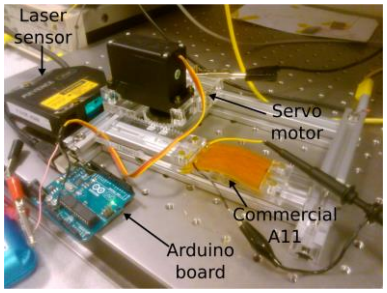

Figure 3. Photograph of the bending setup used for the characterisation of the piezoelectric transducers.

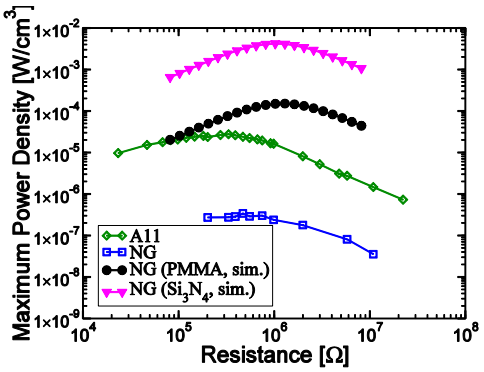

Figure 4. Measured power density (normalized by the volume of the active material) versus resistance curves for A11, NG and two simulated curves (filled symbols) for indealised NGs devices with PMMA and Si_3N_4 matrix.

Simulations show that ideal NGs even with PMMA can outperform actual commercial energy harvesters; stiffer dielectrics would further increase performances. The main reason why the experimental and simulated curves of NG with PMMA are so different lies in ZnO's semiconducting behaviour [7], which was neglected. More information will be included in the final paper.

Acknowledgement

This work received partial support from FLAG-ERA Convergence (French ANR and Italian MIUR via IUNET Consortium), French Nano2017 project and Univ. of Udine, Fondazione CRUP. The NGs were fabricated in CNRS Renatech (PTA) and IMEP-LaHC cleanrooms. We thank S. Basrour from TIMA for his help in characterisation.

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Unified Feature Scale Model for Etching in SF_6 and Cl Plasma Chemistries

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***Abstract*—A novel unified feature-scale model for inductive plasma etching is presented. The model gives an accurate description of passivation layers which form on sidewalls during etch processes, by treating them as independent materials. This allows them to be explicitly included in subsequent etch steps, resulting in a more accurate description of the physical process. Therefore, novel gate stack geometries for advanced nodes can be modelled more rigorously.**

Plasma Etching; Process Simulation; Gate Stack Etching; Levelset; TCAD;

I. Introduction

Continued CMOS device scaling has introduced increased complexity to the formation of the transistor gate stack. Pattering gate transistors to meet critical dimension requirements, as laid out in the ITRS roadmap [1], has become increasingly challenging. Control over sidewall tapering has been attained by using several, individual etch steps for each gate stack layer and the simultaneous deposition of a passivation layer during most of these etch processes [2]. The two etch steps during polysilicon etching are: main etch (ME) and over etch (OE). Both of them provide a polymer layer, which protects the polysilicon during subsequent etching. We propose a unified feature scale model for the simulation of complex etching processes, as used in the patterning of modern transistor gate stacks, which was implemented into ViennaTS [3], a levelset powered topography simulator. This simulation tool can therefore be used to treat the different materials independently and accurately, which is especially important in understanding the behaviour of the deposited polymers and their interaction with other materials in complex geometries.

II. Unified Feature Scale Model

Our model assumes that, in any complex plasma etch process, there are four fundamental types of particles: neutral, etchant, depositing polymer particles and ions [4]. Due to the long etch times, compared to surface reaction time scales, we can safely assume that each of these substances' concentrations will reach a steady state on the surface. Therefore, the surface coverages of all involved particle types φ_x, where x represents etchant (e), polymer (p), etchant on polymer (ep), and ions (i), are expressed by the following equations:

$$\frac{d\varphi_e}{dt} = J_e S_e\left(1-\varphi_e-\varphi_p\right) - k_{ie}J_i Y_e \varphi_e - k_{ev}J_{ev}\varphi_e \approx 0 \quad (1)$$

$$\frac{d\varphi_p}{dt} = J_p S_p - J_i Y_p \varphi_p \varphi_{pe} \approx 0 \quad (2)$$

$$\frac{d\varphi_{pe}}{dt} = J_e S_{pe}\left(1-\varphi_{pe}\right) - J_i Y_p \varphi_{pe} \approx 0 \quad (3)$$

J_x and S_x are the fluxes and sticking probabilities. The values k_x are stoichiometric factors for ion-enhanced etching (k_{ie}) and evaporation (k_{ev}), while the Y_x describe the ion-enhanced etching yields for polymer (Y_p) and etchant (Y_e) as well as the sputtering yield (Y_s). The above equations can be solved to obtain the concentrations at any given point on the surface. From these, the surface rates are determined. If deposition dominates (surface rate is positive), instead of etching, a deposition rate is applied to the material given by:

$$v = \frac{1}{\rho_d}\left(Y_p J_i \varphi_{pe} - J_p S_p\right) \quad (4)$$

Therefore, a new material represented as an independent levelset grows on top of the old material, which is currently being etched. If etching dominates, the following etch rate is applied to the top most material:

$$v = \frac{1}{\rho_m}\left(J_i Y_e \varphi_e + J_i Y_s\left(1-\varphi_e\right) + J_{ev}\varphi_e\right) \quad (5)$$

ρ_d and ρ_m are the densities of the polymer and the material being etched, respectively. The parameters in Equations (4) and (5) can be adjusted systematically to create a set describing a specific etch process, without changing the underlying model. The levelset approach applied in this work, allows for the tracking of complex deformation, separation, and merger of surfaces, essential to represent the thin passivation layers often formed in modern etching techniques. These layers are tracked as separate materials, which is achieved by introducing new surfaces where passivation layers build up and applying deposition only to those. If this new surface is removed during the process, the exposed sections of the underlying material are etched again. This seamless integration of different materials and processes into one model enables efficient and robust simulations of these complex processes, while being able to record deposited polymer layers separately. This is especially useful for sequential simulations, where different passivation layers form on top of one another. Since the materials involved in etch processes interact strongly, the simulated surfaces must not be interpreted as strict boundaries, but rather as rough guides indicating the concentrations of different materials at the interface.

III. Etching in SF_6 Plasma

Since Sulphur Hexafluoride (SF_6) chemistries are often used to etch Silicon (Si) and SiO_2, detailed knowledge about the characteristics of this process is imperative. However, the details of plasma etching in Sulphur and Fluoride chemistries is complex, since both elements are highly volatile, which our model circumvents by assuming a steady state flux from the reactor, impinging on the surface, thereby drastically simplifying the problem.

IV. Etching in Cl Plasma

Chlorine (Cl) based chemistries are mainly used for titanium etching and can show similar behaviour to SF_6 chemistries. However, Cl chemistries can also lead to different geometries depending on the additional gases used during etching, being almost isotropic with high selectivity against Si while also being highly directional and uniform using other additives. The main influencing factors are captured in the few variables described earlier, which enables an accurate representation of the different behaviour of various etch chemistries.

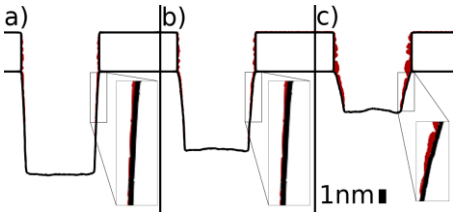

Figure 1. Two-dimensional trenches formed by etching Silicon (black), varying the polymer (red) fluxes to the same mask geometry. Etchant and Ion fluxes were kept constant at 10^{15} $cm^{-2}s^{-1}$ and $1.3 \cdot 10^{16}$ $cm^{-2}s^{-1}$, respectively. Trenches were etched for 25s while the polymer concentration was varied: a)$5 \cdot 10^{15}$, b)10^{16}, and c) $5 \cdot 10^{16}$ $cm^{-2}s^{-1}$.

V. Results

Sample simulations in Figure 1 show how the polymer flux influences the final shape and depth of the etched trenches. A higher polymer flux results in slower etching, and strongly slanted profiles. The figure also shows the different ways the polymer can be treated in the model: While the passivation layer has an associated thickness in some regions, there is no extra layer noticeable in others, although its influence can be seen in the final shape. Etching dominates in the latter, meaning the polymer is removed as soon as it is deposited and therefore cannot form a thick layer. However, this does not mean that there are no polymerising materials on the surface, only that there are too few to form a thick layer.

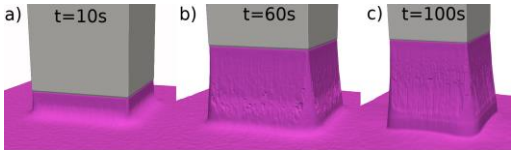

Figure 2. Three-dimensional simulation of Silicon (purple) in a gate stack using a rectangular mask (grey), where a) shows the start of the main etch, b) the start of the over etch step, and c) the end of the Silicon etching. Passivation layers are not shown for clarity.

Sequential simulations, depicted in Figure 2, show the different characteristics of the etch processes in detail: SF_6 etching results in thick passivation layers and therefore leads to strongly slanted profiles of the polysilicon substrate. An intermediate over etch step is applied, which is highly selective in order not to damage the TiN underneath [5]. The subsequent Cl based etch steps are very selective but less directional leading to a complex final shape noted in Figure 3. Here, we clearly demonstrate the ability of the unified model to simulate intricate and sequential etching processes including those essential for the fabrication of advanced node gate stacks.

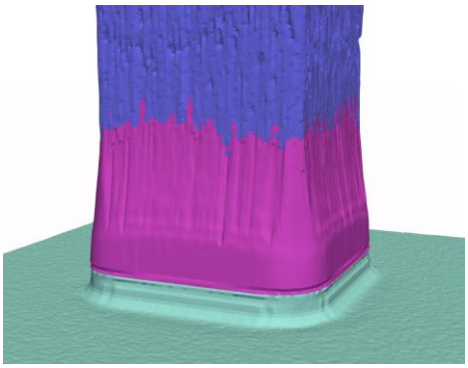

Figure 3. Final profile of a complex gate stack etching simulation. TiN (green) is etched last with an isotropic chemistry resulting in a concave profile, while Silicon (purple) is etched using highly directional chemistries resulting in a tapered profile and deposition of a passivation layer (blue).

VI. Conclusion

A unified feature scale model, implemented in a process simulator, is used to describe many chemically different etch processes effectively. This enables simulations of complex geometries involving many layers and several sequential etch steps. In addition, newly deposited elements, such as passivation layer forming polymers, can be represented as separate materials, enhancing simulation accuracy for complex, nanoscale fabrication processes.

Acknowledgement

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A Design-oriented Charge-based Simplified Model for FDSOI MOSFETs

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***Abstract*—In this paper a design-oriented model for asymmetrical double-gate (ADG) MOSFETs is proposed. Including the back-gate effect into the original simplified EKV bulk model requires only one additional parameter to the existing four, and extends the simplified EKV model to FDSOI processes. This will help the designer to find the right trade-off in terms of design parameters, including the back-gate biasing. A comparison with measurement results from a 28-nm FDSOI CMOS process is provided, assessing the excellent accuracy of the proposed.**

***Index Terms*—simplified EKV, modeling, FDSOI, back-gate**

I. Introduction

In most of the applications that nowadays are dealing with integrated circuits, low-power operation is a key aspect. Due to this fact, conventional design methodologies have been revised in order to exploit at best all the features of advanced technologies [1]. In that sense, the simplified EKV model (sEKV) [2], based on the inversion coefficient (IC), has demonstrated its effectiveness in describing the performance of MOSFETs in all inversion conditions while using only a few parameters. The key of this capability, together with the charge-related basis, is the normalization, that strips off the dependence to a specific technology which is then captured by only a few parameters. This makes the simplified EKV model suitable also as a benchmark for technologies, in addition to helping the designer to explore the design space and find the right trade-off in terms of design parameters [2].

However, the technologies portfolio has been growing rapidly as the scaling-down process gets close to reach physical limits achievable with a standard bulk planar technology. In the latest years, two main alternatives to bulk process has emerged, i.e. finFET and FDSOI processes [3], [4]. If in the case of finFET, the sEKV bulk model is still suitable [2], for FDSOI back-gate effects have to be considered. Therefore, this further degree of freedom has been addressed through a re-adaptation of the sEKV model, so that the design flow can directly focus on the performance trade-offs linked also to the back-gate biasing.

II. Model description

As a starting point, the simplified EKV Model is considered [2]. All voltages are normalized to the thermal voltage $U_\mathrm{T} = K_\mathrm{B}T/q$, where K_B is the Boltzmann constant, T is the temperature and q is the electron charge. The crucial statement that enables the inclusion of back-gate effect is the re-definition of the channel pinch-off voltage v_p. The sEKV model for bulk processes defines it as $(v_\mathrm{g} - v_\mathrm{t0})/n$, that is the difference between the gate voltage and the threshold voltage, rescaled with respect to the slope factor n. Targeting ADG processes, this definition has to be modified accounting for the two independent gates, namely the front-gate voltage v_fg and the back-gate voltage v_bg.

In the range of voltage useful for the designer, the impact of the back-gate voltage can simply be modeled as a threshold voltage with a linear dependence to v_bg (this claim will be confirmed in Section III), so the pinch-off voltage v_p can be defined as

$$v_\mathrm{p} = \frac{v_\mathrm{fg} - v_\mathrm{t}}{n} = \frac{v_\mathrm{fg} - (v_\mathrm{t0} - k_\mathrm{ox} v_\mathrm{bg})}{n}, \tag{1}$$

where v_t0 is the threshold voltage when v_bg is set to 0, and k_ox is a constant parameter directly linked to the device structure, namely to the two gate oxide capacitances ratio:

$$k_\mathrm{ox} = \frac{C_{\mathrm{ox_b}}}{C_{\mathrm{ox_f}}} = \frac{EOT_\mathrm{f}}{EOT_\mathrm{b}}, \tag{2}$$

Hence, through the voltage-charge and current-charge relations of the sEKV including velocity saturation [2], the voltage-current expression related to the front- and back-gate voltages can be derived.

III. Model validation

In order to confirm the validity of the previously described sEKV model, a set of measurement data from a 28-nm FDSOI technology is considered (Fig. 1). In detail, two process options with different front-gate oxide thicknesses have been analyzed. Since the two families of devices differ only by their equivalent front-gate oxide thickness EOT_f, by means of the obtained values for k_ox in the two cases the equivalent back-oxide thickness EOT_b can be extracted. If the theory is valid, the EOT_b values extracted from both families should match.

Considering the case of Thin-Oxide nMOSFETs (Figs. 1a to 1c), the extracted k_ox value is 66.7 mV/V. Since the EOT_f for this family is equal to 1.55 nm, from (2) the value obtained for EOT_b is 23.24 nm. Thus, in order to have the model assessed, from the obtained EOT_b value and the k_ox extracted for Thick-Oxide nMOSFET (158 mV/V), the EOT_f value known *a priori*, 3.7 nm, should be obtained. Indeed, using again (2), a value of 3.67 nm for EOT_f is derived, with less than 1% discrepancy.

Proceeding the same way for Thin-Oxide pMOSFETs (Figs. 1d to 1f, EOT_f=1.7 nm), the extracted k_ox results in

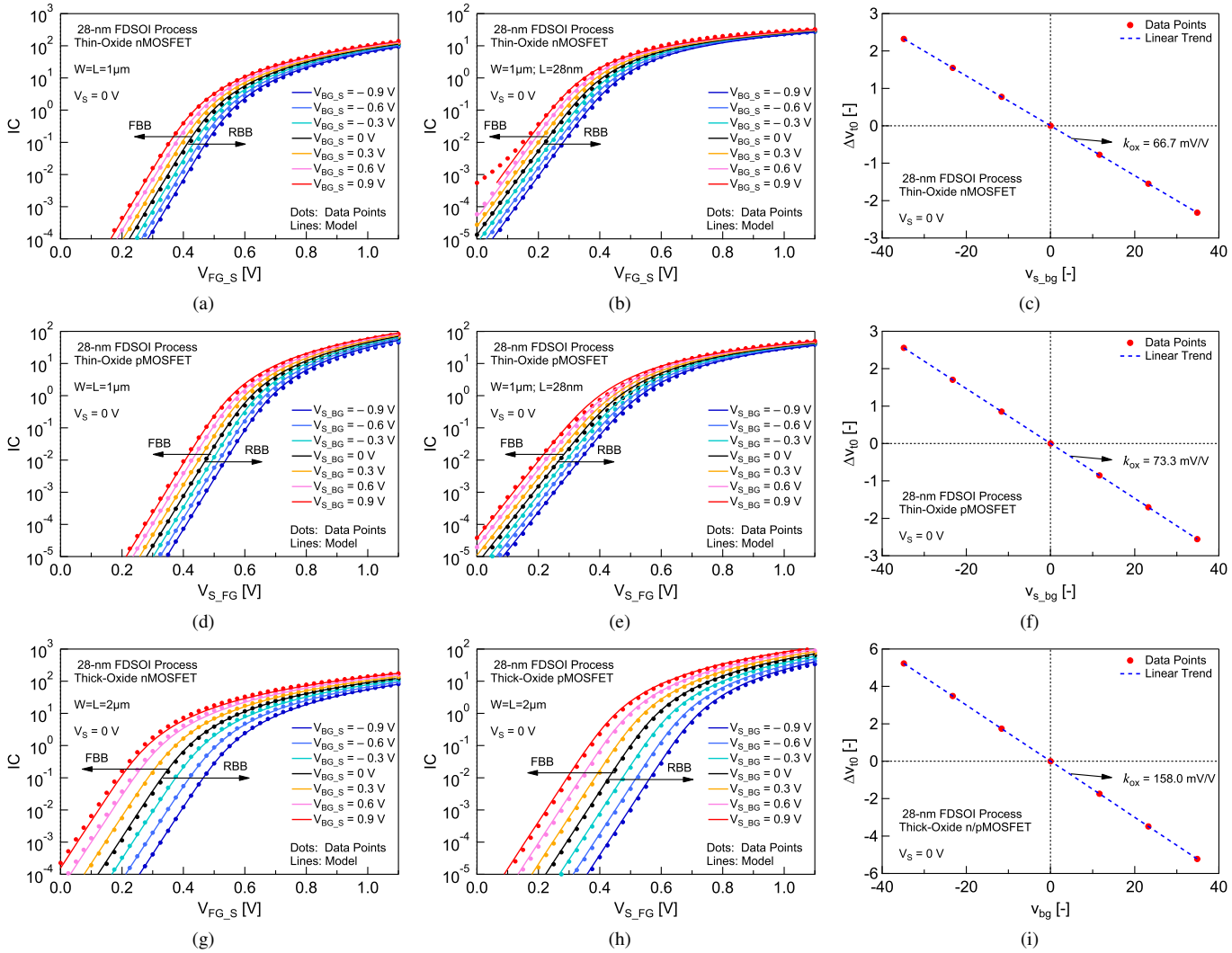

Fig. 1: a),b),d),e),g),h) IC vs front-gate voltage (referred to the source) at different back-gate bias points. c),f),i) k_{ox} extraction from Δv_{t0} vs v_{bg} plots.

73.3 mV/V, that gives an EOT_{b} of 23.28 nm. Consequently, for the Thick-Oxide family an EOT_{f} of 3.68 nm is obtained, close to the expected value of 3.7 nm.

IV. Conclusions

A charge-based simplified model for ADG processes is proposed, that is able to include the effect of back-gate biasing on the threshold voltage by means of only one additional parameter, k_{ox}, with respect to the four used in the bulk model. Through measurement data analysis on two device families from a 28-nm FDSOI process, the approach has demonstrated to be effective, by checking the correspondence between extracted physical parameters, i.e. the equivalent front- and back-oxide thicknesses, and their expected value.

The straightforward consequence of this approach, is that even for FDSOI processes, the IC-based design methodology [5] remains valid including the additional back-gate voltage. On top of that, the new parameter k_{ox} can act as a range shifter for the charge-to-voltage relationship, meaning that for the same front-gate bias point and geometry, the device can operate in a range of ICs, directly linked to the value of k_{ox}. This has been already shown practically [4], but now it can be assessed quantitatively and, above all, simply.

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Characterization of gate overlap capacitances and effective channel size in MOSFETs

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***Abstract*— Characterization of MOSFET gate overlap capacitances is discussed. A new approach for extraction of the gate overlap capacitances and of the channel width and length variation in planar MOSFETs is presented.**

Keywords-MOSFET, CV characteristics, overlap capacitances, channel shortening, cannel narrowing

I. INTRODUCTION

Determination of the gate overlap capacitances has been discussed e.g. in [1,2,3]. However, two issues have not been addressed in those works. Firstly, the channel narrowing (ΔW) and/or shortening (ΔL) affect the gate overlap capacitance extraction. In [1] it was proposed to use I(V) measurements for extraction of these data. In [2] the approximate analytical formulae were used. Secondly, depending on the gate voltage different values of the overlap capacitances may be obtained. We propose simple methods for the parallel extraction of the gate overlap capacitances and channel size variations based on the $C_{gb}(V_{GB})$ and $C_{gs}(V_{GS})$ characteristics measurements.

II. GATE-SUBSTRATE CAPACITANCE CHARACTERIZATION

For the extraction of the gate-substrate overlap capacitance C_{gb0} a series of the MOSFETs with nominal gate lengths L and widths W (W << L) is used (Fig. 1).

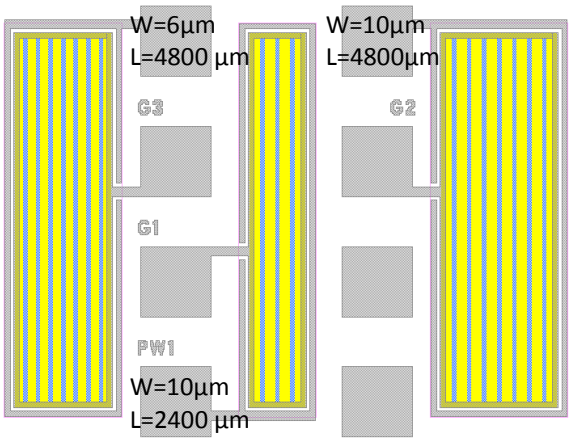

Figure 1. Layout of the long-channel NMOSFETs for extraction of C_{gbo} and ΔW.

We have assumed that the effective channel widths W_{eff} are given by W+ΔW. The measured C_{gb} capacitances (Fig. 2) consist of three components: the measurement setup capacitance $C_{gb,setup}$, the edge capacitance $L \cdot C_{gb0}$, and the inner capacitance $W_{eff} \cdot L \cdot C'_{gb}$ which depends on the gate bias (1).

$$C_{gb}(V_{GB}) = C_{gb,setup} + L \cdot C_{gb0} + W_{eff} \cdot L \cdot C'_{gb}(V_{GB}) \qquad (1)$$

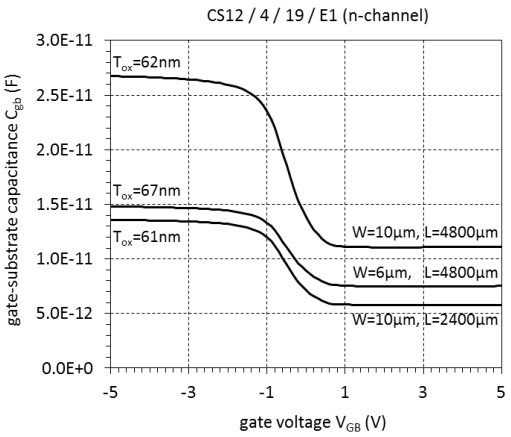

Figure 2. $C_{gb}(V_{GB})$ characteristics of three capacitors shown in Fig.1 with incorrect estimation of gate oxide thickness.

In order to determine $C_{gb,setup}$, the $C_{gb}(V_{GB})$ data is used for a series of MOSFETs with the same width W_{eff}, and different lengths L. We apply a regression of C_{gb} vs L. The regression offset determines $C_{gb,setup}$ (Fig. 3). Next, from (1) we obtain (2).

$$(C_{gb}-C_{gb,setup})/L = C_{gb0} + C'_{gb}(V_{GB}) \cdot (W+\Delta W) \qquad (2)$$

Based on (2), it can be expected, that irrespective to $C'_{gb}(V_{GB})$ the regression lines have a single cross-section at ($-\Delta W$, C_{gb0}). However the unambiguous identification of this point is not always possible (Fig. 4). A similar effect was reported in [4] for the MOSFET output resistance vs channel length measurements. For the unambiguous extraction of ΔW, C_{gb0} we follow the approach proposed in [4] and expressed by (3)

$$(C_{gb}-C_{gb,setup})/L = a \cdot W + b \qquad (3)$$

where $a=C'_{gb}(V_{GB})$, $b=C'_{gb}(V_{GB}) \cdot \Delta W + C_{gb0}$. A regression based on a relationship between $(C_{gb}- C_{gb,setup})/L$ and W

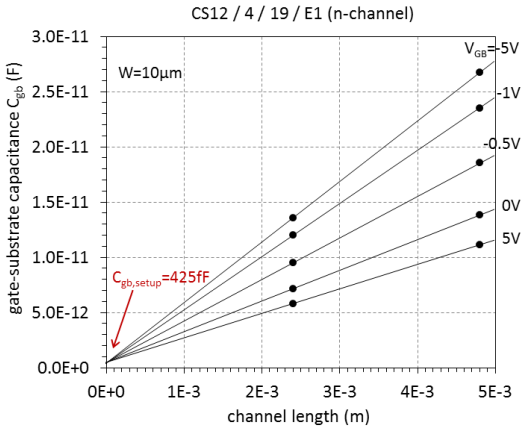

Figure 3. Extraction of $C_{gb,setup}$.

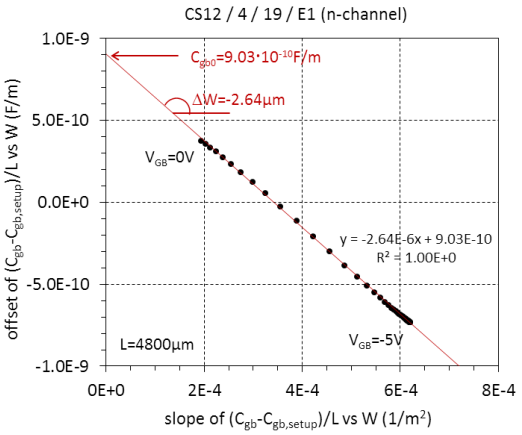

Figure 5. Unambiguous extraction of C_{gb0}, ΔW.

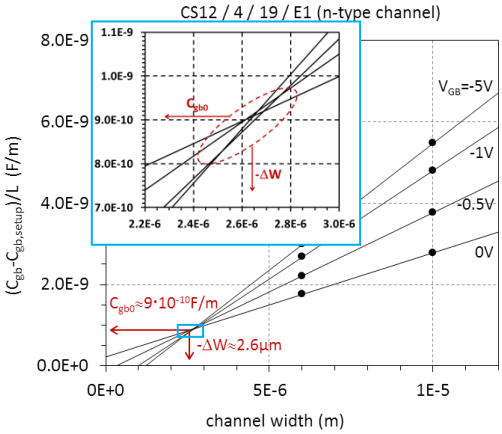

Figure 4. Intersections of the regression lines (C_{gb}-$C_{gb,setup}$)/L vs W demonstrating ambiguity of C_{gb0}, ΔW extraction.

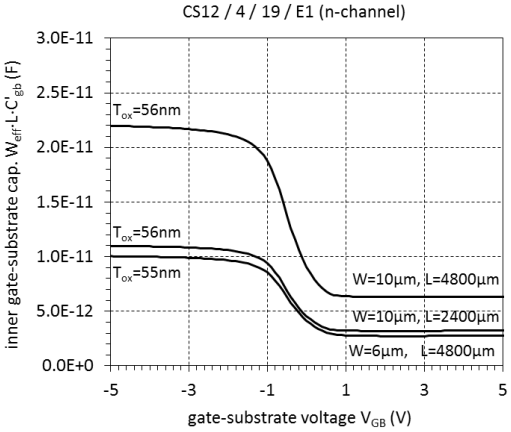

Figure 6. Inner capacitance $C'_{gb}(V_{GB})$ characteristics demonstrating a role of the overlap capacitance C_{gb0} (see Fig.2) and corrected estimation of gate oxide thickness.

for devices with constant length L, and for a given V_{GB} gives the slope a and offset b, where b=a·ΔW+C_{gb0}. The a, b coefficients depend implicitly on V_{GB}, and it is worth mentioning that by extraction of a(V_{GB}) characteristics the inner capacitance characteristics $C'_{gb}(V_{GB})$ is explicitly determined. In order to obtain unique values of ΔW and C_{gb0} we propose to use the regression based on the correlation between a(V_{GB}) and b(V_{GB}) data (Fig. 5). Finally, the inner gate-substrate capacitance may be determined either as W_{eff}·L·$C'_{gb}(V_{GB})$ or as $C_{gb}(V_{GB})$-$C_{gb,setup}$-L·C_{gb0} (Fig.6).

III. GATE-SOURCE CAPACITANCE CHARACTERIZATION

For the extraction of the gate-source overlap capacitance C_{gs0} and of the channel shortening ΔL a series of the MOSFETs with nominal gate lengths L and widths W (W >> L) is used. The parameter extraction sequence is similar to that presented in section II. It is based on the formula (4)

$$C_{gs}(V_{GS})=C_{gs,setup}+W\cdot C_{gs0}+ W\cdot L_{eff}\cdot C'_{gs}(V_{GS}) \quad (4)$$

where $C_{gs,setup}$ is the measurement setup capacitance, C_{gs0} is the gate-source overlap capacitance per unit width, W·L_{eff}·$C'_{gs}(V_{GS})$ is the gate bias-dependent inner gate-source capacitance, and L_{eff}=L+ΔL. The extraction procedure determines subsequently $C_{gs,setup}$, $C'_{gs}(V_{GS})$ characteistics, and unique values of C_{gs0} and ΔL. The full description of the method for C_{gs0} and ΔL extraction and its demonstration using the experimental data will be given if the full version of the paper.

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Effect of Schottky Barrier Contacts on Measured Capacitances in Tunnel-FETs

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***Abstract*—The influence of Schottky barriers at $NiSi_2$ contacts of Si Planar p-TFETs on Ultrathin Body [1] is analyzed in terms of deviations between measurements, TCAD simulations and a proposed compact model for the intrinsic capacitances in TFETs presented in [2]. A theory for the reason of the deviations for the intrinsic capacitances is evolved and discussed. Additionally, TCAD simulations are performed to support the theory.**

Keywords—Tunnel-FET; AC model; intrinsic capacitances; Schottky barrier; TCAD simulations.

I. Introduction

Recently tunnel field-effect transistors (TFET) are in the center of the attractions to be the surrogate of the standard MOSFET. This ever increasing interest owes to their feasibility to overcome the 60 mV/dec subthreshold slope limitation of the standard MOSFETs [3]. In order to perceive the working principle of TFETs and also making circuit simulations using multiple TFETs possible, simulations as well as models which show all aspects of the device are required.

In our previous work [2] a compact model for intrinsic capacitances in TFETs was introduced. Results were compared with measured data of a p-type fabricated device as well as TCAD simulations. In all measured data it could be seen that the gate-source capacitances (C_{gs}) in on-state increase and gate-drain capacitances (C_{gd}), after a certain bias start to decrease. In ambipolar-state same effect could be seen. That is to say, capacitances C_{gd} increase rather than stay steady and capacitances C_{gs} slightly sink (see Fig. 1).

It was expected by including the effect of parasitic resistances [4] and also voltage drop in the channel, this effect would be seen in the model as well. Actually, considering these effects has caused some changes in the correct direction but there is still room to improve it. Therefore, in this work the focus is exclusively laying on this effect and factors which give cause for increase and decrease of capacitances.

II. Small Signal Analysis including Schottky Contacts

In [2] to compensate the unexpected increase and decrease of capacitances, the effect of source and drain parasitic resistances is included in the model. Considering transconductance (g_m) and output conductance (g_{ds}) and their crucial influence on capacitances showed that the effect of parasitic resistances needs to be calculated for on and ambiplolar-state separately. In the measured TFETs $NiSi_2$ is used as contact material. Despite $NiSi_2$ has a mid-gap work function with respect to silicon, high doping of the semiconductor should result in an ohmic contact due to tunneling of carriers through the Schottky barrier (see Fig. 2). But at drain side the doping in TFET often is reduced to suppress the ambipolar current. This lowers the small signal conductance of the contact. Because the tunneling barrier in the TFET is the bottleneck for the current, having a voltage drop of nearly V_{ds}, the voltage across the Schottky barriers at the contacts is almost zero. At this bias the small signal conductance of the Schottky barrier can come into the same order of magnitude as g_m and g_{ds} of the TFET (see Fig. 3).

In on-state it is assumed $C_{gd} >> C_{gs}$. Furthermore, analytical calculations based on the results in [2] and [4] show, that the main impact comes from the drain, therefore the focus in a first attempt is set on the drain Schottky barrier. Considering this assumption, the capacitances affected by parasitic resistances in on-state are defined as

$$C'_{gd} = C_{gd} - C_{gd}\frac{g_{ds}}{g_d} \tag{1}$$

$$C'_{gs} = C_{gs} + C_{gd}\frac{g_m}{g_d}. \tag{2}$$

g_d represents the parasitic small signal conductance of Schottky barrier at drain terminal (see Fig. 2).

TCAD simulations of a TFET structure including two Schottky barriers at source and drain showed poor convergence. However, during the study of this effect convergence has been improved slightly and a few results have been won. They show results which are offering a tendency, but not in total agreement with the theory and analytics. Nevertheless, to calculate g_d, Schottky diodes for a low bias with different drain doping concentrations have been simulated in TCAD. Comparing the resulted current with measured data showed that the current flowing In Schottky diode with drain doping lower than $1 \times 10^{19} cm^{-3}$ is in the same range as in the p-type TFET (see Fig. 3). The transconductance and output conductance are calculated as

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \qquad g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}}. \tag{3}$$

In ambipolar-state it is assumed that $C_{gs} >> C_{gd}$ and g_s is the parasitic small signal conductance of Schottky barrier at source terminal.

$$C'_{gd} = C_{gd} + C_{gs}\frac{g_m}{g_s} \tag{4}$$

$$C'_{gs} = C_{gs} - C_{gs}\frac{g_{ds}}{g_s}. \tag{5}$$

III. VERIFICATION AND CONCLUSION

The pattern which measured TFET capacitances show are not visible in TCAD simulations without Schottky barriers at source/drain (dotted curves in Fig. 4.c). So, it is assumed parasitic small signal resistances of Schottky barriers at source and drain have effect on intrinsic capacitances. This assumption has led to eq. (1), (2), (4) and (5). Regarding the Schottky diode simulations shown in Fig. 3, it is considered $g_d = 1e^{-6}(\Omega\mu m)^{-1}$.

To verify this theory, current curves of a Double-Gate n-TFET are simulated in TCAD and from them g_m as well as g_{ds} corresponding to each drain voltage are calculated. C_{gd} and C_{gs} in the on-state are obtained from AC simulations. Considering the effect of Schottky barrier C'_{gd} and C'_{gs} are calculated by applying eq. (1) and (2) and compared with the corresponding simulations without the consideration of Schottky barrier and the result is depicted in Fig. 4.

By including the effect of Schottky barrier on capacitances, C'_{gd} decreases and C'_{gs} increases. At $V_{ds} = 0.1$ V decrement in C'_{gd} is stronger than at $V_{ds} = 0.3$ V and it is similar to what measurements show. The reason is that for smaller V_{ds}, as it is shown in Fig. 4.b, g_{ds} has higher value and therefore, parasitic small signal resistances of Schottky barrier affect C_{gd} stronger.

It can be seen, including the effect of Schottky barrier on capacitances, simulations are improved and show a similar pattern as in measured data.

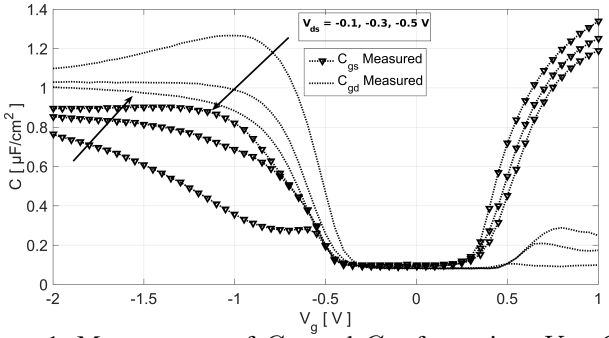

Figure 1: Measurement of C_{gs} and C_{gd} for various V_{ds}. C_{gs} of p-type device in its on-state increases as well as C_{gd} in ambipolar-state.

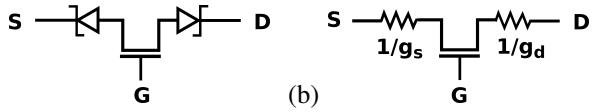

Figure 2: Schematic of p-type device a) considering Schottky diodes and b) small signal conductances of Schottky barriers at source and drain.

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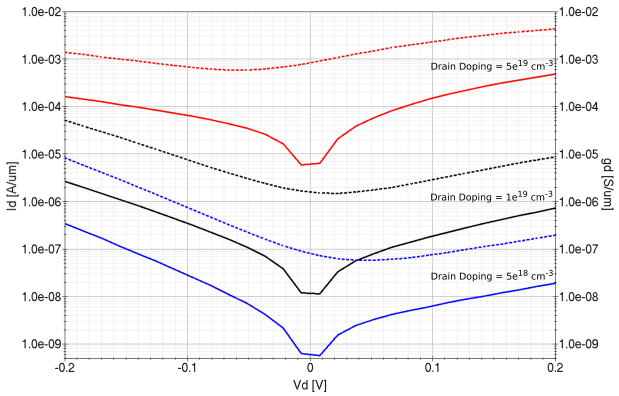

Figure 3: Schottky diodes to estimate the small signal conductance of the Schottky barriers at source/drain of TFET are simulated. Solid lines show the current as a function of the voltage across the Schottky barrier. Dotted curves represent the small signal conductance of corresponding diodes.

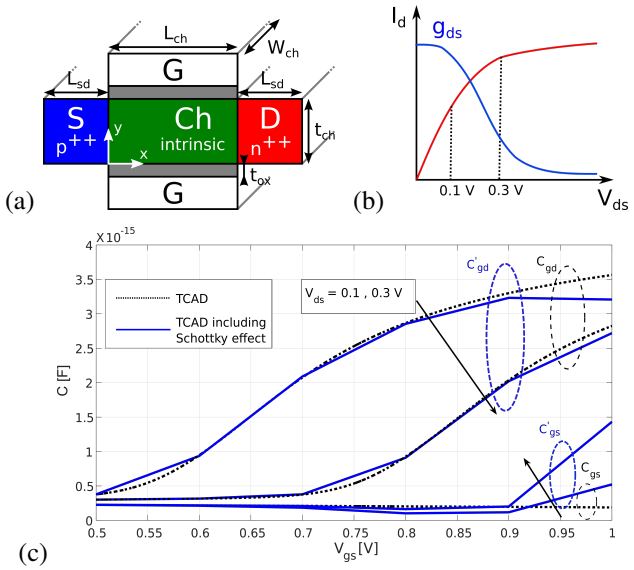

Figure 4: a) Double-Gate n-type TFET structure in TCAD. b) Sketch of the output characteristic and g_{ds}. c) TFET Capacitances simulated in TCAD. Blue solid lines show simulations including Schottky barrier effect. $L_{ch} = 22$ nm, $t_{ch} = 10$ nm, $W_{ch} = 1$ μm and $t_{ox} = 2$ nm. Oxide material is HfO_2.

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An Efficient Model for Charge and Gate Capacitance in III-V Cylindrical Nanowire Transistors

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***Abstract*—In this paper, we present a computationally efficient compact model for calculating the charges and the gate capacitance of III-V cylindrical nanowire transistors. We proposed an approximation which decouples the Poisson and the Schrödinger equation and addresses the issues of developing a computationally efficient analytical model. Using the proposed approximation, we derive a model suitable for the circuit simulators. The model is physics based and does not include any empirical parameters. The accuracy of the model is verified across nanowires of different sizes and materials using simulation results from a 2D Poisson-Schrödinger solver.**

I. Introduction

III-V nanowire (NW) transistors are amongst the most promising contenders for future CMOS technology nodes [1]. Several recent demonstrations have shown the integration feasibility of III-V NW transistors [2]. However, ultimate production of ICs with NW transistors will depend on their circuit performance, whose evaluation needs compact models suitable for circuit simulators. The NW transistors show significant quantum behavior due to the high quantum confinement along with the low effective mass of III-V materials. Since, the existing models are unable to capture these effects in a compact modeling framework, new compact models for III-V NWs are required.

The physics of NW transistors are impacted by geometrical and electrical confinement. To accurately capture both these effects, coupled Poisson-Schrödinger equation (PS) need to be solved self-consistently. Solving the PS equation is computationally very expensive and not suitable for a circuit simulator. The model presented in [3] decoupled the Poisson and the Schrödinger equations by modeling the electrical confinement as a perturbation to the geometrically confined subband energy. The need of the wavefunction and the potential profile inside the channel makes the calculation of this perturbation term implicit. A numerical estimation is required, which is not desirable for a compact model used in circuit simulators. The problem has been recently addressed in [4] where the NW electrostatics are modeled explicitly. The model is accurate although an empirical fitting parameter is used to calculate the subband energies as a function of the gate voltage.

In this paper, we propose a simple but effective approximation which eliminates the need for using the exact form of the wavefunction. The proposed approximation significantly simplifies the calculation of the channel potential profile. Using it, the perturbation term can be calculated analytically and used to model the electrical confinement. The presented compact model is physics-based and computationally efficient. The accuracy of the model is verified by comparing it with the solution provided by a 2D self-consistent PS solver [3].

II. Model Description

Using the Gauss law one can write semiconductor charge (Q_s) as a function of the gate voltage (V_G) and the surface potential (Φ_s) as,

$$Q_s = -C_{ins}(V_G - \Phi_{ms} - \Phi_s) \tag{1}$$

where Φ_{ms} is the metal-semiconductor work function difference and $C_{ins} = 2\pi\epsilon_{ins}/ln(1 + t_{ins}/R_0)$, is the insulator capacitance per unit length, R_0 is the semiconductor radius and t_{ins} is the insulator thickness. Q_s can also be calculated as,

$$\begin{aligned} Q_s =& -q\int_0^{2\pi}\int_0^{R_0} n(r,\theta)drd\theta \\ =& -q\Sigma_{j=0}^{n} g_v \left(\frac{2m^* k_B T}{\pi\hbar^2}\right)^{1/2} F_{-1/2}\left(-\frac{E_j - q\Phi_c}{k_B T}\right) \end{aligned} \tag{2}$$

In (2), g_v is the valley degeneracy, m^* is the effective mass, k_B is the Boltzmann constant, T is the temperature, $\hbar$ is the reduced Plank's constant, $F_{-1/2}$ is the Fermi Dirac integral of order -1/2, E_j is the subband energy level and Φ_c is the center potential.

A relation between Φ_c and Φ_s can be derived using the Poisson equation, which in cylindrical coordinates is given by,

$$\frac{1}{r^2}\frac{\partial^2\Phi}{\partial\theta} + \frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\Phi}{\partial r}\right) = \frac{q}{\epsilon_s}(n(r,\theta) + N_a) \tag{3}$$

and

$$n(r,\theta) = \Sigma_{j=0}^{n} g_v \left(\frac{2m^* k_B T}{\pi\hbar^2}\right)^{1/2} F_{-1/2}\left(-\frac{E_j - q\Phi_c}{k_B T}\right)|\Psi_j(r,\theta)|^2 \tag{4}$$

where $\Psi_j(r,\theta)$ is the wave-function of the j^{th} subband. $\Psi_j(r,\theta)$ can be expressed in terms of Bessels functions. Although mathematically accurate, they complicate the modeling, especially when incorporating the electrical confinement in the compact modeling framework. However, motivated from the fact that a high quantum confinement and low effective mass of III-V material leads to significant volume inversion in the channel, a more heuristic approach would be to approximate the $n(r,\theta)$ with a constant profile such that the Q_s remain same as (2). The use of this constant charge approximation (CCDA) not

only makes $n(r,\theta)$ independent of r and θ but also eliminates the need to use an exact form of $\Psi_j(r,\theta)$. The wavefunction can be approximated as $\Psi_j(r,\theta) = \exp(ij\theta)/\sqrt{\pi}R_0$. Using the CCDA, (4) can be written as,

$$n(r,\theta) \approx \frac{1}{\pi R_0^2} \Sigma_{j=0}^{n} g_v \left(\frac{2m^* k_B T}{\pi\hbar^2}\right)^{1/2} F_{-1/2}\left(-\frac{E_j - q\Phi_c}{k_B T}\right) \quad (5)$$

$$= \frac{Q_s}{q\pi R_0^2} \quad (6)$$

where (2) is substituted in (5). Putting (6) in (3), Φ as a function of r can be calculated analytically as,

$$\Phi(r) = \Phi_c - \frac{Q_s}{\pi R^2 \epsilon_s}\left[\frac{r^2}{4}\right] \quad (7)$$

Note that the potential is symmetric across the angular direction, therefore, Φ is a function of only the radial coordinate. Evaluating (7) at $r = R_0$ and replacing Φ_s in (1) gives,

$$Q_s = -C_{ins,eff}(V_G - \Phi_{ms} - \Phi_c) \quad (8)$$

where $C_{ins,eff}$ is the effective insulator capacitance given by $C_{ins,eff} = C_{ins}/1 + (C_{ins}/4\pi\epsilon_s)$ and captures the effect of the charge centroid. The subband energies E_j can be written as,

$$E_j = E_{j,g} + \Delta E_{j,e} \quad (9)$$

where $E_{j,g}$ is the subband energy considering geometrical confinement and can be calculated as in [4]. The electrical confinement can be modeled by adding the perturbation term $\Delta E_{j,e}$ in E_j, calculated as,

$$\Delta E_{j,e} = < \Psi_j^* | \widetilde{\Phi} | \Psi_j > \quad (10)$$

where the perturbing potential is given by, $\widetilde{\Phi}(r) = \Phi(r) - \Phi_c$. Using the CCDA, (10) can be calculated analytically as,

$$\Delta E_{j,e} = \frac{qQ_s}{8\pi\epsilon_s} \quad (11)$$

Using (8) for Q_s in (11) and substituting in (2) we get

$$Q_s = -C_q \Sigma_{j=0}^{n} F_{-1/2}\left(\frac{q\Phi_c(1-C_x) - E_{j,g} + qC_x(V_g - \Phi_{ms})}{k_B T}\right) \quad (12)$$

Here, $C_q = qg_v(2m^* k_B T/\pi\hbar^2)^{(1/2)}$ and $C_x = C_{ins,eff}/8\pi\epsilon_s$. (8) and (12) can be solved for Φ_c as a function of V_G, which can then be used to get Q_s.

The proposed model is compared with the solution provided by a 2D self-consistent PS solver for different nanowire sizes and materials. The details about the PS solver and the material parameters can be found elsewhere [4].

Fig. 1 and 2 shows the simulated (symbols) and the modeled (solid line) Q_s and C_{GG} as a function of V_G for NW of different sizes and material. The model accurately reproduces the results of the PS solver. This shows that CCDA works well for a range of materials and physical dimensions. Note that only three subbands are considered in the model here.

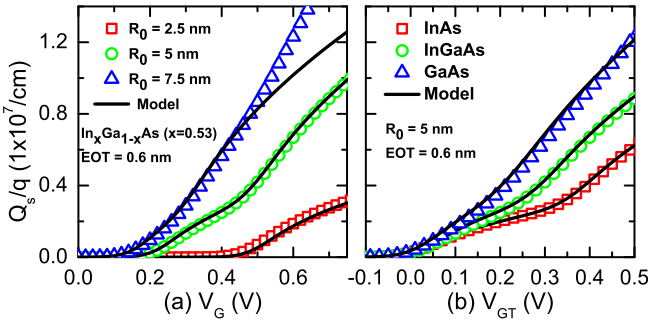

Fig. 1. (a) Semiconductor carrier density Q_s/q as a function of gate voltage V_G for $In_xGa_{1-x}As$ (x=0.53) nanowire transistor of different sizes. (b) Semiconductor carrier density Q_s/q as a function of gate overdrive voltage ($V_{GT} = V_G - V_T$) for a 5 nm radius nanowire transistor with different semiconductor materials. All the data are calculated at zero drain bias.

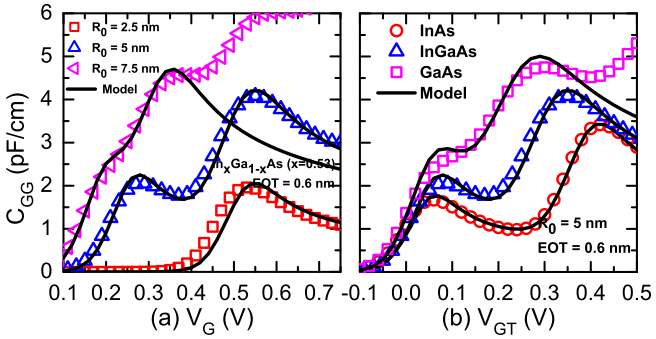

Fig. 2. (a) Gate capacitance C_{GG} as a function of gate voltage V_G for $In_xGa_{1-x}As$ (x=0.53) nanowire of different sizes. (b) Gate capacitance C_{GG} as a function of gate overdrive voltage ($V_{GT} = V_G - V_T$) for a 5 nm radius nanowire transistor with different semiconductor materials. All the data are calculated at zero drain bias.

III. Conclusion

A physics-based compact model for calculating the semiconductor charges and the gate capacitance of III-V cylindrical nanowire transistors was proposed. We introduced an approximation that eliminated the need of knowing the exact form of the wavefunction. This significantly simplified the model derivation. Using this the energy perturbation term could be calculated analytically. A compact model was then derived which is free from any fitting parameters and suitable to be used in a circuit simulator. The accuracy of the model is verified by comparing it with the results of a 2D self-consistent Poisson-Schrödinger solver for different nanowire sizes and materials. The comparison shows the validity of the model across different materials and nanowire dimensions.

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Design Benefits of Self-Cascode Configuration for Analog Applications in 28nm FDSOI Technology

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***Abstract*—This paper showcases SPICE simulated results of single transistors and self-cascode (SC) associations of UTBB transistors from 28FDSOI technology by ST-Microelectronics with a focus on analog integrated circuit design. This comparison demonstrates significant improvement of the voltage gain for the SC association without compromising the transconductance, especially when featuring asymmetric threshold voltages (Asymmetric Self-Cascode – A-SC).**

Keywords-UTBB; FDSOI; Self-Cascode; Analog Design.

I. INTRODUCTION

The improvement of FDSOI technology has led to UTBB or Ultra-Thin Body and Buried oxide (BOX) MOSFETs [1], with channel lengths scaled towards 28nm and below. Thanks to the thin BOX, the MOSFET threshold voltage (V_T) can be controlled by the back-gate bias at relatively small voltages [2]. Still, scaled devices suffer of short channel effects [3] and degraded analog figures of merit, such as the Early voltage (V_{EA}), output conductance (g_D) and, therefore, the intrinsic voltage gain (A_V) [4]. While those characteristics may be improved by simply using longer devices, other parameters, such as the transconductance (g_m), will be degraded [4]. One approach to solve this problem is the use of self-cascode (SC) structures, configured as shown in Fig.1, where V_G is the gate contact, V_D the drain contact, V_S the source contact (for this work, set to ground), V_{BMS} the back gate contact of the transistor close to the source (MS) and V_{BMD} the back gate contact of the transistor close to the drain (MD) [5]. This configuration of separate back gates is possible if the transistors are fabricated over different wells, allowing to apply different biases on each and thus to achieve different V_T for MS and MD transistors. Self-cascodes with both transistors operating at a similar threshold voltage are referred as Symmetric SC (S-SC). SC with V_T of transistor MD smaller than of transistor MS are Asymmetric SC (A-SC). As the effective channel length of the A-SC structure in saturation regime will be closer to the channel length of MS (L_{MS}), g_m is improved, while the added transistor with lower V_T will limit the channel modulation effect, improving g_D, V_{EA} and gain [6], [7]. This work compares single transistors and SCs with focus on analog performance, by means of SPICE simulations using state of the art 28nm FDSOI technology. The SPICE simulations results are solid, since based on industrial models, and the conclusions stand by their own. Analyzed figures of merit include g_m, g_D, V_{EA} and A_V for structures of different channel lengths and different back gate biases.

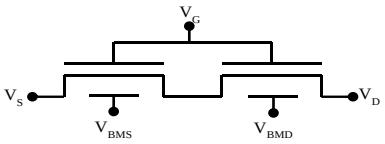


Figure 1. Schematic of the Self-Cascode

II. DEVICE CHARACTERISTICS

The simulated single MOSFETs are n- channels with length of 30 nm and 110 nm, channel width of 1µm. The technology corresponds to ST Microelectronics FDSOI 28nm [8] (effective gate oxide thickness of 1.2 nm and buried oxide thickness of 25 nm) with standard threshold voltage. The results were obtained through simulations performed in SPICE using the software Eldo by Mentor Graphics [9] and the model referenced in [10].

III. CHARACTERISTIC CURVES

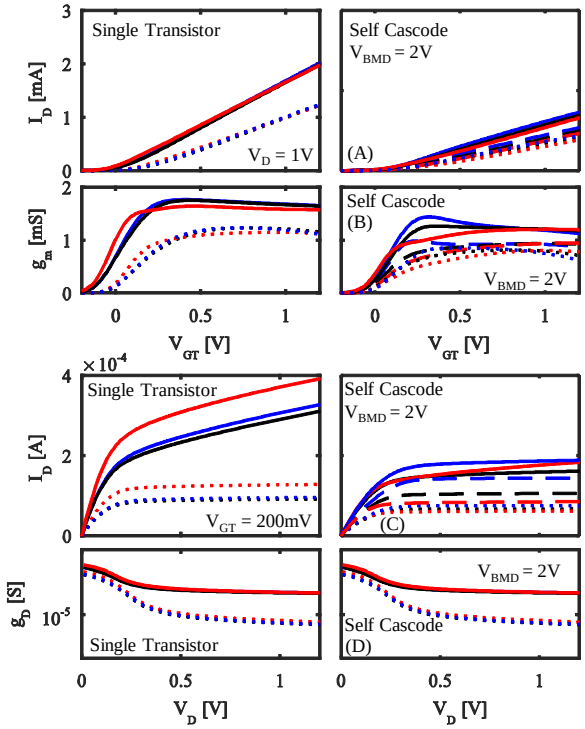
The values for V_T of the single transistors and the SCs at a given back gate bias are shown in Table 1. For the SC, V_{BMD} was maintained at 2 V to achieve the lowest V_T and promote the highest improvement on g_D. It can be noted that even with MD featuring a lower V_T, the V_T of the SC as a whole will be approximately the same as the V_T of MS. In Fig. 2 (A) and (B), the I_D and g_m as a function of the gate voltage overdrive ($V_{GT} = V_G - V_T$) at $V_D = 1$ V are shown. One can see that both I_D and g_m feature lower values for the SC, since the effective channel length tends to L_{MS}, but does not reach it. The I_D and g_D versus V_D at a V_{GT} of 200 mV are shown on Fig. 2 (C) and (D). It is seen that the g_D is successfully reduced by the SC and that the greatest benefit is observed for the largest asymmetry in the back bias, providing the most difference of V_T of MS and MD.

TABLE I. V_T FOR SINGLE TRANSISTORS AND SC

Single Transistor			**Self-Cascode (V_{BMD}=2V)**			
V_B	***L=30nm***	***L=110nm***	**V_{BMS}**	***L_{MS}=30nm L_{MD}=30nm***	***L_{MS}=30nm L_{MD}=110nm***	***L_{MS}=110nm L_{MD}=110nm***
-2V	0.56 V	0.59 V	-2V	0.54 V	0.53 V	0.57 V
0V	0.44 V	0.47 V	0V	0.59 V	0.41 V	0.47 V
2V	0.32 V	0.32 V	2V	0.32 V	0.32 V	0.32 V

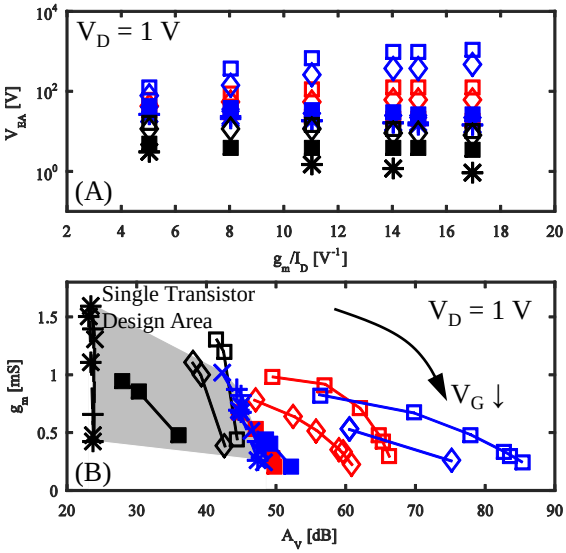
IV. Analog Figures of Merit

Though I_D and g_m are reduced in SC at the same bias point, what matters more for the analog designer are the g_m/I_D and I_D/g_D (=V_{EA}) ratios. The values of V_{EA} are displayed as a function of the g_m/I_D ratio at a V_D of 1V in Fig. 3 (A). The benefits of the A-SC are showcased. Even for the shortest S-SC, an improvement of 65% over the V_{EA} of single transistor of L=30nm and V_B=0V can be seen for g_m/I_D of 5V^{-1}. On Fig. 3 (B), the values of g_m are shown as a function of A_V, for the SC structures and single devices. Different connected points account for different values of front and back gate biases. The hashed area envelops all the potential results of single transistors for L between 30 nm and 110 nm, for the same gate bias range. That area represents the achievable performance trade-off between frequency (given by the g_m/C ratio, C being the load capacitance) and gain area for such single transistors that designers can use in this technology. The results agree with previously published experimental data [11]. SC results with L_{MS}=L_{MD}=30nm are mostly placed within the gray area, but for the most different V_{BMS} and V_{BMD}, designers can already achieve an A_V similar to that of the longest single transistor with V_B=0V, but with a boost of g_m by 87%. By using the SC of L_{MD}=110 nm and L_{MS}=30 nm and V_{BMS}=-2 V, when compared with single transistor of L=110 nm and V_B=-2 V, designers can increase Av by 7 to 18 dB while maintaining the g_m range. Finally, for the SC of L_{MS}=L_{MD}=110nm, a gain improvement by 14 to 37 dB is



Single Transistor (L)			Self Cascode - $V_{B,MD}$ =2V (L_{MS}/L_{MD})			
V_B	30nm	110nm	V_{BMS}	30nm/ 30nm	110nm/ 110nm	30nm/ 110nm
-2	-	···	-2 (A-SC)	-	···	---
0	-	···	0 (A-SC)	-	···	---
2	-	···	2 (S-SC)	-	···	---

Figure 2. I_D (A) and g_m (B) as a function of V_{GT} and I_D (C) and g_D (D) as a function of V_D



Single Transistor (L)			Self Cascode - $V_{B,MD}$ =2V (L_{MS}/L_{MD})			
V_B	30nm	110nm	V_{BMS}	30nm/ 30nm	110nm/ 110nm	30nm/ 110nm
-2	×	×	-2 (A-SC)	□	□	□
0	*	*	0 (A-SC)	◊	◊	◊
2	+	+	2 (S-SC)	▪	▪	▪

Figure 3. V_{EA} as a function of g_m/I_D ratio (A) and transconductance as a function of the voltage gain (B)

achieved. Obviously, such improved analog figures of merit are obtained at the cost of larger die area, but the A-SC implementation remains simple when compared to usually more complex analog design techniques used to boost the gain (while not always improving the transconductance).

V. Conclusion

In this work, simulations of analog figures of merit of UTBB single transistors and self-cascodes with different back biases reveal the improvements that A-SC associations can yield on the A_V - g_m trade-off. SC and back gate tuning combination provides a promising and flexible alternative for analog circuit design with the compromise on the occupied area.

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Impact of BOX thickness and Ground-Plane on non-linearity of UTBB FD-SOI MOS Transistors

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***Abstract*—This work investigates, for the first time, the impact of BOX thickness (T_{BOX}) and Ground-plane (GP) on the non-linearity of the transistors fabricated using UTBB FD-SOI CMOS technology. By extracting 2nd and 3rd order harmonic distortion, we have shown that the T_{BOX} scaling and GP improve the transistor linearity at lower drain currents (low-power applications) in advanced FD-SOI technology nodes. The physics behind this observation is explained in detail by using well calibrated TCAD simulations.**

I. Introduction

Ultra-thin body and BOX (UTBB) fully depleted Silicon-on-Insulator (FD-SOI) MOS transistors have emerged as a promising candidate for low–power mixed-signal systems like 5G communication and Internet of Things (IoT) [1]. The non-linearity is an extremely important Figure-of-Merit (FoM) for communication systems operating at Radio frequencies. The system-level linearization techniques require complex circuitry thereby emphasizing the need of transistors with very low non-linearity. In-spite of its importance, only few studies on UTBB FD-SOI MOS transistor's non-linearity have been reported till date [2]. In this work, we have discussed the impact of T_{BOX} and GP doping (N_{GP}) on the transistor non-linearity. First, we have discussed the additional mobility-limiting factors in UTBB devices by comparing experimental data with TCAD simulations. Then, 2nd and 3rd order harmonic distortions are extracted from the DC simulations and it is shown that lower non-linearity would be achieved in advanced technology nodes owing to the below discussed mobility limiting factors.

II. Mobility Limiting Factors

The UTBB FD-SOI nMOS transistor used in this work (shown in Fig. 1) has un-doped Silicon body with thickness (T_{Si}) of 8nm, T_{BOX} of 10nm and gate length (L_G) of 100nm (~3 times $L_{G,min}$, suitable for analog/RF applications). As shown in Fig. 2, Sentaurus TCAD simulator [3] was accurately calibrated using the measurement data from transistors fabricated using CEA-LETI's 28nm technology. The mobility model accounting for thickness dependence in thin-layer devices (TL) along with unified-mobility model, velocity saturation and quantum mechanical correction is used for accurate calibration. As shown in Fig. 2, mobility (i.e. I_D) increases significantly by switching-off the TL and surface roughness scattering (SRS) models. This emphasizes that the TL (due to the increased interaction between confined acoustic-phonon and electrons in thin-body devices [4]) and SRS (closeness of electrons to Si-SiO_2/HfO_2 interface) are major mobility-limiting factors in UTBB FD-SOI MOS devices.

To further study the impact of N_{GP} and T_{BOX} on effective electron mobility, the simulations are performed by varying one parameter at a time. The work-function difference induced increase in threshold voltage (V_{th}) with p-type GP is taken care of by plotting I_D as a function of (V_{GS}-V_{th}) (shown in Fig. 3). It is inferred from the I_D and g_m reduction that additional mobility degradation occurs with increase in N_{GP}. Note, this additional degradation is not observed once the TL and SRS models are switched-off hence confirming significant role of TL and SRS behind the mobility degradation. To understand the physics behind this observation, the electron-density inside the Si-body for different N_{GP} and at a constant I_D is extracted (shown in Fig. 4). With increase in p-type N_{GP}, the source-channel barrier at back-channel (near body-BOX interface) increases (because of higher work-function difference between the body and Substrate). This confines the electrons near the top-gate interface (channel shifts closer to the top-gate as shown in Fig. 4) resulting in an enhanced TL and SRS degradation.

To analyze the impact of T_{BOX} scaling, simulations are performed for T_{BOX} varying from 100nm down to 10nm for the devices with and without GP. Fig. 5 shows that I_D (i.e. mobility) does not degrade significantly as a function of T_{BOX} for the device without GP. But with GP, there is a significant degradation in I_D (i.e. mobility) with T_{BOX} scaling. Similar to the N_{GP} variation case, mobility degradation for thin BOX is due to higher TL and SRS (as the electrons move closer to the top-gate interface as depicted in Fig. 4). Note, the confinement is higher for devices with GP and scaled T_{BOX} thereby resulting in higher mobility degradation and lower I_D (seen in Fig. 5).

III. Non- Linearity

In order to study the transistor non-linearity, we have extracted 1st, 2nd and 3rd order derivatives of I_D with respect to V_{GS} viz. g_m, g_{m2} and g_{m3} respectively (Fig. 3 and 6). For a memory-less circuit excited with a sinusoidal signal of amplitude V_a, 2nd and 3rd order harmonic distortion are given as, $HD2=(1/4)*V_a*(g_{m2}/g_m)$ and $HD3=(1/24)*V_a^2*(g_{m3}/g_m)$.

Fig. 7 show the HD2 and HD3 variations with I_D for different N_{GP}. At low current levels, the improvement in

linearity (i.e. lower HD2 and HD3 as shown in the inset) is observed with increase in N_{GP} because of lower gm_2 (Fig. 6) and gm_3. The general non-linear increment in I_D with V_{GS} is linearized by the reduction in current (by V_{GS} dependent mobility reduction) as discussed in the previous section.

Similarly, Fig. 8 show that with reduction in T_{BOX}, HD2 and HD3 reduces, especially for low-current levels (shown for 0.1mA/µm). The linearity improvement with T_{BOX} scaling is achieved due to the additional (V_{GS} dependent) mobility degradation similar to the N_{GP} case. Note, the linearity improvement is higher in the case of device with GP compared to without GP. This is consistent with the higher mobility degradation behavior observed in the GP case as shown in Fig. 5.

IV. CONCLUSION

We have highlighted that thickness-dependent mobility and surface-roughness scattering are the major factors limiting the low and high-field mobility in UTBB FD-SOI MOS transistors. Additionally, we report that these factors will further limit the channel-carrier mobility in devices with thinner BOX and higher N_{GP}. By presenting the 2nd and 3rd order harmonic distortion, we pointed out that these factors will improve the transistor linearity in advanced FD-SOI technology nodes (scaled BOX and GP), especially when used in low-power domain.

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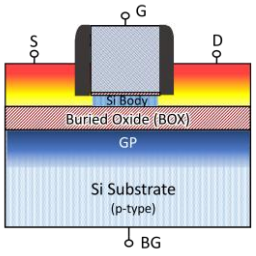

Fig.1. A schematic cross-section of UTBB FD-SOI nMOS transistor

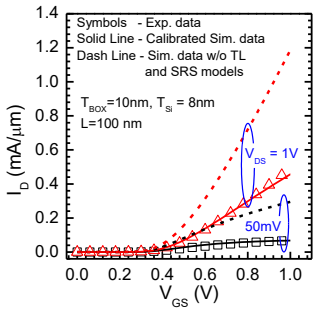

Fig.2. Matching of simulated I_D-V_G with the experimental data. In UTBB FD-SOI devices TL and SRS play a major role in limiting the mobility

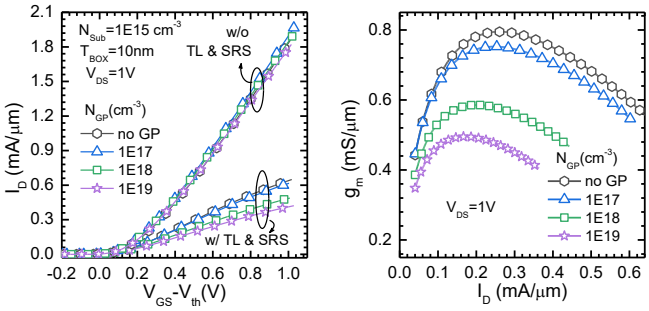

Fig.3. Variation of I_D-(V_{GS}-V_{th}) and g_m-I_D for different N_{GP}. At higher N_{GP} channel-carrier mobility is degraded due to enhanced impact of TL and SRS owing to electron-confinement closer to the top-gate interface

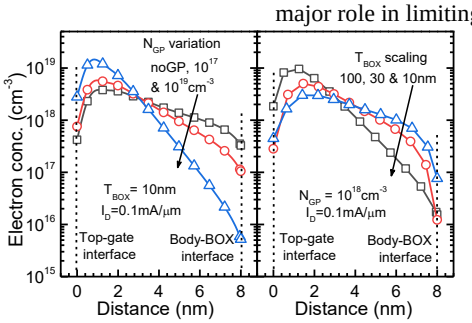

Fig. 4. Simulated electron-density profile within Si-body. Confinement of electrons near top-gate interface for higher N_{GP} and thin BOX leads to additional mobility degradation

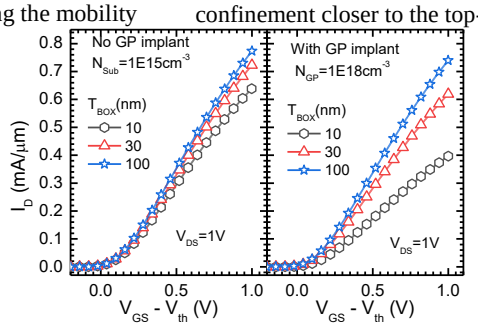

Fig. 5. Variation of I_D with (V_{GS}-V_{th}) for different T_{BOX}. I_D (i.e mobility) degrades with T_{BOX} scaling and the degradation is comparatively higher for device with GP

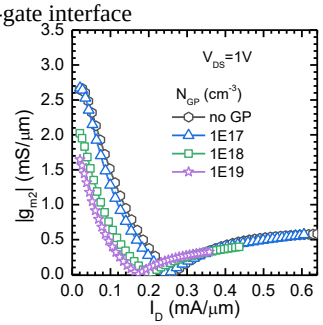

Fig. 6. Behavoir of d^2I_D/dV_G^2 as a function of I_D for different N_{GP}. For lower I_D range, g_{m2} reduces with increase in N_{GP}

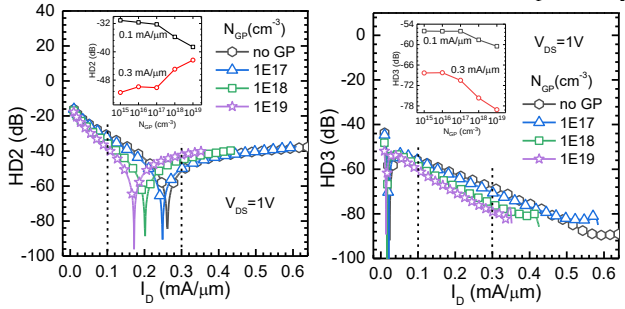

Fig. 7. Variation of HD2 and HD3 as a function of I_D for different N_{GP}. At lower current-levels, higher linearity (lower HD2 and HD3 as shown in the inset) is achieved with higher N_{GP}

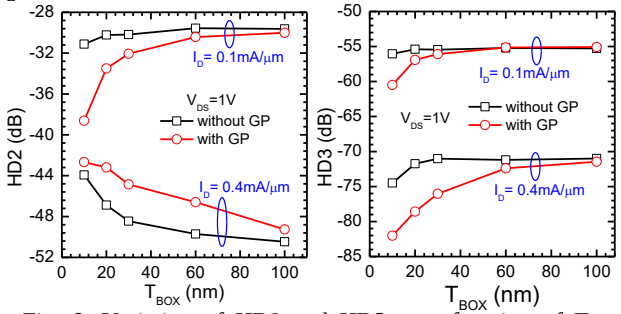

Fig. 8. Variation of HD2 and HD3 as a function of T_{BOX} extracted for different I_D. At lower current-levels (0.1mA/µm), higher linearity (lower HD2 and HD3) is achieved for the devices with thin BOX and GP.

Multilevel Parallelization Approach to Estimate Spin Lifetime in Silicon: Performance Analysis

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***Abstract*- We analyze the performance of a highly parallelized algorithm to calculate the spin lifetime in silicon thin films. The two-level parallelization algorithm is based on a hybrid parallelization approach, using the message passing interface MPI as well as OpenMP. Most efficient way to utilize the computational resources is described.**

Key words- Spin lifetime, MPI, OpenMP, Multi-Level Parallel Computing.

Now-a-days it is becoming possible to solve more and more complex problems, because high performance computational resources are widely accessible for the practical calculations. A lot of efforts have also been directed to utilize the computational power in the most effective way [1,2]. Practically, all systems that belong to TOP500 supercomputers are based on multi-core CPUs [3]. A considerable part of algorithms in physics can be effectively parallelized by dividing the domain into independent parts [4]. Each part can be calculated in a single MPI process without much efforts devoted to communication between separate MPI processes. Application of such approach is limited if each MPI process requires a lot of memory or intensive communication. In some cases, the memory requirements can be significantly reduced if the calculations are performed on a shared memory. For the class of problems for which shared memory can significantly reduce the total amount of memory requirements, a combination between MPI and OpenMP approach is quite promising [1,2,4].

Here we consider a problem of finding a spin lifetime (τ) in (001) ultra-thin silicon films subjected to [110] uniaxial tensile stress (ε_{xy}) [5-10]. The considered problem belongs to a class of problems that can effectively use shared memory to reduce an on-node memory requirements in the combination with weakly coupled domain decomposition. In our earlier work, a two-level parallelization algorithm to solve the problem has been mentioned [11]. At the first stage all static wave functions and energy data are calculated and archived in a binary file as a file-based cache technique which requires about 7GB for one stress point with high accuracy (Level 1). At the second stage the spin lifetime is calculated by loading and using these data in cache memory (Level 2). In this paper, we scrutinize the performance of the algorithm in every level and explain the most efficient way to utilize the resources.

The performance is measured on the Vienna Scientific Cluster (VSC-2) [12]. Each node of the cluster has 2 processors (AMD Opteron 6132 HE, 2.2 GHz and 8 cores) and 32GB main memory. We have examined different configurations of MPI and OpenMP with a fixed number of cores 96 (i.e. number of nodes is 6). A pure-MPI based configuration in Level 1 demands maximally around 5 GB memory per node, which can be perfectly fitted in any modern supercomputer. However, the calculation time increases, when the number of threads is increased and keeping a fixed number of cores (Fig. 1). Therefore, we find that our cache approach is most efficient for a pure MPI configuration.

In the second level, we compute τ by using the archived data in parallel. For variations in our discretization parameters (energy E and backscattering angle Φ), the size of the archived cache is shown in Fig. 2. The smaller E and Φ steps improve the computational accuracy but increase the required cache size. As this huge amount of cache is to be loaded into memory by each MPI job in Level 2, it becomes inevitable to use a hybrid MPI-OpenMP configuration for the spin lifetime computations. Fig. 3 shows maximum memory per node for 8 and 16 threaded MPI application. Each MPI process reads 7GB cache file, thus number of threads is limited by 8. The memory requirements of the application are mainly determined by the size of the serialized cache. The dependence of the total calculation time on the number of cores for a fixed threads number is shown in Fig. 4. Contrary to Fig. 1, increasing the thread numbers from 8 to 16 leads to decrease of the total calculation time for all values of the cores numbers.

This approach is tested with 416 cores and requires only around 40 min for a single relaxation time data point (around 280 core-hours). Finally, our computations show how shear strain can dramatically increase τ by orders of magnitude (Fig. 5).

ACKNOWLEDGEMENT

We acknowledge support from the journal Electronics. The computational results presented have been partly achieved using the Vienna Scientific Cluster (VSC).

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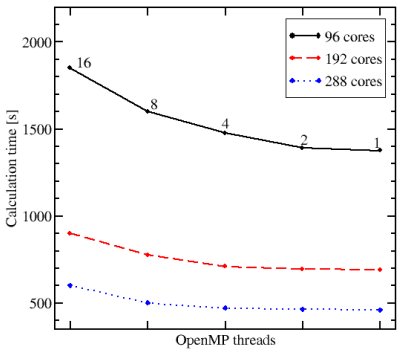

Fig. 1. Dependence of calculation time (Level 1) on different number of threads for a fixed core number is shown.

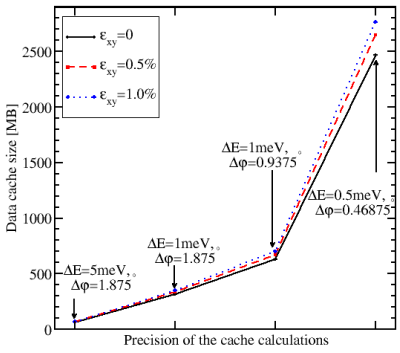

Fig. 2. Dependence of the size of cache on the precision of the calculations fixed by energy and angle steps for different ε_{xy} values is shown. Sample thickness t=1.5nm.

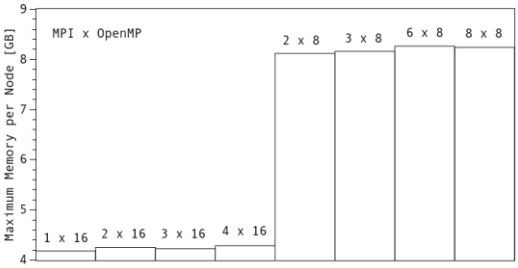

Fig. 3. Maximum required memory per node as reported by VSC-2 for different configurations is shown (Level 2).

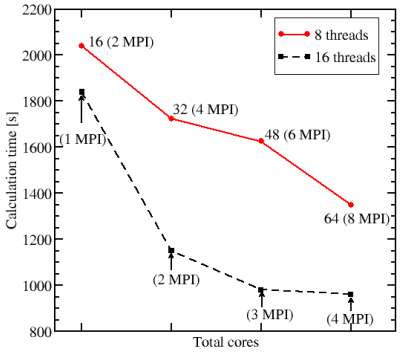

Fig. 4. Dependence of the total calculation time of the spin relaxation on total cores for 8 and 16 threads per MPI process.

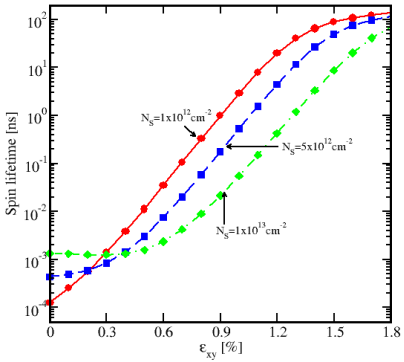

Fig. 5. Variation of spin lifetime with ε_{xy} is shown. t=1.36nm, and electron concentration N_s is a parameter.

Realization of Vertical Ge nanowires for Gate-All-Around transistors

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***Abstract*—Towards gate-all-around (GAA) FETs, we present the top-down realization of vertical Ge nanowires (NWs) with defect-free sidewall and perfect anisotropy. With optimized inductively coupled plasma-reactive ion etching (ICP-RIE) parameters, sub-60 nm diameter Ge nanowires are guaranteed. After RIE, digital etching is followed to further shrink the NW diameter. These NWs will form the base of vertical GAA transistors which are simulated by TCAD tools here. The processing techniques proposed in this work provide a viable option for low power vertical Ge and GeSn NW MOSFETs and Tunnel FETs.**

Keywords— Ge, top-down approach, nanowire, gate-all-around.

I. INTRODUCTION

As the Moore's law proceeds, continued device scaling has become challenging and unacceptable due to higher power consumption and less cost-effective. Recently GAA NW transistors have sparked research interest by offering extreme gate electrostatic control while suppressing leakage current to extend power scaling [1],[2]. For the ultimate CMOS architecture, vertical GAA NW approachs can excel in terms of device layout area, switching speed and power consumption [3],[4]. Even more, vertical NW design allows decoupling of footprint scaling from gate length scaling.

Ge and new emerging GeSn semiconductors are very promising for transistors because they offer, low carrier masses, high carrier mobility and potential direct bandgap [5],[6]. Vertical Ge or GeSn NWs can be synthesized by bottom-up approaches, e.g. the vapor-liquid-solid (VLS) method [7]. Nevertheless, top-down methods employ standard CMOS processing techniques and offer high reproducibility and precise control of NWs. Vertical Ge and GeSn NWs by top-down method have not been fully evaluated and should be comprehensively studied.

In this work, we demonstrate vertical integration of Ge NWs on Si substrate using the top-down approach. ICP-RIE and digital etching are explored to form smooth, thin and highly anisotropic NWs, which can be directly applied to fabricate vertical Ge GAA transistors, and potentially enable GeSn/Ge heterostructrue device applications.

II. EXPERIMENTAL METHODOLOGY

A strain-relaxed Ge layer on Si is used as substrate for NW formation. HSQ resist is spin-coated on Ge and serves as E-beam lithography and RIE mask. Systematic studies with various ICP-RIE parameters were conducted to form Ge NWs. Subsequently digital etching was used to eliminate the RIE-induced damage and further reduce the NW diameter. It's a high-precision etch process consisting of multiple cycles of self-limited O_2 plasma oxidation and HF rinse to remove oxide [8]. The techniques developed here offer a robust way for further vertical NW GAA transistors fabrication.

III. RESULTS AND ANALYSIS

The influence of various etching parameters on the profile of Ge NWs was studied, which finally result in optimized NWs with perfect anisotropy as well as minimal under-cutting and micro-trenching effect. Fig. 1 presents well-defined Ge NWs with D = 60 nm and 100 nm. After ICP-RIE, the digital etching is developed, which consists of two steps: formation of GeO_2 by O_2 plasma at room temperature; oxide removal in diluted HF. By repeating these two steps, the Ge NWs can be thinned in a highly controlled way as indicated in Fig. 2. After 9 cycles, the Ge NWs diameter is reduced from 60 nm to 47 nm (Fig. 2). All defined NWs after digital etching exhibit smooth sidewall and reduced surface roughness. The etching thickness of Ge NW versus the number of cycles shows a linear fit with the extracted etching rate of ~0.75 nm per cycle (Fig. 2c).

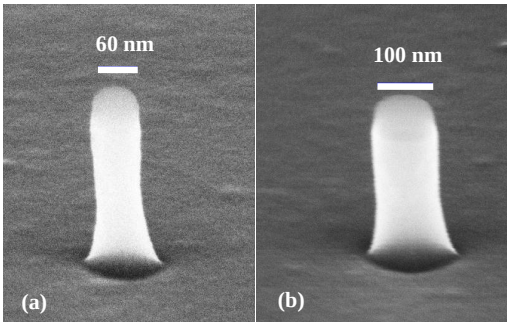

Fig. 1 Tilted SEM images of vertical Ge NWs etched with optimized ICP-RIE conditions (HSQ resist mask is on top): (a) vertical Ge NW with D = 60 nm, (b) D = 100 nm.

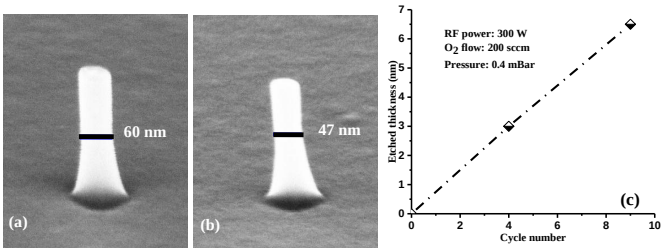

Fig. 2. Tilted SEM images of (a) vertical Ge NWs with D = 60 nm as shown in Fig. 1a. (HSQ is removed) (b) NW profile after 9 cycles digital etching. (c) Radial thickness reduction of Ge NWs as a function of cycles number.

The vertical NW formation by combination of ICP-RIE and digital etching is the first step toward the fabrication of GAA transistors. To better obtain the device guideline, we carry out the TCAD simulation of Ge NW junctionless transistor. Simplified models, e.g. the high-field velocity saturation, doping-dependent bandgap narrowing, are applied, which can capture the basic electrical behavior of transistors [7], [9]. Three working regimes of on-state, partial depletion, and depletion are presented in terms of carrier density distribution in the channel (Fig. 3). On-state regime occurs when the gate bias is below the flat band voltage, leading to carriers being distributed throughout the whole channel. At the partial depletion regime, the conductive path is concentrated at the center of nanowires, while the channel is fully depleted at off-state.

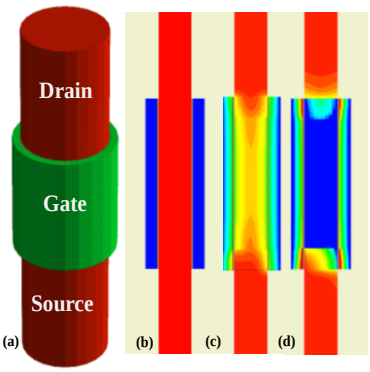

Fig. 3. (a) Sketch of Ge NW junctionless transistor with uniform channel doping (5×10^{18} cm^{-3})and D = 20 nm. (b)-(d) Cross-sectional schematic of carrier density in NW devices. The transistor operates in 3 regimes: (b) on-state: the carriers are filled within the whole channel, (c) partial depletion: conductive path is concentrated at the center of the channel, (d) depletion: the channel is fully depleted.

Fig. 4a shows I_{DS}-V_{GS} curves of Ge junctionless transistors with diameters ranging from 10 nm to 50 nm with a p-type channel doping of 5×10^{18} cm^{-3}. As the diameter is shrunk to 10 nm, the device shows a high Ion/Ioff $>10^8$, which underlines the great potential of GAA NW, while the NW transistors with diameters of 50 and 40 nm exhibit inferior Ion/Ioff ratio due to the difficulty to deplete the channel. The doping influence on the performance is also shown for the 20 nm diameter NW GAA device (Fig. 4b). Decreasing the channel doping is beneficial for switching off the devices but leads to a relatively low Ion. This indicates a trade-off between Ion and device switching, which provides the guideline for device fabrication: with higher doping in the NWs, the NW diameter needs to shrink to obtain decent electrical performance of junctionless transistors.

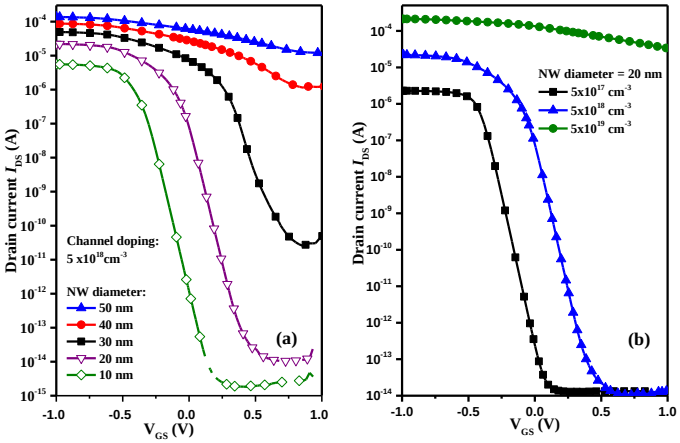

Fig. 4. Simulated I_{DS}-V_{GS} transfer curves of vertical Ge junctionless transistors: (a) comparison of devices with different diameters at a fixed doping concentration of 5×10^{18} cm^{-3}, (b) comparison of transistors with various doping concentration at the diameter of 20 nm.

IV. Conclusion

In this work, vertical Sub-50 nm Ge NWs with smooth sidewall and perfect anisotropy have been realized by optimized ICP-RIE and multiple cycles of digital etching. Design requirements of targeted GAA devices were obtained from TCAD simulation, which investigated the impact of NW diameter and channel doping on the electrical performance. The techniques mentioned here serve as guidelines for future vertical Ge and GeSn-based GAA transistors.

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Scaling down a level shifter circuit in 28 nm FDSOI Technology

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I. Introduction

The miniaturization of MOSFET largely contributed to the benefit of microelectronics industry over the past few decades. What Gordon Moore predicted in 1965 [1], that definition kept on modifying in the following decades without changing much of the original statement. Subthreshold operation has become a research focus for power constrained digital systems in recent years.

Level shifter circuit is essential for most of the microelectronics systems to communicate with the peripheral modules. Several designs have been proposed in different technologies over the years. However, the challenge is to scale those circuits down to 28 FDSOI technology, since the linear scaling is not possible. Wilson current mirror (WCM) based level shifter is one of such designs [2] which paved its way for a lot of topologies thereafter. In our work, we propose a different scaling procedure for such circuits.

II. Scale down procedure

The primary task here, was to find the design space where we will apply the method. We fixed the minimum value of the channel length at 48 nm for the convenience of layout. In FDSOI technology, the transistor width can not be reduced below 80 nm. These two values denote the lower bound of the corresponding search space. For the upper bound, dimensions from the 65 nm design were chosen. To evaluate the circuit performance, propagation delay t_{pd}, total switching energy E_{gate}, static power dissipation P_{stat} and noise margin NM were selected. To measure t_{pd}, the second edge of the input pulse was chosen so that it ensures the circuit is capable of performing the voltage shift. In order to reduce the complexity of the search, the robustness was considered as the constraint for the Pareto selection. Therefore, the noise margin value is restricted to as low as 90 mV.

The circuit contained five transistors. Therefore, we had ten variables to deal with. After the initial run, it was observed that only few variable have dominating effect on the performance of the circuit. It is worth mentioning that the circuit is capable of generating a desired output only when the lengths of P3 and N3 were maintained at 48 nm. Table I contains the final range, within which the circuit can perform as desired.

It was observed that, when the optimization process was run with three metrics, it generated a huge set of Pareto points.

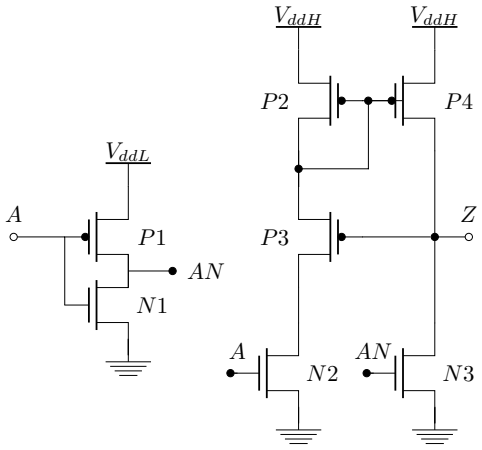

Fig. 1. based level shifter schematic [2]

TABLE I. Working Range of the Transistor Dimensions

Transistor	$\mathbf{W}_{\max}$ [µm]	$\mathbf{W}_{\min}$ [µm]	$\mathbf{L}_{\max}$ [µm]	$\mathbf{L}_{\min}$ [µm]
P2	0.200	0.800	0.400	0.800
P3	0.080	0.360	0.048	0.048
P4	0.200	0.320	0.050	0.065
N2	0.160	0.800	0.048	0.060
N3	0.160	0.480	0.048	0.048

If we take an example of the width of P2 transistor, wp1 from the figure 1, we can see the search results ran with the variation of wp1 in Figure 2. It is clearly visible that there are plenty of points between 200nm and 800nm where the circuit can behave optimally. So we needed to customized the search

As a result, any two parameters were chosen among t_{pd}, E_{gate} and P_{stat} for finding the Pareto front. The benefit is visible in the figure 3.

III. Results and Conclusion

The final set of data was chosen by intersecting the sets of data from figures 3(a) and 3(b). The dimension set with the minimum possible values are finalized for the circuit. Table II shows the comparison of the dimensions across the technologies.

Considering the importance of time to market in current era, the above procedure can be useful for scaling down

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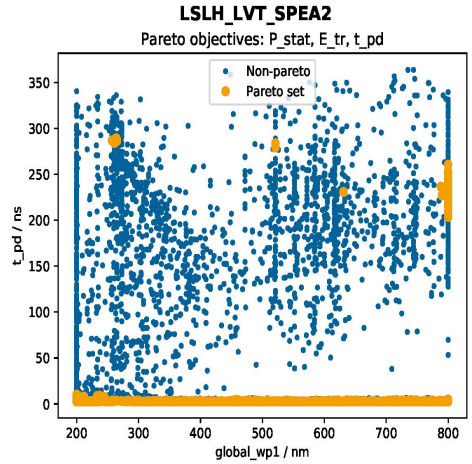
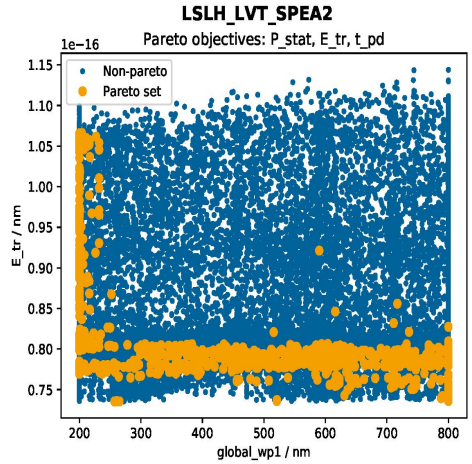
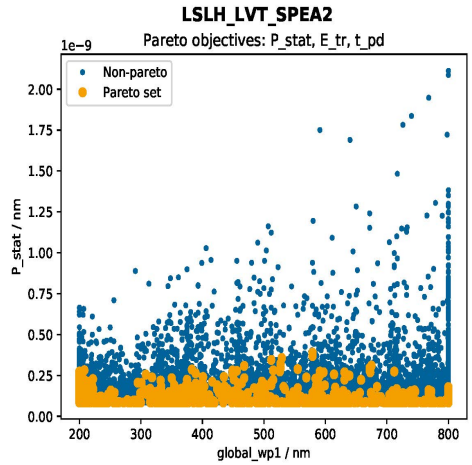


(a) Propagation delay w.r.t. wp1



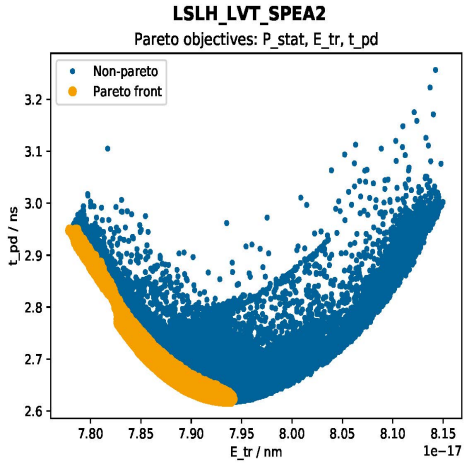
(b) Energy per transition w.r.t. wp1



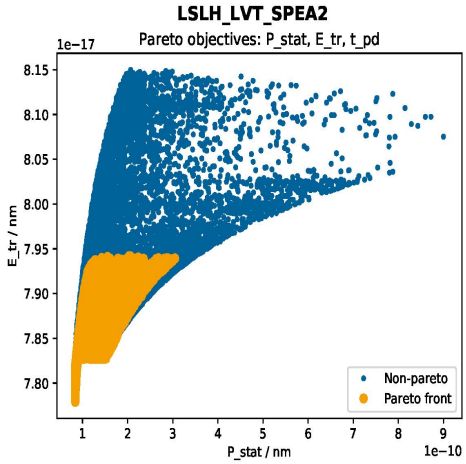
(c) Static power dissipation w.r.t. wp1

Fig. 2. Pareto search with wp1 varying from 200 nm to 800 nm

standalone essential circuits into deep nanotechnologies such as 28 nm FDSOI.



(a) Propagation delay w.r.t. transition energy



(b) Energy per transition w.r.t. static power dissipation

Fig. 3. Final Pareto front

TABLE II. TRANSISTOR SIZE

Transistor	90 nm		65 nm		28 nm	
	Width [µm]	Length [µm]	Width [µm]	Length [µm]	Width [µm]	Length [µm]
P2	0.180	4.700	0.180	4.200	0.762	1.200
P3	0.180	0.150	0.180	0.090	0.080	0.048
P4	0.180	0.200	0.180	0.500	0.200	0.060
N2	0.180	0.330	0.180	0.190	0.160	0.048
N3	0.600	0.330	0.180	0.190	0.160	0.048

IV. ACKNOWLEDGEMENT

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Linear Distortion Analysis of 3D Double Gate Junctionless Transistor with High-k Dielectrics

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***Abstract*—In this paper we have investigated the nonlinearity distortion of junctionless transistor. In order to ensure minimum intermodulation and higher order harmonics at the system output, different linearity parameters like Second Order Voltage Intercept Point, Third Order distortion, Third Order Input Intercept Point and Third Order Intermodulation Distortion are evaluated. The effect of high-k gate dielectric on the junctionless transistor linearity has also been calculated. Deterioration of the linearity is observed for the high-k gate dielectrics in junctionless transistor.**

Keywords—Junctionless transistor; high-k; non-linear distortion; VIP2; VIP3; IMD3; TCAD

I. INTRODUCTION

Scaling of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices improves the packing density, decreases power requirement. It helps to achieve high speed and reduce costs of ICs. But the reduction in size of the devices also contributes to new problems called as short channel effects [1]. Concept of metal oxide semiconductor transistor structure with no junctions was firstly given by J. P. Colinge *et al*. in 2009 [2]. This junctionless transistor is basically an accumulation mode transistor and acts like a gated resistor. Investigations in recent years showed that junctionless transistor has advantages over conventional MOSFETs and been projected as an alternative for deep submicron technology [3-7].

Linearity is an essential requirement for all RF systems to ensure the minimum intermodulation and higher order harmonics at the system output. In order to maximize the sensitivity of the RF systems higher performance of the device in terms of transconductance, linearity, and distortion is required. So, high linearity with high transconductance is the present demand for low noise communication systems. In this context, linearity distortion analysis of the junctionless transistor is crucial. Further, the effect evaluation of different high-k gate dielectrics is essential for future technology. To describe the non-linear phenomena of the device we have analyzed the higher order transconductance coefficients and other figure of merits like VIP2 (Second Order Voltage Intercept Point), VIP3 (Third Order distortion), IIP3 (third order input intercept point), and IMD3 (third order intermodulation distortion). Since JLT is an emerging device and no proper nonlinear behavior analysis is available, we have investigated the JLT nonlinear performance in this paper. The effect of high-k gate dielectrics has also been included.

II. DEVICE STRUCTURE AND SIMULATION STRATEGY

A thin body double gate JLT with 20 nm gate length [8] is considered for our investigation. The 3D structure of double gate junctionless transistor is shown in Fig. 1. The device structural dimensions and parameters are mentioned in TABLE I. Though the channel is narrow, heavy doping of the channel is used to get high on-current flow. A poly-silicon gate material with 4.4 eV work function is used in the device. Synopsys TCAD is used to design, simulate and data extraction. Different tools like 3D device structure editor, Sdevice and Svisual are used. However, different models are also combined to estimate the mobility accurately.

TABLE I. DEVICE DESIGN PARAMETERS OF THE JUNCTIONLESS TRANSISTOR

Parameters	**Values**
Gate Length (L_g)	20 nm
Gate Width (W)	12 nm
Channel Thickness (T_{si})	10 nm
Doping of the channel (N_D, N_A)	1.5×10^{19} cm^{-3}
Donor	Arsenic
Front Gate Oxide Thickness (T_{oxf})	1 nm
Back Gate Oxide Thickness (T_{oxb})	1 nm
Gate oxide type	SiO_2, Si_3N_4, HfO_2,
Gate metal type	Poly-Si

III. RESULTS AND DISCUSSION

The transfer characteristics of junctionless transistor with polysilicon gate and different gate oxides are shown in Fig. 2(a). g_{m1} is transconductance of the device and g_{m2} and g_{m3} are the higher order derivatives of the transconductance. g_{m1}, g_{m2}, and g_{m3} are denoted as $\partial I_D / \partial V_{GS}$, $\partial^2 I_D / \partial V_{GS}^2$, and $\partial^3 I_D / \partial V_{GS}^3$, respectively. The harmonic distortions in MOS devices are present due to the nonlinearity of these higher order components. Hence, their amplitude should be minimized and VIP2, VIP3, and IIP3 should be as high as possible. Further low value of IMD3 causes low distortion. Fig. 2(b), Fig. 2(c) and Fig. 2(d) show the first order, second order and third order transconductance of junctionless transistor with SiO_2, Si_3N_4 and HfO_2 gate oxide.

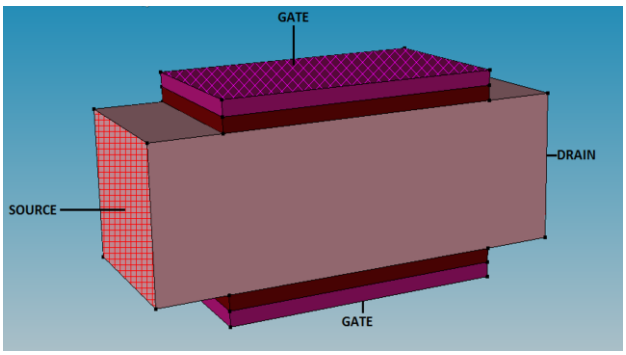

Fig. 1. 3D structure of double gate junctionless transistor.

The VIP2, VIP3, IIP3 and IMD3 are mathematically defined as

$$VIP2 = 4 \times \frac{g_{m1}}{g_{m2}} \tag{1}$$

$$VIP3 = \sqrt{24 \times \frac{g_{m1}}{g_{m3}}} \tag{2}$$

$$IIP3 = \frac{2}{3} \times \frac{g_{m1}}{g_{m3} \times R_S} \tag{3}$$

$$IMD3 = [\frac{9}{2} \times (VIP3)^3 \times g_{m3}]^2 \times R_S \tag{4}$$

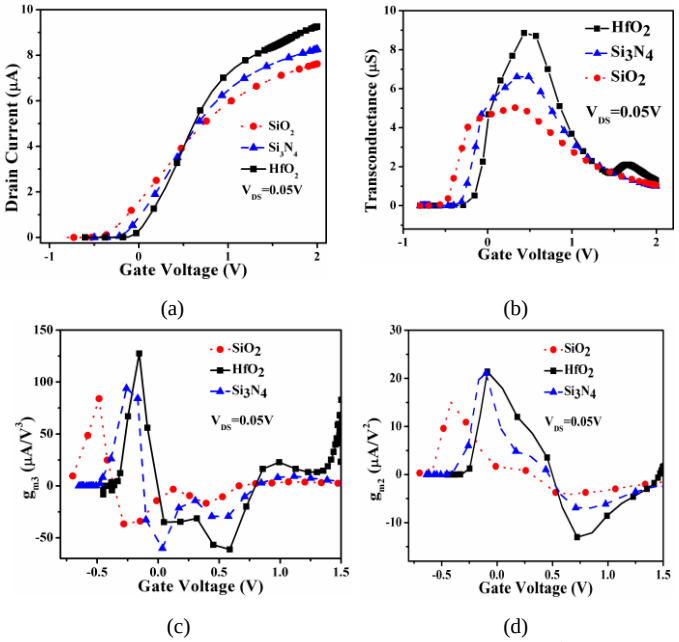

Fig. 2. (a) I_D-V_{GS} characteristics (b) g_{m1} (c) g_{m2} (d) g_{m3} of junctionless transistor with polysilicon gate and different gate dielectrics.

JLT with HfO_2 has lower VIP2 value. JLT with SiO_2 shows higher VIP3 for all gate voltages compared to Si_3N_4 and HfO_2. Variation of VIP2 and VIP3 characteristics with applied gate voltage in the JLTs are shown in Fig. 3(a) and Fig. 3(b), respectively. The IIP3 variation with applied gate voltage for JLTs is shown in Fig. 3(c). Though IIP3 should be high for high linearity of the device, JLT with HfO_2 has encountered low IIP3 value for all gate voltages. For all the gate voltages in Fig. 3(d), lower IMD3 value is observed in JLT with HfO_2 gate oxide. Lower value of IMD3 is always desired to achieve less intermodulation distortion. So, intermodulation distortion is comparatively less in case of the JLT with HfO_2.

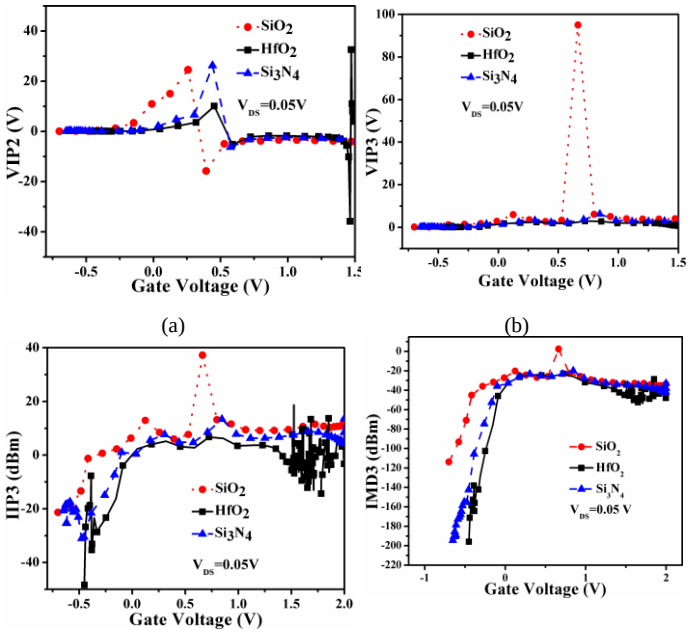

Fig. 3. (a) VIP2 (b) VIP3 (c) IIP3 (d) IMD3 of junctionless transistor with polysilicon gate and different gate dielectrics.

IV. Conclusion

This paper presents a detail linearity distortion analysis of junctionless transistor. As VIP2 for JLT increases with the gate voltage in the subthreshold region, it becomes more linear. But VIP2 is constant at higher gate voltage. Application of high-k gate dielectric does not have any improvement on linearity. JLT with HfO_2 shows lower values of VIP2, VIP3 and IIP3 compared to Si_3N_4 and SiO_2. But lower value of IMD3 in JLT with HfO_2 confirms less intermodulation distortion. JLT with SiO_2 shows overall better linearity.

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InSb Nanocrystals Containing SOI Structures: Preparation and Properties

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***Abstract*—The InSb nanocrystals embedded in buried SiO_2 layer of a SOI structure were obtained by the In^+ and Sb^+ ion implantation into the SiO_2 layers thermally grown on Si wafers followed by the hydrogen transfer of a Si film and high-temperature annealing. Transmission electron microscopy, energy dispersive spectroscopy, Raman spectroscopy and photoluminescence (PL) were used to study the structure properties. The spherical shaped InSb nanocrystals bimodal size-distributed on the depth close to ion profiles were obtained. The TO-LO splitting obtained in the Raman spectra from the InSb nanocrystals was 3 cm^{-1} less than that from the monocrystalline InSb, and was discussed in the frames of decreasing the transverse dynamic effective charge, as well as that of the surface phonon influence. The obtained PL peak at the 1524 nm (0.81 eV) corresponds to the quantization energy in the InSb nanocrystals of about 13 nm size.**

Keywords- silicon-on-insulator, InSb, nanocrystals, ion implantation, Raman scattering, photoluminescence

I. INTRODUCTION

The incorporation of A_3B_5 semiconductor performance advantages in the mature complimentary metal-oxide-semiconductor technology is a way to realize the silicon-based optical interconnection. From this point of view, InSb nanoctructures attract particular interest because of their excellent electrical and optical properties resulting from their very small electron and hole effective masses and very high permittivity. Nanometer-sized InSb nanocrystals demonstrate their photoluminescence in the region 1.6-1.8 μm [1], a large optical absorption edge blue shift from the infrared to ultraviolet spectral region [2], and an enhanced nonlinear optical coefficient [3]. The narrow band gap and the high electron and hole mobility at room temperature makes it suitable for short-channel transistor applications, too.

The nanostructures properties depend on the preparation method [1-3]. The ion-beam synthesis is a method in which new phases formation occurs in ion-irradiated layers. The ion-beam synthesis consists of the ion implantation and subsequent high-temperature annealing of ion-implanted samples. These two steps are the standard manufacturing operations in the current silicon technology. Previously, we studied the InSb nanocrystal formation conditions as well as the structural properties of the InSb nanocrystals synthesized within the buried SiO_2 layers and at the Si/SiO_2 bonding interface of silicon-on-insulator (SOI) structures [4, 5]. The two-stage mechanism of InSb phase formation, including the antimony precipitation followed by In and Sb atoms diffusion, was obtained. Under these conditions, the InSb nanocrystals grow as a liquid phase followed by the crystallization under cooling. The difference of the atom density in liquid and solid InSb phases, as well as different thermal expansion coefficients of InSb nanocrystals and the surrounding matrix, can result in the respective In-Sb bond stresses. In the present paper, the optical properties of InSb nanocrystals ion-beam synthesized in buried SiO_2 layers were studied.

II. EXPERIMENTAL

The InSb nanocrystals in the buried SiO_2 layers of SOI structures were formed by a technique described elsewhere [5]. In^+ and Sb^+ ions at the energy of 200 keV and doses 8.0×10^{15} were embedded into the 300 nm thick SiO_2 films thermally-grown on p-type, (100)-oriented Si wafers by oxidation in a wet oxygen ambient at the temperature of 1100° C. The ion implantation parameters produced Gauss-like In and Sb atom distributions with the peak concentrations ~1.2×10^{21} cm^{-3} at a depth of about 110 nm below the top surface. H_2^+ ions at an energy of 140 keV to the dose of 2.0×10^{16} cm^{-2} were incorporated into another Si wafer. Then, in a vacuum chamber, the wafers were joined with the implanted sides, simultaneously detaching the Si layer over the internal hydrophobic surface created by H_2^+ ions and transferring this silicon layer onto the first wafer. The transferred silicon film thickness was about 600 nm. Then the wafers were cleaned and cut in small pieces which were heat-treated at a temperature of 500 – 1100° C for 0.5 hour in the N_2 ambient. Transmission electron microscopy (TEM), Raman spectroscopy and photoluminescence (PL) were employed to study the produced layer properties.

III. RESULTS AND DISCUSSION

Beginning with the annealing temperature of 800°C, the nanocrystal formation in the buried SiO_2 layer occurred. Both the nanocrystal distribution and their dimensions depended on the annealing temperature. As the annealing temperature grew from 800 to 1100°C, the mean

nanocrystal diameters increased from 5-15 to 13-25 nm respectively, and their distribution changed nonmonotonically. The largest nanocrystals are generally located close to the top Si/SiO_2 interface. The interplanar spacing of the nanocrystal lattice is about 0.374 nm and that corresponds to the (111) InSb lattice orientation.

No evidence of the In-Sb optical phonon mode was obtained in the Raman spectra from the as-implanted samples, as well as from the samples annealed at temperatures below 800°C. As the annealing temperature reached 800°C, a broad scattering band ranging between 180 cm^{-1} and 200 cm^{-1} appeared. The next increase in the annealing temperature to ≥900°C resulted in this Raman scattering band intensity growth. In addition, within this band, two peaks at about 187 cm^{-1} and 195 cm^{-1} become sharp.

The obtained LO-like and TO-like modes in the nanocrystals are high-frequency shifted by 4.3 cm^{-1} and 7.3 cm^{-1}, as compared to these in monocrystalline InSb (190.7 cm^{-1} and 179.7 cm^{-1}, respectively). The observed high-frequency shifts of the In-Sb mode suggest that the In-Sb bonds in the ion-beam synthesized nanocrystals must be stressed. However, the experimentally observed frequency shift is an effective value resulted from both the In-Sb bond stress and the optical phonon localization in the nano-sized InSb crystals. In order to separate these two effects contributions to the frequency shift, the Raman spectra of the InSb nanocrystals were calculated within the phonon confinement model [6]. It was obtained for the nanocrystals larger than 10 nm, the LO and TO modes approach practically their respective values in the bulk crystalline InSb matrix. It suggests the experimentally observed Raman frequency shift is generally provided by the In-Sb bond stresses. The relative lattice constant expressed in terms of the atom density in liquid and solid InSb phases was estimated. It is about -1/3%. The TO-LO splitting obtained from the Raman spectra of the ion-beam synthesized InSb nanocrystals was 3 cm^{-1} less than that from the unstressed bulk monocrystalline InSb. The obtained effect is discussed in the frames of decreasing the transverse dynamic effective charge, as well as that of the surface phonon influence.

The room-temperature PL spectra were recorded in the visible spectral range both from the as-implanted sample and those heat-treated at a temperature of 800-1100 °C under the excitation laser wavelength of 325 nm. The high-intensity PL band peaked at 361 nm (3.43 eV) was excited after annealing at 800 °C. Its intensity grew as the annealing temperature increased to 900 °C. A further increase in the annealing temperature to 1100 °C was accompanied by a drop of this PL band intensity.

The PL peaks intensity correlation with that of the Raman peaks suggests the connection between the radiation recombination centers and the formed InSb phase. However, the violet emission does not originate from the quantum-confinement effect because of the large energy shift. In addition, its energy position remains invariable as the annealing temperature growth. Usually, this emission band origin is attributed to the electron-hole recombination via the energy level of the oxygen-definition defects in the silicon dioxide matrix. An analogous structure, modified by substituting one or two silicon atoms by In or Sb atoms, can be realized at the interface between an InSb nanocrystal and surrounding matrix.

The PL spectra were measured at the temperature of 10 K in the infra-red spectral region ranged from 900 to 1600 nm, too. The excitation wavelength was 488 nm. The high intensity PL band composed of three narrow peaks around 1210 nm (~ 1.0 eV) was excited from the as-implanted samples. As the annealing temperature grew to 800 °C, the emission band diminished. An increase in the annealing temperature to 900 °C was accompanied by the appearance of a new narrow PL peak at 1526 nm (0.81 eV). The observed PL peaks remained invariable as the annealing temperature was raised to 1000 °C.

The origin of the strong infrared PL band (between 1100-1400 nm) observed just after the implantation of In and Sb ions can be also attributed to the radiative recombination in silicon dioxide via the defect levels. Its inverse dependence intensity on the annealing temperature is an argument in favor of this mechanism. However, the nature of this centre needs further investigations. The PL peak formation at 1526 nm (0.81 eV) correlates also with an increase in the Raman scattering on the optical phonons in InSb nanocrystals. Its energy position corresponds to the quantization energy in the InSb nanocrystals of about 13 nm in size.

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Detailed analysis of frequency-dependent impedance in pseudo-MOSFET on thin SOI film

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***Abstract*—This paper reports detailed measurements of impedance in frequency domain and discusses the mechanisms affecting the ac response of pseudo-MOSFET method for SOI wafer with thin SOI film. The interplay between capacitance, channel resistance and contact resistance is demonstrated. Solutions for obtaining reliable C-V curves are proposed.**

(key words) pseudo-MOSFET; split-CV; impedance; contact resistance

I. INTRODUCTION

Recently, ac measurements with pseudo-MOSFET method have been performed and applied to characterize the electrical property of the interface between SOI film and BOX layer [1][2]. The impedance (Z) is implicitly used to obtain the basic components of series and parallel circuit models in ac measurement: capacitances (C_S=-1/(2πf·Imag(Z)), C_P=Imag(Z^{-1})/(2πf)), resistance (R_S=Real(Z)) and conductance (G_P=Real(Z^{-1})),. By analyzing the frequency dependence of measured impedance Z(f) directly, the mechanisms affecting the ac response of pseudo-MOSFET can be clarified. This abstract reports systematic measurements of the impedance and phase in the frequency domain (40Hz-2MHz).

II. EXPERIMENTAL SETUP

Figure 1 shows the schematic of pseudo-MOSFET method used in our measurement. The polarity of SOI wafer is p-type for both SOI and substrate. The SOI and BOX layer thicknesses are 88 and 145 nm, respectively. Si islands were isolated on SOI film. Low-resistance contact between the back surface of SOI wafer and the metal chuck was achieved by applying vacuum [2]. The four probes loaded onto the SOI film are grounded. The dc voltage V_G and superimposed ac signal (with 20 mV amplitude) are applied to the substrate of the SOI wafer, which works as a gate terminal in pseudo-MOSFET method. Keysight 4294A precision impedance analyzer

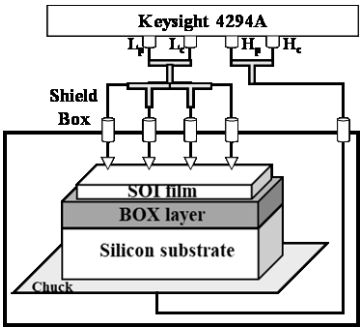

Figure 1. Schematic of pseudo-MOSFET method to measure the impedance.

is used to measure the frequency dependence of the impedance by sweeping the frequency from 40Hz to 2MHz at each gate voltage V_G.

III. MEASUREMENT RESULT

Figure 2 shows C_P-V_G and Z-V_G characteristics measured with one single probe. The applied frequency is 40Hz. Typical C_P-V_G curves are obtained (Fig. 2a) and confirm earlier results with pseudo-MOSFET method [1]. Threshold (V_{TH}) and flatband (V_{FB}) voltages extracted from the inflection points are 2.8V and -1.8V, respectively.

The absolute value of measured impedance |Z| and the phase θ are shown in Fig. 2b. It is clear that resistance component of measured impedance becomes dominant around V_{TH} and V_{FB} since the phase is nearly 0°. The phase expected for pure capacitor (-90°) is not reached. Even for the case of applying high gate voltage (strong inversion/accumulation, reflected by the capacitance saturation in C_P-V_G curves (Fig. 2a), the phase of measured impedance is 75-85°, lower than -90°. This result indicates a large resistive component in measured impedance that is comparable to the impedance induced by the capacitance of BOX layer (C_{BOX}).

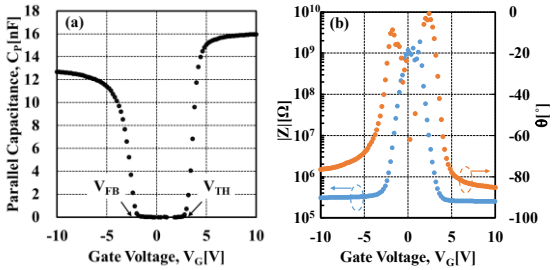

Figure 2. (a) Capacitance C_P-V_G and (b) amplitude |Z|-V_G and phase θ of impedance versus gate voltage measured with one probe at 40 Hz

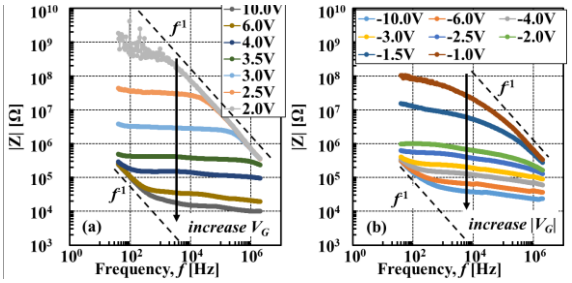

Figure 3. Frequency dependence of the impedance for variable V_G: (a) electron channel, (b) hole channel.

Figure 3 shows the frequency dependence of measured impedance as a function of V_G in accumulation and inversion modes. The shape of the curves further documents the influence of the resistive component observed in Z-V_G of fig. 2. An impedance plateau, almost independent of applied frequency, is visible in both cases of positive and negative voltages. Since the impedance of pure resistor does not depend on the applied frequency, these plateaus correspond to a dominating resistive components.

There are two regions where |Z| inversely depends on frequency. The one observed at low frequency for large V_G is due to C_{BOX}, that is connected in series with resistive component. The other observed at high frequency for low V_G is due to parasitic capacitance between the probes. At intermediate gate voltage, from around V_{TH} or V_{FB} to the value leading to capacitance saturation, the measured impedance is governed by the resistive component and no 1/f dependent component could be observed. This result indicates that C_P-V_G near V_{TH} and V_{FB} is ruled by resistance, not by inversion capacitance. Method to eliminate the resistive component is needed to extract the precise inversion or accumulation capacitance, which reflects the amount of trap concentration and carrier density, in time-dependent measurements with pseudo-MOSFET.

To analyze the resistive component in detail, the resistance values were extracted with Cole-Cole plot [3] as a function of V_G. Fig. 4 shows that the resistance value becomes on the order of MΩ around V_{TH} and depends on

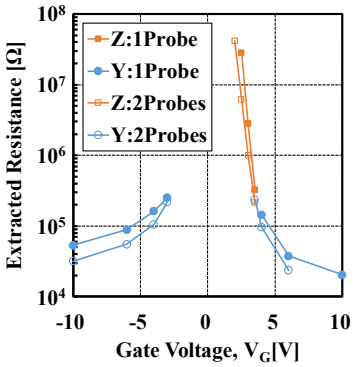

Figure 4. Extracted resistance value of the resistive component as a function of V_G.

the number of probes. The resistive component of the impedance includes the resistance of the inversion charge as well as the contact resistance (R_C) between the probe and SOI layer. We will present a model able to discriminate these values.

Time constant of the series circuit consisting of C_{BOX} and R_C becomes on the order of millisecond to second, which is comparable to that of the interface trap [4], at V_G between V_{TH} and V_{FB}. Indeed, the magnitudes of C_{BOX} and R_C are over 10nF and 100k-100MΩ, as observed in figs. 2 and 4. As a result, this suggests that long delay time is required to ensure static condition when measuring current I_D or capacitance characteristics, at V_G between V_{TH} and V_{FB}.

IV. Conclusion

The frequency-dependence of measured impedance is useful to analyze the physical mechanism affecting the ac response of pseudo-MOSFET with thin SOI film. The concept of the equivalent circuit and its components was clarified experimentally. The problems induced by contact resistance and channel resistance were revealed. To obtain reliable results with pseudo-MOSFET method, in particular at V_G around V_{TH} and V_{FB}, the influence of the contact resistance must be treated carefully.

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Potential of Thin (∼10 nm) HfO_2 Ferroelectric FDSOI NCFET for Performance Enhancement in Digital Circuits at Reduced Power Consumption

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Abstract- The use of HfO_2 as a ferroelectric in NCFETs is attractive for its high switching speed and compatibility with existing fabrication techniques [1]. Several studies on the use of HfO_2 as a ferroelectric have been reported [2]–[4]. Although these existing studies do highlight the immense potential HfO_2 has as a ferroelectric, to the best of our knowledge, a comprehensive study of HfO_2 FDSOI NCFET at the gate level has not been reported. In this paper, a detailed study of performance of thin HfO_2 ferroelectric FDSOI NCFETs is reported for digital applications along with average power consumption. The FDSOI NCFET has been used to build 3-stage ring oscillators and 2-input universal gates, namely, NAND and NOR gates. A comparison has been made with the same circuits made using FDSOI MOSFETs (baseline devices). The baseline devices are FDSOI MOSFETs with Partial Ground Planes (PGP FDSOI MOSFET) as shown in Fig. 1(a) [5]–[7]. Both baseline devices and NCFETs are identical in all respects except the gate stack [Fig. 1(b)]. The devices have a metal gate length of 20 nm. The silicon layer thickness is 5 nm and the BOX thickness is 10 nm. The PGPs are located 6 nm from source/channel and drain/channel junctions with same dimensions as in [5]. The silicon layer which forms the channel is intrinsically doped (10^{15} cm^{-3}). The source and drain are degenerately doped (10^{20} cm^{-3}). The simulations of baseline devices have been performed using Silvaco ATLAS TCAD [8]. 2D electrostatics obtained from TCAD were used to simulate an FDSOI NCFET by implementing 1D Landau-Khalatnikov equation in MATLAB [9]. The Landau coefficients of HfO_2 used in this study have been obtained from [2]. The circuits comprising of 3-stage CMOS ring oscillator, a 2-input NAND gate driving an inverter and a 2-input NOR gate driving an inverter were simulated using Synopsys HSPICE using a look-up table approach [10]. The propagation delay, τ_p was based on the charge-current relationship [11].

The transfer characteristics (I_D vs. $V_{GS,TOP}$) of the baseline FDSOI MOSFET and FDSOI NCFET with increasing ferroelectric thickness (T_{FE}) are shown in Figs. 2(a) and 2(b) at $\mid V_{DS} \mid$=0.5 V. FDSOI NCFETs used for our study have a T_{FE} of 10 nm HfO_2 as ferroelectric. No hysteretic behaviour of FDSOI NCFET was observed at this thickness of HfO_2. While FDSOI NCFETs with a T_{FE} of 20 nm did not show hysteresis in DC simulations, hysteresis was observed at the circuit level for this thickness of HfO_2 ferroelectric. This is consistent with the behaviour reported in [12]. The output characteristics (I_D vs. V_{DS}) of the FDSOI n-NCFET and FDSOI p-NCFET (T_{FE}=10 nm) are shown in Figs. 3(a) and 3(b) respectively. The output characteristics of the baseline FDSOI n-MOSFET and FDSOI p-MOSFET are shown in Figs. 4(a) and 4(b) respectively. The threshold voltage was determined using the constant current method at a drain current of 100 μA/μm. Thus, the threshold voltage of baseline FDSOI n-MOSFET is 0.5 V and that of FDSOI n-NCFET is 0.34 V. The threshold voltage of FDSOI p-MOSFET is -0.5 V and the threshold voltage of FDSOI p-NCFET is -0.3 V. The performance of FDSOI NCFET gate was studied at V_{DD} of 0.5 V which is also the threshold voltage of the baseline device. Further, the comparison of FDSOI NCFET gate with the baseline gate was also done at V_{DD} ranging from 0.5 V to 0.9 V.

For obtaining gate delay, our model assumption was that intrinsic capacitance, C_{int}, of the NAND gate scales with gate capacitance and we have assumed $C_{int,NAND-2} \simeq C_G$ and external capacitance, C_{ext} being input capacitance of inverter loading the gate which is C_{ext} = $C_{GS,n}$ + $C_{GS,p}$ + $C_{GD,n}$(1-A_V) + $C_{GD,p}$(1-A_V), shown in Fig. 5. The worst case input pattern for NAND-2 was assumed for obtaining τ_{PHL}(A=1, B=0→1) and τ_{PLH}(A=1, B=1→0). The ferroelectric capacitance, C_{FE} was calculated as $C_{FE} \approx 1/(2\alpha T_{FE})$ as outlined in [13]. For FDSOI NCFETs, the effective C_{GS} and C_{GD} ($C_{GS,eff}$ and $C_{GD,eff}$) were calculated as series combination of $C_{GS,BL}$ (or $C_{GD,BL}$) and C_{FE}, where $C_{GS,BL}$ and $C_{GD,BL}$ are gate-to-source and gate-to-drain capacitances of the baseline FDSOI MOSFETs.

For the analysis of gates, the frequency of the input signal was varied from 5 kHz to 20 GHz at reduced V_{DD} of 0.5 V to draw a comparison of performance vs. power between FDSOI NCFET and FDSOI MOSFET based gates, which is consistent with results in Table I. The 3-stage FDSOI NCFET ring oscillator frequency at V_{DD} of 0.5 V was observed to be 71 GHz. Table II shows the results of performance and power consumption of FDSOI NCFET and baseline MOSFET based NAND-2 gates as function of V_{DD}. It is clearly seen that for comparable performance of FDSOI NCFET (V_{DD}=0.5 V) and baseline (V_{DD}=0.7 V) gates, the average power consumption of FDSOI NCFET gate is significantly lower (∼63%) in comparison to the baseline gate. This is true for other values of V_{DD} also for given performance. Similar results were obtained for NOR-2 gates. The paper will present detailed results on performance and power consumption of thin HfO_2 ferroelectric FDSOI NCFET universal gates.

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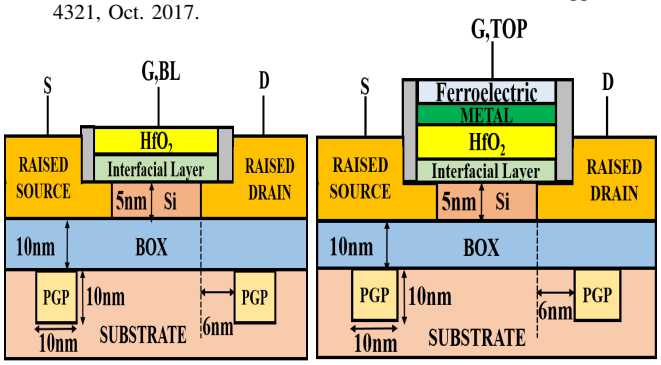
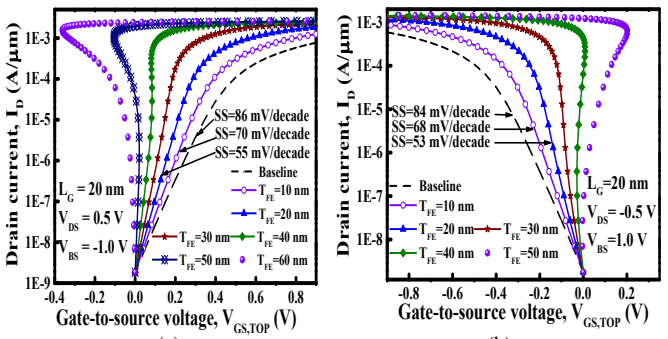


(a) (b)

Fig. 1. (a) Schematic of PGP FDSOI MOSFET (baseline MOSFET) as proposed in [5]. The metal gate length is 20 nm. HKMG is used as gate stack with an EOT of 0.9 nm. (b) Schematic of PGP FDSOI NCFET with ferroelectric (HfO_2) in gate stack. For baseline MOSFET, $V_{GS,TOP}$=$V_{GS,BL}$.



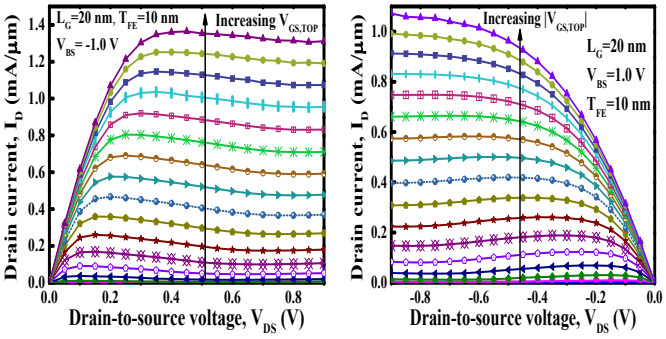
(a) (b)

Fig. 2. Transfer characteristics of FDSOI (a) n-NCFETs and, (b) p-NCFETs, at | V_{DS} | of 0.5 V, with varying T_{FE} of HfO_2. The subthreshold swing (SS) improvement can be clearly seen in FDSOI NCFETs.

TABLE I

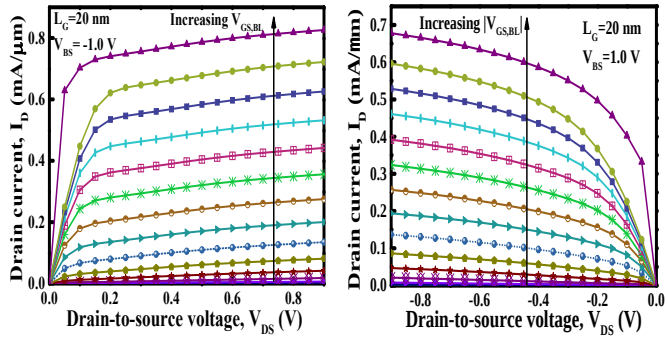
PERFORMANCE OF 3-STAGE RING OSCILLATORS

V_{DD} (V)	$f_{osc,BL}$ (GHz)	$f_{osc,NCFET}$ (GHz)
0.5	21	71
0.6	46	106
0.7	73	138
0.8	99	163
0.9	120	181



(a) (b)

Fig. 3. Output characteristics of FDSOI (a) n-NCFETs and, (b) p-NCFETs, T_{FE} = 10 nm, with increasing | $V_{GS,TOP}$ |, | V_{BS} | = 1 V.



(a) (b)

Fig. 4. Output characteristics of baseline FDSOI (a) n-MOSFETs and, (b) p-MOSFETs, with increasing | $V_{GS,BL}$ |, | V_{BS} | = 1 V.

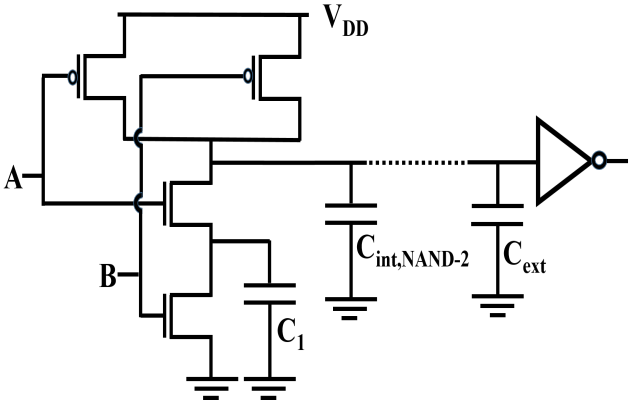


Fig. 5. Schematic of NAND-2 gate followed by an inverter showing the intrinsic and external capacitances of NAND-2 which have been considered to evaluate the performance of the gate.

TABLE II

PROPAGATION DELAY AND AVERAGE POWER CONSUMPTION FOR NAND-2 GATES USING FDSOI NCFETS AND BASELINE DEVICES. THE SIGNAL FREQUENCY IS 20 GHZ.

V_{DD} (V)	$\tau_{p,BL}$ (ps)	$\tau_{p,NCFET}$ (ps)	$P_{avg,BL}$ (μW)	$P_{avg,NCFET}$ (μW)
0.5	7.05	2.35	8.86	11.15
0.6	3.3	1.67	13	16
0.7	2.15	1.4	17.69	18.52
0.8	1.67	1.22	23	28
0.9	1.41	1.12	29	35

Three P-Silicon Layers in Reliblale Lateral Double Diffused Metal Oxide Semiconductor Transistor

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***Abstract*— Inserting three p-layers in the drift region and buried oxide of the Lateral Double Diffused MOSFET (LDMOS) is the main goal of this paper. One of these layers is considered in the drift region and two others are in the buried oxide. Moreover, these layers have different lengths. The new structure helps to have high breakdown voltage and low on-resistance that improves Figure Of Merit (FOM) in this power transistor. Also, replacing p-silicon layer instead of silicon dioxide under the drift region reduces lattice temperature and helps to have a reliable device. The electrical parameters of the novel structure are compared with the conventional one using ATLAS simulator.**

Keywords- LDMOS, Breakdown voltage, Specific on-resistance, Temperature.

I. INTRODUCTION

Nowadays power transistors are attracted by electronic industries for the high voltage applications. The breakdown voltage and specific on resistance are two main parameters in power transistors especially in lateral double diffused metal oxide semiconductors (LDMOSs) [1, 2]. Using silicon-on-insulator technology [3] in power transistors improves vertical breakdown voltage but in high breakdown voltage the devices suffer high temperate [4]. The insulator acts as a barrier for heat transfer and in the active region, the temperature increases which change the electrical characteristics such as drain current, mobility, off current and so on [5].

In this paper, a new LDMOS structure is proposed that high breakdown voltage occurs in lower temperatures. The purpose is achieved using three silicon P-layers in the device. These layers have different lengths. The first layer is considered in the drift region and the others are located in the buried oxide. The P-layers have high doping density than the drift region. This condition causes low specific on resistance and reduced lattice temperature in the device. Also, the breakdown voltage increases due to the different P-layers in the device. The new structure which is named as Three P^+ Layers in LDMOS Transistor (TPL-LDMOS) is simulated using two dimensional ATLAS simulator [6] and compared with Conventional LDMOS (C-LDMOS) structure.

II. DEVICE STRUCTURE

The schematic cross section of the proposed structure is shown in Fig. 1. As it is clear, three silicon P-layers are considered in the drift regions and buried oxide like steps. The channel and drift lengths are 5 µm and 18 µm, respectively. The buried oxide and top silicon thicknesses are 0.4 µm and 0.6 µm. The P-layers 1, 2 and 3 lengths are 6 µm, 12 µm and 18 µm, respectively and their thicknesses are 0.2 µm. the channel and drift doping densities are 1×10^{17} cm^{-3} and 1×10^{16} cm^{-3}. The doping density of Source/drain is 1×10^{20} cm^{-3}. Moreover, the P-layers doping density is 1×10^{18} cm^{-3}.

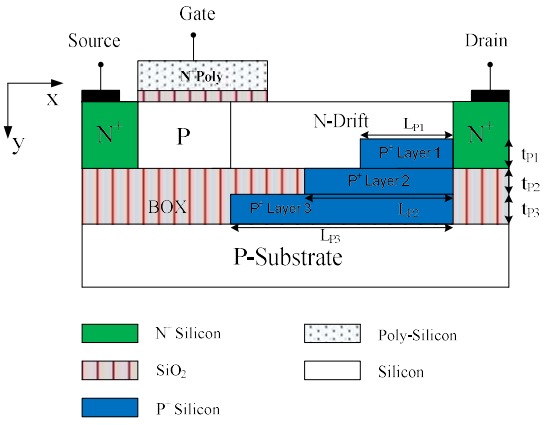

Figure 1. The schematic of TPL-LDMOS.

III. RESULTS AND DISCUSSION

Considering P-layers in step form creates new peaks in the electrical field profile reducing the main peaks. So, the breakdown voltage increases. Fig. 2 shows the breakdown voltage versus drift length for both the proposed structure and the conventional one. The figure proves that the proposed structure has higher breakdown voltage.

As it was mentioned, the main peaks of electric field are reduced in the proposed structure. So, the electron temperature reduces. Fig. 3 shows the electron temperature for the proposed structure and the conventional one. It is clear that this temperature is significantly reduced in TPL-LDMOS.

Silicon has higher thermal conductivity than SiO_2. In the proposed structure, silicon P-layers are considered instead of part of the buried oxide. So, the lattice

temperature can be reduced. The lattice temperature along drift region is plotted in Fig. 4 for the proposed structure and the conventional one. The figure shows that TPL-LDMOS has smaller lattice temperature achieving more reliable device.

The on-resistance is an important parameter in transistors. Reducing on-resistance can be a goal for achieving better drain current. This parameter can be reduced by increasing the doping density. Considering silicon P-layer with higher doping density in the drift region reduces the on-resistance. Fig. 5 shows the specific on-resistance versus drift length for TPL-LDMOS and C-LDMOS. It is clear that the proposed structure has smaller on-resistance.

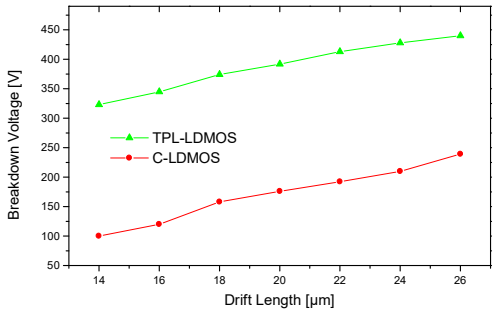

Figure 2. The breakdown voltage for the proposed and conventional structures.

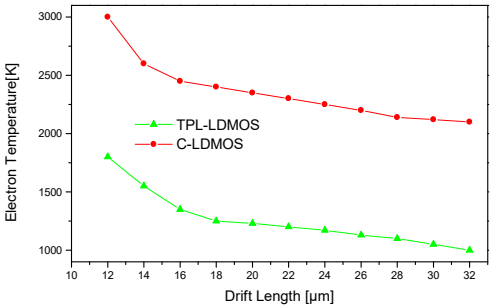

Figure 3. Electron temperature for for the proposed and conventional structures.

By reducing on-resistance and increasing the breakdown voltage, Figure Of Merit is improved. Moreover, more reliable device is achieved which can be used in power applications.

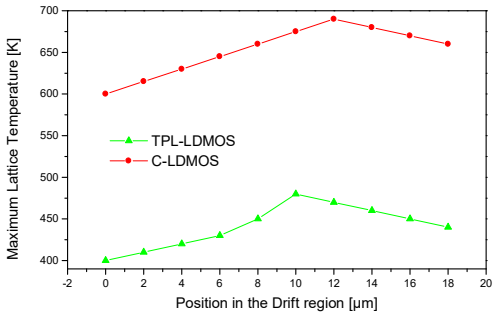

Figure 4. Maximum Lattice temperature for the proposed and conventional structures.

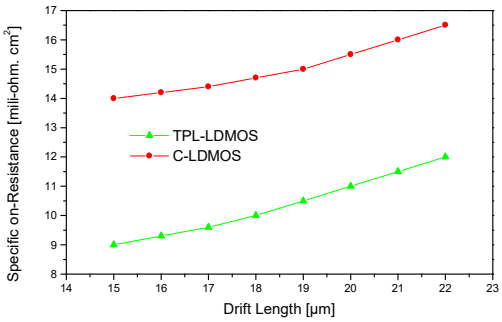

Figure 5. Specific on-resistance for the proposed and conventional structures.

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Inserting PN Junction in a Power Device for Achieving Improved Figure Of Merit

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***Abstract*— lateral double diffused metal oxide semiconductor field effect transistors (LDMOS) in silicon on insulator (SOI) technology are widely applied in power applications. The breakdown voltage is high in these devices. In this paper a new LDMOS is presented to improve the performance achieving more reliable device. The idea is based on considering two silicon layers (P-type and N-type) in drift and insulator regions, respectively. The simulation with two dimensional ATLAS simulator shows that the breakdown voltage is increased. Moreover, the specific on-resistance and lattice temperature are improved. So, the Figure Of Merit (FOM) is significantly improved.**

Keywords- Lateral Double diffused Metal Oxide Field Effect Transistor, Silicon On Insulator, Breakdown voltage, Lattice temprature.

I. INTRODUCTION

Lateral Double Diffused Metal Oxide Semiconductor Field Effect Transistors (LDMOSFET) are widely used in RF power amplifiers [1, 2]. The performance of these devices is increased using Silicon On Insulator (SOI) technology [3, 4]. During last decade many researchers have attempted to improve the performance of SOI LDMOSFET. Extending the buried oxide into the drift region can increase the breakdown voltage [5]. Creating local minimum by changing the structure of source region can improve the kink effect [6].

In this paper, a new SOI LDMOSFET is proposed to improve its application. In the new structure which is called SP-LDMOS, two silicon layers are applied. The first one which is N-type is considered in top of insulator under the channel and the drift regions. The second one (P-type) is considered in bottom of drift region. The added layers create new peaks reducing the main peaks achieving more uniform electric field. So, the breakdown voltage increases. The P-type layer in drift region with higher doping density decreases the on-resistance. Moreover, the N-type layer in the insulator has better conductivity that leads to reducing the lattice temperature. The Simulation with ATLAS simulator [7] represents the superiority of the proposed structure.

II. DEVICE STRUCTURE

The schematic of the proposed structure is presented in Fig. 1. As it is clear in the figure, an step P-type layer is considered in the bottom of the drift region. Moreover, the N-type silicon layer is placed in top of insulator region under channel and drift regions. The channel, drain and source lengths are 2 µm, 3 µm and 3 µm, respectively. d_s and d_p are 0.2 µm, o.3 µm. Drift length is 8 µm. silicon thickness and buried oxide thickness are 5 µm and 4 µm. P-type and N-type doping densities are 1×10^{18} cm^{-3}. Drift region, source, drain and channel doping densities are 1×10^{16} cm^{-3}, 1×10^{20} cm^{-3}, 1×10^{20} cm^{-3} and 1×10^{18} cm^{-3}.

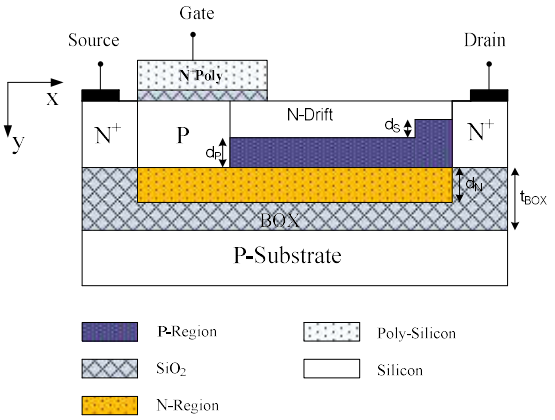

Figure 1. The schematic cross section of the proposed LDMOS

III. RESULTS AND DISCUSSION

In this section, the results of ATLAS simulation are discussed. In Fig. 2 the horizontal electric field is plotted for the proposed structure and the conventional one. Considering the P-type layer in the drift region in step form creates a new peak in the electric field profile reducing the main peaks. So, more uniform electric field is obtained for the proposed structure. Moreover, reducing the main peaks leads to increasing the breakdown voltage. Fig. 3 shows the breakdown voltage for both the proposed and the conventional structures. As it is clear in the figure, this voltage for the proposed structure is higher than the conventional one. For drift

length of 8 µm, this voltage is about 200 V for the proposed structure and 75 V for the conventional one.

Small specific on-resistance is desirable in LDMOSFETs. This resistance has a reverse relation with doping density. So, considering P-type layer in drift region with higher doping density than drift region reduces on-resistance as it is shown in Fig. 4.

For reducing the lattice temperature, N-type layer is considered instead of part of insulator layer. Silicon has higher thermal conductivity than SiO_2. So the heat can be transferred reducing the lattice temperature. Fig. 5 shows the lattice temperature for the proposed and conventional structures. As it is clear in this figure, this temperature is significantly reduced in the proposed structure.

It is concluded that the Fugure Of Merit (FOM) is significantly improved by reducing on-resistance and increasing breakdown voltage.

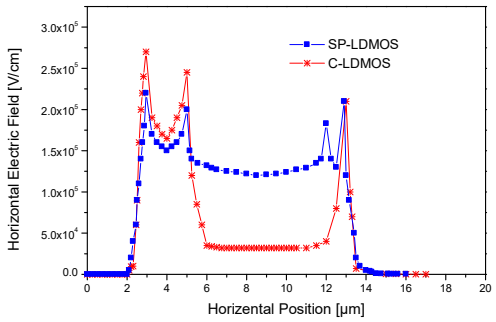

Figure 2. The horizontal electric field for the proposed and the conventional structures.

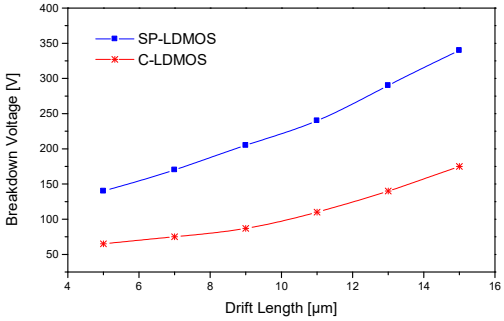

Figure 3. The breakdown voltage for the proposed and conventional structures.

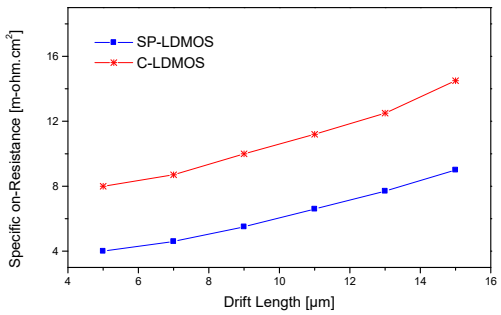

Figure 4. The specific on-resistance for both the proposed and conventional structures.

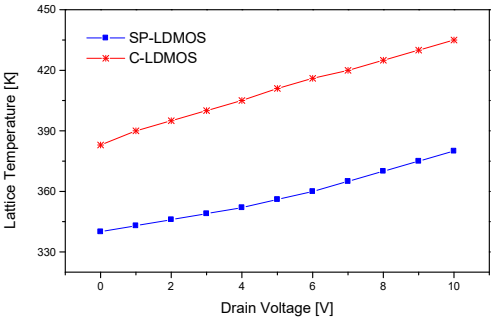

Figure 5. The lattice temperature for both the proposed and conventional structures.

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Design of Wideband Cascode Low Noise Amplifier using E-mode GaN based MOS-HEMT for RF and Microwave Applications

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***Abstract*— In this paper a wideband Cascode Low Noise Amplifier (LNA) is designed using Verilog-A models and different passive components. The look up table (LUT) based Verilog-A models are developed for gate recessed GaN based MOS-HEMT and HEMT with reference to TCAD simulation results. The models are incorporated into Cadence EDA tool in order to use in circuit simulations. The RF, noise and linearity performances of the GaN MOS-HEMT based LNA have been investigated and compared with GaN HEMT based LNA.**

Keywords - GaN; LUT; MOS-HEMT; TCAD; Verilog-A

I. Introduction

GaN HEMT is emerged as a front runner technology for RF front-end receiver design due to its high breakdown voltage, high power density, high frequency, high efficiency, better linearity and low noise operation [1-3]. Due to high power handling capability of the device the GaN HEMT LNA circuit does not require any protection circuit and hence suitable for low area and low cost. Most of the developed AlGaN/GaN based HEMTs and MOS-HEMTs are depletion type due to unique material properties of GaN which leads to spontaneous and piezoelectric polarizations for 2DEG formation at the heterointerface [2-3]. Although depletion mode HEMTs are applicable for microwave power amplifiers, low noise and RF switching devices, enhancement-mode (E-mode) MOS-HEMT [4-5] has added advantages in simpler circuit design and low power consumption due to elimination of negative power supply [5] which is best suitable for RF IC design. So in this work a LNA is designed using E-mode GaN MOS-HEMT and different performances of the circuits are analyzed by developing a look up table (LUT) based Verilog-A model.

II. Device Structure and Verilog-A Model

Figure 1 represents the 2D structure of E-mode GaN MOS-HEMT. In order to reduce the different parasitic capacitances and resistances a double decked T-shaped gate structure is proposed. The device has a gate length (L_g), gate to source spacing (L_{gs}), gate to drain spacing (L_{gd}), and gate recess depth of 60 nm, 0.9 µm, 0.9 µm and 15 nm respectively.

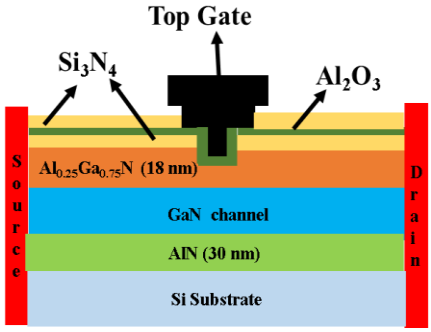

Figure 1. Cross-sectional view of single gate GaN MOS-HEMT

The Verilog-A model consists of LUTs in a tabular form and each LUT is again splitted into inputs and outputs individually. The DC characteristics of the device are defined in the LUT by considering inputs as gate voltage (V_{gs}) and drain voltage (V_{ds}) and the outputs by drain current (I_{ds}). Also the radio frequency (RF) and noise performance of the circuit is being mentioned in the LUT by considering frequency along with the bias voltages *i.e.* V_{gs} and V_{ds} as inputs and S_{11}, S_{12}, S_{21} and S_{22} as outputs. The developed LUT based Verilog-A model is then incorporated into Cadence circuit platform in order to design the wideband LNA.

III. Design and Simulation of Wideband LNA

Figure 2 shows the designed differential Cascode LNA which consists of a source coupled pair designed by the common source input MOS-HEMTs (M_6 and M_7). In order to maintain wide bandwidth two common gate MOS-HEMTs (M_4 and M_5) are connected in Cascode to the source coupled MOS-HEMT (M_6 and M_7) which reduces the Miller effect. Two source follower MOS-HEMTs (M_{10} and M_{12}) are used to buffer the output of

the LNA. In order to maintain the wide bandwidth shunt feedback resistance and capacitors are used which increases bandwidth in the expense of gain.

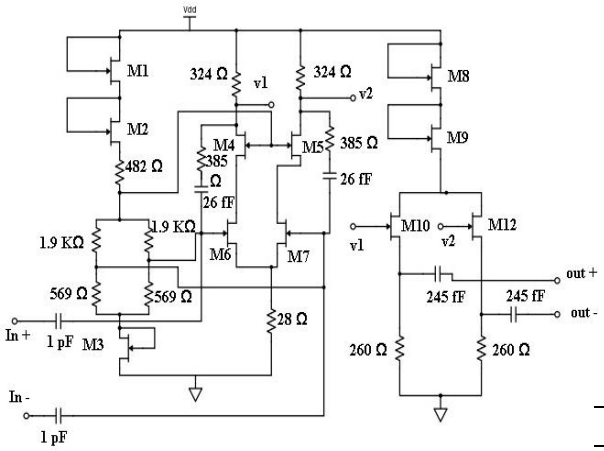

Figure 2. Schematic diagram of wideband Cascode LNA using GaN MOS-HEMT

Figure. 3 represents the S-parameter and noise Figure simulation of the designed LNA. It shows a maximum gain of 24 dB at frequency of 26 GHz with variation of gain of 1 dB in the frequency range of 10-40 GHz. It also shows minimum input and output return loss of -15 dB and -6 dB at a frequency of 23 and 39 GHz. The noise Figure of the LNA is between 1 dB and 3 dB from 10 GHz to 40 GHz. Due to low noise resistance of GaN MOS-HEMT the deviation between NF and NF_{min} is very small as shown in Figure 3. So there is not any significant penalty for noise mismatching. Similarly Figure 4 shows variation of gain with respect to P_{in} for different f_{in}. It shows the input referred 1dB compression point of the designed LNA which varies from -15 to -12.5 dBm along the frequency range of 10 GHz to 40 GHz. Table 1 compares the RF and noise performance between GaN MOS-HEMT and HEMT LNA. It shows GaN MOS-HEMT based LNA shows better RF and noise performance.

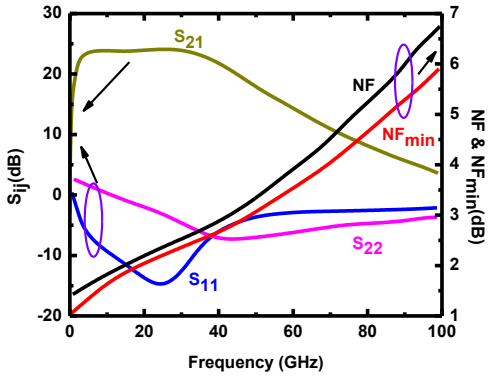

Figure 3. S-parameters and Noise Figure variation of LNA with respect to different frequencies

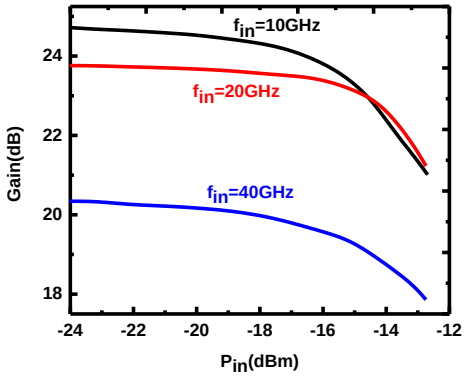

Figure 4. Variation of gain with respect to P_{in} for different f_{in}

TABLE I. COMPARISON OF DIFFERENT PARAMETERS BETWEEN GAN HEMT AND MOS-HEMT LNA AT 25 GHZ

Parameters	*GaN MOS-HEMT LNA*	*GaN HEMT LNA*
S_{11}(dB)	-15	-10
S_{22}(dB)	-6	-5
S_{21}(dB)	24	16
NF_{min}(dB)	2.4	3.1

IV. CONCLUSION

A LUT based Verilog-A model has been developed for GaN HEMT and E-mode MOS-HEMT which are incorporated in Cadence circuit platform. Both the device models are used for designing a wideband Cascode LNA for comparing the performance analysis of the circuit. It is concluded that GaN MOS-HEMT LNA shows better intrinsic gain (S_{21}) of 24 dB, lower input and output return losses of -15 dB and -6 dB respectively. It has relatively lower minimum Noise Figure of 2.4 dB at 25 GHz as compared to GaN HEMT LNA. Hence GaN based MOS-HEMT can be suitably useful in RF and microwave applications.

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Analytical Model Development for Gate Workfunction Engineered Short Channel E-mode n-Polar GaN MOS-HEMT

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***Abstract*— In this paper an enhancement mode (E-mode) short channel n-polar GaN MOS-HEMT is proposed. In order to mitigate different short channel effects, work function engineering technique is applied to the gate electrode by incorporating single, double and triple materials gate. An analytical model for surface potential and electric field is developed for the device and validated with TCAD simulation results. It is observed that device with triple material gate shows better control of short channel effects as compared to single and double material gate based devices.**

Keywords-GaN; MOS-HEMT; n-Polar; SCE; TCAD; Work function

I. INTRODUCTION

GaN HEMT has been emerged as potential candidate for high power, high frequency and low noise applications due to the unique material properties of GaN. By aggressively scaling down the gate length of GaN HEMT, the device can be operated in THz frequency range [1]. In recent years there has been significant progress in high-frequency GaN HEMTs by scaling down the gate length to 20 nm and by reducing parasitic drain and source resistances by integrating source/drain regrowth [3]. These devices are by default normally 'on' due to its inherent material properties. Different techniques are reported in various literatures to obtain normally-off GaN HEMT operations. But when the gate length is scaled down the device becomes normally "on". Normally-off devices are attractive due to elimination of negative power supply which simplifies the circuit design.

N-polar GaN HEMT technology is also emerged as an attractive candidate for ultra-scaled normally-off device. Additionally providing electron confinement, it offers many alternative advantages for transistors for high-frequency operation of GaN HEMT. N-polar GaN HEMTs with a top gate insulator and wide bandgap AlN back-barrier induces charges at bottom, provides a device structure similar to UTB-SOI (Ultra-Thin Body Silicon on Insulator) MOSFET. Hence it has potential advantages in scaling down to 20 nm technology [3].

However, scaling down of gate length of the device into deep sub-micron (DSM) regions results in increase in short channel effects (SCEs) which in turn affects the RF performance of the device and also suppress the modulation and carrier transport efficiency [3]. Therefore in order to overcome these limitations a novel device structure is required to neglect the high electric field produced at the drain side by reducing SCEs in addition improving the modulation and carrier transport efficiency. Many researchers have proposed different gate engineering techniques in device in order to minimize the SCEs and improved carrier transport efficiency [4]. In this work a noble E-mode triple material gate n-polar GaN MOS-HEMT is proposed. An analytical model of surface potential and electric field is developed first time for GaN MOS-HEMT and is validated with TCAD simulation results.

II. E-MODE N-POLAR GAN MOS-HEMT STRUCTURE AND MODEL DEVELOPMENT

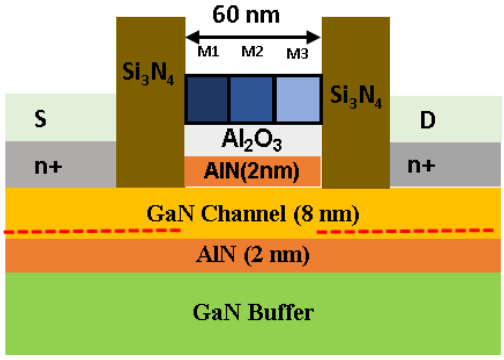

Figure1. Cross-sectional view of triple material gate (TMG) n-polar MOS-HEMT

Figure 1 shows the cross-sectional device structure of 60 nm gate length n-polar E-mode GaN MOS-HEMT. E-mode operation of the device is obtained by removing

AlN layer from both the sides by incorporating Si_3N_4 passivation layer. The gate electrode consists of triple material gate having highest work function at the source end and lowest at the drain end. It results in higher efficiency in carrier transport and decrease in peak electric field at the drain end which reduces the hot carrier effects.

The total surface potential model is developed and is written as

$$\psi_a(x) = P_i e^{+\lambda x} + Q_i e^{-\lambda x} + V_{gsi} + h_i \beta^2 \quad (1)$$

where *i*, is the different regions under different metal regions and is given as

$$i = \begin{cases} 1, & 0 \le x \le L_1 \\ 2, & L_1 \le x \le L_1 + L_2 \\ 3, & L_1 + L_2 \le x \le L_1 + L_2 + L_3 \end{cases} \quad (2)$$

Similarly, the total electric field along the channel is derived as

$$E_{tot}(x) = E_1(x) + E_2(x) + E_3(x) \quad (3)$$

The development of the model is presented in other research paper.

III. Results and Discussion

Figure 2 shows the variation of surface potentials along the channel from source to drain side for various material gates of SMG (single material gate), DMG (double material gate) and TMG (triple material gate). It shows a single step in potential for DMG at the interface of M_1 & M_2 and double step in potential at the interfaces of M_1 & M_2 and M_2 & M_3. It results in improvement of carrier concentration and electron velocity.

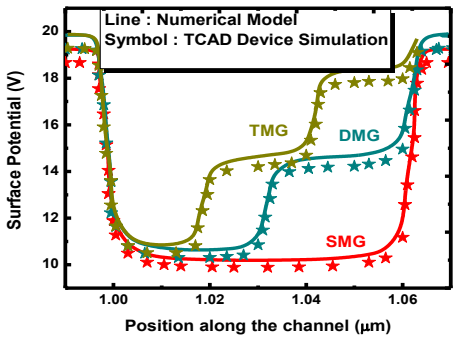

Figure 2. Comparison of Surface potential distribution between TMG, DMG and SMG devices

Figure 2 and Figure 3 also show a good agreement between numerical model and TCAD device simulation results which validates our proposed model. It also shows that the change in slope of surface potential in case of TMG is lower at the drain side as compared to DMG and SMG device. It produces lowering of electric field at the drain end at the interface of M_1 and M_2 as shown in Figure 3 which is the main reason behind the suppression of various short channel effects such as DIBL, output conductance etc. Figure 4 shows the variation of DIBL with respect to different channel lengths. It shows that the DIBL is higher for short channel device. Since the TMG device provides better screening of gates as compared to DMG and SMG devices, it produces lower DIBL as shown in Figure 5.

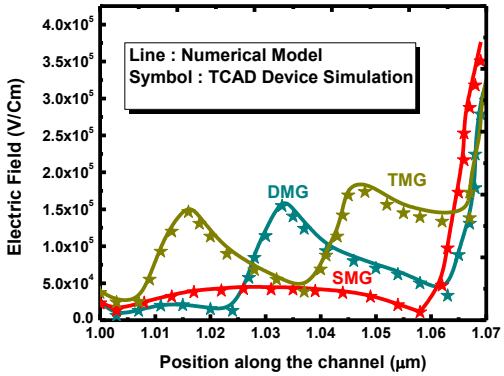

Figure 3. Comparison of Electric field distribution between TMG, DMG and SMG devices

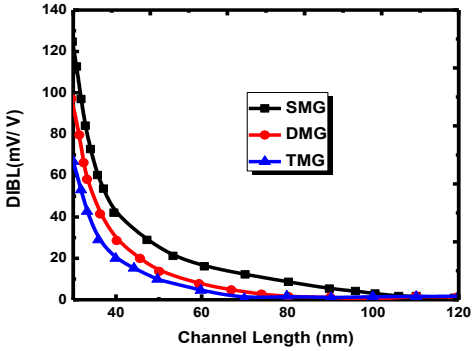

Figure 4. Comparison of DIBL effects between TMG, DMG and SMG devices

IV. Conclusion

A short channel n-polar GaN MOS-HEMT is proposed by applying gate work function engineering techniques for the first time. An analytical model of surface potential and electric field is developed and is validated with TCAD device simulation results. It is concluded that TMG device shows better suppression of short channel effects as compared to DMG and SMG device.

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III-V CMOS: *Quo Vadis?*

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In the last few years, there has been a great deal of interest in the potential of certain III-V compound semiconductors, notably InGaAs, to advance CMOS scaling in the future. The electron transport properties of InGaAs and other III-Vs are truly extraordinary, with electron velocities that are several fold those of Si. Yet, in spite of impressive device demonstrations, this effort has recently fizzled out. Understanding the reasons for this is important in order to have a realistic evaluation of the potential of III-V electronics. The value proposition behind III-V CMOS largely stands on the ability of nanoscale III-V transistors to deliver high current at low voltage. This would enhance the energy efficiency of logic operations leading to improvements in transistor density, the heart of Moore's law. At its core goal, III-V transistors have yet to deliver. The performance of the most advanced InGaAs FinFETs, to pick a relevant device structure, has yet to match that of Si devices. The reasons are not fully understood. Low channel effective mass, gate oxide trapping, interface states and sidewall scattering are likely to be contributors. Further, a successful CMOS technology must deliver stable characteristics that are also robust to manufacturing variations. In III-Vs, processing temperature constraints compromise gate oxide quality making trapping a major source of device instability. Also, the low effective mass of electrons in InGaAs results in prominent quantum effects at the target dimensions greatly amplifying the impact of feature size variability. Further, in future CMOS, off-current control is critical. Transistors based on InGaAs, with its narrow bandgap and long mean free path, have shown significant excess off-state current induced by band-to-band tunneling amplified by a parasitic floating-base bipolar transistor effect. This makes it difficult to achieve extremely low I_{off} devices needed for mobile applications as well as the implementation of "turbo" performance at high supply voltage, as required in others. Compounding these difficulties, the integration of III-Vs with Si with the required defect control remains an unresolved concern. This talk will review these and other problematic issues with III-V CMOS as well as discuss possible solutions.

Monomaterial Schottky Junction based on Semimetals

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***Abstract*—In this study, a Schottky junction is realised for a single elemental film, namely, bismuth, engineered to have two regions with different thicknesses to form a hetero-dimensional junction between a thick and a thin region with near ideal diode operation at room temperature. This work demonstrates that the fundamental laws of quantum mechanics can be harnessed to enable nanoelectronics innovation for electronic devices to be manufactured on the length scale of tens of atoms. Close agreement between atomic scale simulations and experimental results is obtained.**

Keywords-Bismuth; density functional theory; quantum confinement; Schottky junction; semimetals

I. Introduction

Nanoscale field-effect-transistors (FETs) enable the continuation of Moore's law for future technology generations, permit high device density at lower power per device, and consequently high function per integrated circuit at lower unit cost. For critical dimensions of a few nanometers, quantum confinement has pronounced effects on electronic band structures. Bulk bismuth is a semimetal with band overlap between the valence and conduction bands of 38meV and 98meV at 2K and 300K, respectively [1–4]. Quantum confinement in a low-dimensional bismuth leads to a semimetal-to-semiconductor transition [1].

II. Bi Film Growth and Characterisation

28nm, 14nm, 5.7nm, and 3.2nm Bi films used in this study were grown by molecular beam epitaxy (MBE) on undoped Si [111] wafers [5]. Prior to the deposition, the Si substrates were chemically cleaned by the HF-last RCA procedure to remove the native oxide and to passivate the surface with hydrogen. The substrates were subsequently heated *in-situ* to 700°C for 20 minutes to desorb the hydrogen atoms from the Si surface. The Bi material flux was generated by an effusion cell operated at a temperature of 550°C, which yields a growth rate of 17nm/hour. Thickness and crystallographic orientation are the key parameters determining the resulting electronic structure of the thin films. A cross-sectional transmission electron microscopy (XTEM) image of the 5.7nm film is shown in Fig. 1. Temperature dependence of carrier concentration obtained from Hall measurements is shown in Fig. 2 for the three Bi film thicknesses of 28nm, 5.7nm, and 3.2nm. For the thicker Bi film, the carrier concentration is largely independent of temperature for the range shown indicating semimetallic behavior. However for the 5.7nm film, more than an order of magnitude increase in the carrier concentration is seen over the temperature range from 200K to 300K revealing characteristic semiconducting behavior consistent with the onset of a quantum confinement induced bandgap. Although the 3.2nm Bi film is not single crystal (note the higher carrier concentration relative to the 5.7nm film), it possesses a remarkably high mobility, similar to the crystalline 5.7nm film.

III. Atomic Scale Simulation Results

Density functional theory (DFT) is standard method to study the atomic and electronic structure of materials. However, DFT methods are well known to suffer deficiencies with respect to predicting bandgaps primarily due to commonly used approximations for the electronic exchange and correlation energies.

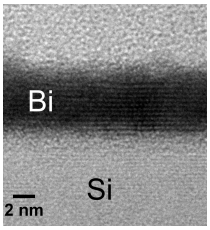

Figure 1. XTEM of 5.7nm Bi film grown by MBE on Si(111).

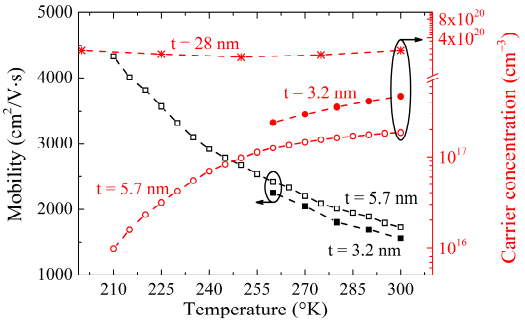

Figure 2. Temperature-dependent Hall data of the Bi films.

These approximations typically result in a large and systematic underestimation of bandgaps in semiconductors. To provide an improved description of the confinement effect in bismuth thin films, particularly with respect to determining bandgap energies, the *GW* (G: Green's function, W: screened Coulomb interaction) method in conjunction with a first order many body perturbation theory (MBPT) correction is used [6] based on the Kohn-Sham DFT solutions [7]. The role of surface chemistry in the bandgap is investigated by considering *–H* and *–OH* terminated surfaces. Bandgap versus film thickness and surface termination from *GW* calculations for Bi (111) slabs is shown in Fig. 3. Effects of spin orbit coupling and more detailed studies of the influence of surface termination on the (111) surface will be included in future investigation of the Bi electronic structure.

IV. Monomaterial Schottky Junction

To form a heterodimensional rectifier by forming a three dimensional (3D) to two dimensional (2D) junction in bismuth nanolayers, an etch recipe was developed to selectively thin regions of the Bi film in a controlled manner. Ti/Au was deposited on a 12nm semimetallic Bi film and patterned to form circular transfer length method (cTLM) electrical contacts. The metal contact structure was then used as a hard mask and the Bi film thinned using argon plasma etch.

Electrical measurements of the cTLM contacts on the 12nm un-etched sample (reference sample) showed Ohmic current-voltage (IV) characteristics over a temperature range of −40°C to 20°C yielding a contact resistance of $9\times10^{-4}\Omega\cdot cm^2$. The sheet resistance obtained from the cTLM analysis of $\rho_{cTLM} \approx 8\times10^{-4}\Omega\cdot cm$ is in good agreement with the Hall measurements $\rho_{Hall} \approx 6\times10^{-4}\Omega\cdot cm$. To vary the thickness of the bismuth film exposed to the etch step, the etch duration was varied between 60s and 80s. IV characteristics of the thick/thin devices are shown in Fig. 4 for the resulting 8.2nm, 4nm, and 1.5nm Bi films exposed to the etch step with thickness determined by TEM. The IV characteristic of the 12nm/8.2nm junction is approximately temperature independent consistent with the quantum confinement effect not playing an appreciable role in 8.2nm thick films. The dependence on temperature increases for

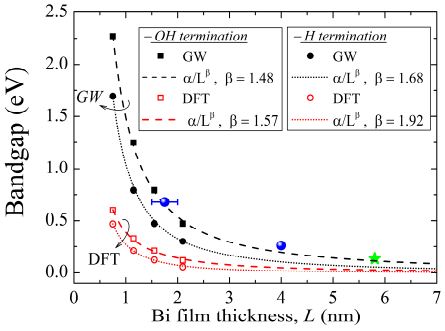

Figure 3. Bandgap versus film thickness (L) and surface termination from DFT calculations and implementing *GW* correction for Bi (111) slabs. Green/blue points indicate experimental data.

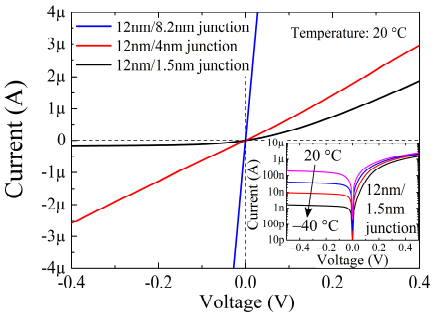

Figure 4. IV characteristics at 20 °C for thick/thin junctions. Inset shows the temperature-dependent IVs of the 12nm/1.5nm junction.

the12nm/4nm junction since the band offset at the thick/thin interface (*i.e.*, 132meV) is not large enough to prevent thermionic emission dominating the reverse current at room temperature. As the exposed bismuth region is further thinned to approximately 1.5-2nm, the formation of a Schottky barrier diode is observed through the rectifying nature of the IV characteristic. The semimetal-semiconductor barrier is further increased to ~0.34eV for the 1.5nm film as determined from the temperature dependence of the reverse saturation current (inset of Fig. 4). For a mid-gap Fermi level alignment, the estimated bandgap is ~0.70eV, which is in good agreement with the theoretical calculations as compared in Fig. 3. Near ideal diode behavior was observed for a diode fabricated in a heterodimensional junction using a single material, in this case bismuth, at room temperature.

Acknowledgment

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Large Area Growth of Non-intentionally Doped MoS_2 in a 300mm Atomic Layer Deposition Reactor

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***Abstract* - In this work, we grow MoS_2 using $Mo(CO)_6$ and H_2S by chemical vapour deposition (CVD) which is achievable over a 300mm diameter large area growth. Cross-sectional transmission electron microscopy (XTEM) shows that polycrystalline and layered MoS_2 is formed. Raman, x-ray photoelectron spectroscopy (XPS) and x-ray diffraction (XRD) all confirm the formation of MoS_2. Hall analysis, that also incorporates a four-point (4P) measurement, shows that the non-intentionally doped MoS_2 is *n*-type with a very low carrier concentration (~10^{14}cm^{-3}) and a very high resistivity (~kΩ-cm) most probably due to a high purity and small grain size of the MoS_2. Hall mobility is found to be 3.3-16.7cm^2/V.s. Excellent repeatability is achieved for four different growth runs and on three different substrates (SiO_2, sapphire and amorphous Al_2O_3). Circular transmission line method (c-TLM) total resistance measurements give a similar kΩ-cm resistivity result that infers a similar carrier concentration assuming a mobility of ~10cm^2/V.s.**

Keywords - CVD; MoS_2; $Mo(CO)_6$; H_2S; large area growth; Hall-effect; c-TLM; 300mm ALD reactor

I. Introduction

Two-dimensional (2D) materials such as Transition Metal Dichalcogenides (TMDs) of the form MX_2 (in this case, M=molybdenum and X=sulphur) are under investigation for applications spanning sensors, solar cells, logic transistors, low temperature electronics, super capacitors, photonic devices and solar water splitting for hydrogen-based energy generation [1]. One of the primary challenges prior to practical applications of 2D semiconductors is the ability to grow large area monolayer or multilayer TMDs using reproducible methods while developing high purity CVD processes [2, 3]. There is also a need to form TMD films with reduced contamination, as contaminants can lead to unintentional doping and variability in electronic properties [4, 5]. In this work, we report on the structural and electrical properties of non-intentionally doped MoS_2 deposited using high purity precursor flow of 99.99% $Mo(CO)_6$ + 99.999% H_2S by a reproducible industry-compatible CVD process in a 300mm atomic layer deposition (ALD) reactor.

I. Growth Details

The MoS_2 was deposited by CVD at 550°C/2.2Torr using $Mo(CO)_6$ and H_2S as precursors on a selection of substrates including SiO_2/Si, sapphire and amorphous alumina (a-Al_2O_3) by ALD on sapphire substrates. Growth time was ~2.5 hours. No post-growth anneal was performed. Fig. 1 shows the MoS_2 film uniformly covering the SiO_2/Si substrate. Deposition was achievable across a 300mm diameter.

II. Results and Discussions

XTEM images of the CVD grown MoS_2 on SiO_2/Si and sapphire substrates are shown in Fig. 2. Growth on both substrates shows that polycrystalline and layered MoS_2 is formed. There is no interfacial layer formed between MoS_2 and SiO_2, but an amorphous interfacial layer of ~0.5nm is observed between MoS_2 and sapphire, which is still being investigated. The growth of MoS_2 on sapphire presents more "out-of-plane" features and is not as ordered as the growth on SiO_2/Si. Fig. 2(c) suggests a small grain size of up to ~20nm on SiO_2/Si, and Fig. 2(d) suggests a small grain size of up to ~5nm on sapphire. Plan-view TEM (not shown) is also performed on the MoS_2 on SiO_2/Si and early results also suggest polycrystalline MoS_2 is formed with grain sizes of ~5-20nm. Work on the plan-view TEM is still ongoing.

Raman analysis (Fig. 3(a)) on the MoS_2 deposited on SiO_2/Si shows a clear MoS_2 signal with well-defined E^1_{2g} and A_{1g} peaks. XPS is also performed (Fig. 3(b)) confirming the formation of MoS_2. Fig. 4(a) shows the XRD of the MoS_2 deposited on SiO_2/Si, sapphire and a-Al_2O_3/sapphire substrates. Growth on all substrates show the MoS_2 (002) peak indicating the preferred c-axis orientation of the film. A high resolution XRD is also performed on MoS_2 on SiO_2/Si (Fig. 4(b)), which also reveals the MoS_2 (004) and (006) peaks. The (002) signal is weaker and broader on sapphire and on a-Al_2O_3/sapphire, suggesting that the growth may not be as ordered as on SiO_2/Si. This is consistent with the XTEM shown in Fig. 2. Work is ongoing to improve the grain size and horizontal order (i.e. less "out-of-plane" features) of the MoS_2. Identifying the nature of the *n*-type dopant is also a priority.

Hall/4P measurements are carried out at room temperature (RT) on MoS_2 deposited on sapphire and a-Al_2O_3/sapphire (sample size: 1cm x 1cm) under a Van der Pauw structure (Fig. 5(a)). Table I gives a summary of Hall/4P results, showing that the non-intentionally doped MoS_2 grown by CVD is *n*-type with very low carrier concentrations on the order of ~10^{14}cm^{-3}, electron mobility in the range 3.3-16.7cm^2/V.s, and high resistivity values (~kΩ-cm). In addition, RT c-TLM analysis, which is at a much smaller device scale than the Hall/4P measurements (see Fig. 5(b)), is performed on MoS_2 on SiO_2/Si. Linear current-voltage (IV) curves are observed under c-TLM analysis (Fig. 6(a)), consistent with the excellent Ohmic behaviour measured in the Hall/4P system (not shown). Fig. 6(b) shows the non-linear total resistance versus the outer radius (r_o) of the c-TLM, which is assessed to extract the resistivity, sheet resistance, transfer length and specific contact resistivity (Table II). The resistivity determined from the micro-scale RT c-TLM analysis (ρ=0.916kΩ-cm) is in reasonable agreement with those obtained from the macro-scale Hall/4P analysis on 1cm x 1cm substrates. Using the resistivity from c-TLM, assuming a Hall factor = 1 and Hall mobility (μ_H) = 10cm^2/V.s based on the mobility values from Hall/4P in Table I, carrier concentration is predicted to be 6.82 x 10^{14}cm^{-3}, which is very similar to the carrier concentrations obtained directly from the Hall/4P measurements (Table I).

III. Conclusions

We report continuous films of *n*-type MoS_2 by CVD which is achievable over a 300mm diameter large area growth using high purity precursors. XTEM shows that polycrystalline and

layered MoS_2 is formed. Raman, XPS and XRD all confirm the formation of MoS_2. Room temperature electrical analysis across different growth runs, substrates and from small (c-TLM) to large (Hall/4P) areas give similar results of very high resistivity (~kΩ-cm) and very low carrier concentration estimates (~10^{14}cm^{-3}). Hall mobility in the range 3.3-16.7cm^2/Vs is achieved with a grain size ranging from ~5-20nm. Work is ongoing to improve the grain size and horizontal order (i.e. less "out-of-plane" features) of the MoS_2 in order to improve the electrical characteristics.

ACKNOWLEDGMENT

The authors acknowledge the financial support of Science Foundation Ireland through the projects ATOM^2/AMBER (SFI-12/RC/2278) and INVEST (SFI-15/IA/3131). Lee A. Walsh would like to acknowledge funding from the European Union's Horizon 2020 research and innovation program under the Marie Skłodowska-Curie grant agreement no. 713567.

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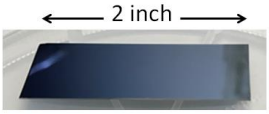

Fig. 1: A large coupon of CVD grown MoS_2 deposited on a SiO_2/Si substrate. Such coupons are placed over the area of the 300mm chuck and a uniform thickness is obtained indicating that continuous MoS_2 films are achievable over a 300mm diameter large area growth.

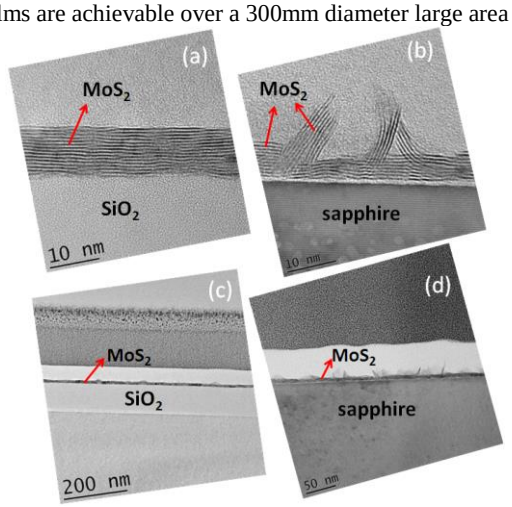

Fig. 2: XTEM of MoS_2 grown on (a, c) SiO_2/Si and (b, d) sapphire substrates showing polycrystalline and layered MoS_2 in (a) ~10nm thick on SiO_2/Si with no interfacial layer between the MoS_2 and SiO_2, and in (b) ~6-7nm thick on sapphire with a ~0.5nm amorphous interfacial layer (still being assessed). The growth on sapphire presents more "out-of-plane" features which may give a greater effective thickness than ~6-7nm as it is not as well ordered as the growth on SiO_2/Si. Zoomed-out XTEM of MoS_2 in (c) on SiO_2/Si and in (d) on sapphire suggest a possible grain size of up to ~20nm and ~5nm on SiO_2/Si and sapphire, respectively.

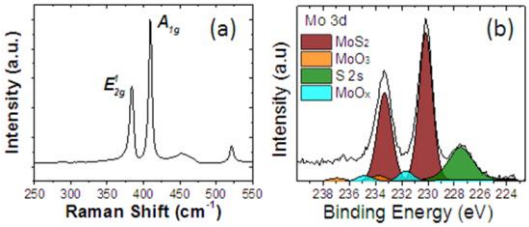

Fig. 3: (a) Raman and (b) XPS of the MoS_2 on SiO_2/Si. Raman shows characteristic MoS_2 peaks (E^1_{2g} in-plane and A_{1g} out-of-plane modes). XPS shows MoS_2 formed with low oxide contributions.

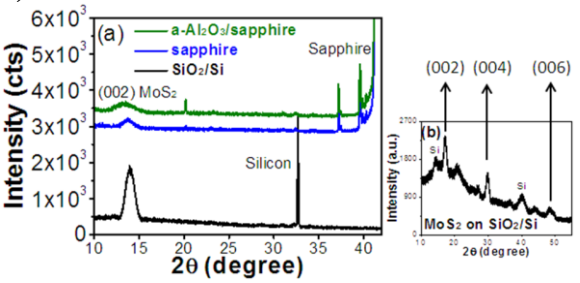

Fig. 4: XRD of the MoS_2 on SiO_2/Si, sapphire and a-Al_2O_3/sapphire all show a (002) peak confirming the layered crystalline growth of MoS_2. The growth on sapphire and a-Al_2O_3/sapphire show a weaker and broader (002) signal suggesting the growth may not be as well ordered as on SiO_2/Si, consistent with the XTEM in Fig. 2. High resolution XRD on MoS_2/SiO_2/Si also reveals (004) and (006) peaks.

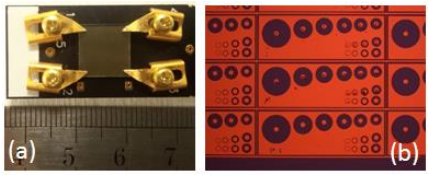

Fig. 5: Illustrations of (a) MoS_2 on sapphire (size: 1cm x 1cm) for RT Hall/4P measurements under a Van der Pauw structure, and (b) the c-TLM structure (outer radius r_o: 40-150μm of 8 devices used).

Table I: RT Hall/4P results on MoS_2 (nominally 10nm) deposited on sapphire and a-Al_2O_3/sapphire substrates. The MoS_2 is *n*-type with a high resistivity and a low carrier concentration.

Growth substrate	Resistivity (kΩ-cm)	Carrier type	Carrier concentration (cm^{-3})	Mobility (cm^2/V.s)
sapphire (sample 1)	3.561	*n*-type	1.05 x 10^{14}	16.7
sapphire (sample 2)	12.10	*n*-type	1.44 x 10^{14}	3.58
a-Al_2O_3/ sapphire	5.768	*n*-type	3.28 x 10^{14}	3.3

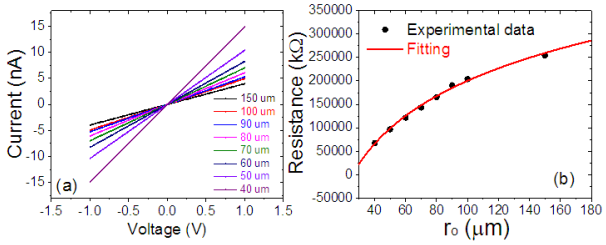

Fig. 6: (a) IV curves of c-TLM devices at RT. All IV curves are linear, consistent with the excellent Ohmic behaviour observed by Hall/4P measurements (not shown); and (b) total resistance data to extract the components of resistivity, sheet resistance, transfer length and specific contact resistivity.

Table II: The c-TLM resistance components on MoS_2 on SiO_2/Si that includes a resistivity of 0.916kΩ-cm. Recalculating a carrier concentration based on this resistivity, and assuming a Hall factor of 1 and a Hall mobility (μ_H) of 10cm^2/V.s (from Table I), we can approximately reproduce the Hall/4P carrier concentration, reflecting the similarity in the micro-scale and macro-scale resistivity.

Resistivity (ρ)	0.916kΩ-cm
Sheet resistance (R_s)	916MΩ
Transfer length (L_t)	2.47 x 10^{-5}cm
Specific contact resistivity (ρ_c)	5.61 x 10^{-1}Ω-cm^2
Carrier concentration = 1/(μ_H.ρ.e)	6.82 x 10^{14}cm^{-3}

Current and Shot Noise at Spin-dependent Hopping in Magnetic Tunnel Junctions

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***Abstract*— Upcoming mass production of energy efficient spin-transfer torque magnetoresistive random access memory (MRAM) will revolutionize modern microelectronics by introducing non-volatility not only for memory but also for logic [1]. However, the pressing issue is to boost the sensing margin by improving the tunneling magnetoresistance ratio (TMR). We demonstrate that spin-dependent trap-assisted tunneling in magnetic tunnel junctions (MTJs) can increase the TMR. The influence of spin decoherence and relaxation on the current and shot noise at trap-assisted hopping is investigated.**

Keywords-Spin-dependent hopping, shot noise, spin relaxation, MTJ, MRAM

Spins injected from a nonmagnetic semiconductor on a trap are oriented in arbitrary direction with equal probability. In case the spin is parallel to the magnetization of the ferromagnetic electrode with the polarization p, its escape rate to the ferromagnet is enhanced by a factor $(1+p)$, while it is decreased by a factor $(1-p)$ for the antiparallel orientation. In the later case, the electron is locked on the trap for a longer time. At the same time the electron blocks another electron from entering the trap (the Coulomb blockade). Thus, due to spin correlations the current is reduced as compared to trap-assisted tunneling between the normal electrodes.

Spin decoherence described by the time T_2 is effectively equivalent to the strong magnetic field [2], see Fig.1. Spin relaxation (T_1) reduces spin correlations and the magnetoresistance modulation (Fig.1). The current and the spectral function of the current fluctuations at low frequency $S(\omega=0)$ and the Fano-factor $F(\omega=0)=S/2eI$ are calculated by a Monte Carlo technique [3], with escape rates from the trap determined by the matrix equation:

$$\frac{d}{dt}\begin{pmatrix} n \\ s_x \\ s_y \\ s_z \end{pmatrix} = -\mathrm{A}\begin{pmatrix} n \\ s_x \\ s_y \\ s_z \end{pmatrix},$$

$$\mathrm{A} = \begin{pmatrix} \Gamma_\mathrm{F} & p\Gamma_\mathrm{F}\sin\Theta & 0 & \Gamma_\mathrm{F}\cos\Theta \\ p\Gamma_\mathrm{F}\sin\Theta & \Gamma_\mathrm{F}+1/T_2 & \omega_\mathrm{L} & 0 \\ 0 & -\omega_\mathrm{L} & \Gamma_\mathrm{F}+1/T_2 & 0 \\ p\Gamma_\mathrm{F}\cos\Theta & 0 & 0 & \Gamma_\mathrm{F}+1/T_1 \end{pmatrix} \quad (1)$$

Θ is the angle between the magnetic field and the magnetization, ω_L is the Larmor frequency. Fig.2 shows that the noise is enhanced above the single-electron limit (F=1) due to spin correlations. Spin dephasing reduces the noise to below the single-electron limit, when the magnetic field is perpendicular to the magnetization. Spin relaxation suppresses spin correlations everywhere and brings the noise to the spin-independent value.

In an MTJ the second electrode is a ferromagnet with the magnetization along the direction determined by the angles (ζ, φ) relative to the magnetic field ($\varphi = 0$ in the following) and the polarization p_2. The current and the noise are evaluated with the help of (1) complemented with the initial condition that the trap is occupied by an electron (n=1) with a non-zero average spin determined by the injection from the source ferromagnet:

$$\begin{pmatrix} n \\ s_x \\ s_y \\ s_z \end{pmatrix}(t=0) = \begin{pmatrix} 1 \\ p_2\sin\zeta\cos\varphi \\ p_2\sin\zeta\sin\varphi \\ p_2\cos\zeta \end{pmatrix} \quad (2)$$

Fig.3 shows the dependence of the current as a function of Θ for several values of ζ, $\Gamma_\mathrm{N}=10\Gamma_\mathrm{F}$, $\omega_\mathrm{L}=\Gamma_\mathrm{F}/2$, $p=p_2=0.8$. The current has a maximum at $\Theta=\zeta$, where the contact magnetizations are parallel. The noise shown in Fig.4 is enhanced around $\Theta\approx\zeta\approx 0$, when the current is large. This appears to be in contradiction to Fig.2, where the noise has a maximum at the minimum of the current. However, the noise enhancement in both cases is due to spin correlations.

For the drain magnetization parallel to the magnetic field ($\Theta=0$) the transport is determined by the two channels with the rates $\Gamma_\mathrm{F}(1\pm p)$. The probability to excite the channels is proportional to the injection rates $\Gamma_\mathrm{N}(1\pm p_2)$ for $\zeta\approx 0$. The time-dependent charge transfer process is represented by the bursts of high currents through the fast channel, separated by long periods with low current through the slow channel. As the probability to excite the fast channel is largest at $\zeta=0$, the current is maximal. At the same time, the charge transferred during the current bursts between the two periods of low currents is maximal, which determines the high value of the shot noise in the high current state of MTJs.

Fig.5 shows the effect of spin dephasing and relaxation on the charge current due to trap-assisted tunneling through an MTJ, for $\zeta=0$. As in Fig.1, the difference between the maximum and the minimum currents is enhanced at strong dephasing. Importantly, the TMR at spin-dependent hopping with strong dephasing is larger than the TMR at direct tunneling [4], indicating the potential of spin-dependent hopping for MTJs' transport properties optimizations.

Fig.6 displays the influence of spin dephasing and relaxation on the low frequency noise for $\zeta=0$. Spin relaxation suppresses spin correlations and brings the noise to the level of spin-independent hopping. Spin dephasing shifts the current maximum to finite Θ, where the noise is significantly suppressed as compared to its highest value at $\Theta=0$. In conclusion, strong spin dephasing at spin-dependent hopping enhances the TMR, while simultaneously reducing the noise level.

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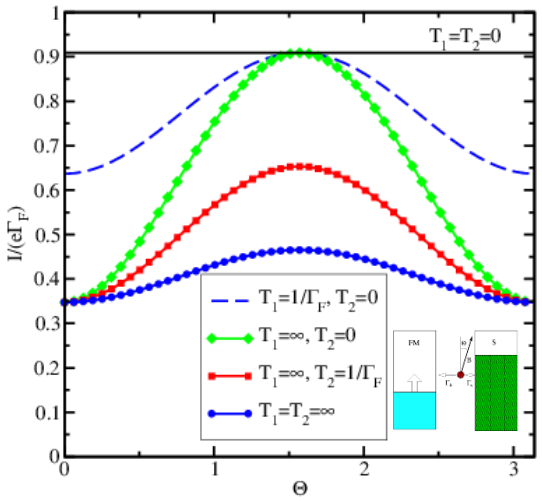

Fig.1. Current between the normal and ferromagnetic electrodes due to trap-assisted hopping (Inset) as a function of the angle Θ between the magnetic field and the magnetization. The parameters are described in the caption of Fig.2.

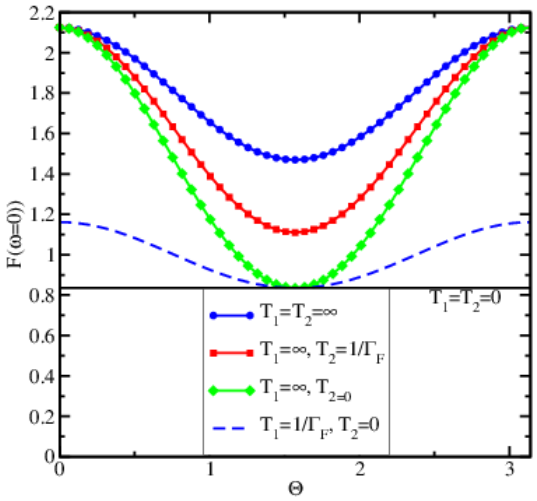

Fig.2. The Fano factor $F=S/2eI$ characterizing the low frequency current noise as a function of Θ, for several values of the spin decoherence time T_2 and relaxation time T_1. The parameters (Fig.1, Fig.2) are: $\Gamma_N=10\Gamma_F$, $\omega_L=\Gamma_F/2$, p=0.8.

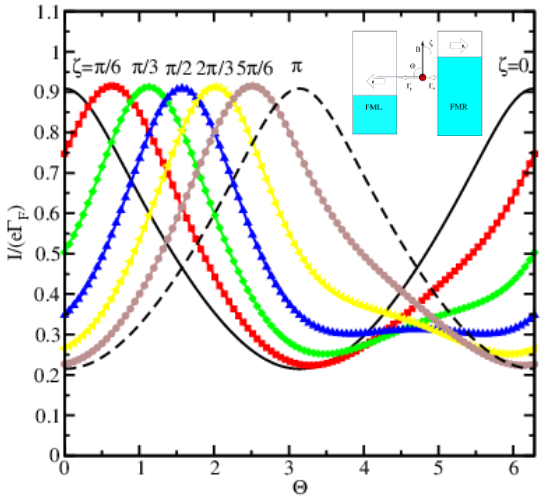

Fig.3. Spin-dependent trap-assisted current through an MTJ (Inset) as a function of the angle Θ, for several values of the angle ζ between the magnetic field and the source magnetization. The same parameters as in Fig.4.

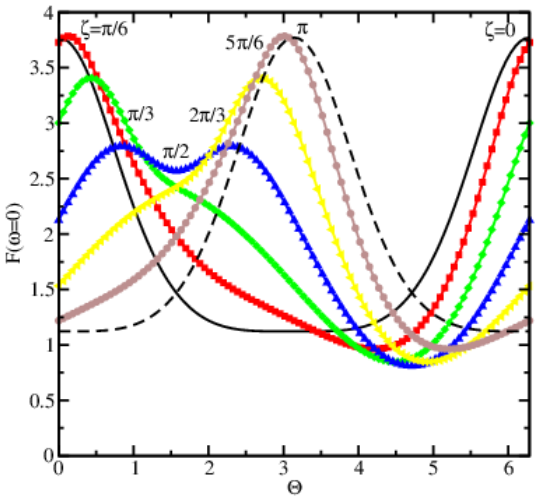

Fig.4. The Fano factor at spin-dependent hopping in an MTJ. The parameters (Fig.3-Fig.6) are: $\Gamma_N=10\Gamma_F$, $\omega_L=\Gamma_F/2$, $p=p_2$=0.8. It is assumed that there is no spin relaxation nor dephasing in Fig.3, Fig.4.

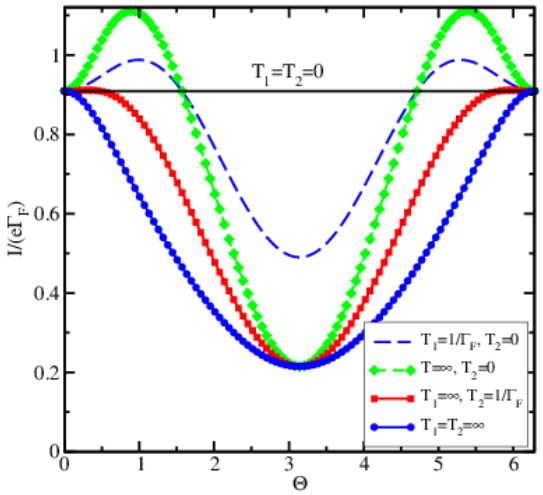

Fig.5. Influence of dephasing/relaxation on the current in Fig.4 for $\zeta = 0$ (the source magnetization is along the field).

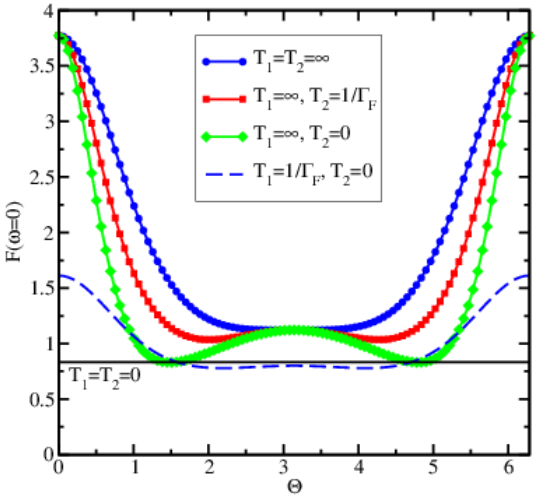

Fig.6. The Fano factor for parameters in Fig.5. Strong dephasing boosts the TMR and suppresses the noise.

3D Scaling of Si-IGBT

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***Abstract*—Three dimensionally (3D) scaled IGBTs that have a scaling factor of 3 (*k*=3) with respect to current commercial products (*k*=1) were fabricated. The scaling was applied to the lateral and vertical dimensions as well as the gate voltage. A significant decrease in ON resistance, -- V_{CEsat} reduction from 1.70 to 1.26 V -- was experimentally confirmed for the 3D scaled IGBTs.**

Keywords-component;3D; scaling; silicon; IGBT

I. Introduction

Si power devices such as IGBTs (Insulated Gate Bipolar Transistors) are attractive for the huge volume market, and therefore, the innovation of Si IGBT technology is still strongly demanded.

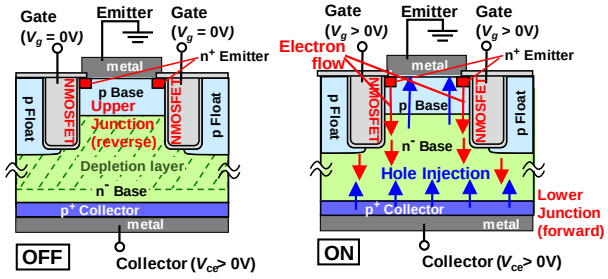

Figure 1. Schematic trench gate IGBT structure.

Fig. 1 shows a schematic cross-section of a typical trench gate IGBT. When the NMOSFET at the trench surface is OFF, huge depletion layer is formed in the n- base region by the huge reverse bias at the upper pn junction, resulting in the prevention of the breakdown. So, the n- base donor concentration should be as low as possible and n- base layer should be sufficiently very thick – such as 120 μm for 1,200 V blocking voltage device , while the p base layer is only several μm thick.

When, the NMOSFET is ON, the ON current raises the voltage at the bottom of the n- base, finally causing the heavy injection of the carriers into the n- base at the lower pn junction.

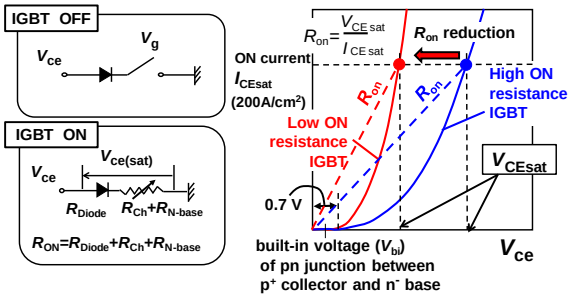

Figure 2. Relation between V_{CEsat} and ON resistance.

Reduction of the ON resistance, or lowering the collector emitter saturation voltage, V_{CEsat}, is an essential requirement for low energy-loss IGBTs (Fig. 2). Because the resistance of the n- base region is the major part of the ON resistance due to its huge thickness, it is important to keep the high carrier concentration storage in the n- base (Fig.3).

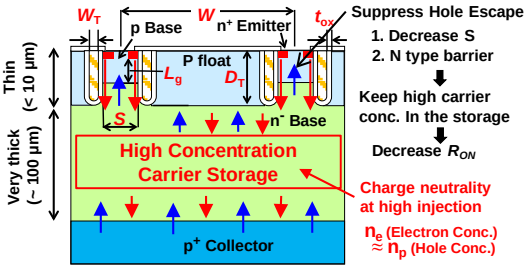

Figure 3. Carrier storage to reduce ON resistance.

To satisfy this requirement, some concepts have been proposed such as decreasing the mesa width, S [1] and forming a potential barrier by inserting an n layer with higher donor concentration between p and n- bases [2], both of which suppress the hole carrier flow from the carrier storage region (Fig.3), and thus increase the hole concentration at the storage. Because of the charge neutrality principle, electron and hole concentrations in the n- base are almost equal at the high injection mode, the increase of the hole concentration results in the electron Injection Enhancement from the NMOSFET (IE effect) [1,2], and the high carrier concentration in the storage region reduces the ON resistance significantly. Several experimental and simulated investigations have verified increase in the IE effect with significant reduction of V_{CEsat} [3,4].

Some problems for decreasing only the mesa width (1D scaling) have been reported [3,5]. One problem is an increase of the mesa resistance and another is the short circuit endurance degradation by the collector induced barrier lowering [12]. An obvious solution to the narrow mesa problems could be the scaling of both the width and height of the mesa region (2D scaling) with slight sacrifice of the IE effect. The 2D scaling of IGBT structures was investigated by device simulation [6], showing significant reduction in V_{CEsat} even with the trench depth reduction. The experimental verification of the merit of the 2D scaling was conducted with the newly proposed 3D scaling design, presented at IEDM in December 2016 [7]. This paper explains the 3D scaling scheme of IGBT and demonstrates excellent low ON resistance for the scaled device.

II. Scaling Design for This Work

Our 3D scaling concept is shown in Fig. 4. Most of the parameters including the gate voltage (V_g) were decreased by a factor of 1/k, while keeping the cell pitch (W) at 16 μm. A decrease in trench depth (D_T) from 6 to 2 μm leads to a significant reduction in fabrication cost, as well as lowering the thermal budget for dopant drive-in, resulting in a possible prevention of the carrier lifetime degradation. The trench width (W_T) is scaled moderately considering fabrication easiness.

Parameters in IGBT, symbols	k=1	k=3	Scaling factor
Cell pitch, W (μm)	16	16	1
Mesa width, S (μm)	3	1	1/k
Trench depth, D_T (μm)	6	2	1/k
Trench width, W_T (μm)	1.5	1.0	2/k
P-Base depth, D_P (μm)	3	1	1/k
N-Emitter depth, D_N (μm)	0.4	0.13	1/k
Gate oxide thickness, t_{ox} (nm)	100	33	1/k
Length of p$^+$ region, L_{p+} (μm)	4.5	1.5	1/k
Length of n$^+$ region, L_{n+} (μm)	4.5	1.5	1/k
Gate voltage, V_g (V)	15	5	1/k

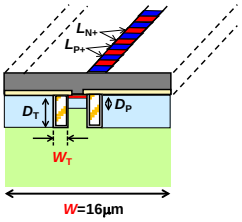

Figure 4. Our 3D scaling scheme

Scaling in the p-base depth (D_P), results in a higher sheet resistance for the p-base region and it may cause latch-up. To overcome this problem, the lengths of the emitter (n$^+$)/body (p$^+$) periodic patterns formed on the mesa top surface, L_{n+} and L_{p+}, (Fig. 4) were also scaled by a factor of 1/k. This decreases the p base length to the ground contact, resulting in the p base resistance decrease. This is scaling along the direction perpendicular to the cross section, so that the 3D scaling on the IGBT structure is employed in this work.

III. Results and Conclusions

Both k=1 and k=3 IGBTs designed for 1.2 kV were fabricated using n$^-$/n$^+$/p$^+$ Si substrates as a starting material. Detailed process conditions are explained in [7]. The results are shown in Figs.5 and 6, and Table I.

Two times higher emitter current, or one half ON resistance, was obtained with k=3, even with V_g scaling (Fig.5). Significant V_{CEsat} reductions from 1.70 to 1.26V, and from 1.96 to 1.26 V @ 200 A/cm^2 at room temperature and 150°C, respectively, were verified by the scaling from k=1 to k=3 (Fig.6, Table I). Performance improvements of Si-IGBT have been confirmed with the 3D scaling.

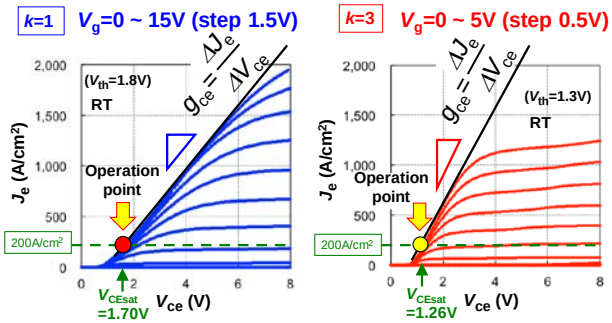

Figure 5. J_e –V_{ce} characteristics for K=1 and 3

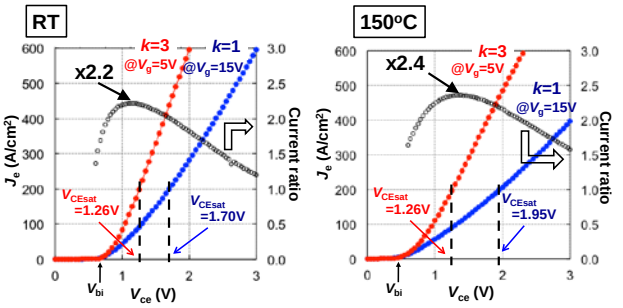

Figure 6. J_e –V_{ce} characteristics at RT and 150°C

Table I Bench mark of V_{Cesat} [8,9]

	This work k=3 (chip)	This work k=1 (chip)	IGC99T120 T8RM Infineon (chip)	FGW25N 120W Fuji Electric (package)
Target blocking voltage (V)	1200	1200	1200	1200
V_g (V)	5	15	15	15
V_{CEsat} (V) T_j=25°C	1.26	1.70	1.75	2.0
V_{CEsat} (V) T_j=150-175°C	1.26	1.95	2.05	2.6

Acknowledgment

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The Role of the Bottom and Top Interfaces in the 1^{st} Reset Operation in HfO_2 based RRAM Devices

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I. Introduction

Resistive random access memory (RRAM) technology has emerged in recent years as a promising platform to carry out several electronic device applications such as non-volatile memories (NVM), artificial synapses in neuromorphic networks and random number generators (RNG) [1]–[3]. In RRAM devices based on hafnium oxides (Hf-Ox) the resistive switching (RS) effect is attributed to the creation and disruption of nanometer scale conductive filaments (CFs) in the insulator layer, consisting of oxygen vacancies (V_O) [4]. Creation process, referred as set operation, moves RRAM devices in a low resistive state (LRS), whereas disruption process, referred as reset operation, brings the device in a high resistive state (HRS) [5]. To activate these switching operations a preliminary soft breakdown in the insulator, referred as forming operation, is required [6]. The 1^{st} Reset operation after forming has been reported in literature as a particular case compared to subsequent reset operations [7]. In this work a new approach to explain this behavior is proposed, which highlights the role of both metal-oxide interfaces, namely, $Ti_xO_yN_z/HfO_{2-x}$ (bottom interface) and HfO_{2-x}/Ti_xO_y (top interface).

II. Experimental

The measurements were performed on 128 1T1R devices constituted by a NMOS transistor, manufacturated in IHP's 0.25 μm CMOS technology, whose drain is connected in series to the metal-insulator-metal (MIM) resistor, placed on the metal line 2 of the CMOS process (Fig. 1(a)). The MIM cell consists of a TiN/Hf-Ox/Ti/TiN stack of 150 nm TiN layers deposited by magnetron sputtering, a 7 nm Ti layer (under TiN top electrode) and a 6 nm Hf-Ox layer grown by atomic layer deposition (ALD), with an area of about 0.4 μm^2.

In order to reduce the cell-to-cell variability, the incremental step with verify algorithm (ISPVA) has been the programming strategy used to perform the switching operations (forming, reset and set) in our studies for recent years [9]. The ISPVA technique consists of a sequence of increasing voltage pulses (Fig. 1(b)) applied on the drain terminal during set and forming operations, whereas this sequence is applied on the source terminal during reset operation. After every pulse a read-verify operation is performed by using a read-out pulsed voltage of

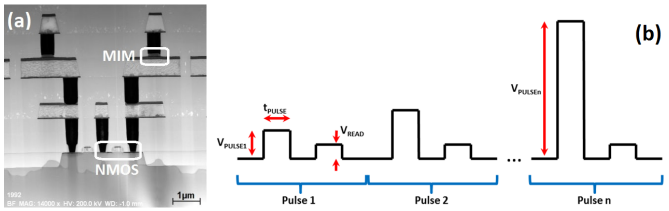

Fig. 1. Cross-sectional TEM image of the 1T1R integrated cell (a), and schematic illustration of the incremental step pulse with verify algorithm (ISPVA) (b) [8].

0.2 V. In this work each pulse featured a duration of t_{PULSE} = 10 μs. The programming operation is stopped on a cell when the read-out current reach a specific target value, referred as threshold current (I_{th}).

III. Results and Discussion

For the forming operation the amplitude of voltage pulses in ISPVA was swept in the range of 2-5 V applying a gate voltage (V_g) of 1.4 V and defining I_{th} = 30 μA. The evolution of the current values measured after each pulse in the sweep is shown in Fig. 2(a). For reset and set operations the amplitude of programming pulses was swept between 0.2 and 3.5 V. Reset operation was performed applying a V_g = 2.7 V and defining I_{th} = 5 μA, while in set operation the values used for these two parameters were the same as in forming operation. As shown in Fig. 2(b), the evolution of current values measured for the 1^{st} Reset feature a significant increase before performing the reset transition. Such a current increase is suppressed in subsequent reset operations, as shown in Fig. 3(b) for the second reset operation. This difference is usually attributed to a current overshoot occurring during forming transition, which does not occur during set transitions, caused by the parasitic capacitances present in the RRAM device [10]. However, because of the use of the read-verify scheme this increase in the CF conductivity must be related with a change in the CF morphology at that specific time. Thus, we propose a new approach to explain the increase of CF conductivity during the 1^{st} Reset by highlighting the crucial role played by both metal-oxide interfaces. In Fig. 4 are depicted the CF morphologies corresponding to five relevant scenarios. During forming, the drift of V_O, formed by the scavenging ability of Ti in the

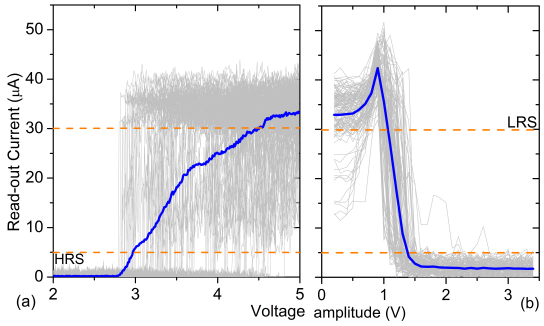

Fig. 2. Evolution of read-out current values during ISPVA for forming (a) and the 1^{st} Reset (b) operations on 128 devices (grey) and its average (dark blue).

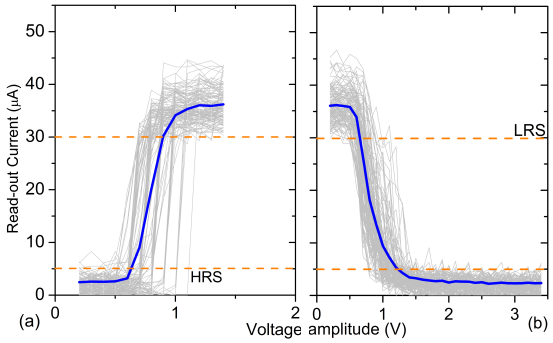

Fig. 3. Evolution of read-out current values during ISPVA for set (a) and second reset (b) operations on 128 devices (grey) and its average (dark blue).

Hf-Ox layer, creates a weak CF (Fig. 4(a)) [11]. According to Walczyk et al. [12] a thin $Ti_xO_yN_z$ layer appears on the bottom interface, which supports the formation of V_O close to this interface. At the beginning of the 1^{st} Reset, these V_O drift making stronger the tip of the CF (Fig. 4(b)), which is in line with the current increase in Fig. 2(b). Afterwards, such a drift opens a gap along the CF (Fig. 4(c)) moving the device to HRS. By applying the set operation the CF is reconstructed (Fig. 4(d)). The resultant CF is more conductive than after forming operation because of its stronger tip on the bottom interface. Moreover, the CF is less conductive than in the 1^{st} Reset peak because only a few V_O fill the gap depleted during reset operation. Subsequent reset operations (Fig. 4(e)) open the gap without morphology changes in the CF on the bottom interface, which suppresses the current increase as shown in Fig. 3(b). Thus, the maximum current values achieved during the second reset are essentially the same as in LRS after set operation.

IV. Conclusions

The increase in the CF conductivity before its disruption during the 1^{st} Reset operation has been studied by using ISPVA in 1T1R RRAM devices. The read-out currents measured in different scenarios were illustrated with the corresponding morphologies of the CF, which gives insights about the role played by both metal-oxide interfaces. The top interface is crucial for the forming operation whereas the bottom interface

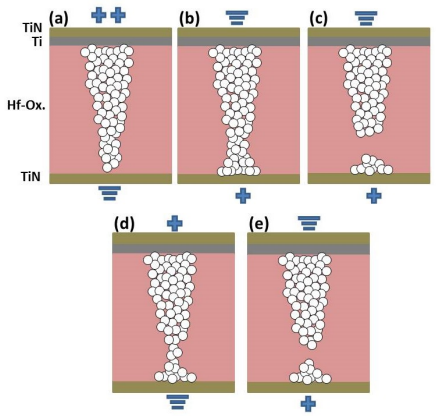

Fig. 4. Conductive filament (CF) morphologies after forming (a), at the current peak in the 1^{st} Reset (b), after the 1^{st} Reset (c), after set (d), and after the second reset (e).

seems to be the responsible of the current increase during the 1^{st} Reset.

Acknowledgment

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A Flexible Characterization Methodology of RRAM: Application to the Modelling of Conductivity Changes

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***Abstract*— In this work, an automatic measurement setup, which allows a massive electrical characterization of RRAM with pulsed voltages, is presented. A single pulse test-scheme is introduced as an example of application for neuromorphic engineering, where the fine analog control of the device conductivity state is required. Results are further modelled including device-to-device variability, allowing the simulation of crossbar arrays and their performance.**

The extraordinary properties offered by RRAM devices make them very promising devices in multiple applications, as memory [1-4], logic [1, 3] or neuromorphic [4-7] systems. In the latter case, the RRAM conductivity varies in a specific value range [4-7], so that the device operation conditions must be carefully chosen. For pulse programing, the control of the RRAM electrical properties with the suitable amplitude, width and polarity of the pulses becomes mandatory in order to achieve a fine analog tuning of its conductivity state. Therefore, electrical characterization methods oriented to evaluate the impact of the applied pulses on the device conductivity would be beneficial [2,6]. In this work, an automatic electrical measurement setup, which allows a massive electrical characterization of individual RRAM devices is presented. Experimental data are represented as conductivity state maps for each sample, as proposed by the compact model in [8]. The obtained information permits to extend the above mentioned model to perform system-level simulations of RRAM-based crossbar arrays.

Tested samples consist in TiN-Ti-HfO_2-W Metal-Insulator-Metal (MIM) structures with 10nm oxide thickness and an area of 5x5μm^2. The equipment used involves a Semiconductor Parameter Analyzer (SPA) and a Pulse Generator (PG), which are connected to a computer and are controlled via GPIB. The top and bottom electrodes of the sample are connected to the SPA and PG, respectively, as shown in Fig. 1 (Top). Here, the voltage drop at the sample is defined as V_p. It must be emphasized that the SPA and PG cannot be simultaneously active: when the SPA applies signals, the PG is grounded, and vice versa. With this configuration, a switch (to alternate the connection of the sample between the SPA and PG) is not needed. Then, the transient response of the system is improved, since the effects of the switch parasitic capacitance are avoided, which might affect the measurements when low pulse width pulses (~100ns) are applied and the RRAM resistance is high. The PG can be flexibly configured, to apply single pulses or pulse trains, with amplitude, pulse width (PW), frequency and polarity defined by the user. The SPA is in charge of switching the device state (SET or RESET) and measuring the device properties after the pulses application. In Fig. 1 (Bottom), a flux diagram of the adopted measurement scheme is shown. After the forming cycle is applied to the sample with the SPA, a sequence begins, which starts with a RESET and current limited SET processes. These RESET and SET events enable to control the initial conductivity of the device with the current limited SET process and fixing the maximum applied voltage in the RESET process [9]. After that, a subsequence of *n* steps begins, during which pulsed voltages are applied. The subsequence consists in the application of the pulse(s) with the PG and the conductivity state (G) measurement with the SPA. The subsequence can be repeated *N* times, changing in each iteration some parameter of the applied pulse(s) (e.g. amplitude, PW, polarity). The number *N* of iterations is a parameter controlled by the user, and might be used to control the initial conductivity value with a current-controlled SET [9]. The measurement procedure is fully automated, with real time monitoring of data acquisition and processing, allowing a massive characterization. The versatility offered by the proposed characterization setup allows the evaluation of the electrical properties of the tested devices for a wide range of applications, such as memories, logic or neuromorphic engineering, where a pulse programming scheme is required. In this work, we focus on the characterization of the RRAM after the application of single pulses, as a necessary previous step for the understanding of the effects of pulse trains on the RRAMs conductivity. A test scheme designed for obtaining conductivity state maps is introduced, which allows the further modelling of the tested devices for system-level simulations.

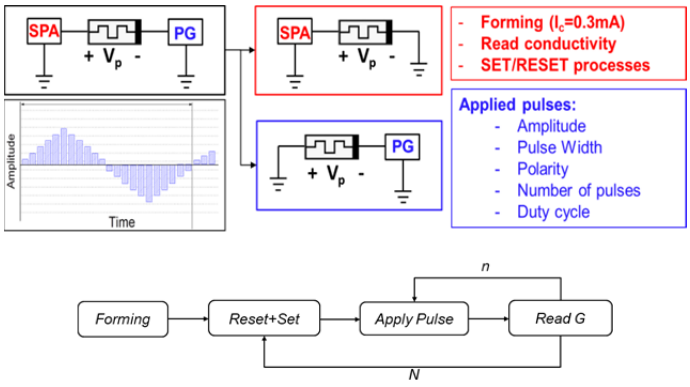

Fig. 1. (Top) Characterization setup and scheme of the applied voltage wave-form for the obtention of the G-V characteristics. (Bottom) Flux diagram of the performed experiment.

In this case, the measurement is the achieved conductivity after a single pulse. The proposed test scheme consists in the following steps: the initial conductivity was set within known ranges, by inducing a current-controlled SET process [9] (SPA). Then, increasing amplitude voltage pulses with a fixed PW were applied (from 0 to |1.5|V), for both polarities (PG). The conductivity state G of the devices is read after each pulse (SPA). The obtained data, displayed in Fig. 2 in red, shows that G can be controlled with the pulse amplitude and polarity, and depends on the past activity of the device, matching the predicted behavior stated in [8], where a time-independent compact model for non-linear memristive devices was provided. An extension of this model is made according to the obtained experimental data, which allows to perform a statistical study of the model parameters. This extended model is a static model for the conductance because for $\Delta V=0$ nothing changes over time. It takes into account the electrical history, i.e. the previous conductivity of the device, for the calculation of the conductivity extreme values. Defining α as the derivative of G over V, it is straightforward to deduce (1):

$$g_i = \alpha(V)\cdot\Delta V + g_{i-1} \quad (1)$$

Where g_i is the updated and normalized conductivity state, g_{i-1} is the normalized conductivity state before the application of a voltage pulse, and in our case, $\Delta V=\pm 0.1V$. The $\alpha(V)$ can be calculated from the numerical derivative of the curves plotted in Fig.2. In Fig.3, the experimental $\alpha(V)$ function is depicted: gray lines correspond to all the data, and the blue dotted line to the mean. This function is defined by parts according to the following expressions, where $\beta=\text{sign}(\Delta V)$ and $Vc^{\pm}$ is a voltage threshold:

$$\text{if } |V|<|V_c^{\pm}|;\ \alpha(V) = A^{\pm}\cdot\exp\left(\beta\,(V-V_c^{\pm})\,/\,B^{\pm}\right) \quad (2)$$

$$\text{if } |V|>|V_c^{\pm}|;\ \alpha(V) = A^{\pm}\cdot\exp\left(-\beta\,|V-V_c^{\pm}|\,/\,C^{\pm}\right) \quad (3)$$

The fitting parameters A, B, C and V_c that are extracted from the experimental data shown in Fig.3 (gray lines) are displayed in Table I. The modelled $\alpha(V)$ function is depicted in Fig.3 (red line):

TABLE I. MODEL PARAMETERS

	Model parameters			
	$A\ (V\Omega)^{-1}$	$B\ (V^{-1})$	$C\ (V^{-1})$	$V_c\ (V)$
$\beta = +1$	54.53±14.89	-0.14±0.05	-0.77±1.35	0.73±0.12
$\beta = -1$	90.73±15.19	-0.05±0.01	-0.09±0.02	0.97±0.02

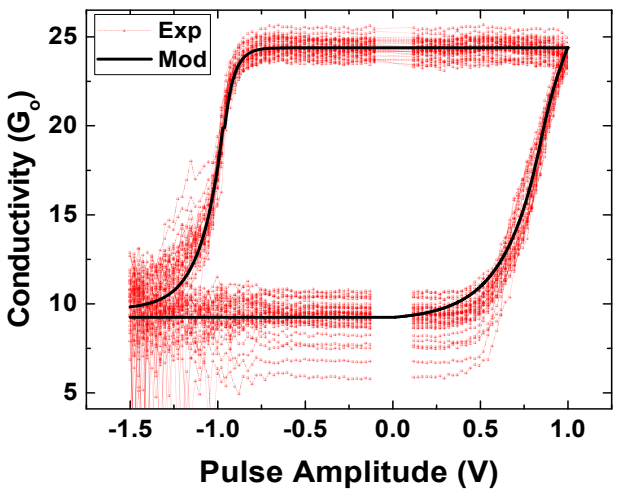

Fig. 2. Experimental G-V characteristics (red dots). G-V characteristics according to the model (black line).

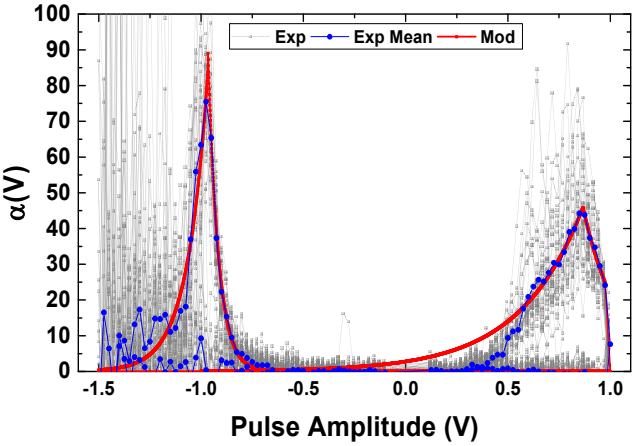

Fig. 3. Experimental dG/dV for each G-V characteristic (gray line) and for the whole dataset mean (blue dotted line). In black, the modelled dG/dV.

The proposed RRAM variability-aware compact model can be used for system-level simulations in a wide range of applications. An example can be found in [10], where the device-to-device variability impact on a crossbar-array performance is studied when a neuromorphic application is considered.

CONCLUSIONS

An automatic electrical setup for RRAM conductivity measurement is presented, allowing their flexible and massive characterization for pulse programming schemes. In this work, a particular test scheme is proposed to obtain the devices G-V characteristics. Results show that the achieved conductivity after a pulse application is dependent on the pulse amplitude, width, polarity and the previous conductivity of the device. A proper operation range for the tested samples can be defined for the target application. The experimental data has been used to make a variability-aware extension to a time-independent compact-model for the hysteretic loops in non-linear memristive devices. The extension takes into account the previous conductivity of the device and its history, allowing to include variability effects. The extended model is the basis of further studies on the RRAM conductivity changes induced by pairs of pulses or pulse trains, and are essential for the device modelling in order to perform device or system-level simulations.

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Investigation of SiGe channel introduction in FDSOI SRAM cell pFET and assessment of the Complementary-SRAM

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***Abstract*— In this work, we investigate the introduction of SiGe in FDSOI SRAM bitcells by the means of spice simulation. The classical SRAM configuration performance at a given leakage is only slightly impacted because of the SiGe stress partial relaxation in the small Pull-Up active dimensions. Since the SiGe compressive stress strongly enhances the hole mobility for long active stripes, it is relevant to design a Complementary-SRAM bitcell, using SiGe pFETs as both Pull-Up and Pass-Gate devices. In such a configuration, the read current is enhanced by +21% with respect to the reference at the same leakage.**

I. INTRODUCTION

The introduction of SiGe channel in Ultra-Thin Buried oxide and Body Fully Depleted Silicon On Insulator (UTBB-FDSOI) logic pFET allows standard cells of high performance in the 14nm CMOS technology [1-3]. In addition, the excellent mismatch properties [4] enables 6T-SRAM bitcells of ultra-low leakage [5,6]. In the 14nm memory (Fig.1), Si channel is often preferred in the channel of pMOSFETs (with a p-doped well) because high threshold voltage (V_T) is required. In this work, based on SPICE simulations, the introduction of SiGe channel in 14nm FDSOI SRAM is discussed for the first time. Two configurations are studied: The introduction of SiGe channel in the Pull-Up or as the Pass-Gate in Complementary-SRAMs (CSRAM) [7].

II. SIGE INTRODUCTION IN CLASSICAL 6T-SRAM

The introduction of SiGe in pFET channel has two major impacts on the transistor characteristics: the threshold voltage lowering and the mobility increase (Fig.2a). Also, it has been shown that SiGe channel pFET are subjected to strong local layout effects because of patterning-induced strain relaxation [3,8-10]. More precisely, for short gate-to-STI distance (named SA), the SiGe channel pFET V_T increases because of the partial stress relaxation. At SA=350nm, the SiGe pFET I_{ODLIN} outperforms the Si nFET I_{ODLIN} by +10% (Fig.2b, exp.). This layout effect is accounted for in our compact model by the stress-based model described in [11] with a V_T stress- and Germanium-sensibilities of $|S_{stress}|$=100mV/GPa and $|S_{Ge}|$=6mV/%. Using spice, SRAM cell is simulated with different Ge concentrations x_{Ge} (Fig.3). Obviously, the leakage of the bitcell is highly impacted by the SiGe introduction because of PU V_T reduction (Fig.3). The SiGe introduction reinforces the PU and makes it more difficult to write a '0' in the internal node (see Fig.3). The PG>PU criterion for write operation being weakened, the Write Noise Margin WNM and write current I_W are degraded. At same leakage (obtained with a manual V_T shift of $\Delta V_{T,p}$=+250mV) the SRAM cell with SiGe channel PU is almost similar to the reference (Fig.4). This can be explained by the fact that the PU active area is small (i.e. short SA, SB and narrow W, see Fig.1). The PU is thus strongly impacted by the SiGe relaxation, resulting in similar hole mobility in Si and SiGe and in turn in similar SRAM metrics.

III. COMPLEMENTARY-SRAM

In the classical SRAM cell, in order to satisfy the PD>PG and PG>PU criteria (required for proper read and write operations, respectively), the PDs and PGs are nFETs while the PUs are pFETs because the electron mobility is higher than the hole mobility in Silicon. However, by introducing SiGe in the pFET channel, the hole mobility can be greatly enhanced. This is particularly true when the active is long in the source/drain direction (high SA) [10]. In such a geometry, the simulated $I_{ODLIN}(W)$ for both nFET and pFET predicts that $Si_{0.75}Ge_{0.25}$ pFET outperforms Si nFET by +27% at W=66nm (active width of the PG in our SRAM cell). This makes it relevant to use pFET in Pass-Gate in a so-called Complementary-SRAM (CSRAM, Fig.5). The transistors are here referred as CPG, CPD and CPU. The operation of the bitcell is reversed. Especially, the Word Line is biased to V_{DD} in retention and the Bit Lines are biased to the ground for a read operation. The criterion PD>PG for reading becomes CPU>CPG and the PG>PU one for writing becomes CPG>CPD. In the following, the different configurations are studied at a given leakage, obtained after a proper pMOS V_T re-targeting (which can be obtained by metal gate workfunction tuning, channel doping, back-biasing or change of ground-plane type). Fig.6 shows both the read and write currents w.r.t. the leakage. With 25% of Germanium, the read current of the CSRAM is enhanced by +21% with respect to the SRAM reference (Fig.6). Fig.7 summarizes the different SRAM metrics at the same leakage (the required V_T shift is also given). A read current enhancement of +21 is observed with 25% Ge w.r.t the reference SRAM. However the write operation of the CSRAM cell is slightly degraded (lower WNM and -5% I_W). In the reference SRAM, the hole mobility in Si PU is low compared to the one of electron in PG, ensuring a high PG>PU ratio. In the CSRAM, the hole mobility in the CPG is enhanced by the SiGe integration, compared to hole mobility in Si but finally "only" 27% higher than the electron mobility. This results in a CPG/CPD drive ratio not as strong as the PG/PU one. For $Si_{0.75}Ge_{0.25}$, the pFET V_T shift to compensate for the introduction of SiGe is +300mV, which might be challenging to achieve. A solution for a CSRAM bitcell construction is proposed in Fig.8. In order to achieve low leakage, the CPG and CPU feature N-type gate and N-type well. In addition, the pFET back-bias is changed to V_{DD} while nFET one is maintained to the ground in a dual well architecture.

IV. CONCLUSION

In this work, we have studied by spice simulation the introduction of SiGe in FDSOI SRAM bitcells. In the classical SRAM configuration, the memory performance at a given leakage is only slightly impacted because of the partial SiGe stress relaxation induced by the small PU active dimensions. On the opposite, for long active stripes, the $Si_{0.75}Ge_{0.25}$ compressive stress strongly enhances the hole mobility. This makes it relevant to design a Complementary-SRAM bitcell, using SiGe pFETs as both Pull-Up and Pass-Gate devices. It is demonstrated to enhance the read current by +21% with respect to the reference at the same leakage.

ACKNOWLEDGMENT: This work was partly funded by the ECSEL WAYTOGO- FAST project, and by the French Public Authorities through the NANO2017.

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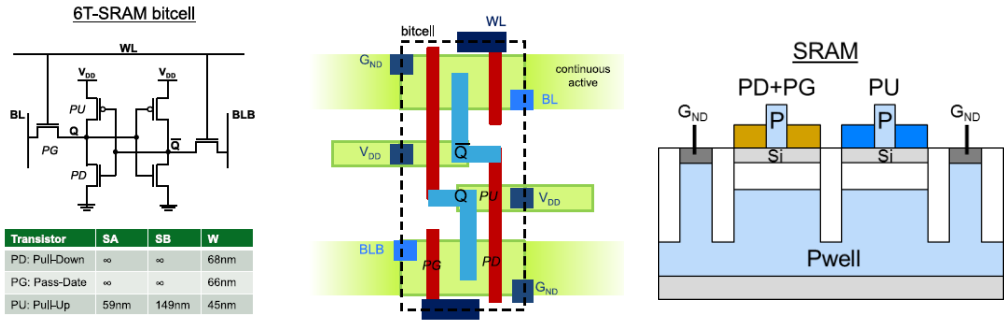

Fig. 1. 6T-SRAM schematic, layout and construction.

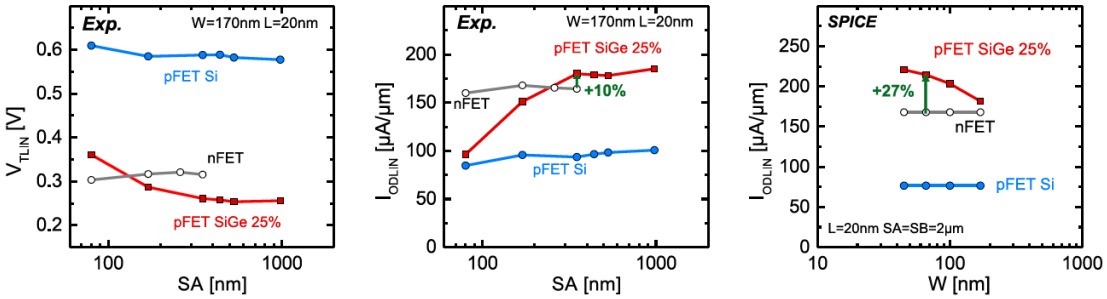

Fig. 2. Local Layout Effects of SiGe channel pFET compared with Si pFET and nFET.

%Ge =	0%=REF	10%	20%	25%
SNM [mV]	**147**	170	189	196
WNM [mV]	**336**	333	289	232
I_W [µA]	**31**	28	23	20
I_{READ} [µA]	**17**	17	17	17
$I_{leakage}$ [pA]	**23**	36	358	1677

Fig. 3. SRAM metrics for different SiGe concentrations in the PU.

%Ge =	0%=REF	25%
ΔV_T,p [mV]	**0**	+250
SNM [mV]	**147**	153
WNM [mV]	**336**	324
I_W [µA]	**30.6**	29.7
I_{READ} [µA]	**17.4**	17.4
$I_{leakage}$ [pA]	**23**	24

Fig. 4. SRAM metrics benchmarked at same leakage for $Si_{0.75}Ge_{0.25}$ channel PU.

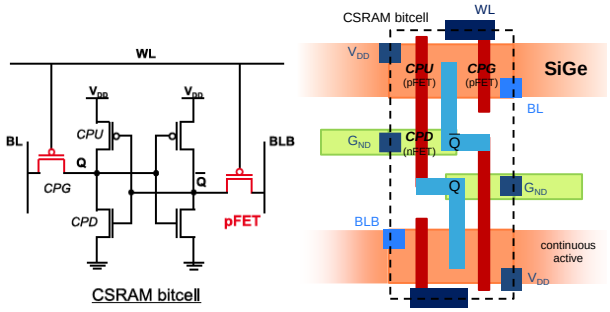

Fig. 5. CSRAM schematic and layout. Pass-Gates are made of pFET (i.e. CPG).

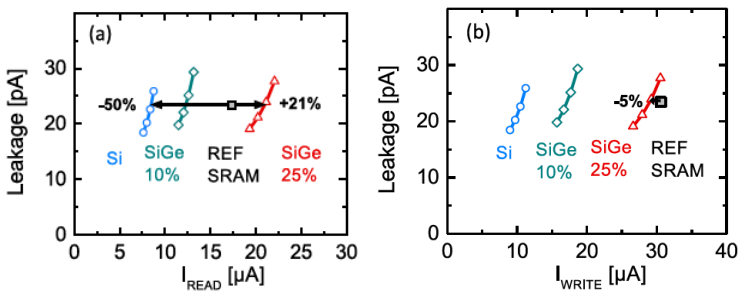

Fig. 6. (a) I_{READ} and (b) I_{WRITE} *vs.* Leakage at V_{DD}=0.8. +21% read current expected with 25% Ge and -5% I_{WRITE}.

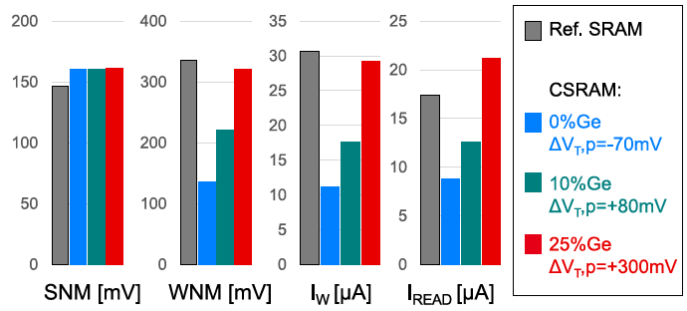

Fig. 7. CSRAM metrics at same leakage compared to reference SRAM for different Ge concentrations.

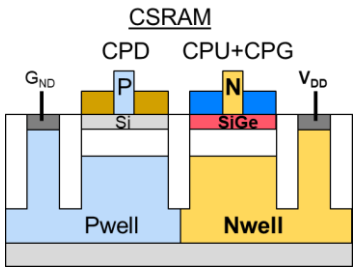

Fig. 8. CSRAM construction.

Ferroelectric properties of HfO_2 interlayers in SOI and SOS pseudo-MOSFETs

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***Abstract*— Formation of a multi-crystalline HfO_2 film, containing ferroelectric phase O2 ($Pmn2_1$), after a high-temperature annealing at 1100°C, was experimentally observed for the first time in SOI and SOS structures obtained by a hydrogen transfer of silicon layer on Si or c-sapphire substrates respectively. PEALD HfO_2 interlayers with the thickness of 20 nm were deposited on silicon before bonding to reduce the defects and the magnitude of their charge at the SOI and SOS interfaces. SOI and SOS pseudo-MOS transistors demonstrate normal drain-gate characteristics with the charge carriers mobility as in bulk silicon and a smaller positive charge ($\leq 1.2x10^{12}$ cm^{-2}). Moreover, a stable ferroelectric hysteresis with ΔV_g ~600 V promising for the embedded memory formation and they extend the functionality of logic circuits.**

Keywords- SOS and SOI pseudo-MOSFETs, hafnium oxide interlayer, ferroelectric phase, polarization mechanism

I. INTRODUCTION

Ferroelectric field effect transistors (FeFETs) with enhanced functionality allow new memory and logic cell architectures for computing [1]. For the implementation of such devices we developed and studied metastable ferroelectric (FE) layers of hafnium dioxide as one of the two dielectrics gates in SOI and SOS FeFETs. FeFETs will allow to change the functionality of the logic cell providing two-gate or optical control of the charges for reconfigurable logic, executing functions of memory and learning integral schemes, which can be used in future for brain simulating computers. The purpose of this work was the study of the properties of metastable ferroelectric phases in hafnium oxide interlayer in SOI and SOS pseudo-MOSFETs, using structural and electrophysical measurements.

II. EXPERIMENT

The transfer of the (100) silicon layer (n-type, 10-20 Ohm·cm and electron density n = 3-5x10^{14} cm^{-3}) on Si or c-Al_2O_3 substrates was carried out by implanted hydrogen according to the patented technology [2]. The hafnium dioxide layer (PEALD HfO_2) with a thickness of 4 to 20 nm was grown by the plasma-enhanced atomic layer deposition (PEALD) at 300°C on Si wafers before bonding. Immediately before the hot bonding, the wafer pairs of sapphire and silicon were undergoing a treatment in the O^+ or N^+ plasma and after bonding a transfer of the silicon layer with a thickness of 0.5 μm. SOI and SOS heterostructures were being then annealed in the Ar atmosphere in the temperature range of 800-1100 °C for 2 hours. The layer structural properties and composition were determined by the transmission electron microscopy cross-section (XTEM) and electron dispersion spectroscopy (EDS) using microscopes JEOL JEM4000 and JEM2000FX, respectively. The electrical properties of SOI and SOS structures were determined from the drain-gate characteristics of pseudo-MOSFETs, with tungsten needles tip radius of 20 μm and the pressing force of 60 g, used as drain-source contacts.

III. RESULTS AND DISCUSSION

The structural properties and composition of silicon layers in the SOS structures were determined on 100 mm c-orientation sapphire substrates (Fig. 1, 2). The silicon layers, after annealing at temperatures from 1000°C and above, contain almost no defects and do not differ in their properties from the original silicon. The originally amorphous PEALD HfO_2 layers are recrystallized in multi-crystalline layers. A cross-section of such layers, including the obtained microimages in high-resolution electron microscopy (HREM), is shown in Fig. 1, 2. The result of such annealing is an intermediate layer formation between silicon and PEALD HfO_2, which contains, according to the EDS, mainly silicon and oxygen (Fig. 2). Due to the overlap of Si K and Hf Ma lines, as well as a partial overlap of Al Ka and Hf M lines and the small (2-3 nm) thickness of the intermediate layer between the silicon dioxide and hafnia, it was not possible to establish its content, although considering the low electron density in this layer (Fig. 1, 2), its most probable composition is silicon oxide with hafnia inclusions, repeatedly observed experimentally. White arrows (inset of Fig. 1b) show the crystallographic directions in the lattice of PEALD HfO_2 between which the angles are: 34.0° (AB); 84.5° (AC). The best way of

describing the experimental data (Table 1) is by using the lattice data for orthorhombic phase of HfO_2 P-O2 ($Pmn2_1$), stabilized by tetragonal distortion of stretching along the axes (19.5° to normal) and biaxial compression in the plane in most part of the interlayer. Phase HfO_2 P-O2 was not previously observed experimentally, but, according to the theoretical calculations, it should be more stable than the tetragonal phase at such strain [3].

TABLE I. INTERPLANAR DISTANCES AND ANGLES FOR THE KNOWN MONOCLINIC (M) TETRAGONAL (T), TWO ORTHORHOMBIC (O1, O2) FROM [3] AND EXPERIMENTAL (EXP) PHASE OF HAFNIA

Phase	a(Å)	b(Å)	c(Å)	β(°)	γ(°)
M	5.15 (5.14[a], 5.12[b])	5.20 (5.20[a], 5.17[b])	5.33 (5.31[a], 5.29[b])	99.7 (99.8[a], 99.2[b])	90 (90[a], 90[b])
T	5.08 (5.08[a], 5.08[c])	5.08 (5.08[a], 5.08[c])	5.23 (5.28[a], 5.20[c])	90 (90[a], 90[c])	90 (90[a], 90[c])
P-O1	5.06 (5.01[a], 4.90[c])	5.09 (5.08[a], 4.92[c])	5.27 (5.29[a], 5.10[c])	90 (90[a], 90[c])	90 (90[a], 90[c])
P-O2	5.13 (5.12[a])	5.13 (5.12[a])	5.18 (5.18[a])	90 (90[a])	84.07 (83.51[a])
Exp	**5.01**	**5.01**	**5.24**	**90**	**84.5**

[a] Ref. 13, [b] Ref. 31, [c] Ref. 32, from [3]

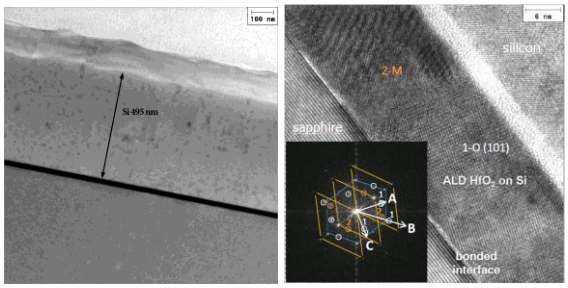

Figure 1. XTEM microimage of the SOS structure with a 0.5 μm Si layer and a PEALD HfO2 layer with a thickness of 20 nm after annealing at 1100°C (left); HREM microimage for the SOS-structure with two HfO_2 microcrystals with the grain boundary between crystallites 1-O (orthorhombic) and 2-M (monoclinic phase) (right). Inset: FFT map of the HREM image consisting of three diffraction patterns from the Si layer, sapphire and HfO_2

The transport properties measurements were carried out using pseudo-MOS transistors with a field gate from the substrate. The embedded positive charge value decreases, and the normal characteristics of pseudo-MOSFETs were obtained for the structures with an interlayer of hafnia in a thinned sapphire substrate (Fig. 3). The stable hysteresis ΔV_G ~ 400 V in drain-gate characteristics of the pseudo-MOS SOS-transistor confirms the ferroelectric phase formation in the hafnium oxide layer after the annealing at 1100°C, while the direction of hysteresis, due to a charge capture in the traps, would be the opposite. The polarization of high-k dielectric HfO_2 shifts the n-, p- threshold ΔV_{FT} ~ 400-600 V at Vg = ±3 kV, which corresponds to a change in ΔV_{HfO2} = ±80 mV, and the maximum field $3.5x10^4$ V/cm in the HfO_2 layer provides the remnant polarization P= ± (80-100) nC/cm^2, compared to the theoretical value of P= 56 μC/cm^2 in a coercive field (1-2)x10^6 V/cm, when the most stable phase of hafnia is orthorhombic [3]. Only part of the interlayer possessed ferroelectric properties, and the surface breakdown hindered the increase in the range of substrate potential. However, the field and remnant charge polarization in the hafnia interlayer can be increased further by reducing the sapphire thickness as in the case of UTBB SOI wafers.

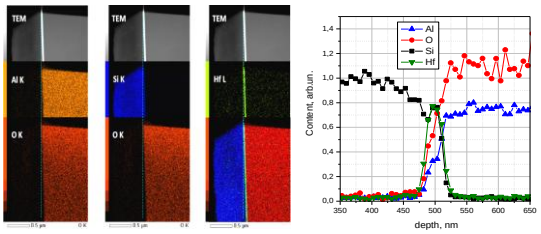

Figure 2. XTEM and EDS micro-images of the SOS with 0. 5 μm layer of Si and a 20nm layer of PEALD HfO2 after annealing at 1100°C (left); integrated profiles of O, Al, Si and Hf (along the y-coordinate of the EDS maps) near the interface, normalized to the density of atoms in the volume of silicon and sapphire

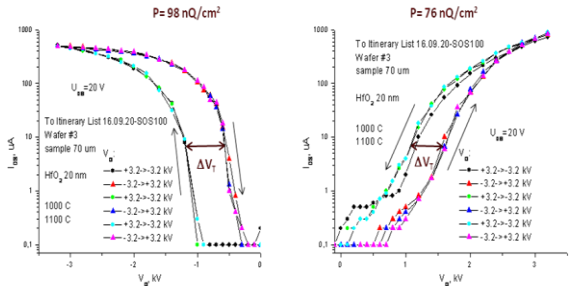

Figure 3. Hysteresis of drain-gate characteristics for pseudo-MOS SOS transistor with an interlayer of hafnia on sapphire with a thickness of 70 μm at V_{ds}=-20 V for holes (left) and at V_{ds}=+20 V for electrons (right)

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Random Discrete Dopant Induced Variability in Negative Capacitance Transistors

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***Abstract*—In this work we investigate the impact of random discrete doping (RDD) induced statistical variability in ferroelectric negative capacitance field effect transistors (NCFETs). We couple the 3D 'atomistic' statistical device simulator GARAND with the Landau - Khalatnikov (L-K) equation of the ferroelectric for this study. We find that the presence of the ferroelectric layer can lead to suppression of the RDD induced threshold voltage (V_t) and OFF-current ($I_{\rm OFF}$) variability. This immunity to RDD increases with increase in the ferroelectric thickness. In contrast, the ON-state current ($I_{\rm ON}$) variability does not follow the ferroelectric thickness monotonically.**

***Keywords*—Negative capacitance, MOSFET, Ferroelectric, statistical variability, Random Discrete Dopants**

I. Introduction

NCFETs are constructed by introducing into the gate stack a layer of a ferroelectric material that acts as a conditionally negative capacitor. Such devices have been demonstrated to achieve a sub-60 mV/dec subthreshold swing [1], [2] and consequently they are being pursued as a means to scale down supply voltage without loss of performance [3], [4].

Variability induced due to intrinsic statistical nature of discrete dopants in the semiconductor channel of MOSFETs has been an important source of variability, and their role in limiting the performance of existing CMOS technologies has been well studied [6], [7]. In this work we compare the impact of RDD in conventional MOSFETs and ferroelectric based negative capacitance transistors combining 3D TCAD with the steady state L-K model.

II. Simulation Methodology

We examine bulk NCFETs with the MFMIS (Metal–Ferroelectric–Metal–Insulator–Semiconductor) structure which essentially consist of a conventional MOSFET with a ferroelectric layer in between the gate of the conventional MOSFET and an external metal gate as shown in Fig. 1.

We use the 3-D device simulator GARAND [8] to obtain the charge-voltge and current-voltage characteristics of the reference MOS transistor. We then calculate the potential drop across the ferroelectric using the steady-state Landau-Khalatnikov equation [9], [10]. Finally we map the internal gate bias to the actual (external) gate bias using voltage balance, thus obtaining the terminal characteristics of the NCFET. The simulation flow and assumptions therein have been shown in Fig. 2. We run 1000 simulations each with a random distribution of dopants and one simulation assuming continuous doping without any dopant fluctuation. Drift-diffusion transport model with density gradient quantum correction is employed for the simulations.

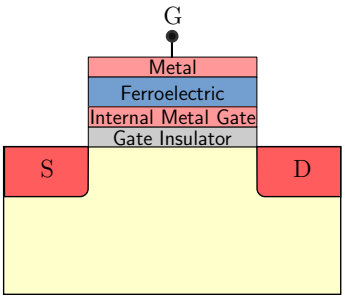

Fig. 1. Cross-sectional schematic of an NCFET. The ferroelectric is sandwiched between the internal and external metal gates.

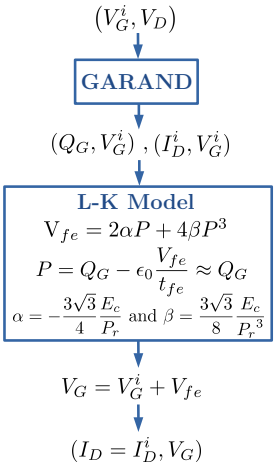

Fig. 2. NCFET simulation flow: V_G^i is the internal gate voltage, V_{fe} is the voltage drop across the ferroelectric, P is the polarization, Q_G is the gate charge density, α and β are the ferroelectric parameters which can be expressed in terms of the coercive field, E_c and remnant polarization, P_r. t_{fe} is the ferroelectric thickness. I_D and V_G denote the drain current and post-processed gate voltage for the NCFET.

We use a CMOS process compatible metal doped HfO_2 ferroelectric having a coercive field, E_c = 1 MV/cm and remnant polarization, P_r = 5 μC/cm^2 [11]. We have set each nominal NCFET device to be hysteresis-free (this limits the maximum t_{fe} to ~7nm). The operation of NCFETs based on capacitance matching, their typical characteristics and dependence on ferroelectric thickness and matarial parameters have been described elsewhere (e.g. see [9], [10], [12], [13]) and will not be discussed here. Also, note that the variability in the ferroelectric layer itself is not considered here, as the focus is to isolate the impact of the NC effect on RDD induced variability.

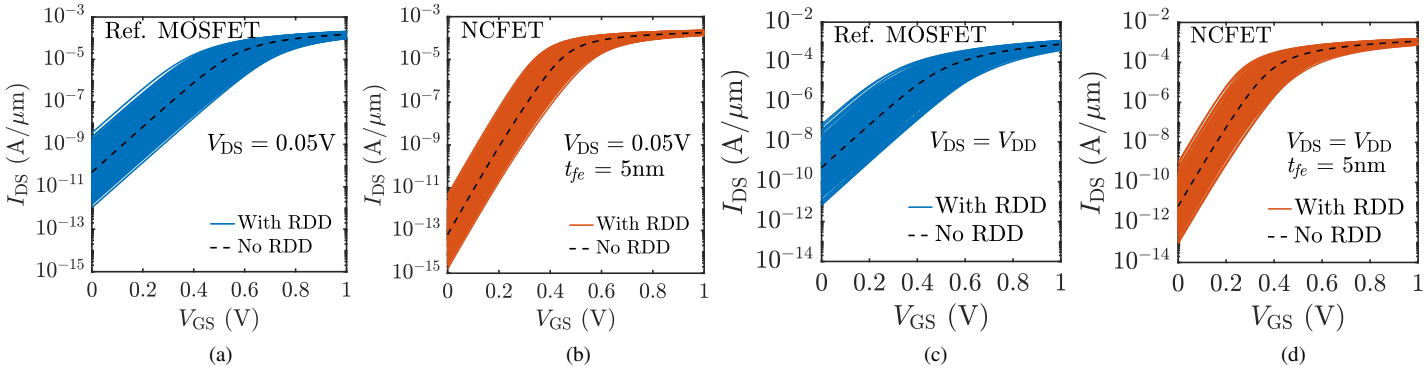

Fig. 3. $I_{DS} - V_{GS}$ curves for the reference MOSFET and NCFET (t_{fe} = 5 nm) obtained from statistical simulation (solid lines) and continuous doping profiles with no RDD (dashed lines). (a) - (b): at V_{DS} = 0.05V. (c) - (d): at $V_{DS} = V_{DD}$. The nominal NCFET curves are shifted to have iso-V_t, and the same amount of shift is applied to the statistical data for NCFETs.

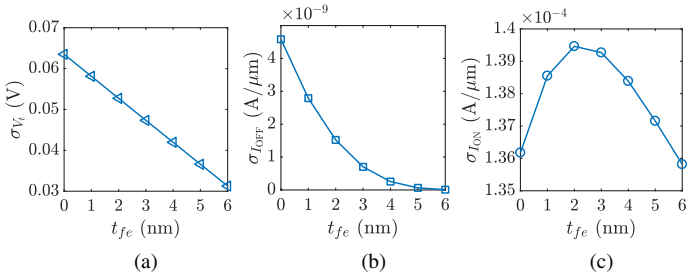

Fig. 4. Variability in (a) V_t, (b) I_{OFF} and (c) I_{ON} with t_{fe}.

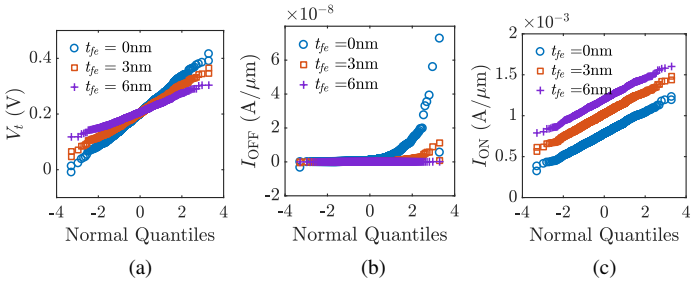

Fig. 5. Q-Q plots for (a) V_t, (b) I_{OFF} and (c) I_{ON} for the reference MOSFET (t_{fe} = 0 nm), and NCFETs with t_{fe} = 3 nm and 6 nm.

III. Results and Discussion

For a reasonable comparison, the threshold voltage (V_t) of the RDD-free NC device at each t_{fe} is set to that of the reference MOSFET. The $I_{DS} - V_{GS}$ curves of the NCFETs with RDD are shifted by the same offset. Fig. 3 shows the transfer characteristics of the reference MOSFETs and NCFETs (with t_{fe} = 5nm) at low and high drain biases. The reduction in variability is evident. In Fig. 4, we show the impact on the standard deviation in V_t, I_{OFF}, and I_{ON} as a function of the ferroelectric thickness. σ_{V_t} and $\sigma_{I_{OFF}}$ decrease, while $\sigma_{I_{ON}}$ shows a non-monotonic behavior with increase in t_{fe}. Quantile-quantile plots for these figures of merit which corroborate these observations are shown in Fig. 5 for the reference device and NCFETs with different ferroelectric thicknesses. Similar results were reported in a recent study on geometrical process variations in negative capacitance based FinFETs using a compact modeling approach [5].

IV. Conclusion

We have shown that the negative capacitance effect of the ferroelectric in an NCFET can result in higher immunity towards statistical variability induced by random discrete dopants in the transistor channel. In particular, NCFETs show reduced RDD induced V_t and I_{OFF} variability with the immunity increasing with increase in the ferroelectric thickness. On the other hand, the variability in the ON-state current is not a monotonic function of the ferroelectric thickness.

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Steep Slope Negative Capacitance FDSOI MOSFETs with Ferroelectric $HfYO_X$

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***Abstract*— Negative capacitance MOSFETs on FDSOI with sub-thermal subthreshold swing (SS) were demonstrated. SS of 30 mV/dec was achieved for 3 decades. We found that the sub-thermal SS degrades with the sweeping numbers, which is caused by the traps in the gate oxide.**

Keywords-negative capacitance MOSFET, steep slope, Ferroelectricity

I. Introduction

Negative capacitance (NC) MOSFETs have been proposed to conquer the thermal limit of subthreshold swing of conventional MOSFETs, because of the intrinsic voltage amplification provided by the ferroelectric gate oxide [1]. The presence of NC in experiments is elusive. Although NC MOSFETs have been demonstrated, a reliable methodology to NC is still absent. The capacitance matching, oxide quality, domain dynamics and other factors influencing the performance of NC MOSFETs need to be investigated [2, 3]. In this work, we present NC MOSFETs fabricated on SOI with $HfYO_x$. The effects of traps in the ferroelectric layer are studied.

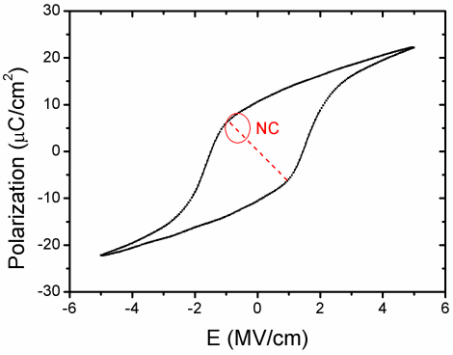

Figure 1. P-E curve of TiN/10 nm $HfYO_x$/TiN capacitor.

II. Device Fabrication

NC MOSFETs were fabricated on 20 nm SOI wafers with a 145 nm thick buried oxide layer. Photolithography and reactive ion etching were used to define the mesa. An amorphous $HfYO_x$ layer was deposited by Atomic Layer Deposition (ALD) with a thickness of 5 nm. 60 nm TiN was deposited by sputtering as metal gate. RTP at 700 °C in Ar atmosphere was performed for 30 s to both crystallize the $HfYO_x$ into orthorhombic phase and activate the S/D dopants. The final device has a gate width (length) of 2 (2) μm.

III. Results and Discussion

The ferroelectricity of the $HfYO_x$ layer was characterized by the polarization measurement on a TiN/$HfYO_x$/TiN capacitor with a 10 nm $HfYO_x$ layer. The P-E curve in Fig. 1 shows typical ferroelectric hysteresis, with a remnant polarization of 12 μC/cm^2 and a coercive electric field (E_c) of 1.44 MV/cm.

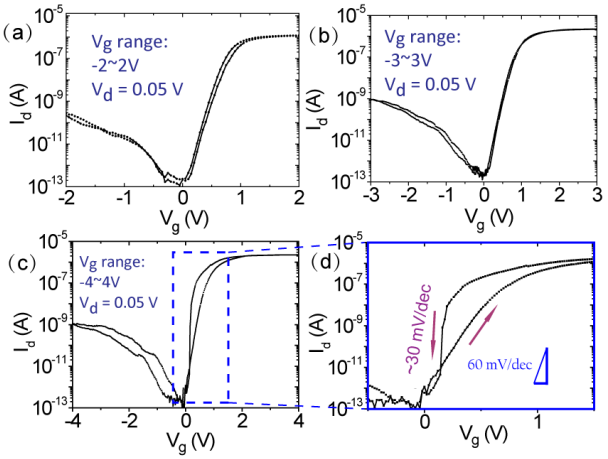

Figure 2. Transfer characteristics of an NC MOSFET with various V_g sweeping rang of: (a) -2~2V; (b) -3~3V; and (c)-4~4V. (d) Enlargement of the subthreshold region in Fig. 2(c), showing a sub-thermal SS.

Fig. 2 shows the transfer characteristics of an NC MOSFET with an $HfYO_x$ thickness of 5 nm for different gate voltage sweeping ranges of (a) -2~2V; (b)-3~3V and (c) -4~4V. At a V_g sweeping range smaller than 4V, the transfer curves show small clockwise hysteresis without steep slopes (< 60 mV/dec), as indicated in Fig. 2 (a) and (b). However, once the gate voltage increased to 4V and swept backward, steep slopes as small as 30 mV/dec were observed (Fig. 2(c)), and clearly shown in the enlarged view of Fig. 2(d). In this case the transfer curves show a counter clockwise hysteresis, in contrast to the clockwise hysteresis in Fig. 2(a) and 2(b), indicating the ferroelectricity in the $HfYO_x$ layer is only activated at such a high voltage. The fact that sub-thermal SS only exists in the reverse sweeping direction after high gate voltage application is due to the adequate domain

polarization at +4V and the successive domain flips in the subthreshold region, causing the NC effect located at the left side of the NC line in the P-E curve (as indicated in Fig. 1 with the red circle and the dashed line).

The reverse SS of the NC MOSFET is shown in Fig. 3. The sub-thermal SS extends over 3 decades. The average of the sub-thermal SS is ~30 mV/dec, with a minimum SS of 8 mV/dec.

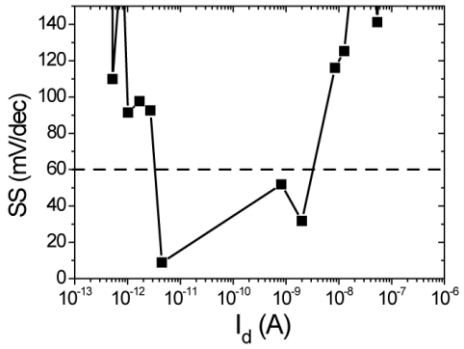

Figure 3. SS of the NC MOSFET extracted from the backward sweeping in Fig. 2(d).

The NC MOSFET suffers SS degradation after cycle-sweeping measurements as shown in Fig. 4. A measurement sequence was performed on the same device with the same bias condition (V_g=4~-0.5V, V_d=0.05V). As the measurement sequence goes, the current range with sub-thermal slopes shrinks and finally vanishes. The threshold voltage shifts towards left side.

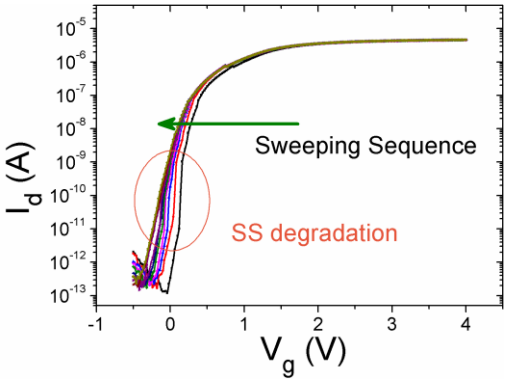

Figure 4. SS degrades with sweeping numbers.

We assume the degradation of SS is caused by the electrically enhanced traps inside the ferroelectric oxide layer. The traps cause a clockwise hysteresis of the transfer curves at low gate voltages as shown in Fig. 2 (a) and (b) [4]. We analyzed the trap effects as following: after each measurement sweeping from 4V to -0.5V as shown in Fig. 4, the forward and backward I_d-V_g curves sweeping from -2V to 2V were measured. The clockwise hysteresis caused by traps (trap hysteresis) was extracted from the I_d-V_g curves (Fig. 5(a,b)). Fig. 5(c) shows the trap hysteresis for the first and last measurement in Fig. 5(a) for a clear view. The trap hysteresis as a function of the sweeping numbers was plotted in Fig. 5(d), which shows a hysteresis increase, indicating increasing density of traps with cycle measurements. Therefore, the results shown in Fig. 4 is caused by the effects of both NC and traps. In other words, traps might suppress the NC effect. The traps may arise from the oxygen vacancies in the $HfYO_x$. The high electric field needed to activate the ferroelectricity can generate more oxygen vacancies or force the existing oxygen vacancies mobile, acting as traps. The presence of NC effect requires a dedicate charge balance, i.e. an imperfect screening of the polarization, which can be degraded by the charged traps.

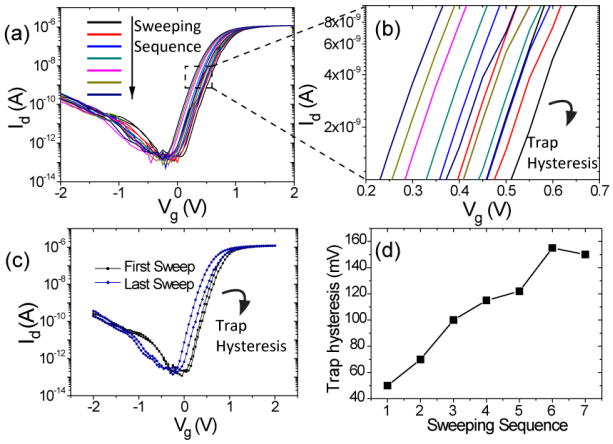

Figure 5. (a) Transfer curves swept at V_g=-2~2V, showing the trap hysteresis. (b) Enlarged view of the trap hysteresis. (c) Trap hysteresis for the first and last measurements in (a). (d) The trap hysteresis increasing with sweeping numbers.

IV. Conclusion

NC MOSFETs on FDSOI have been demonstrated. Sub-thermal SS of 30 mV/dec has been achieved for 3 decades. The SS degrades with the sweeping numbers, which is caused by the trap increase in the oxide layer. Thus, high quality oxide with a better channel interface is essential for the presence and stabilization of NC effect.

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Electrical Characterization of HfO_2 Based Resistive RAM Devices Having Different Bottom Electrode Metallizations

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***Abstract*— HfO_2 based resistive RAM devices as the important candidates of future non-volatile memory technology were investigated using state of art physical and electrical characterization methods. Memory stacks used for measurements, named MARS, having four different bottom electrode materials fabricated by CEA-LETI and ASM cooperation. The effects of bottom electrode metallization on forming, switching and capacitive characteristics were studied and most efficient combinations were determined among these structures. It was observed that devices having atomic layer deposited (ALD) bottom electrode have some capacitive properties. Also TiN and TiWN bottom electrodes have promising switching characteristics and low operation voltages.**

Keywords-Resistive RAM, RRAM, OxRAM, HfO_2, resistive switching, non-volatile memory, resistive memıory.

I. INTRODUCTION

The need for investigating new types of non-volatile memory devices arises from the inadequacy of currently dominant Flash memory against the developments in the semiconductor memory manufacturing technology [1-2]. HfO_2 based resistive RAM devices are the most promising emerging memory type in order to meet the requirements in the new technology nodes [3-4]. These devices have really good scalability, low operation power, high density, reliability, good endurance and retention and they are compatible with the CMOS technology [5-6]. In this paper, it was aimed to determine the most efficient device configuration by comparing different bottom electrode structures and their effects on the performance and reliability.

II. TECHNOLOGICAL DETAILS

MARS memory devices as fabricated by CEA-LETI and ASM cooperation having four different bottom electrode (BE) structures are showed in Fig. 1. All memory stacks have 10nm atomic layer deposited (ALD) HfO_2 layer as the resistive switching medium and 50nm TiN top electrode over a 10nm Ti layer. One of the devices has physical vapor deposited (PVD) TiN bottom electrode and it is considered as the reference stack. The other three devices have additional ALD deposited TiN, TiWN and WN layers as the bottom electrode.

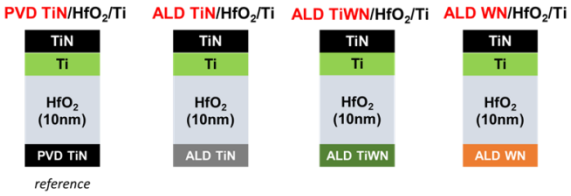

Figure 1. Cross sections of HfO_2 based MARS samples having four different bottom electrode structures.

A Keithley 4200 semiconductor characterization system and an HP4192A impedance analyzer with probe stations were used for quasi-static current-voltage and impedance measurements. Since the devices have two terminal 1R structures, two probes were used to get electrical contact from the 80µm^2 top and bottom contact pads of the samples.

III. RESULTS AND DISCUSSION

In Fig. 2, initial resistances measured for 20 different cells of each memory are shown. The reference PVD BE stack showed a wide dispersion about 4 decades. Initial resistance of ALD BE TiN stack is lower and more dispersed compared to other ALD bottom electrodes.

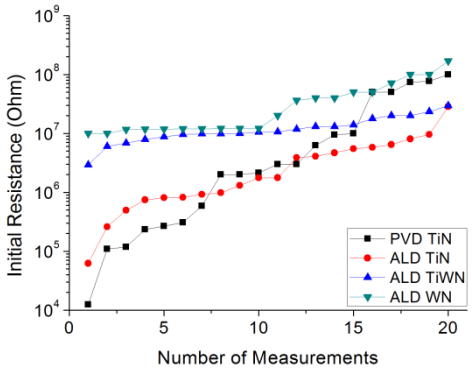

Figure 2. Initial resistance distributions measured over 20 cells of each memory.

Forming voltage distributions measured for 20 cells of each memory stack are shown in Fig. 3. The reference PVD BE TiN has a forming voltage of 1.5V and wide voltage dispersion similar to its initial resistance values. ALD BE TiN has the lowest forming voltage of 1.3V and its distribution is slightly higher than the other ALD BEs. The forming voltages of ALD BE TiN and WN are 2.5V and 2.7V respectively.

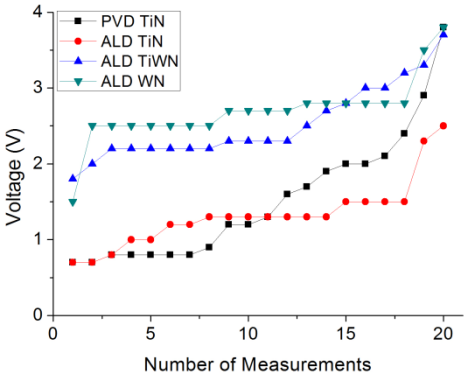

Figure 3. Forming voltage distributions measured over 20 cells of each memory.

In Fig. 4, the averages of 5 quasi-static cycles performed on 4 different cells of each memory are shown. Resistive switching was observed on all memory devices except ALD BE WN. For PVD BE TiN, Reset voltage is -0.8V and Set voltage is 0.5V. For ALD BE TiN, Reset voltage is -0.5V and Set voltage is 0.5V. For ALD BE TiWN Reset voltage was found -1V and Set voltage is 0.6V.

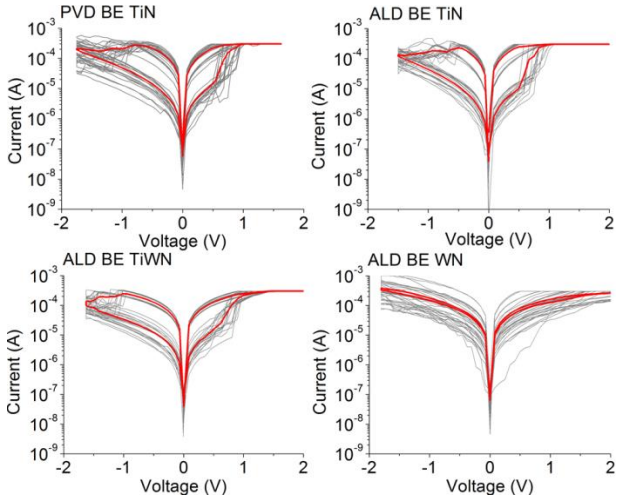

Figure 4. Quasi-static switching cycles performed on each memory at 300μA compliance current.

The evolution of low resistive state (LRS) and high resistive state (HRS) during 10 quasi-static cycles performed on 3 different cells for all BEs are shown in Fig. 5.

The highest memory window (2 decade) was observed on some cells of PVD BE TiN but its high resistive state showed a high dispersion. ALD BE TiN also has a high memory window (more than one decade) and its HRS is more stable than PVD BE TiN. ALD TiWN has a lower memory window compared to others and its HRS dispersion is medium. As mentioned before, since no switching was observed on ALD BE WN, its memory window values could not be evaluated indicating the worse case among others.

Frequency dependent capacitance measurements were done on four memory device by sweeping frequency 1kHz to 7MHz at a 100mV rms voltage as shown in Fig. 6. ALD BE memories showed capacitive behavior but PVD BE TiN did not show any capacitive property.

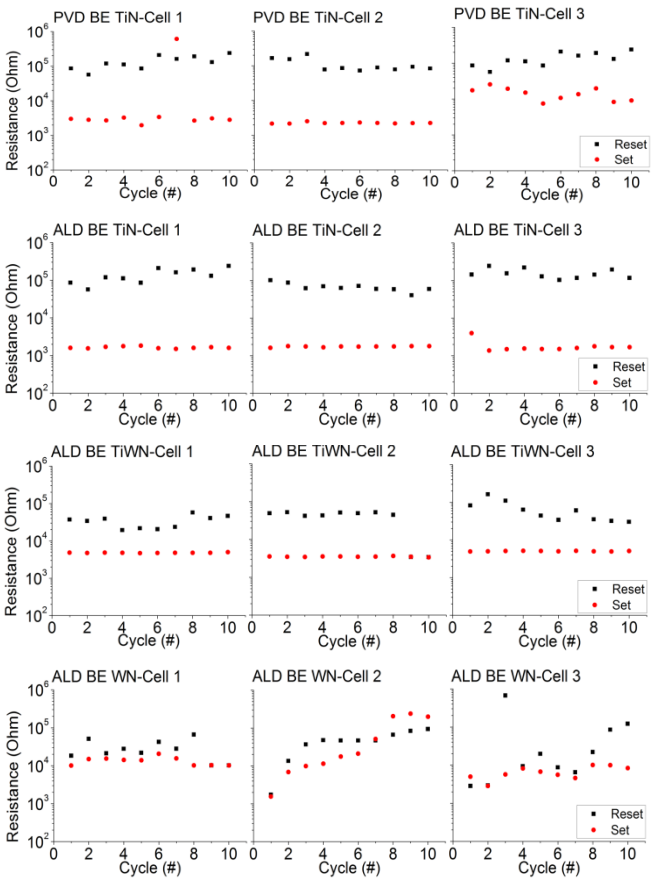

Figure 5. Resistance difference between reset and set states (memory window) of each memory.

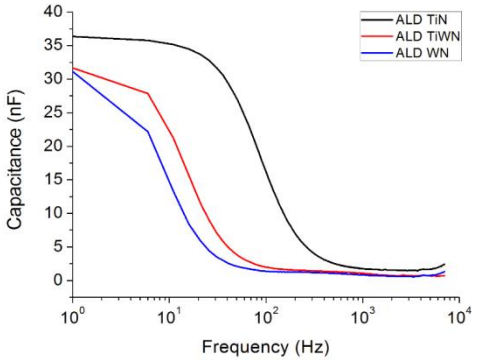

Figure 6. Frequency versus capacitance measurement on ALD BE memories.

IV. Conclusion

In the scope investigating optimum bottom electrode configuration for HfO_2 based resistive RAM devices, quasi-static I-V and frequency dependent capacitance measurements were done. According to the results, devices having ALD BE layer are more promising in comparison with the PVD. Especially ALD BE TiN and TiWN have very low operation voltages which is an important property for low power applications. Their average forming voltages among 20 memory cells are 1.3V and 2.5V respectively. They also have 0.5V Set voltage but Reset voltage of TiWN is slightly higher than

28 FDSOI Analog and RF Figures of Merit at Cryogenic Temperatures

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***Abstract*—This work presents a detailed characterization of 28 nm FDSOI CMOS process at cryogenic temperatures. Electrostatic, Analog and RF Figures of Merit (FoM) are studied for the first time to our best knowledge. At cryogenic temperatures, 20-70% enhancement of I_d and g_{m_max} values as well as up to 100 GHz f_T increase are demonstrated. Temperature behavior of analog and RF FoMs is discussed in terms of mobility and series resistance effect. This first study suggests 28FDSOI as a good contender for future read-out electronics around qubits.**

Keywords-FDSOI;UTBB;Analog and RF FoMs;Cryogenic

I. INTRODUCTION

28 FDSOI technology has already demonstrated improved DC, analog and RF performances at room temperature (RT) [1][2]. Our present work extends those studies and investigates, for the first time to the best of our knowledge, the potential of the technology for future cryogenic applications, such as e.g. read-out circuitry of quantum bits ("qubits") by an integrated control system [3]. Nowadays high interest for quantum computing is motivated by a strong enhancement of computational power at deep cryogenic temperatures [4]. Influence of cryogenic temperature on 28 nm bulk technology was already demonstrated with a main focus on analog parameters and EKV model [4]. In this paper, we investigate electrostatic, analog and RF figures of merit (FoMs) of nMOSFETs from 28FDSOI with different gate lengths in a temperature range down to 77K. Our focus is on the main MOSFET parameters and FoMs, such as threshold voltage (V_{th}), subthreshold slope (SS), transconductance (g_m), transconductance-to-drain current ratio (g_m/I_d), Early voltage, intrinsic gain (A_v), and current gain cutoff frequency f_T.

II. DEVICE AND MEASUREMENT DETAILS

Devices studied in this work come from 28 FDSOI process by ST-M with gate lengths L_g from 25 to 90 nm. The Si film, BOX and the equivalent gate oxide thicknesses are 7, 25 and 1.3 nm, respectively. Channel is left undoped. More process details can be found in [5]. Studied nMOSFETs feature 60 fingers of 2 µm width, embedded in CPW pads for RF characterization. I-V and S-parameters measurements were done down to liquid nitrogen temperature (77K).

III. RESULTS AND DISCUSSION

A. Electrostatic parameters

Fig. 1 shows typical transfer I_d-V_g and g_m-V_g plots obtained in linear (V_d =50 mV) and saturation (V_d = 1 V) regimes for 77K and 300K for the 30 nm-long device. Threshold voltage (V_{th}) is increasing by ~0.1 V with temperature, T, reduction from 300 to 77 K. This is smaller than reported previously for 28 bulk technology [4]. Contrarily to bulk device, V_{th} variation in fully depleted device is only due to Fermi level potential variation and is shown to be strongly attenuated in ultra-thin devices [6][7]. $\Delta V_{th}/\Delta T$ is ~ 0.5 mV/°C which agrees well with numbers reported for high-temperature variation in thin-film MOSFETs [6][7]. Next to that, SS improves at 77K. However, this improvement is not as strong as one could expect from the theoretical proportionality to T. Moreover, the improvement is lesser in shortest devices, as was already pointed out for the bulk counterparts [4]. Attenuated SS improvement with temperature could be related to the interface traps- and body factor -related effect.

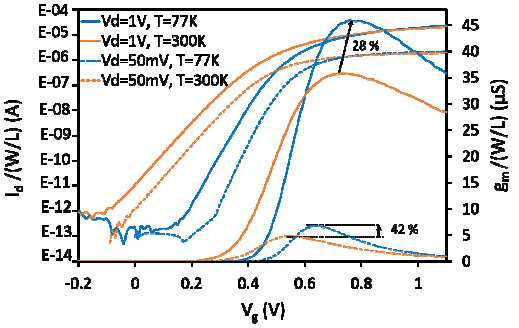

Fig. 1. I_d-V_g and g_m-V_g curves at 77K and 300 K. L_g=30 nm.

B. DC Analogue Figures of Merit

Fig. 2 shows g_m/I_d as a function of normalized I_d extracted at 300 and 77 K for 30 nm and 60 nm-long devices. One can see the g_m/I_d maximum improvement (directly linked with SS increase) as well as enhancement of $I_{d\_norm}=I_d/(W/L)$ at a fixed g_m/I_d (both in moderate and strong inversion regimes). Extraction of I_{d_norm} at a fixed g_m/I_d allows removing the effect of V_{th} shift with temperature. Fig. 3 shows I_{d_norm} taken at g_m/I_d=10 and 5 V^{-1} (which correspond to ~V_{th}+0.2 and +0.4 V, respectively) and maximum g_m for various gate lengths for 77 and 300 K. Improvement of g_{m_max} and I_{d_norm} is 20 to 70% depending on the gate length and regime of operation. These values are comparable with the observations for the 28 nm bulk technology [4]. There are two reasons for the reduced improvement of g_{m_max} and I_{d_norm} in short channels. Firstly, effect of series resistance, R_{sd}, (known to increase at lower temperatures) is stronger. This reason is supported by stronger improvement observed for the regimes at which the impact of series resistance is smaller, as e.g. i) I_{d_norm} taken at g_m/I_d =10 V^{-1} w.r.t taken at 5 V^{-1} and ii) g_{m_max}

extracted in linear w.r.t saturation regime (Fig.1). Secondly, mobility, μ, improvement in short channel devices is smaller than in long ones, as reported previously [8]. Indeed, short-channel mobility is strongly affected by the presence of defects in the extensions and source/drain regions. Resulting mobility temperature dependence is defined through the balance between two mechanisms: Coulomb scattering on the defects (with μ_{coul} reduction with T lowering) and phonon scattering (with μ_{ph} increase with T lowering). Furthermore, improvement rate first slows down with temperature lowering and then drops exhibiting a maximum at ~100 K (not shown due to lack of space).

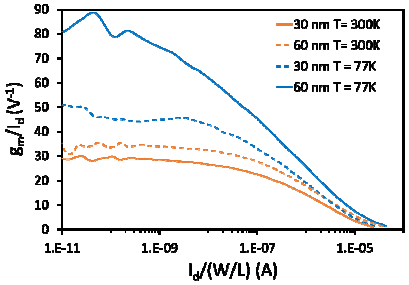

Fig. 2. g_m/I_d vs. $I_d/(W/L)$ at 77K and 300K. L_g = 30 and 60 nm.

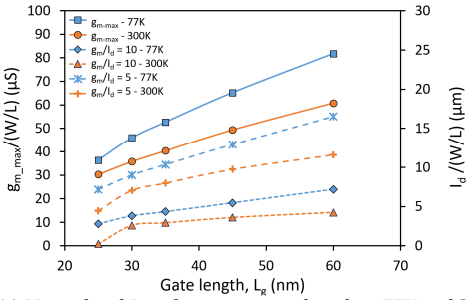

Fig. 3. (a) Normalized I_d and g_{m_max} vs gate length at 77K and 300K.

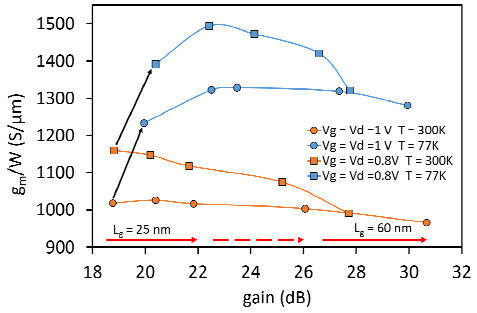

Fig. 4. Normalized g_m versus gain at 77K and 300K.

Fig. 4 shows g_m-A_v metric widely used for comparative assessment of analog FoM of technology. One can see that temperature lowering results in simultaneous g_m and A_v improvements (except for the longest device showing almost invariable A_v). However, the improvement is smaller in shortest devices for the reasons discussed above.

C. RF FoMs

Fig. 5a shows one of the main RF FoMs i.e. current gain cutoff frequency f_T versus gate length at 77K and 300K in saturation and at V_g that corresponds to maximum g_m. It is extracted by extrapolation of H_{21} parameter to 0 dB. This advanced technology node is known to feature very high f_T reaching several hundreds of GHz at RT [1] and [9]. Temperature reduction from 300K to 77K results in strong f_T improvement (due to μ and, hence, g_m improvement). This increase ($\Delta f_T = f_{T\_77K} - f_{T\_300K}$) becomes particularly significant in shorter devices (inset in Fig. 5a). f_T temperature dependence for 25 nm device is illustrated in Fig. 5b. Temperature dependence exhibits a maximum at 100 K (similarly to DC g_{m_max} and I_d improvements discussed above). The same trends are observed in RF "extrinsic", g_{me}, (i.e. including R_{sd}), and "intrinsic", g_{mi}, (i.e. without R_{sd} effect) values extracted from S parameters measurements [1] (inset in Fig. 5b). As the same shape is observed both in g_{me} and g_{mi} curves, we can suggest that the main reason of such trend is related to the μ(T) dependence, discussed above.

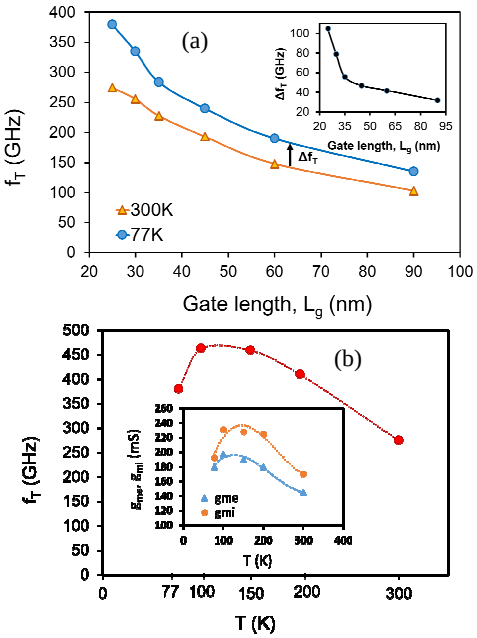

Fig. 5. (a) f_T versus L_g at 77K and 300K. The f_T improvement at 77K, $\Delta f_T = f_{T\_77K} - f_{T\_300K}$ vs. L_g is shown in the inset, (b) f_T versus temperature for L_g = 25nm. The inset shows g_{me} and g_{mi} versus temperatures.

IV. CONLUSION

Potential of 28 FDSOI MOSFETs for future cryogenic applications has been assessed for the first time. Electrostatic, analog and RF FoM have been considered. Threshold voltage was shown to be more stable versus temperature than in the bulk counterpart. Temperature reduction down to 77 K has been shown to result in improvements of g_{m_max} and I_d (20-70%), f_T (~100 GHz) as well as stable gain suggesting 28FDSOI as a promising candidate for the cryogenic circuits' implementation. Analog and RF FoM behaviors at cryogenic temperature have been discussed in terms of mobility and R_{sd} effect. The work will further be extended to the temperature range down to 4.2 K.

ACKNOWLEDGMENT

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Cryogenic Operation of Ω-Gate p-type SiGe-on-Insulator Nanowire MOSFETs

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1. Abstract

This work evaluates the operation of p-type $Si_{0.7}Ge_{0.3}$-on-insulator (SGOI) nanowires (NWs) from room temperature (T) down to 5.2K. Electrical characteristics are shown for long channel devices comparing narrow Ω-gate to quasi-planar MOSFETs (wide fin width – W_{FIN}). Results show oscillations in both transconductance (g_m) and gate to channel capacitance (C_{GC}) curves for T smaller than 50K for W_{FIN}=20nm due to quantum confinement effects. Improvement of the effective mobility (μ_{eff}) for SGOI in comparison to SOI NWs is still observed for NW width scaled down to 20nm. Similar phonon-limited mobility contribution (μ_{ph}) dependence on T is obtained for both narrow SGOI and SOI NWs.

2. Introduction

NWs have shown to be a promising alternative for future technological nodes, allowing the continuity of the CMOS roadmap due to reduced short channel effects and great scalability [1], [2]. In order to fulfill higher drive current requests for p-MOSFETs, compressively strained SiGe materials have been investigated in multiple gate structures, showing significant advantages thanks to hole mobility enhancement [3], [4]. In this work we present performance and transport of p-FET SGOI NWs operating down to cryogenic temperatures. The analysis is performed as a function of W_{FIN} and results are compared to SOI p-FET NWs. Threshold voltage (V_{TH}), subthreshold slope (S), DIBL, g_m, C_{GC} and μ_{eff} are evaluated and discussed.

3. Devices Fabrication

Ω-gate [110]-oriented SGOI NWs have been fabricated at CEA-LETI with 145nm BOX thickness, $Si_{0.7}Ge_{0.3}$ channel of 13nm (H_{FIN}), $Si_{0.7}Ge_{0.3}$:B raised S/D, gate stack composed by HfSiON/TiN giving effective oxide thickness (EOT) of 1.4 nm and channel length of 10µm. SOI NWs used for comparison present same gate stack and similar dimensions. Devices with W_{FIN}=10µm have a single fin while narrower transistors are multiple finger structures of 50 fins. Further fabrication details can be found in [2], [4], [5]. For SGOI devices, the channel is in biaxial compression for wide devices (typically W_{FIN}>240nm), corresponding to ~2.1GPa, whereas strain relaxation occurs on the edge for narrower transistors, leading to uniaxial compressive stress along [110] direction [4].

4. Results and Discussion

Figs. 1 and 2 presents V_{TH}, S and DIBL as a function of T for NWs with W_{FIN}=20nm and 10µm. Fig. 1 shows lower V_{TH} for SGOI devices in comparison to SOI ones due to lower band gap for cSiGe and E_V band offsets [6]. Besides, quasi-planar MOSFETs show stronger temperature dependence ($\Delta V_{TH}/\Delta T$) in comparison to narrow NWs because of increased surface potential variation with T as previously discussed in literature for FinFETs [7]. Fig. 2a shows S results similar to the theoretical limit (dashed line), following linear T dependence down to 100K and then increasing due to higher effective trap density under cryogenic operation [8]. Fig. 2b reveals lower DIBL with T reduction because of stronger channel coupling and therefore higher immunity against V_{DS} influence [9]. Narrow SGOI NW DIBL stabilizes close to ~2mV/V at 100K, as expected for long channel transistors, showing excellent channel immunity do DIBL.

Transconductance results as a function of V_{GS} are shown for SGOI NW with W_{FIN}=20nm varying T from 300K down to 10K in Fig. 3a. It is possible to observe oscillations for T≤50K, indicating holes are confined in two directions (across fin height and width), energy subbands are formed and density of states becomes one-dimensional (1D DoS) [10]. Temperature reduction allows the observation of g_m oscillations because thermal energy (ϕ_T=4.3meV at 50K) becomes lower than energy difference between subbands, so mobility degradation due to inter-subband scattering is clear even when the NW has both H_{FIN} and W_{FIN} larger than 10nm (usual dimension from which quantum confinement effects are expected at room temperature [10]). Fig. 3b shows that g_m oscillations disappear for wider NWs and devices with W_{FIN}>40nm do not show any oscillation even at 10K. Fig. 4 presents g_m oscillations dependence on V_{DS} at 5.2K (a) and 50K (K) for SGOI NW with W_{FIN}=20nm. When the thermal energy is very low (ϕ_T=0.45meV at 5.2K) and V_{DS} is -10mV, 4 distinguished peaks are observed at V_{GS} positions indicated by dotted lines. When V_{DS} is much higher than energy separation between subbands, oscillations can no longer be observed, as in Fig. 4a at V_{DS}=-100mV. Fig. 4b shows that the two last peaks are barely seen at 50K even at V_{DS}=-10mV, indicating that thermal energy must be higher than the energy levels difference between the two subbands. Fig. 5a shows $C_{GC}(V_{GS})$ for SGOI NW with W_{FIN}=20nm varying T from 300K down to 5.2K. As previously investigated in [11], oscillations are also observed in C_{GC} in relation with 1D DoS. Fig. 5b presents μ_{eff} extracted by split C-V as a function of inversion charge density (N_{inv}) for SGOI NW with W_{FIN}=20nm at T=5.2K and V_{DS}=-10mV and -40mV. Very smooth oscillations at V_{DS}=-10mV are noticed at N_{inv} values (dotted lines) corresponding to V_{GS} where g_m peaks are identified in Fig. 4. Although g_m peaks are still observed in Figs. 3 and 4 at V_{DS}=-40mV, μ_{eff} oscillations have already disappeared at this V_{DS} value.

Fig. 6 compares $\mu_{eff}(N_{inv})$ varying T of SOI (a) and SGOI (b) NWs with W_{FIN}=20nm. Improvement in SGOI NWs due to higher mobility in uniaxial compressively strained $Si_{0.7}Ge_{0.3}$

reaches 61% and 86% at 300K and 10K, respectively. Fig. 7 shows $\mu_{eff}(W_{FIN})$ for different T at $N_{inv}=0.8\times10^{13}cm^{-2}$ for SOI and SGOI NWs. Due to hole mobility enhancement in (110)-oriented sidewalls in comparison to (100) inversion surface, SOI NWs μ_{eff} increases 18% from quasi-planar NWs down to W_{FIN}=20nm at 300K. On the other hand, mobility in SGOI NWs shows almost no dependence with W_{FIN} below 100nm. The better hole mobility expected for SiGe (110)//[110] oriented sidewall channel with respect to SiGe(100)//[110] one [12] may be overridden by the higher strain effect in uniaxial compressed SiGe(100)//[110] [13]. However, a slight mobility decrease for the narrowest dimension (W_{FIN}=20nm) is observed, which may be due significant corner effects that have been evidenced in scaled TG-NWs [14]. Fig. 9a shows that maximum mobility (μ_{max}) is approximately constant below 100K as surface roughness limited contribution (μ_{SR}) dominates at these low temperatures. Besides, μ_{SR} is lower for narrow NWs because of lateral interface quality [11]. Since $\mu_{eff}^{-1}=\mu_{ph}^{-1}+\mu_{sr}^{-1}$ at high N_{inv} [15], μ_{ph} has been estimated by subtracting μ_{eff}^{-1} measured at a given T≥100K from μ_{eff}^{-1} at 10K, because μ_{sr} does not depend on T and limits μ_{eff} at bellow 100K. Fig. 8b shows very close temperature dependence coefficient (γ) extracted from linear regression of $\mu_{ph}(T)$ [15] curves for both SGOI and SOI NWs with W_{FIN}=20nm, showing slight effect of alloy scattering and of strain on phonon limited mobility [16].

1. Conclusions

SGOI NWs have been studied down to 5.2K. Higher $\Delta V_{TH}/\Delta T$ is obtained for SGOI devices in comparison to SOI NWs with same W_{FIN}. Clearer g_m and C_{GC} oscillations due to 1D DoS have been observed decreasing T, W_{FIN} and V_{DS}. Mobility enhancement due to SiGe channel material remains as high as 38% for narrow NWs down to 20nm. Similar temperature dependence coefficient is obtained for narrow SGOI (-3.1) and SOI (-3.3) NWs.

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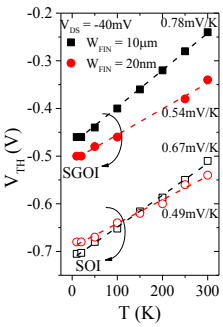

Fig.1: *Threshold voltage as a function of temperature for quasi-planar and narrow p-NWs SOI SGOI at V_{DS}=-40mV.*

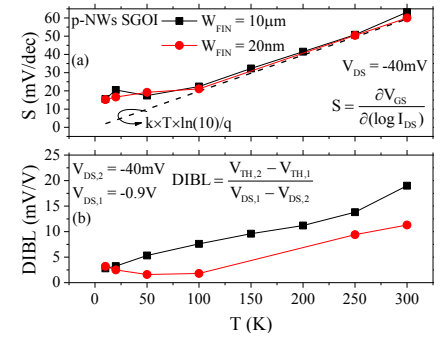

Fig.2: *Subthreshold slope (a) and DIBL (b) as a function of temperature for quasi-planar and narrow p-NWs SGOI. Dashed line in (a) indicates the theoretical limit for S calculated by k×T×ln(10)/q. Channel length is 10μm.*

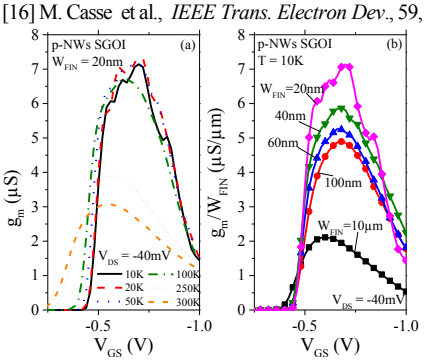

Fig.3: *Transconductance as a function of gate voltage of p-NWs SGOI varying temperature for W_{FIN}=20nm (a) and varying W_{FIN} for T=10K (b), V_{DS}=-40mV.*

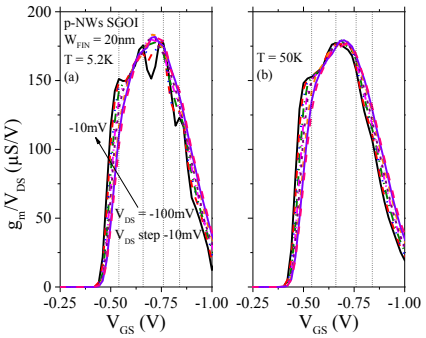

Fig.4: *Transconductance as a function of gate voltage of p-NWs SGOI varying V_{DS} from -10 to -100mV for W_{FIN}=20nm at 5.2K (a) and 50K (b). Dotted lines indicate V_{GS} position of g_m peaks.*

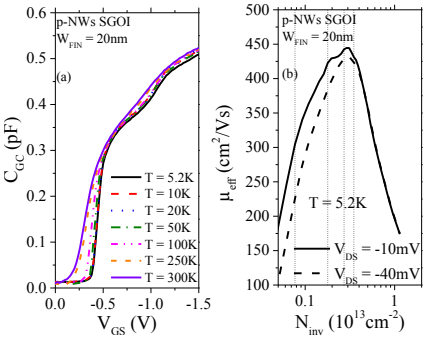

Fig.5: *Gate to channel capacitance as a function of gate voltage (a) and effective mobility as a function of inversion charge density (b) of p-NWs SGOI with W_{FIN}=20nm.*

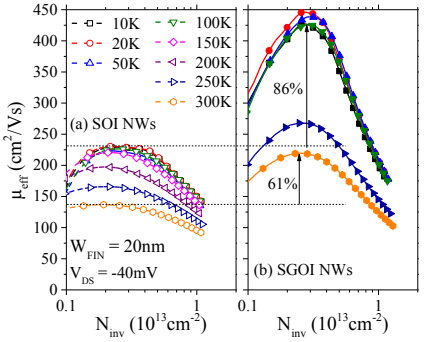

Fig.6: *Effective mobility as a function of inversion charge density for p-NWs SOI (a) and SGOI (b) with W_{FIN}=20nm, varying T from 300K down to 10K and V_{DS}=-40mV*

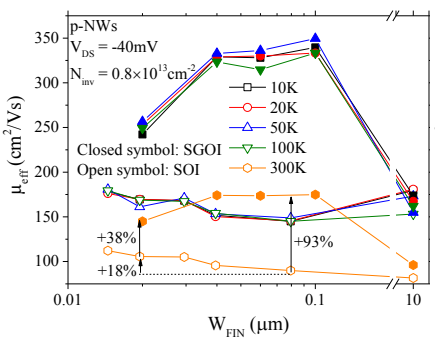

Fig.7: *Effective mobility extracted at N_{inv}= $0.8\times10^{13}cm^{-2}$ and V_{DS}=-40mV as a function of fin width for several p-NWs SGOI and SOI varying T from 300K down to 10K.*

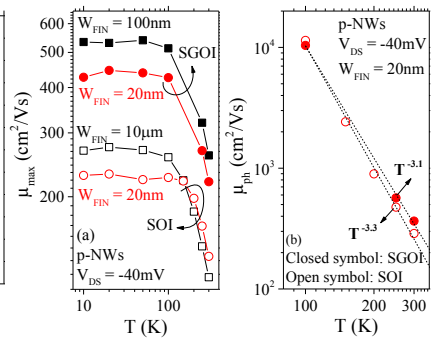

Fig.8: *Maximum mobility (a) and phonon-limited mobility (a) as a function of temperature for p-NWs SGOI and SOI at V_{DS}=-40mV. Dotted lines in (b) indicate linear regression of data points.*

Experimental measurement on GDNMOS and GDBIMOS devices for ESD protection in 28nm UTBB FD-SOI CMOS technology

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***Abstract*— GDNMOS (Gated Diode merged NMOS) and GDBIMOS (Gated Diode merged BIMOS) were fabricated using the 28nm UTBB FD-SOI high-k metal gate CMOS technology. These devices were measured and investigated for ESD protection applications.**

***Index Terms* - Electrostatic Discharges ESD, FD-SOI, GDNMOS, GDBIMOS**

I. INTRODUCTION

Previous studies were conducted on the GDNMOS (Gated Diode merged NMOS) in thin film silicon [1,2]. It is an ESD protection device where a gated diode was merged with an NMOS transistor. The anode and the cathode of the device correspond to the anode of the diode and the source of the MOS respectively. The shared area is located in the cathode of the diode, which is also the drain of the MOS (Figure 1). The GDBIMOS (Gated Diode merged BIMOS) was also simulated and compared to the GDNMOS [3]. This device is composed of a gated diode merged with a BIMOS (Figure 2). A BIMOS [4,5] is an NMOS transistor on which a P+ body contact is placed in order to have access to the channel of the MOS. For ESD applications, this contact and the gate are both plugged to the same resistor.

In this work, we present the experimental measurements for those two types of devices in order to show their robustness to ESD events along with their design window.

II. PRESENTATION OF THE EXPERIMENTS

TCAD simulations are process compliant and meshed in 3D. The surge is an Average Current Slope (ACS) stress [6]. The device were subjected to a current ramp with a maximum of 0.1A and a rise time of 100ns, in order to recreate a Transmission Line Pulse (TLP) test for Human Body Model (HBM). All the structures have 10µm width (1 finger).

Test devices were fabricated using the 28nm FD-SOI ST process in the ultra-thin silicon film. The standard high-k metal gate stack (GO1) was used. All the structures have 100µm total width (10 fingers of 10µm). TLP measurements were performed on several dies with a 10ns rise time and a duration of 100ns at room temperature.

The GDNMOS devices were arranged depending on the biasing conditions and are presented as follow: device 1 corresponds to a GDNMOS with grounded front gates. Devices 2 - 5 have a grounded diode gate and their MOS gate is plugged to a polysilicon resistor (the value of the resistor increases with the device number: $R_1 < R_2 < R_3 < R_4$). Devices 6 - 9 have a grounded MOS gate and their diode gate is plugged to a resistor. Devices 10 – 13 have both gates tied together and plugged to a resistor. The back gate is grounded for all the devices. The measured GDBIMOS devices have all their front gates plugged to a resistor (device 14 – 18). Devices 14 – 17 have a grounded back gate while device 18 has the back gate plugged to a pad in order to apply different biasing conditions.

III. ROBUSTNESS

All the devices that have a grounded diode gate have a robustness issue with an early break (Figure 3, 4). This is because there is no resistor to protect the gate of the diode, which is just next to the anode. The resistor on the diode gate helps the diode gate to be biased through the parasitic capacitance between the anode and the gate of the diode C_{AGD}. Therefore the difference between the anode voltage V_A and the voltage of the diode gate V_{GD} is minimized. Else, without a resistor, the difference of potential between the anode and the diode gate can reach the breakdown voltage of the spacer that lies between them. The value of this resistor should be sufficiently high in order to protect the gate.

A low leakage current around 2nA at 1V is measured on all the devices.

IV. INFLUENCE OF THE FRONT GATE

The ESD behavior of the GDNMOS devices with different biasing conditions on the front gates was investigated.

If the gate of the diode is plugged to a resistor and the gate of the MOS is tied to the ground, the V_{t1} of the structure does not change with the value of the resistor (Figure 5).

In the case where the gate of the diode and the gate of the MOS are tied together and connected to a resistor, V_{t1} decreases (Figure 6). The higher the resistor, the lower the V_{t1}. This is because the parasitic capacitances of both gates are responsible in raising the voltage on the gates through the resistor. A higher voltage on the gates allows the MOS part of the device to conduct current for a lower anode voltage.

TCAD simulations confirm this V_{t1} shift according to the gates biasing conditions (Figure 7).

V. INFLUENCE OF THE BACK GATE

The GDNMOS devices have the same Vt1 as the GDBIMOS devices for a same value of resistor plugged to both of the gates (Figure 8).

The influence of the back gate on the GDBIMOS was investigated. The higher the back plane voltage is, the lower the device triggers (Figure 9). An increase of leakage for an increased positive back plane biasing is observed.

CONCLUSION

In this work, we present the ultrathin film GDNMOS and GDBIMOS devices whose behavior was evaluated using both simulations and measurements. We can note that no SCR behavior and no latch-up were observed. The devices can be used for high-voltage ESD protection due to their good integration. The protections are reconfigurable since the trigger voltage can be shifted according to the gates connectivity.

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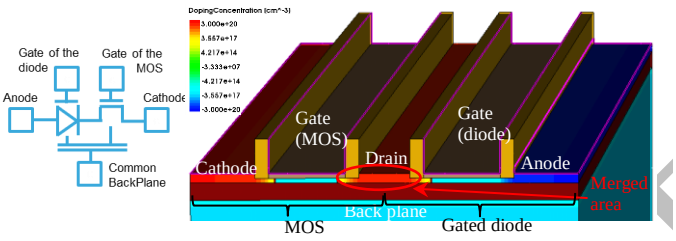

Fig. 1: Schematic (left) and 3D view (right) of GDNMOS structure.

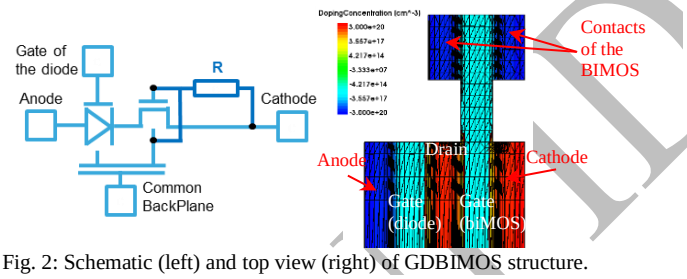

Fig. 2: Schematic (left) and top view (right) of GDBIMOS structure.

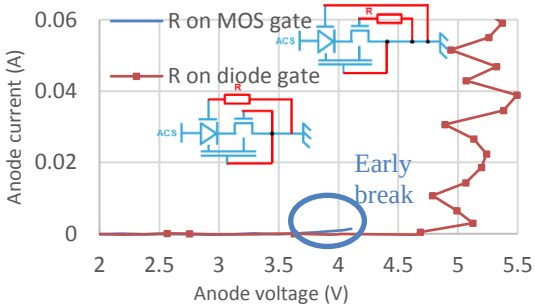

Fig. 3: Multi-trig TLP measurements of device 4 (R on MOS), and of device 8 (R on diode gate).

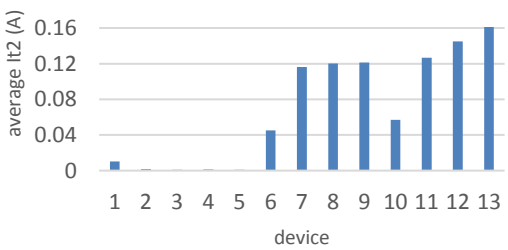

Fig. 4: Average breaking current I_{t2} for each device, extracted from TLP measurements performed on many dies.

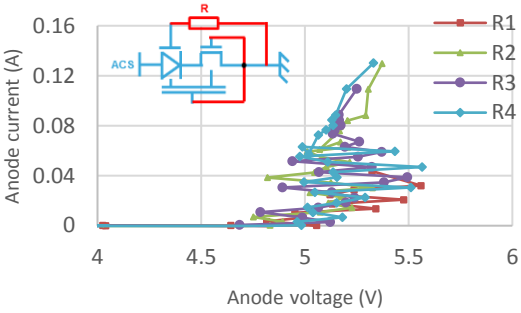

Fig. 5: TLP measurements of a GDNMOS with different values of resistor (R_1 < R_2 < R_3 < R_4 corresponding to device 6 – 9 respectively) plugged to the diode gate. The MOS gate is tied to the ground.

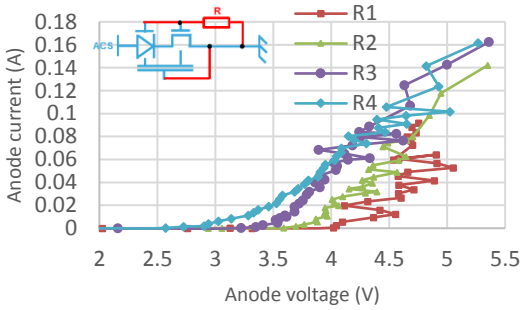

Fig. 6: TLP measurements of a GDNMOS with different values of resistor plugged to both of the gates. (devices 10, 11, 12, 13)

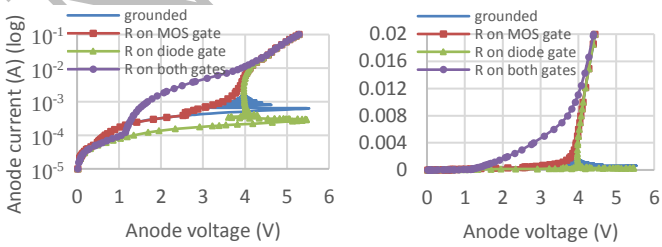

Fig. 7: ACS I-V 3D TCAD simulation of GDNMOS with different biasing conditions: both gates grounded (corresponds to device 1), grounded diode gate and MOS gate plugged to a resistor (device 4), grounded MOS gate and diode gate plugged to a resistor (device 8), and both gates tied together and plugged to a resistor (device 12).

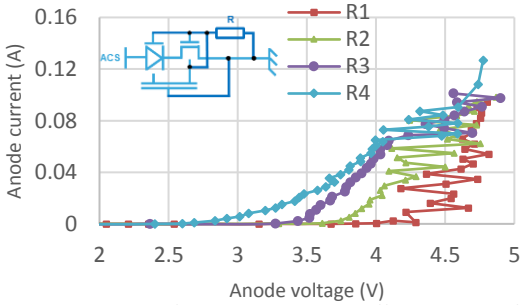

Fig. 8: TLP measurements of a GDBIMOS with different values of resistor plugged to both of the gates. (devices 14, 15, 16, 17)

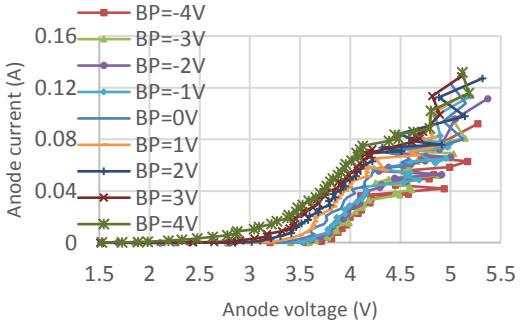

Fig. 9: TLP measurements of a GDBIMOS with different back plane biasing. (device 18)

High-performance GaN HEMT for Power Applications

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***Abstract*—In this work, three different types of gate recessed E-mode GaN MIS-HEMTs were fabricated by different gate oxide stack techniques. The gate oxide stacks were designed with different oxide potential barrier, resulting in the device with different threshold voltages. Each device performance was evaluated, compared and discussed. The proposed device with charge trap gate stack showed the best device performance with high threshold voltage and high maximum drain current density in this work.**

Keywords-GaN;MOSHEMT;Ferroelectric;

I. INTRODUCTION

Gallium nitride (GaN) materials have been widely used for power electronic applications because of its wide bandgap (3.4eV), high saturation velocity (2.5×10^7cm/s), and large breakdown electrical field (3.3 MV/cm). Enhancement-mode (E-mode) GaN high-electron-mobility transistors (HEMTs) have been widely investigated recently for electric vehicle applications due to the simplicity of the circuit design and safety issue.

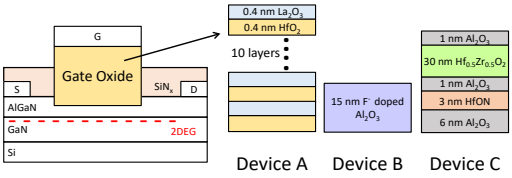

Fig.1 Schematic cross section of the fabricated E-mode GaN MIS-HEMT with three different types of gate oxide stacks (Device A with 10 layers of La_2O_3 (0.4-nm)/HfO_2 (0.4-nm) composite gate insulator. Device B with fluorine doped Al_2O_3. Device C with a novel charge trap gate oxide stack.)

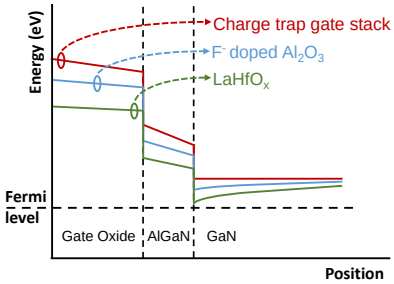

Fig.2 Schematic band diagram of fabricated device with three different gate oxide stacks.

[1]. Several approaches have been demonstrated to achieve E-mode GaN HEMTs in the past, such as recessed-gate , p-type GaN, and fluorine implantation. To effectively suppress ON-state gate leakage current and increase gate swing, E-mode devices have been fabricated by combining recessed-gate and MIS (metal-insulator-gate) approaches [2]. These approaches increase the potential barrier underneath the device gate region to positively shift the threshold voltage. Even though these approaches can achieve the device with E-mode operation, the device performance still cannot satisfy real power device application needs, such as high threshold voltage (>3V), low ON-resistance and large gate swing.

In this work, we compared the device performance of three types of gate recessed E-mode GaN MIS-HEMTs with different gate oxide stack techniques. Device A with the high interface quality composite high-k dielectric as the gate oxide. Device B with fluorine doped gate dielectric. Device C with a novel charge trap gate oxide stack.

II. DEVICE FABRICATION

The epitaxial wafers of the devices were grown by metal-organic chemical vapor deposition (MOCVD) on Si (111) substrate. The wafers consisted of a 1-μm thick GaN buffer layer and a 25-nm-thick $Al_{0.22}Ga_{0.78}N$ barrier layer with a 3-nm undoped GaN cap layer on the top of the structure. The device fabrication started with ohmic contact formation with alloyed Ti/Al/Ni/Au metal stack. Mesa isolation using inductively coupled plasma (ICP) etching was employed to define the active region of the device. For device passivation, in-situ nitrogen plasma treatment was performed using PECVD machine, followed by the deposition of a 50-nm PECVD SiNx layer as the passivation layer. The nitride etch and gate recess were performed by low power ICP-RIE system, the remaining barrier thickness after etch was about 7 nm. The gate oxide deposition was performed by three different methods as shown in Fig.1. For Device A, the composite La_2O_3/HfO_2 was deposited by the molecular beam deposition (MBD) system at 200°C at a pressure of 10-7 Torr. Post-deposition annealing (PDA) at 600°C was performed to improve the oxide film quality. For Device B, 15 nm Al_2O_3 was deposited by ALD system. After gate window was opened, fluorine ions were

directly implanted into the gate region by Varian E500HP ion implanter. The implantation energy and ion dose were 10 keV and $1x10^{12}$ cm^{-2}, respectively. A post–implantation annealing at 400 °C was performed in N_2 ambient. For Device C, 6 nm Al_2O_3/3 nm $HfON/Hf_{0.5}Zr_{0.5}O_2$ was deposited by ALD system. A post–deposition annealing (PDA) at 400 °C was performed in N_2 ambient. Ni/Au was deposited by electron beam evaporation as the gate metal, subsequently. The gate length of all devices was 2 µm, and the gate-to-source and gate-to-drain distances were 3 µm and 15 µm, respectively.

III. Result and Discussion

Fig. 2 shows the schematic band diagram with different gate oxide techniques. Due to the fact that LaHfOx has low energy bandgap (5~6 eV) and high dielectric constant (~23), Device A shows the lowest oxide potential barrier, resulting in the GaN conduction band edge close to the Fermi level at the AlGaN/GaN interface, causing to low threshold voltage for Device A. Device B with the fluorine doped Al_2O_3 gate oxide layer shows higher oxide potential barrier than Device A, which was caused by the negatively charged fluorine ions implanted into Al_2O_3. It is consistent with the previous reports that fluorine ions incorporated into Al_2O_3 could effectively increase the oxide potential barrier due to the negative charge fluorine ions [3]. Device C has a novel charge trap gate oxide stack to trap more electrons into the gate oxide stack. After initialization process (applied a high gate voltage at gate electrode to make electron inject into the gate oxide layer), a lot of electrons are trapped in the gate oxide stack, obtaining the much higher potential barrier. As a result, the E-mode GaN MIS-HEMT has a high threshold voltage. The I-V characteristics results of devices are summarized in Table I. Device A shows the lowest hysteresis of threshold voltage (ΔVth) due to the excellent interface quality of LaHfOx film. All devices show good ON/OFF ratio > 10^7, demonstrating the potential for power application due to low static power consumption. Besides, all devices show low ON-resistance (<11 Ω·mm) and high maximum drain current density (> 600 mA/mm). It indicates the channel mobility does not suffer from severe degradation caused by gate recess or fluorine doping. Device C shows the best device performance of high threshold voltage (+4.4 V) with high current density (770 mA/mm) as shown in Fig. 3. This is attributed to the fact that the charge trap gate stack greatly increases the potential barrier due to the electron trapping in the gate stack structure. Furthermore, there is no obvious current reduction before and after electron trapping in the gate stack. In contrast, Device B with fluorine doping achieved higher threshold voltage, but fluorine doping causes the current density reduction due to the mobility degradation. Device A with high-k gate dielectric has low threshold voltage. The device cannot achieve high threshold voltage without the deep recess depth, and that would cause large current degradation.

	Device A	**Device B**	**Device C**
Gate Oxide	$LaHfO_x$	F^- doped Al_2O_3	Charge trap gate stack
$I_{D,MAX}$ (mA/mm)	648	675	770
$G_{m,MAX}$ (mS/mm)	165	106	116
V_{th} (V)	0.4	1.9	4.4
R_{on} (Ω·mm)	9.4	9.5	10.0
Subthreshold Swing(mV/decade)	114	87	100
I_{on}/I_{off} ratio	3.6×10^7	9×10^9	3.1×10^9
Hysteresis(mV)	45.5	100	150

Table I. Comparison of the DC characteristics of fabricated E-mode GaN MIS-HEMT

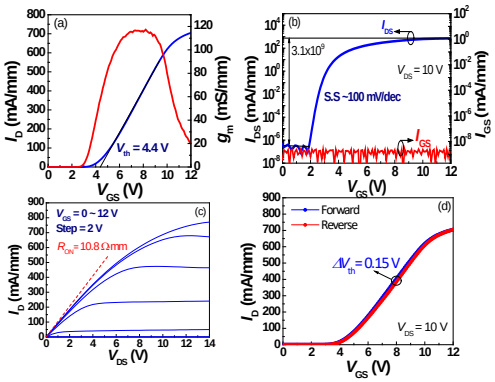

Fig. 3 *I-V* characteristics of Device C with charge trap gate stack: (a) transfer curve curves in linear scale and (b) in the log scale, (c) I_{DS}-V_{DS} curve, and (d) I_{DS} -V_{GS} curve by up and down sweep measurements.

IV. Conclusion

In this work, three gate recessed E-mode GaN MIS-HEMTs were fabricated by different gate oxide stack techniques. Because the gate oxide stacks have different oxide potential barriers, the device performances were different. The device with charge trap gate stack shows the best device performance with high threshold voltage and maximum drain current density as demonstrated. Thus, E-mode GaN MIS-HEMTs with charge trap gate stack is the most promising architecture among the three proposed for future GaN power electronic applications.

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Low-Frequency Noise in Surface-treated AlGaN/GaN HFETs

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***Abstract*— We investigated the 1/f noise generation mechanism in surface-treated AlGaN/GaN heterojunction field-effect transistors (HFETs) with gate length of 2 μm and 20 μm. From the plotting of normalized drain current power spectral density (PSD) S_{Id}/I_d^2 versus I_d, the AlGaN/GaN HFETs with L_g = 2 μm exhibited two distinct noise characteristics; one is Hooge mobility fluctuation (HMF) in subthreshold region and the other is the carrier number fluctuation (CNF) above threshold gate voltage. On the other hand, the device with longer gate of 20 μm follows the correlated mobility fluctuation (CMF), irrespective of the gate bias. The input gate voltage PSD proves that the device with shorter gate length suffers from higher interface roughness scattering.**

Keywords-AlGaN/GaN; HFET; carrier number fluctuation; correlated mobility fluctuation; Low-frequency noise;

I. INTRODUCTION

AlGaN/GaN heterostructure field-effect transistors (HFETs) are most promising devices for high-power and high-frequency (RF) applications due to their excellent material properties, such as wide bandgap, high breakdown voltage and high 2DEG density [1]. However, it is known that the (Al)GaN surface is easily reacted with oxygen atoms in the dielectric layer and forms non-uniform interfacial oxides such as GaO_x and AlO_x during high-temperature RTP needed for the formation of S/D ohmic contacts [2]. This deteriorates the surface morphology which presents poor roughness after the removal of the dielectric layer. It is therefore important to recover the degraded surface prior to the gate metallization since the poor interfacial properties and surface morphology can significantly deteriorate the overall device characteristics.

In this paper, we have fabricated a surface-treated AlGaN/GaN HFETs using a tetramethylammonium-hydroxide (TMAH) plus hydrogen chloride (HCl) solution prior to the gate metallization, which completely removes the interfacial oxide layer to effectively recover the surface of the AlGaN/GaN HFET. The I_{ds}-V_{gs} and the low-frequency noise (LFN) characteristics of the fabricated devices have been measured at low drain bias in order to find the origin of noise mechanism.

II. DEVICE FABRICATION

GaN (3 nm)/AlGaN (14 nm)/GaN heterostructure was grown on sapphire (0001) substrate by MOCVD. For the device isolation, mesa etching was carried out to define the active region by RIE using a BCl_3/Cl_2 gas mixture. 7 nm-thick ALD Al_2O_3 dielectric layer for the surface protection was then deposited at 450 °C and the layer was selectively etched for the source/drain ohmic contacts. Metal stacks for ohmic contact (Si/Ti/Al/Ni/Au) were deposited and followed by two-step RTP at 500 °C for 20 sec and 800 °C for 30 sec in N_2 ambient. 50 nm-thick SiN layer was then deposited by PECVD as a hard mask for the TMAH treatment and patterned for the gate metallization by RIE in CF_4 ambient. The exposed Al_2O_3 layer was first etched in TMAH solution (25 % concentration) and the surface treatment was sequentially performed for 8 min 30 sec plus H_2O:HCl (1:1, HCl) for 30 sec at room temperature. Finally, Ni/Au gate metal was deposited as shown in Fig. 1. The gate lengths of the fabricated AlGaN/GaN HFETs were 2 and 20 μm.

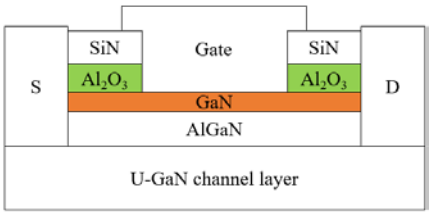

Figure 1. Cross-sectional schematic of the fabricated GaN-cap/AlGaN/GaN HFETs.

III. RESULTS AND DISCUSSION

Fig. 2 shows the I_d - V_{gs} curves in linear region for the fabricated AlGaN/GaN HFETs with two different gate lengths. The devices exhibit normally-on operation with

$V_{th} \approx -1$ V and drain current inversely proportional to the gate length.

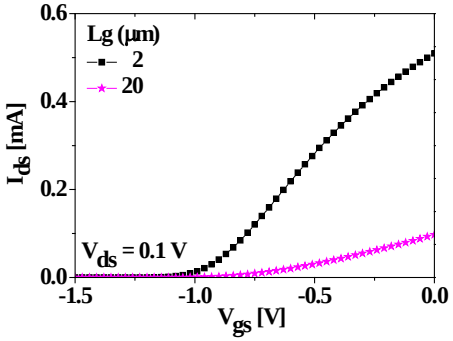

Figure 2. I_{ds}-V_{gs} characteristics at V_{ds} = 0.1 V for various gate lengths.

LFN measurements were performed at room temperature in the linear region (V_{ds} = 0.1 V), using an automatic LFN measuring system by Synergy concept [3]. The gate bias was varied from depletion to strong accumulation. Fig. 3 shows the drain power spectral density in the frequency range of 4 – 10^4 Hz. To find the noise generation mechanism in AlGaN/GaN HFET, the normalized drain current noise according to the drain current was plotted at V_{ds} = 0.1 V and f = 10 Hz. When comparing the S_{Id}/I_d^2 and the $(g_m/I_d)^2$ for both devices, the S_{Vfb} of the AlGaN/GaN HFET with L_g = 2 μm is 3 × 10^{-13} Hz, approximately 10 times larger than that of the L_g = 20 μm. This means that the trap densities in both devices are the same considering their gate lengths. For the AlGaN/GaN HFET with L_g = 2 μm, S_{Id}/I_d^2 curve clearly follows the Hooge mobility fluctuation (HMF) noise model in the subthreshold region and the carrier number fluctuation (CNF) model in the strong accumulation region, because it is approximately proportional to $I_d^{-0.5}$ and I_d^{-2} in each region, as shown in Fig. 3(a). The AlGaN/GaN HFET with L_g = 20 μm, however, follows the CMF noise model since the S_{Id}/I_d^2 is approximately proportional to I_d^{-1} regardless of current level, as shown in Fig. 3(b). This difference in noise behaviour between devices with two different gate lengths indicates that the trapped electrons in the AlGaN barrier layer can further induce the fluctuation of 2DEG mobility in the channel region for longer gate length device. It is also noticed that the S_{Id}/I_d^2 for the longer device is lower than that of the device with 2 μm gate length, which implies that the shorter gate device suffers from higher interface roughness scattering than the device [4]-[5].

ACKNOWLEDGMENT

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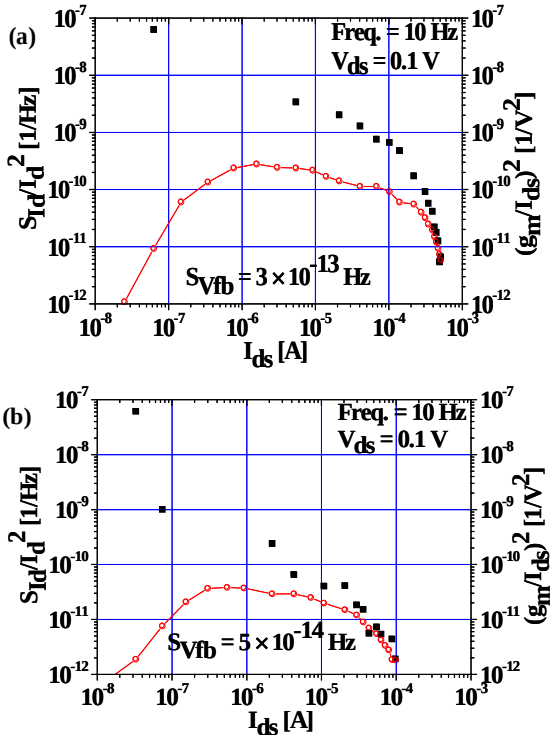

Figure 3. Measured normalized drain current noise spectral density S_{Id}/I_d^2 (black filled square) and $(g_m/I_d)^2$ (red empty circle) versus drain current from subthreshold region to strong accumulation region at f = 10 Hz and V_{ds} = 0.1 V. (a) L_g = 2 μm and (b) L_g = 20 μm.

Discussion on the 1/*f* noise behavior in Si gate-all-around nanowire MOSFETs at liquid helium temperatures

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***Abstract*—In this work, gate-all-around nanowire MOSFETs are studied at very low temperature (4.2 K) and drain voltage, where quantum transport prevails over the usual drift diffusion mechanism. The 1/*f* noise level is investigated in order to study the impact of quantum transport on the noise mechanism.**

1/f noise, MOSFET, Gate-All-Around, nanowire, liquid helium temperature

I. Introduction

Due to their optimal electrostatic control over the channel, silicon Gate-All-Around (GAA) nanowire (NW) MOSFETs are known to be the best solution for reaching sub-10 nm node technological specifications [1]. Moreover studying these devices at liquid helium temperatures is of interest for two reasons. The first one is that cryogenic temperatures are used as operating temperature for certain scientific space missions. The second reason is that low temperatures can enhance several parameters, such as the subthreshold swing and the carriers mobility. In order to provide a further understanding of the transport mechanisms in Si GAA nanowires at very low temperature (4.2 K), static and low frequency noise measurements have been performed.

II. Devices and Methodology

The studied devices have been fabricated at imec (Leuven, Belgium) in order to lead to a comparative study between triple-gate FinFETs and GAA NW FETs built with nearly the same technological process [2]. The transistors are integrated on a Silicon On Insulator (SOI) substrate and consist of non-intentionally doped nanowires. The nanowires are 10 nm wide and 22-23 nm high, giving a total gate width W_G = 325 nm while the gate length is L_G = 50 nm. The GAA stack is made of an interfacial SiO_2 layer, a HfO_2 high-κ dielectric, a TiN EWF gate and a W-fill metal deposition, giving an equivalent oxide thickness EOT = 1.9 nm and a surface gate oxide capacitance $C_{ox} = 1.79 \cdot 10^{-6}$ F·cm^{-2}.

These devices have been biased in their linear operation regime for both static and Low Frequency Noise (LFN) measurements. They have been placed in a Lakeshore TTP4 probe station and the inner temperature has been set at about 4.4 K with a Lakeshore 331 Temperature Controller. An HP 4156B Precision Semiconductor Parameter Analyzer has been used for DC measurements while an HP 3562A Dynamic Signal Analyzer has been used for measuring the noise Power Spectral Densities (PSDs). Both gate voltage noise PSD Sv_g and drain current noise PSD Si_d have been measured.

III. Results and Discussion

A. Quantum transport evidence at 4.2 K

Transfer characteristics $I_{DS}(V_{GS})$ have been measured for several drain voltage V_{DS} values. For low drain voltages (V_{DS} < 5 mV), the transfer characteristics exhibit steps in their evolution, as seen in Fig. 1, whereas they seem to be smoother for higher V_{DS} values. Previous work on similar devices showed that these steps can be attributed to quantum transport [3]. Indeed the energy brought by the temperature $k_B \cdot T/q$ (k_B being the Boltzmann constant and q the elementary electrical charge) and the energy brought by the drain voltage $q \cdot V_{DS}$ are much lower than the energy spacing between the discrete subbands ΔE (Fig. 1). As a consequence, quantum transport of the carriers leads to step-like variations in the transfer characteristics. However both quantum conduction and drift diffusion exist at the same time, the latter becomes dominant when the energy brought to the carriers by the lateral electric field is high enough. The valleys in the transconductance characteristics can be associated with successive energy subband fillings in the 2D density-of-states as the gate voltage V_{GS} increases. The valleys "width" in term of V_{GS} gives access to the energy spacing between subbands ΔE using the methodology detailed in [4].

B. Impact of quantum transport on the 1/f noise

In order to study the impact of the quantum transport on the low frequency noise, the drain current noise PSD Si_d has been measured as a function of the drain current at V_{DS} = 300 µV and V_{DS} = 20 mV, as the quantum

transport is dominant in the first case while the drift diffusion mechanism prevails in the second one. The noise PSDs are known to be formed by the contribution of three independant noise sources:

$$S_{i_d} = K_w + \frac{K_f}{f} + \sum_{i=1}^{N} \frac{A_i}{1+(f/f_{0,i})^2} \qquad (1)$$

where K_w represents the white noise level and K_f the $1/f$ noise level. The third term corresponds to the Lorentzians due to the generation-recombination noise. Using (1) to model the PSDs, the $1/f$ noise level evolution can be traced against the drain current for both V_{DS} bias values.

As shown on Fig. 2 $K_f(I_D)$ at V_{DS} = 20 mV is proportional to $g_m^2(I_D)$, which indicates that the $1/f$ noise mechanism corresponds to carrier number fluctuations. At V_{DS} = 300 µV, $K_f(I_D)$ also follows the g_m^2 variations. In the case of number fluctuations the ratio between K_f and g_m^2 corresponds to the flat-band voltage noise PSD Sv_{fb}. This represents the oxide trap density and therefore it should be independent of the drain voltage. However one can observe that $Sv_{fb} = 6 \cdot 10^{-9}$ V^2 for V_{DS} = 300 µV and $Sv_{fb} = 3 \cdot 10^{-11}$ V^2 for V_{DS} = 20 mV. This is not in accordance with the number fluctuations theory.

Finally the evolution of the $1/f$ noise level K_f as a function of V_{DS} has been studied in strong inversion (V_{GS} = 0.8 V). For V_{DS} higher than a few mV, e.g. where drift diffusion prevails, $K_f(I_D)$ follows I_D^2 and can be explained by the number fluctuations mechanism. For lower V_{DS} values (i.e. when quantum transport prevails) it can be observed that the unusual $1/f$ levels cannot be explained by the previous model. This suggests a change of the responsible fluctuation mechanism. In the framework of the mobility fluctuations model, the gate voltage noise Sv_g should decrease with the drain current. Taking into account that $Si_d = Sv_g \cdot g_m^2$, the unusual behavior of the $1/f$ noise level may be related to the transconductance oscillations due to the quantum transport. However, additional study is necessary to confirm this correspondence.

IV. CONCLUSION

It has been shown in this work that quantum transport prevails over the drift diffusion mechanism in silicon GAA NW FETs when V_{DS} is very low (lower than a few mV) and temperature is very low. Indeed $q \cdot V_{DS}$ and $k_B \cdot T/q$ are much lower than the energy spacing between the discrete subbands. Unexpected behavior of the low frequency noise under quantum transport regime has been evidenced, while number fluctuations can explain the $1/f$ noise when drift diffusion becomes dominant. Further results should lead to more information in order to identify the responsible $1/f$ noise mechanism under quantum transport operation.

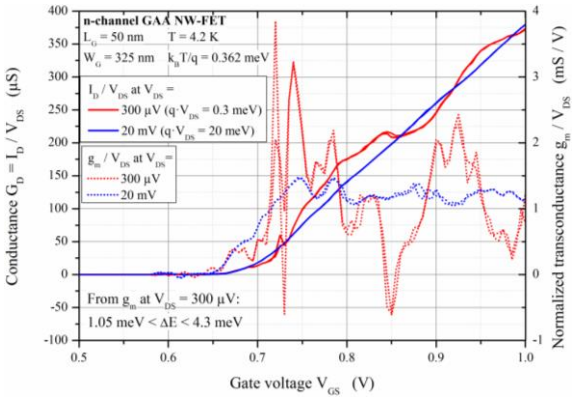

Figure 1. Typical conductance $G_D(V_{GS})$ and transconductance $g_m(V_{GS})$ characteristics at V_{DS} = 300 µV and V_{DS} = 20 mV at 4.2 K.

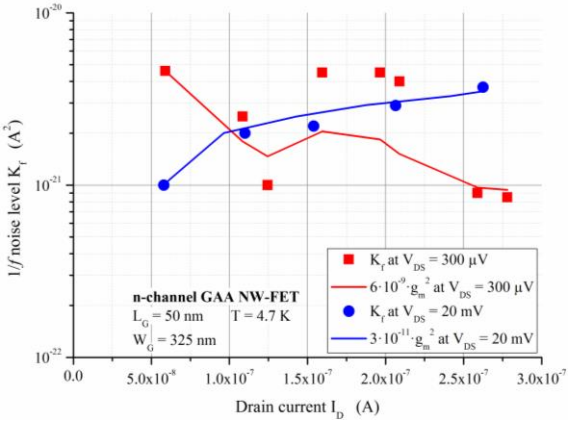

Figure 2. $1/f$ noise level K_f evolution as a function of the drain current I_{DS} at V_{DS} = 300 µV and 20 mV.

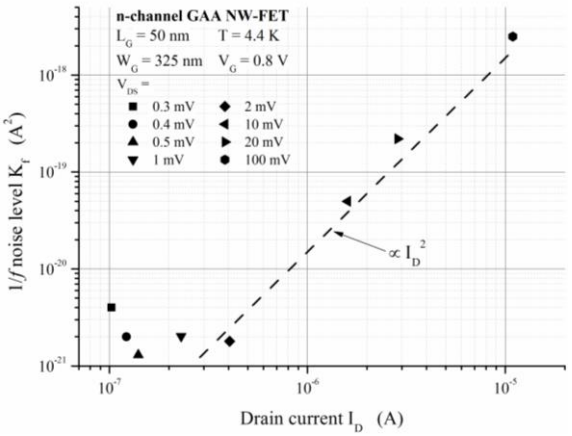

Figure 3. $1/f$ noise level K_f evolution as a function of the drain voltage V_{DS} at V_{GS} = 800 mV (i.e. in strong inversion).

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A Noise and RTN-Removal Smart Method for the Parameter Extraction of CMOS Aging Compact Models

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***Abstract*— In this work, a new method for the statistical obtention of the emission times and related ΔV_{th} of nanometer CMOS transistors' oxide defects is presented. The method identifies the V_{th} drops associated to oxide trap emissions during BTI and HCI aging recovery traces while removing RTN and background noise contributions to avoid artifacts during data analysis.**

Keywords- CMOS; BTI; HCI; parameters; extraction; method; RTN; defects; aging;

I. INTRODUCTION

With nowadays CMOS technology downscaling, BTI and HCI aging and RTN transient effects, have reemerged as important time-dependent variability (TDV) phenomena that must be taken into account in the design of digital and analog VLSI integrated circuits (ICs). During circuit operation, these variability effects, related to the trapping/detrapping in/from oxide defects, could result in circuit malfunction due to the shift of some transistors' parameters, such as the threshold voltage (V_{th}) [1]. Thus, it is critical for IC circuit designers to take into account TDV effects to implement reliability-aware circuits [2]. For this, TDV compact models that distinguish the defects contribution due to aging from that due to RTN and other noise sources are necessary. On the other hand, an accurate defects parameters extraction method requires statistical characterization of transistors under accelerated conditions [3].

Conventional BTI/HCI aging characterization techniques are based in the application of serialized measurement-stress-measurement sequences to one or a few CMOS transistors simultaneously by using probe stations. However, to get sufficient statistical data, a massive aging test, with hundreds of transistors, must be performed. Doing so serially (one device at a time) may however take several months. In our work, we use the 65-nm technology ENDURANCE IC chip to execute BTI/HCI aging tests over hundreds of CMOS transistors with a stress parallelization technique that significantly reduces the total aging test time [4]. Aging can be modeled by analyzing the emission times (τ_e) and related ΔV_{th} (η) of defects during the recovery phases after the application of overvoltage stress [5]. Figure 1(a) shows a few experimental recovery traces attained after the execution of a massive BTI test, where charge detrapping from oxide defects can be clearly seen during the recovery time as abrupt current jumps. Note also from Figure 1(b) that the simultaneous presence of RTN in the traces could mask or significantly increase the current increments related to BTI/HCI aging, so it is critical to distinguish between current levels that are linked to BTI/HCI or to RTN.

In this work, we introduce a novel defects parameter extraction method that massively identifies the emission times and η values in experimental transistor recovery traces when RTN and background noise are present. The defect parameter extraction method 'cleans' the RTN and background noise from the recovery traces and performs the extraction of the $\{\tau_e, \eta\}$ tuple of each defect discharge to model the effect of aging without noise-masking issues.

II. DESCRIPTION OF THE METHOD

The CMOS defect parameters extraction method identifies the ΔV_{th} levels in recovery traces by previously cleaning the noise and RTN (if any). It then extracts the τ_e and η of all defect discharges found. This is done in 5 steps:

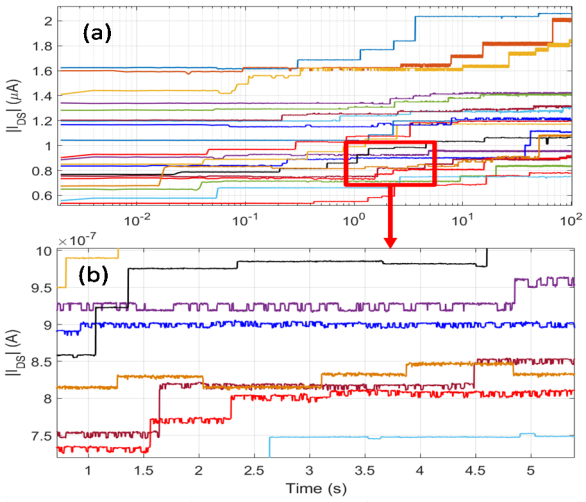

Figure 1. (a) Several recovery traces from a massive BTI test involving 400 80nm/60nm transistors, showing discrete current increment steps and, (b) a zoom-in of 5 seconds showing traces with RTN behavior mixed with BTI defect discharges.

1) For each tested device, the I_{DS} measured as a function of time during the measurement phase of the aging test is converted into the equivalent ΔV_{th} by means of the pre-stressed I_{DS}-V_{GS} curve [6].

2) The next step consists in the application of the Weighted Time Lag Method (WTLM) to the full recovery trace, in order to identify the number and value of ΔV_{th} levels present [7].

3) Once the ΔV_{th} levels are identified, the method filters out the background noise of the trace and assigns, to each sample in the ΔV_{th} trace, the closest ΔV_{th} level obtained with the WTLM. This step digitizes the ΔV_{th} recovery trace, erasing the backgroud noise and leaving only ΔV_{th} levels associated to BTI/HCI discharges and RTN phenomena. For instance, Figure 2 (a) shows two ΔV_{th} traces (blue traces), both showing high ΔV_{th} degradation due to previous stress, and also displays the ΔV_{th} trace reconstruction (red trace) with the background noise removed. During the recovery period (i.e., from 2ms to 100s), different V_{th} levels can be observed because of defect emissions mixed with RTN phenomena, as shown in the zooms in Figure 2(b) and (c).

4) In order to distiguish between RTN and BTI/HCI emissions, the method registers and stores the transitions between different ΔV_{th} levels. In the case of RTN, fast defects identification leads to multiple transitions between two ΔV_{th} levels while, for slow defects emissions, only a single transistion between two ΔV_{th} levels is counted.

5) The last step consists in obtaining τ_e and η parameters of only the aging related discharges, using the information in step 4, that can be easily evaluated from the filtered ΔVth trace, as shown in Figure 2(d). For this example, a total of 4 and 3 discharges are extracted from trace 1 and trace 2, respectively.

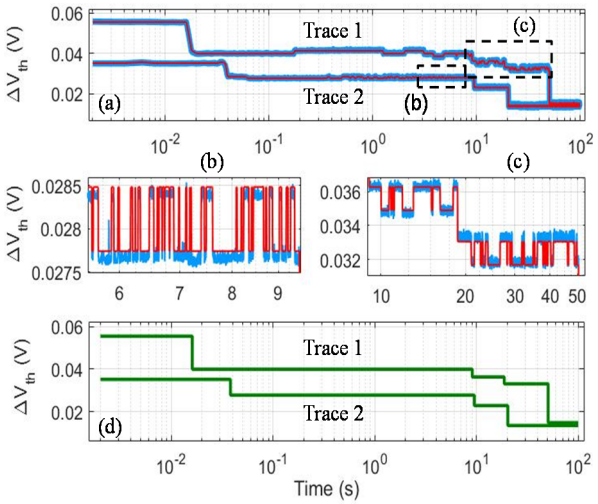

Figure 2. (a) Recovery traces from two different devices (blue) with the reconstructed trace without noise (red). (b), (c) Zoom in the signals showing RTN (blue traces) and trace reconstruction without background noise (red traces). (d) Filtered recovery traces without noise and RTN ready for defect parameter extraction.

III. Method Application

In order to evaluate the parameter extraction method, 4 BTI tests, each one involving 138 CMOS transistors with 8 different channel sizes (i.e., W and L), will be considered for defect extraction. The accelerated stress consisted in 4 stress/measurement cycles with increasing V_{GS} stress at 1.2V, 1.5V, 2V and 2.5V and V_{DS} at 0V, while measurement (i.e., recovery) phases were set at $V_{GS} \approx V_{th}$ and V_{DS} = 0.1V. The parameters extracted from the BTI tests using the proposed method have identified a total of 2,625 aging defect emissions, as shown in Figure 3(a).

The figure verifies that by increasing the stress voltage (i.e., $V_{GS} \geq 1.2$V) a large number of defects are detected because defects with smaller capture times are activated. Figure 3(b) shows the exponential distribution of η for the 8 different geometries, showing that $<\eta>$ increases as the area of the tested devices decreases. If the RTN phenomena was not removed from the recovery traces before the slow defects identification, a large number of 'false' defects (with equal ΔV_{th} value as the RTN amplitude) would have been taken into account during the $<\eta>$ calculation. Therefore, the resulting $<\eta>$ value would have been close to the ΔV_{th} of the fastest RTN, masking the actual $<\eta>$ of the defects.

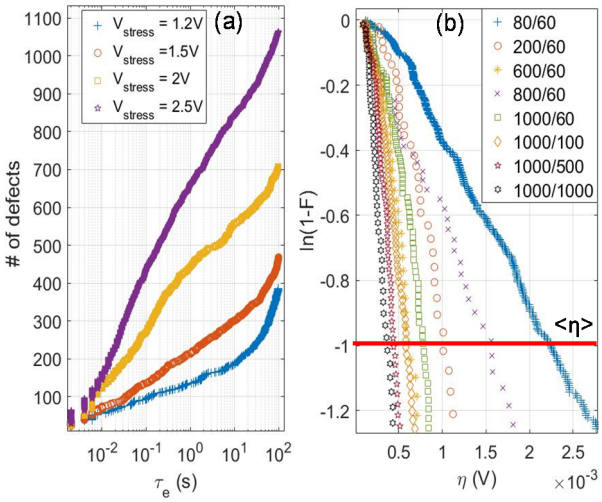

Figure 3. (a) Distribution of number of defects as a function of τ_e for each gate stress voltage. (b) Cumulative distribution function of the η values extracted from a 4 cycle BTI test with V_{GS} = 2.5V and different W/L ratios.

Acknowledgment

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Scaling FDSOI Technology down to 7 nm – a Physical Modeling Study Based on 3D Phase-Space Subband Boltzmann Transport

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***Abstract*—We present the first truly full-band approach to solving the subband Boltzmann transport (SBTE) equation in three-dimensional phase space. The solution is applied to investigate the evolution of the FDSOI MOSFET towards the 7 nm node. Our findings show that single-gate FDSOI technology can be effectively scaled down to the 14 nm node, because the on-current gains are large enough to offset the SS-degradation. Beyond 14 nm a double-gate thin-body geometry is required to maintain electrostatic control.**

Based on our previous work with nanowire FETs and FinFETs [1], we have extended the two-dimensional phase-space solution of the subband Boltzmann transport equation (SBTE) to three-dimensional phase space, by adding the lateral **k**-space component, as shown in Fig. 2.

In contrast to previous works using Fourier expansion [2, 3], our approach employs a rectangular **k**-grid, with axes aligned to the real-space-grid, which is **capable of reproducing the ballistic and dissipative distribution function accurately**. It does not require the subband structure to be monotonous, as is the case with the Fourier expansion, but works with arbitrary numeric $E(\mathbf{k})$-relations, making it the **first truly full-band SBTE implementation**, available as part of GTS Nano Device Simulator (NDS) [4].

The aggressive scaling trends observed in last FinFET technology nodes [5, 6], is replicated to see if fully-depleted silicon-on-insulator (FDSOI) technology can keep up with such scaling. NMOS and PMOS devices were simulated, ranging from the **28 nm to the 7 nm** node.

Beside the physical gate length scaling, it was assumed that at the 10 nm node the interfacial oxide could be thinned down from 1.2 nm to 0.6 nm, and that the **SOI channel** could be **thinned down to 5.5 nm** for the 14 nm node **and further down to 4.5 nm** for the 7 nm node. A source/drain doping of $2 \times 10^{20}\,\mathrm{cm}^{-3}$ was assumed for all devices and the surface of the SOI wafer was assumed as (001), while the channel orientation [110] was chosen.

Using the SBTE methodology, low and high-V_{DS} transfer characteristics were obtained for all nodes and device polarities, and are shown in Figs. 3 and 4. The **threshold voltages have been adjusted** for every device to have the **off-current** $I_{\mathrm{off}} = 1 \times 10^{-6}\,\mathrm{mA}/\mu\mathrm{m}$.

While **scaling** down the gate length seems **beneficial down to the 14 nm** node, the **benefits diminish beyond 14 nm**. For PMOS, the trend even reverses at some point, and the PMOS performs worse at 7 nm than at 14 nm. Moreover, it becomes clear that the gain in on-current is not enough to compensate for the losses from the degrading sub-threshold slope (SS) and drain-induced barrier lowering (DIBL). The device characteristics are summarized in Fig. 5.

Finally, the 7 nm single-gate (SG) FDSOI PMOS is compared to a comparable 7 nm double-gate (DG) or nano-sheet [7] (NS) PMOS. with a relaxed Si film thickness of 5.5 nm. Due to its additional gate, the **DG PMOS delivers an almost ideal SS of 66.6 mV/dec**, drives a current almost four times higher the the SG and has a **ballistic ratio** of 0.43 (less than 0.35 in SG).

Using a **novel, unique, and effective approach** to solving the **subband BTE** in thin-body transistors, simulations were performed to show that **scaling single-gate FDSOI MOSFETs is unlikely to be feasible beyond the 14 nm node**. However, a **double-gate thin-body** geometry provides sufficient electrostatic control for scaling **down to 7 nm**.

Acknowledgment

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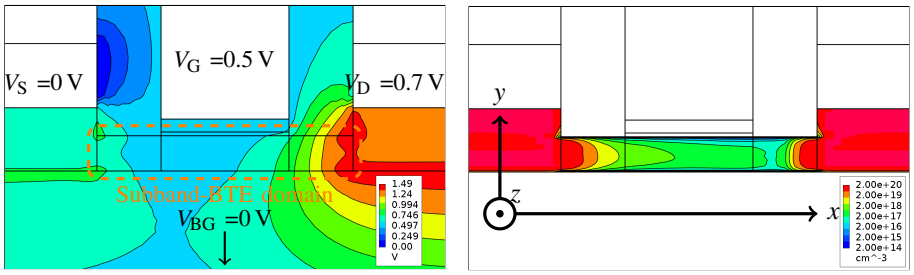

Fig. 1. **Potential** (left) and **electron concentration** (right) the in the 14 nm NMOS device biased at $V_{DS} = 0.7\,V$, $V_G = 0.5\,V$ with the back-gate voltage being $V_{BG} = 0\,V$; the dashed box in the left image indicates the domain where the **k·p**-Schrödinger equation and subband Boltzmann transport equation (SBTE) are solved, whereas the remainder of the device is treated using drift-diffusion and density-gradient.

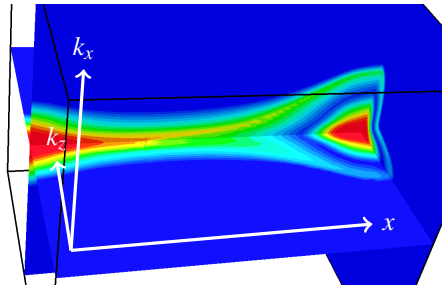

Fig. 2. **Electron distribution function** represented in **three-dimensional phase space** corresponding to the device and bias conditions shown in Fig. 1; the **k**-grid axes are aligned to the real-space axes in Fig. 1; k_x points in the direction of carrier transport along the channel, x, while k_z points perpendicular to the device plane.

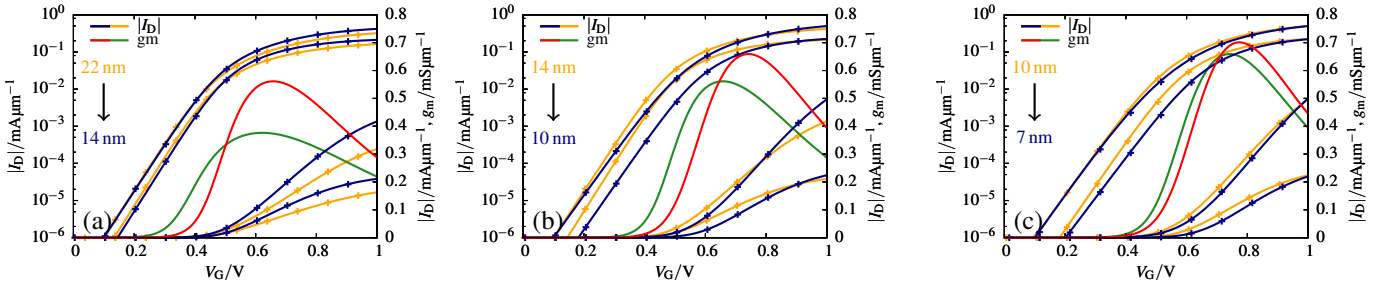

Fig. 3. **NMOS gate length scaling**; the four images (a)-(d) show the comparisons between each two of the consecutive technology nodes. The transfer characteristics were taken at $V_{DS} = -0.05$ and $-0.7\,V$. The off-current is normalized to 1×10^{-6} mA/μm to clearly show the differences in on-current.

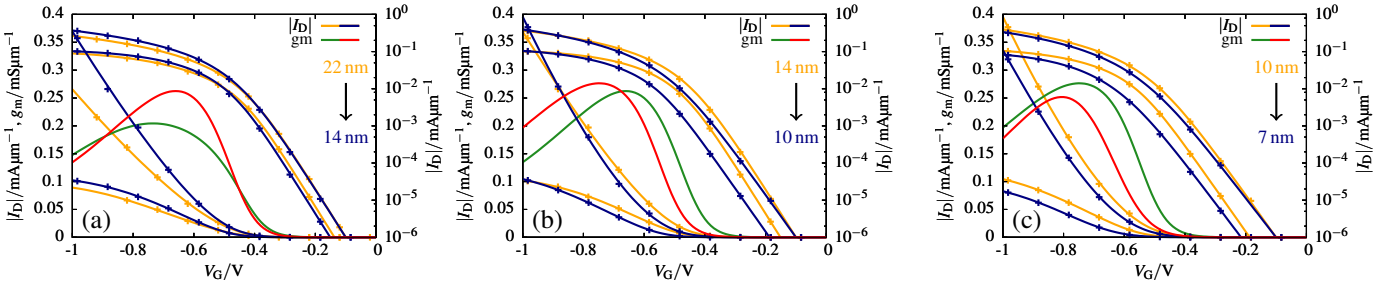

Fig. 4. **PMOS gate length scaling** - same as Fig. 3; the transfer characteristics were taken at $V_{DS} = -0.05$ and $-0.7\,V$. 10 nm and 14 nm show the same on-current performance, while 7 nm performs worse than 10 nm.

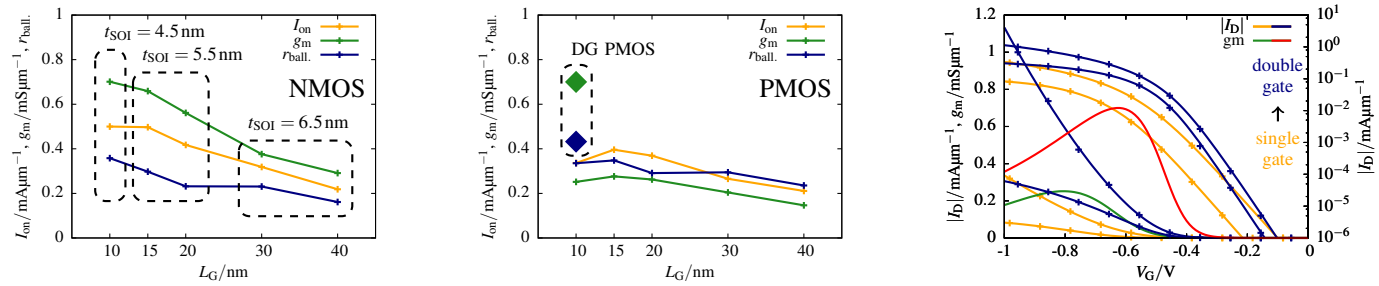

Fig. 5. I_{on}, g_m, **and ballistic ratio** as function of the physical gate length for NMOS (left) and PMOS (right); both ballistic ratios show no increase between 30 nm (22 nm node) and 20 nm (14 nm node), due to the narrowing of the SOI from 6.5 nm to 5.5 nm which specifically increases surface roughness scattering.

Fig. 6. **7 nm single-gate vs. double-gate PMOS**; the improved electrostatic control yields an almost perfect 67 mV/dec SS, outperforming the single-gate PMOS by a factor of four in terms of I_{on}.

Design-oriented Modeling of 28 nm FDSOI CMOS Technology down to 4.2 K for Quantum Computing

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***Abstract*—In this paper the DC characteristics of a commercial 28 nm FDSOI CMOS technology is accurately modeled from room temperature down to 4.2 K. Relying on the design-oriented simplified EKV model, the influence of cryogenic temperatures on the analog performance is assessed. This leads to a main step towards the development of a cryo-compact model for the design and large-scale integration of cryo-CMOS qubit-control and read-out circuits implemented in a 28 nm FDSOI technology.**

***Keywords*—28 nm FDSOI CMOS, cryo-CMOS, cryoelectronics, cryogenic, quantum computing, 4.2 K**

I. Introduction

Quantum computing can reshape many fields by providing the computing power to solve exponentially-growing problems. However, nowadays, the scale-up of qubit numbers is the main challenge [1]. In this context, silicon-on-insulator technology provides an excellent platform for scalable quantum computing systems in which both the qubits and control circuitry operate at cryogenic temperatures [2]. CMOS-compatible spin qubits developed in a FDSOI nanowire technology [3], [4] can be co-integrated with the required analog/RF circuits (including multiplexers, low-noise amplifiers, and oscillators) to improve qubit-control and read-out [5]. To this purpose, a 28 nm FDSOI CMOS process was previously characterized in [6]. In this work, we model the DC electrical behavior of this technology down to 4.2 K, aiming at the extension of industry-standard compact models [7] to cryogenic temperatures for the design of large-scale qubit control systems in FDSOI.

II. Characterization and Modeling

1) Measurements and Characterization: The transfer characteristics of 28 nm FDSOI CMOS devices with various aspect ratios were measured in [6], for the linear (V_{DS}= 50 mV) and saturation regimes (V_{DS}= 0.9 V) at different temperatures (Figs. 1a-c). The back-gate voltage (V_{back}) is swept from -0.9 V to 0.9 V. The cryogenic output characteristics (down to 1.4 K) were obtained for different gate voltages at V_{back}= 0 V. The subthreshold swing (SS), slope factor (n), threshold voltage (V_{th}), transconductance (G_m), normalized low-field mobility (μ_0), and on-state current (I_{on}) have been extracted.

2) Modeling and Discussion: As illustrated in Fig. 2a, for temperatures below $\approx$ 160 K, the SS shows an increasing offset from the thermal limit, $U_T \ln 10$, where $U_T = kT/q$ is the thermal voltage. Similarly to [8], the temperature-dependence of $n \propto 1/U_T$ (plotted in Fig.2b) can be explained by including the Fermi-Dirac occupation of interface traps. This leads to $SS = n(T)U_T \ln 10 = n_0 U_T \ln 10 + \Delta SS$, where n_0 is the slope factor without interface traps and a ΔSS-offset is given by $(qD_{it}/C_{ox}) \ln 10\,[g_t/(1+g_t)]$ with D_{it} the density-of-interface-traps and g_t the trap degeneracy factor. Note that in this model, D_{it} does not become multiplied with U_T, resulting in reasonable extracted values for D_{it} at 4.2 K ($\approx$ 10^{11}-$10^{12}\,\mathrm{cm}^{-2}$) lower than [9], [10]. The ΔSS-offset increases below $\approx$ 160 K since the Fermi-level moves closer to the band edge to create inversion, where D_{it} is higher. The extracted normalized low-field mobility is plotted versus temperature in Fig. 2c. The simplified EKV model [11] accurately predicts the transfer characteristics down to 4.2 K for long and short devices (Fig.3). The V_{T0}-model-parameter captures the effect of the back-gate at 4.2 K (Fig. 4a). In Fig.4b it is verified that the G_m/I_D-design-methodology remains valid for a 28 nm FDSOI technology down to 4.2 K. As illustrated in Fig.4b, the output conductance, G_{ds}, remains largely independent of temperature, and no kink effect is observed below a supply voltage of 1 V.

III. Conclusion

A 28 nm FDSOI technology is investigated down to 4.2 K using the simplified EKV model, showing promising results for cryogenic analog design, although interface trapping limits the achievable subthreshold swing at 4.2 K.

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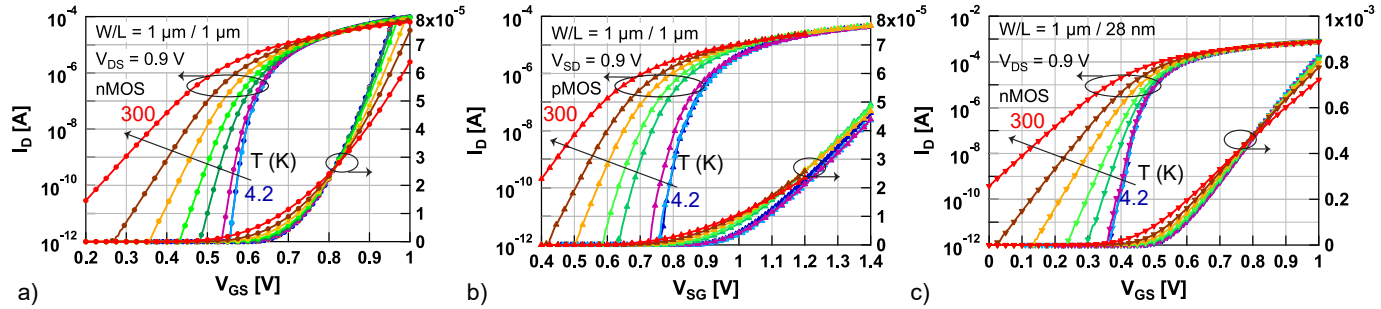

Fig. 1. Transfer characteristics measured in saturation ($|V_{DS}|$ = 0.9 V) on a 28 nm FDSOI CMOS process at 300, 210, 160, 110, 77. 36, 10, and 4.2 K for a) nMOS $W/L = 1$ µm / 1 µm, b) pMOS $W/L = 1$ µm / 1 µm, and c) nMOS $W/L = 1$ µm / 28 nm. The EOT for nMOS is 1.55 nm, and for pMOS 1.7 nm. The gate-source voltage is increased with a step size of $|V_{GS}|$ =5 mV. The back-gate voltage is 0 V. Colors indicate the temperature, and markers the device.

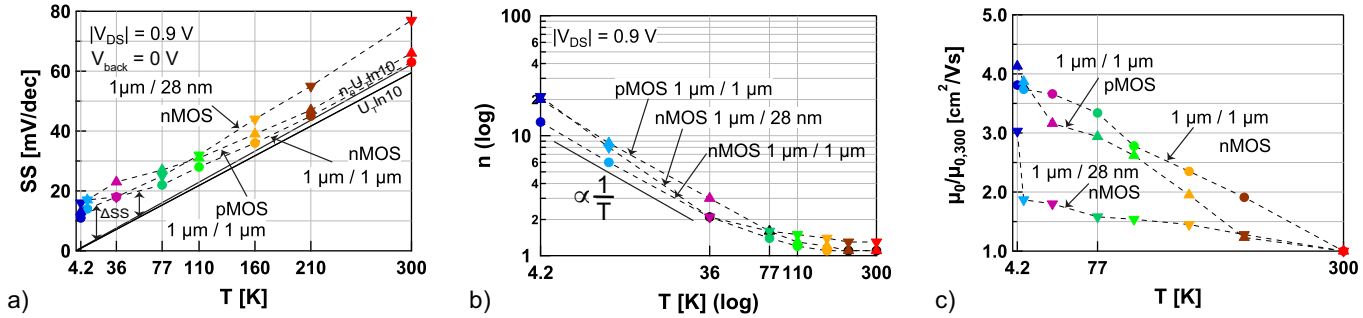

Fig. 2. Parameter extraction at 300, 210, 160, 110, 77. 36, 10, and 4.2 K, a) Subthreshold swing, modeled for long channel devices by $SS = n_0 U_T \ln 10 + \Delta SS$, with $\Delta SS \propto D_{it}$ [8], b) Slope factor in log-log scale highlighting its hyperbolic temperature dependency, c) Normalized low-field mobility (Y-function method).

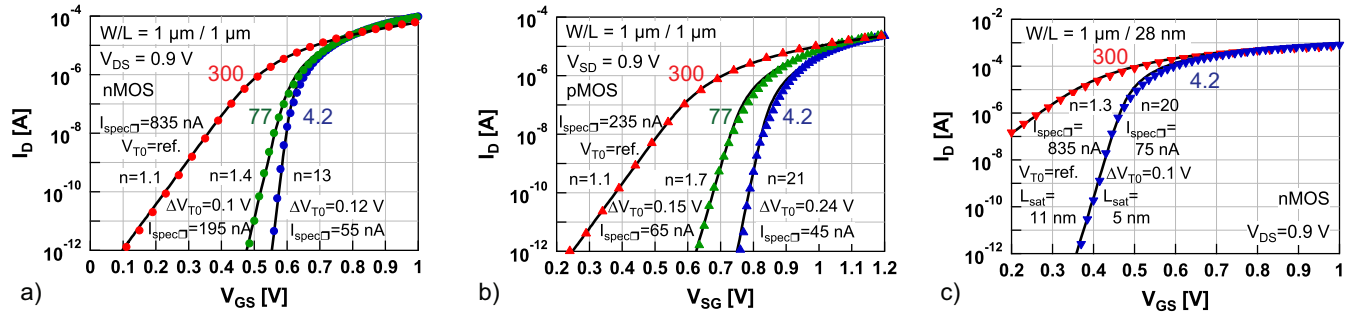

Fig. 3. Simplified EKV (solid lines) for a) nMOS $W/L = 1$ µm / 1 µm, b) pMOS $W/L = 1$ µm / 1 µm, and c) nMOS $W/L = 1$ µm / 28 nm at 300, 77, and 4.2 K (markers) for V_{back}=0 V. The model parameters, n, V_{T0} (threshold voltage), $I_{spec\square}$ (specific-current-per-square), and L_{sat} (saturation length), are shown.

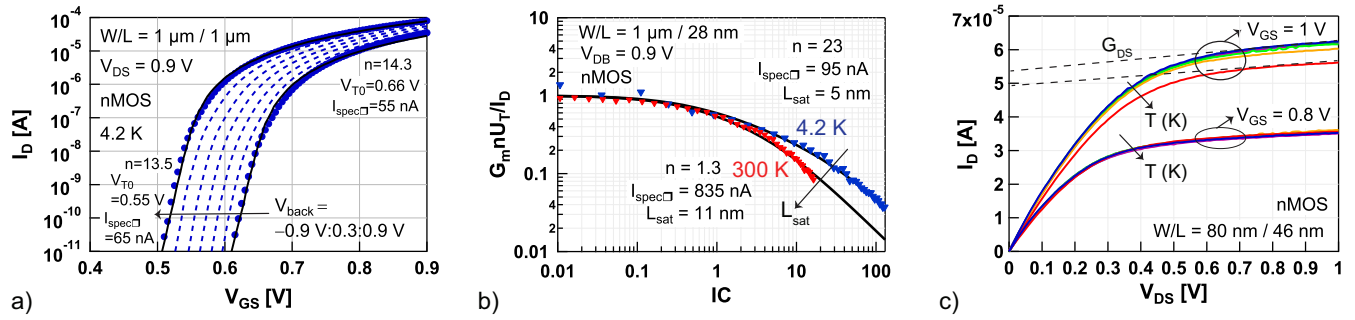

Fig. 4. a) Back-gate sensitivity at 4.2 K modeled with simplified EKV. The model is shown for V_{back}=−0.9 V and 0.9 V with solid lines. Markers and dashed lines indicate measurements at 4.2 K, b) Normalized transconductance efficiency versus the inversion coefficient, IC, at 300 and 4.2 K, c) Output characteristics of nMOS $W/L = 80$ nm / 46 nm at V_{GS} = 0.8 V and 1 V for all temperatures. The output conductance, G_{ds}, is extracted at V_{DS} =0.9 V.

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Adaption of Triple Gate Junctionless MOSFETs Analytical Compact Model for Accurate Circuit Design in a Wide Temperature Range

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***Abstract*—This paper presents the necessary adaptions on a proposed compact analytical model of triple gate junctionless nanowire transistors for accurate description of device electrical characteristics in a wide temperature range. The model validation is performed by comparison against experimental results showing very good agreement for the drain current and its derivatives.**

***Keywords*—Junctioless transistor; compact model; temperature.**

I. INTRODUCTION

Triple gate Junctionless Nanowire Transistors (JNTs) are promising devices for new generations of integrated circuits due to their excellent electrostatic control of the channel, reducing the short-channel effects (SCEs). The Subthreshold slope (*S*) is close to the ideal case, DIBL is lower than in inversion FinFETs and the threshold voltage roll-off appears at shorter channel lengths [1]. In addition, these devices present simpler fabrication process reaching sub-10 nm channel lengths [2] and demonstrated very good characteristics for analog applications [3].

JNTs are characterized by having two types of operation regimes: partial depletion and accumulation. The device is in off state when the silicon film is fully depleted. This state is highly dependent on the device geometry and doping concentration. At gate voltages (V_G) lower than flatband voltage (V_{FB}) but high enough to create a neutral path in the body region, the transistor works in partial depletion regime, conducting predominantly by the body center. On the other hand, when the gate voltage is biased at V_{FB}, the device body becomes neutral. For gate voltages higher than V_{FB}, an accumulation layer is formed at the silicon film interface and an additional current component starts to flow.

As integrated circuits work at temperatures several tenths of degrees higher than room temperatures, the JNT models must consider the temperature dependence on the devices electrical characteristics. Recently, a new compact analytical model for triple gate structures, from double-gate to nanowires, was proposed [4]. This model is charge-based, continuous in all regimes of operation and accounts for SCEs. In the present work, we indicate the model parameters depending on temperature, including the variation of carrier concentration due to the high doping concentration. The model is validated with the experimental measurements at temperatures in the range from 20 ºC up to 170 ºC.

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II. TRIPLE GATE CORE MODEL DESCRIPTION

Figure 1 presents the cross section view of a triple gate JNT, where t_{ox} and t_{oxb} are the gate oxide and buried oxide thicknesses, respectively, W_{Fin} is the fin thickness, H_{Fin} is the fin height, L is the channel length and L_{ext} is the length of the device extensions. Because of symmetry one half of the device is modeled and its effective width is $W_{eff}=H_{Fin}+W_{Fin}/2$.

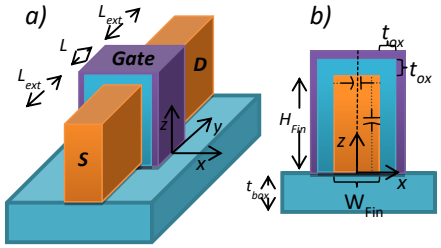

Fig. 1. Tridimensional (a) and x-z plane (b) cross section view of juntionless nanowire transistor.

The gate oxide capacitance per unit of length is given as $C_{oxL} = C_{ox}W_{eff} + 2C_f$ where $C_f = 2\varepsilon_S/\pi \cdot ln(2)$ accounts for the fringing capacitances. The silicon film capacitance per unit length is given as $C_{SL} = (\varepsilon_S/W_{Fin})H_{Fin} + (\varepsilon_S/H_{Fin})W_{Fin}$. The Gauss relation between the surface potential, φ_{SL}, and the applied gate and drain voltages, V_G and V_D, is given by:

$$V_G - V_{FB} = \varphi_{SL} + sign(\alpha_L)\,\varphi_t\,\beta_L\sqrt{e^{\frac{\varphi_{SL}-V_D}{\varphi_t}} - \xi_L\cdot\alpha_L - 1} \quad (1)$$

where α_L is the difference of potential between surface and the center α_{btL} is difference of potentials at deep subthreshold and φ_t is the thermal potential, $\beta_L = \sqrt{\frac{2C_{SL}\cdot q_{bL}}{C_{oxL}}}$, $\xi_L = \left(1 - \frac{1}{\alpha_{btL}}\right)$ and $q_{bL} = (qN_DW_{FIN}/C_{oxL}\varphi_t)H_{fin}$ is the normalized fixed charge. The analytical solution for the surface potential φ_{SL} is obtained as described in [4]. Both depletion and accumulation charges are expressed as a function of a single variable as $q_{depL} = \beta_L\sqrt{e^{\xi_L\cdot\alpha_L} - \xi_L\cdot\alpha_L - 1} - q_{bL}/2$ and $q_{accL} = -\beta_L\sqrt{e^{\frac{\varphi_{SL}-V}{\varphi_t}} - \frac{\varphi_{SL}-V}{\varphi_t} - 1} - q_{bL}/2$.

To obtain a continuous semiconductor charge, q_{nL}, from depletion to accumulation, a smoothing function is required [5]. The threshold voltage, V_{TL}, is obtained following the method described in [4]. At the device body region, where the electric field is low, the bulk current in depletion regime exhibits a constant mobility value μ_0. However, in accumulation regime, the current reduces the mobility due to scattering at the interface. The surface mobility can be calculated as in [5].

The series resistance, R, defined as the sum of drain and source resistances, are not negligible due to the extension length L_{ext} and its doping concentration. R is included in the model by using the well-known linearized MOSFET method when the transistor is turned on [3]. The expression for the correction current factor including R is:

$$KK_L = \frac{1}{\left(1-\frac{\Delta L}{L}\right)} \cdot \frac{K_L\,\varphi_t}{1+K_L\,R\left(V_G-V_T-nV_{Deff}\right)\frac{1}{2}\left[1+\tanh\left(2\left(V_G-V_T-nV_{Deff}\right)\right)\right]} \quad (2)$$

where $K_L = 2(C_{ox}W_{eff})\mu_{eff}/L = 2C_{oxL}\cdot\mu_{eff}/L$ is the current factor and n is an adjusting parameter. Due to the symmetry of the device on the x-axis, the drain current is given by:

$$I_D = KK_L \int_{V_S}^{V_D} q_{nL}\, dV \quad (3)$$

The solutions of charge expressions integrals on depletion and accumulation regimes result in the compact analytical model for I_D. A more detailed description of the model and the inclusion of short-channel effects can be found in [4].

III. Temperature-Dependent Parameters and Adjustment

To make the core model [4] valid for temperatures higher than 300 K, the required adjustments are described in this section. The thermal potential is $\varphi_t = kT/q$, where T is the absolute temperature, k is the Boltzmann constant and q the electron charge.

The silicon bandgap E_G as function of T and N_D is equal to:

$$E_G(T,N_D) = \left[1.08 + 4.73x10^{-4}\left(\frac{300^2}{300+363} - \frac{T^2}{T+363}\right)\right] - DE_G(N_D) \quad (4)$$

where the bandgap narrowing due to doping concentration is given as:

$$DE_G(N_D) = \left[9x10^{-3}\ln\left(\frac{N_D}{10^{17}}\right) + \sqrt{\ln\left(\frac{N_D}{10^{17}}\right)^2 + 0.5}\right] \quad (5)$$

The intrinsic carrier concentration as a function of T is:

$$n_i(T,N_D) = \sqrt{N_C N_V}\, e^{\frac{E_G(T,N_D)}{2\varphi_t}} \quad (6)$$

where N_C and N_V are the densities of states at the conduction and valence bands, respectively, described as $N_C = 2.8.10^{19}(T/300)^{1.5}$ and $N_V = 1.04.10^{19}(T/300)^{1.5}$. Equations (4) to (6) are used to correct the Fermi potential in the model equations. For the silicon electron affinity, the temperature increase dependence is described as:

$$\chi_{ef}(T,N_D) = 4.17 - \frac{1}{2}\left[E_G(T,N_D) - E_G(300,N_D)\right] + DE_G(N_D) \quad (7)$$

As described in [6], although JNTs use highly doped silicon layers close to the Mott transition, not all the dopant elements are ionized even at room temperature. To account for the partial carrier ionization and temperature influences, the pseudo-Boltzmann approximation [7] has been used and the effective carrier concentration $N_{D,eff}$ is analytically calculated:

$$N_{D,eff} = N_D\left\{\xi + \frac{1}{2}\left[(1-\xi+c) - \sqrt{(1-\xi+c)^2 + 4\xi c}\right]\right\} \quad (8)$$

where a=0.7888, b=0.857, c=0.0033, $\xi = ae^{\gamma(b-1)}$ and $\gamma = (E_F - E_G(T,N_D) + E_i)/\varphi_t$, where E_F and E_i are the Fermi and intrinsic levels, respectively. Additionally to the corrections in the device electrostatics, the temperature influences on carrier velocity saturation (v_{sat}) and low field mobility (μ_{0T}) are described by $v_{sat} = 2.4x10^7/(1+0.8e^{T/600})$ and $\mu_{0T} = \mu_0/(T/300)^{\alpha}$, respectively, where α is a model parameter, assuming that the main mobility degradation mechanism is phonon scattering.

IV. Results and Discusion

The measured n-type JNTs were fabricated in CEA-Leti on a silicon-on insulator wafer with a 145 nm thick buried oxide [8]. The gate stack is composed of HfSiON/TiN/poly silicon, presenting an effective oxide thickness (EOT) of about 1.7 nm. The fin height is 10 nm, the fin width is 20 nm, the channel length is 100 nm and the doping concentration is 5×10^{18} cm^{-3}. Figures 2 and 3 present the comparison between measured and modeled results of drain current, transconductance and output conductance for different biasing conditions and temperatures.

The results of Figs. 2 and 3 show very good agreement, showing that the proposed adjustment on the analytical model is adequately describing the temperature increase influences in the output characteristics of JNTs. The model allows a precise determination of the zero-temperature coefficient. Both threshold voltage reduction and subthreshold slope increase with temperature are well described by the model.

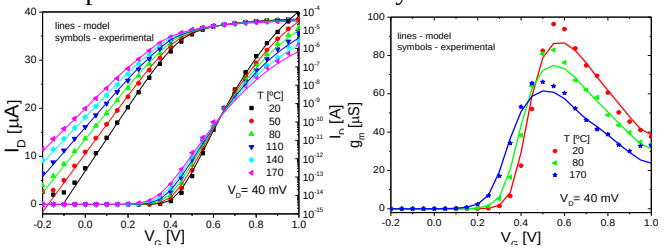

Fig. 2 – Comparison between measured (symbols) and modeled (lines) results of I_D and g_m as a function of V_G with variable temperature.

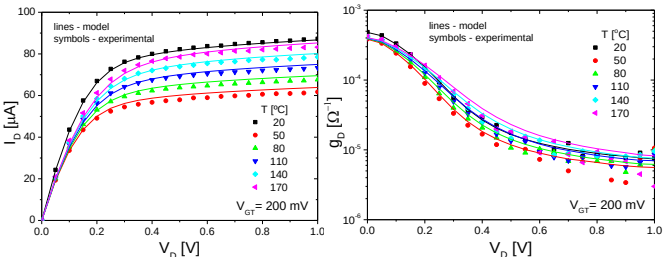

Fig. 3 – Comparison between measured (symbols) and modeled (lines) results of I_D and g_D as a function of V_D with variable temperature.

V. Conclusion

The required adaptions on the compact analytical model of junctionless nanowire transistors for describing the temperature variation influence on the electrical characteristics have been presented and validated. The drain current and its derivatives are accurately described by the analytical model.

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2D and 3D TCAD Simulation of III-V Channel FETs at the End of Scaling

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I. Introduction: The high electron mobility and injection velocity of III-V-compounds-based FETs make them promising candidates to replace n-type strained Si MOSFETs at future technology nodes with gate lengths shorter than 20 nm [1]. The aggressive scaling causes quantum effects which have a critical influence on the device performance. For instance, geometrical quantum confinement in the body with thickness (t_{body}) below 12 nm leads to a shift in the threshold voltage [2]. Moreover, at gate lengths shorter than 20 nm, the potential barrier between source and drain becomes thin enough, so that source-to-drain tunneling (STDT) deteriorates or even determines the sub-threshold swing (*SS*) [3]. Quantum transport (QT) simulators start to find their way into industrial environments, however, they are computational expensive for large and complex 2D and 3D devices [4]. In this paper, we systematically show how quantum drift-diffusion (QDD) tools [5] in combination with a TCAD-friendly ballistic mobility model [10] can be used to simulate the described quantum effects. A reasonable agreement with QT simulation results is achieved for *SS*, but I_{ON} is still too high in the linear regime.

II. Simulation Approaches: First, we performed 2D simulations of the ultra-thin body (UTB) double-gate (DG) transistor shown in Fig. 1 (a) using the quantum transport code QTx [4]. The same structure was simulated for different gate lengths (L_G) ranging from 10 nm to 25 nm. Next, 3D simulations using QTx were done for gate-all-around (GAA) nanowire (NW) FETs. Their design parameters are the same as for the DG UTB FETs. The dimensions are given in Tab. I. The I_DV_{GS}-characteristics simulated with QTx were used as reference to calibrate the QDD simulation setup. Effective masses (m_e) and non-parabolicity parameters were calculated from a full-band version of the QT code. To simulate the geometrical confinement perpendicular to the transport direction in the 2D and 3D structures we used two models: (i) The Density Gradient (DG) model [2], which adds a quantum potential in the computation of the carrier density (n). This model depends on n, m_e and a fitting parameter γ. The latter was found using the the 1D electron density (n_e) profile along a vertical cut in the middle of the DG UTB from a Schrödinger-Poisson solver [4]. For the GAA NWs, $\gamma$was calibrated using a 1D n_e vertical profile in the middle yz-plane of the device, and the QTx density integrated perpendicular to the transport direction was taken as reference. (ii) The Modified Local Density Approximation (MLDA) [9].

TABLE I. Dimensions of the GAA NWs according to future technology nodes as described in [6].

Node	L_G [nm]	t_{ox} [nm]	t_{body} [nm]	m_e
A	15	3.75	7	0.0642
B	10.4	3.25	5.5	0.0674

To include STDT, the Nonlocal Tunneling (NLT) model was used [5] in combination with the MLDA and the anisotropic DG model, respectively. The tunneling mass (m_c) corresponds to m_e. In a first instance, to mimic the ballistic QTx case, a constant and artificially high channel mobility (μ_d) of 2.26x10^4 cm^2/Vs was used in the simulations of the DG UTB FETs. In the simulations of the GAA NWs, to assess the behavior of a parameter-free ballistic mobility model [11] in a 3D FET and to improve the agreement with the on-current in the QTx I_DV_{GS}-characteristics, we applied μ_{ball} for the channel mobility, included STDT, but disregarded vertical quantization. The latter has the main effect of shifting the threshold voltage and is usually covered by the work function (WF) fit in TCAD.

III. Results: The small difference in the threshold voltage between QTx and QDD (≈ 30 mV) in Figs. 2-4 originates from the definition of the energy zero in the different simulators. In the case of Fig. 5, the difference is larger since t_{body} in this device is thinner than 7 nm and geometrical confinement is much stronger than in the other structures. Fig. 2 shows the fitted I_DV_{GS}-characteristics for the DG UTB FETs for three L_G computed with the combination of the anisotropic DG model and NLT. The *SS* of the transistor with the shortest L_G (where the effect of STDT is strongest) is best reproduced by the anisotropic DG model. Fig. 3 shows the I_DV_{GS}-characteristics for the DG UTB FETs using MLDA+NLT, and Fig. 4 (Fig. 5) presents the transfer curves for GAA NW A (B), where DG+NLT, MLDA +NLT were used, respectively.

TABLE II. Extracted on-current I_{ON} at V_{GS} = 0.5 V.

Node	I_{ON} – Qtx	I_{ON} - μ_{ball} + NLT	I_{ON} - DG+NLT
A	1x10^{-4}	1.56x10^{-3}	1.7x10^{-2}
B	3.7x10^{-4}	1.8x10^{-3}	1.8x10^{-2}

IV. Conclusion: The NLT used in combination with the anisotropic DG model can fairly reproduce the reference *SS* of the DG UTB FETs in the case of strong STDT. In GAA NWs the excellent gate electrostatic control reduces *SS* significantly compared to the DG UTB FETs with the same L_G [6]. Thus, the MLDA+NLT and DG+NLT approaches slightly exacerbated the *SS*, even in the case of the shortest GAA NW (B). The usage of a ballistic mobility μ_{ball} reduces I_{ON} by one order of magnitude as compared to the simulation with μ_d, however, it is still too large when compared with the QT value. This can be due to the fact that the true 1D DOS can hardly be mimicked in S-Device (convergence problems). Another possibility is the used model for μ_{ball} itself, which overestimates the current in the linear regime [11].

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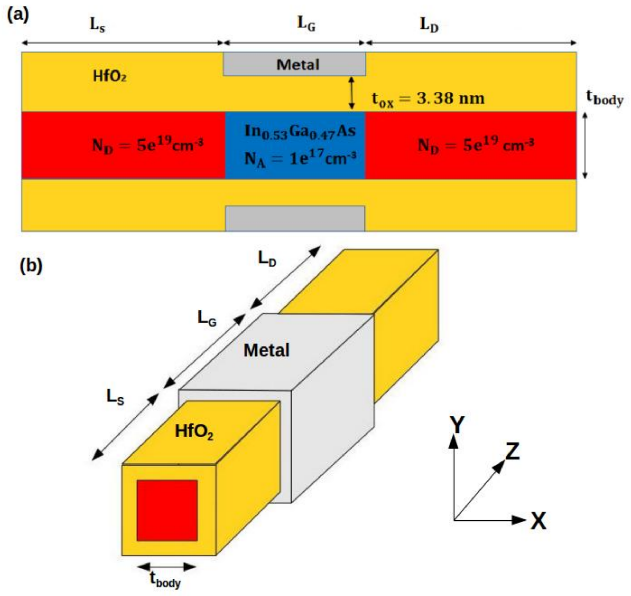

Fig. 1: Schematic of (a) In0.53Ga0.47As double-gate ultra-thin-body and (b) In0.53Ga0.47As gate-all-around nanowire transistor.

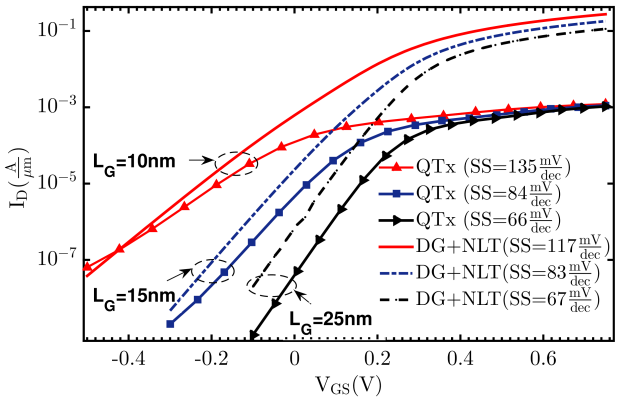

Fig. 2: I_DV_{GS}-characteristics obtained from the combination DG+NLT for a 7 nm DG UTB FET with different gate lengths. V_{DS} = 0.05 V, m_c = 0.0516 m_0 and μ_d= 2.26x104 cm2/Vs.

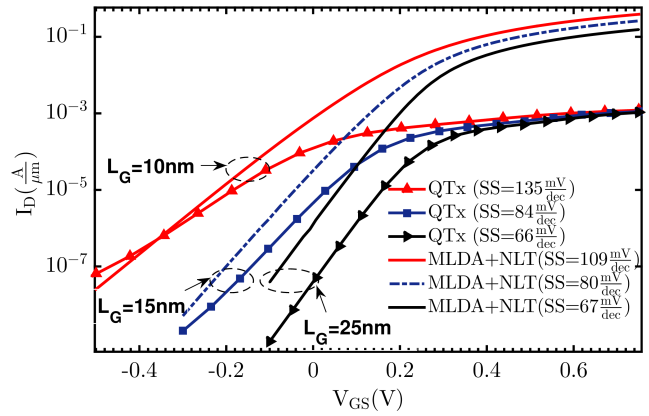

Fig. 3: I_DV_{GS}-characteristics obtained from the combination MLDA+NLT for a 7 nm DG UTB FET with different gate lengths. V_{DS} = 0.05 V, m_c = 0.0516 m_0 and μ_d= 2.26x104 cm2/Vs.

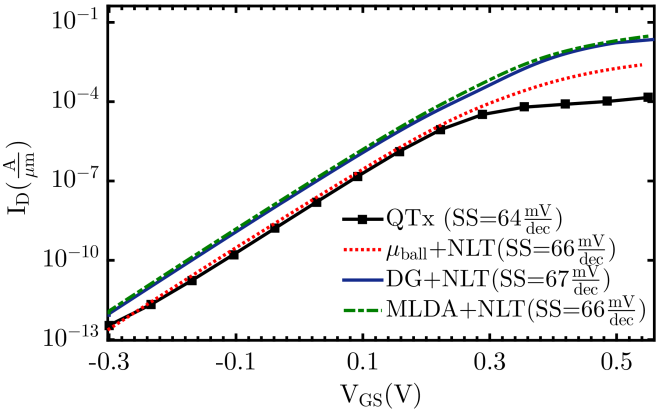

Fig. 4: I_DV_{GS}-characteristics obtained from the combination DG+NLT, MLDA+NLT, and ballistic mobility μ_b for a GAA NW FET with t_{body} = 7 nm. V_{DS} = 0.05 V, m_c = 0.0642 m_0.

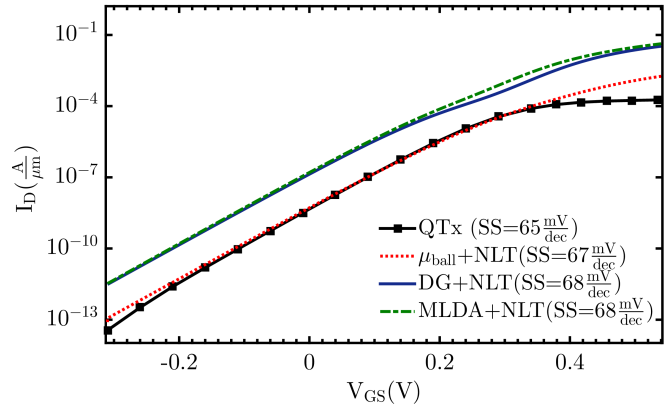

Fig. 5: I_DV_{GS}-characteristics obtained from the combination DG+NLT, MLDA+NLT, and ballistic mobility μ_b for a GAA NW FET with t_{body} = 5.5 nm. V_{DS} = 0.05 V, m_c = 0.0674 m_0.

Investigation on Temperature Effects of Electrical Characteristics in GaAs DMG FinFET

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***Abstract*—Here, we have reported a dual material gate (DMG) GaAs FinFET and compared its performance parameters with similar sized single material gate (SMG) GaAs FinFET. A significant improvement in electrical parameters is observed in DMG GaAs FinFET. We also investigated the impact of temperature on various electrical parameters like drain current, transconductance, and gate capacitance in the proposed DMG GaAs FinFET through TCAD simulator. At lower temperature better performance is obtained than a higher temperature.**

Keywords—DMG; FinFET; GaAs; SOI; Temperature.

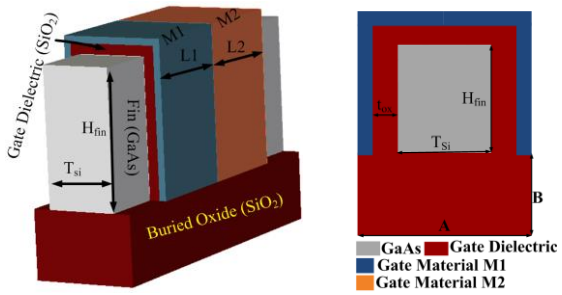
I. INTRODUCTION

It is well established that continuous scaling of the MOSFET transistors has degraded its control over the channel, which leads to increased short channel effects (SCEs) and high leakage current [1]. In this regard, FinFET provides themselves as strong candidate, due to better scalability and excellent immunity against SCEs [2]. To improve the performance of FinFET, researchers have introduced various techniques like channel materials beyond silicon, modification of device architecture, gate work function engineering and so on. Among gate engineering, dual material gate (DMG) and triple material gate (TMG) FinFETs provide better short channel and current characteristics than conventional FinFET [3-4]. The electrical property of any device is dependent on temperature and such properties changes with the variation in temperature [5]. The effect of temperature on I_{on}/I_{off} ratio for different channel material with the variation in temperature reported that InAs channel shows best temperature stability [6]. An investigation of electrical parameters and digital inverter performance due to variation in temperature is analyzed for GaAs SOI FinFET and average delay of inverter degrade with increase in temperature [7]. In this paper, an analysis on the effect of temperature on various electrical parameters in the dual material gate (DMG) GaAs FinFET is carried out. A comparative study of important electrical characteristics between DMG and SMG GaAs FinFETs is presented.

II. DEVICE STRUCTURE AND SIMULATION SETUP

The 3D and 2D schematics of the proposed DMG GaAs FinFET are shown in Figs. 1(a) and (b), respectively. In this structure, material (M1) with high work function (ϕ_{M1}=4.77 eV) and material (M2) with low work function (ϕ_{M2}=4.1 eV) are considered at length L1 and L2, respectively. The n^+ source/drain is doped with a concentration of 10^{19} cm^{-3} and p-type channel is uniformly doped with concentration of 10^{16} cm^{-3}. The value of V_{DS} is considered as 0.5 V. The various device dimensions are taken as gate length (L)= 30 nm with L1=L2=15 nm, fin thickness (T_{si})=10 nm, fin height (H_{fin})= 20 nm, gate oxide thickness (t_{ox})= 1.5 nm, and buried oxide height (B)= 60 nm.

Simulation of the proposed GaAs DMG FinFET is carried out in TCAD Sentaurus tool [8]. In simulator the models we have activated as Fermi-Dirac distribution, Phonon mobility SRH recombination, quantum density gradient for quantum correction effect, and bandgap narrowing model.



(a) (b)

Fig.1. (a) 3D view of proposed DMG GaAs FinFET and (b) 2D view of DMG GaAs FinFET.

III. RESULTS AND DISCUSSION

Here, a comparative study between SMG and DMG FinFET is presented. An investigation on the effect of temperature on various electrical parameters in DMG GaAs FinFET is discussed.

A. *Comparison between SMG and DMG GaAs FinFETs*

The comparison of surface potential between SMG and DMG GaAs FinFETs is shown in Fig. 2(a). Due to the presence of two different work function in the gate region, a step potential is observed in DMG structure which reduces the impact of drain bias and leads to improvement in DIBL effect. The comparison of drain current characteristic between SMG and DMG FinFETs is summarized in Fig. 2(b) and a significant improvement in on and off current are achieved for the DMG-GaAs FinFET. Furthermore, SS value of SMG and DMG GaAs FinFETs are 76.95 and 69.75 mV/dec, respectively. Because of these advantages, an analysis on the effect of temperature has been investigated in the proposed device.

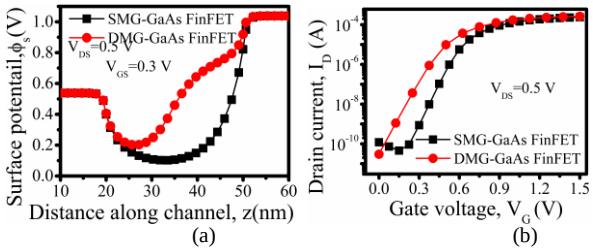


Fig. 2. Comparison between SMG and DMG GaAs FinFETs (a) Surface potential and (b) Drain current.

B. *Effect of Temperature on Electrical Parameters in DMG-GaAs FinFET*

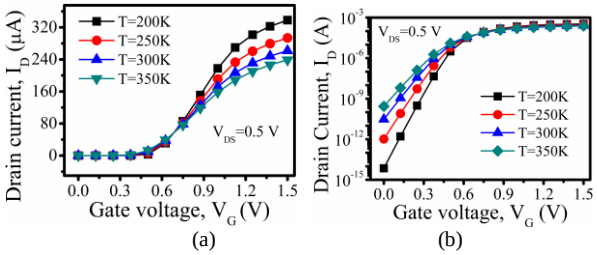


Fig. 3. Effect of temperature on drain current in (a) linear scale and (b) log scale.

The effects of temperature on drain current in linear and log scale are portrayed in Figs. 3(a) and (b), respectively and an opposite effect of temperature is observed at low and high gate bias. At high gate voltage, the mobility of the carrier degrades due to scattering effect [7] which reduces the value of on current as shown in Fig. 3(a). However, at low gate bias, the effect of mobility degradation is not prominent and energy bandgap reduces with increase in temperature [7], which increases the off current as shown in Fig. 3(b). A zero temperature coefficient (ZTC) is observed in drain current characteristics at a gate voltage of 0.6 V. As subthreshold current increases with a rise in temperature which leads to increase in threshold voltage.

Transconductance $(g_m = \partial I_D / \partial V_{GS})$ also shows the same trend as drain current. At high gate, it increases with decrease in temperature and an opposite behavior is observed at low gate bias (Fig. 4(a)). It is seen from Fig. 4(b) gate capacitance increases with increase in temperature and this is due to a reduction in energy barrier with temperature which increases the amount of charge carrier and hence gate capacitance increases.

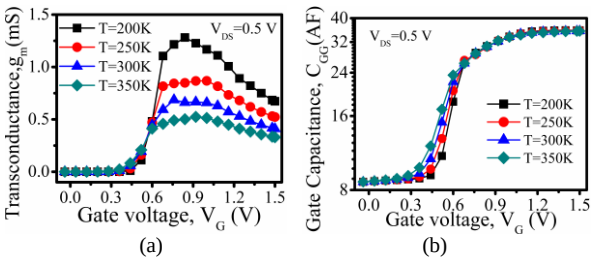


Fig. 4. Effect of temperature on (a) Transconductance and (b) Gate capacitance.

IV. Conclusions

An investigation on the influence of variation in temperature on drain current characteristic, transconductance, and gate capacitance is reported for DMG GaAs-FinFET. The result shows that as temperature increases drain current increases and decreases in subthreshold and superthreshold region, respectively. Like drain current, transconductance also shows similar trends with rise in temperature. Therefore, the temperature has a prominent effect on device characteristics and such analysis will be beneficial for design consideration of this device.

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On the Impact of Channel Compositional Variations on Total Threshold Voltage Variability in Nanoscale InGaAs MOSFETs

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Introduction. The latest International Roadmap for Devices and Systems (IRDS) report on "Moore More" gives prominence to variability in InGaAs MOSFETs for logic applications [1]. Specifically, it states that: *"V_T variability due to channel dimensions and composition appears to become a major impediment in using III-V channel material in scaled devices"*. While variability due to channel dimensions fluctuations has been already investigated [2, 3], there are not recent works on variability related to the InGaAs channel compositional variations (i.e., Indium (In) mole fraction fluctuations) in III-V MOSFETs. In this paper, we present for the first time a thorough investigation of threshold voltage (V_T) variability in scaled InGaAs Dual-Gate Ultra-Thin Body (DG-UTB) MOSFETs that includes the effects of compositional variations in the InGaAs channel on device physical properties as well as on the other V_T variability sources. Simulations results are exploited to identify the worst-case total relative V_T variability at different amounts of In mole fraction variations, which may serve as a reference for technologists. Moreover, by analyzing sensitivity to channel compositional variations we assess their side-effects on both V_T and the other variability sources.

Simulations setup. The InGaAs DG-UTB MOSFET implemented in the Synopsys Sentaurus device simulator is shown in Fig. 1. The template device (physical gate length L_G = 15 nm, V_{DD} = 0.63 V) is realized starting from the International Technology Roadmap for Semiconductor (ITRS) prescriptions [4]. Our simulations are fully-3D quantum-corrected drift-diffusion (QDD), calibrated against higher-order models [5], see Fig. 2. The process parameters nominal values are included in Tab. I.

Variability modeling. Variability is assessed with the statistical IFM method [6]. The sources of statistical variability considered in this work are Random Dopant Fluctuation (RDF in both channel and source/drain regions), Work Function Fluctuation (WFF), Body- and Gate- Line Edge Roughness (B-LER/G-LER), and Band Gap Fluctuation (BGF). In Fig. 3, we show results for V_T variability, i.e. $\sigma(V_T)$, due to the five variability sources. The parameters related to the modeling of these sources are summarized in Tab. I, and are taken either from ITRS (RDF, LER) or specific literature (WFF) [7]. BGF stems from InGaAs compositional variations, and the modeling of BGF-induced variability requires considering the spatial inhomogeneity in the InGaAs crystal lattice [8, 9] and the associated bandgap variation (δE_G). Our modeling approach considers the shifts of both valence and conduction band edges when calculating the total δE_G, according to the simple model in Tab. I, relating it to electron affinity variations $\delta\chi$ [10]. We modeled the In content spatial inhomogeneity by means of a granular approach (similar to WFF, adopted for gate metal granularity [3, 7]). The channel domain is divided into "grains" of different types and sizes, each type associated with a different bandgap value (E_G) and occurrence probability; the size is randomized around an average value. Figures 4 and 5 show for example two different tessellations considering 20 and 2 possible grain types, respectively. Another possible solution (computationally more effective) relies on approximating the grain tessellation with a continuous random profile, shown in Fig. 6, obtained using a Fourier approach with Gaussian covariance function (hereafter, Gaussian approach) [6], characterized by the correlation length, Λ_{BGF} (analogous to the avg. grain size) and the peak E_G variation value, δE_G, see Tab. I. A comparison between the two approaches is reported in Fig. 7, showing the BGF-induced $\sigma(V_T)$ vs. either Λ_{BGF} or the avg. grain size. The Gaussian approach well approximates the grain tessellation one when considering only two possible grain types. A larger number of possible grain types reduces the BGF-induced $\sigma(V_T)$. In all cases, $\sigma(V_T)$ saturates at high Λ_{BGF} or avg. grain size. Thus, by adopting a Gaussian approach with Λ_{BGF} = 300 nm, see Fig. 7, we can perform a worst-case estimation of the BGF-induced $\sigma(V_T)$. Since the latter only depends on δE_G, the E_G variations can be translated into corresponding In mole fraction (x) variation, Fig. 8, by considering the $E_G(x)$ model implemented in the simulator (see inset in Fig. 8). Experimental $E_G(x)$ curves in Fig. 8 (inset) are reported for reference [12].

Results. Starting from BGF-induced $\sigma(V_T)$ results shown in Fig. 8, we define corner cases for In mole fraction variations, which can be useful from a technological perspective to project useful worst-case boundaries for x (for a given $\sigma(V_T)$). Three corner cases (CCs) are under study: CC1 is obtained considering E_G variations leading to a BGF-induced $\sigma(V_T)$ value equal to the G-LER $\sigma(V_T)$ (the least impacting source, see Fig. 3). Similarly, in CC3 we consider WFF- and B-LER (the most impacting sources) [3]. CC2 is instead obtained by requiring a total V_T variability (given by the square sum of the individual sources), i.e., $\sigma_{TOT}(V_T) < 25$ mV, including BGF. This value stands in between the experimental $\sigma_{TOT}(V_T)$ of the 22nm and 14nm nodes for Si technology [11], see Fig. 9, and is chosen as a reasonable limit for $\sigma_{TOT}(V_T)$ in InGaAs at the 14nm node. Indeed $\sigma_{TOT}(V_T)$ in InGaAs cannot achieve the same low value as in Si [1-4] but the $\sigma_{TOT}(V_T)$ target value of 25 mV could still be large enough to accommodate BGF effects, see Fig. 9. Although *no significantly large experimental V_T variability datasets for $In_{0.53}Ga_{0.47}As$ scaled devices can be found in the literature*, the dependability of our simulation approach for variability is supported by the agreement of simulations with experimental Si variability data, Fig. 9 [3, 11]. Simulations results are exploited to identify the worst-case total relative V_T variability at different amounts of mole fraction variations, Fig. 10. This outcome may serve as an important reference for technologists to *i)* target appropriate x control to attain reasonable variability; *ii)* get worst-case total variability projections of their fabricated devices, see the comparison with experimental data [9] in Fig. 10. Besides causing BGF (and associated V_T shifts), mole fraction variations have side-effects that may impact other variability sources, due to the associated variation in dielectric constant and effective mass. To investigate these potential issues, we perform a sensitivity analysis [3]: we use the three CCs to define six varied devices with different mole fractions, as each CC has one possible maximum and minimum x value (considering x variations as both x increment and decrement). For each varied device, we analyze variability in terms of $\sigma(V_T)$ for RDF, WFF, B-LER and G-LER. Results in Fig. 11 show that these variability sources are negligibly affected by x variations, except for B-LER. Thus, x variations can change the relative importance of B-LER and WFF, that both dominate in nominal conditions. Indeed, in Fig. 12 we show that B-LER can become the only dominant source (for x increment) or be less impacting than WFF (for x decrement). In addition, mole fraction variations directly affect the nominal V_T. The plot in Fig. 13 clearly indicates that side-effects of BGF are significant, both on $\sigma_{TOT}(V_T)$ and V_T, and must be properly considered for the optimization of process conditions in the variability-limited scaling context forecasted by IRDS for InGaAs technology [1].

Conclusions. We analyzed V_T variability in scaled InGaAs MOSFETs including the role of channel compositional variations. By appropriately modeling the resulting E_G fluctuations, we identified the worst-case total relative V_T variability at different amounts of In mole fraction variations, providing technologists with an important reference. Side-effects of channel compositional variations on other variability sources are found to have a non-negligible impact on B-LER only. These outcomes can be useful for process optimization in the variability-limited scaling context.

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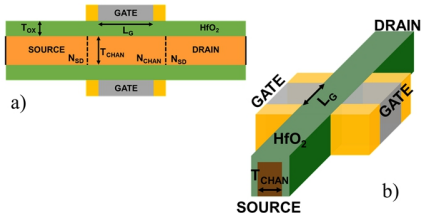

Fig. 1 – DG-UTB structure representation. (a) Cross-section and (b) bird's eye view of the 3D device implemented in the simulator.

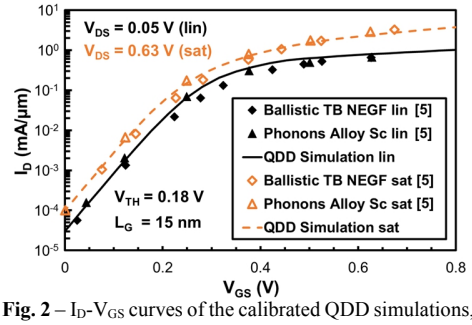

Fig. 2 – I_D-V_{GS} curves of the calibrated QDD simulations, in both linear (black line) and saturation (orange line) regimes. Symbols are higher-order simulations [5].

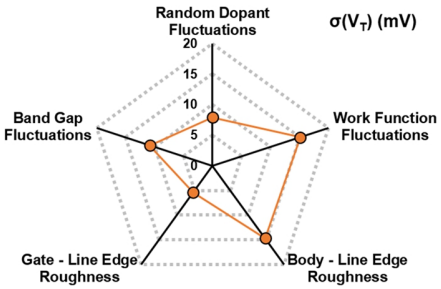

Fig. 3 – Comparison of the V_T variability for the sources considered in our simulations, including BGF ($\delta\chi$ = 10 meV, Λ_{BGF} = 300 nm, see Tab. I).

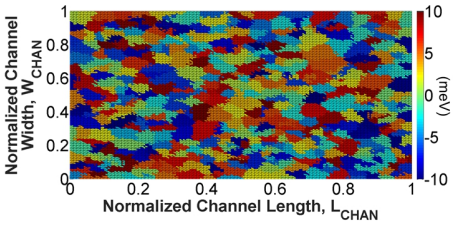

Fig. 4 – InGaAs band-gap variation in a 2D slice of the channel, distributed with Grain tessellation. In this case, 20 types of grains (each with different E_G value) are considered. The band-gap variations are between ±10 meV. The average normalized grain size is 0.02.

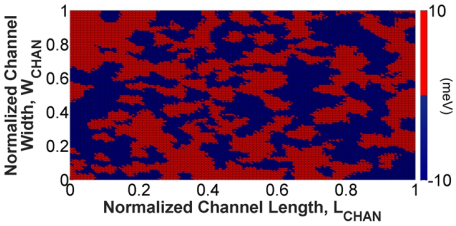

Fig. 5 – InGaAs band-gap variation in a 2D slice of the channel, distributed with Grain tessellation. In this case, 2 types of grains (each with different E_G value) are considered. The band-gap variations are between ±10 meV. The average normalized grain size is 0.02.

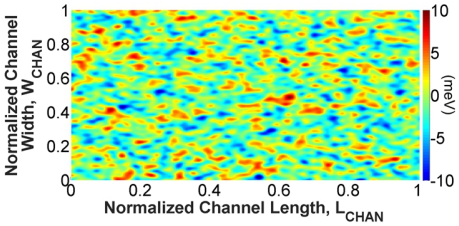

Fig. 6 – InGaAs band-gap variation in a 2D slice of the channel, distributed with Gaussian approach. The band-gap variations are between ±10 meV. The normalized correlation length (Λ_{BGF}) is 0.02.

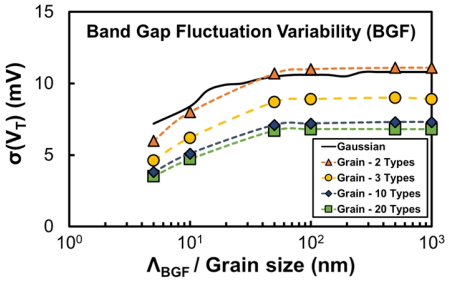

Fig. 7 – BGF-induced variability dependence on Gaussian correlation length (Λ_{BGF}) or avg. grain size. Solid line refers to the Gaussian approach, dashed lines to grain tessellation. Different symbols are related to a different number of possible grain types. In all cases $\delta\chi$ = 10 meV, see Tab. I.

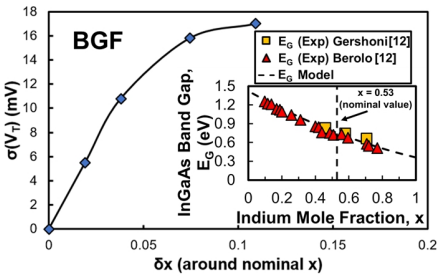

Fig. 8 – BGF-induced variability dependence on mole fraction variation, δ*x*. The inset shows the E_G vs. *x* model used in the simulator (compared with experimental data [12], symbols).

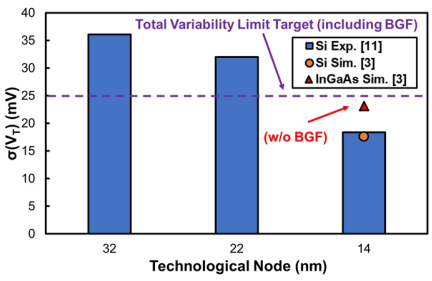

Fig. 9 – Total variability for Si (experimental and simulation) and for InGaAs (sim. only). The target variability limit is evidenced, imposing a maximum tolerable BGF value for a specific corner case (CC2).

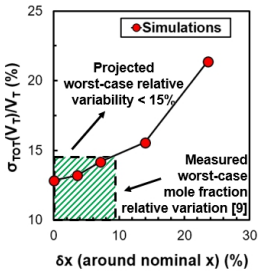

Fig. 10 – $\sigma_{TOT}(V_T)/V_T$ % variation vs. *x* % variation, δ*x*. Measured worst-case δ*x* [9] gives a projected worst-case $\sigma_{TOT}(V_T)/V_T$<15%.

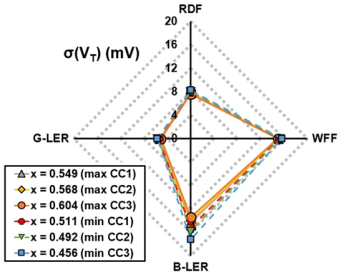

Fig. 11 – Variability due to RDF, WFF, B-LER and G-LER for different In mole fractions. Three corner cases are analyzed (each with min/max *x* values).

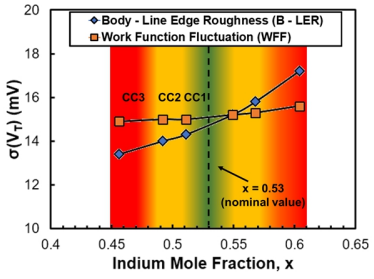

Fig. 12 – Variability dependence on In mole fraction for B-LER and WFF. The three corner cases are highlighted with colored areas in the background.

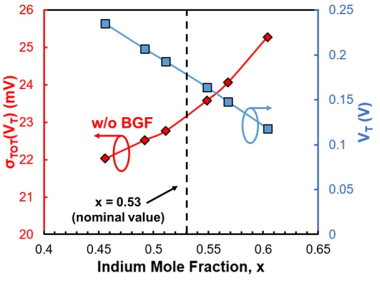

Fig. 13 – Total variability w/o BGF (left y-axis) and threshold voltage (right y-axis) dependence on *x*.

Process Parameters Nominal Values	Band Gap Fluctuations	Gate- and Body-Line Edge Roughness	Work Function Fluctuations
L_G =15 nm			
W_G = 26 nm	$\delta\chi$ = 10 meV	Δ_{rms} = 1.8 nm	Avg. Grain Size = 5 nm
N_{CHAN} = 10^{17} cm^{-3}	Λ_{BGF} = 300 nm		P_{WF1} = 60%
$N_{S/D}$ = $5\cdot10^{19}$ cm^{-3}	α = -1.3		
T_{OX} = 3.8 nm	$\delta E_G = \alpha \cdot \delta\chi$	Λ_{LER} = 15.5 nm	P_{WF2} = 40%
T_{CHAN} = 7 nm			

Tab. I – Process parameters nominal values [3, 4] and parameter values for the variability sources according to ITRS specifications and specific literature [7]. The only parameters needed for RDF are the nominal doping in the channel, N_{CHAN}, and in the source/drain regions, $N_{S/D}$.

Effects of Stress and Strain Distribution on Performance Analysis of GaN/InGaN/GaN Core/Shell/Shell Radial Nanowires for Solar Energy Harvesting

S. R. Routray, *Student Member, IEEE* and T. R. Lenka, *Sr. Member, IEEE*

***Abstract*—In this paper the influence of stress and strain distribution on the performance of III-Nitride nanowire photovoltaic devices are investigated. The strain-induced polarization behavior of GaN/$In_xGa_{1-x}N$/GaN core/shell/shell triangular nanowire solar cell with {0001}, {1-10-1}, {-110-1} or {000-1}, {1-101}, {-1101} set of facets are intensively studied by numerical modeling. It is observed that nanowire solar cells possess an irregular pattern of polarization charges due to complex distribution of stress and strain parameters depending upon growth orientations. Finally, effect of polarization charges on optical and electrical performance of nanowire solar cell are investigated in detail. It reveals that stress and strain distribution in nanowires and its consequent polarization effects have favorable influence on III-Nitride NW photovoltaic devices. This numerical study demonstrates that the issues of self-induced electric field and crystal quality in III-Nitride planar solar cell can be overcome by recent state-of-the-art growth techniques of NWs.**

Keywords: Polarization, Stress, Strain, Solar cell, Energy

1. Introduction

Over a decade, Gallium Nitride and its alloys such as InGaN have attracted more attention as next generation resourceful building block to harvest solar energy due to their outstanding physical and chemical stabilities, radiation resistance, high light absorption capability and tunable bandgap (~0.64eV to ~3.4eV) [1], [2]. However, conversion efficiency of planar solar cell is limited to 2-3% till date [3], [4] due to poor quality of crystal growth of InGaN on GaN template and generation of polarization charges at the interface. Due to the intrinsic asymmetry of the bonding in the wurtzite crystal structure, inherent charges exist in the material which, in general known as *spontaneous* polarization. Additionally, due to *pseudo-morphic* growth of heterojunction, deformations at the interface takes place to accommodate the different lattice constant [5]. This process leads to generation of stress and strain and stuck immobile charge carriers at interface, known as *piezoelectric* polarization. Alternatively, application of GaN/InGaN nanowire (NW) solar cell could be a potential solution to this problem due to its partially relaxed stress and strain effect, efficient carrier collection into orthogonal spatial direction, efficient light trapping and low dislocation density due to substrate free standing [1], [5-6].

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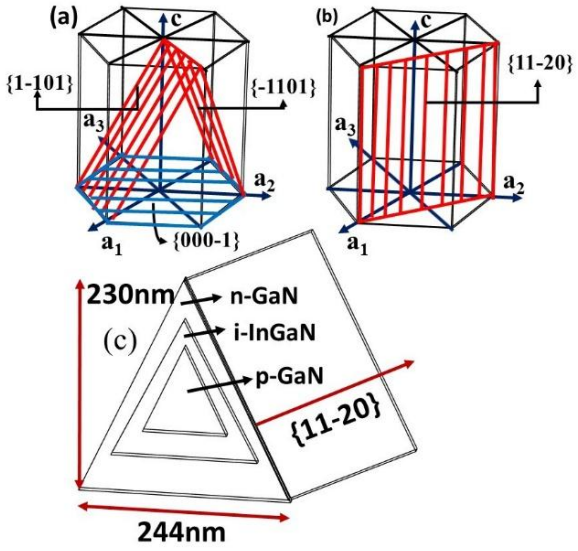

Fig. 1 Six-fold hexagonal crystal structure showing (a) triangular crystal plane (b) {11-20} growth direction (c) triangular nanowire facets

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Prototype of NW photovoltaic and photonics devices based on GaN/$In_xGa_{1-x}N$/GaN core/shell/shell (CSS) structure have already been reported with different structural motifs [6-10]. A complete crystal growth planes of triangular NW and its growth direction along {11-20} in a six-fold wurtzite crystal structure are shown in Fig.1 (a) and (b) respectively. Depending on the growth conditions, geometry of triangular nanowire may have two distinct sets of crystal planes of either {0001}, {1-10-1}, {-110-1} or {000-1}, {1-101}, {-1101} as shown in Fig. 1(c). Since two side wall facets of NW are inclined to base plane, stress and strain effect have a complex dependency on this growth orientation, thickness and angle of inclination of different facets in nanowire [11].

It is understood from our previous investigation that, performance of the reported GaN/$In_xGa_{1-x}N$/GaN solar cells are mainly affected by a strong internal polarization field, when the growth of the InGaN layer is terminated along the Ga-face [0001] orientation of {11-20} growth direction [12], [13]. Mastro *et al.* also investigated the polarization charges at different polar and semipolar facets of NW transistor but they neglected study of stress and strain effect of the NW [14-16]. To the best of author's knowledge, the theoretical and practical studies of III-Nitride CSS NW solar cell considering appropriate calculation of polarization effect are still in the infant stage. Therefore, in this paper, estimation of strain, stress and consequent polarization charges are performed using numerical calculations.

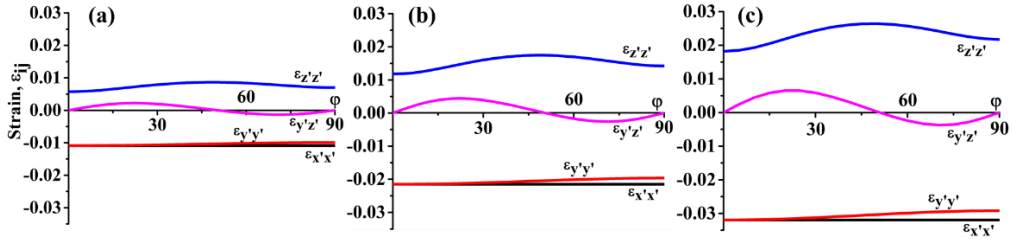

Fig.2 Elastic Strain in GaN/InGaN anisotropic mismatched layer as a function of inclination angle φ for (a) x=0.1 (b) x=0.2 and (c) x=0.3

2. Device Structure and Parameters

The triangular nanowire structure consists of n-GaN outer shell of thickness 40 nm followed by i-InGaN inner shell of thickness 25 nm, p-GaN core of thickness 100 nm and other thicknesses are calculated by an isosceles trigonometric calculations and simulated using Victory 3D Luminous [17]. The InGaN crystal has a larger lattice constant than p-GaN, thus a-axis lattice spacing must compress to match with underlying GaN lattice. In order to accommodate a compression in a-axis lattice spacing, c-axis lattice requires to increase its spacing. This contraction along the c-axis of metal atom and N atom at {0001} plane leads to induce a stress and consequently negative piezoelectric polarization field parallel to surface normal. The crystal lattice parameter a_L and c_L for $In_xGa_{1-x}N$ can be calculated using linear interpolations of Vegard's law as [18]:

$$a_L = x.a_{\mathrm{InN}} + (1-x).a_{\mathrm{GaN}},$$
$$c_L = x.c_{\mathrm{InN}} + (1-x).c_{\mathrm{GaN}} \quad (1)$$

where, $a_{\mathrm{InN}}, a_{\mathrm{GaN}}, c_{\mathrm{InN}}$ and c_{GaN} are the lattice parameters of InN and GaN [18]. In order to describe strain effect, the proposed model considers two coordinate systems *i.e. xyz* and x′y′z′ for natural c-axis coordinate of wurtzite crystal and prime surface normal coordinates oriented in semipolar crystal respectively. Considering symmetrical space group *P6₃mc* of wurtzite III-Nitrides, polarization charges are related to the strain effect between two subsequent layers and is given by [18]:

$$P^{pz} = \begin{pmatrix} e_{15}\varepsilon_{xz} \\ e_{15}\varepsilon_{yz} \\ e_{31}(\varepsilon_{xx}+\varepsilon_{yy}) + e_{33}\varepsilon_{zz} \end{pmatrix}, \quad (2)$$

The total polarization component P_{total} between polar and semipolar layer is determined in the prime-coordinate system as [18]:

$$P_{total} = -\left[P_{Lz'}^{pz} + \left(P_L^{sp} - P_T^{sp}\right)cos\varphi\right] \quad (3)$$

where, P_L^{sp} and P_T^{sp} are the spontaneous polarization of the top layer and bottom template respectively and can be calculated as Ref. [18]. The strain induced piezoelectric polarization component, $P_{Lz'}^{pz}$ is calculated by [15, 18]

$$P_{Lz'}^{pz} = \varepsilon_{x'x'}(e_{31}cos\varphi) + \varepsilon_{y'y'}\left(e_{31}\cos^3\varphi + \frac{e_{31}-e_{15}}{2}\sin\varphi\sin 2\varphi\right) + \varepsilon_{z'z'}\left(\frac{e_{31}+e_{15}}{2}\sin\varphi\sin 2\varphi + e_{33}\cos^3\varphi\right) + \varepsilon_{y'z'}\left((e_{31}-e_{33})\cos\varphi\sin 2\varphi + e_{15}\sin\varphi\cos 2\varphi\right) \quad (4)$$

where strain tensor components $\varepsilon_{i'j'}$ are determined by simulating the strain profile using NextNano3 [19], which performs global strain minimization based on macroscopic elastic theory and stiffness coefficients, C_{ij} for the simulations are considered from Ref. [20] . The distribution of stress components can be calculated by Hook's law using strain parameters [18] as follows.

$$\sigma_{x'x'} = C_{11}\varepsilon_{x'x'} + (C_{12}\cos^2\varphi + C_{13}\sin^2\varphi)\varepsilon_{y'y'} + (C_{12}\sin^2\varphi + C_{13}\cos^2\varphi)\varepsilon_{z'z'} + (C_{12} - C_{13})\sin 2\varphi\,\varepsilon_{y'z'} \quad (5)$$

$$\sigma_{y'y'} = (C_{12}\cos^2\varphi + C_{13}\sin^2\varphi)\varepsilon_{x'x'} + \left(C_{11}\cos^4\varphi + \frac{C_{13}+2C_{44}}{2}\sin^2 2\varphi + C_{33}\sin^4\varphi\right)\varepsilon_{y'y'} + \left[\left(\frac{C_{11}+C_{33}}{4} - C_{44}\right)\sin^2 2\varphi + C_{13}(\sin^4\varphi + \cos^4\varphi)\right]\varepsilon_{z'z'} + \sin 2\varphi\left[(C_{11}-C_{13})\cos^2\varphi + (C_{13}-C_{33})\sin^2\varphi - 2C_{44}\cos 2\varphi\right]\varepsilon_{y'z'} \quad (6)$$

$$\sigma_{z'z'} = (C_{12}\sin^2\varphi + C_{13}\cos^2\varphi)\varepsilon_{x'x'} + \left[\left(\frac{C_{11}+C_{33}}{4} - C_{44}\right)\sin^2 2\varphi + C_{13}(\sin^4\varphi + \cos^4\varphi)\right]\varepsilon_{y'y'} + \left[C_{33}\cos^4\varphi + \left(\frac{C_{13}}{2} + C_{44}\right)\sin^2 2\varphi + C_{11}\sin^4\varphi\right]\varepsilon_{z'z'} + \left[(C_{11}-C_{13})\sin^2\varphi + (C_{13}-C_{33})\cos^2\varphi + 2C_{44}\cos 2\varphi\right]\sin 2\varphi\,\varepsilon_{y'z'} \quad (7)$$

$$\sigma_{y'z'} = \left(\frac{C_{12}-C_{13}}{2}\right)\sin 2\varphi\,\varepsilon_{x'x'} + \left[\left(\frac{C_{11}-C_{13}}{2}\right)\cos^2\varphi + \frac{C_{13}-C_{33}}{2}\sin^2\varphi - C_{44}\cos 2\varphi\right]\sin 2\varphi\,\varepsilon_{y'y'} + \left(\frac{C_{11}-C_{13}}{2}\sin^2\varphi + \frac{C_{13}-C_{33}}{2}\cos^2\varphi + C_{44}\cos 2\varphi\right)\sin 2\varphi\,\varepsilon_{z'z'} + \left[\left(\frac{C_{11}+C_{33}}{2} - C_{13}\right)\sin^2 2\varphi + C_{44}\cos^2 2\varphi\right]\varepsilon_{y'z'} \quad (8)$$

where, C_{11}, C_{12}, C_{13}, C_{33} and C_{44} are the fourth rank elastic stiffness tensor coefficients in prime coordinate system. $\sigma_{i'j'}$ is the stress tensor parameters in prime coordinate system [18].

3. Results and Discussion

Proper determination of stress and strain profile at each interface leads to an efficient design of III-Nitride solar cell. Fig. 2 represents elastic strain ($\varepsilon_{x'x'}, \varepsilon_{y'y'}, \varepsilon_{z'z'}$) and shear strain ($\varepsilon_{y'z'}$) at different inclination angle φ. In general, the zero cross-over point depends on different 'In' content of InGaN

alloy due to variation in lattice parameter but this dependency are less than 1° in case of InGaN/GaN interfaces.

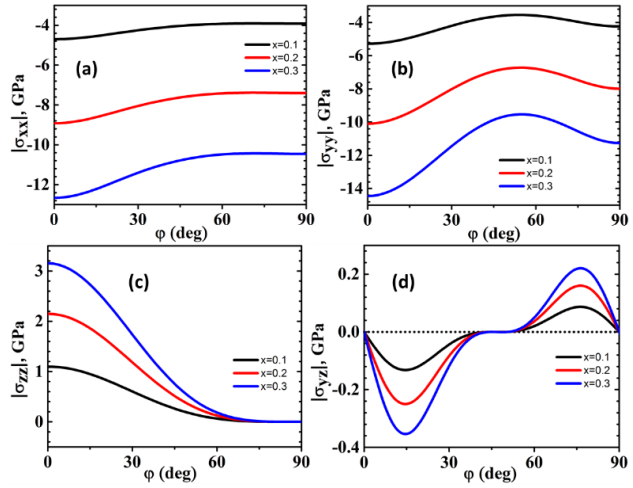

Fig. 3 Stress distribution parameter (a) $\sigma_{x'x'}$ (b) $\sigma_{y'y'}$ (c) $\sigma_{z'z'}$(d) $\sigma_{y'z'}$ as a function of inclination angle φ.

Thus this effect is neglected for stress and strain calculations. The strain components are further calculated to obtained stress distribution and total polarization at polar and semipolar facets of nanowire as given in Eqs. (3) and (4). The reliable data for spontaneous polarization, piezoelectric coefficient and elastic constants are taken from Ref. [12-13], [21] and Vegard's law of linear interpolation is applied to calculate parameters for InGaN alloys.

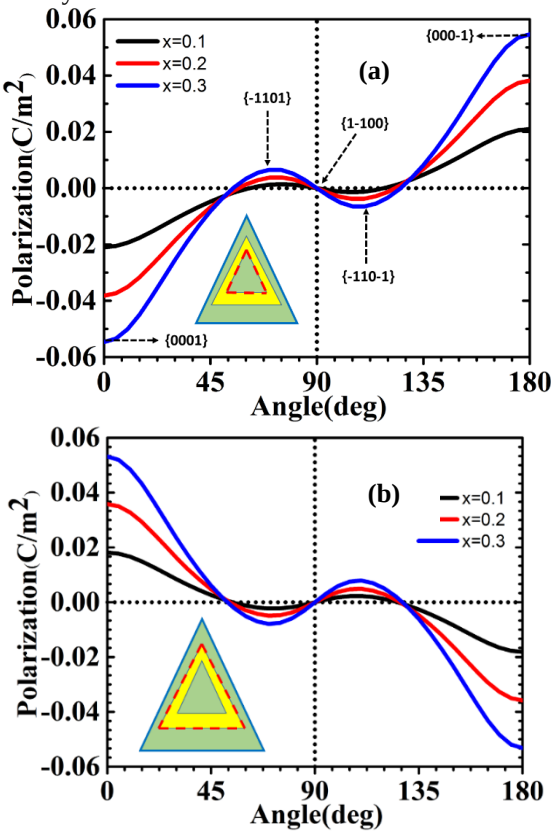

Fig. 4 Net Polarization charges composed of spontaneous and piezoelectric polarization at (a) Core/Shell (p-GaN/i-InGaN) (b) Shell/Shell (n-GaN/i-InGaN) interfaces of Core/Shell/Shell NW as a function of c-axis inclination angle, φ. Insets show the corresponding n-GaN/i-InGaN and i-InGaN/p-GaN interface of triangular NW solar cell under consideration.

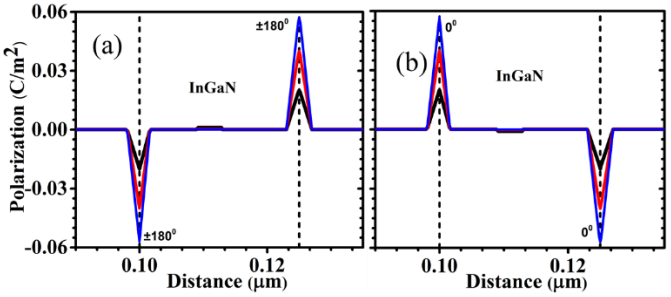

Fig. 5 Density of total polarization charges $\boldsymbol{P_{total}}$ along vertical cut of (a) {000-1}/±180° and (b) {0001}/0° plane of triangular NW.

Fig. 3 (a)-(d) show the stress tensor components as function of inclination angle of NW facets. It shows that generation of stress due to lattice deformation are high along X and Y direction of NW at 60° to 90° inclination angle (semipolar planes) as shown in Fig. 3(a) and (b). However, stress along these directions doesn't affect much on the carrier separation process of NW solar cell. In other hand, Stress formation are negligible at 60° to 90° and high at 0° along Z direction and Y-Z direction of nanowire as shown in Fig. 3 (c) and (d), which is the spatial direction of carrier separation in nanowire solar cell. Thus effect of stress along semipolar facets of nanowire with inclination angle of 62° have less influence on performance of solar cell. Additionally stress along X-Y and X-Z direction are neglected due to traction free surface [18]. It is noteworthy to mention that stress distribution at 118° and 180° inclination angle are just the mirror image of 62° and 0° respectively. Fig. 4 (a) and (b) show net polarization field of NW along n-GaN/i-InGaN and i-InGaN/p-GaN interfaces along 0° to 180° inclination angle of facets respectively, which are also in a good agreement with the theoretical results reported by Mastro *et al.* (2010). The analogous cosine wave polarization charges observed at {0001} and {000-1} planes of NW is due to inverted crystallographic orientation at ±180°/{000-1} as that of 0°/{0001} plane. It follows from the polarization plot that for $\varphi = 90°$, piezoelectric and spontaneous charges tend to zero, which provide a zero cross-over at this inclination angle. However, zero cross-over at $\varphi \approx 45°/135°$ are due to the cancellation of piezoelectric charges and spontaneous charges having opposite sign. But growth of NW along these zero polarization angle is an experimental constrain till date due to unstable crystal growth. Alternatively, polarization charges are peak at 0° and ±180° since P*sp* and P*pz* charges are in same phase. Polarization charges at {000-1} plane are same in magnitude as {0001} plane but opposite in polarity. It is because of the termination of InGaN layer with N-face at {000-1} growth direction as compared to Ga-face at {0001} direction.

The simulation of the proposed triangular NW solar cell is carried out by incorporating corresponding polarization charges at different facets under the illumination of one sun AM1.5 global irradiance by exposing the light vertically on the front surface (as shown in Fig.1) of the NW. The {0001} facet of NW is characterised as 0°, and inverted {000-1} plane as ±180° as mentioned in Fig. 1 (c). It is observed that polarization charges are counter-productive at 0° due to compensation of normal built-in electric field by self-induced electric field and hence, the total electric field reduces. However, polarization

charges are favorable at ±180° as built-in electric fields are in same phase with self-induced electric field of NW solar cell. Small magnitude oscillations are observed along 45° to 90° which are originated from the stress relaxation along these angle as discussed in Fig.3. Since stress is a basic parameter in lattice mismatched interfaces, it affects polarization charges up to a great extent. It is also clear from the relationship as given in Eq.4-8, where strain is a common parameter between stress and polarization charges. The effect of polarization charges along these planes possess negligible importance on carrier dynamics of NW solar cell. Thus, investigations are more focused at polar plane (0°) and reversed-polar plane (±180°) because these planes are considerably influence the carrier separation mechanism in NW solar cell. Fig.5 (a) and (b) show the overall polarization field of n-GaN/i-InGaN/p-GaN CSS NW Solar cell along the interfaces of vertical cut line at ±180° and 0° respectively. It is clear that polarization charges at 0° and ±180° are opposite to each other in polarity along n-GaN/i-InGaN and i-InGaN/p-GaN interfaces, which are due to lattice expansion/compression of InGaN layer above/under the p-GaN/n-GaN layer respectively.

It is remarkable that two-dimensional electron gas (2DEG) is observed at n-GaN/i-InGaN interface along {000-1} facet, which accumulates some of the carriers at higher bias voltage. Thus, carrier collection at {000-1} facet may also affect at higher 'In' content due to high recombination rate and carrier accumulation in 2DEG [29]. Considering overall effect of reversed-polar {000-1} and all semi-polar {-1101} facet of NW and comparing with polar facet (0001) as discussed above, it is evident that 10% 'In' composition in InGaN absorber layer shows better performance as compared to 20% and 30%, because of low recombination rate, negligible carrier accumulation by potential well and favorable energy band tilting for efficient carrier collection.

4. Conclusion

The theoretical calculation and simulation of stress and strain distribution show a nonlinear dependence of spontaneous and piezoelectric charges with inclination angles of nanowire facets. It suggest that n-GaN/i-$In_xGa_{1-x}N$/p-GaN CSS NW with {000-1}, {1-101}, {-1101} set of planes is favorable for photovoltaic applications due to reversed polar plane and semipolar planes. Moreover, {1-101} and {-1101} planes of nanowire are quite insensitive to polarization field due to relaxation of stress and strain at 62° inclination angle. These novel findings provide possibility of fabricating high-efficiency III-Nitride NW solar cells for energy harvesting.

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