Passivation controlled field effect mobility in 2D semiconductor based FET devices for high performance logic circuit development on flexible platform

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Introduction

In two-dimensional transition metal dichalcogenides (TMDs) based micro and nanoelectronic devices, optimal passivation and doping strategies is an issue of utmost importance for improved charge carrier mobility, desirable operating points, hysteresis-free operation and long-term stability. For devices on flexible platform, additional issues like mechanical flexibility of the coatings and lower thermal treatments also need considerations. In the current work, we present our results on impact of different passivation methods on the performance of CVD grown MoS_2 based FET devices on flexible substrates.

Experimental

For the experiment, MoS_2 based backgated MOSFET structure was selected with following device configuration. After the device fabrication, different dielectric layers like ALD grown Al_2O_3, evaporated Parylene N, Parylene C and their combinations were used for passivation and their electrical properties characterized in ambience and in vacuum at different temperatures.

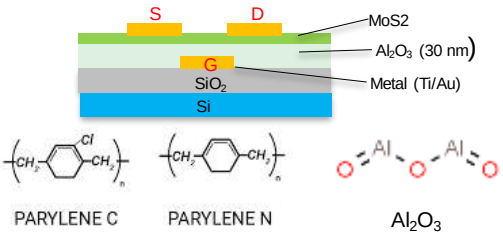

Figure 1. Device architecture (top panel) and chemical structure of the dielectric passivation layers (bottom panel) used in the experiment.

Results

Device current and mobility

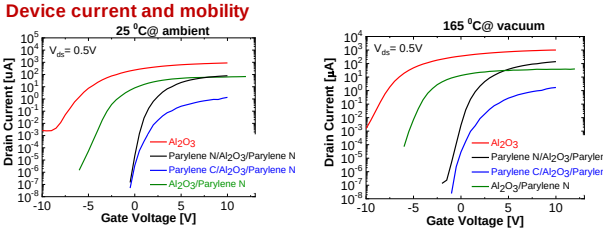

Figure 2. I_{ds}-V_{gs} characteristics at a fixed V_{ds} for the four fabricated devices at ambience (Left) and at high temperature and in vacuum.

Measurement at ambience and under vacuum at high temperature of 165 ^{0}C shows similar trend in I_{ds}-V_{gs} characteristics at a fixed drain-source bias, V_{ds}. The samples with Al_2O_3 passivation shows highest *n*-doping leading to strong negative side shift of the threshold voltage with highest output current. With Parylene passivation, the output current decreases, however, the operating point shifts towards the positive voltage.

The Field effect mobility of the devices were calculated using the equation

$$\mu = (dI_{ds}/dV_{gs}).\ (L/W).\ (1/C_i.V_{ds})$$

where C_i is the capacitance per unit area between the conducting channel and the back gate ($C_i = \varepsilon_0\varepsilon_r/d$; ε_r = 7 for Al_2O_3; d is the thickness of Al_2O_3 (30 nm), L is the channel length (~1 µm) and W is the channel width (365 µm). The typical field effect mobility of the devices varies from 10^{-3} cm^2 V^{-1} s^{-1} for Parylene C/ Al_2O_3/ Parylene N coated FETs to **1.7 cm^2 V^{-1} s^{-1}** for 100 nm Al_2O_3 coated FETs. Best device on/off ratio vary between 10^7 for Al_2O_3 coated devices to 10^9 for Parylene N/Al_2O_3/ Parylene N coated devices.

Hysteresis

In terms of hysteresis in the I_{ds}-V_{gs} curves, the sample coated with Parylene N/Al_2O_3/ Parylene N showed smallest hysteresis between up and down sweeps when measured in ambience and in vacuum with significant improvement in vacuum annealed samples.

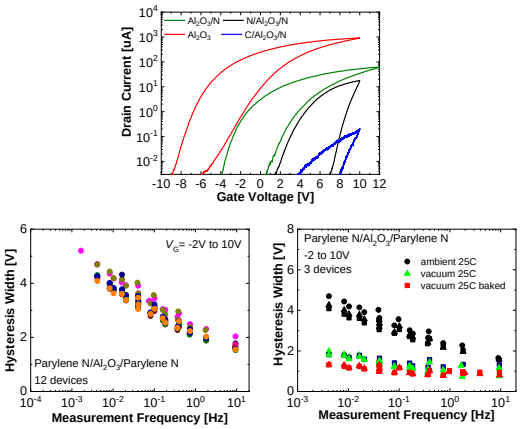

Figure 3. (Top) I_{ds}-V_{gs} hysteresis for up and down sweeps of V_{gs} at a fixed V_{ds} for the four fabricated devices at ambience. (Bottom) Hysteresis as a function of measurement frequency for the Parylene N/ Al_2O_3/ Parylene N coated devices at room temperature (left) and in vacuum (right) showing significant improvement in hysteresis due to baking in vacuum.

This improvement in hysteresis in vacuum annealed samples clearly indicate charge transfer from/to absorbed molecules like water, the most abundant dipolar adsorbate under ambient condition, to be the major reason for hysteresis in the MoS_2 transistors. Defect sites, caused by the absorbed water molecules at the MoS_2/ dielectric interface form charge trapping sites, causing a large hysteresis. Significantly reduced and nearly measurement frequency independence of hysteresis in the vacuum annealed samples indicate presence of lower amount of charge trapping sites in these samples, which is expected due to removal of water vapor when heated to 165 ^{0}C in vacuum. Therefore, it can be concluded that thermal annealing in high vacuum condition and a proper encapsulation before taking the sample out in ambience can significantly improve device hysteresis.

Reproducibility

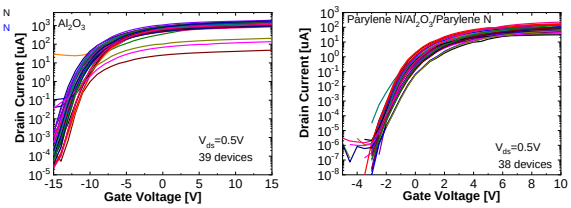

Figure 4. (Left) I_{ds}-V_{gs} characteristics of (left) Al_2O_3 coated 39 devices and (right) Parylene N/ Al_2O_3/ Parylene N coated 38 devices showing good reproducibility beween devices.

Conclusion

In conclusion, data from differently passivated MoS_2 FET devices show that it is possible to modify the field effect mobility of the devices by 3 orders of magnitude only through passivation control. The best mobility value arises due to strong *n*-doping arising from ALD grown Al_2O_3 encapsulation layer, while alternate layers of Parylene N and Al_2O_3 gives best performance in terms of hysteresis and passivation, together with a positive shift in the operating point. This study provides potential direction for low thermal budget, high mechanical flexibility strategies to control carrier doping and prevent challenges like poor yield, performance degradation, irreproducibility and instability of TMD based fully integrated circuits on flexible platform.

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