Gate-stack engineered NBTI improvements in high-voltage logic-for-memory high-κ/metal gate devices

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***Abstract*— Potential solutions for the reliability challenges of high-κ metal gate (HKMG) integration into DRAM high-voltage peripheral logic devices are reported. A detailed study of Negative Bias Temperature Instability (NBTI)-degradation, supported by physical analysis, assessing the impact of various tuning components within the stack (interface layer, high-κ fluorination and/or cap, metal gate) is presented. The presence of Nitrogen throughout the HKMG stack can originate either from high-k processing or metal-nitride gate electrode. It is shown that preventing nitrogen diffusion towards the Si/SiO_2 interface region, together with AlO_x (and F) incorporation at the HKMG interface, can tune device threshold voltage and modulate access to donor trap-defect bands. The result of these effects is a vast improvement in NBTI performance.**

***Index Terms*-- Logic for memory, NBTI, defect band access, AlO_x cap**

I. Introduction

The logic-based components on memory chips include sense amplifiers, row decoders, internal refresh, and Input & Output (I/O) access transistors. Collectively, they are frequently referred to as the periphery. Given the range of functionality served by these devices, different V_{dd} values are required for some applications. These peripheral devices have hitherto been based on poly/SiO_2 and lately SiON technologies, with multiple SiO_2 thickness layers employed to enable the required V_{dd} modulation. Among the challenges to continued scaling of the DRAM periphery is the increasing gate leakage current density of the high performance (thinner oxide) devices operating at the lower V_{dd}. Their proposed evolution towards high-κ dielectric/metal gate stacks (HKMG) [1] can mirror that of sub-45 nm CMOS logic technologies, thereby enabling continued cost-limited scaling in next-generation memory devices. Although the leakage-limiting properties of HKMG are not required on the higher V_{dd} / high-voltage (HV) devices *per se*, the use of a single stack across the entire peripheral region enables a cost-limiting integration, as shown schematically in Figure 1 [2].

These logic devices are fabricated in a gate-first scheme, thereby precluding cutting-edge logic processing (e.g. replacement metal gate [3]). DRAM BEOL thermal budgets [4] are sufficiently high to enable elemental diffusion within the HKMG gate stack and introduce reliability challenges: previous reports have demonstrated that high voltage pFET devices (~5nm equivalent oxide thickness, EOT) are vulnerable to Negative Bias Temperature Instability (NBTI) [2, 5].

In this work, the impact of various gate stack process optimizations for high-voltage logic memory applications are explored. These include the SiO_2 layer formation and treatment, materials contained within the high-κ material, and the metal gate electrode. These are assessed in terms of defect density and location in the gate stack. Results demonstrate significant differences in reliability characteristics which are explained.

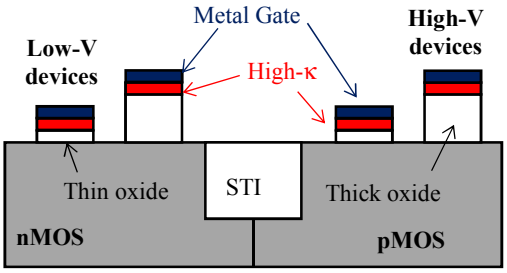

Figure 1. Schematic diagram of varying oxide thickness on devices in the periphery of memory devices, enabling fabrication of varying-V_{dd} devices utilising a single high-κ/Metal gate process, albeit on multiple oxide thicknesses.

II. Device and Measurement Procedure

A. Device Fabrication

The gate-first process employed involves a high temperature oxidation step to form an SiO_2 layer (~5 nm), followed by depositing 2 nm of ALD HfO_2 and a PVD TiN or TaN based metal gate electrode. Subsequent anneal steps include junction activation, simulated DRAM BEOL thermal budget, and sintering [2]. The results of four experiments are reported in this study as follows: 1) the oxidation method for the SiO_2 interface layer, with ISSG (in-situ steam generated), dry thermal oxide, and low temperature ALD SiO_2 followed by high temperature anneal layers compared; 2) the impact plasma nitridation on the SiO_2 layer prior to high-κ deposition; 3) the impact of nitrogen introduced via the gate electrode and 4) the impact of fluorine and/or AlO_x cap incorporation on the high-κ layer.

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B. Experimental procedure

NBTI measurements (using extended MSM [6]) were performed at 125°C on 10x1 µm² planar structures. Data was analysed by (a) multi-variate power law fitting, following (1)

$$\Delta V_t = A_0 * E_{ov}^{\gamma} * t^n, \quad (1)$$

where ΔV_t is the measured threshold voltage shift, E_{ov} the effective electric field, $(V_{g\ stress} - V_t)/EOT$, γ the field power law exponent, t stress time, n the time exponent of ΔV_t degradation, and A_0 a fitting parameter containing the temperature dependent term (which is not varied in this work). NBTI lifetime results are reported as V_{ov}, (or E_{ov}) which is the maximum overdrive voltage (or field) to survive 10 year operation at 30 mV threshold voltage degradation. Data was also analysed by performing (b) Universal model fitting [6], thereby enabling decoupling of the V_t degradation into constituent recoverable (ΔN_R) and permanent (ΔN_P) components [6]. Defect band properties in both the SiO_2 and HfO_2 layers were calibrated to the measured ΔV_t-V_g-t datasets with (c) the Comphy tool. This enables parameters of the 2-state NMP model and simple double-well (DW) [7] which best describe the measured dataset be obtained and analyzed. The measured ΔV_t values were transformed to an effective charge density, to enable an oxide-thickness independent sample to sample comparison, described in (2)

$$\Delta N_{eff} = \frac{\Delta V_t * C_{ox}}{q}, \quad (2)$$

where C_{ox} is the oxide thickness and q is the electronic charge.

The impact of timing of the e-MSM measurement was explored, with the conventional system applied (incorporating ~1 ms delay time between end of stress and commencement of collection of data during relaxation), compared to an ultra-fast system, which reduces this delay time to ~ 1 µs. These results are shown in Figure 2, together with data collected at 1 ms delay time from the ultrafast method.

Note the reduction of the time exponent on increasing the stress time (for $t_s \geqslant 1$ s) observed for the 1 µs ultrafast method, and the higher ΔV_t observed in this case. It is seen that data collected at 1 ms from the ultrafast method overlaps that collected from the conventional method (also at 1 ms). Comphy fits to the ΔV_t-t data are displayed, to which the measured data converges, and increasingly so for the 1 µs delay time. The Recoverable and Permanent defect contributions evaluated from Universal Model fitting are also shown in Figure 2, together with the sum of the two components. This defect density, derived *from the conventional 1 ms delay data,* is higher than that measured at even 1 µs delay time, suggesting some defects in the stack have already relaxed in this time frame, but can be considered with this fitting methodology. This implies defects with sub-microsecond relaxation times are included in the ΔN_R and ΔN_P analysis.

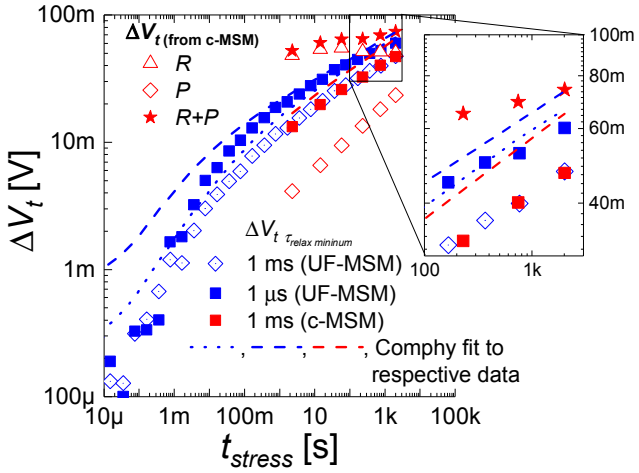

Figure 2. Defect kinetics revealed by conventional and Ultra-Fast-MSM (c and UF, respectively) are comparable for 1 ms $t_{relax\ minimum}$. $\Delta V_{t\ R+P}$ from Universal Model Fitting (to which Comphy fits converge) exceeds $\Delta V_{t\ \tau_{relax} \geq 1\mu s}$, suggesting fast-trap (<1 ms) contribution detected by Universal model [6] fits to c-MSM data.

Capacitance-Voltage measurements were also performed on 50x50 µm² device structures, at 100 kHz *a.c.* frequency, at temperatures in the range 25 to 125°C. Flat-band voltage (V_{fb}) and effective work-function (ϕ_m) values were extracted from CVC fits [8] to the measured data. Changes in V_{fb} with temperature were derived with (3)

$$V_{fb} = \phi_m - \chi_{Si} - \frac{E_g}{2} - \frac{kT}{q} log\left(\frac{N_a}{n_i}\right) - \frac{Q_f}{C_{ox}} \quad (3)$$

where χ_{Si} is the silicon electron affinity, E_g the (temperature-dependent) silicon bandgap, k Boltzmann constant, T temperature, N_a acceptor concentration, n_i the (temperature-dependent) intrinsic carrier concentration, Q_f the fixed charge, and C_{ox} the oxide capacitance.

III. Data/Results and Discussion

A. Effect of SiO_2 oxidation mode

Given the proclivity of near-channel hole traps to contribute to NBTI, several methods for SiO_2 growth/deposition were compared, in a bid to ascertain whether this oxide layer plays a strong role on the near-interface defects. Defect generation kinetics are similar for oxide layers generated from ISSG, thermal oxidation, or PEALD and subsequently annealed, as displayed in Figure 3. All high-κ/MG stacks explored show lower n value than the less defective SiO_2/poly stack. Similar γ values and ΔN_{eff}, suggest no significant impact of oxidation conditions, and that the considerable difference between SiO_2/poly and HKMG stacks are related to other elements in the stack.

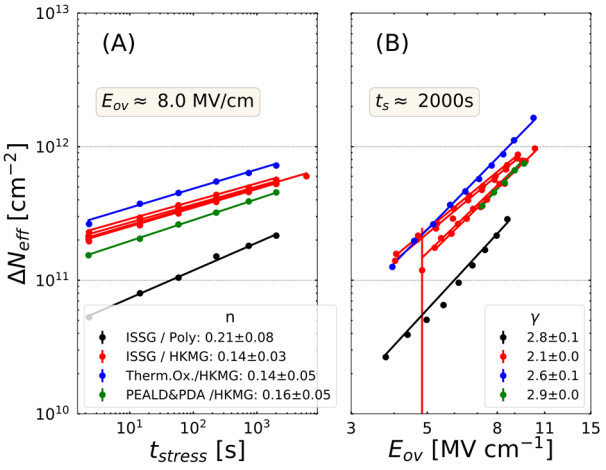

Figure 3. Defect generation (A) kinetics and (B) bias dependence for Si/SiO_2/HK/MG stacks, where the SiO_2 fabrication method was varied. Similar characteristics for all SiO_2 oxidation methods are shown and have higher defectivity than the poly/SiO_2 reference.

B. Impact of Nitrogen incorporation in the dielectric layer

Incorporation of nitrogen in the HK stack has been shown to improve [2] or conversely, degrade device reliability [9]. Varying intensity of a decoupled plasma nitridation (DPN) step, by changing the power during deposition, can modify the N depth profile, together with O content towards the top of the stack (Figure 4), as revealed by ToF-SIMS analysis. For the most intense DPN step, nitrogen permeates almost fully through the underlying SiO_2 layer, while the top region shows similar oxygen and nitrogen concentrations, suggesting the presence of an SiO_xN_y layer. As seen in Figure 5, both the oxygen and nitrogen profiles are depth dependent, and their impact on the BTI reliability was studied.

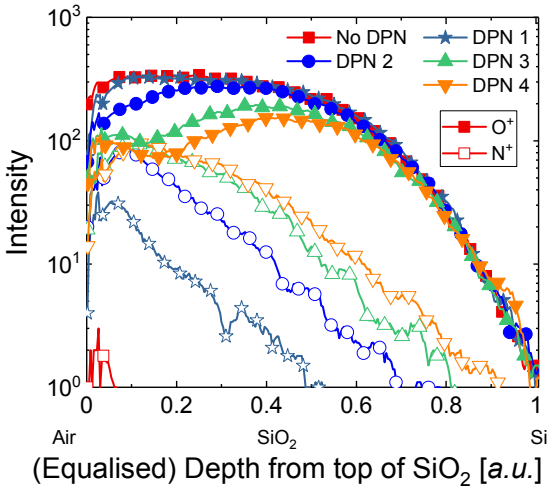

Figure 4. N^+ and O^+ profiles from ToF-SIMS, in SiO_2 layers subjected to DPN steps of varying intensity, show the modification of the interlayer as a function of the DPN step applied. Profiles were equalised to ensure Si signals overlap, with the Si/SiO_2 interface located between 0.6 and 0.7 x-axis

ΔN_R and ΔN_P values derived from Universal Model fitting of measured BTI data are shown in Figure 5(A-B). Increasing the DPN intensity reduces ΔN_R, in agreement with the increasingly N-rich SiO_xN_y acting as a more efficient diffusion barrier for metals (Al, Ti, Hf) [2] during the BEOL anneal steps, with resultant V_{ov} increase (Figure 5(C)). However, on further increasing N, nitrogen permeates closer to the channel, with resultant increase in ΔN_P, and NBTI degradation, consistent with [9]. The incorporation of an SF_6 step, performed subsequent to the plasma nitridation has the effect of reducing the permanent defect density values towards that of the poly/SiO_2 case, together with the optimum DPN step and brings about a significant increase in the achieved NBTI performance, shown in Figure 5(C). The key learning is the competing impact of nitridation and its location within the dielectric stack: combining the optimum DPN with an F-incorporating plasma step, reduces ΔN_P to poly/SiO_2 levels, with strong NBTI improvement.

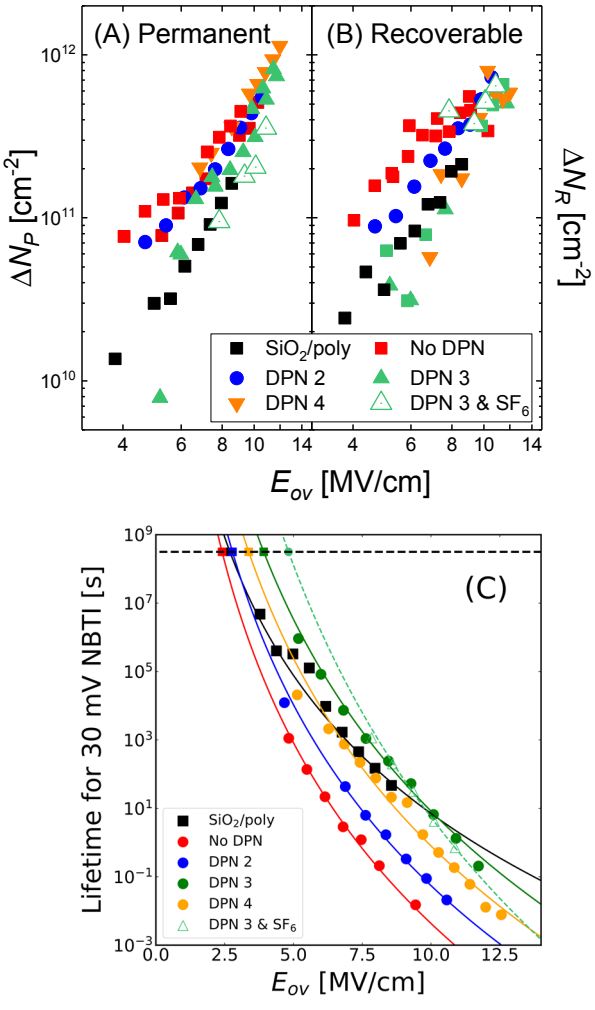

Figure 5. Universal Model fit results show (A) ΔN_P and (B) ΔN_R changes with E_{ov} as a function of DPN intensity, while (C) shows the estimated lifetime for 30 mV plotted against the effective field, E_{ov} (i.e. V_{ov}/EOT) for the samples. An optimum in NBTI robustness with DPN3, which is further enhanced by F incorporation is shown.

C. Impact of Nitrogen incorporation in the Metal Gate

1) Physical Analysis

TaN-gated high-voltage pFET stacks have been shown to demonstrate superior NBTI robustness to TiN-gated stacks [5]. In a bid to understand the rationale for this, EDS analysis was performed on TEM micrographs, which yields elemental profiling through the dielectric stack, as shown in Figure 6. Immediately clear from comparing the images for (A) TiN and (B) TaN electrodes is the increased thickness for the TaN case, and the lower Ta signal in the MG region, which is due to an overlap of signal between Tantalum and Silicon. However, a difference in Nitrogen in the metal gate is also clearly evident, with higher concentration for TiN gate. A difference in nitrogen profile throughout the gate-region, and interestingly, close to the channel (shaded areas in Figure 6) is noted.

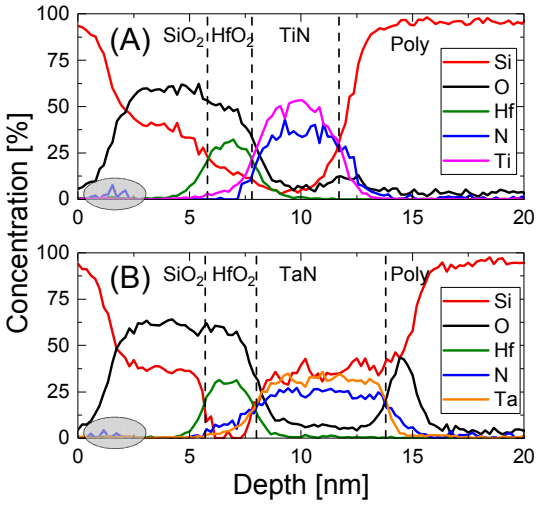

Figure 6. EDS signal from TEM measurements shows higher N content in SiO_2 for (A) TiN than (B) TaN-gated HKMG stacks.

2) NBTI characterisation

The role of the near-channel Nitrogen (Figure 6) on permanent and recoverable defect densities in the respective samples is shown in Figure 7. There is a clear increase in both ΔN_R and ΔN_P in the case of the TiN-gated samples, together with the bias dependence thereof (i.e. accessibility of these defects bands, represented as γ), with the TaN based samples showing similar defect densities to the SiO_2/poly reference. The observed differences in ΔN_P are consistent with the presence of defects resulting from N incorporation near the channel, the presence of which are demonstrated in Figure 6(A). These results corroborate the reduction in low-frequency noise for such samples [10].

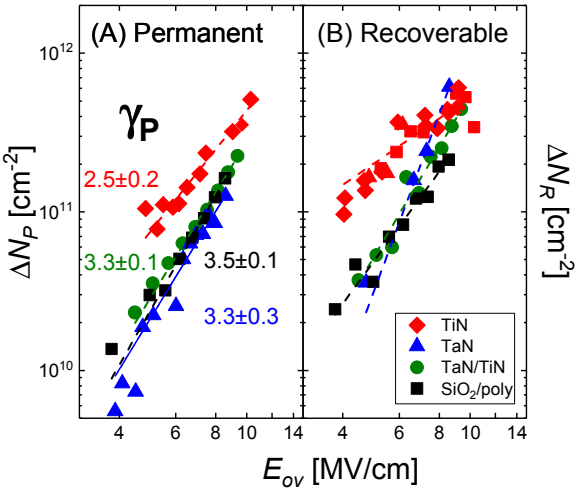

Figure 7. Permanent and Recoverable defect densities derived from Universal Model fitting of NBTI data for the gate-electrode options explored, reveal that TiN-gated stacks results in higher (A) ΔN_P and (B) ΔN_R, together with higher bias dependence for both defect types.

The differences in ΔN_R seen in Figure 7(B) on changing metal gate electrode are believed to be related to the absence of Ti diffusion in the TaN sample together with reduced N content, as seen in the DPN experiments of Figures 4 & 5(B). Strong diffusion of Ti has previously been reported for such structures, when subjected to the thermal budgets that are consistent with DRAM BEOL [2]. Unfortunately, this distinction cannot be quantified in the dielectric of the TaN-gated stack, due to the Si/Ta EDS signal overlap. The differences in defect profiles are consistent with V_t degradation kinetics, with higher time exponent, n, for (less-defective) TaN, shown in Figure 8.

Interestingly, utilising a 5 nm TaN-layer between the poly-contacting (5nm) TiN layer is sufficient to duplicate the TaN-trend, shown in Figures 7 and 8, suggesting this prevents the nitrogen and titanium diffusion towards the channel, and higher NBTI seen in the TiN-gate case. This combination also brings the added benefit of a more viable etch chemistry.

3) Modelling of measured NBTI characteristics

Relaxation of stress-induced threshold voltage degradation, as a function of stress time and field for TiN and TaN-gated samples are presented in Figure 9(A and B, respectively). The increase in ΔV_t at a given stress condition is evident for the TiN-gated sample, with marginal EOT reduction notwithstanding. The excellent fits obtained with Comphy for these datasets are shown in Figure 9, as solid lines. The extracted trap parameters, presented in Table 1, indicate an increase in N_{ot} (donor traps located 0.1-0.6 nm from Si/SiO_2 interface) for the TiN-gated sample, shown in Table 1. This defect band's contribution to NBTI is enhanced with the ~50 mV V_t increase for the TiN-gated stack, consistent with the differences in γshown in Figure 7(A).

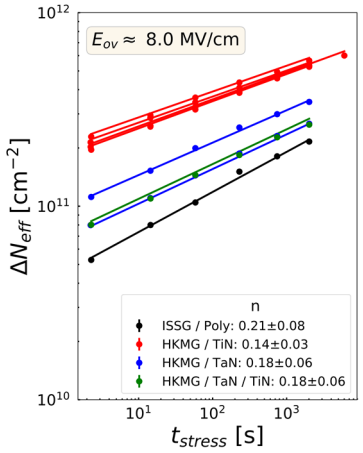

Figure 8. Defect generation kinetics as a function of gate electrode, showing higher ΔN_{eff} and lower time exponent for TiN based stacks, than TaN-based or poly/SiO_2 reference.

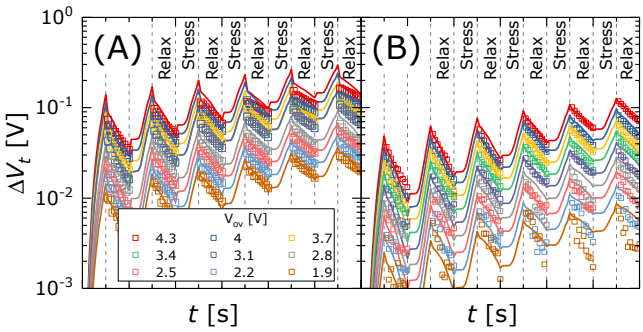

Figure 9. Measured ΔV_t-t data at varying V_{ov} (symbols), during consecutive stress (incrementing from ~2 to ~1000s) and relax (1ms-10s) cycles for (A) TiN and (B) TaN-gated stacks. Solid lines are Comphy fits of measured dataset. Each stress and relax step are plotted on their own individual log scale.

Table 1. Fit parameters derived from Comphy for TiN gate and TaN gate samples. The obtained fits are consistent with an increase in defect density in the TiN-gated sample.

	TiN	TaN
$\langle E_t \rangle \pm \sigma_{E_t}$ [eV]	-1.4 ± 0.24	-1.4 ± 0.21
N_{ot} [cm^{-3}]	1.4x10^{20}	8.0x10^{19}
$\langle S \rangle \pm \sigma_S$ [eV]	5.6 ± 2.7	5.6 ± 2.2
R	2.2	2.2

D. Impact of V_t tuning-capping layers on NBTI

1) Device characteristics

The impact of gate stack engineering on NBTI has been reported [e.g., 11] to enable significant improvements. In this work, AlO_x capping layers (between HK & MG), with or without an F plasma step are studied, with variations in the timing of F and AlO_x. Device characteristics are detailed in Figure 10. Drive current follows the expected 1/C_{ox} trendline, suggesting no additional mobility degradation. Incorporation of an AlO_x cap results in a significant V_t reduction (~180 mV). This V_t-tuning method has been applied for logic devices [12], and as shown here, is still applicable on 5 nm SiO_2 layers, together with HKMG. Its impact on device reliability is the focus of this section.

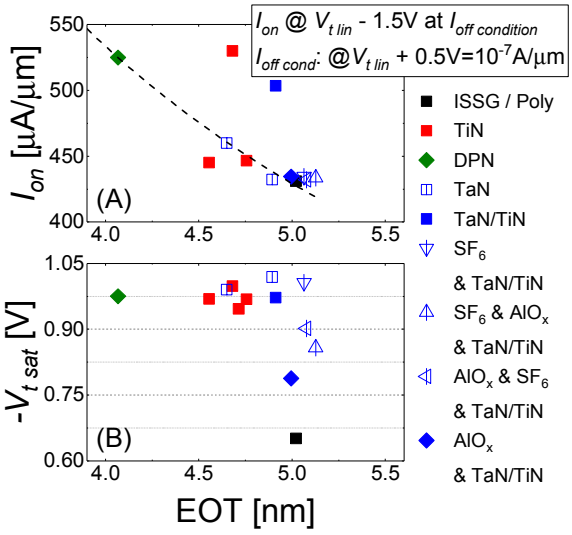

Figure 10. (A) I_{on} and (B) V_t-EOT trends for novel stacks HKMG explored, showing negligible impact on device performance, and strong V_t reduction on AlO_x incorporation.

2) Charge and effective workfunction characterisation

In this study, the impact of AlO_x cap, in combination with a TaN/TiN electrode are explored, and compared to samples which also had SF_6 treatment, either before or after the AlO_x deposition. CV measurements on *p*-Si enable similar substrate-hole injection mode as a *p*-channel MOSFET, and V_{fb} values obtained from CVC fitting, at multiple temperatures are plotted in Figure 11(A). At a given temperature, there is limited impact of the SF_6 process on V_{fb} or effective work-function, $\phi_{m\,eff}$, values, while the AlO_x incorporation results in ~170 mV increase. Interestingly, the presence of AlO_x in direct contact with the metal gate shows a higher V_{fb} shift than observed when an SF_6 step is performed *after* the AlO_x deposition. This suggests the dipole inducing the V_{fb} and V_t shifts is modified by F incorporation between the AlO_x and MG layers (shown in Figure 10(B)). The temperature dependence of V_{fb} was calculated from (3), and shown in Figure 11(A), where the Q_f term was calculated in the range 2-3 x10^{10} cm^{-2} for all samples. The calculated and measured trends follow the expected temperature dependence, implying no varying thermally-activated charge/interface-state component from the elements being added.

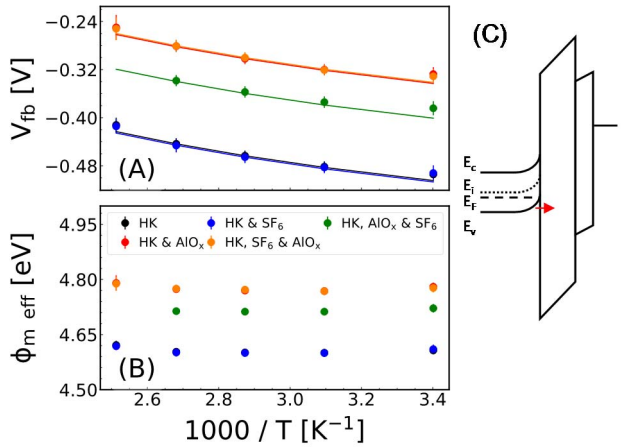

Figure 11. Results from Capacitance-Voltage measurements show (A) measured (symbol) and fitted (solid line) flat band voltage, V_{fb}, and (B) effective work-function, $\phi_{m\ eff}$, as a function of measurement temperature, while (C) shows the band alignment corresponding to the accumulation of the *p*-Si substrate.

3) *Reliability Characterisation*

The calculated electric filed overdrive voltage to withstand 30 mV NBTI after ten year operation for the samples considered are plotted in Figure 12, where an astonishing increase in NBTI robustness is achieved on addition of the AlO_x cap, with ~1 MV/cm E_{ov} increase (corresponding to ~500 mV V_{ov} increase) compared to the HKMG stack. Unlike the DPN case, this change is not related to a change in EOT (see Figure 10), but instead due to fundamental changes in the stack on AlO_x incorporation.

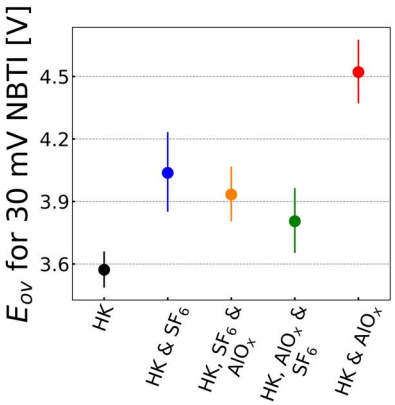

Figure 12. E_{ov} for 10-year NBTI lifetime at 30 mV degradation for TaN/TiN-electrode stacks examined, showing a significant increase on AlO_x incorporation into the pFET devices. Intermediate values are attained after SF_6, with or without AlO_x.

To understand the reasons behind this difference, Universal Model fitting, shown in Figure 13, reveals that ΔN_R does not change on AlO_x incorporation, whereas γ_P for permanent defects increases significantly, together with a reduction in ΔN_P at low values of electric field. This suggests a modification of access to the near-interface defect band results on incorporation of AlO_x into the stack. This trend is seen, to varying degrees, across all samples explored, and detailed in Figure14(A).

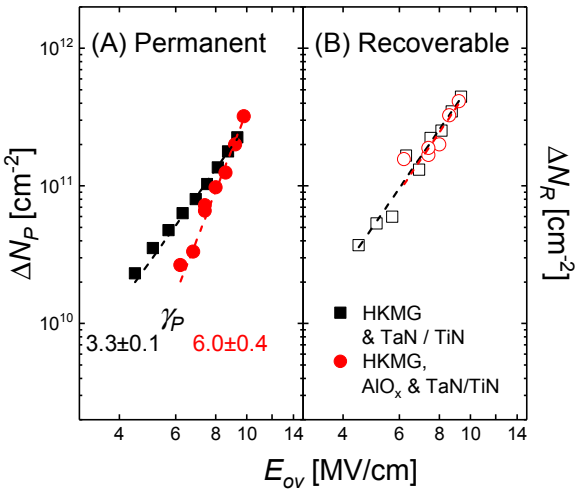

Figure 13. Impact of AlO_x cap on (A) ΔN_P and (B) ΔN_R for TaN/TiN-gated samples is limited to the permanent defect contribution, which shows lower density and higher bias dependence.

This modification of access to defects responsible for the permanent degradation correlates with the AlO_x induced V_t shift, as seen in Figure 14(B). Comphy fitting of measured datasets was performed, and it is seen that the energy level of the donor trap band near to the channel is modified on AlO_x incorporation, also displayed in Figure 14(C). Incorporation of AlO_x reduces V_t, limits band-bending and accessibility of the donor trap band, while reducing the energy level of the defect band. These concomitant effects enable the BTI improvements observed in this work.

E. *Summary of NBTI study for High Voltage Applications*

An overview of all results achieved in our study of the NBTI reliability for high voltage logic for memory device applications are presented in Figure 15, where the overdrive for 10 year NBTI lifetime @ 30 mV ΔV_t degradation is plotted against the equivalent oxide thickness. Some datapoints displayed have previously been reported [2, 5], but are included again to summarise the current status of research on this topic. Also included for benchmarking are datapoints from [13], where results on ultra-thin oxide layers were reported.

Immediately clear from the figure is the impact of metal gate electrode, with systematically higher values for TaN gate than TiN gate across all process variations explored. For a given gate electrode, significant improvements in BTI robustness can be achieved, at similar EOT, by incorporation of AlO_x, Fluorine. For TaN and TiN gate electrodes, these reliability improvements are cumulative. The impact of DPN yields

significant improvement in NBTI robustness, at reduced thickness, which is also cumulative with F and AlO_x induced effects, whereby the E_{ov} achieved can be quite high, and best results are comparable to the AlO_x cap with TaN/TiN gate electrode, which shows $E_{ov} > 4$ MV/cm NBTI robustness.

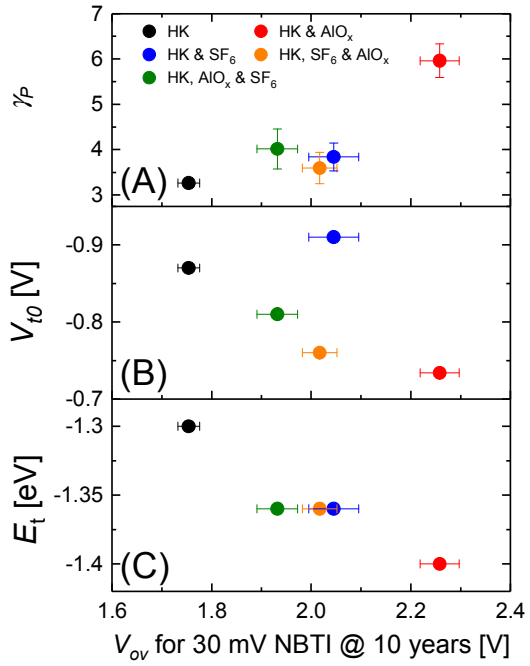

Figure 14. V_{ov} for 30 mV NBTI degradation observed on AlO_x / SF_6 incorporation of TaN/TiN-gate stacks correlates with (A) accessibility to near-interface permanent defect band, γ_p, from Universal Model fitting, (B) initial V_t, and (C) donor-band defect trap energy level, with respect to E_{F_i} silicon, derived from Comphy

IV. Conclusions

To continue the evolution of memory device scaling, incorporation of high-κ metal gate constituents in the logic peripheral devices will become a requirement. To facilitate a single gate stack across the peripheral region, adjacent high voltage devices will also have this HKMG incorporated, albeit on a thicker oxide layer. The impact of this on device reliability is significant, with the enhanced BEOL thermal budgets enabling diffusion of materials from the high-κ and metal gate towards the channel, and significantly degrading NBTI.

In this work, we demonstrate some gate stack combinations which limit this diffusion and reveal promising NBTI characteristics. These are achieved by varying the choice of metal gate electrode, controlling the Nitrogen content within the stack, incorporation of AlO_x cap layers, and F incorporation. These processing options playing roles in modifying the defect densities present, together with the access to those near-channel defect bands which can also be tuned, and consequently promising dielectric stack options for such applications are reported.

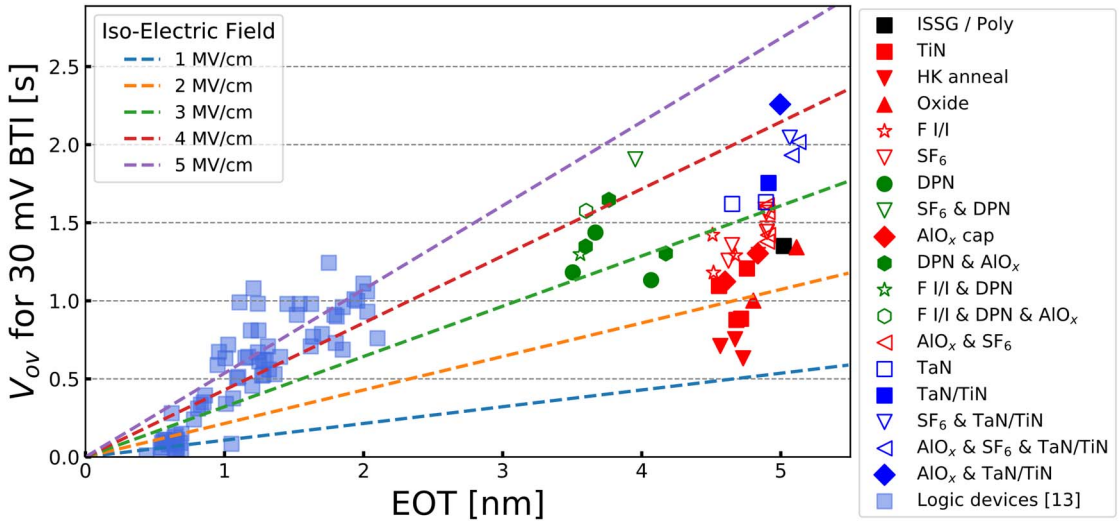

Figure 15. Overview of updated V_{ov}-EOT trends for NBTI degradation on HV memory peripheral transistors. Significant differences in V_{ov} are attained, at EOT ~4.5nm with gate stack engineering. TiN-gated stacks (red symbols) show lower robustness, but yet significant dependence on stack engineering. TaN based stacks (blue symbols) show similar stack-impact, together with higher V_{ov} values for the reasons detailed above. The DPN-based (TiN-gated, green symbols) stacks show reasonable V_{ov} increase, at lower EOT. Best NBTI performance was obtained with F incorporated and/or AlO_x-capped stacks with TaN/TiN electrode (or DPN-processed TiN gate), which can survive 10 year stressing at $E_{ov} > 4$ MV/cm.

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