Low Cost and High Performance Radiation Hardened Latch Design for Reliable Circuits

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***Abstract*—With decreasing device dimension, the susceptibility of transistors and circuits to external noise sources increase especially in radiative environments. In this work, a radiation hardened latch based on NMOS only Schmitt trigger with voltage booster (NST-VB) is proposed. We first analyze the critical charge at the internal nodes of different latch designs to identify the most sensitive node. By doing so our results reveal that the proposed circuits show highest robustness to single event transients, compared to reference designs. Furthermore, the results show that the critical charge decreases with temperature and increases for higher supply voltages, and it is further observed that the critical charge decrement with temperature variation, exhibiting best performance for the NST-VB based latch compared to others circuits. For the validation of proposed latch, a figure of merit, i.e. the charge to power delay area product ratio (QPAR), considering the most important performance parameters is calculated. We clearly observe that the proposed latch exhibits significantly enhanced performance as compared to existing designs.**

***Index Terms*—Transient faults, soft errors, single event transient, radiation hardened latch, robust design.**

I. Introduction

With the availability of highly optimized and only a few of tens of nanometer small transistors, the performance of integrated circuits (ICs) gets significantly improved. However, with this enhancement reliability issues of complex ICs become a more serious concern for the researchers and developers. Due to the scaling of the circuit's supply voltage and node capacitance, the amount of charge stored at a single node gets also reduced, which makes circuits more susceptible to the external noise, like strikes from neutrons or alpha particles originating from terrestrial environment [1]. When such particles strike at a sensitive node of a logic circuit, they can generate secondary carriers which can get collected by the source/drain regions of a single transistor and lead to a glitch. Such kind of erroneous behavior is typically referred to as transient fault (TF) [2]. Within a circuit, particle strikes may appear as an electrical pulse, i.e. single event transient (SET), which may propagate through combinational logic paths if not properly masked. SETs may be harmful to the operation for sequential elements like latches and flip-flops, and give rise to unwanted changes of logic states. This can happen if particle hits cause an increase of the charge stored at a certain node which then exceeds the critical charge, which is referred to as single event upset (SEU) [3].

The schematic of a conventional unhardened latch is shown in Fig. 1 as is used as reference latch in this work. In order to maximize the soft error tolerance for such logic circuits several methods have been proposed. For instance, the introduction of a Sin-LC hardened latch [4] provides a strong protection of internal nodes, but fails to protect the output nodes of the latched data from to radiation effects. To overcome this a Schmitt trigger (ST) based hardened latch design has been proposed [5], as shown in Fig. 2. The authors introduce a ST inverter in order to protect the internal nodes against TF, with the drawback that the circuit delay increases due to the hysteresis effect of the ST inverter. As according to [4] the internal nodes of the circuit are more susceptible to soft errors compared to the other nodes we focus on the analysis of the soft error susceptibility considering the internal nodes (N1, N2, and NQ) only.

To further enhance the ST based solution with respect to bias temperature instabilities we recently proposed a new NMOS only Schmitt trigger with voltage booster (NST-VB) [6] based radiation hardened inverter by employing the 32nm PTM technology model [7] using HSPICE [8]. For

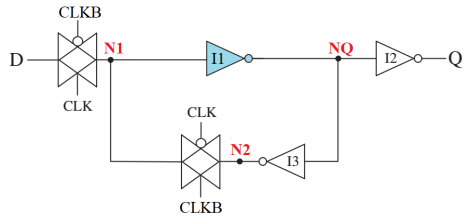


Fig. 1. Schematic of a conventional unhardened latch used in this work. The node N1, N2, and NQ are the internal nodes, the nodes D and Q are the input and output of the latch, respectively, and CLK and CLKB are the system clock. The circuit elements I1, I2, and I3 are CMOS inverters.

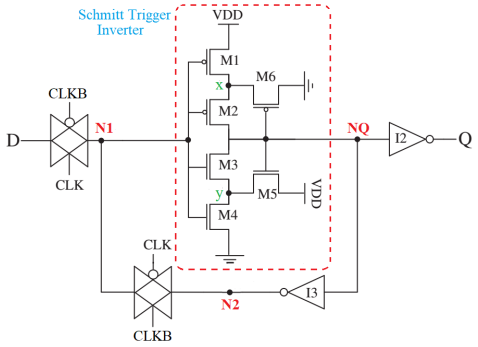


Fig. 2. Schematic of Schmitt trigger based hardened latch.

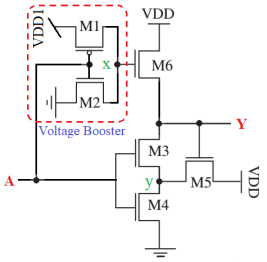


Fig. 3. Schematic of NMOS only Schmitt trigger with voltage booster (NST-VB) based inverter. The voltage booster is the CMOS inverter with $V_{\rm th}$ higher supply voltage ($V_{\rm DD1}$ = $V_{\rm DD}$ + $V_{\rm th,n}$).

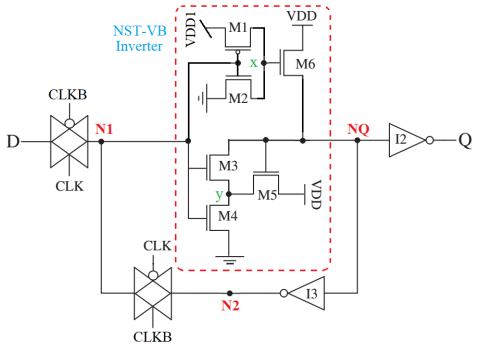


Fig. 4. Schematic of proposed NST-VB based hardened latch.

comparison, we replace inverter I1 with the NST-VB inverter as I1 is replaced by the ST inverter in [5]. Afterwards extensive simulations are performed and the results are discussed compared the recently proposed design. Further, most sensitive nodes, temperature variation and supply variation in terms of critical charge ($Q_{\rm crit}$) are analyzed for all the considered latches.

II. NST-VB Based Latch

As previously mentioned, we propose to replace the inverter I1 with an NMOS only Schmitt trigger with a voltage booster (NST-VB) based inverter in order to further improve radiation hardening of the latch.

A. NST-VB Circuit

The main attribute of this circuit is the use of only NMOS transistors in the critical path. This can be achieved by replacing the PMOS transistors from PUN (M1, M2 and M6 from Fig. 2) of ST with an NMOS counterpart. The schematic of the achieved NST-VB is shown in Fig. 3 and consists of a combination of a ST and an NMOS inverter. If one would only modify the inverter the performance improvement would not be as high as achieved for the NST-VB circuit due to the small noise margin, reduced maximum output voltage ($V_{\rm DD} - V_{\rm th,n}$), and short circuit current from $V_{\rm DD}$ to ground caused by the NMOS inverter. The latter exists when PDN is turned ON since PUN is always in the ON state in NMOS inverter. To overcome those weaknesses a voltage booster (VB) is added, as visible in Fig. 3. The VB is especially advantageous to overcome the direct current problem and also to increase the output voltage swing. In addition to enhance the full voltage swing the supply voltage of the voltage booster is chosen to be about $V_{\rm th,n}$ larger than the power supply of the circuit.

If we consider the circuit from Fig. 3 from the radiation hardening perspective, the situation now is different from the CMOS and ST inverter. As only NMOS transistors drive the output of the NST-VB circuit the only critical condition that we need to consider is when its input is logic 0, and the output is logic 1. In this case, the only sensitive region is the drain junction of the transistor M3, where a high energetic particle hit could induce a negative glitch at the inverter output. In the opposite case when the input is logic 1 and the output is logic 0 the transistors M4 and M3 are in the ON state, whereas transistor M6 is in the OFF state. If now a SET occurs at node x, a glitch could turn ON transistor M6 and gets so propagated to the output of the circuit. But in this case a large amplitude of the SET is required to generate the glitch at the output, because due to the feedback controlled pull-down network the glitch recovers very fast and suppresses a SET at the circuit output. In this case, the only potential sensitive region is the drain junction of M6. However, there is no electric field in this region which could split the generated electron-hole pairs and produce a net charge that alters the output voltage. The voltage drop across this junction is negligible as the drain and substrate are held at ground potential.

B. NST-VB based Latch

Fig. 4 shows the proposed NST-VB inverter based radiation hardened latch. We place an NST-VB inverter in the transparent path of the latch to improve the radiation hardening as previously discussed. For further radiation hardening improvement it would be conceivable that one replaces all three inverters with the NST-VB inverter. However, this would increase the circuit complexity. For the latch, in case of CLK is logic 0 the circuit will be in the latch mode and when CLK is logic 1 the circuit will be transparent mode. As the effect of radiation is more severe during latch mode [5], all the analysis have been performed considering latch mode to keep the circuit complexity as low as possible.

III. Evaluation and Comparison of Latch

To study the performance of circuits considering radiation hardened design, we use the PTM 32nm CMOS node [7]. All the simulations are performed using HSPICE [8] considering a supply voltage of $V_{\rm DD}$ = 0.9V and the operating temperature is set to room temperature $T = 25°$C.

A. Radiation Hardening Analysis Methodology

To inject SEU into the simulations, the current induced by α-particle strikes is modeled by an additional double exponential current source [9] specified by

$$I_{\rm inj}(t) = I_{\rm peak} \times (e^{-t/\tau_f} - e^{-t/\tau_r}) \qquad (1)$$

where $I_{\rm peak}$ is the peak value of the injected current injected at the respective sensitive node. The parameters τ_f and τ_r are

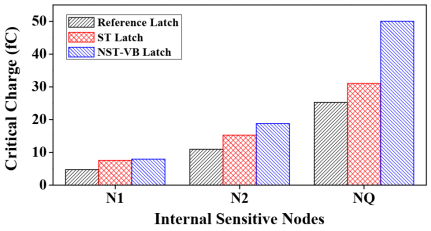
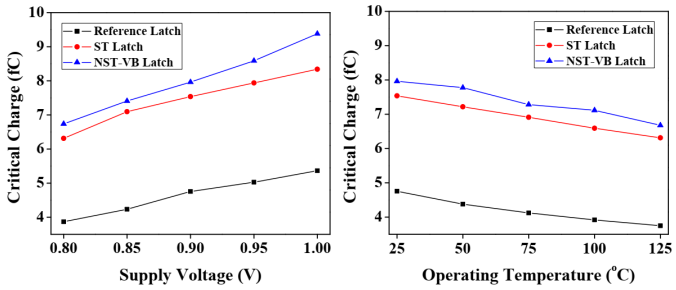


Fig. 5. Critical charge at the internal nodes of the different latches.



(a) (b)

Fig. 6. Critical charge at the most sensitive node N1 of different latches for (a) different supply voltages at room temperature $T = 25°$C and (b) different operating temperatures at $V_{\rm DD} = 0.9$V.

material dependent time constants. In our simulations we use τ_r = 1ps and τ_f = 50ps according to [10].

After injecting the strike-equivalent current peak at the sensitive node of the circuit the critical charge $Q_{\rm crit}$ is calculated. For this we determine the minimum magnitude and duration of injected current pulse that is required to flip the state of a logic output. In that way $Q_{\rm crit}$ is determined by integrating over the current pulse for the time interval $t = 0$ to $t = T_{\rm crit}$, leading to the critical charge

$$Q_{\rm crit} = \int_0^{T_{\rm crit}} I_{\rm inj}(t)dt \tag{2}$$

where $I_{\rm inj}(t)$ is the injected current pulse at sensitive node considered for the SEU analysis.

B. Critical Charge Analysis

At the begin we estimate the critical charge at all the internal sensitive nodes N1, N2, and NQ for reference latch, ST latch, and proposed NST-VB latch as shown in Fig. 5. Our results show that the node N1 has the smallest critical charge for all the considered latches. The critical charge at node N1 is roughly about a factor of two lower than compared to the extracted critical charge at node N2 for all three cases. Similarly, the critical charge at node N1 is also lower as compared to critical charge at node NQ (5.31×, 4.12×, and 6.28× for all three cases). As node N1 exhibits the smallest critical charge for all considered latches, node N1 is maximum sensitive to the soft error. For this we look at node N1 more precisely in our analysis.

Also the impact of process voltage, and temperature (PVT) variations on the soft error tolerance is an important measure for stable circuit operation. The effect of supply voltage and temperature variations on the critical charge of node N1 is shown in Fig. 6. Fig. 6(a) shows the evolution of the critical charge with supply voltage variation in the range of 0.8V to 1V for the considered circuits. The results demonstrate that the critical charge increases with the supply voltage as node capacitance increases with supply voltage. It is also observed that the critical charge for proposed NST-VB based latch is higher as compared to the two other cases indicating that the proposed NST-VB based latch is more hardened to soft errors caused by supply variations. Fig. 6(b) shows the trend of the critical charge with the temperature ranges from $T = 25°$C to $T = 125°$C. The result shows that with the increasing temperature, the critical charge decreases because the device carrier mobility decreases. It can be further observed that the absolute decreases of the critical charge of the NST-VB based latch shows the smallest value of 16.11%. This indicates that the critical charge of the proposed NST-VB based latch is less sensitive to the temperature variations than for the two other circuits emphasizing the increased robustness to the soft errors of the proposed NST-VB based latch.

C. Timing and Delay

Fig. 7 shows the transient response and the timing diagram of the NST-VB based latch. The signals CLK and CLKB are the system clocks, D is the data input, and Q is the data output, and N1, N2, and NQ are the internal sensitive nodes. The parameters $t_{\rm CLK-Q}$ and $t_{\rm D-Q}$ are the propagation delay of the latch from CLK to output Q and data input D to output Q, respectively. The value for $t_{\rm setup}$ is the minimum time between a change in the data signal D and the trailing edge of the CLK in a way that the new value of D can propagate to the output Q of the latch [5]. The total latch propagation delay further is

$$t_{\rm delay} = t_{\rm setup} + t_{\rm CLK-Q}. \tag{3}$$

The various timing and delay components for all the considered latches are summarized in Table I. Results show that $t_{\rm delay}$ for the NST-VB based latch is higher as $t_{\rm CLK-Q}$ is larger than for the reference circuit. The increase in $t_{\rm CLK-Q}$ for NST-VB latch is because of the absence of feedback connection in the pull-up network of NST-VB inverter whereas the ST inverter has this feedback connection in both pull-up

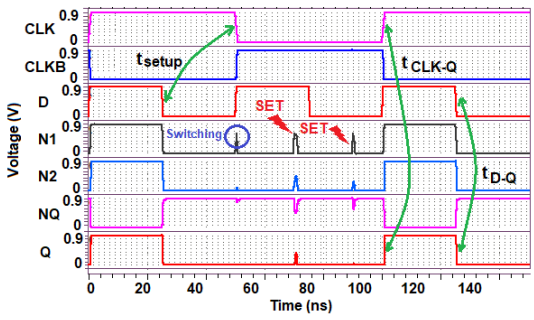


Fig. 7. Transient response and timing diagram of the NST-VB based latch.

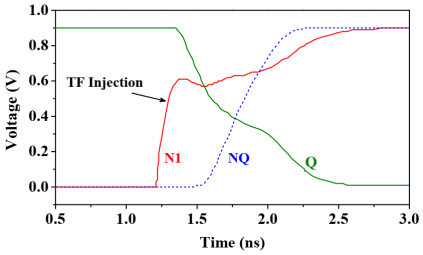


Fig. 8. Characteristics of the transient fault injection at the sensitive node N1 of the proposed NST-VB based latch.

TABLE I
PERFORMANCE COMPARISON OF DIFFERENT LATCHES

Performance Parameters	Latch		
	Reference	ST	NST-VB
Critical Charge (fC)	4.755	7.539	7.961
Dynamic Power (μW)	6.425	5.978	0.141
t_{setup} (ns)	0.750	0.750	0.750
$t_{\mathrm{CLK-Q}}$ (ns)	0.166	0.201	0.387
$t_{\mathrm{D-Q}}$ (ns)	0.279	0.844	0.186
t_{delay} (ns)	0.916	0.951	1.137
Area (μm^2)	15.360	24.576	22.534
PDP (fJ)	5.885	5.686	0.160
QPAR	0.053	0.054	2.210

and pull-down networks, which provides the fast transitions. However, $t_{\mathrm{D-Q}}$ for the proposed NST-VB latch shows the lowest value. Fig. 8 shows the transient fault injection at the most sensitive node N1 of the proposed NST-VB based latch. As can be seen, the proposed NST-VB latch requires a higher value of transient fault injection charge (7.961 fC) to flip the stored logic in the latch.

D. Circuit Area and Power Delay Product

Table I shows the comparison of the circuit area and power delay product (PDP) of different latches. Even though the number of transistors in the NST-VB inverter is the same as ST based inverter, the latch requires less area as compared to ST based latch. The largest chip area is required for the ST based latch compared to NST-VB based latch because ST inverter requires a large size transistor to get the same characteristics as for the NST-VB inverter. Further, we evaluate the PDP for different latch designs and observe that the PDP for proposed NST-VB based latch is minimum compared to the other two designs. The lower dynamic power of the NST-VB based latch is responsible for reducing the PDP.

E. Charge to PDAP Ratio

An increase in critical charge can be achieved by increasing critical node capacitance. However, this may require large transistor geometry, and thus would increase the area overhead. Slightly increasing the supply voltage also increases the critical charge, but also increases the power dissipation. To account for all the above factors, a new performance metrics considering critical charge, PDP, and area can be introduced. This metric is referred to as charge to PDAP ratio (QPAR) [5] and given by

$$\mathrm{QPAR} = \frac{\text{Critical Charge}}{\text{Power} \times \text{Delay} \times \text{Area}}. \tag{4}$$

A larger value of QPAR leads to a higher soft error tolerance, low power consumption, and high performance of the latch. From Table I, the QPAR of the proposed NST-VB based latch is higher as compared to reference latch and ST based latch which clearly underlines the advantages of the proposed NST-VB based latch circuit.

IV. Conclusion

In this paper, we propose a new NST-VB based radiation hardened latch. The NST-VB based latch shows improved performance and significantly enhanced radiation hardening as compared to existing latch circuits. Furthermore, the proposed latch is cost effective due to the low required chip area, low power dissipation, and higher critical charge at the most sensitive node of the latch. For validation of proposed latch considering a large set of performance parameters, a figure of merit called QPAR is analyzed, and we clearly observe that the proposed latch exhibits enhanced performance as compared to existing designs. Due to its better radiation hardening, the latch is suitable for the applications where the effect of external radiation is crucial for its applications, for instance in space environment, i.e. electronic circuits for aircrafts.

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