I1-1: Spin-based Electronics: Recent Developments and Trends

Viktor Sverdlov

Christian Doppler Laboratory for Nonvolatile Magnetoresistive Memory and Logic
Institute for Microelectronics, TU Wien, Gusshausstr. 27-29, 1040 Vienna, Austria
E-Mail: Sverdlov@iue.tuwien.ac

Continuous miniaturization of semiconductor devices is the key driving force ensuring breathtaking increase of performance of modern integrated circuits. With chips based on 5nm technology approaching production, the semiconductor industry is focusing on the 3nm technology node [1]. To sustain the growing demand for high performance small area CPUs and high-capacity memory, an introduction of a disruptive technology employing conceptually new computing principles becomes paramount. At the same time, the critically high power consumption becomes incompatible with the global demands of sustaining and accelerating the vital industrial growth, prompting an introduction of new solutions for energy efficient computations. An attractive path to dramatically reduce the power consumption and eliminate leakages in modern integrated circuits is to introduce non-volatility. Magnetic tunnel junctions (MTJs) with large magnetoresistance ratio are perfectly suited as key elements of nonvolatile CMOS-compatible magnetoresistive embedded memory. MTJs possess a simple structure and are characterized by long retention time. A MTJ is a sandwich made of two ferromagnetic layers separated by a thin tunnel barrier. The information can be encoded into two relative magnetization states with parallel (P) or anti-parallel (AP) orientations. Due to the tunneling magnetoresistance effect the resistances of the two states are different and the information can be sensed. The relative configuration of the two layers can switch by means of the spin transfer torque (STT) due to the current passing through the structure. All major FABs claimed to begin production of embedded STT MRAM production in the near future, with the most recent report from Intel [2].

To further reduce the energy consumption, it is essential to replace static RAM in modern hierarchical multi-level processor memory caches with a non-volatile memory. Although STT-MRAM can in principle be used in L3 cache [3], the switching current floating through the tunneling oxide becomes very large at an access time of 5ns and faster. This prevents STT-MRAM from entering in L2 and L1 caches currently mastered by static RAM (SRAM). Three-terminal spin-orbit torque (SOT) MRAM is an electrically addressable non-volatile memory combining high speed, high endurance, and long retention. Recently, IMEC presented a technology to integrate SOT-MRAM on a 300mm CMOS wafer using CMOS compatible processes [18]. For SOT-induced deterministic switching of a perpendicular free magnetic layer a static magnetic field is required. A scheme employing the two orthogonal current pulses is suitable for achieving the sub-ns deterministic switching without an external magnetic field [5].

The electron spin offers an additional functionality to digital switches based on field effect transistors. SpinFETs and SpinMOSFETs are promising devices, with the nonvolatility introduced through the relative magnetization orientation between the ferromagnetic source and drain. Several fundamental problems including spin injection from a metal ferromagnets to a semiconductor, spin propagation and relaxation, as well as spin manipulation by the gate voltage were resolved in order to demonstrate such devices. However, boosting the spin injection efficiency as well as increasing efficient electrical spin control represents the challenges to be resolved before these devices appear on the market.

The introduction of non-volatility to data processing offers outstanding advantages over standard CMOS-based computing. This paves the way for a new low power and high-performance computation paradigm based on logic-in-memory and in-memory computing architectures, where the same nonvolatile elements are used to store and to process the information.

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3. S. Sakhare et al., “Enablement of STT-MRAM as Last Level Cache for the High Performance Computing Domain at the 5nm Node”, IEDM Proc., pp.420-423, Dec. 2018.
4. K.Garello et al., “SOT-MRAM 300mm Integration for Low Power and Ultrafast Embedded Memories”, VLSI Technology and Circuits, 2018, p.C8-2, 2018.
5. V. Sverdlov et al., “Two-pulse Sub-ns Switching Scheme for Advanced Spin-Orbit Torque MRAM”, Solid-State Electron., DOI: 10.1016/j.sse.2019.03.010, in press, 2019.