Distribution Function Based Simulations of Hot-Carrier Degradation in Nanowire FETs

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***Abstract*—Hot-carrier degradation (HCD) is again becoming a growing VLSI reliability problem. This work reports hot-carrier simulations for Si nanowire field-effect transistors (NW FETs) based on the carrier energy distribution function (DF) and compares the results to measured data. The importance of impact ionization for HCD simulations is discussed. A 1-to-1 relation between the extent of interface defects generated by hot-carriers in the channel and the degradation of several FET parameters is observed.**

***Index Terms*—hot-carrier degradation, nanowire FETs, carrier energy distribution function, interface defects, TCAD**

I. Introduction

Continued transistor scaling at approximately constant supply voltage leads to increased hot-carrier degradation (HCD) in the latest CMOS technologies [1], [2]. HCD is mainly caused by the breakage of Si-H bonds at the Si-SiO_2 interface. A single incident carrier with sufficient energy can break the bond through the so-called single vibrational excitation (SVE) mechanism. Alternatively, bond breakage can occur by multiple carriers which individually have insufficient energy to break the bond. In that case, the carriers induce vibrational excitations of the bond and increase its energy. This lowers the potential barrier for the bond rupture reaction, which allows a less energetic carrier to break the bond [3]. The latter process is called the multi vibrational excitation (MVE) mechanism.

Because of the interaction between SVE and MVE mechanisms, knowledge of the carrier energy distribution function (DF) is required to accurately model HCD. DF-based simulations have been done for HCD in planar FETs [4]–[6], finFETs [7] and high-voltage devices [8] before. However, for NW FETs, only HCD data were reported so far and modeling efforts have been limited to known empirical models [9], [10], sometimes supplemented with (non DF-based) simulations to understand qualitative trends [11]. This work focusses on modeling HCD of NW FETs using simulations of the DF and quantitatively compares the results to measurements. To the best of the authors' knowledge, this is the first report of such a study.

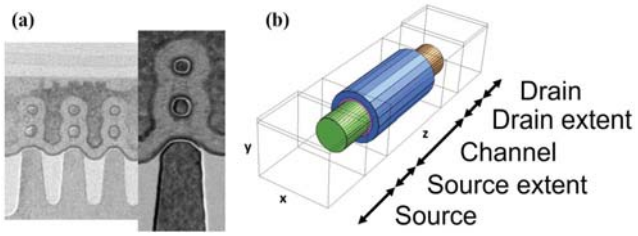

Fig. 1. (a) TEM cross-section and (b) the simulated structure of the nanowire FET. The nanowire diameter is $\sim$ 9 nm. Only 1 nanowire (of 8) is simulated.

II. Methodology

Si nMOS NW FETs consisting of 8 wires with a gate length of 28 nm and a diameter of 9 nm were used in this work (Fig. 1a). The fabrication [12], [13] and hot-carrier measurements [9] of these devices were reported before. A reverse-engineered 3D simulation structure with 1 NW was made (Fig. 1b). The time-0 threshold voltage and subthreshold slope were calibrated by adjusting the doping profiles in the device and comparing the output of drift-diffusion simulations in Minimos-NT [14] with the measurements (Fig. 2), similar to Bufler *et al.* [15]. Calculation of the I-V curves by solving the subband Boltzmann Transport Equation (BTE) gives the same subthreshold slope and threshold voltage as by solving the drift-diffusion equations (Fig. 2a), except for a difference in gate work function of 30 meV.

The electron DF is obtained by solving the subband BTE for the NW FETs in the channel and in the source/drain extension regions using GTS NDS [16], [17]. Phonon, ionized impurity and surface roughness scattering are considered in the calculation of the DF, but impact-ionization (I/I) and electron-electron scattering are presently not. Quantum effects are captured by solving the coupled Schrödinger-Poisson equations in the planes perpendicular to the transport direction. In position (z) - wave vector (k) space, a 'high probability stream' towards increasing positive momenta p ($p = \hbar k$) is visible in the DF for increasing z values (Fig. 3a). This represents the movement of electrons from the source to the drain. Scattering in the device

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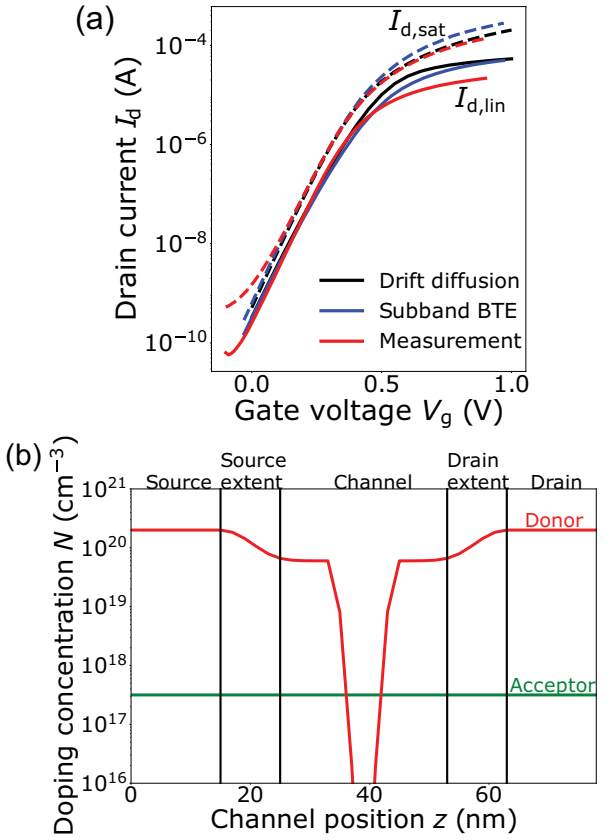

Fig. 2. (a) Time-0 calibration of the nanowire I-V curves using the drift-diffusion simulation scheme (black curves) and the subband BTE simulation scheme (blue curves). The 2 schemes give a difference in gate work function of 30 meV. (b) Reverse-engineered doping profiles obtained after the calibration.

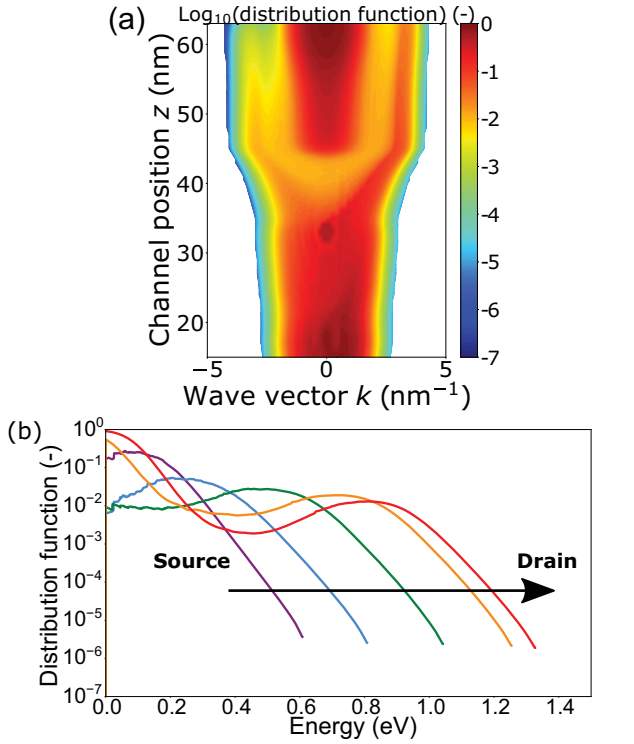

Fig. 3. (a) Distribution function in position (z) - wave vector (k) space for V_g = 1.9 V, V_d = 1 V. (b) Distribution functions at varying channel positions for the same bias condition as in (a).

leads to the development of a second, smaller stream towards negative momenta. When viewed as a function of energy, the tail of the DF moves to higher energies when going from source to drain (Fig. 3b).

From the DF, the stress-induced density of interface defects (broken Si-H bonds) is obtained, similarly as was done by Bina *et al.* [5]. The vibrational states of the Si-H bonds are modeled using a truncated harmonic oscillator potential with a total bond breakage energy of 2.25 eV and a 0.25 eV distance between the vibrational levels [18]. We consider all superpositions of the MVE and SVE processes, i.e. dissociation of the bond is possible from every level. The device with interface defects is then simulated again to extract the degradation ($\Delta V_{\rm th}$, $\Delta I_{\rm d,lin}$, $\Delta I_{\rm d,sat}$, $\Delta I_{\rm d,sat,rev}$). Post-stress I-Vs were obtained by solving the drift-diffusion equations.

Pre-existing bulk oxide defects in the HfO_2 were included in the simulations to model the bias temperature instability component in the measurements. These oxide defects are located 3.82 eV above the valence band edge with a fixed concentration of 2.9 x 10^{20} cm^{-3} (cfr. Rzepa *et al.* [19]). The oxide defect occupancy was calibrated to the measured data for every V_g at V_d = 0.1 V and further assumed independent of V_d in the (V_g,V_d) bias space.

Simulations were done for T = 125 °C and t = 530 s, corresponding to the measurements in [9]. The sense drain voltages in the linear and saturation region were 0.05 V and 0.9 V respectively.

III. Results and Discussion

The degradation of several FET parameters ($V_{\rm th}$, $I_{\rm d,lin}$, $I_{\rm d,sat}$, $I_{\rm d,sat,rev}$) was simulated over the entire (V_g,V_d) bias space. A uniform density of states $g(\epsilon)$ as function of energy ϵ was assumed for the interface defects such that $g(\epsilon) = g_0 =$ constant for $\epsilon_{\rm min} < \epsilon < \epsilon_{\rm max}$ and $g(\epsilon) = 0$ otherwise. By varying the energy positions $\epsilon_{\rm min}$ and $\epsilon_{\rm max}$, the simulated degradation was matched to the measured one. Reasonable agreement between both could be obtained for $V_d < V_g$ (Figs. 4 - 7). This best fit required placing the defects over the energy range [$\epsilon_{\rm min} = \epsilon_v + 0.11$ eV, $\epsilon_{\rm max} = \epsilon_v + 1.21$ eV], with ϵ_v being the Si valence band edge.

For $V_d > V_g$, the simulations do not reproduce the measured degradation. For some (V_g,V_d) points in this area, degradation is completely missing in the simulations (Fig. 8, white shaded area, compare with Fig. 3 in [9]), while for other points the simulated degradation is too low. We speculate that the discrepancy is due to the absence of I/I in the simulations. In the cases without agreement, defects are created at the drain side in the simulations, but they do not extend deep enough into the channel to cause the (larger) measured degradation. With I/I, the generated holes would travel toward the source,

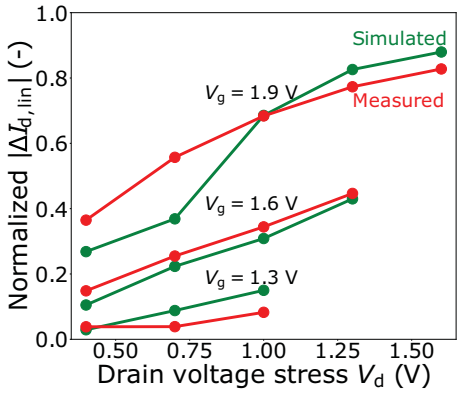

Fig. 4. Comparison of the simulated with the measured degradation of linear drain current for $V_d < V_g$.

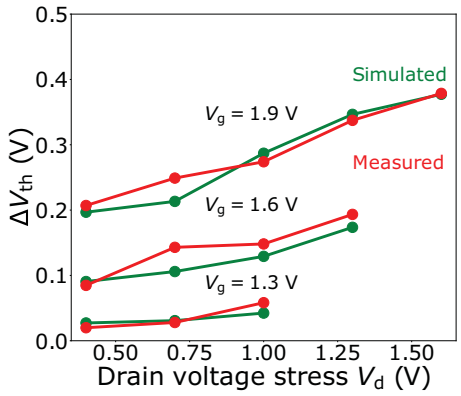

Fig. 5. Comparison of the simulated with the measured degradation of threshold voltage for $V_d < V_g$.

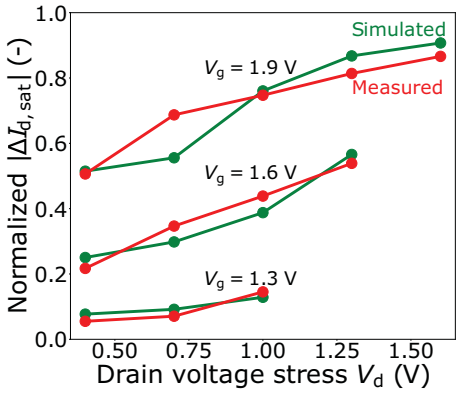

Fig. 6. Comparison of the simulated with the measured degradation of saturation drain current for $V_d < V_g$.

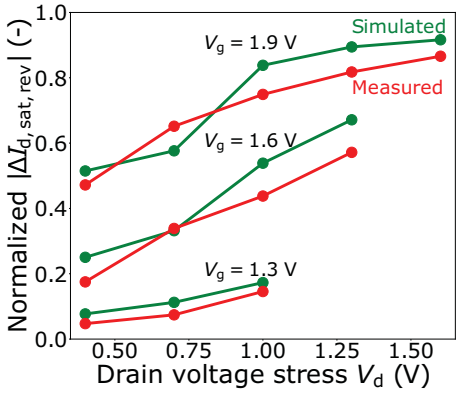

Fig. 7. Comparison of the simulated with the measured degradation of saturation reverse drain current for $V_d < V_g$.

gaining energy in this process and creating defects deeper in the channel, as suggested by Tyaginov *et al.* [20].

For the simulated bias points showing agreement with the measurements ($V_d < V_g$), a defect front is seen to propagate from the drain towards the source with increasing time (Fig. 9), a behavior which is quite common for HCD. The extent of defects in the channel can be quantified by choosing a threshold value for the defect density (here $N_{it,th} = 10^{12}$ cm^{-2}) and looking for the position z^* along the channel, starting from the source, where the defect density first crosses this threshold value (Fig. 9). When plotting the degradation of the linear drain current (contribution by interface defects only) versus z^*, the different stress biases for different stress times fall on a single curve (Fig. 10). The same is observed for the three other FET parameters (ΔV_{th}, $\Delta I_{d,sat}$, $\Delta I_{d,sat,rev}$, not shown). Quantifying the extent of interface defects by integrating the defect density profile over the position z and dividing this integral by the saturation defect density gives the same result (not shown). This implies that there is a unique 1-to-1 relation between the FET degradation and the extent of interface defects in the channel.

IV. Conclusions

Simulations of HCD based on the carrier energy DF were carried out for NW FETs and compared to measurements. Reasonable agreement between both was obtained for $V_d < V_g$. The importance of I/I in the description of HCD was discussed. A 1-to-1 relation between the extent of interface defects in the channel and the degradation of FET parameters was found.

Acknowledgment

Michiel Vandemaele is supported by a PhD Fellowship of the Research Foundation - Flanders (application number 11A3619N). Stanislav Tyaginov is supported by the European Union's Horizon 2020 research and innovation programme (Marie Sklodowska-Curie grant agreement number 794950).

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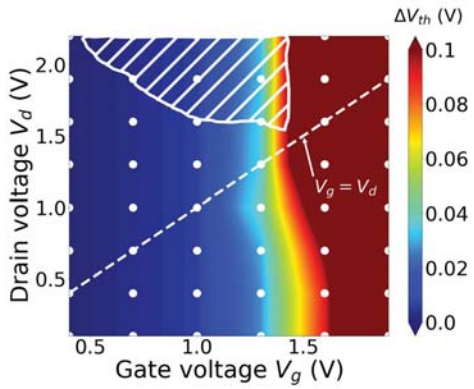

Fig. 8. Simulated $(V_{\mathrm{g}}, V_{\mathrm{d}})$ map of the degradation of threshold voltage V_{th}. The white dots indicate the simulated bias points for which stress was applied. The white shaded area indicates degradation which is observed in the measurements [9], but is missing in the simulations. The color scale was cropped at 0.1 V.

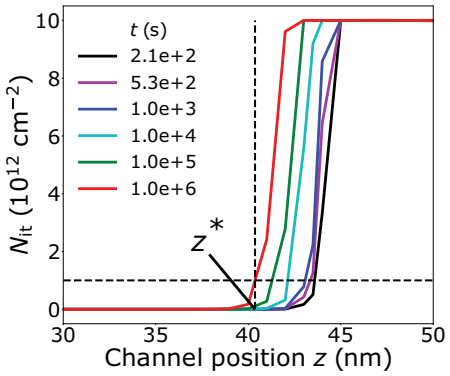

Fig. 9. Simulated interface defect profiles for the stress condition V_{g} = 1.9 V, V_{d} = 0.7 V. With increasing stress time, a defect front propagates from drain to source. The extent of defects in the channel was quantified by setting a threshold defect density (10^{12} cm^{-2}, horizontal dotted line) and looking for the channel position z^* where, starting from the source, the defect density first crosses this threshold value (vertical dotted line).

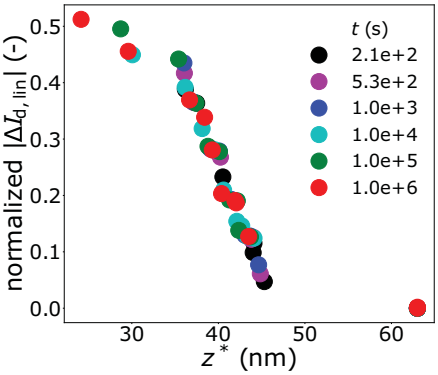

Fig. 10. When plotting the degradation of linear drain current versus the extent of defects into the channel z^*, the different $(V_{\mathrm{g}},V_{\mathrm{d}})$ stress points for different stress times fall on a single curve. In this plot, the degradation only includes the effect of interface defects (oxide defects were not included).

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