An ultra-low power, reconfigurable, aging resilient RO PUF for IoT applications

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ABSTRACT

Physically Unclonable Functions (PUF) have emerged as security primitives which can generate high entropy, temper resilient bits for security applications. However, the power budget of the ring oscillator (RO) PUF limits the use of RO PUF in IoT applications, in this concern a low power variant of RO PUF is much needed. In this paper, we have presented an ultra-low power, lightweight, configurable RO PUF based on the 4T XOR architecture. The proposed architecture is aging resilient; hence it produces a stable PUF output over the years. Also, it has a large number of challenge-response-pair (CRP) compared to the other architectures, which makes it suitable for chip identification as well as cryptographic key generation. The proposed PUF is implemented on 40 nm CMOS technology, and for the validation of design, we have also implemented on FPGA. The simulation results show that it has a uniqueness of 0.489 and worst-case reliability of 96.43% and 93.15% at 125 ℃ and 1.2 V, respectively. Compared to the conventional RO PUF it consumes 98.06% and 95.47% less dynamic and leakage power, respectively.

1. Introduction

Internet of things (IoT) is being used in a variety of emerging applications, such as smart homes, smart factories, intelligent vehicles, highways, wearable electronics, remote health care, agriculture, environmental monitoring system, personal health monitoring devices, and many more [1]. The IoT utilizes real-time analysis and machine learning methods to process data and make decisions; hence, security failure of these devices can affect billions of lives and huge financial loss with privacy invasion [2,3]. These make the security as one of the main concerns in the deployment of IoT devices on a large scale [4,5]. With the development of various hardware hacking methods, such as side-channel attacks and use of machine learning algorithms, make the key stored in non-volatile memory vulnerable to an attacker. To protect the sensitive data, Physically Unclonable Functions (PUF) have emerged as a promising security solution. PUF generates a unique, reliable, and secure key not only for cryptography but also for hardware authentication applications. It is well known that during fabrication, each chip experiences some unpredictable and uncontrollable semiconductor manufacturing process variations, which are usually undesired. These random process variations result in random changes in MOS parameters like the threshold voltage \(V_{th}\), and channel length \(L_{eff}\). By exploiting these inherent physical variations, a PUF generates a practically uncloneable, random functions. These variations are then converted into information in the form of response (output) corresponds to a challenge (input). Since manufacturing process variations are uncontrollable, unpredictable and random in nature, therefore, it is nearly impossible to have two chips with the same response for the same circuit. Hence, PUF can be considered as a unique fingerprint of the selected chip. This makes the PUF response as an active research area in the field of cryptography [6]. Broadly, PUF can be categorized into two categories: strong PUFs and weak PUFs [7]. The strong PUF has a large number of challenge-response pairs (CRPs), while CRPs of a weak PUF are limited [8]. A strong PUF is an ideal candidate for chip identification, as the chip can be identified using different challenges in each session without repeating any challenge.

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Many PUF architectures have been introduced in the literature like, Ring Oscillator (RO) PUF [8], Arbiter PUF [9], SRAM PUF [10], DRAM PUF [11] and RS latch PUF [12]. In the studies it has been observed that RO PUF is one of the best candidates for implementations in both FGPGAs [13–16] as well as ASIC in the following ways:

- It offers fabrication simplicity and high security over the others [6, 8, 16].
- The hard macro of RO can be instantiated multiple times. This makes all the ROs identical in terms of routing and placement. Also, the oscillation frequency of RO does not depend on routing delay.
- Delay difference due to process variations can be further amplified by allowing ROs to oscillate for a longer time.

To make a PUF useful in any of the aforementioned applications, the PUF response should be stable over time. However, due to aging, voltage and temperature variations, the performance of ASIC degrades, and the output becomes unreliable over time [17–19]. The transistor also suffers from various temporal degradations: Hot Carrier Injection bond defects at Si/SiO2 interface, which increases the threshold voltage and the output becomes unreliable over time [17–19]. The transistor PUF response should be stable over time. However, due to aging, 

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some of the traps are eliminated and the threshold voltage reduces. This phenomenon is called recovery phase. However, during recovery phase all the trapped charges cannot be recovered and hence threshold voltage increases with time. The final change in threshold voltage can be expressed in terms of stress and recovery time as [23]:

\[ \Delta V_{TH} = \Delta V_{TH,Stress} \times \left( 1 - \eta \times \frac{t_{Recovery}}{t_{Stress} + t_{Recovery}} \right) \]  \hspace{1cm} (2)

where \( t_{Stress}, t_{Recovery} \) are stress time, recovery time respectively and \( \eta \) is a constant with value 0.35.

2.1. NBTI effect in PUF

Fig. 3 shows the conventional RO PUF. Since a PUF is only used when an authentication takes place, or a key is required which is roughly 10% of the chip lifetime. The problem with the conventional architecture is even when the PUF is disabled still approximately half of the PMOSs of RO chain are in stress condition, which reduces the PUF reliability over time. To address the aging effect, very few architectures have been proposed. In Ref. [25], to improve the reliability against aging a configurable RO is proposed in which out of 8 ROs pairs one RO pair with maximum frequency difference is used to generate the PUF response. In Ref. [24], an aging resilient RO is proposed, to mitigate NBTI effects two extra transistors are added in each RO stage as shown in Fig. 4. This architecture has two limitations — first, the presence of additional transistors that can be considered as hardware overhead. Second, the PMOSs are still experiencing some NBTI effects even when PUF is not in use because the gate-to-source voltage (\( V_{GS} \)) of PMOS transistor is not completely zero.

3. The 4T XOR cell architecture used in RO PUF

We have modified the transmission gate based XOR gate [26] by removing one inverter as shown in Fig. 5. It can be seen from Fig. 5 that two additional transistors (\( M_3, M_4 \)) are added to the conventional CMOS inverter (\( M_1, M_2 \)). In the architecture, the supply lines have been replaced by control signals (\( C, \overline{C} \)) to make the architecture data-driven.

When \( C = '1', M_1 \) and \( M_2 \) forms an inverter whereas \( M_3 \) and \( M_4 \) are in cut-off state. Hence, the output is an inverted version of the input. On the other hand, when \( C = '0', M_1 \) and \( M_2 \) are in cut-off and based on input either \( M_3 \) or \( M_4 \) is in saturation state, this forms a transmission gate and hence without any degradation, the output is same as the input and the pass transistors (\( M_3 \) and \( M_4 \)) may add more process variations to PUF. Based on input signals the state of transistors can be defined as follows:

**Case 1:** when \( V_{DD} \) and \( V_{IN} = V_{DD} \)

In this case, CMOS inverter is powered through \( C \) and \( \overline{C} \), Hence the

\[ V_{OUT} = '0', \text{ Now for } M_3 \]

\[ V_{GS_{M3}} = V_C - V_{IN} = 0 \]

Similarly for \( M_4 \)

\[ V_{GS_{M4}} = V_{over} - V_{OUT} = 0 \]

From (3) and (4) it is clear that \( V_{GS_{M3}} > V_{TP} \) and \( V_{GS_{M4}} < V_{TN} \) and both will remain in cut-off.

**Case 2:** when \( C = V_{DD} \) and \( V_{IN} = '0' \)

Similarly to the previous stage, in this case also CMOS inverter is powered through \( C \) and \( \overline{C} \), Hence the

\[ V_{OUT} = V_{DD}, \text{ Now for } M_3 \]

\[ V_{GS_{M3}} = V_C - V_{OUT} = 0 \]

Similarly for \( M_4 \)

\[ V_{GS_{M4}} = V_{over} - V_{IN} = 0 \]

Referring to (5) and (6) \( V_{GS_{M3}} > V_{TP} \) and \( V_{GS_{M4}} < V_{TN} \) and both will remain in cut-off state.

**Case 3:** when \( C = '0' \) and \( V_{IN} = V_{DD} \)

In this case, the power supply of CMOS inverter is reversed; hence it does not act as an inverter anymore. Now for \( M_3 \)

\[ V_{GS_{M3}} = V_C - V_{IN} = -V_{DD} \]

Similarly for \( M_4 \)

\[ V_{GS_{M4}} = V_{over} - V_{OUT} = V_{DD} - V_{OUT} \]

(7) and (8) state that \( M_3 \) will always remain ON while \( M_4 \) goes to cut-off once \( V_{OUT} > V_{DD} - V_{TN} \)

For \( M_1 \)

\[ V_{GS_{M1}} = V_{IN} - V_{OUT} \]

Similarly for \( M_2 \)

\[ V_{GS_{M2}} = V_{IN} - V_{OUT} \]
Since $M_3$ and $M_4$ are ON, due to which $V_{OUT} = V_{IN}$, hence, $V_{DS3} = V_{DS4} = 0'$. 

**Case 4: when $C = '0'$ and $IN = '0'$**

In this case also, CMOS inverter does not work. Now for $M_3$

$$V_{DS3} = V_C - V_{OUT} = -V_{OUT}$$  \(11\)

Similarly for $M_4$

$$V_{DS4} = V_C - V_{IN} = V_{DD}$$  \(12\)

(11) and (12) state that $M_4$ will always remain ON while $M_4$ goes to cut-off once $V_{OUT} < V_{TP}$ and $M_1$ and $M_2$ remain off as in case 3.

Both $M_1$ and $M_2$ remains off and current flows due to $M_3$ and $M_4$ only. From case 1 and case 2, we can conclude that when $C = V_{DD}$ the additional transistors $M_3$ and $M_4$ do not affect the state of the output. Similarly, $M_1$ and $M_2$ remain off when $C = '0'$ and output is same as the input. These two additional transistors provide reconfigurability and may add more uniqueness to PUF.

4. The proposed PUF architecture

Fig. 6(a) shows the chain of our proposed RO, when a ‘1’ is received as a challenge the corresponding stage is configured as an inverter, and $M_3$ and $M_4$ are in cut-off otherwise it acts as a buffer and $M_1$ and $M_2$ are in cut-off, as shown in Fig. 6(b). When RO is not in use, the feedback loop is broken by setting $Enable = '0'$, and all the 4T XOR cells are configured as buffers by setting all the challenge bits to ‘0’ as shown in Fig. 6(c). Setting $Enable = '0'$ forces the output of AND gate to ‘0’ since all the cells are configured as a buffer, the input and output of all the cells become ‘0’, and there are no oscillations. Referring to (11) and (9), in this case the $V_{GS}$ of $M_1$ and $M_3$ will be ‘0’ and $-V_{OUT}$ respectively. For a buffer $V_{OUT} = V_{IN}$ and since $V_{IN} = '0'$, $V_{GS}$ of $M_3$ will be ‘0’ also. Hence the proposed architecture does not experience NBTI when not in use.

Fig. 7 shows the complete mechanism of our proposed PUF architecture where the shaded block is shared by all the ROs. In the conventional RO PUF, two ROs are used to generate only a single bit. However, in our proposed architecture two ROs can generate multiple bits. For the proper operation of the proposed architecture numbers of 1’s in the challenge must be odd. To fulfill the above conditions, either user can be asked, or a PUF controller can be used. Fig. 8 shows the flowchart of the PUF controller with Linear Feedback Shift Register (LFSR) counter used in our design. We have generated challenges from the PUF controller in two ways: (i) challenges having all odd number of ones (between 3 and 25) and (ii) challenges having $n$ number of ones, where $n$ can be any odd number. Following are the steps to generate the aforementioned challenges:

i. First, a 25-bit number is generated using the seed and then the number of ones is calculated.

ii. If the total number of ones are $n$, where $n$ can be either any odd number between 3 and 25 as shown in Fig. 8(a) or a user-specified odd number (15, 17, 19 or 21) as shown in Fig. 8(b) then the generated number is given to PUF as a challenge; otherwise, the next number is generated, and step (ii) is repeated.

iii. The PUF response is stored and the next challenge is generated using the step (ii). Steps (ii) and (iii) are repeated to collect a large set of challenge-response pairs.

For the effectiveness of the design, we have implemented the proposed PUF architecture in ASIC as well as in FPGA.

5. Experimental results: the functional testing

The functionality testing of the proposed PUF architecture is done on ten Basys3 FPGA boards using Xilinx Vivado. FPGA implemented architecture is shown in Fig. 9. On each FPGA we have implemented 32 instances of PUF in four different places. Challenges to PUF are given by using a 25-bit LFSR counter, and then responses are transmitted to PC using UART. In FPGA implementation of our proposed PUF 4T architecture is replaced by XOR gates and to avoid any routing effect, all
the ROs are placed manually. The resource utilization report is shown in Table 1.

### 5.1. Uniqueness

The uniqueness distinguishes two PUF instances. It is calculated using the inter-die Hamming distance (HD). It suggests that when imposing the same challenge to any two PUF instances then half of the response bit should be different. It has an ideal value of 50%.

Let us consider that corresponds to a challenge $C$, $R_a$ and $R_b$ are respectively two $n$-bit responses from randomly selected chip $a$ and $b$ out of $m$ number of available chips. The uniqueness ($U$) from $m$ chips can be expressed as:

$$U = \frac{2}{m(m-1)} \sum_{a=1}^{m-1} \sum_{b=a+1}^{m} \frac{HD(R_a, R_b)}{n} \times 100\%$$  \hspace{1cm} (13)

In the experiment, on each FPGA we have instantiated proposed PUF in four different places, extracted a thousand of 32-bit response from each of the instantiation and calculated uniqueness. We have also calculated the uniqueness between any two instantiations of proposed PUF on the same FPGA as intra-chip uniqueness. On a single FPGA, we have instantiated the proposed PUF on four different locations, hence we have total of six intra-chip CRPs for a single FPGA. Among all of the CRPs of ten FPGA boards, the maximum, minimum and mean value of intra-chip and inter-chip uniqueness for each case is reported in Table 2.

Table 2 shows that inter-chip and intra-chip uniqueness are lower when the number of inverters is 21, and it is the highest when the number of inverters is 17. Hence when the number of inverters is closed to the number of buffers the proposed PUF shows better inter-chip and intra-chip uniqueness. The distribution for inter-chip Hamming distance is shown in Fig. 10 shows the distribution of inter-chip Hamming distance for uniqueness value of 0.487, 0.469, 0.465 and 0.489 for 17, 19, 21 and all odd number of inverters (between 3 and 25), respectively.

Similarly, the distribution of intra-chip Hamming distance for uniqueness value of 0.475, 0.469, 0.458 and 0.490 for 17, 19, 21 and all odd number of inverters (between 3 and 25), respectively is shown in Fig. 11. Additionally, the average intra-chip Hamming distance for uniqueness between any two PUF response pair is 0.485, 0.488 and 0.479 for 17, 19 and 21 number of inverters, whereas, 0.501 for all odd number (between 3 and 25) of inverters. Further, we have also validated our design by performing simulation at 40 nm CMOS process as discussed in the subsequent section.

### 6. Simulation results

To generate a 32-bit response, 64 instances of ARO PUF, conventional RO PUF and proposed PUF are implemented using 40 nm CMOS process and each RO contains 25 inverting stages. Minimum size transistors ($W_{NMOS} = 120n\text{m}$ and $W_{PMOS} = 300n\text{m}$) are used for conventional RO and proposed RO and for ARO as specified in Ref. [24].

By sharing the controller block for each RO stage and using drain sharing technique, the proposed RO PUF has very less area overhead compared to the ARO PUF. Also the area overhead for aging reliability enhancement is zero. Fig. 12 shows the layout of the conventional RO pair, ARO pair and the proposed RO pair having a total area of 29.33 $\mu$m$^2$, 59.67 $\mu$m$^2$ and 53.84 $\mu$m$^2$, respectively. We have performed 1000 sets of Monte Carlo simulation with $\pm 3\sigma$ deviation to generate 32-bit CRPs and found that the uniqueness for the proposed PUF is 0.489, 0.478, 0.471 and 0.491 for 17, 19, 21 and all odd number (between 3 and 25) of inverters, respectively. The histogram for inter-chip Hamming distance is shown in Fig. 13. Simulation results
Table 2
Inter-chip and intra-chip uniqueness.

<table>
<thead>
<tr>
<th># Inverters (Out of 25)</th>
<th>Inter-chip Uniqueness</th>
<th>Intra-chip Uniqueness</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>17</td>
<td>0.489</td>
<td>0.476</td>
</tr>
<tr>
<td>19</td>
<td>0.477</td>
<td>0.466</td>
</tr>
<tr>
<td>21</td>
<td>0.470</td>
<td>0.458</td>
</tr>
<tr>
<td>All odd numbers (between 3 and 25)</td>
<td>0.491</td>
<td>0.477</td>
</tr>
</tbody>
</table>

for uniqueness are approximately equal to the FPGA results; hence the simulation results are confirmed by the FPGA results.

The power, area, and frequency of any circuit are essential parameters, which govern the effectiveness of the design. Apart from configurable and aging resilient the proposed RO is data-driven; hence, it requires very lower power and provides moderate output frequency. The dynamic power, leakage power, output frequency and area comparison among our proposed RO and other ROs, are shown in Fig. 14. For a total of 64 instances, our analysis indicates that the proposed RO consumes 95.4% and 98.06% less dynamic power, 99.93% and 99.94% less leakage power with 82.84% higher and 59.29% lower frequency, compared to the ARO and conventional RO, respectively. Also, the proposed design takes 83.56% more and 18.89% less area compared to the conventional RO and ARO, respectively.

![Fig. 10. Distribution of Inter-chip Hamming distance for proposed PUF for (a) 17 inverters and 8 buffers (b) 19 inverters and 6 buffers (c) 21 inverters and 4 buffers (d) All odd number (between 3 and 25) of inverters.](image)

![Fig. 11. Distribution of Intra-chip Hamming distance for proposed PUF for (a) 17 inverters and 8 buffers (b) 19 inverters and 6 buffers (c) 21 inverters and 4 buffers (d) All odd number of inverters (between 3 and 25).](image)

![Fig. 12. Layout of (a) Conventional RO pair (b) ARO pair and (c) Proposed RO pair.](image)

![Fig. 13. Distribution of Hamming distance for proposed PUF for (a) 17 inverters and 8 buffers (b) 19 inverters and 6 buffers (c) 21 inverters and 4 buffers (d) Any odd number of inverters.](image)
6.1. NBTI resiliency

Reliability analysis is carried out on Cadence RelXpert available in Cadence environment using 40 nm standard CMOS technology. Threshold variation due to NBTI under various stress time is shown in Fig. 15. Simulations results show that the proposed RO has 79.46% and 51.89% less degradation in PMOS threshold voltage compared to the conventional RO and ARO, respectively. The reason for improved threshold value is that even when disabled, instead of 0, the $V_{GS}$ of PMOS in ARO and conventional RO are $-V_{TN}$ and $-V_{DD}$, respectively. The mobility of the charge carrier is also affected by NBTI.

6.2. Reliability

Reliability is used to measure the stability of a PUF in various environmental conditions. Ideally, the difference between any two responses of the same challenge under different environmental conditions should be zero. Temperature variation and supply voltage fluctuations are the factors which affect circuit delay in practice, and due to these factors, the PUF response may become unstable. Reliability has been measured by comparing the two responses taken at different time instances. The reliability $R$ of a chip can be measured by:

$$R = 1 - \frac{1}{k} \sum_{m=1}^{k} \frac{HD(R_m, R'_m)}{n} \times 100\%$$

(14)

where $k$ is the number of samples, $n$ is the number of generated bits, and $HD(R_m, R'_m)$ is the hamming distance between $R_m$ and $R'_m$. Since temperature and supply voltage are two effective factors to affect circuit delay, we have checked the reliability of proposed PUF under varying temperature and supply voltage. Table 3 shows the reliability of proposed PUF under various operating temperatures and Fig. 16 shows Hamming distance for proposed PUF output bits with varying temperature.

From Table 3, it can be seen that the proposed PUF has better thermal stability, it has a bit-error-rate (BER) of 0.57%, 0.64%, and 0.78% for 17, 19 and 21 number of inverters at 50 °C, respectively. Out of the four transistors in Fig. 5, two transistors forming the inverters are more affected by the temperature as compared to the rest two transistors. The BER also increases slightly with the increased number of inverters. The BER for proposed design is increased by 3.55%, 3.87% and 4.88% for 17, 19 and 21 number of inverters, respectively, at 125 °C.

Similarly, for the analysis of power supply variation on the proposed PUF, the supply voltage is varied with ±10% as shown in Table 3. Out of the four transistors of Fig. 5, M3 and M4 are the pass transistors, and they are less affected by the supply voltage variations as compared to $V_{DD}$.
M1 and M2. Hence, as the number of inverter increases, the BER also increases.

Hamming distance for proposed PUF output bits with varying supply voltage is shown in Fig. 17. From Table 3 it can be shown that at 1.2 V the BER is maximum, which is 6.85%, 7.15% and 7.86% for 17, 19 and 21 number of inverters, respectively.

6.3. Randomness

Apart from being unique and reliable, the PUF output must be random. This means that from a set of PUFs, the responses of a specific PUF are unpredictable. To evaluate the randomness of the proposed PUF we have used the PUF responses as input to the NIST randomness test suite [27]. Table 4 shows that the proposed PUF passes all the NIST randomness tests that we are able to perform. Due to the limited number of the dataset, the NIST randomness tests that require large dataset have been omitted.

Fig. 18 shows the PMOS mobility degradation due to aging in conventional RO, ARO and proposed RO. After ten years of operation, the mobility degradation for conventional RO, ARO, and proposed RO are 2.23%, 0.76%, and 0.21%, respectively, from its initial value. Hence, our proposed RO PUF has better aging resiliency compared to both conventional RO and ARO PUF.

Table 4

<table>
<thead>
<tr>
<th>NIST Test</th>
<th>P-Value</th>
<th>Proportion</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>0.0884</td>
<td>328/330</td>
<td>Pass</td>
</tr>
<tr>
<td>Block Frequency</td>
<td>0.4628</td>
<td>326/330</td>
<td>Pass</td>
</tr>
<tr>
<td>Cumulative Sums (Forward)</td>
<td>0.0404</td>
<td>328/330</td>
<td>Pass</td>
</tr>
<tr>
<td>Cumulative Sums (Reverse)</td>
<td>0.1023</td>
<td>329/330</td>
<td>Pass</td>
</tr>
<tr>
<td>Runs</td>
<td>0.0151</td>
<td>329/330</td>
<td>Pass</td>
</tr>
<tr>
<td>Serial</td>
<td>0.0145</td>
<td>326/330</td>
<td>Pass</td>
</tr>
</tbody>
</table>

7. Conclusion

In this paper, we have presented an ultra-low power, lightweight, NBTI resilience reconfigurable PUF for IoT applications which consume very less power as compared to the other architectures. We validated our design by implementing on the FPGA as well as simulations. Results show that the proposed design has better uniqueness with less hardware compared to the other considered circuits. We also found that proposed architecture is less sensitive to temperature variations compared to the supply voltage variations. The effect of NBTI on proposed design is very less; hence, the design is resilient to temporal degradations. From the above discussion we can conclude that the proposed design is ultra-low power, lightweight, aging resilient and reconfigurable; hence it is best suited for the low power, high performance, and reliable IoT applications.

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