A12: Spintronic Memories

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With chips based on the 5nm technology node approaching production, the semiconductor industry is focusing on the 3nm technology node [1]. However, to sustain the growing demand for high performance small area CPUs and high-capacity memory, an introduction of a disruptive technology employing conceptually new computing principles becomes paramount. An attractive solution to significantly reduce the power consumption and eliminate leakage currents in modern integrated circuits is to employ the electron spin. Magnetic tunnel junctions (MTJs) are perfectly suited as key elements of nonvolatile CMOS-compatible magnetoresistive random access memory (MRAM) [2]. The information is encoded into two relative magnetization states with parallel or antiparallel orientation of the MTJ's magnetic layers. The resistances of the two states are different providing a way to sense the information electrically. The relative magnetization orientation can be switched by means of the spin transfer torque (STT) due to the current, which acts on a free recording layer.

Perpendicular MTJs (p-MTJs) are perfectly suited for high-density memory applications [2]. The discovery of an interface-induced perpendicular anisotropy at the CoFeB/MgO interface [3] enabled p-MTJ based MRAM. Thereby the switching current density is reduced, while the thermal barrier separating the two states - the thermal stability – is increased at the same time [2]. A p-MTJ structure with a composite free layer CoFeB/Ta/CoFeB with two MgO interfaces [4] boosts the thermal stability while reducing the Gilbert damping and the switching current. The use of shape anisotropy allows MTJ diameter scaling beyond 10nm [5]. STT-MRAM is processed on CMOS wafers before the back-end-of-line (BEOL) process [6]. For embedded applications, a successful implementation of 8Mb 1T-1MTJ STT-MRAM on a 28nm CMOS logic platform [7] was demonstrated. Recently, 128Mb embedded MRAM with 14ns write speed was reported [8]. An embedded MRAM solution compatible with Intel's 22FFL FinFET technology is available [9].

To further reduce the energy consumption, it is essential to replace the static RAM in modern hierarchical multi-level processor memory caches with a non-volatile memory. Spin-orbit torque (SOT) assisted MRAM is suitable for next-generation SRAM replacement [10]. In this memory cell the MTJ's free layer is grown on a material with a large spin Hall angle. The SOT acting on the adjacent magnetic layer is generated by passing the current through this material. However, for deterministic SOT-induced switching of a p-MTJ a magnetic field is required. A scheme employing two orthogonal current pulses is suitable for achieving sub-ns deterministic switching without an external magnetic field [11].

The introduction of non-volatility to data processing offers outstanding advantages over standard CMOS-based computing as it paves the way for a new low-power and high-performance computation paradigm based on logic-in-memory and in-memory computing architectures, where the same nonvolatile elements are used to store and to process the information. The availability of high-capacity nonvolatile memory in the proximity to high-performance CMOS circuits allows exploring conceptually new logic-in-memory [12] and computing-in-memory [13], [14] architectures for future artificial intelligence and cognitive computing [15].

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A13: What makes lead-based perovskites incommensurate

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Antiferroelectric perovskites are key part in highly pyro- and piezoelectric PZT ceramics. Prospective applications of antiferroelectrics include energy storage due to structural switching and non-volatile memory based on antiferroelectric domain walls. Physics behind antiferroelectric behavior is still puzzling. Why are these materials not ferroelectrics, as $BaTiO_3$ and $PbTiO_3$? This question is fascinating for quite some time.

The defining property of antiferroelectrics, such as $PbZrO_3$ and $PbHfO_3$, is the anti-polar arrangement of Pb^{2+} ion displacements in the low-symmetry phase. On the