Spin-Based CMOS-Compatible Memories

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***Abstract*—With CMOS device scaling slowing down, exploring new devices' working principles becomes paramount. The electron spin, as a complement to the charge, attracts much attention. The electron spin is characterized by the two well-defined projections on a given axis and is suitable for digital applications. Magnetic tunnel junctions (MTJs) feature different resistances in parallel and antiparallel magnetization configuration and enable spin-based types of non-volatile magnetic memories. MTJs are quite CMOS compatible as they are fabricated with a CMOS-friendly process. The relative magnetization configuration is manipulated by means of a spin-transfer torque (STT) acting on the free layer. The electrically addressable non-volatile STT memory is nearing mass production for stand-alone and embedded applications. The current status and modeling approaches of state-of-the art STT and spin-orbit torque memory are briefly reviewed.**

Keywords – Spin-transfere torque MRAM, spin-orbit MRAM, perpendicular magnetization, magnetic field free switching, two-pulse switching

Continuous miniaturization of semiconductor devices is the key driving force ensuring a breathtaking increase of performance of modern integrated circuits. With chips based on the 5nm technology node approaching production, the semiconductor industry is focusing on the 3nm technology node [1]. To sustain the growing demand for high performance small area CPUs and high-capacity memory, an introduction of a disruptive technology employing conceptually new computing principles becomes paramount. At the same time, the critically high power consumption becomes incompatible with the global demands of sustaining and accelerating the vital industrial growth, prompting an introduction of new solutions for energy efficient computations. An attractive path to dramatically reduce the power consumption and eliminate leakages in modern integrated circuits is to introduce non-volatility. Magnetic tunnel junctions (MTJs) are perfectly suited as key elements of nonvolatile CMOS-compatible magnetoresistive random access memory (MRAM) [2]. The MTJ is a sandwich made of two ferromagnetic layers separated by a thin tunnel barrier. The information can be encoded into two relative magnetization states with parallel or antiparallel orientations. The resistances of the two states are different providing a way to sense the information electrically. The relative magnetization orientation can be switched by means of the spin transfer torque (STT) acting on a free recording layer. The STT is generated by a current passing through the structure [3], [4].

Perpendicular MTJs (p-MTJs) are perfectly suited for high-density memory applications [2]. However, it is difficult to find a material with the uniaxial anisotropy so strong that it overcomes the demagnetization effects of the free recording layer. The discovery of an interface-induced perpendicular anisotropy at the CoFeB/MgO interface [5], which enforces the very thin CoFeB layer perpendicularly magnetized, was a critical technological step to enable p-MTJ based MRAM.

One of the key challenges in STT-MRAM is to reduce the switching current density while increasing the thermal barrier separating the two states - the thermal stability - at the same time [2]. A p-MTJ structure with a composite free layer CoFeB/Ta/CoFeB with two MgO interfaces [6] allows boosting the thermal barrier. The use of the p-MTJ structure with the two CoFeB/MgO interfaces also reduces the Gilbert damping by half, thus allowing to simultaneously decrease the switching current.

To reduce the diameter of the MTJ beyond 10nm, the use of shape anisotropy is attractive [7]. It has been shown that the thermal stability can be significantly increased for small diameters without sacrificing on the tunneling magnetoresistance ratio (TMR) and without new materials to be employed, as FeB for the ferromagnetic free layer and MgO for the tunnel barrier were used.

In order to integrate STT-MRAM with the CMOS fabrication process, MTJs must sustain the 400Cº temperature typical for the back-end-of-line (BEOL) process. Recently, a process allowing to preserve the high TMR and the thermal stability of MTJs was reported [8]. In this process the fixed layer is on the top of the MTJ. An additional synthetic ferromagnet instead of an antiferromagnet is employed to pin the magnetization of the fixed layer to sustain the BEOL process temperature. However, an additional compensating magnet is required to achieve symmetric switching between the parallel and the antiparallel configuration and back.

A large TMR ratio is needed for reliably reading the information in MRAM. Indeed, the middle reference resistance, to which the low and high resistance MTJ states are compared, must be well separated from either of them. However, with downscaling it becomes increasingly difficult to control the bit-to-bit resistance variation. As the resistance variation dispersion increases, the TMR must also increase to provide a sufficiently broad window for reliable reading. Obtaining a TMR significantly larger than 350% is an important challenge [9] to overcome, in order to continue with the devices scaling down.

STT-MRAM is fast (10ns), possesses high endurance (10^{12}), has a simple structure, and is compatible with the BEOL CMOS process. It is particularly promising to be used in internet of things (IoT) and automotive applications. It is also attractive as a nonvolatile

replacement of conventional volatile CMOS-based DRAM and nonvolatile flash memory. High-density STT-MRAM arrays with 4Gbit capacities have been already demonstrated [10]. For embedded applications, a successful implementation of 8Mb 1T-1MTJ STT-MRAM on a 28nm CMOS logic platform [11] was demonstrated. Recently, 128Mb embedded MRAM with 14ns write speed was reported [12]. An embedded MRAM solution compatible with Intel's 22FFL FinFET technology is available [13].

To further reduce the energy consumption, it is essential to replace static RAM in modern hierarchical multi-level processor memory caches with a non-volatile memory. Although STT-MRAM can in principle be used in L3 caches [14], the switching current flowing through the tunneling oxide becomes very large and may damage the tunnel barrier at an access time of 5ns and faster. Among the newly discovered physical phenomena suitable for next-generation MRAM is spin-orbit torque (SOT) assisted switching at room temperature in heavy metal/ferromagnetic [15], [16] or topological insulator/ ferromagnetic [17], [18] bilayers. In this memory cell the MTJ's free layer is grown on a material with a large spin Hall angle. The SOT acting on the adjacent magnetic layer is generated by passing the current through this material. The relatively large switching current is injected in-plane along the heavy metal/ferromagnetic bilayer and does not flow through the MTJ, while a much smaller read current is applied through the MTJ. Three-terminal spin-orbit torque (SOT) MRAM can be integrated on a 300mm CMOS wafer using CMOS compatible processes [19]. However, for deterministic SOT-induced switching of a perpendicular free magnetic layer a static magnetic field is required. A scheme employing the two orthogonal current pulses is suitable for achieving the sub-ns deterministic switching without an external magnetic field [20].

The introduction of non-volatility to data processing offers outstanding advantages over standard CMOS-based computing as it paves the way for a new low power and high-performance computation paradigm based on logic-in-memory and in-memory computing architectures, where the same nonvolatile elements are used to store and to process the information. The availability of high-capacity nonvolatile memory in the proximity to high-performance CMOS circuits allows exploring conceptually new logic-in-memory [21] and computing-in-memory [22], [23] architectures for future artificial intelligence and cognitive computing [24].

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