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Physics-based Modeling of Hot-Carrier Degradation in Ge NWFETs

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Abstract

Hot-carrier degradation (HCD) has been reported to be weaker in Ge NWFETs than in their Si counterparts. We consider HCD in Ge NWFETs to be controlled by dissociation of Ge-O bonds which creates O-vacancies consistent with atomistic calculations. The mean value of the activation energy for this reaction is 5.6 eV and the standard deviation is 0.6 eV. This is because – due to segregation of Ge into the SiO_2 film – the IL dielectric is non-stoichiometric $Si_xGe_yO_{2(x+y)}$. In simulations, we also retain a relatively low concentration of Si-H bonds with a large value of the energy dispersion equal to 0.6 eV (due to Ge rich environment) and a mean energy of 2.4 eV (slightly lower than in the Si/SiO_2 system). Our approach can represent experimental degradation traces with good accuracy for different combinations of stress voltages and explain superior HC reliability of Ge NWFETs.

1. Introduction

The arrival of the mobile era requires long battery lifetime and, therefore, further reduction of the OFF current in modern field-effect transistors (FETs). This goal can be achieved by two strategies: introduction of novel device architectures such as fin and nanowire (NW) FETs and employment of high mobility channel materials [1,2]. Among the elemental semiconductors Ge was suggested to be the most promising candidate [2]. Nevertheless, commercialization of any novel devices/materials can be hindered by reliability problems and therefore reliability of Ge (and SiGe) FETs has been a subject of extensive research over last years [3].

Among reliability issues, hot-carrier degradation (HCD) was reported to be the most severe parasitic effect in ultra-scaled devices on Si [4]. Ge has higher mobilities of electrons and especially holes compared to Si and one can, therefore, envisage that HCD in Ge devices is more detrimental than in FETs on Si (for same stress conditions). Quite surprisingly, in one of the recent publications *imec* reported better HC reliability of Ge NWFETs than in their Si counterparts [5]. More general, a model for HCD in Ge transistors based on physical principles is still missing.

In this paper we propose a physics-based model for HCD in Ge NWFETs based on an accurate description of carrier transport and microscopic defect physics.

2. Devices and Experiment

We used Ge p-channel gate-all-around test-structures (see Fig. 1) with a channel length of 100 nm and 44 stacked wires. These devices have operating and threshold voltages of V_{dd} = -0.5 V and V_{th} ~ 0.15 V, respectively. A high-k gate stack (including SiO_2 and HfO_2 layers) was fabricated on a 6 monolayer Si cap on top of the Ge surface. Assuming segregation of Ge through the Si cap into the SiO_2 layer the resulting interfacial layer is $Si_xGe_yO_{2(x+y)}$, i.e. is composed from suboxides of Si and Ge. The devices received high pressure hydrogen anneal at the end of the process [6].

These NWFETs were subjected to hot-carrier stress at a fixed overdrive voltage of V_{ov} = -1.5 V and three different values of the drain voltages: V_{ds} = -1.0, -1.3, and -1.5 V. Ambient temperature was set to T = 298 K. To assess HCD, relative changes in the saturation drain current, $\Delta I_{d,sat}$ ($I_{d,sat}$ corresponds to V_{gs} = V_{ds} = -0.5 V), as functions of stress time, t, were recorded and are summarized in Fig. 2.

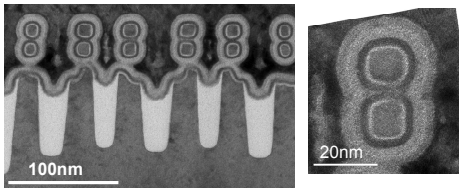

Fig. 1. The cross-section of the Ge NWFETs

3. Simulation Framework

To model HCD in Ge NWFETs we use the modeling approach which was developed to describe HCD in Si FETs [7-9]. This approach covers and links three main subtasks related to HCD: carrier transport modeling, a defect generation description and modeling of the degraded devices.

For **carrier transport modeling** we implemented Ge in the deterministic solver of the Boltzmann transport equation ViennaSHE [10], which evaluates carrier energy distribution functions (DFs) for specified stress conditions and device architecture (which is obtained from the Sentaurus Process simulator). Our calculations demonstrated that hole DFs in Ge based devices have high-energy tails which propagate to energies higher than those typical for DFs in Si devices of a comparable architecture. Based on this behavior one can imagine that HCD should be stronger in Ge NWFETs.

Therefore, we expect that the opposite trend reported in [5] stems from the **defect generation kinetics**. In other words, higher carrier temperatures in Ge devices can be compensated by higher activation energies for trap creation typical for the $Si_xGe_yO_{2(x+y)}$ film. Ge and Si have the same crystalline structure and the precursors of defects generated during HC stress in Si devices are the Si-H bonds. Reasoning by analogy, we can conclude that in the IL dielectric layer consisting of Ge suboxides the Ge-H bonds are the defect precursors. However, studies based on atomistic *ab initio* calculations with density functional theory (DFT) performed by Houssa and co-authors [11] have shown that although Ge-H bonds can be formed during hydrogen anneal with a relatively low barrier of ~1.4 eV these bonds spontaneously dissociate with the energy barrier for this reaction being ~0.5 eV. Note that DFT calculations by the Vanderbilt group [12] confirm these results.

However, Houssa *et al.* [11] suggested that O-vacancies can be responsible for parasitic effects in devices based on Ge dioxides/suboxides. This idea was also confirmed by

other groups [13,14]. Therefore, in this work we assume that HCD in Ge FETs is driven by dissociation of Ge-O bonds at the SiGe/$Si_xGe_yO_{2(x+y)}$ interface which results in creating O-vacancies. Our own DFT calculations with the CP2K code and using a hybrid functional show that the potential barrier for the reaction which converts Ge-O bonds to O-vacancies is ~5.5 eV. The process has been modeled as a realistic reaction pathway for the creation of an oxygen vacancy in a periodic model of crystalline GeO_2.

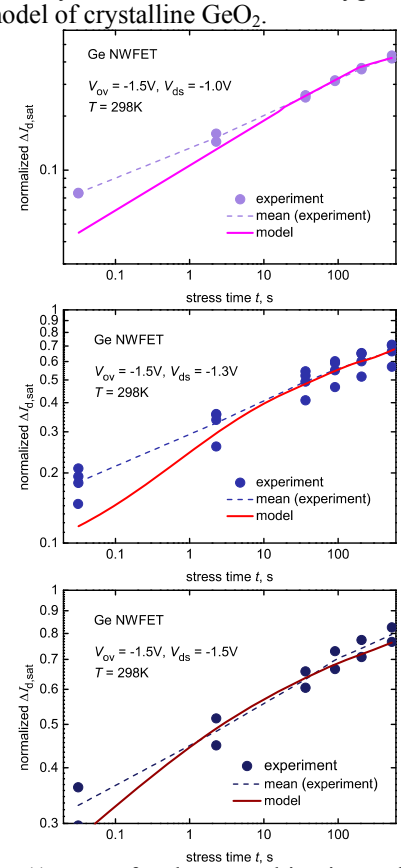

Fig. 2. $\Delta I_{d,sat}(t)$ traces for three combinations of stress voltages: experiment (multiple devices) vs. simulations.

Ab initio calculations performed by Oeffner *et al.* [15] showed that the bond-breakage potential can be parameterized with the Morse potential and therefore we model the bond-breakage rate based on this potential. Note that for modeling of dissociation of Si-H bonds we used the harmonic potential [7-9]. Like in the case of HCD in Si devices we consider the interplay between multiple- and single-carrier processes of bond dissociation. In the case of the harmonic potential, only transitions $i \rightarrow i + 1$ (bond excitation) and $i \rightarrow i - 1$ (bond deexcitation), where i is the bonded level index, are allowed. As for the Morse potential, all transitions are possible and therefore we solve the Pauli master equation to calculate the rate of the multiple-carrier mechanism. Since the Ge-O bonds are located in the non-stoichiometric $Si_xGe_yO_{2(x+y)}$ film we use a large values of the bond-breakage energy dispersion of $\sigma_{E,Ge\text{-}O}$ = 0.6 eV; the mean value of this energy is $E_{Ge\text{-}O}$ = 5.6 eV (close to the value obtained with DFT). The concentration of pristine Ge-O bonds in the model is relatively high: $N_{Ge\text{-}O} = 7 \cdot 10^{12} cm^{-2}$.

Si-H bonds are still present at the SiGe/$Si_xGe_yO_{2(x+y)}$ interface and the corresponding bond-breakage rates should be considered. We model them in the same manner as in the case of HCD in Si devices. However, in the current case the Si-H bonds are placed in Ge rich environment and therefore we use a large value of the standard deviation of the bond dissociation energy, namely $\sigma_{E,Si\text{-}H}$ = 0.6 eV, while the mean bond-breakage energy is $E_{Si\text{-}H}$ = 2.4 eV, i.e. slightly lower than that typical for the Si/SiO_2 system (2.56 eV [8]). The concentration of virgin Si-H bonds is $N_{Si\text{-}H} = 2 \cdot 10^{12} cm^{-2}$, i.e. substantially lower than in the case of Si FETs (~$7 \cdot 10^{12} cm^{-2}$, see [9]).

4. Results and Discussion

Fig. 2 shows good agreement between experimental and simulated $\Delta I_{d,sat}(t)$ degradation traces. Some discrepancy is visible at short stress times and probably related to lack of self-heating in our modeling approach.

For comparison, we also plotted $\Delta I_{d,sat}(t)$ dependencies obtained by considering only Si-H bonds as the precursors with the concentration $N^*_{Si\text{-}H}$ equal to the sum of both precursor concentrations $N_{Ge\text{-}O} + N_{Si\text{-}H} = 9 \cdot 10^{12} cm^{-2}$, see Fig. 3. From Fig. 3 one can conclude that these $I_{d,sat}$ changes have much higher values than experimental ones and those obtained by considering both precursors (Fig. 2). In other words, hypothetical Si devices of a similar architecture subjected to HCD at the same carrier energies would degrade much stronger than real Ge NWETs. This trend is consistent with data from [5].

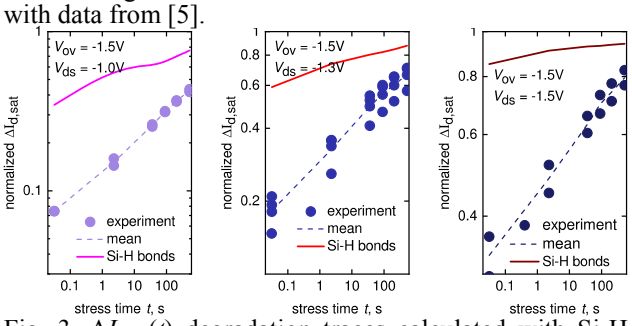

Fig. 3. $\Delta I_{d,sat}(t)$ degradation traces calculated with Si-H bonds only (the concentration is $N^*_{Si\text{-}H} = 9 \cdot 10^{12} cm^{-2}$).

5. Conclusion

We presented and validated a physics-based model for hot-carrier degradation in Ge NWFETs. This model is based on two types of defects (and their precursors), i.e. considers O-vacancies and Si-H bonds at the SiGe/$Si_xGe_yO_{2(x+y)}$ interface. Our approach has been shown to accurately reproduce $\Delta I_{d,sat}(t)$ traces for three stress conditions and can explain superior hot-carrier reliability of Ge NWFETs as compared to Si devices.

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