# Understanding and Physical Modeling Superior Hot-Carrier Reliability of Ge pNWFETs

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**Abstract**: Hot-carrier degradation (HCD) of Ge pNWFETs has been shown to be significantly lower and different than that of Si pNWFETs. Here we accurately model degradation and the time-to-failure (TTF) measured during HC stress in Ge pNWFETs. For this, we use our HCD framework validated against hot-carrier degradation in Si devices, and first we show here that it thoroughly represents HCD Si pNWFETs. This framework is naturally extendable to incorporate new defects (O-vacancies) and their precursors (Ge-O bonds) which are involved in HCD in Ge transistors. These Ge-O bonds are present due to segregation of Ge through the Si cap into the $SiO_2$ film of the high-$k$ gate stack with subsequent formation of the $SiGe/Si_xGe_yO_{2(x+y)}$ interface. The Ge-H bonds are argued to be unstable while a low concentration of Si-H bonds with a broad distribution of the bonding energy should still be considered. Our unified model has been demonstrated to accurately capture degradation and TTFs in both Ge and Si pNWFETs, with the superior slope of the TTF vs. drain current dependency in the Ge devices determined by the defect creation energetics, hereby supported by *ab initio* calculations.

## Introduction

Hot-carrier degradation (HCD) is being repeatedly reported to be the dominant degradation mechanism in modern field-effect transistors (FETs) on Si [1]. In this spirit, models for HCD in Si devices have evolved from simplified empirical approaches to quite sophisticated physical models which capture the microscopic picture behind this detrimental phenomenon [2–4]. While transistors are optimized by introducing novel device topologies such as FinFETs, multi-gate structures, and nanowires (NWs) [5, 6], further optimization will be achieved by using high mobility channel materials. Among the elemental semiconductors, Ge has the highest hole mobility [6] and hence ultra-scaled transistors with Ge channels appear to be very attractive.

We have recently reported superior HC reliability of Ge NWFETs as compared to their Si counterparts [7]. Fig. 1 shows dependencies of the time-to-failure (TTF) on the stress drain current $I_d$ acquired in Ge and Si pNWFETs (sketched in Fig. 2) measured at $T = 298$ K. One can see that in Ge devices TTF reduces with the current ($I_d$) as $\sim I_d^{-41}$, while in Si NWFETs this dependency is much more gradual, i.e. TTF$\sim I_d^{-12}$. This trend suggests that at stress currents corresponding to the operating regime Ge devices should have much better TTFs.

Based on this, we conclude that *HCD in Ge and Si devices is fundamentally different*. Previously we have developed and validated a physics-based model for HCD in Si FETs [8, 9] which will be shown to capture degradation traces in Si pNWFETs (Fig. 3) and the corresponding TTF dependency. Then this *framework will be extended to incorporate new defects/precursors* responsible for HCD in Ge devices and to eventually reproduce HCD in Ge pNWFETs (Figs. 4-10).

## Devices and Experiment

We used p-channel Ge and Si gate-all-around NWFETs with a gate length of 100 nm (TEM images of their cross-sections are given in Fig. 2). Each transistor is made up of 22×2 stacked wires with a diameter of 9 nm. The high-$k$ gate stack consists of $SiO_2$ and $HfO_2$ layers with physical thicknesses of 0.7 and 2.1 nm. In the case of Ge devices the high-$k$ stack was fabricated on a 6 ML Si cap wrapping the Ge channel [10]. The operating voltages $V_{dd}$ are -0.5 and -0.9 V for Ge and Si NWFETs, respectively. Recent SIMS measurements [11] carried out using the same Ge technology evidence segregation of Ge through the Si cap. Fig. 4 shows Ge and Si concentrations extracted from SIMS data in the area surrounding the channel/cap interface of the Ge NWFET – the Ge concentration in the Si cap is high. Note that these concentrations are obtained before oxidation which formed the Ge rich non-stoichiometric $Si_xGe_yO_{2(x+y)}$ layer (containing Si and Ge sub-oxides). Both Ge and Si devices were exposed to high pressure hydrogen anneal [10].

The transistors were subjected to HCD at different combinations of gate and drain voltages ($V_{gs}$, $V_{ds}$) at room temperature (for more details see [7]). To ensure that BTI does not provide a significant contribution to the entire degradation we chose regimes with $V_{ds} > 1.0$ V in combination with $T = 298$ K (see [7]); in this regime the degradation is dominated by the multiple-carrier process of bond dissociation. During stress ($t \sim 500$ s) relative changes of the saturation drain current $\Delta I_{d,sat}$ were monitored ($I_{d,sat}$ corresponds to $V_{gs} = V_{ds} = V_{dd}$); some of $I_{d,sat}(t)$ traces are plotted in Figs. 9 and 3. Then TTFs were evaluated based on the $\Delta I_{d,sat} = 0.1$ criterion, see Fig. 1. Since Ge and Si FETs have substantially different threshold voltages and electrostatics such *TTF plots provide a cumulative metric of HC reliability* which is more informative than comparison of particular $\Delta I_{d,sat}(t)$ traces.

## The model

Our simulation framework for hot-carrier degradation [8, 9] covers and links three main modules: a description of carrier transport, modeling defect generation kinetics, and simulations of the degraded FETs. **The carrier transport module** is based on the deterministic solver of the Boltzmann transport equation ViennaSHE [12]. ViennaSHE employs the spherical harmonics expansion method and incorporates the full-band effects as well as different scattering mechanisms. To describe carrier confinement in ultra-scaled devices ViennaSHE uses a model similar to the density gradient approximation [13]. Hole energy distribution functions (DFs) obtained with ViennaSHE are depicted in Fig. 5. One can see that the DFs are significantly shifted from equilibrium and this is especially pronounced at the device drain where the carriers are substantially hot. Comparison of DFs calculated for the same combination of $V_{gs}$ and $V_{ds}$ (Fig. 5, right panel) for different channel materials shows that in Ge channels the DF high-energy tails extend to higher energies and therefore holes in the Ge FETs are hotter than in Si devices. This trend is consistent with a substantial asymmetry of hole mobilities in Ge and Si materials. Based on this reasoning one could expect that HCD would be more detrimental in Ge NWFETs; however, experimental data show the opposite trend (Fig. 1).

Therefore, we suppose that higher carrier energies typical for the Ge device must be compensated by higher activation energies of the **defect generation** reaction which is responsible for HCD in Ge FETs. HCD in Si devices is driven by dissociation of Si-H bonds at the $Si/SiO_2$ interface [2–4]. Since the $Si_xGe_yO_{2(x+y)}$ layer contains Ge and Si sub-oxides, it is natural to expect that the defect precursors are Ge-H and Si-H bonds at the $SiGe/Si_xGe_yO_{2(x+y)}$ interface. However, *ab initio* calculations with density function theory (DFT) performed by Houssa *et al.* [14] demonstrated that although passivation of dangling Ge- bonds with H results in formation of Ge-H bonds (the activation energy of this reaction is ∼1.4 eV) these bonds are not stable and easily dissociate (with a very low dissociation energy of ∼0.5 eV). Similar results were published also by the Vanderbilt group [15]. DFT calculations reported by the EPFL group [16, 17] as well as by Chang *et al.* [18] suggested that O-vacancy related defects result in energy transition levels which can degrade the Ge device characteristics.

In order to investigate mechanisms of how vacancies could form in $GeO_2$, we conducted our own **DFT calculations**. We used DFT as implemented in the CP2K code with all energies evaluated only at the Γ-point of the Brillouin zone [19]. The hybrid PBE0 exchange correlation functional was used due to its ability to accurately reproduce the band gap of oxides [20]. The basis sets employed to evaluate the energies were a mixed Gaussian and plane waves basis set [21]. For the Gaussian basis

set, we used a double Zeta basis set with polarization functions on both the Ge and O atoms. The plane wave basis set was truncated at 1200 Ry. In order to mitigate the expense of the hybrid functional, we utilized an approximation known as the auxiliary density matrix method [22]. For evaluating reaction barriers, we used the climbing image variant of the nudged elastic band method [23].

To get an idea of the energy required to create an oxygen vacancy, we explicitly modeled a Frenkel pair formation reaction in crystalline $GeO_2$. We started with a 3×3×3 supercell of crystalline $GeO_2$ with a quartz structure whose cell parameters and atomic structure were optimized with respect to the total energy within our DFT setup. This resulted in two Ge-O bond environments of 1.78 Å and 1.74 Å. Analysis of the electronic structure reveals a band gap of 5.64 eV. These results are in good agreement with previous experiments [24]. To create a Frenkel pair, we then displaced an O ion from its equilibrium position between two Ge atoms towards a neighboring Ge atom and then optimized the structure. This resulted in the final configuration shown in Fig. 6. We therefore obtained our initial and final states for Frenkel pair creation. Starting from a linear interpolation between these two states, we used nudged elastic band to optimize the reaction pathway and obtain the minimum energy pathway between them. We found an activation energy of ∼5.5 eV with the reaction pathway shown in Fig. 6.

Similar to modeling HCD in Si FETs we consider all superpositions of multiple- and single-carrier (MC- and SC-) processes of bond dissociation [9]. In the case of Si devices the HCD models [2–4] parameterize the Si-H bond using the harmonic potential and this strategy provides a good trade-off between computational efficiency and accuracy. However, this approach is not applicable to Ge-O bonds, which have a much higher bond-breakage energy (Fig. 6) and where anharmonicity plays a substantial role. Therefore, we use the Morse potential to parameterize the barrier for the Ge-O bond dissociation reaction, see Fig. 7 and Eq. 1. In contrast to the harmonic potential – where only transitions $i \rightarrow i+1$ (bond excitation) and $i \rightarrow i-1$ (bond deexcitation) are permitted – transitions between any arbitrary levels are possible. For calculating occupation numbers of the bond levels and hence the MC-process rate we solve the Pauli master equation (see Fig. 7, Eqs. 2 and 3); note though that this substantially increases computational time.

Finally, Si-H bonds still remain at the $SiGe/Si_xGe_yO_{2(x+y)}$ interface. However, strictly speaking, in the $Si_xGe_yO_{2(x+y)}$ environment Si-H and Ge-H are not discernible and the bond-breakage energy of such hybrid bonds should vary in the range between 2.6 eV typical for Si-H bonds at the $Si/SiO_2$ interface [25] and 0.5 eV corresponding to Ge-H bonds placed in the idealized $Ge/GeO_2$ system [14]. To limit the number of adjustable parameters of the model we assume that the Si-H bonds are present with a low concentration at the interface and their mean bonding energy is $\langle E_{\mathrm{a,Si-H}} \rangle = 2.6\,\mathrm{eV}$, but its standard deviation $\sigma_{\mathrm{E,Si-H}}$ is large. From Fig. 5 it is seen that the concentration of carriers with energies higher than $\langle E_{\mathrm{a,Si-H}} \rangle$ is very low and therefore both O-vacancy and $P_b$-center generation reactions are dominated by the MC-process.

**Simulations of the degraded devices** were conducted using the device and circuit simulator MiniMOS-NT. To capture quantization effects MiniMOS-NT employs the density gradient and improved modified local density approximation methods [26]. The device architectures were obtained from Sentaurus Process [27]; the device and process simulators were coupled and calibrated consistently in a manner to represent characteristics of unstressed transistors. This step is not only important to ensure that our simulation setup is properly calibrated but also required for accurate modeling of the drain currents needed for representing the $\mathrm{TTF}(I_{\mathrm{d}})$ curves, Fig. 1.

## Results and Discussion

**HCD in Si pNWFETs**: the model accurately captures normalized changes of the saturation drain current $\Delta I_{\mathrm{d,sat}}$ (changes of the current are normalized to $I_{\mathrm{d,sat}}(t=0)$) with good accuracy, see Fig. 3. The concentration of pristine Si-H bonds used in the model was set to $N^{(0)}_{\mathrm{Si-H}} \sim 3{\times}10^{12}\,\mathrm{cm}^{-2}$. Note that such a concentration lies in the same range as those values we employed for HCD modeling in different Si technologies [8, 28, 29]. Finally, the properly calibrated model allowed us to represent experimental dependencies of TTF vs. the stress current (Fig. 1) and obtain a time slope of 11 which is quite close to the experimental one equal to 12.

The HCD model for the **Ge pNWFETs** has been calibrated to represent degradation traces $\Delta I_{\mathrm{d,sat}}$, see Fig. 9. For Ge-O bonds we used the mean value and the standard deviation of the bond-breakage energy of $\langle E_{\mathrm{a,Ge-O}} \rangle = 5.6\,\mathrm{eV}$ and $\sigma_{\mathrm{E,Ge-O}} = 0.8\,\mathrm{eV}$. The $\langle E_{\mathrm{a,Ge-O}} \rangle$ value is consistent with our DFT results (see Fig. 6), while the large $\sigma_{\mathrm{E,Ge-O}}$ reflects the fact that Ge-O bonds are placed in the non-stoichiometric $Si_xGe_yO_{2(x+y)}$ film. We also used a relatively high concentration of pristine Ge-O bonds, i.e. $N^{(0)}_{\mathrm{Ge-O}} \sim 7{\times}10^{12}\mathrm{cm}^{-2}$; we suppose that this is a reasonable value because the Ge concentration at the interface is very high (Fig. 4). As previously discussed, we employed a low concentration of Si-H bonds $N^{(0)}_{\mathrm{Si-H}} = 6{\times}10^{11}\,\mathrm{cm}^{-2}$ (this value is much lower than that used to model HCD in Si NWFETs) and a large standard deviation $\sigma_{\mathrm{E,Si-H}} = 0.67\,\mathrm{eV}$. Other parameters of the Si-H bond dissociation reaction – such as vibrational lifetimes, energy distances between the parabolic potential eigenstates, etc. – were set to standard values typical for the stretching vibrational mode of the Si-H bond [9].

The model calibrated in this manner is capable of capturing $\Delta I_{\mathrm{d,sat}}(t)$ degradation traces with good accuracy, see Fig. 9. Moreover, our HCD model results in a slope of ∼39 of the TTF dependency against the stress current, while the slope extracted from experimental data is ∼41, i.e. experimental and theoretical values are in good agreement (Fig. 1). Note that carriers in the Ge NWFETs are substantially hotter than those in the Si devices and this results in very rapid dissociation of Si-H bonds. From Fig. 8, left panel one can see that the interface trap density profiles have two saturation levels corresponding to concentrations of the two precursors, $N^{(0)}_{\mathrm{Ge-O}}$ and $N^{(0)}_{\mathrm{Si-H}}$. The concentration of O-vacancies is localized in the drain section of the device, while the concentration of broken Si-H bond is spread much wider, see Fig. 8, left and central panels. Finally, Fig. 8, right panel shows $N_{\mathrm{it}}$ profiles in a hypothetical Si device of a similar architecture and subjected to HC stress at the same carrier energies as the Ge transistor; the concentration of Si-H precursors in such a device is equal to the total concentration ($N^{(0)}_{\mathrm{Ge-O}} + N^{(0)}_{\mathrm{Si-H}} \sim 8{\times}10^{12}\,\mathrm{cm}^{-2}$) of both precursors in the Ge NWFET. One can see that almost the entire device is heavily degraded (Fig. 8) and the corresponding degradation traces have severely overestimated values (Fig. 10). This again shows that Ge transistors are more reliable to HC stress than FETs on Si.

We can summarize that *the superior TTF of the Ge NWFETs stems from different precursors/defects* contained in Ge devices (primarily Ge-O bonds and O-vacancies with a low concentration of Si-H bonds and $P_b$-centers) compared to Si devices (Si-H bonds and $P_b$-centers with typical densities).

## Conclusions

*The fundamental difference between hot-carrier degradation in Si and Ge devices is due to different sets of defects and their precursors* involved in HCD in FETs with different channel materials. We *naturally extended our thoroughly validated HCD modeling framework* – which captures HCD in Si pNWFETs – by incorporating the reaction which transforms neutral Ge-O bonds (precursors) into O-vacancies (defects) which are located at the $SiGe/Si_xGe_yO_{2(x+y)}$ interface. Our approach also considers a low concentration of Si-H bonds with a large standard deviation of their bond-breakage energy, while Ge-H bonds are not stable and do not contribute to HCD. The model has been shown to thoroughly capture $\Delta I_{\mathrm{d,sat}}(t)$ traces as well as the slope of the time-to-failure dependency on the stress current. The *superior TTF in Ge devices* has been explained by a much *higher energy needed to break Ge-O bonds* and form O-vacancies (our DFT calculations showed that this energy is ∼5.5 eV) compared to the Si-H bond rupture energy (∼2.6 eV).

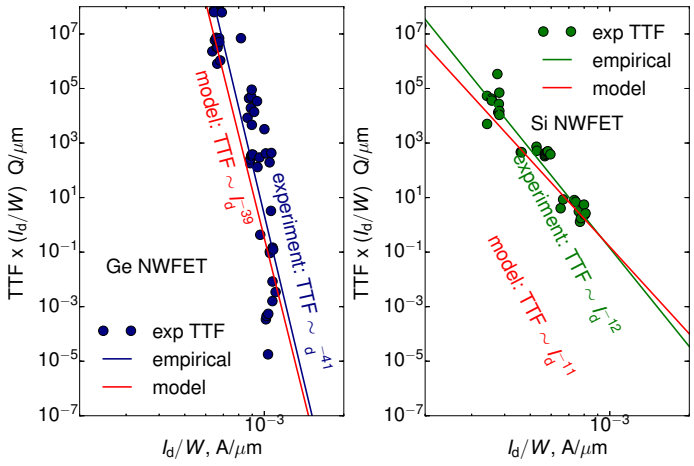


Figure 1: Dependencies of normalized TTFs on normalized stress currents measured and modeled for Ge and Si NWFETs. One can see good agreement between experimental and simulated data.

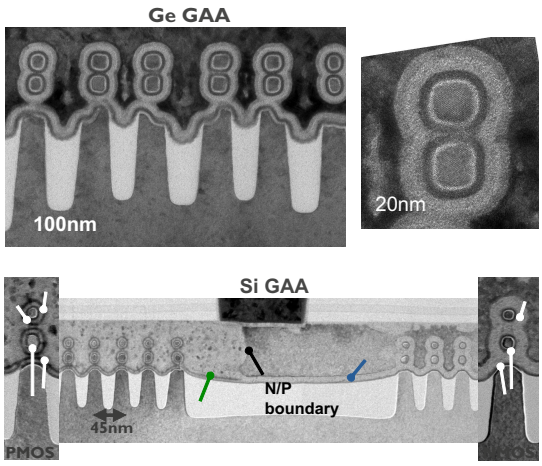


Figure 2: TEM images for cross sections of Ge (upper panel) and Si (lower panel) gate-all-around NWFETs.

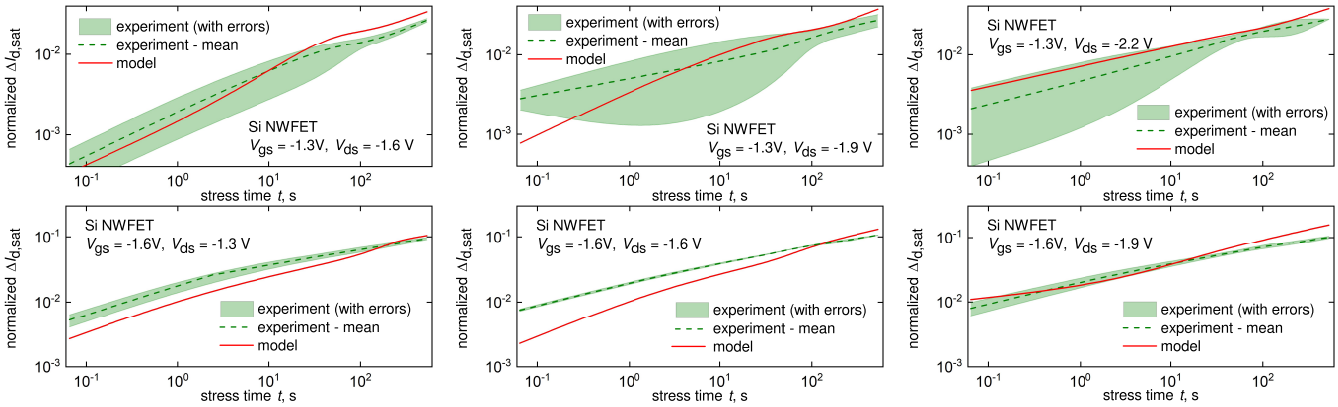


Figure 3: Normalized changes in the saturation drain current $\Delta I_{d,sat}$ acquired for Si NWFETs as functions of stress time $t$ for different combinations of $V_{gs}$ and $V_{ds}$: experimental data vs. modeling results. For each stress condition, several devices with relatively high variability were used and therefore experimental data are represented by mean values $\langle \Delta I_{d,sat} \rangle$ and continuous error bars. The model accurately captures experimental $\Delta I_{d,sat}(t)$ traces.

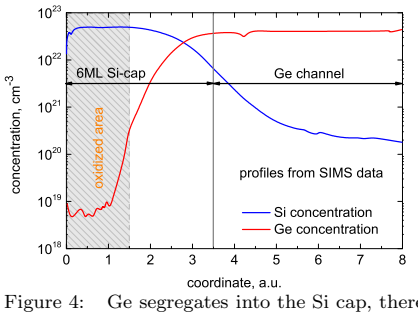


Figure 4: Ge segregates into the Si cap, thereby leading to a $Si_xGe_yO_{2(x+y)}$ layer formed after oxidation. Profiles are from SIMS data before oxidation.

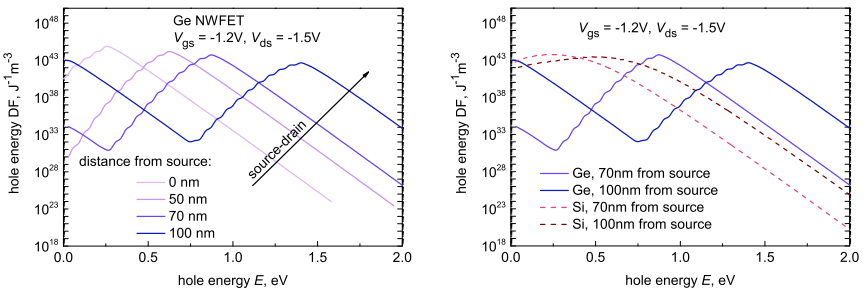


Figure 5: Hole energy DFs calculated for different positions in the Ge device at $V_{gs}$ = -1.2 V and $V_{ds}$ = -1.5 V (left panel) and comparison of drain DFs for Ge and Si FETs at $V_{gs}$ = -1.2 V and $V_{ds}$ = -1.5 V (right panel). Holes in the Ge NWFETs are hotter than those in the Si counterparts.

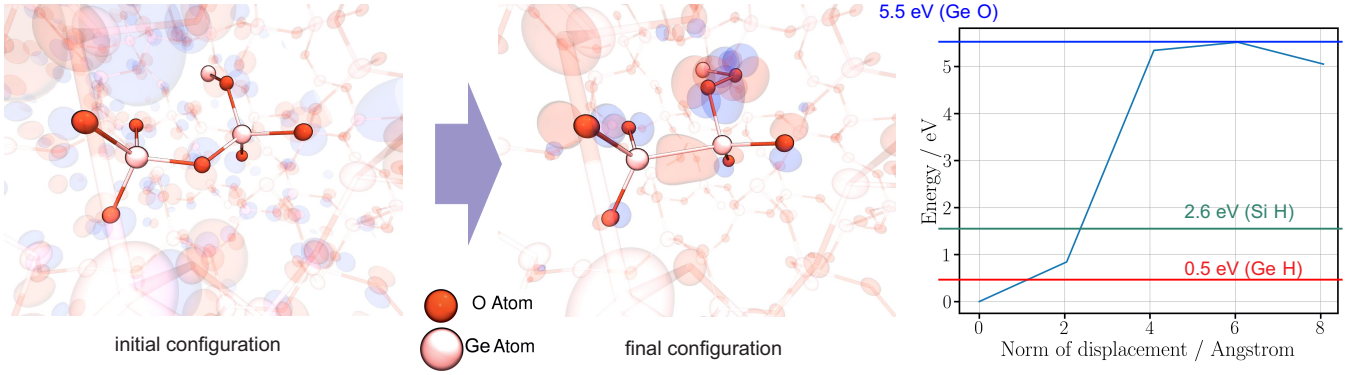


Figure 6: A schematic representation of the trap generation reaction responsible for HCD in Ge devices which transforms neutral precursors (Ge-O bonds) to electrically active defects (O-vacancies) and the reaction pathway (DFT calculations) with the activation energy of ~ 5.5 eV.

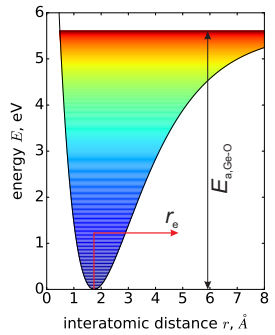


Figure 7: The Morse potential for the Ge-O bond.

**Morse potential for Ge-O bond rupture**

$$E(r) = E_{a,Ge-O}\,[1 - \exp(-\alpha(r - r_e))]^2 \qquad (1)$$

$E_{a,Ge-O}$ is normally distributed
Mean bond-breakage energy: $\langle E_{a,Ge-O}\rangle = 5.6\,\text{eV}$
Standard deviation of $E_{a,Ge-O}$: $\sigma_{E,Ge-O} = 0.8\,\text{eV}$
Steepness: $\alpha = 0.55\text{Å}^{-1}$
Equilibrium distance: $r_e \sim 1.75\,\text{Å}$
Eigenfrequency: $\nu_0 = \frac{\alpha}{2\pi}\sqrt{2\,E_{a,Ge-O}/M} \sim 10^{13}\,\text{s}^{-1}$
$M$ is the reduced mass
Eigenstates $E_i$ are not equidistantly spaced
$E_i = h\nu_0(i+1/2) - [h\nu_0(i+1/2)]^2/4E_{a,Ge-O}$
$\Delta_{i,j}$ – distance between the levels $|E_i - E_j|$

**Pauli master equation for oscillator steady-state**

$\frac{dn_i}{dt} = \sum_i A_{i,j} n_j$
$n_i$ – occupancy of level $i$, $A_{i,j}$ – transition matrix

$$A_{i,j} \equiv \begin{cases} P_{i,j} & i \neq j \\ -\sum_{k\neq j} P_{k,j} & i = j \end{cases} \qquad (2)$$

$P_{i,j}$ – rate of the $i \to j$ transition

$$P_{i,j} \equiv \begin{cases} \nu_0 + I_{i,j} & i > j \\ \nu_0 \exp(-\Delta_{i,j}/k_B T_L) + I_{i,j} & i < j \end{cases} \qquad (3)$$

$I_{i,j}$ – carrier acceleration integral for the MC-process [8]:
$I_{i,j} = \int f(E)g(E)v(E)\sigma(E-\Delta_{i,j})dE$
$f(E)g(E)$ – DF, $v(E)$ – velocity, $\sigma(E)$ – cross section

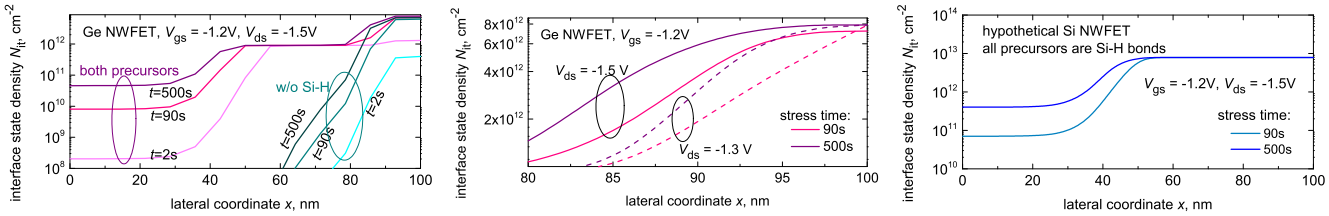


Figure 8: Interface state densities $N_{it}$ in Ge pNWFETs at a fixed combination of stress voltages $V_{gs}$ = -1.2 V, $V_{ds}$ = -1.5 V and three different stress times (left panel), at two different $V_{ds}$ of -1.3 and -1.5 V (central panel); $N_{it}$ for a *hypothetical* Si pNWFETs subjected to HC stress with the same carrier energies as the Ge device in assumption that all precursors are Si-H bonds with the concentration $N^{(0)}_{Ge-O} + N^{(0)}_{Si-H} \sim 8\times10^{12}\,\text{cm}^{-2}$ calculated for $V_{gs}$ = -1.2 V, $V_{ds}$ = -1.5 V (right panel). The lateral coordinate $x$ corresponds to the source-drain direction.

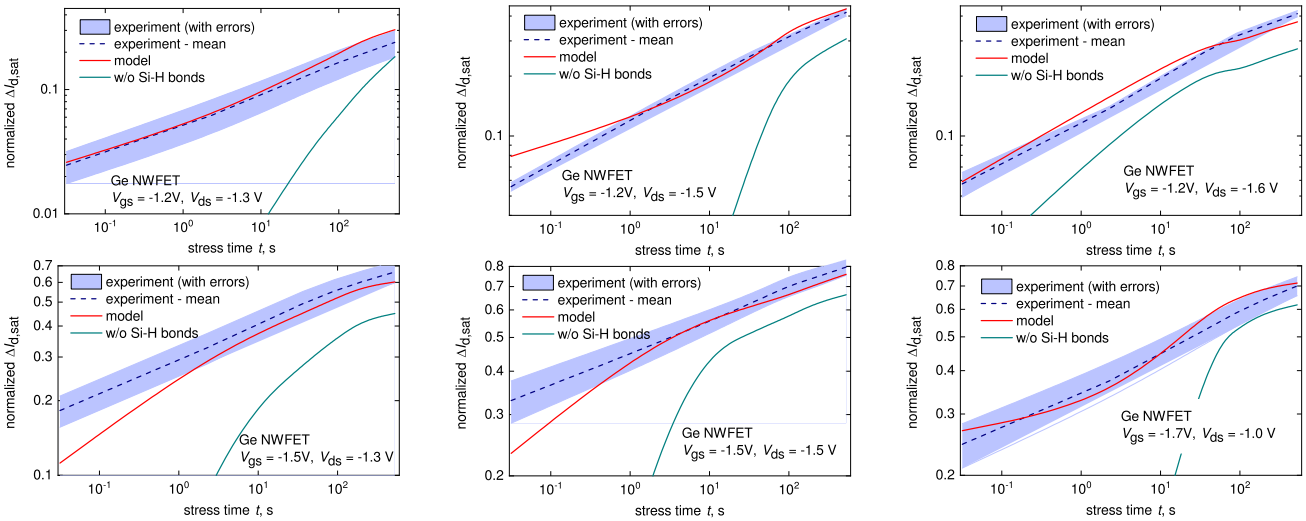


Figure 9: Normalized changes in the saturation drain current $\Delta I_{d,sat}$ acquired for Ge NWFETs as functions of stress time $t$ for different combinations of $V_{gs}$ and $V_{ds}$: experimental data vs. modeling results. For comparison, $\Delta I_{d,sat}(t)$ traces obtained by ignoring breakage of Si-H bonds are also shown. One can see that at some stress time step the HCD component related to Si-H bonds saturates (this is consistent with Fig. 8, right panel) and the slope of the $\Delta I_{d,sat}(t)$ curves is determined by rupture of Ge-O bonds. This trend suggests that a *model which considers only Si-H bonds is not capable to capture HCD in Ge transistors while our model provides good accuracy* between experimental and simulated degradation characteristics.

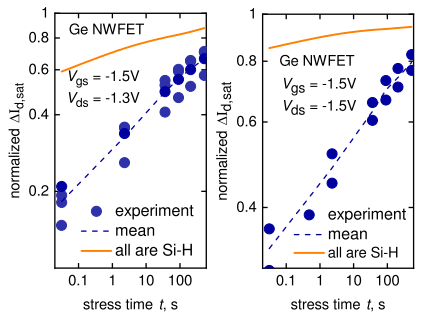


Figure 10: $\Delta I_{d,sat}(t)$ degradation traces simulated assuming that all the precursors are Si-H bonds with a concentration being a sum of both Ge-O and Si-H bond concentrations, i.e. $\tilde{N}^{(0)}_{Si-H} = N^{(0)}_{Ge-O} + N^{(0)}_{Si-H} \sim 8\times10^{12}\,\text{cm}^{-2}$.


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