CaF_2 Insulators for Ultrascaled 2D Field Effect Transistors

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Fabrication of ultrascaled 2D field effect transistors (FETs) requires 2D semiconductors with sizable bandgaps and high carrier mobilities as well as competitive insulators to separate the channel from the gate. However, so far the focus has been put on channel materials, while insulators suitable for ultrascaled 2D FETs have not been identified. The most common choice is oxides known from Si technologies, e.g. SiO_2, Al_2O_3, and HfO_2. However, despite the respectable performance of some devices, the interfaces of these oxides with 2D channels are of poor quality and contain numerous defects which degrade their performance and reliability. On the other hand, while 2D insulators such as hBN form well-defined van der Waals interfaces with 2D channels, the poor dielectric properties of hBN make it unsuitable for scaling.

As an alternative, we have recently suggested the use of calcium fluoride (CaF_2) as an insulator for 2D FETs [1]. Few-nanometers thin CaF_2 layers can be grown on Si(111) by molecular beam epitaxy (MBE) which forms an F-terminated inert surface with no dangling bonds [2]. This results in a quasi van der Waals interface with 2D materials (Fig.1a), similar to those known from hBN. Furthermore, due to its good dielectric properties, the tunnel currents through CaF_2 are lower than for most high-k oxides with equal EOT, not to mention SiO_2 and hBN [1].

The gate currents of our CVD-grown MoS_2 FETs with epitaxial CaF_2 insulators of record-small thickness of only about 2 nm (EOT less than 1nm) are small compared to the drain current (Fig.1c). Thus, already in the first bare channel prototypes we achieve competitive on/off current ratios of up to 10^7 and SS down to 90 mV/dec (Fig.2a). At the same time, the hysteresis in our devices is even smaller than in Al_2O_3 encapsulated SiO_2(25nm)/MoS_2 FETs [3] (Fig.2b). In Fig.2c we compare the normalized hysteresis widths for various technologies where only CaF_2 gives comparable results to Si/high-k FETs. In addition, we analyzed the reliability of our devices and found it to be significantly improved compared to available 2D FETs [4].

In summary, we demonstrated the feasibility of FETs with CaF_2 insulators and found that the virtually defect-free nature of CaF_2 leads to good performance, small hysteresis, and excellent reliability.

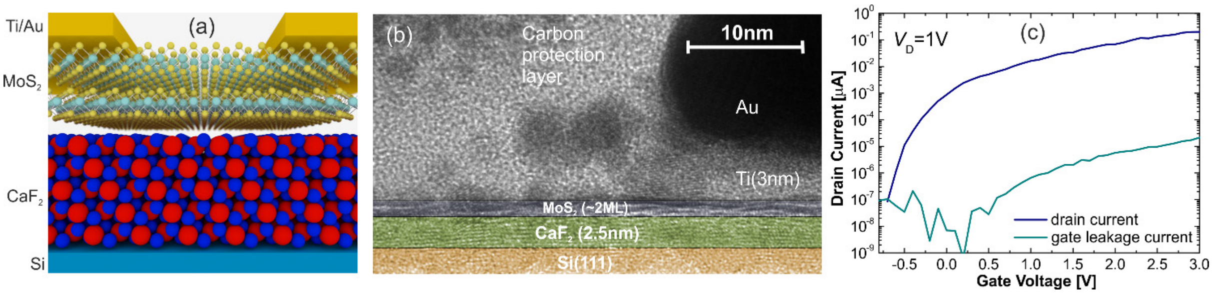

Fig.1. (a) Schematic device layout. (b) TEM image of the channel area. (c) Drain and gate current vs. gate voltage.

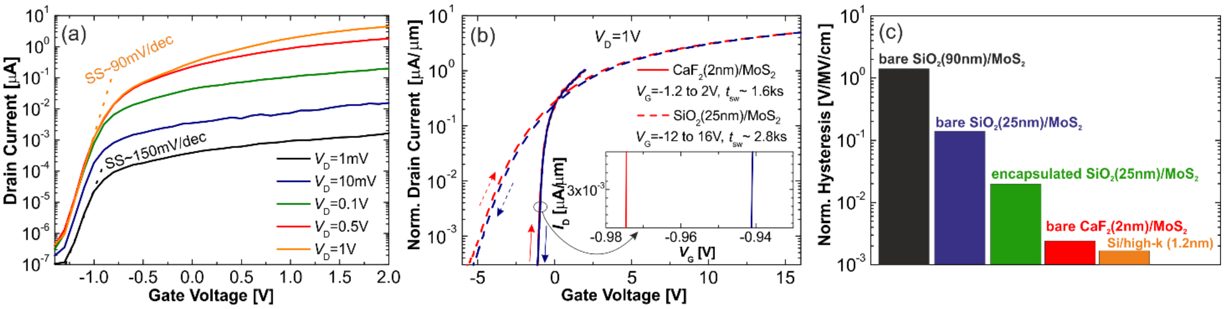

Fig.2. (a) The I_D-V_G characteristics of our CaF_2/MoS_2 FETs. (b) Slow sweep I_D-V_G characteristics of the CaF_2/MoS_2 and SiO_2/MoS_2 FETs. (c) Comparison of the hysteresis width normalized by the insulator field factor for different MoS_2 FETs and Si/high-k devices.

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[4] Yu.Yu. Illarionov *et al*, “Reliability of scalable MoS_2 FETs with 2 nm Crystalline CaF_2 Insulators”, 2D Materials, 2019.