Charge Pumping of Low-Voltage Silicon Trench Powers MOSFETs

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***Abstract*—Interface- and border-traps at the Si-SiO_2 interface are investigated in trench power MOSFETs. We show that the popular charge pumping method is not limited to conventional lateral devices but can also be applied to these more complex structures. A new approach for the localization of defects is presented, using devices with two or more differently doped areas adjacent to the Si-SiO_2 interface. Based on those doping profile variations, different areas of the interface can be assigned to particular intervals of the measured charge pumping signal. By varying the geometrical aspect ratios and the areas of the investigated devices, we demonstrate that the interface- and border-trap density on the edges of the structures is significantly higher than in the active area. Finally, challenges arising in the measurement setup are discussed.**

***Index Terms*—Low-voltage trench MOSFET, charge pumping.**

I. Introduction

DUE TO the increasing demand for more efficient DC-DC switching applications, the efficiency increase of low-voltage silicon power MOSFETs is a main driving factor in the development of these devices. Recently, trench designs have been increasingly used instead of lateral designs to obtain higher channel packing densities. Further performance improvements can be obtained by shrinking the device geometries and by using a compensating field-plate [1]. In addition to electrical performance, reliability should not only be maintained but even improved with the advancement of technology. Many electrical reliability issues originate from the quality or degradation of the oxides and their interfaces to silicon within the device structure. Charge pumping (CP) is an excellent method to investigate electrically active traps at or near the Si-SiO_2 interface and has been used for many decades, mostly on planar structures [2]. Suliman *et al.* [3] applied CP to trench devices with separated source and body contacts. Passmore *et al.* [4], [5] have also successfully implemented CP on trench devices. They developed a three-terminal CP (3T-CP) method which circumvents the issue that separate body and source contacts are, as in our case, not routinely available in trench structures.

It is commonly agreed that the charge pumping current is dominantly due to charge capture and emission events at interface states and the current due to these fast states scales linearly with the CP frequency. On the other hand, it has been shown that slower border states can also contribute to the CP signal [6]–[8], with their impact increasing at lower frequencies and higher temperatures. Our goal is to extend the understanding of the CP effect in trench structures with respect to border- and interface traps and to localize those chargeable defects. In contrast to [4] and [5], we implement the traditional CP setup instead of the 3T-CP variant. In our approach, the lack of separate body and source contacts is compensated by omitting the source implantation process step during fabrication as it impedes the measurement. As a result, no n- and p-doped areas near the investigated interfaces are shorted and thus, no carriers produced by the CP effect are annihilated.

In order to correctly interpret CP signals of the geometrically complex trench structures, it is necessary to investigate devices of varying geometries. It is shown that the edges of trench structures, consisting of two termination and trenches each (Fig. 2), behave differently from the active area. Such an edge influence is negligible in lateral structures, which are usually investigated with CP. Additionally, a spatial CP method for devices with two or more differently doped areas (n and p, n+ and n or p+ and p) adjacent to the investigated Si-SiO_2 interface is introduced. When a certain device area, which is needed for this investigation, is exceeded, issues with the measurement setup have to be tackled. Those experimental peculiarities are throughly discussed in the Appendix.

II. Structures

In the following, two device structures are discussed: Single and dual poly-silicon electrode trench MOSFETs, as shown in Fig. 1 which have their contacts embedded in SiO_2. A full device consists of multiple trenches in parallel. The field plate of the dual poly FET is usually shorted with the source/body contact, inducing a compensating field as discussed in [1] to increase the breakdown voltage. In our test structures, which have been specifically designed for interface quality analysis, the field plate can also be contacted separately. Body and source, however, are always shorted via a metal contact. Due to the presence of the n+ source doping, carriers created by

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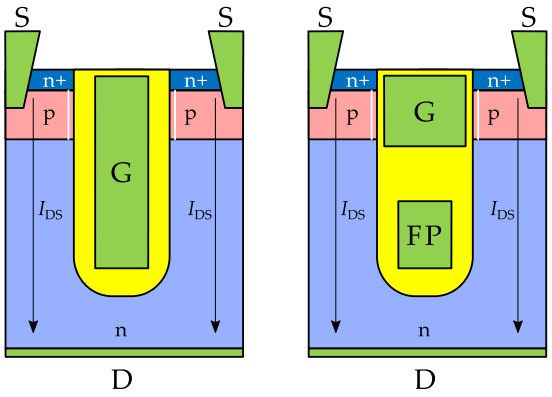


(a) Single-poly trench FET. (b) Dual-poly trench FET.

Fig. 1. Schematic cut through a trench MOSFET with the source/body (S), drain (D), gate (G) and field plate (FP) contacts. The white line indicates the channel region, green areas contacts and yellow SiO_2.

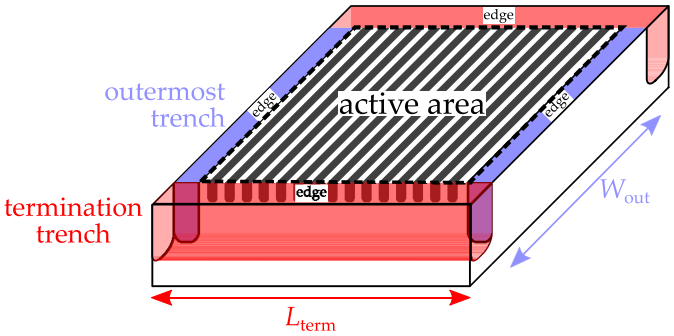


Fig. 2. Schematics of the device structure for both single and dual poly silicon electrode trench MOSFETs. The trenches in the active area (black) are depicted in Fig. 1. The edge of the structure consists of the outermost trenches (blue) and termination trenches (red). Image not to scale.

the CP effect in the p-doped body region would be annihilated by recombination processes. Therefore, the n+ doping is omitted during fabrication for those structures used to investigate the interface in the body region. This leaves the source/body contact connected to the p-doped body only. In the following, this contact will still be referred to as source/body, even if the source implant is omitted.

The edge of a complete structure consists of termination trenches perpendicular to the trenches of the active area as well as two outermost trenches (Fig. 2). The four edge trenches need to be wider as they are used to contact the gate and field plate electrodes of the active area trenches. They contain the same electrodes as the trenches of the active area and are connected to them.

III. Execution of the Charge Pumping Measurements

All measurements are performed on wafer level with a needle prober wired to a switching matrix, which is connected to a semiconductor parameter analyzer with source measurement units (SMUs) and pulse generator units (PGUs). The SMUs feature ammeters used in the measurement of the charge pumping current. In our trench devices, the gate or field plate can be pulsed and the CP current is obtained from the source/body and drain contacts. This is analogous to the well-known CP setup of lateral devices where source and drain are shorted and the CP current is obtained from the body [6], [8]–[10]. The duty cycle of the CP pulses is always set to 50%.

IV. Results

We investigated both dual and single poly-silicon electrode devices. Dual poly structures, on the one hand, allow a distinct investigation of the trench bottom due to the spatial separation of the field plate electrode. The rounded structure of this part of the trench could be prone to defects and, thus, electrically active traps. Single poly devices, on the other hand, can be used to detect degradation at all positions of the trench Si-SiO_2 interface. They lack a compensating field plate electrode, though, which is why dual poly structures are more desirable for actual product design.

A. Impact of Edges

Trench device geometries are often optimized in two dimensions, i.e., the spatial extension of the trenches is neglected. While this approach is sufficient for most parameters, it does not cover effects caused by edges. Naturally, the termination of the edges and outermost trenches may very well influence important parameters such as the breakdown voltage [11]. They also behave differently from the active area trenches due to their wider geometry. In particular, we will demonstrate that the outermost trenches have higher defect densities. It is worth noting that the term ‘edge’ always refers to the edges of the geometry as shown in Fig. 2 while ‘border traps’ is used in the context of traps in the oxide as opposed to interface traps [12].

In the following, the influence of the edges on the overall CP signal is determined by analyzing die area variations in detail. For this, trench MOSFETs with varying structure areas and geometrical aspect ratios W_{out}/L_{term} are investigated. L_{term} is the length of the termination trenches, W_{out} the width of the outermost trench. The active area is varied by changing the width W_{out}, length L_{term} or both. CP frequency sweeps are depicted in Fig. 3 to allow for an analysis of the trapping time constants. Devices with a smaller active area seem to have higher trap densities. Furthermore, the trap density decreases more significantly with increasing frequency for smaller active areas. As the layout of the active area is identical for all devices, this difference can only be caused by the edge of the structure. For a quantitative analysis of the phenomenon, the frequency dependent trap densities are fit to a logarithmic function

$$N(f) = N_{tot} - N_{bt} \log(f/1\,\mathrm{Hz}). \quad (1)$$

The parameter N_{tot} in eq. (1) is associated with the total contribution of border and interface traps while N_{bt} indicates the density of frequency dependent border traps. This is motivated by the nature of border traps causing the frequency dependence of the CP current. Their time constants are distributed with large variance [13] and thus nearly uniformly distributed over the small investigated frequency range. The contribution

of each border trap to the total trap density $N(f)$ is exponentially dependent on its time constants. The sum of those border trap contributions can therefore be well approximated by a logarithm [14]. The validity of this model can be shown by removing the offset N_{tot} (bottom inset Fig. 4) from the data and normalizing them to an arbitrary frequency f_0 which yields

$$N_{\mathrm{norm}}(f) = \frac{N(f) - N_{\mathrm{tot}}}{N(f_0) - N_{\mathrm{tot}}} = \frac{\log(f)}{\log(f_0)}. \tag{2}$$

As shown in Fig. 4, our data follow the trend predicted by (2). The noise increases with decreasing N_{bt} coefficients due to the normalization.

For most investigations, it is relevant to separate the trap density contributions of the edge and active area. These parameters scale with the geometry of the structures

$$N_{\mathrm{tot}} = N_{\mathrm{tot}}^{\mathrm{act}} + N_{\mathrm{tot}}^{\mathrm{edge}} \frac{W_{\mathrm{out}}/L_{\mathrm{term}}}{A} \tag{3a}$$

$$N_{\mathrm{bt}} = N_{\mathrm{bt}}^{\mathrm{act}} + N_{\mathrm{bt}}^{\mathrm{edge}} \frac{W_{\mathrm{out}}/L_{\mathrm{term}}}{A} \tag{3b}$$

where A is the total die area in cm^2, $N_{\mathrm{tot}}^{\mathrm{act}}$ and $N_{\mathrm{bt}}^{\mathrm{act}}$ represent the contribution of the active area in cm^{-2} and $N_{\mathrm{tot}}^{\mathrm{edge}}$ and $N_{\mathrm{bt}}^{\mathrm{edge}}$ the absolute number of traps located at the edge of the device. Both $N_{\mathrm{tot}}^{\mathrm{edge}}$ and $N_{\mathrm{bt}}^{\mathrm{edge}}$ are dimensionless. For a constant active area, an aspect ratio favoring the width of the outermost trench W_{out} will cause higher edge trap densities. Furthermore, for a constant aspect ratio, larger devices will suffer less from the impact of edge defects. With these findings, the total edge contributions can be estimated as 80%, 33% and 5% of N_{tot} while the border trap edge contributions are 92%, 52% and 17% of N_{bt} for the 0.01 mm^2, 0.1 mm^2 and 0.5 mm^2 structures, respectively (top inset Fig. 4). When all edge traps are subtracted from the data, the active area contribution of all structures can be calculated. The results are plotted in full lines in Fig. 3 and are consistent with the assumption that the active area trap densities should be similar for all device sizes. Small deviations of the remaining active area contribution is attributed to noise in the data.

Investigations of the oxide of trench MOSFETs should therefore always consider this edge influence before any conclusions about the active area are drawn. It is also important to ensure that the CP signal saturates in the constant base level and constant high level measurements before conclusions on the density of interface traps can be drawn as the saturation indicates complete trap filling in all areas that can be accessed by CP.

B. Localization of Stress-Induced Traps via Doping Variation

CP allows to resolve the position of stress induced degradation with respect to differently doped silicon areas. To show the potential of this method, we investigate the single poly-silicon electrode trench FET without n+ source implantation.

We use the common constant base level and constant high level CP measurements, where the high level or base level of the pulse, respectively, is swept. The constant level must be set such that the channel region of the MOSFET is in deep accumulation or inversion. The CP current increases rapidly

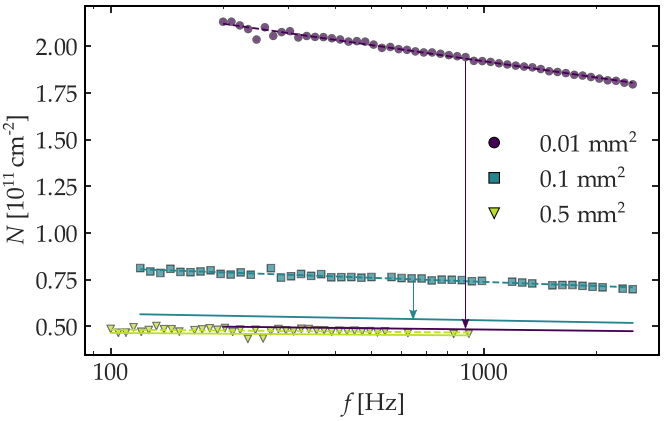


Fig. 3. Comparison of the trap density N of dual poly trench MOSFETs over the frequency for varying active die areas. The CP pulse with a base level of −15 V, amplitude of 30 V and slope of 0.2 V/µs has been applied to the field plate. Thus, only contributions of the n-doped drain are detectable. All devices have n+ source implantation. The geometrical aspect ratios $W_{\mathrm{out}}/L_{\mathrm{term}}$ were approximately 2.12, 2.78 and 1.00 for the 0.01 mm^2, 0.1 mm^2 and 0.5 mm^2 structures, respectively. Dashed lines represent the fit according to (1), full lines the calculated active area trap contribution.

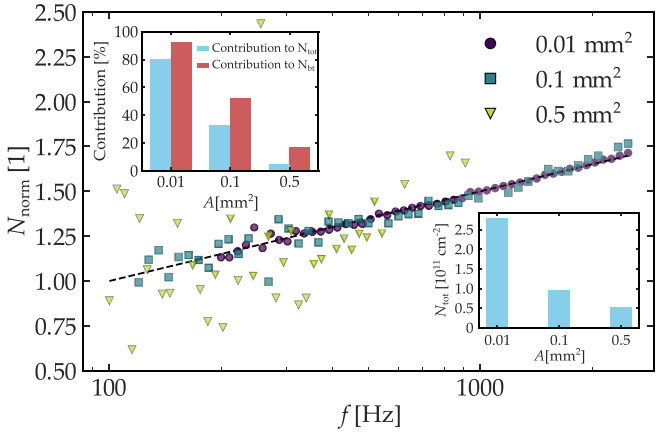


Fig. 4. Data from Fig. 3 normalized to $f_0 = 100$ Hz according to eq. (2). The dashed black line represents $\log(f)/\log(f_0)$. Inset bottom: Total contribution of border and interface traps N_{tot}. Inset top: Total trap contributions of the edge to N_{tot} and border trap contributions of the edge to N_{bt} in devices of different size.

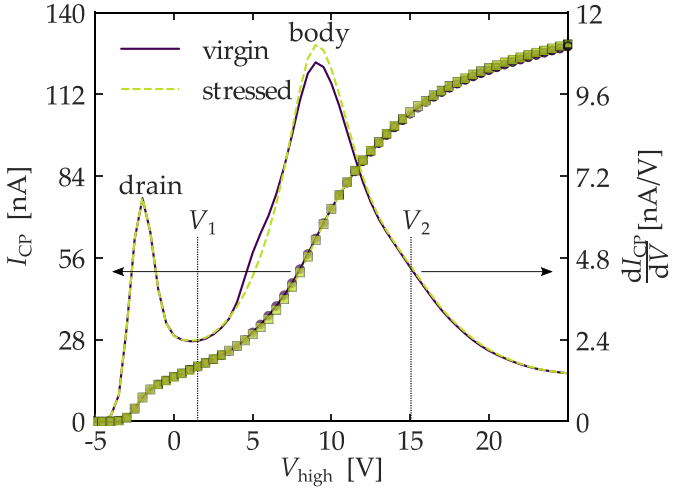
when inversion or accumulation of a doped area adjacent to the pulsed Si-SiO$_2$ interface is reached by the voltage level and the holes and electrons can reach the doping areas of the respective carrier type. For each doping profile, a peak in the derivatives of the constant high level CP current and constant low level CP current is observed. Those 'doping-induced peaks' can be described by the derivative of the CP current [15]

$$I_{\mathrm{CP}} = W\, q\, f \int_0^{L_{\mathrm{eff}}(V_{\mathrm{low}}, V_{\mathrm{high}})} N_{\mathrm{it}}(x)\ \mathrm{d}x \tag{4}$$

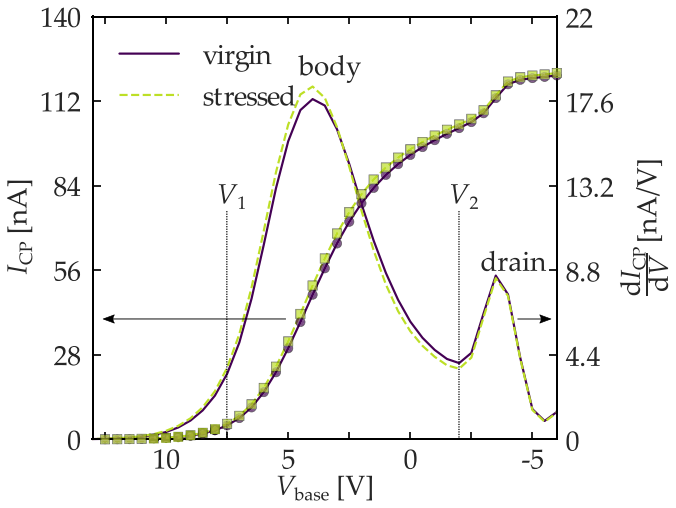
which yields [15]

$$\frac{\mathrm{d}I_{\mathrm{CP}}}{\mathrm{d}V} = q\, f\, N_{\mathrm{it}}(L_{\mathrm{eff}})\, W\, \frac{\mathrm{d}L_{\mathrm{eff}}}{\mathrm{d}V}. \tag{5}$$

In (4) and (5) W represents the width of the CP active area, f the CP frequency, q the elementary charge, $N_{\mathrm{it}}(x)$ the trap

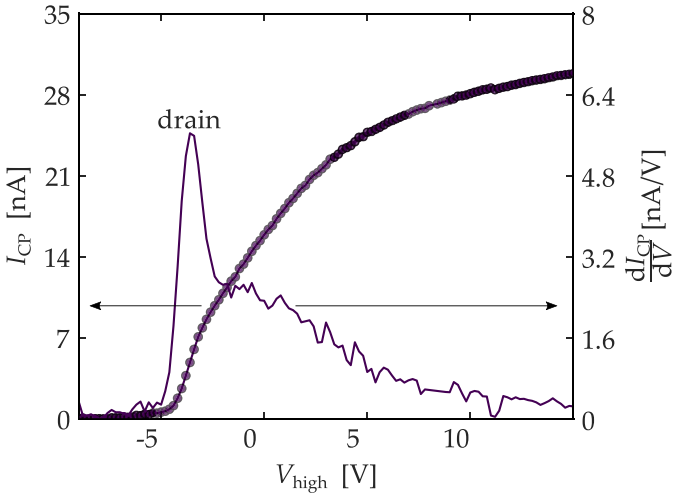


(a) Constant base level CP signal on a single poly trench device with a base level of -6 V. By sweeping the high voltage, the doping-induced peak of the body is associated with the threshold voltage of the p doping. The threshold voltage must be positive, thus the right peak is the body peak.

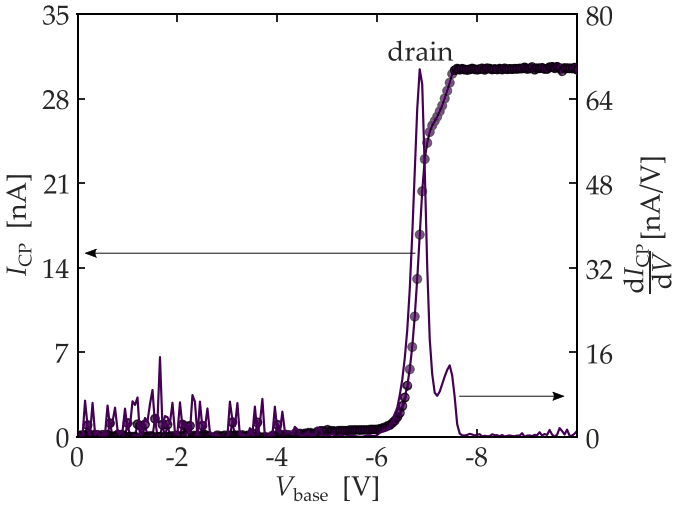


(b) Constant high level CP signal on a single poly trench device with a high level of 20 V. By sweeping the base voltage, the doping-induced peak of the drain is associated with the threshold voltage of the n doping. The threshold voltage must be negative, thus the right peak is the drain peak.

Fig. 5. Constant high/constant low level CP measurement of a single poly trench MOSFET at a CP frequency of 100 kHz and a slope of 12.5 V/µs. The symbols mark the measurement data, lines are the derivatives. The borders of the body peak used in the evaluation in the text are labeled with V_1 and V_2. The devices were stressed by applying 6.8 V to the gate and 20 V to drain for 14 hours. Source was grounded.



(a) Constant base level CP signal on a dual poly trench device with a base level of -10 V.



(b) Constant high level CP signal on a dual poly trench device with a high level of 15 V. By sweeping the base voltage, the doping-induced peak of the drain is associated with the threshold voltage of the n doping. The threshold voltage is negative as expected.

Fig. 6. Constant high/constant low CP measurement on the field plate of a dual poly trench MOSFET at a CP frequency of 500 Hz and a slope of approx. 26.3 V/ms. The symbols mark the measurement data, lines are the derivatives. Only the drain doping-induced peak is visible. A constant offset was removed with the method described in Section V.

density at the position x along the Si-SiO$_2$ interface and $L_{\text{eff}}(V_{\text{low}}, V_{\text{high}})$ the length of the CP active area. In (5), V equals V_{low} for constant high level CP or V_{high} for constant low level CP. The terms $W\,\mathrm{d}L_{\text{eff}}/\mathrm{d}V$ and $N_{\text{it}}(L_{\text{eff}})$ in (5) show the origin of two kinds of peaks, respectively: The extension of the active CP area $W\,\mathrm{d}L_{\text{eff}}/\mathrm{d}V$ causes doping-induced peaks [15]. If a stress does not generate local but uniform degradation, the increase of the CP current manifests itself in a change of the already present doping-induced peaks. They either increase in width, amplitude or both. The second kind of peak predicted by (5) is caused by a sudden increase of $N_{\text{it}}(L_{\text{eff}})$. It is due to variations in trap densities along the Si-SiO$_2$ interface. Such a so-called 'degradation peak' appears after strongly localized defects are caused by stress. We could not identify a degradation peak in our investigations due to uniform degradation, i.e., constant $N_{\text{it}}(L_{\text{eff}})$ after stress. Rather, the preexisting doping-induced peaks increased in height and width.

Constant base level and constant high level CP of the aforementioned single poly-silicon electrode trench structure shows two doping-induced peaks in the derivative of those signals. This is due to the two differently doped silicon areas bordering the oxide interface. In our approach we measured the device before and after a stress. The conditions were similar to a hot-carrier degradation stress: 6.8 V were applied to the gate with an additional drain bias of 20 V for 14 hours. The measurement results are plotted in Fig. 5. The two doping-induced

peaks, which appear in both constant base and constant high measurements, are labeled according to their respective doping area. For both constant high and constant low CP signal derivatives, the drain doping-induced peaks do not change by stress, while the body doping-induced peaks increase in width and hight. This confirms that the major contribution of the degradation was indeed caused near the top of the trench. It is worth noting that this is not due to a change of the material doping but an increase of the defect density.

As expected, a dual poly structure, where CP measurements are performed on the field plate electrode only, shows the drain doping-induced peak (Fig. 6). The measured dual poly device incorporates the n+ source doping to ensure that no contributions from the body are observed. Due to oxide thickness variations at the trench bottom, a second small drain doping-induced peak appears in the constant high CP measurement (Fig. 6(b)). This is because a small area with a thicker oxide reaches full inversion of the adjacent n-type silicon only at slightly higher voltages. Another observation that can be made in the constant base and constant high CP measurements is the deviation of the width of the doping-induced drain peaks between the constant base and constant high CP measurement. The peak in the constant high CP measurement is much narrower because the field plate electrode only covers the interface in the n-doped region. While the high level (i.e., electron accumulation in the n-region) is kept constant, the connection of the p-region, the source for holes, is pinched off until the base level reaches sufficiently low voltages (approx. -7 V). At this point, the surface potentials at the interface allow for full inversion and accumulation during the base and high level of the CP pulse, respectively. The much wider doping-induced peak in the constant base measurement also conceals the second small peak observed in the constant high CP measurement.

For a quantitative description of the trap density of the interface area adjacent to the doping causing the respective peak, we integrate over the peaks in the derivative of the constant high or constant low signal. Assuming that $N_{\mathrm{it}}(L_{\mathrm{eff}})$ is constant, i.e., $N_{\mathrm{it}}(L_{\mathrm{eff}}) = \overline{N_{\mathrm{it}}}$ one obtains

$$\int_{V_1}^{V_2} \frac{\mathrm{d}I_{\mathrm{CP}}}{\mathrm{d}V}\,\mathrm{d}V = qf\,\overline{N_{\mathrm{it}}} \int_{V_1}^{V_2} W\,\frac{\mathrm{d}L_{\mathrm{eff}}}{\mathrm{d}V}\,\mathrm{d}V, \tag{6}$$

where V_1 and V_2 are the lower and upper boundary of the respective doping-induced peak (see also Fig. 5). The integral

$$A_{\mathrm{dop}} = \int_{V_1}^{V_2} W\,\frac{\mathrm{d}L_{\mathrm{eff}}}{\mathrm{d}V}\,\mathrm{d}V \tag{7}$$

can be associated with the area of the interface adjacent to the respective doping. Inserting equation (7) into (6) yields

$$\overline{N_{\mathrm{it}}} = \frac{I_{\mathrm{CP}}(V_2) - I_{\mathrm{CP}}(V_1)}{qf\,A_{\mathrm{dop}}} \tag{8}$$

This means that, in a certain doping volume, the increase of the CP current is directly proportional to the trap density in this area. This increase of I_{CP} is directly proportional to the trap density in the area defined by V_1 and V_2. In our single poly structure, we can therefore easily calculate the trap densities generated by the stress. An extraction from the constant base level CP method yields a trap density increase of 2.97×10^8 cm^{-2}, while the constant high level CP method gives 3.47×10^8 cm^{-2} for the same structure. The difference of 14% can be attributed to the limited resolution of the digital ammeter. For V_1 and V_2, two respective points are considered. The first one is located at the local minimum between doping induced peaks. The second point is located at a position where the derivative of the CP current does not differ before and after stress. This choice of V_1 and V_2 allows for the analysis of different local parts of the device. In this example, only the body volume is analyzed as the signal changes only there with stress. For more precise allocation of V_1 and V_2 to respective doping areas, TCAD simulations can be used.

It is worth noting that this method is not limited to trench structures. It can be applied to all devices where multiple CP doping-induced peaks are observed.

Previously [15], a different method for spatial localization of stress generated defects, application of reverse bias, was used. This method cannot be applied to our problem because a reverse bias on the body diode reduces the active area for CP to investigate the spatial distribution of defects on the interface [15], [16]. This method is only applicable if two conditions are fulfilled: On one hand, an additional degradation peak must appear after stress in the derivative of the constant high or constant base measurement. This peak is supposed to vanish after a reverse bias is applied during the measurement because the reverse bias induces a space charge region which deactivates the CP mechanism. On the other hand, it is necessary to reach the areas of the interface where the degradation has taken place with that space charge region and map the reverse bias to the location of it. The first condition depends on the degradation mechanism itself and is not fulfilled in our case. The second condition may be hard to fulfill in complex two-dimensional structures unless the measurement results are supported by TCAD simulations.

V. Conclusion

We have shown that charge pumping (CP) measurements on trench devices are meaningful only if the influence of the edge contribution is properly understood. As in all CP measurements, the constant low and constant high level signals should saturate to ensure that all areas of the device are scanned and complete trap filling can be assumed. The edges of the particular structures are shown to contribute significantly to the measurement of the trap density. Usually, the active area is more relevant than the edge, thus, bigger structures are generally better suitable. By variation of the active area and aspect ratio of our devices we have been able to quantitatively determine the contributions of edge and active area. The upper limit for device sizes is governed by the measurement equipment. The measurement range must be set according to eq. (9) as steep slopes cause high charging and discharging currents that must be covered by said range. This degrades the

signal-to-noise ratio as the CP signal is obtained by averaging over these (dis)charging currents.

The CP theory was also extended by a spatial profiling method that relies on variation in doping type and concentration. It has been shown that even a very small degradation impact can be assigned to the spatial position along the interface of the geometrically complex trench structure.

APPENDIX
IMPROVING CHARGE PUMPING RESULTS

This section provides some general considerations to improve the accuracy of CP measurements. They are not only limited to trench MOSFETs but can be applied all kinds of traditional CP measurements.

Most authors measure the CP current on the body contact. We recommend to connect ammeters to both the body and the source/drain terminals to verify the plausibility of the signal. As dictated by Kirchhoff's law, both meters must show the same value with opposite sign if oxide leakage currents are negligible, i.e., for thick oxides. A deviation is not only an indicator for an unexpected leakage current through the oxide but can also show issues with the measurement units. Leakage currents can be easily detectable by DC measurements whereas deviations caused by the measurement units can result from incorrect ammeter ranging settings, wrong averaging approaches as well as offset errors. The range adjustment and a possible method to remove offset errors are discussed hereafter.

A. Correct Measurement Range Setting of the Ammeters

The correct setup of the measurement range of the ammeters used in the CP experiment must be ensured at all times. In order to achieve this goal, all current contributions must be examined. Peak charging and discharging currents of the gate capacitance at steep slopes can negatively affect the measurement of the CP current I_{CP}. The total current flow during CP consists of (dis)charging currents of the MOS-capacitance and the CP current itself. I_{CP} is obtained by averaging over a few hundreds of periods where the aforementioned charging and discharging currents cancel out. In most SMUs, the measurement range is not only supposed to cover the magnitude of the averaged signal, but also its peak values. Typically, averaged CP currents are orders of magnitudes smaller than the peak charging currents of the MOS-capacitance investigated. This can cause significant noise in the CP signal. The signal to noise ratio is worse for short rise and fall times as the CP signal has to be obtained from the charging and discharging of the MOS structure by averaging over those currents. These MOS (dis)charging currents are proportional to the slope $\mathrm{d}V/\mathrm{d}t$. Even though steeper slopes make it possible to obtain a slightly larger CP signal due to the enlargement of the measurable band gap, the charging current of the MOS-capacitance increases far more significantly. CP currents only increase logarithmically with the slope for a constant density of states $D(E)$, while MOS charging currents increase linearly with the slope. For a correct range setting of the ammeter, the lower boundary for the current measurement range I_{range} can be approximated by

$$I_{\mathrm{range}} > C_{\mathrm{MOS}} \frac{\Delta V}{t_{\mathrm{r/f}}^{\mathrm{min}}} \tag{9}$$

where ΔV is the pulse amplitude and $t_{\mathrm{r/f}}^{\mathrm{min}}$ the shortest rise- or fall time of the CP pulses. A constant capacitance, where $C\,\mathrm{d}V = I\,\mathrm{d}t$ can be applied, is assumed. The range chosen according to a minimum rise and fall time must, on the other hand, also have sufficient resolution to resolve the averaged CP signal. Therefore, it can be necessary to sacrifice a small section of the measurable band-gap by increasing rise- or fall times in order to be able to use a smaller range with a better resolution.

B. Offset Error Removal of Charge Pumping Currents

Ammeters are inevitably afflicted with offset errors which become especially significant when the selected measurement range is orders of magnitudes larger than the CP current signal. It is possible to remove this deviation by executing the CP measurement with either the source/body or the drain contact floating. As minority carrier generation time is too large compared to the period of the CP signal, minority carriers can be neglected over majority carriers in the CP measurement. This means that either holes or electrons - depending on which contact is left floating - will be missing in the CP process. Thus, no physical net CP current can be present on the remaining non-floating contact. Therefore, the actual measured current on that contact must be caused by the measurement setup and can later be subtracted in the complete CP measurement.

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