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Cryogenic Characterization of NH_3 Post Oxidation Annealed 4H-SiC Trench MOSFETs

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Abstract. We employed the thermal dielectric relaxation current method (TDRC) for the cryogenic characterization of ammonia (NH_3) post oxidation annealed 4H silicon carbide (4H-SiC) trench MOSFETs. We studied differences and similarities between annealing in nitric oxide (NO) and NH_3. In NO and NH_3 annealed trench MOSFETs, the same type of traps was found near the conduction band edge of 4H-SiC. The TDRC-signal consists of two peaks caused by interface states with a thermal emission barrier of 0.13 eV and near interface traps (NITs) with an emission barrier of approximately 0.3 eV. Significantly more interface traps close to the conduction band edge were found for the NH_3 annealed devices compared to the NO annealed ones. Our TDRC results indicate that NH_3 post oxidation anneal (POA) affects trap levels in a different way than NO POA.

Introduction

SiC is an attractive material for high-power MOSFETs because of its high breakdown field strength. As opposed to other wide band gap semiconductor materials its native oxide is silicon dioxide (SiO_2) [1], which allows to transfer processing knowledge from silicon technology. One drawback of SiC MOSFETs is that currently achieved inversion channel field effect mobilities are still far lower [1, 2] than the bulk mobility because of trapping at and near the SiC/SiO_2 interface. In order to reduce trapping, a POA can be performed. At the moment, nitric oxide (NO) is the most common annealing gas leading to significantly improved MOSFET performance and reliability [3, 4, 5]. However, it has been reported that an even higher mobility can be achieved by NH_3 anneal [6]. In order to identify the nature of the defects responsible for the mobility degradation and to investigate differences in trap level densities between NO and NH_3 annealed devices, we investigated n-channel trench MOSFET test structures using TDRC measurements. So far, other research groups have applied TDRC only to n-MOS structures or lateral MOSFETs [7, 8, 9]. Also, NH_3 annealed MOS structures were mainly studied using capacitance voltage measurements (cf. [10]). In [10], a reduction of deep interface states was reported for NH_3 pre-oxidation annealed capacitors on 6H-SiC with additional N_2 or N_2O POA compared to samples without the NH_3 pre-oxidation anneal.
In this work, we show that the same kind of trapping states are present in NO and NH_3 annealed trench MOSFETs. However, both gases affect these traps differently.

Experimental

Differently annealed n-channel trench MOSFETs were fabricated on 4° off-axis, n-type 4H-SiC substrates. The SiO_2 gate oxide was deposited by chemical vapor deposition with subsequent POA in N_2, NO or NH_3 (NH_3 (1): $t_1$min @ T_1°C, NH_3 (2): $t_2 = 3t_1$ @ $T_2 = T_1 + 15\%$). A cross-section of the studied trench MOSFETs can be found in Fig. 1.

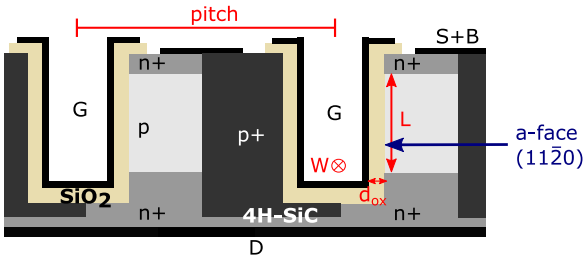


Fig. 1: Cross-section of the studied trench MOSFET test structures. The channel forms in the (11$\bar{2}$0) crystal plane (a-face). L channel length, W channel width, G gate contact, S source contact, B bulk contact and D drain contact.

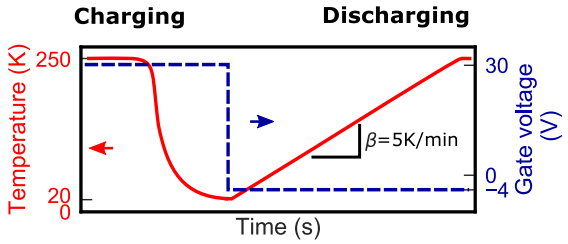


Fig. 2: TDRC measurement principle: $V_{\mathrm{ch}} = 30\,\mathrm{V}$ is applied to the gate while the temperature is decreased from $T = 250\,\mathrm{K}$ to $20\,\mathrm{K}$ (approx. 1 hour). Then, the bias is switched to $V_{\mathrm{dis}} = -4\,\mathrm{V}$ and the temperature gradually increased with $5\,\mathrm{K/min}$.

The TDRC measurement procedure is indicated in Fig. 2. Source and drain of the MOSFETs are grounded and the gate is charged with $V_{\mathrm{ch}} = 30\,\mathrm{V}$ at a temperature of $250\,\mathrm{K}$. During charging, electrons are attracted to the SiC/SiO_2 interface where they can get captured in available trapping states. During the end of the charging process, the temperature is lowered to $20\,\mathrm{K}$ to slow down the emission of charges from their trapped state. Then, the gate bias is switched to $V_{\mathrm{dis}} = -4\,\mathrm{V}$ (depletion) and the temperature is increased with a constant heating rate $\beta = 5\,\mathrm{K/min}$. At certain temperatures, the thermal energy approaches the emission barrier and trapped electrons are thermally re-emitted into the 4H-SiC conduction band, leading to temperature dependent peaks in the gate displacement current $I(T)$. This signal can be transformed into a density of states D_{it} and an emission barrier $E_{\mathrm{C}} - E_{\mathrm{t}}$ as described in [11], assuming the validity of Shockley-Read-Hall theory. For trench MOSFETs, the signal not only results from the channel region but from the whole trench SiC/SiO_2 interface. This area was extracted from CV curves at $V_{\mathrm{G}} = 15\,\mathrm{V}$. The apparent channel mobility as an indicator of device performance was determined using the method of Ghibaudo [12].

Results and Discussion

The results of the TDRC measurements are shown in Fig. 3. In general, the TDRC signal of all tested trench MOSFETs consists of two peaks representing two different trap levels. Peak A corresponds to interface traps with an emission barrier of $0.13\,\mathrm{eV}$, trap level B to near interface traps (NITs) with an emission barrier of $0.3\,\mathrm{eV}$. NITs were first described by Afanas'ev et al. [13]. The type of traps was determined by the variation of charging (V_{ch}) and discharging (V_{dis}) voltage (cf. [8, 14], Fig.4a and 4b). All studied POAs show the same qualitative results. The measured density of trap states in both peaks increases with higher V_{ch} indication a larger amount of trapped electrons. For more negative V_{dis}, the devices show an increasing TDRC signal in peak A and a decreasing signal in peak B. This behavior is attributed to interface traps and NITs [8].
The highest interface state density D_{it} in peak A is measured for N_2 annealed MOSFETs. For NO and NH_3 annealed devices, we see a reduced D_{it} near the conduction band edge compared to the inert anneal in N_2. This supports results by McDonald et al. [15] and Soejima et al. [6] who observed

similar behavior on different lattice planes. We therefore conclude that NO and NH_3 POAs passivate interface traps (peak A) to a certain extent. Additionally, both NH_3 POAs lead to higher D_{it} than NO with $D_{it}^{NO} < D_{it}^{NH_3\ (2)} \leq D_{it}^{NH_3\ (1)}$. We can thus clearly see that NH_3 has a less effective annealing effect on this trap level than NO. Regarding the density of NITs (peak B), no reliable conclusions can be drawn with TDRC measurements because most NITs can tunnel directly into the conduction band and are therefore not detectable with state-of-the-art measurement equipment [8].
From earlier work, we expect a weak correlation between D_{it} (peak A) and the apparent channel mobility among other factors [14]. A reduced D_{it} compared to the N_2 annealed MOSFET comes with an improved mobility. However, a higher mobility was measured for NH_3 (2) than for NH_3 (1) (cf. Fig. 5) even though the density of interface states of peak A is similar to NH_3 (1). Therefore, only a very weak correlation between peak A and the mobility may exist. Generally, a higher density of interface states in peak A was found after NH_3 POA than after NO POA and a lower one than after N_2 POA (Fig. 5 and Fig. 3). From this, it can be concluded that peak A only partly contributes to the mobility degradation and that there are other factors, e.g. other trap levels, which have a stronger influence on the channel mobility. We assume a trap level with $E_C - E_t > 0.13\,\text{eV}$ to mainly cause the mobility degradation. Because [16] reports that traps close to the conduction band edge cause a low mobility, we suggest closer research on the correlation between NITs (peak B) and the apparent channel mobility with other measurement techniques.

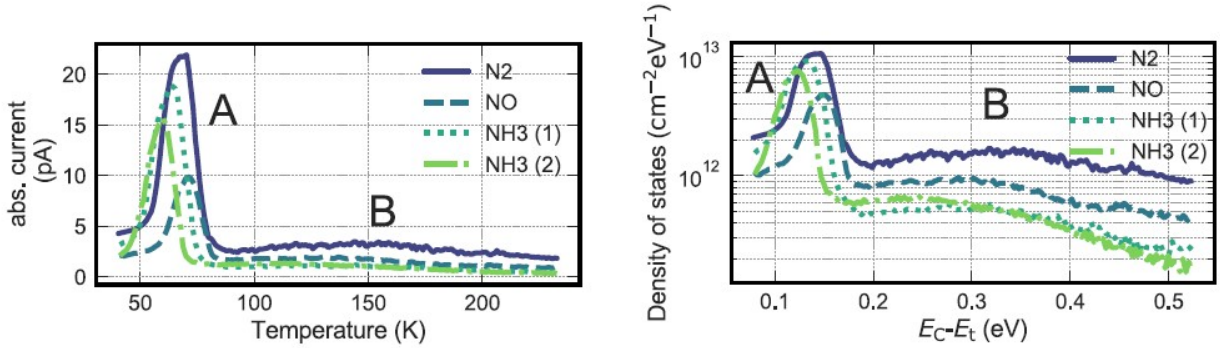
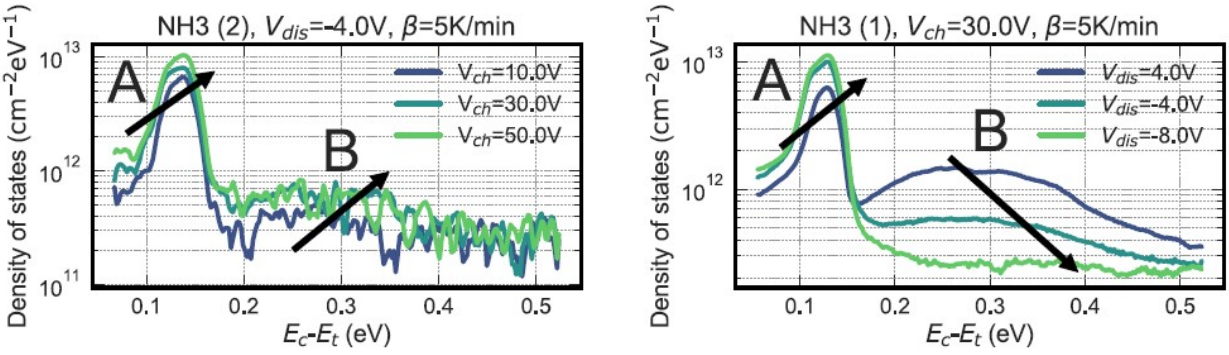


Fig. 3: TDRC results of differently annealed trench MOSFETs. Left: $I(T)$ plot. Right: D_{it} vs. emission barrier calculated from the TDRC $I(T)$-plot.



(a) Variation of charging voltage.

(b) Variation of discharging voltage.

Fig. 4: Energy distribution for a variation of the measurement parameters. All POAs lead to qualitatively similar results.

Summary

TDRC measurements were carried out for trench MOSFETs annealed in different ambient. NO, NH_3 and N_2 annealed trench MOSFETs all show the same trap levels near the 4H-SiC conduction band edge. An interface trap level with an emission barrier of 0.13 eV (A) and a near interface trap level with an emission barrier of 0.3 ± 0.1 eV (B) were found. In trap level A, we see a higher trap density for the NH_3 annealed devices compared to NO even though NH_3 (2) has a better apparent channel mobility. NH_3 (2) suffers from slightly less interface states than NH_3 (1) but has a strongly improved channel mobility. Therefore, peak A only has a very weak contribution to the degradation of the channel mobility. The main annealing effect of NH_3 POA, which leads to an improved channel mobility, is not identified so far. It presumably takes place in peak B (no conclusion possible with TDRC) or towards midgap. NO and NH_3 POA lead to the reduction of the interface trap level (peak A), however, the annealing effect on NITs (peak B) cannot be evaluated with TDRC.

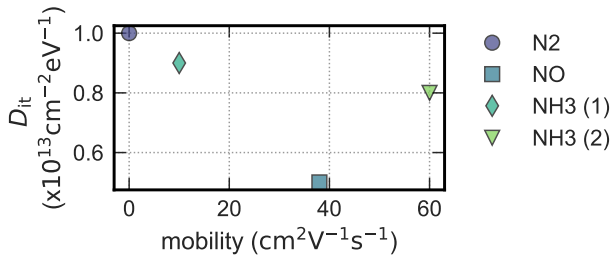


Fig. 5: Anti-correlation between D_{it} of peak A and Ghibaudo mobility for annealing in different ambients.

Acknowledgment

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