Simulation of the Effects of Postimplantation Annealing on Silicon Carbide DMOSFET Characteristics

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***Abstract*— Technological control of doped regions is exceptionally important for all semiconductor devices. For the wide bandgap semiconductor silicon carbide, the activation state of dopants is determined by the postimplantation annealing step which consequently affects device operation and characteristics. We perform a detailed analysis of the effects of postimplantation annealing on the electrical characteristics of silicon carbide-based double-implanted metal–oxide–semiconductor field-effect transistors. We predict acceptor and donor concentrations according to various annealing times, temperatures, and total doping concentrations. The findings are used as a basis for the combined process and device simulations, providing the capability to characterize a reference device and predict the annealing dependence of output and transfer characteristics. Our results are in excellent agreement with the experiments and show precisely how annealing steps influence channel potential, drain current, ON-state resistance, and threshold voltage. Finally, we predict device characteristics based on the annealing variables, showing a high sensitivity of the threshold voltage on annealing time and temperature.**

***Index Terms*— Annealing, double-implanted metal–oxide–semiconductor field-effect transistor (DMOSFET), electrical activation, implantation, silicon carbide.**

I. Introduction

SILICON-based power electronics exhibits several limitations for high-voltage, temperature, and frequency applications. Wide bandgap semiconductors, in particular, silicon carbide (SiC), are especially suitable to replace traditional silicon in order to increase device properties with higher switching frequency, blocking voltages, and current densities [1]. However, fabricating SiC devices is very challenging: many processes are not fully understood [2], which prevents using the material to its full potential [3]. Understanding and optimizing, in particular, the annealing process is essential for SiC devices and research is currently focused on the annealing step's influence on oxide quality [4], stacking faults [5], and Hall density and mobility [6]. The latter two are correlated with the (active) carrier concentration, which is investigated in this work.

The most widely used technology for selective doping of SiC is ion implantation [6]–[8], which requires a postimplantation annealing treatment in order to repair crystal defects and to increase the activation of dopants [2], [9]. SiC-based metal–oxide–semiconductor field-effect transistors (MOSFETs) are very desirable for power electronics due to the excellent balance between conduction and switching loss at blocking voltages of less than 3.3 kV [3]. In order to optimize the performance of SiC power double-implanted MOSFETs (DMOSFETs)—a particularly attractive power electronics device [3]—typically four design variables are considered [10]–[12]: drift region doping, spreading layer doping, and junction width and doping. These variables, however, do not capture the effects which would occur during device fabrication annealing steps. In order to further optimize the involved processes and resulting device characteristics, it is therefore critically important to accurately predict the effects of postimplantation annealing [13].

In this work, we present a comprehensive study of the impact of the dopant-specific annealing step on key DMOSFET parameters, such as threshold voltage (V_{th}), ON-state resistance (R_{on}), and breakdown voltage (V_{B}). We utilize our recently developed empirical time-dependent activation model [14] to perform a study based on an extensive series of coupled process and device simulations, which were compared to experimental results.

II. Method

We investigate the impact of the annealing process on device parameters by incorporating an empirical activation model into the combined process and device simulations. In this section,

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we present the activation model, discuss the series of simulated fabrication steps, and describe the employed device models.

A. Activation Model

The transient model for electrical activation of dopants in SiC is described with a differential equation and represents the reaction of the dopants' activation process [14]. The concentration of electrically active dopants C_{act} is expressed as a function of the reaction rate coefficient k_{r}, the total implanted dopant concentration C_{tot}, the annealing temperature T_{A}, and the annealing time t_{A}, such that

$$\frac{dC_{\mathrm{act}}}{dt} = -k_{\mathrm{r}}(T_{\mathrm{A}})\left(C_{\mathrm{act}} - C_{a,f}(T_{\mathrm{A}}, C_{\mathrm{tot}})\right). \tag{1}$$

The active dopant concentration in the steady-state

$$C_{a,f}(T_{\mathrm{A}}, C_{\mathrm{tot}}) = \frac{C_{\mathrm{tot}}}{1 + \frac{C_{\mathrm{tot}}}{C_{\mathrm{ss}}(T_{\mathrm{A}})}} \tag{2}$$

is governed by C_{ss}, which is related to the solid solubility of the impurities in SiC. The model parameters k_{r} and C_{ss} follow an Arrhenius law:

$$A = Z\,\exp\left(-\frac{E_{\mathrm{a}}}{k_{\mathrm{B}}T_{\mathrm{A}}}\right), \quad A = C_{\mathrm{ss}} \text{ or } k_{\mathrm{r}} \tag{3}$$

with the exponential prefactor Z, the activation energy E_{a}, and the Boltzmann's constant k_{B}. Our model is calibrated for aluminum (Al), which is the preferred acceptor-type dopant species in SiC for low-resistivity applications [6], [15] and the commonly employed donor-type dopant phosphorus (P) [16]. We have investigated extensively experimental data of various postimplantation steps of Al and P impurities in SiC from more than 70 studies and identified a subset which reflected identical SiC polytypes and crystal orientations as well as similar implantation steps, annealing steps, and measuring techniques. The fabrication steps generally include polishing and capping techniques, which significantly improve the surface quality [1]. We assume that surface roughness and interface (e.g., SiC-oxide) quality are not affected by postannealing implantation steps [14]. The resulting model parameters are given in Table I. The calibrated model provides the capabilities to estimate the minimally required T_{A} and t_{A} for a certain C_{tot} to acquire full (i.e., above 90%) activation of the implanted SiC region. The ratio of electrical activation $R_{\mathrm{act}} = C_{\mathrm{act}}/C_{\mathrm{tot}}$ as predicted by our model is illustrated in Fig. 1.

The differing parameters for Al and P reflect the different chemical solid solubilities and activation kinetics [7], [8], which are highly important to consider in devices which rely on the implantation of multiple species. One of the general implantation-related issues of SiC is that the rate of the dopant activation after high dose implantation (above 10^{18} cm^{-3}) decreases significantly [2], [17], that is, saturates, which limits the achievable ratio of electrical activation. For the optimization of the annealing process with regard to thermal budget, process time, and the desired device characteristics, it is essential to accurately predict the saturation region of activation [14], [15].

The common approach to overcome the saturation limitation is to employ elevated temperatures during the implantation process ("hot implantation") [8], [17]. However, implantation temperatures as high as 1000 °C are required to enhance the activation efficiency to achieve nearly full activation [8]. In order to guarantee consistent and reliable calibration of the postimplantation model (1) and (2), the parameters C_{ss} and k_{r} (given in Table I) originate from numerous studies employing implantation temperatures up to 650 °C [14]. Hence, we assume idealized implantation process conditions in which the postimplantation annealing is the dominant process and the implantation temperature does not significantly affect the activation efficiency.

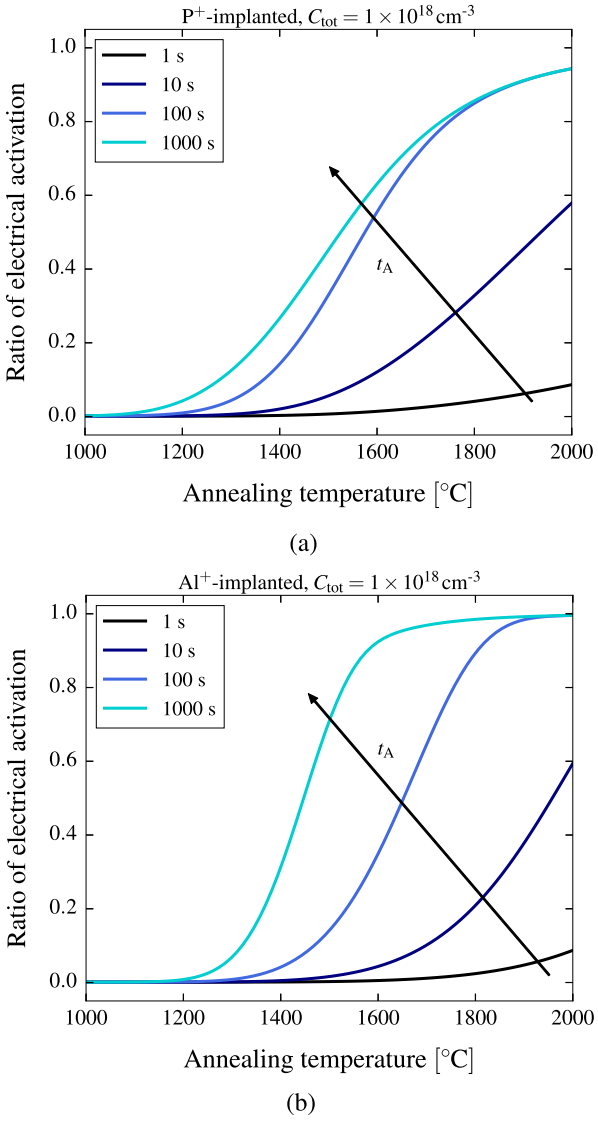


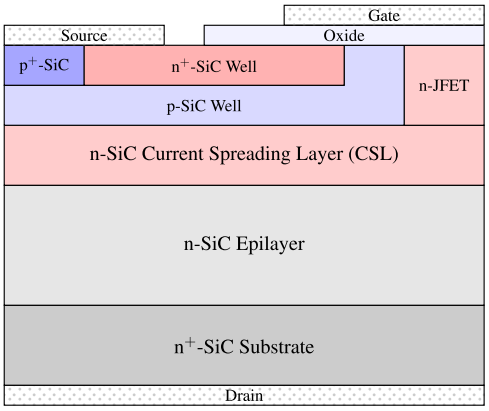
Fig. 1. Ratio of electrical activation as predicted by the transient annealing models (1) and (2) for (a) P- and (b) Al-implanted 4H-SiC as function of annealing temperatures for different annealing times. For both species, a total implanted concentration $C_{\mathrm{tot}} = 10^{18}\ cm^{-3}$ is assumed.

B. Process Modeling

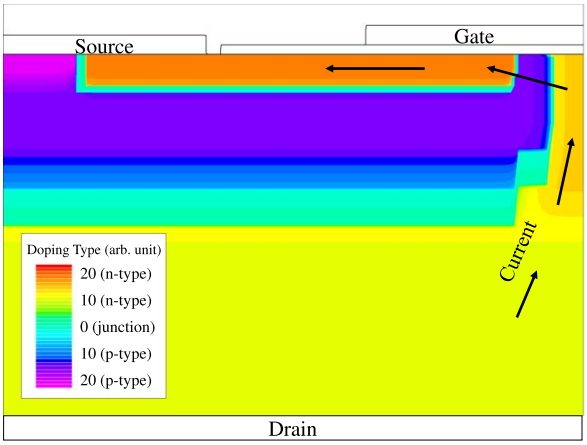
The transient annealing model (1) and (2) has been implemented into Silvaco's Victory Process simulator [18], allowing to simulate the fabrication of advanced 4H-SiC DMOSFETs. In this paper, we consider the low-voltage short-channel

TABLE I
ARRHENIUS PARAMETERS OF THE CHARACTERISTIC RATE AND SOLID SOLUBILITY FOR THE P- AND AL-IMPLANTED 4H-SIC, AS PRESENTED IN [14]

	k_r		C_{ss}	
Dopant	Z (1/s)	E_a (eV)	Z (cm^{-3})	E_a (eV)
P	1.09×10^2	1.38	7.17×10^{23}	2.09
Al	9.72×10^4	2.72	1.21×10^{26}	2.58



(a)



(b)

Fig. 2. (a) Schematic cross section of the examined 4H-SiC DMOSFET. This vertical power device is fabricated by implanting Al (p-type) and P (n-type) into an n-doped epitaxial layer. (b) Cross section of the device structure after process simulation, illustrated with the net concentration of implanted dopants. Arrow: path of the conduction current.

4H-SiC power DMOSFET presented by Saha and Cooper [19], which is schematically shown in Fig. 2(a). The geometry (e.g., layer thickness and implantation mask dimensions) and doping profiles follow the reference fabrication process presented by Saha and Cooper and include the following steps.

1) Epitaxial growth of a lightly n-doped 6-μm epitaxial layer ($N_D = 10^{16}$ cm^{-3}).
2) Epitaxial growth of a 0.9−μm n-doped layer ($N_D = 10^{17}$ cm^{-3}). This layer forms the current spreading layer (CSL) and the junction FET (JFET) region in the final device.

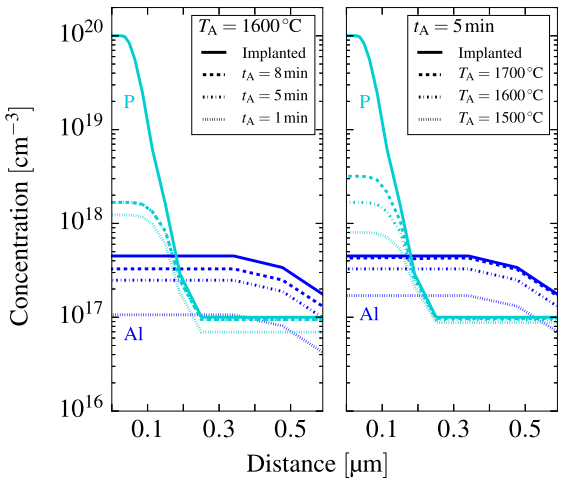


Fig. 3. Doping profiles for various annealing times (temperatures) for $T_A = 1600\,°C$ ($t_A = 5$ min). Solid (dashed) lines: implanted (electrically active) doping profile. Due to the high-implanted P concentrations, the activation efficiency is strongly limited by the annealing temperature. For the implanted Al dopants, this is not the case, because the total implanted concentration is two orders of magnitude lower.

3) Formation of the implantation mask (SiO_2).
4) Ion implantation of Al and P to form the p-well, highly doped n-well, and the highly p-doped region below the source contact. The implantation energies are chosen to produce a p-well with a depth of 0.6 μm, which is also illustrated in Fig. 3 (solid lines).
5) Annealing step, characterized by t_A and T_A, employing the activation model (1) and (2). The surface is capped with SiO_2.
6) Thermal oxidation to form the gate oxide with a thickness of 50 nm.
7) Metal deposition to form the contacts (source, gate, and drain).

Fig. 2(b) depicts the resulting device structure after process simulation, which is characterized by a vertical current path and a defined channel region which can be electrostatically controlled by the gate contact. The considered DMOSFET fabrication process relies on implantation and activation of two species, Al and P. Thus, the activation model is employed for both. In contrast to silicon, where introduced dopants strongly diffuse during the annealing process, the diffusion coefficients for Al and P in 4H-SiC are exceptionally low [1]. Hence, the geometry of doped regions can be precisely controlled by ion-implantation process parameters, that is, ion energy and dose. However, the electrical properties of the device are strongly affected by the annealing step. Therefore, subsequent device simulations are performed to investigate these effects.

C. Device Modeling

The concentration of electrically active dopants is an essential quantity for the fabricated DMOSFET device. In order to investigate the impact of the annealing step, device simulations are performed with Silvaco's Victory Device (VD) simulator [18]. The simulator solves the continuity equations using the drift diffusion model in conjunction with several

TABLE II
MODELING PARAMETERS USED FOR DEVICE SIMULATIONS IN VD [18]

Model	Statement	Parameters
	General Setup	
Drift Diffusion	(Default)	
Fermi-Dirac Statistics	models fermidirac	
Two-Level Incomplete Ionization [20]	(Default)	P: calibrated in VD Al: ea.cubic $= 2 \times 10^{-1}$ eV ea.hexagonal $= 2 \times 10^{-1}$ eV
	Bandgap Modeling	
Universal Energy Bandgap Model (Varshni) [23]	(Default)	eg300 $= 3.235$ eV egalpha $= 3.3 \times 10^{-2}$ eV K^{-1} egbeta $= 1 \times 10^{5}$ K
Slotboom and De Graaf Bandgap Narrowing Model Calibrated for 4H-SiC [21, 24]	models bgn	calibrated in VD
	Mobility Modeling	
Uhnevionak Combined Mobility Model for 4H-SiC [26]; p values reproduce Caughey Thomas Model	mobility altcvt.n altcvt.p	calibrated in VD for electrons alt.n.delta $= 1.5 \times 10^{12}$ cm^2 V^{-1} s^{-1} alt.p.mubp1 $= 1.25 \times 10^{2}$ cm^2 V^{-1} s^{-1} alt.p.mubp2 $= 0$ alt.p.mumin $= 1.59 \times 10^{1}$ cm^2 V^{-1} s^{-1} alt.p.alpha $= -5.0 \times 10^{-1}$ alt.p.exp1 $= -2.15$ alt.p.exp3 $= 1.0$ alt.p.exp4 $= 3.4 \times 10^{-1}$ alt.p.nref $= 1.76 \times 10^{19}$ cm^{-3}
High-Field Mobility (Canali) [32] 300 K	models fldmob	vsatn $= 2.2 \times 10^{7}$ cm s^{-1} vsatp $= 1.0 \times 10^{7}$ cm s^{-1} betan $= 1.2$ betap $= 1.0$
Anisotropic Mobility [33]	mobility	n.anisotropic $= 1.2$
	Generation and Recombination	
Shockley-Read-Hall [27]	models srh	taun0 $= 1.0 \times 10^{-9}$ s taup0 $= 1.0 \times 10^{-9}$ s
Auger Recombination [28]	models auger	augn $= 1.0 \times 10^{-29}$ cm^6 s^{-1} augp $= 1.0 \times 10^{-29}$ cm^6 s^{-1}
Impact Ionization Selberherr [29, 30]	impact selberherr	impact: an1,2 $= 3.44 \times 10^{6}$ cm^{-1} ap1,2 $= 3.5 \times 10^{6}$ cm^{-1} bn1,2 $= 2.5 \times 10^{7}$ V cm^{-1} bp1,2 $= 1.7 \times 10^{7}$ V cm^{-1} betan $= 1.0$ betap $= 1.0$
Interface Traps (Effective acceptor-like trap; density and e.level fitting parameters)	inttrap	acceptor: density $= 3.0 \times 10^{12}$ cm^{-2} e.level $= 7.5 \times 10^{-2}$ eV

bandgap, mobility, and recombination models with 4H-SiC-specific parameters. A summary of the model parameters used in this paper is given in Table II.

Due to 4H-SiC being a compound semiconductor, the dopants can reside on hexagonal and cubic lattice sites, which is accounted for by a two-level incomplete ionization model for the donor impurity P [20]. The associated donor ionization energies for cubic and hexagonal sites are 90and 50 meV, respectively [20]. We employ a single-level incomplete ionization model for the acceptor impurity Al with a corresponding ionization energy of 200 meV [1]. The incomplete ionization model provides the density of ionized dopants and is based on the active dopant concentration predicted by the

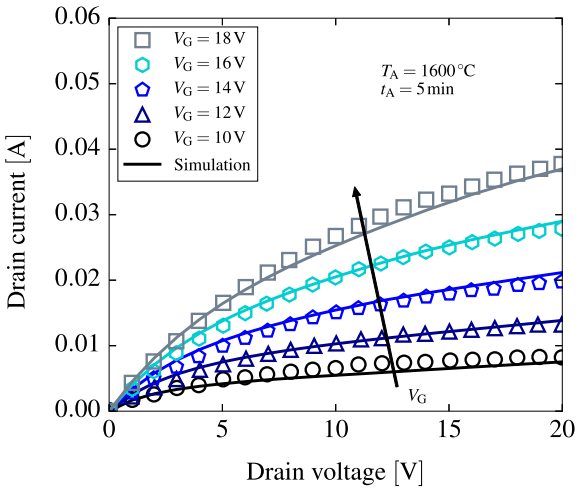


Fig. 4. Simulated and experimentally observed DMOSFET output characteristics for the annealing process parameters and device geometry as presented by Saha and Cooper [19]. The simulations accurately reproduce the experimentally obtained characteristics for any given gate voltage from 10 to 18 V.

postimplantation annealing model (1) and (2) during process simulation.

The temperature-dependent bandgap is accurately described by calibrating Varshni's model [22] to experimental data [23]. Bandgap narrowing is taken into account by using the model of Slotboom and De Graaff [24], calibrated for 4H-SiC with parameters as given by Lades [21]. For the considered DMOSFET, the model of Slotboom and De Graaff results in around 1% error in the threshold voltage compared with the more elaborate bandgap shrinkage model by Lindefelt [25]. A comprehensive mobility model, which has been specifically proposed for 4H-SiC, is the Uhnevionak *et al.* [26] model, which also takes mobility anisotropy induced by the 4H-SiC's hexagonal crystal structure into account. Furthermore, Shockley–Read–Hall [27] and Auger recombination [28], as well as impact ionization [29], [30], are considered. The material interface between 4H-SiC and SiO_2 exhibits interface state densities, which are typically two orders of magnitude higher than the densities associated with the Si–SiO_2 interface [31]. The resulting interface charge strongly affects the electrostatics in the channel region and is modeled by introducing interface traps with the energetic distribution and density as free parameters. Both quantities are kept constant for all annealing conditions in order to isolate the impact of the postimplantation annealing process on the threshold voltage of the final DMOSFET, while minimizing the influence of interface effects.

III. RESULTS

Based on the models and parameters discussed in Section II, we show here the coupled process and device simulation results to examine the influence of the annealing variables (i.e., time and temperature) and the implanted impurity concentration on the DMOSFET's device characteristics. Fig. 4 shows the DMOSFET's output characteristics for operation at room temperature. Our simulations accurately reproduce the data presented by Saha and Cooper [19] for any given gate voltage (V_G) from 10 V to 18 V. The experimental data have been

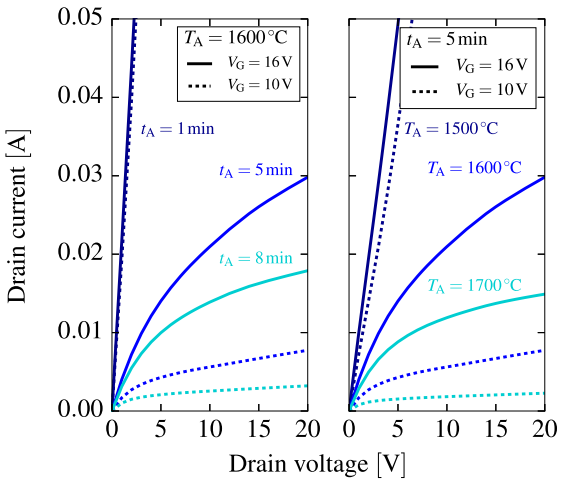


Fig. 5. Output characteristics for various annealing times (temperatures) for $T_A = 1600$ °C ($t_A = 5$ min). The output characteristics are very sensitive to the annealing variables, which is a consequence of a shift of the threshold voltage (see also Fig. 7). In addition, two annealing configurations which result in purely resistive behavior are shown. In these cases, the active acceptor concentration is insufficient to form the n-p-n sequence.

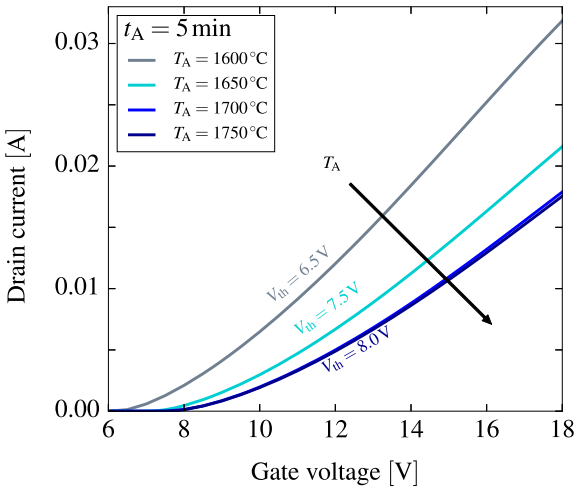


Fig. 6. Transfer characteristics for different annealing temperatures. Elevated annealing temperatures result in higher electrically active Al concentration in the channel, which causes a threshold voltage shift.

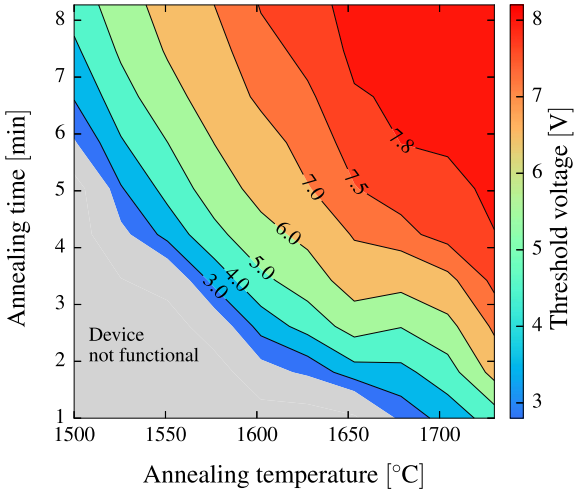


Fig. 7. Phase diagram of the threshold voltage as a function of annealing temperature and annealing time. The gray region is the phase space of the annealing variables which result in nonfunctional devices.

obtained by annealing the implanted regions at 1600 °C for 5 min. In addition, we obtain the specific ON-state resistance of approximately $R_{ON} = 7\ \Omega\ cm^2$ (for $V_G = 16\ \ V$ and drain voltage $V_D = 20$ V) and a breakdown voltage of $V_B = 1$ kV, which is consistent with experimental data [19].

The depth profiles of the devices are shown in Fig. 3, which illustrate the impact of the annealing variables on the doping profiles. The first depth profile plot investigates the annealing time at constant $T_A = 1600$ °C and the second investigates the annealing temperature for constant $t_A = 5$ min. Elevated annealing temperatures (above 1600 °C) increase the active Al and P concentration. If the annealing parameters are not sufficient (annealing time too short or temperature too low), the consequent low active acceptor concentration in the channel is too small to form an n-p-n sequence. Hence, a potential barrier between the n^+-well and the JFET region is missing, which makes the device nonfunctional. With that, the output characteristics of the 4H-SiC DMOSFETs are investigated in detail for various annealing times and temperatures, shown in Fig. 5. The results show, for example, that the annealing steps of 5 min at 1500 °C and 1 min at 1600 °C are not sufficient to fabricate a functional DMOSFET due to very low active Al concentration. In this case, the active Al concentration (p-type) is lower than the epitaxial CSL's donor concentration. Consequently, a purely resistive behavior is observed, which cannot be controlled by the gate voltage. By optimizing these process variables, one is able to find the optimal balance between the desired drain currents and efficient annealing configurations.

We have characterized the transfer properties as a function of annealing temperatures, shown in Fig. 6. The transfer characteristic shows the threshold voltage (V_{th}) shift of 1.5 V, when increasing the annealing temperature from 1600 °C to 1700 °C. This is caused by the enhanced active acceptor concentration in the channel region, which determines carrier depletion and inversion. Likewise, extended annealing times enhance the threshold voltage.

The transient annealing model enables a comprehensive investigation of the impact of the annealing parameters on the threshold voltage. We have performed coupled process and device simulations for more than 200 annealing conditions. Fig. 7 visualizes the threshold voltage for annealing temperatures from 1500 °C to 1750 °C and annealing times up to 8 min. The obtained results confirm that choosing suitable annealing conditions is essential for the DMOSFET's viability. The gray regions in Fig. 7 correspond to the set of annealing variables which result in purely resistive devices lacking gate control capabilities. The threshold voltage is mainly determined by the active Al concentration in the channel, giving rise to a strong impact of annealing time and temperature on the transfer characteristics. For instance, given a constant annealing temperature of 1600 °C, enhancing the annealing time from 3 to 7 min leads to a threshold voltage shift of approximately 3 V which significantly alters the device operation.

IV. Conclusion

Our recently proposed transient model to predict activation of Al and P impurities in SiC has been calibrated and verified to accurately reproduce experimental SiC DMOSFETs under various conditions. This approach enables optimizations of SiC-based devices considering annealing process variables, that is, annealing time and temperature, and total implanted concentration. We have performed process and device simulations using Silvaco's Victory Process and VD simulators to characterize numerous SiC DMOSFETs. The obtained output characteristics of the devices have been compared to experiments, which not only shows a very good agreement for any given gate voltage, but also clearly highlights the importance of accurate activation models to correctly predict the device characteristics. The impact of the annealing temperature and time has been demonstrated to be crucial for DMOSFET operation. In particular, we have shown that the threshold voltage is very sensitive to the annealing conditions, e.g., increasing the temperature during the annealing step from 1600 °C to 1700 °C results in a threshold voltage shift of 1.5 V. Our investigations corroborate the need for a transient activation model which enables optimizing the annealing step.

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