

Similarities and Differences of BTI in SiC and Si Power MOSFETs

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Abstract— Bias temperature instability (BTI) is a serious reliability concern not only in 4H silicon carbide (4H-SiC) power MOSFETs, but also in Si technology. Even though previous studies presented large BTI drifts for some SiC devices compared to Si, we show that BTI in modern SiC may become uncritical by improved device processing. As will be shown, NBTI can even be reduced to a similar drift level as in Si power MOSFETs. Furthermore, we demonstrate that BTI in SiC and Si devices share many features such as a comparable time and voltage evolution. Thus, BTI in SiC MOSFETs can be described with the same empirical and simple physical models, and is therefore as predictable as for Si-based devices. In addition, this indicates that BTI in SiC and Si power MOSFETs is caused by the same physical origin of the degradation.

Index Terms—Bias temperature instability, power MOSFET, reliability, silicon carbide, silicon devices, silicon dioxide.

I. INTRODUCTION

The wide-bandgap semiconductor, silicon carbide (SiC), is an emerging material for high-power electronics because of its attractive material properties. Compared to conventional silicon (Si), SiC offers a wider bandgap, and therefore a higher breakdown field, a higher thermal conductivity and a conveniently high electron mobility [1], which makes it especially attractive for high-voltage classes. Furthermore, SiC forms silicon dioxide (SiO₂) as native oxide, as is the case for Si, allowing for thermal oxidation.

For both technologies, bias temperature instability (BTI) is a challenge, as it may lead to an increased on-resistance, a decrease in efficiency, an increase in leakage currents, and other undesirable effects [2–4]. BTI is observed under both positive (PBTI) and negative (NBTI) gate bias stress. Even though BTI has been widely investigated, there is currently no generally accepted physical PBTI model available [5, 6], although intrinsic electron trapping is a very likely trigger mechanism [7, 8]. Therefore, the classic power-law description (cf. [9]) is still commonly used for lifetime predictions. Even though BTI is also present in Si-based power devices, it has been reduced to a very low level. In contrast, BTI in SiC has only been studied for the last decade [10]. Some literature reports significantly higher threshold voltage shifts for SiC than those known for Si devices (cf. [2] for example). In contrast, we will show that BTI in SiC

power devices can be reduced to an uncritical level by process optimization.

In order to obtain comparable BTI measurements, industrial standards for reliability testing of Si devices have been established, such as e.g. JESD22 [11] and its extension AEC-Q101 [12], however, allowing for delays between device stress and readout. Recent studies have shown that the existing standards developed for Si as listed above can lead to ambiguous drift results depending on the delay between stress and readout when applied to SiC MOS devices [13–17] due to a relatively large electron trapping component at interface states. Therefore, an alternative well-defined measurement sequence is needed to separate the reversible and fast-recovery device drift from the electron trapping component in order to obtain reliable and reproducible results, which are (nearly) independent of the readout timing.

So far, most research groups focus on BTI in either Si devices or SiC devices. In contrast, in this paper, we directly compare BTI of Si superjunction MOSFETs and SiC trench MOSFETs for the first time, using an adapted measurement sequence, which delivers reliable readouts for both SiC and Si only weakly dependent on the time of readout. Based on this, we will show that BTI drift in SiC power MOSFETs can be significantly reduced by appropriate device processing. Additionally, indications were found that the quasi-permanent PBTI component in SiC/SiO₂ and Si/SiO₂ likely has the same origin.

II. EXPERIMENT

A. Studied Devices

Si superjunction power MOSFETs were compared to differently processed 4H-SiC n-channel trench power MOSFET test structures. In all studied devices, the SiO₂ gate oxide thickness is comparable (>50 nm). The SiC trench MOSFET test structures were produced on commercial Si-face 4H-SiC substrates using an industrial process. The conductive channel forms only on one side of the trench along the (11 $\bar{2}$ 0) crystal plane (a-face). A schematic cross section of the studied SiC devices can be found in [18]. The studied SiC MOSFETs received different post-oxidation anneals (POA) in order to

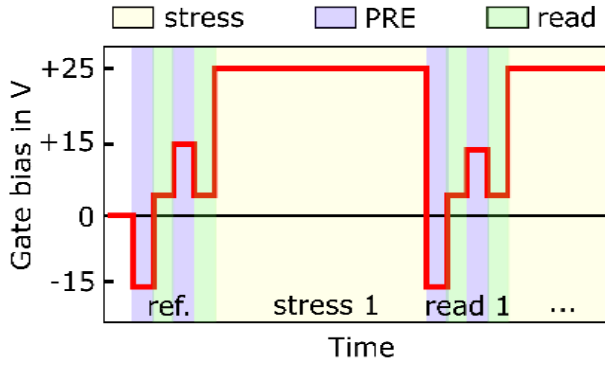


Figure 1: Preconditioning pattern used for BTI measurement. Before the readout (1 s, green), a negative (−15V) and a positive (+15V) preconditioning pulse (PRE, purple, 1 s each) is added to define the charge state of the interface traps. Hysteresis effects can be monitored as the difference between the readout after positive and negative preconditioning. After the full preconditioning sequence, a stable readout value is obtained.

reduce trapping effects and improve the device performance and reliability. The POAs differ in annealing ambient, temperature and time (SiC_(A), SiC_(B), SiC_(C)).

B. Measurement Principle

As reported in the literature [2, 3, 13–17], standard measure-stress-measure (MSM) BTI readout patterns, or industrial measurement standards developed for Si technology, can lead to ambiguous drift readouts depending on the delay between stress and readout. While the effect of readout timing has been known in Si technology for a long time [19], the measured threshold voltage shift ΔV_{th} of SiC MOSFETs depends strongly on the readout timing and the device history due to fully reversible hysteresis effects. In order to obtain more stable V_{th} drift readouts for both SiC and Si devices which are less sensitive to short delays, a preconditioning pattern consisting of an inversion and accumulation pulse (−/+15 V) was introduced before each readout, as suggested in [13] (Figure 1). This ensures a comparable interface trap occupancy before each readout. With this procedure, fast and fully reversible charging/discharging effects such as the “sub-threshold sweep hysteresis” [20] are removed so that mainly the quasi-permanent drift component is monitored. In this way, the drift depends only weakly on readout timing. Nevertheless, the drift of the hysteresis can still be monitored by monitoring the voltage shift between readout after the positive and negative preconditioning pulse [13]. Here, however, we focus on the quasi-permanent drift component.

In order to compare the threshold voltage drifts in SiC and Si power MOSFETs, BTI stress with different gate stress biases between 10 V and 40 V and at different temperatures (30°C–200°C) was applied (S and D grounded). Note that most stress conditions lie significantly above the data-sheet specifications for SiC ($V_{GS}=15$ V, 175°C) and are therefore significantly higher than needed for standard applications. The readout was performed with the help of a switching matrix in the gated-diode (GD) configuration, i.e. gate (G) and drain (D) contacts

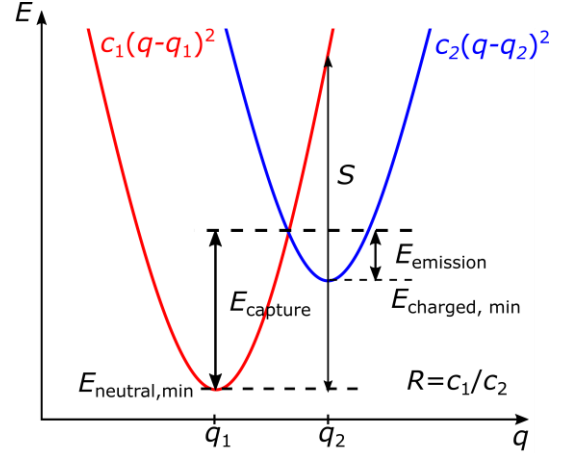


Figure 2: Effective 2-state NMP model with the relaxation energy S , the ratio of the curvatures R , the barrier for the capture or emission process $E_{capture/emission}$. One parabola represents the neutral state, the second one the charged state. For the transition from one state to another, a certain capture or emission barrier has to be overcome [7, 8].

Parameter	Defect Band	Defect Band shifted
$E_T \pm \sigma$ [eV]	1.73±0.3*	2.18±0.3
$S \pm \sigma$ [eV]	4.93±1.95	4.93±1.95
R [1]	0.44	0.44
N_T [cm ⁻³]	3.44×10 ¹⁹	3.44×10 ¹⁹

Table 1: Exemplary electron defect bands used for the qualitative Comphy simulations, with the mean trap energy E_T , the relaxation energy S , the ratio of the curvatures R , the trap density N_T of the two-state NMP model. The original trap band was taken from Schleich *et al.* [24] ($*E_T \pm \sigma = 1.73 \pm 0.16$) and represents slow traps, extracted on lateral MOSFETs. The trap energy was broadened in order to get higher drifts.

were shorted, and the source (S) terminal grounded. A current of $I_D=1$ mA was forced, and the resulting gate voltage V_G measured. This measurement configuration allows us to measure a threshold voltage easily and directly using a current criterion. After each stress and readout sequence, the stress time is increased. The results presented here always show the cumulated stress times.

C. Mathematical Description of BTI

For lifetime predictions, BTI can be expressed by either an empirical power law or exponential model [9]. Both mathematical attempts lack a physical background, and generally result in an overestimation of the drift, as they do not account for saturation of the degradation [6, 21]. In industry, the power-law description is more commonly used, especially to predict end-of-lifetime drifts. The time-evolution model predicts the drift dependence on the total stress time [9] as

$$\Delta V_{th}(V_G, t) = A(V_{G,ref}, t_{ref}) \cdot \left(\frac{t}{t_{ref}}\right)^n \quad (1)$$

with the stress time t , the reference time t_{ref} , a prefactor A depending on the point of reference (i.e. the measured drift after

a certain stress duration with a fixed gate voltage), the threshold voltage shift ΔV_{th} and the time evolution exponent n . The same approach can be used to find an estimate for the drift caused by different stress biases. The power-law voltage acceleration model is given as [9]

$$\Delta V_{th}(V_G) = A(V_{G,ref}, t_{ref}) \cdot \left(\frac{V_G}{V_{G,ref}}\right)^m \quad (2)$$

with the power-law acceleration factor m , the gate voltage V_G and the reference gate voltage $V_{G,ref}$. Both power-law models are not based on any physical models. Therefore, effects like saturation of the drift, which can be observed in the experiments especially for long stress times, are not considered in these purely empirical models.

A more physical approach to describe BTI is to consider the observed experimental behavior as the tail of a Gaussian or logistic distribution of the activation energy of the trap [22]. Neglecting recovery effects, the simpler thermal activation model can be derived [22] as

$$\Delta V_{th} = \frac{\Delta V_{th,max}}{2} \operatorname{erfc}\left(\frac{E_a - k_B T \log\left(\frac{t_s}{\tau_0}\right)}{\sqrt{2}\sigma}\right) \quad (3)$$

with the Boltzmann constant k_B , the temperature T at which the measurement was performed, the stress time t_s , an inverse attempt frequency τ_0 and the width σ of the Gaussian trap distribution. E_a describes the mean effective activation energy of the Gaussian trap distribution, and basically represents the energy barrier, which needs to be overcome to either change the charge state in the 2-state non-radiative multi-phonon (NMP) model (cf. $E_{capture}$ Figure 2) or that of any other first-order chemical reaction [22]. Note that this model is only a simplified description, and therefore limited in its accuracy, as it only has four data-fit parameters (E_a , σ , τ_0 , and $\Delta V_{th,max}$).

Measurement data of the tested devices were fitted with the power law voltage and time acceleration models, and the power law exponents compared to each other. Additionally, measurements with temperature variations were used to extract

the end-of-lifetime drift using the simple thermal activation model given in Equation (3). Unlike the widely used power-law approach, this model considers saturation effects, and therefore gives more accurate drift estimations especially for long timescales.

D. Compact Physics Framework

We used the 1D reliability simulator Comphy [7, 23] in order to explain the differences and similarities in BTI of SiC and Si devices. Comphy uses an effective 2-state NMP model (Figure 2) to calculate transient shifts of the threshold voltage based on charge capture and emission in a given set of pre-existing oxide traps (trap bands). Based on the work of Schleich *et al.* [24] for lateral SiC MOSFETs, we calibrated the electrostatics to our trench technology. We calculated the resulting BTI degradation (MSM sequence) using electron traps only in relation to the relative position of conduction band versus traps, while keeping all other parameters untouched. To do so, we carefully calibrated our simulation environment starting with trap parameters from the literature [24] with a slightly broadened trap-energy distribution. Second, we repeated the simulation using the same trap properties but with the mean trap energy shifted upwards by 0.45 eV (to emulate the conduction band offset between SiC and Si, Table 1). Thus, we ensure the same active energy region for both setups for all positions of the surface potential. We focus on the slow trap band, as this trap band is expected to dominate our experimental results using preconditioning. Even though this is only a qualitative calculation, it provides valuable information for a qualitative study of the impact of the conduction band offset between SiC and Si. The stress bias and temperature were varied, and the readout level in the simulation was selected as 4 V, which is close to the readout level in the experiments. The drift is extracted after 1 s.

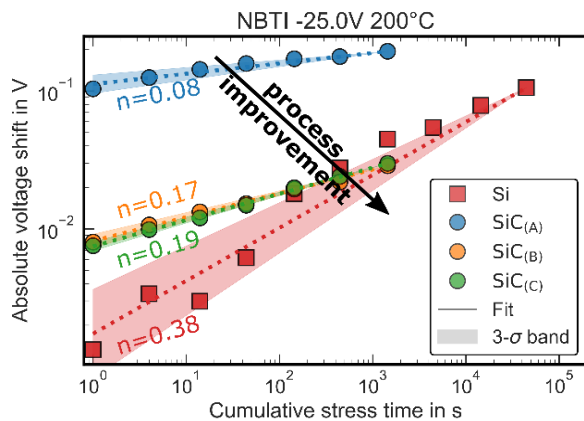


Figure 3: Absolute NBTI threshold voltage shift vs. cumulative stress time for a -25 V stress at 200°C . SiC_(A) (blue) shows the highest drift level. For SiC_(B) and SiC_(C) (orange, green), the drift is significantly lower and in the same range as for the Si MOSFET (red) due to process improvements. Note that due to preconditioning, mostly the contribution of the slow traps is monitored.

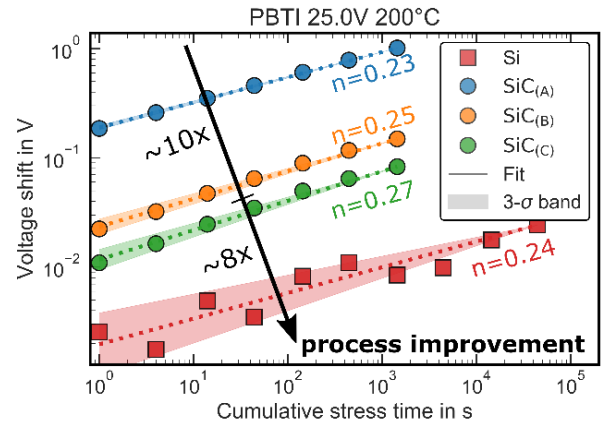


Figure 4: PBTI threshold voltage shift vs. cumulative stress time. The measurement data were fitted with an empirical power law and the power law exponent n determined. SiC and Si devices show similar time evolution. For SiC, adjustments in device processing can significantly reduce the PBTI drift so that even lower drifts appear obtainable for further improvements.

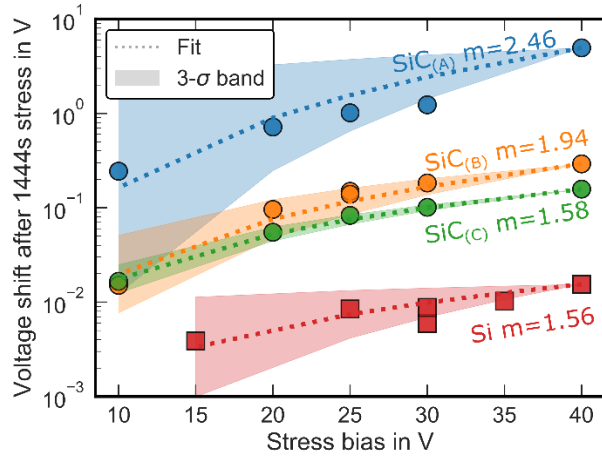


Figure 5: Threshold voltage shift for various stress biases measured after 1.4 ks of PBTI stress at 200°C. The circles represent the measurement data, the dotted line the power-law fit to the voltage acceleration model with the power-law acceleration factor m . Both technologies show comparable power-law acceleration factors indicating a similar origin.

III. RESULTS AND DISCUSSION

First, the threshold voltage shifts over time caused by positive and negative BTI (PBTI/NBTI) at 200°C with ± 25 V were studied. Figure 3 shows the NBTI drift of the tested devices. For NBTI, drifts in the 10 mV range are observed for the SiC samples with optimized processing conditions in contrast to older literature [2], where drifts >1 V were presented after a few hours of stress. The highest NBTI drift is observed for SiC_(A). This drift has been significantly improved by process optimizations resulting in final drifts in a similar range as the tested Si power MOSFETs. Additionally, the measurements were fitted with the power-law time evolution model presented above. The resulting power-law exponents shown in Figure 3 are significantly lower for the SiC devices than for Si. This means that for long stress times, an even lower drift can be expected for SiC_(B) and SiC_(C) than for the Si MOSFET. In total, NBTI in SiC devices can be reduced at least to a similar level as for Si by optimizing device processing. In SiC_(B) and SiC_(C), NBTI has been reduced to very low levels.

Figure 4 shows the PBTI threshold voltage drift of the tested devices at 200°C. Despite the different substrate materials, the SiC and Si curves are mainly shifted in parallel along the voltage drift axis, i.e. showing the same time evolution. As was the case for NBTI, a strong improvement in the drift can be achieved by optimizing the POA conditions confirming the findings in [16]. An improvement was achieved between SiC_(A) and SiC_(B) or SiC_(C) by about a factor of 10. Even though the total drift of the best SiC process variants in this split experiment is still around 8 times higher than for the Si MOSFET, we are optimistic that even lower drifts might be achievable by further process optimization.

When extracting the power-law coefficients for the time evolution, power-law coefficients in the range 0.23 to 0.27 are obtained for the quasi-permanent drift component. This is in the typical range for Si devices ($0.1 < n < 0.25$) [9]. As we will show

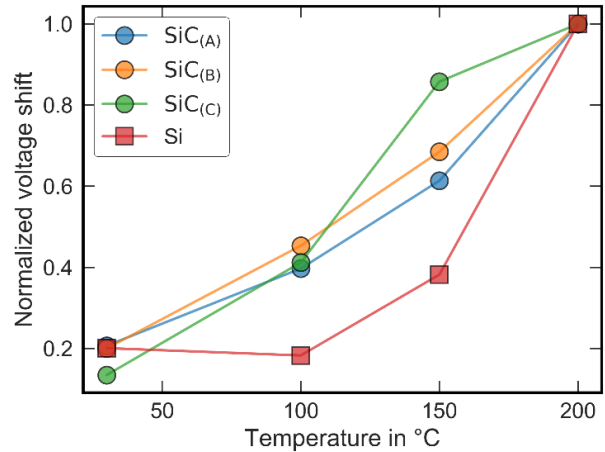


Figure 6: Normalized temperature-dependent threshold voltage drift for a PBTI stress with 25 V. SiC devices were stress 1.4 ks and Si devices 44 ks; the drift values were normalized to the drift at 200°C. All SiC test structures show a similar temperature dependence, whereas Si shows a slightly different one. However, this could be related to larger uncertainties caused by the lower absolute voltage drift.

in the following subsections, SiC and Si show a similar dependence on PBTI stress parameters such as stress time, stress bias and temperature. Therefore, PBTI in both technologies very likely has the same origin. It has previously been speculated [24, 25] that both technologies interact with the same intrinsic SiO₂ trap [26] close to the conduction band edge of Si and SiC. The slightly higher conduction band minimum of SiC by 0.45eV facilitates interaction of these traps with minority carriers in the channel. In addition, we expect different trap densities in SiC compared to Si as well as in the different SiC samples because of the different processing conditions.

To further test the hypothesis that BTI in SiC and Si is caused by the same electron trap in SiO₂, the dependence on the stress voltage was investigated. Figure 5 shows the stress bias

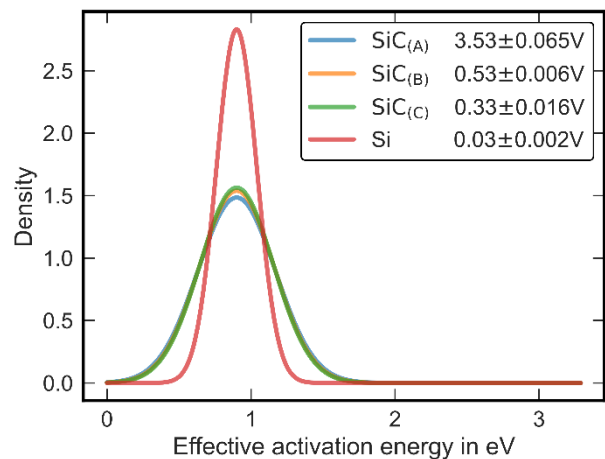


Figure 7: Normal distribution of the effective activation energy of the electron traps responsible for PBTI, extracted with the simple thermal activation model using measurements at different temperatures. SiC samples were stressed with 25 V and Si samples with 40 V in order to get higher drifts for better fitting. For fitting, $E_a=0.9$ eV was assumed for both SiC and Si and the maximum drift values extracted (see legend).

dependence of PBTI measured at 200°C. Again, PBTI drifts for SiC and Si show a similar dependence on stress voltage, especially for $V_{GS} \geq 20$ V. As described in section II, measurement data were fitted with the power-law voltage acceleration model (Equation (2)) and the power-law exponents m extracted. Considering fitting errors, all test structures show comparable power-law coefficients of around 1.5 to 2.5. Because of the stronger band bending at higher stress biases, energetically higher traps in the oxide become accessible for trapping. The observed similarity is an additional indicator that BTI in SiC and Si is due to traps at the same trap level.

Furthermore, the temperature dependence of the PBTI drift was studied. Figure 6 shows the temperature dependence of PBTI after a cumulative stress time of 1.4 ks for SiC devices and 44 ks for Si devices with 25 V stress bias, respectively. For Si, longer stress times were chosen in order to obtain larger and therefore better measurable drifts. For better comparison, also with regard to the longer stress time of the Si devices, the drifts were normalized to the drift value at 200°C. All SiC devices show nearly the same temperature dependence, which results in a higher drift at higher temperatures. The Si device behaves a bit differently. Interestingly, at 30°C, SiC and Si MOSFETs both show 15-20% of the shift at 200°C. Between 30°C and 200°C, a slightly slower increase in drift is observed with elevated temperatures for the Si test structures. Because of the overall very low PBTI drift in the tested Si MOSFETs, the small difference between SiC and Si can very likely be caused by uncertainties in the measurement or the larger stress time. Therefore, we conclude that a similar temperature dependence was found for SiC and Si power MOSFETs within the limits of measurement accuracy, which further supports the hypothesis that the same trap levels are responsible for BTI in SiC and Si devices.

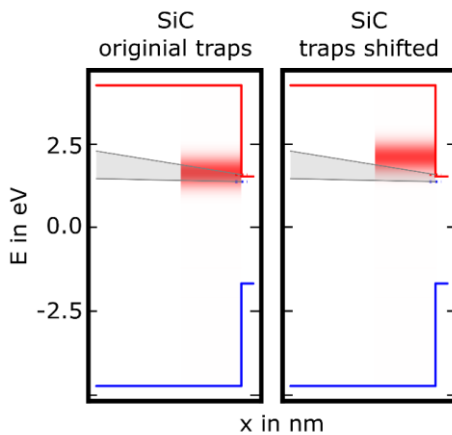


Figure 8: Band diagrams of the simulated trap bands (red shaded area) from Table 1 for a SiC material system. The left diagram shows the real SiC/SiO₂ and trap band configuration. The right diagram shows a configuration with shifted trap bands for studying the impact of the location of the conduction band minimum on PBTI drift with otherwise identical material parameters, thereby mimicking the different band offsets between SiC and Si. The grey-shaded area represents the active energy window from which the measured charges result for a 40 V PBTI stress (upper grey line) and readout at 4 V (lower grey line).

In order to correlate the measurement results with a physical model, the simple thermal activation model as suggested in [22] was used. As described in the previous section, this model is based on the assumption of a normal distribution of the activation energy with a mean activation energy E_a and a standard deviation σ . Since the experiments presented so far indicate that PBTI in SiC and Si is likely due to the same defect level, we assumed a fixed mean activation energy of 0.9 eV for both material types. Next, we extracted the trap distribution of the measurements at various temperatures using Equation (3) (Figure 7) with satisfying fitting results. Note that for Si, a higher stress bias had to be chosen in order to receive larger drifts for more accurate fitting. With this model, the maximum voltage shift, i.e. the drift saturation when all traps are filled, can be extracted. Thus, more reliable drift values can be obtained with the simple thermal activation model compared to the conventional power-law extraction, which can lead to an overestimation of drifts. The maximum voltage shift extracted when all available trap levels are filled is expected to be around 30 mV for the Si MOSFETs and 330 mV for the best SiC test structure (SiC_(C)) (see inset of Figure 7). The fact that both SiC and Si can be conveniently fitted using the same activation energy strongly supports the hypothesis that BTI in both technologies is likely related to the same traps [24]. On the one hand, the higher conduction band minimum in SiC compared to Si facilitates trapping in bands of higher energy, and on the other hand, the filling of more traps of the same trap band.

In order to test the hypothesis in more detail, we simulated a BTI MSM sequence with various stress biases and temperatures in Comphy, using the trap bands presented in the previous section (Table 1). As was already suggested in [24, 25], PBTI in SiC and Si is caused by the same intrinsic traps in SiO₂. The different drifts might be due to the conduction band offset between SiC and Si. In the simulations, the same

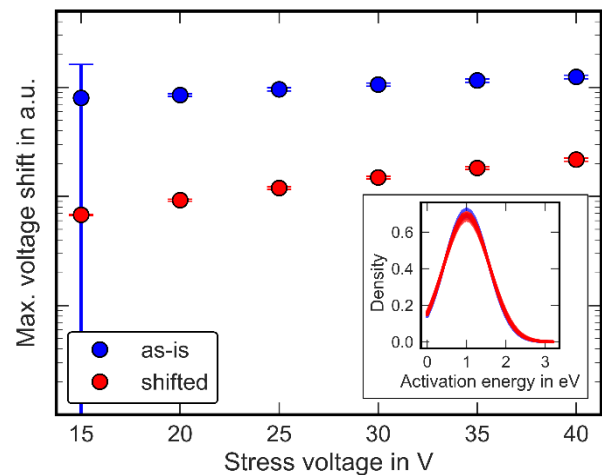


Figure 9: Maximum voltage shift extracted with the thermal activation model in relation to the PBTI stress bias of a simulated BTI MSM sequence. PBTI drifts of SiC with the regular trap band position (as-is) and an up-shifted (shifted) trap band were simulated with Comphy. The simulated data were then fitted with the simple thermal activation model. The maximum drift was extracted using a fixed mean activation energy of 1 eV for the Gaussian trap distribution for both variants (see inset). For the presented set of simulation parameters (trap band, stress voltage and time), the voltage dependence of E_a is negligible.

temperatures and voltages as in the experiments were studied. First, the PBTI threshold voltage drift over time for SiC devices with the regular position of the trap bands was simulated. In a second step, only the position of the trap band was shifted by 0.45 eV, which equals the conduction band offset between SiC and Si ($\Delta E_C = E_{C,SiC} - E_{C,Si} = 0.45$ eV), and the PBTI drift was simulated again. The resulting band structures including the exemplary trap bands and the active energy window for the highest simulated stress bias (40 V) can be found in Figure 8. In our simulation, the active energy window of the setup with the higher trap energy representing Si covers only a smaller share of the same trap distribution in comparison to SiC. Next, the simulated drifts for both configurations were fitted to the simple thermal activation model, as was done with the experimental data presented in the previous section, to investigate the impact of the conduction band offset on the maximum BTI drift. Consistent with the experiments' results, the simulated drifts can also be fitted with a fixed activation energy, which is 1 eV for the simulated trap distribution. This activation energy depends only marginally on the stress bias, so that the same E_a could be used for all combinations of simulated stress parameters, in agreement with the previous results on Si [21]. In general, we observed that small changes in the activation energy only change the fit insignificantly. Hence, more detailed investigations on this topic with experimental results are needed.

Figure 9 shows the maximum voltage drift extracted with Equation (3) for the simulated stress sequence using SiC band parameters and the regular and shifted trap bands. For the simulated trap bands, the shift of the conduction band edge by 0.45 eV leads to a significant reduction of the maximum drift, which is consistent with the experiments. As can be seen in Figure 8, the active energy window of the setup with the shifted trap band covers only the lower tail of the Gaussian trap distribution, therefore leading to lower drifts. This result strongly supports the hypothesis that BTI in SiC and Si is caused by the same defects [24]. The higher conduction band edge of SiC enables trapping in a larger fraction of the trap distribution compared to silicon, explaining the overall larger drift. We recall that higher trap densities are expected for SiC MOS structures because of a less efficient interface passivation in SiC/SiO₂ compared to Si/SiO₂. Nevertheless, device processing is continuously improved, leading to a reduction of the total trap density, and therefore to lower drifts. Thus with the current state of knowledge, the conduction band offset between SiC and Si can consistently explain the higher PBTI drift in the SiC test structures compared to silicon, supporting the findings from [24].

IV. CONCLUSION

A comparison of BTI in Si and SiC power MOSFETs was presented. With regard to NBTI, the presented process variants SiC_(B) and SiC_(C) can compete with Si power MOSFETs. Here, drifts of the same magnitude were measured. For PBTI it was found that SiC and Si follow very similar dependencies on stress time, stress bias and temperature. The different test structures mainly differ in the magnitude of the threshold voltage drift. The drift dynamics as well as voltage and

temperature acceleration can be described using the same empirical and simple physical models as developed for Si MOSFETs. Furthermore, qualitative simulations on the impact of the position of the conduction band minimum on the PBTI drift were presented. Both the experiment results and the simulations indicate that BTI in SiC and Si is caused by the same intrinsic SiO₂ trap located close to the SiC conduction band. Whereas the active energy region of Si devices covers only the lower tail of the trap distribution, the significantly higher conduction band minimum of SiC enables the filling of more traps of the same distribution, resulting in a higher total drift compared to Si. Additionally, different trap densities are expected depending on the efficiency of the interface passivation process.

Finally, we presented BTI results of differently processed SiC test structures. We showed that process optimization, in this case, more efficient interface passivation, can significantly reduce BTI. As an example we presented a reduction of PBTI drifts by a factor of 10 between the worst and the best process variant as well as NBTI comparable to Si MOSFETs.

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